Universidad Zaragoza
1542

Trabajo Fin de Grado

Anexos

Autor

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Director/es

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Escuela de ingeniería y arquitectura

Curso 2016/2017

Contenido

1.Filtro 10kHZ

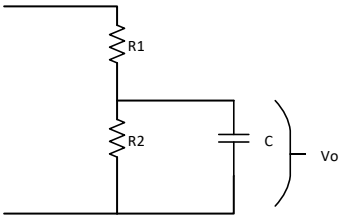


Fig.1 Filtro Paso bajo

$$V_{out} = \left|\frac{R_2 \parallel X_C}{R_1 + R_2 \parallel X_C}\right| = \frac{-jR_2 \cdot \frac{1}{\omega_C}}{R_2 - j\frac{1}{\omega C}} = j\frac{R_2}{j - \omega C R_2}$$

$$V_{out} = \frac{j\frac{R_2}{j - \omega C R_2}}{R_1 + \frac{R_2}{j - \omega C R_2}} = \frac{jR_2}{jR_1 - \omega C R_1 R_2 + jR_2} = \frac{-R_2}{-R_1 - R_2 - j\omega C R_1 R_2}$$

$$|V_{out}| = \frac{R_2}{\sqrt{(R_1 + R_2)^2 + (\omega C R_1 R_2)^2}} \xrightarrow{\omega \to 0} \frac{R_2}{R_1 + R_2}$$

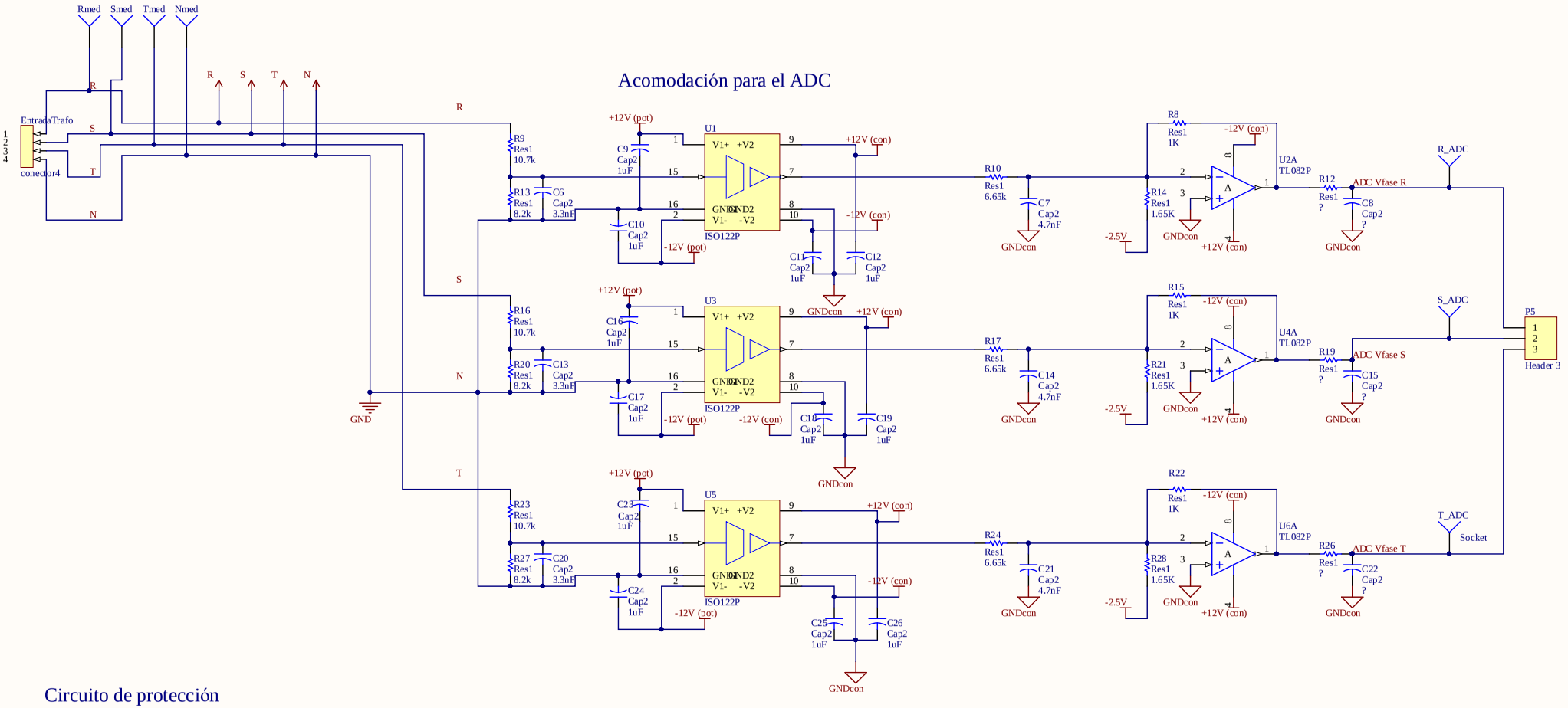
Como la frecuencia de corte es el 0.7 *del valor total*:

$$0.7\frac{R_2}{R_2 + R_1} = \frac{R_2}{\sqrt{(R_1 + R_2)^2 + (\omega C R_1 R_2)^2}} \rightarrow \frac{0.7^2}{(R_1 + R_2)^2} = \frac{1}{\omega^2 C^2 R_1^2 R_2^2 + (R_1 + R_2)^2}$$

$$C^2 = \frac{(R_1 + R_2)^2 - 0.7^2(R_1 + R_2)^2}{0.49\omega^2 R_1^2 R_2^2} = \frac{0.51(R_1 - R_2)^2}{0.49\ \omega^2 R_1^2 R_2^2} = \frac{\sqrt{0.51}}{0.7}\frac{R_1 + R_2}{R_1 R_2 \omega}$$

$$= 1.0202\frac{R_1 + R_2}{R_1 R_2 \omega} \approx \frac{R_1 + R_2}{R_1 R_2 \omega}$$

2. Esquema General



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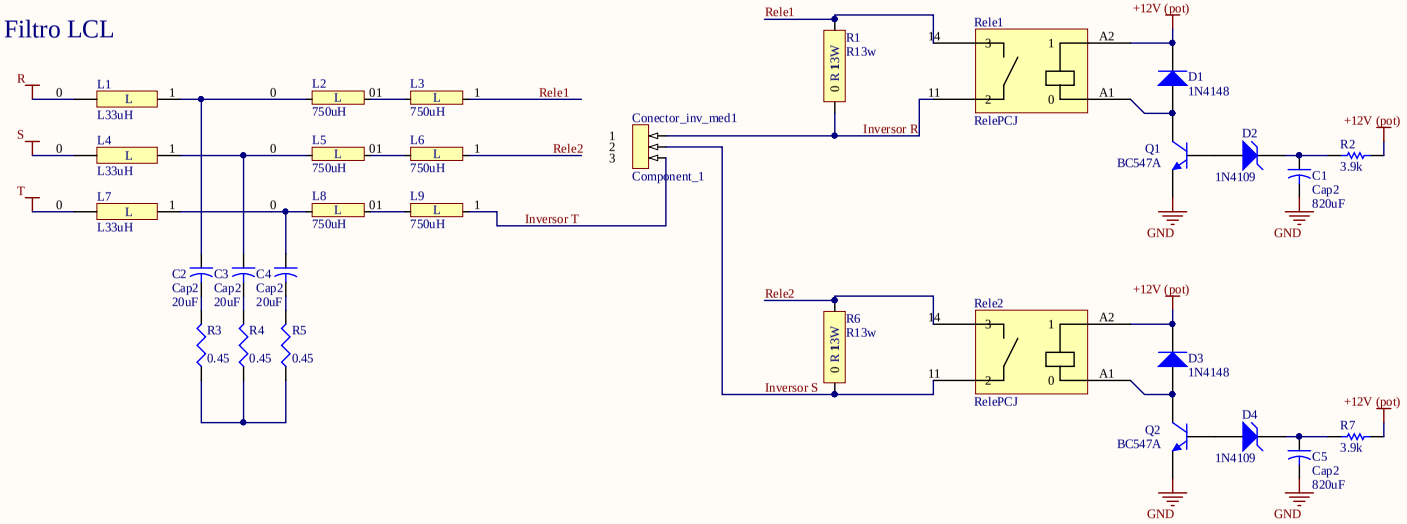
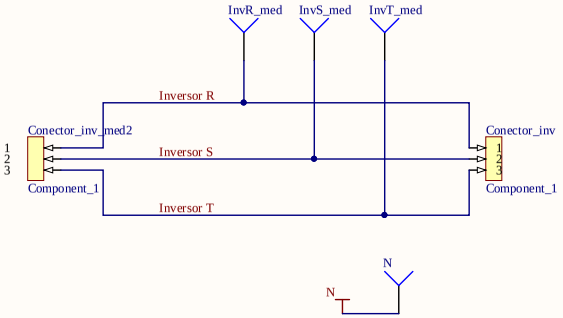
Size: A3	Number: 1	Revision:
Date: 19/06/2017	Sheet of	
File: Sheet1.SchDoc	Drawn By: Jesús Aybar	

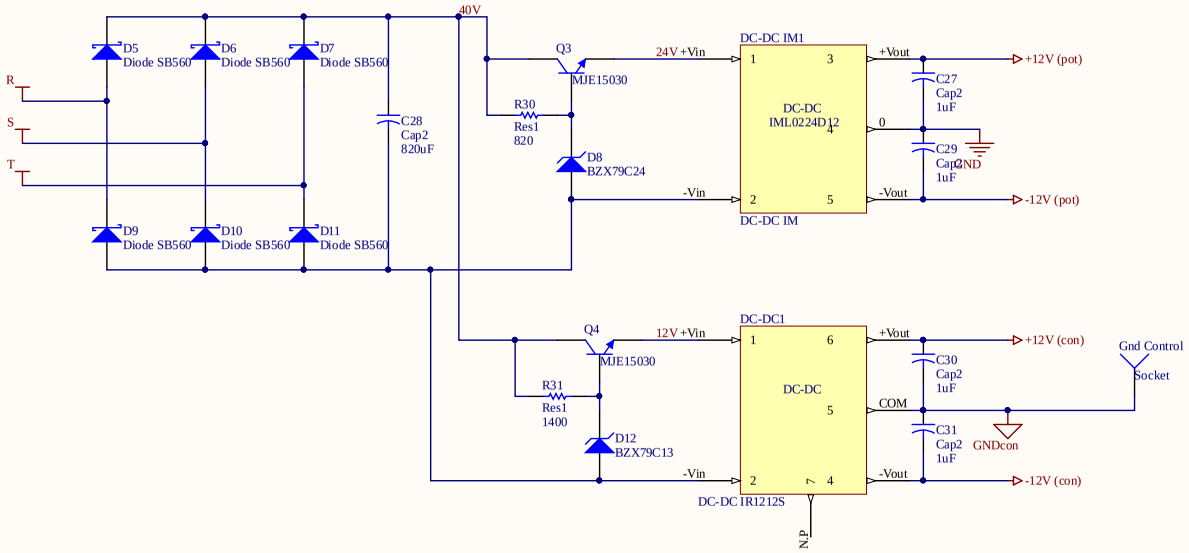
Filtro LCL



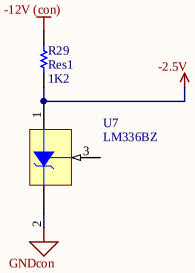
Conexión Inversor



Rectificador trifásico con conversor a +-12V



Regulador de -2.5V



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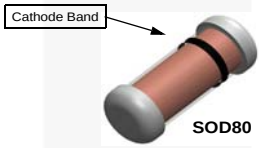
Size: A3	Number: 2	Revision:
Date: 19/06/2017		Sheet of
File: Sheet2.SchDoc		Drawn By: Jesús Aybar

3.Datasheet

June 2015

1N/FDLL 914/A/B / 916/A/B / 4148 / 4448
Small Signal Diode

DO-35
Cathode is denoted with a black band



LL-34
THE PLACEMENT OF THE EXPANSION GAP HAS NO RELATIONSHIP TO THE LOCATION OF THE CATHODE TERMINAL

SOD-80 COLOR BAND MARKING

DEVICE	1ST BAND
FDLL914	BLACK
FDLL914A	BLACK
FDLL914B	BLACK
FDLL4148	BLACK
FDLL4448	BLACK

-1st band denotes cathode terminal and has wider width

Ordering Information

Part Number	Marking	Package	Packing Method
1N914	914	DO-204AH (DO-35)	Bulk
1N914_T50A	914	DO-204AH (DO-35)	Ammo
1N914TR	914	DO-204AH (DO-35)	Tape and Reel
1N914ATR	914A	DO-204AH (DO-35)	Tape and Reel
1N914B	914B	DO-204AH (DO-35)	Bulk
1N914BTR	914B	DO-204AH (DO-35)	Tape and Reel
1N916	916	DO-204AH (DO-35)	Bulk
1N916A	916A	DO-204AH (DO-35)	Bulk
1N916B	916B	DO-204AH (DO-35)	Bulk
1N4148	4148	DO-204AH (DO-35)	Bulk
1N4148TA	4148	DO-204AH (DO-35)	Ammo
1N4148_T26A	4148	DO-204AH (DO-35)	Ammo
1N4148_T50A	4148	DO-204AH (DO-35)	Ammo
1N4148TR	4148	DO-204AH (DO-35)	Tape and Reel
1N4148_T50R	4148	DO-204AH (DO-35)	Tape and Reel
1N4448	4448	DO-204AH (DO-35)	Bulk
1N4448TR	4448	DO-204AH (DO-35)	Tape and Reel
FDLL914	Black	SOD-80	Tape and Reel
FDLL914A	Black	SOD-80	Tape and Reel
FDLL914B	Black	SOD-80	Tape and Reel
FDLL4148	Black	SOD-80	Tape and Reel
FDLL4148_D87Z	Black	SOD-80	Tape and Reel
FDLL4448	Black	SOD-80	Tape and Reel
FDLL4448_D87Z	Black	SOD-80	Tape and Reel

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{RRM}	Maximum Repetitive Reverse Voltage		100	V
I_O	Average Rectified Forward Current		200	mA
I_F	DC Forward Current		300	mA
I_f	Recurrent Peak Forward Current		400	mA
I_{FSM}	Non-repetitive Peak Forward Surge Current	Pulse Width = 1.0 s	1.0	A
		Pulse Width = 1.0 µs	4.0	A
T_{STG}	Storage Temperature Range		-65 to +200	°C
T_J	Operating Junction Temperature Range		-55 to +175	°C

Note:

1. These ratings are limiting values above which the serviceability of the diode may be impaired.

Thermal Characteristics

Symbol	Parameter	Max.	Unit
		1N/FDLL 914/A/B / 916/A/B / 4148 / 4448	
P_D	Power Dissipation	500	mW
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	300	°C/W

Electrical Characteristics(2)

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Max.	Unit
V_R	Breakdown Voltage		I_R= 100 µA	100		V
			I_R= 5.0 µA	75		V
V_F	Forward Voltage	914B / 4448	I_F= 5.0 mA	0.62	0.72	V
		916B	I_F= 5.0 mA	0.63	0.73	V
		914 / 916 / 4148	I_F= 10 mA		1.0	V
		914A / 916A	I_F= 20 mA		1.0	V
		916B	I_F= 20 mA		1.0	V
		914B / 4448	I_F= 100 mA		1.0	V
I_R	Reverse Leakage		V_R= 20 V		0.025	µA
			V_R= 20 V, T_A= 150°C		50	µA
			V_R= 75 V		5.0	µA
C_T	Total Capacitance	916/916A/916B/4448	V_R = 0, f = 1.0 MHz		2.0	pF
		914/914A/914B/4148	V_R = 0, f = 1.0 MHz		4.0	pF
t_{rr}	Reverse Recovery Time		I_F = 10 mA, V_R = 6.0 V (600 mA) I_{rr} = 1.0 mA, R_L = 100 Ω		4.0	ns

Note:

2. Non-recurrent square wave P_W= 8.3 ms.

Typical Performance Characteristics

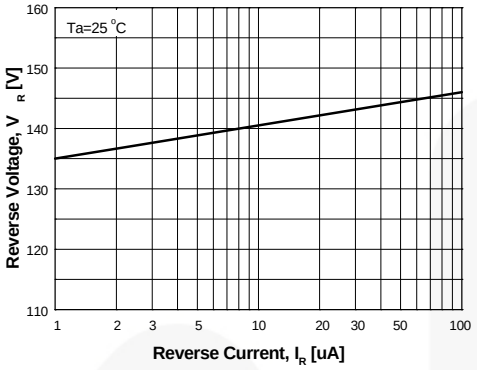


Figure 1. Reverse Voltage vs. Reverse Current
B_V - 1.0 to 100 µA

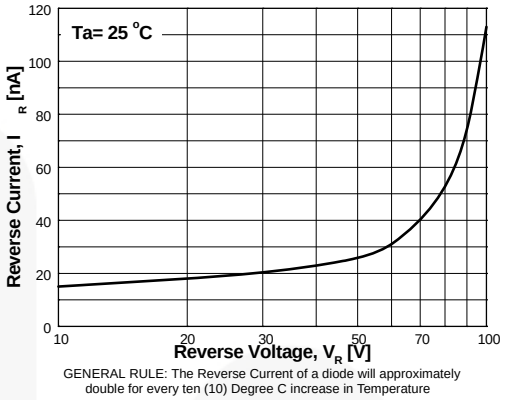


Figure 2. Reverse Current vs. Reverse Voltage
I_R - 10 to 100 V

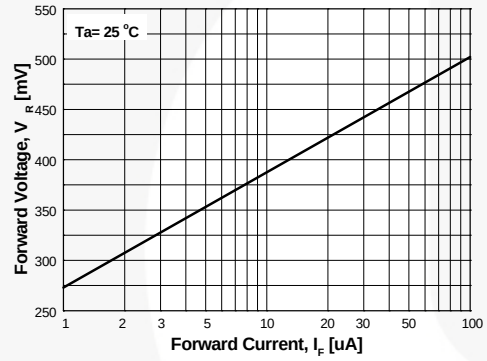


Figure 3. Forward Voltage vs. Forward Current
V_F - 1 to 100 µA

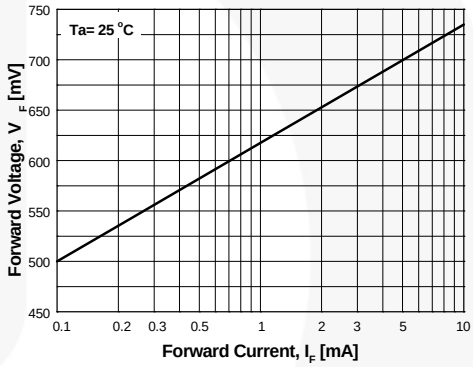


Figure 4. Forward Voltage vs. Forward Current
V_F - 0.1 to 10 mA

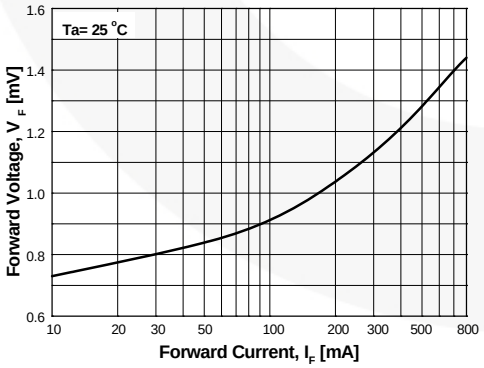


Figure 5. Forward Voltage vs. Forward Current
V_F - 10 to 800 mA

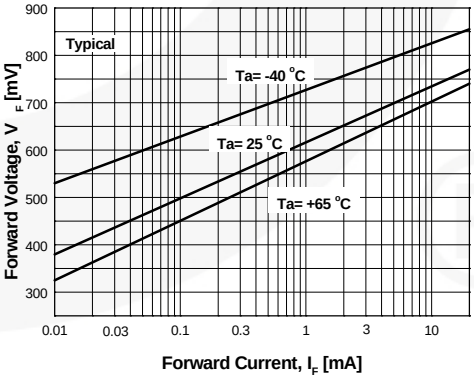


Figure 6. Forward Voltage vs. Ambient Temperature
V_F - 0.01 - 20 mA (- 40 to +65°C)

Typical Performance Characteristics (Continued)

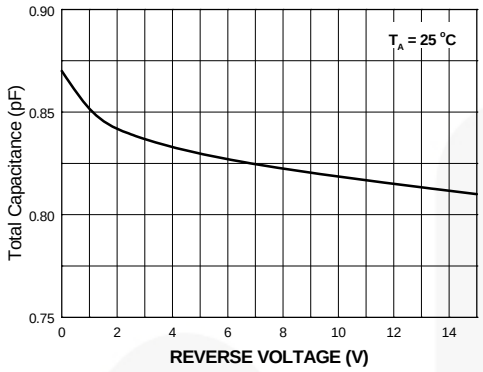


Figure 7. Total Capacitance

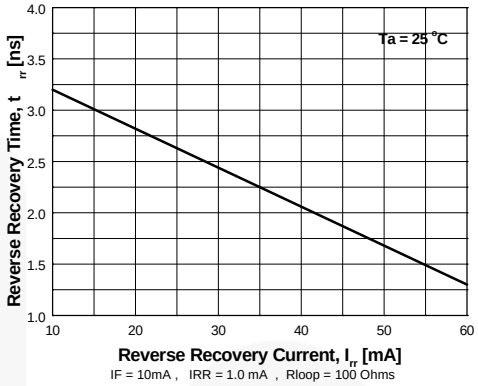


Figure 8. Reverse Recovery Time vs. Reverse Recovery Current

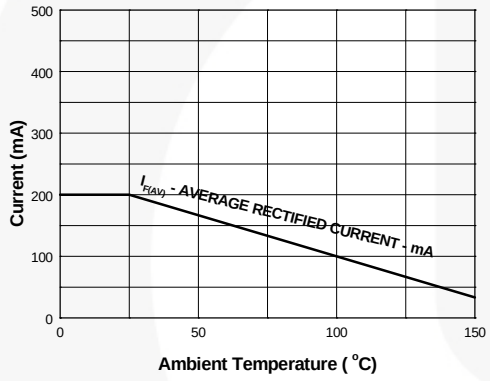


Figure 9. Average Rectified Current ($I_{F(AV)}$) vs. Ambient Temperature (T_A)

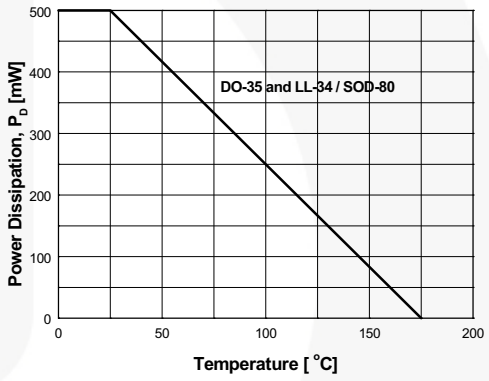


Figure 10. Power Derating Curve

Physical Dimensions

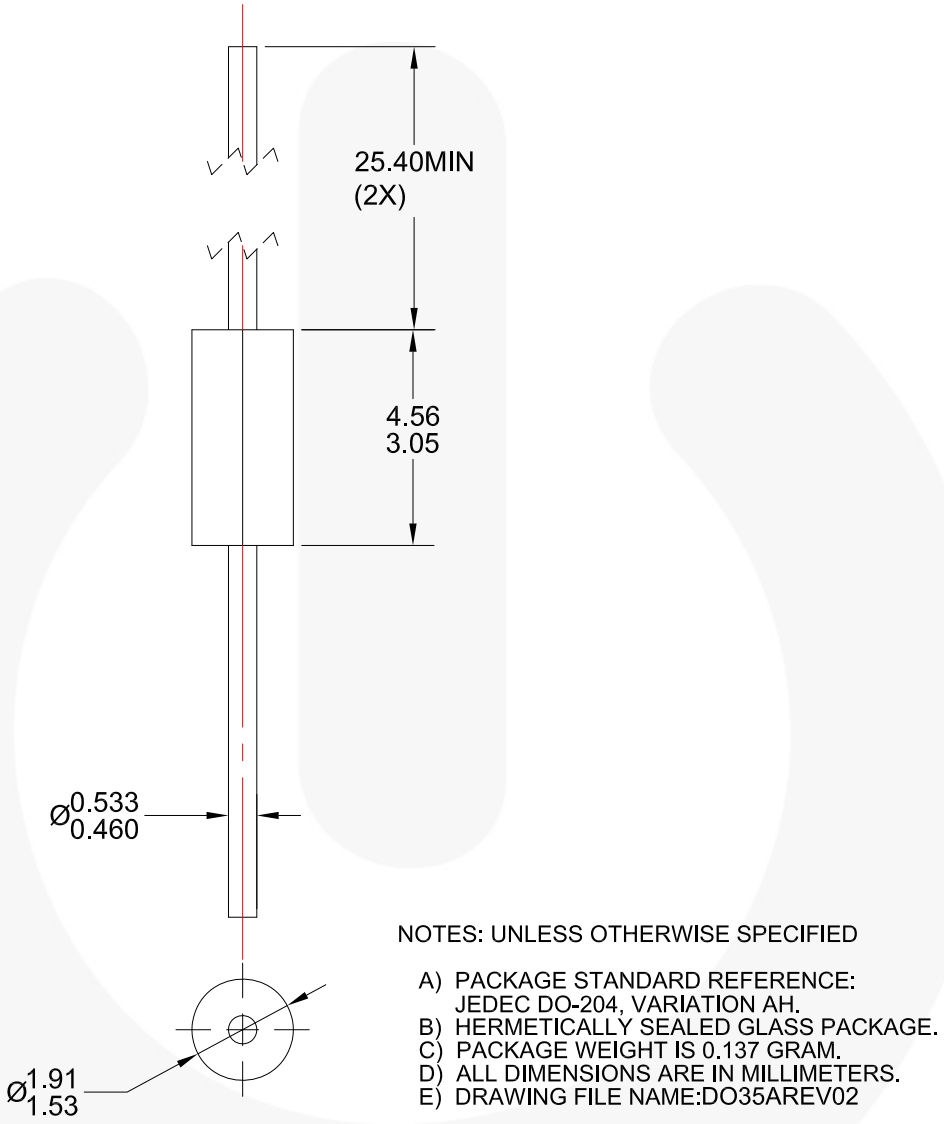
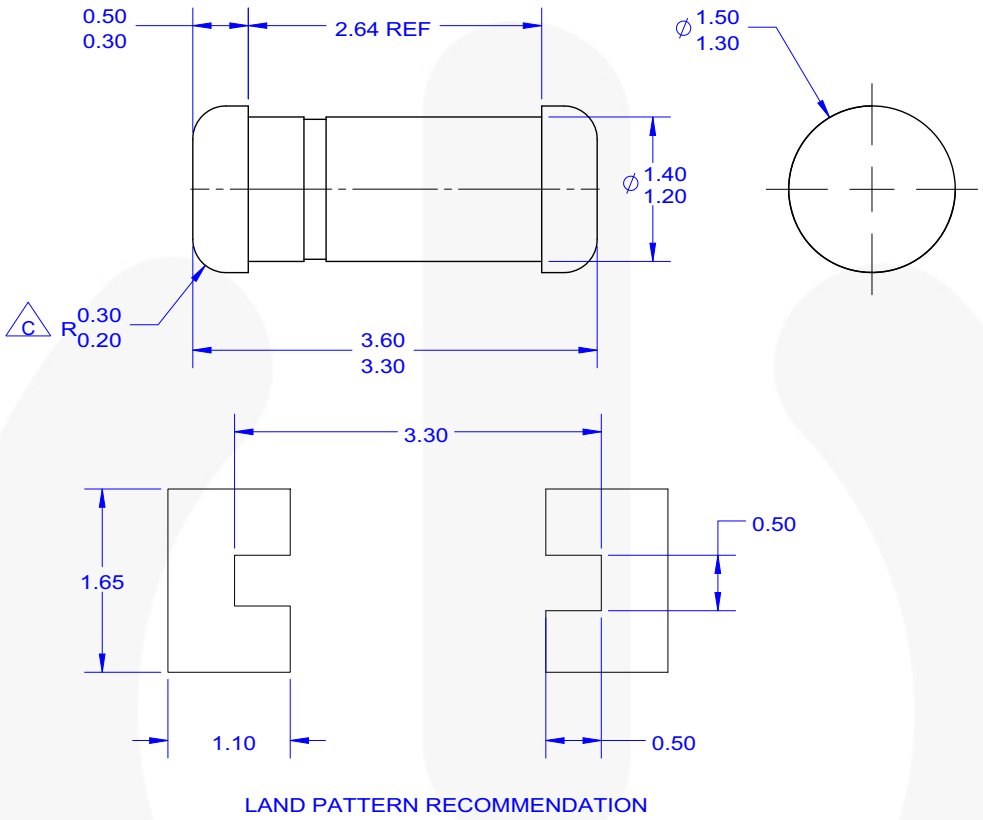


Figure 11. AXIAL LEADED, GLASS, JEDEC DO204, VARIATION AH, DO-204AH (DO-35)

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE:
JEDEC DO-213, VARIATION AC.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C CORNER RADIUS IS OPTIONAL.

D) LAND PATTERN RECOMMENDATION PER IPC DIOMELF3414N

E) DRAWING FILE NAME: SOD80A REV3

Figure 12. 2-TERMINAL, SOD-80, JEDEC DO-213AC, MINI-MELF

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I74

FAIRCHILD SEMICONDUCTOR®

July 2013

1N5221B - 1N5263B
Zener Diodes

Tolerance = 5%

DO-35 Glass case
COLOR BAND DENOTES CATHODE

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Units
P_D	Power Dissipation	500	mW
	Derate above 50°C	4.0	mW°C
T_{STG}	Storage Temperature Range	-65 to +200	°C
T_J	Operating Junction Temperature Range	-65 to +200	°C
	Lead Temperature (1/16 inch from case for 10 s)	+230	°C

Note:

1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
   Non-recurrent square wave Pulse Width = 8.3 ms, T_A = 50°C

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted .

Device	V_Z (V) @ I_Z (2)			Z_Z (Ω) @ I_Z (mA)		Z_{ZK} (Ω) @ I_{ZK}(mA)		I_R (μA) @ V_R (V)		T_C (%/°C)
	Min.	Typ.	Max.							
1N5221B	2.28	2.4	2.52	30	20	1,200	0.25	100	1.0	-0.085
1N5222B	2.375	2.5	2.625	30	20	1,250	0.25	100	1.0	-0.085
1N5223B	2.565	2.7	2.835	30	20	1,300	0.25	75	1.0	-0.080
1N5224B	2.66	2.8	2.94	30	20	1,400	0.25	75	1.0	-0.080
1N5225B	2.85	3	3.15	29	20	1,600	0.25	50	1.0	-0.075
1N5226B	3.135	3.3	3.465	28	20	1,600	0.25	25	1.0	-0.07
1N5227B	3.42	3.6	3.78	24	20	1,700	0.25	15	1.0	-0.065
1N5228B	3.705	3.9	4.095	23	20	1,900	0.25	10	1.0	-0.06
1N5229B	4.085	4.3	4.515	22	20	2,000	0.25	5.0	1.0	+/-0.055
1N5230B	4.465	4.7	4.935	19	20	1,900	0.25	2.0	1.0	+/-0.03
1N5231B	4.845	5.1	5.355	17	20	1,600	0.25	5.0	2.0	+/-0.03
1N5232B	5.32	5.6	5.88	11	20	1,600	0.25	5.0	3.0	0.038
1N5233B	5.7	6	6.3	7.0	20	1,600	0.25	5.0	3.5	0.038
1N5234B	5.89	6.2	6.51	7.0	20	1,000	0.25	5.0	4.0	0.045
1N5235B	6.46	6.8	7.14	5.0	20	750	0.25	3.0	5.0	0.05
1N5236B	7.125	7.5	7.875	6.0	20	500	0.25	3.0	6.0	0.058
1N5237B	7.79	8.2	8.61	8.0	20	500	0.25	3.0	6.5	0.062
1N5238B	8.265	8.7	9.135	8.0	20	600	0.25	3.0	6.5	0.065
1N5239B	8.645	9.1	9.555	10	20	600	0.25	3.0	7.0	0.068
1N5240B	9.5	10	10.5	17	20	600	0.25	3.0	8.0	0.075
1N5241B	10.45	11	11.55	22	20	600	0.25	2.0	8.4	0.076
1N5242B	11.4	12	12.6	30	20	600	0.25	1.0	9.1	0.077
1N5243B	12.35	13	13.65	13	9.5	600	0.25	0.5	9.9	0.079
1N5244B	13.3	14	14.7	15	9.0	600	0.25	0.1	10	0.080
1N5245B	14.25	15	15.75	16	8.5	600	0.25	0.1	11	0.082
1N5246B	15.2	16	16.8	17	7.8	600	0.25	0.1	12	0.083
1N5247B	16.15	17	17.85	19	7.4	600	0.25	0.1	13	0.084
1N5248B	17.1	18	18.9	21	7.0	600	0.25	0.1	14	0.085
1N5249B	18.05	19	19.95	23	6.6	600	0.25	0.1	14	0.085
1N5250B	19	20	21	25	6.2	600	0.25	0.1	15	0.086
1N5251B	20.9	22	23.1	29	5.6	600	0.25	0.1	17	0.087
1N5252B	22.8	24	25.2	33	5.2	600	0.25	0.1	18	0.088
1N5253B	23.75	25	26.25	35	5.0	600	0.25	0.1	19	0.088
1N5254B	25.65	27	28.35	41	4.6	600	0.25	0.1	21	0.089
1N5255B	26.6	28	29.4	44	4.5	600	0.25	0.1	21	0.090
1N5256B	28.5	30	31.5	49	4.2	600	0.25	0.1	23	0.09
1N5257B	31.35	33	34.65	58	3.8	700	0.25	0.1	25	0.092
1N5258B	34.2	36	37.8	70	3.4	700	0.25	0.1	27	0.093
1N5259B	37.05	39	40.95	80	3.2	800	0.25	0.1	30	0.094
1N5260B	40.85	43	45.15	93	3.0	900	0.25	0.1	33	0.095
1N5261B	44.65	47	49.35	105	2.7	1000	0.25	0.1	36	0.095
1N5262B	48.45	51	53.55	125	2.5	1100	0.25	0.1	39	0.096
1N5263B	53.2	56	58.8	150	2.2	1300	0.25	0.1	43	0.096
V_F Forward Voltage = 1.2V Max. @ I_F = 200mA										

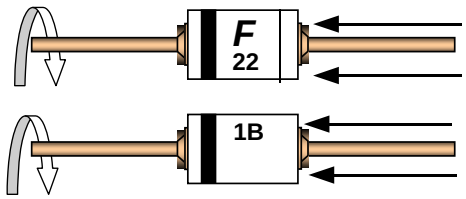
Note:

2. Zener Voltage (V_Z)
The zener voltage is measured with the device junction in the thermal equilibrium at the lead temperature (T_L) at 30°C ± 1°C and 3/8” lead length.

Top Mark Information

Device	Line 1	Line 2	Line 3
1N5221B	LOGO	22	1B
1N5222B	LOGO	22	2B
1N5223B	LOGO	22	3B
1N5224B	LOGO	22	4B
1N5225B	LOGO	22	5B
1N5226B	LOGO	22	6B
1N5227B	LOGO	22	7B
1N5228B	LOGO	22	8B
1N5229B	LOGO	22	9B
1N5230B	LOGO	23	0B
1N5231B	LOGO	23	1B
1N5232B	LOGO	23	2B
1N5233B	LOGO	23	3B
1N5234B	LOGO	23	4B
1N5235B	LOGO	23	5B
1N5236B	LOGO	23	6B
1N5237B	LOGO	23	7B
1N5238B	LOGO	23	8B
1N5239B	LOGO	23	9B
1N5240B	LOGO	24	0B
1N5241B	LOGO	24	1B
1N5242B	LOGO	24	2B
1N5243B	LOGO	24	3B
1N5244B	LOGO	24	4B
1N5245B	LOGO	24	5B
1N5246B	LOGO	24	6B
1N5247B	LOGO	24	7B
1N5248B	LOGO	24	8B
1N5249B	LOGO	24	9B
1N5250B	LOGO	25	0B
1N5251B	LOGO	25	1B
1N5252B	LOGO	25	2B
1N5253B	LOGO	25	3B
1N5254B	LOGO	25	4B
1N5255B	LOGO	25	5B
1N5256B	LOGO	25	6B
1N5257B	LOGO	25	7B
1N5258B	LOGO	25	8B
1N5259B	LOGO	25	9B
1N5260B	LOGO	26	0B
1N5261B	LOGO	26	1B
1N5262B	LOGO	26	2B
1N5263B	LOGO	26	3B

Top Mark Information (Continued)



1st line: F - Fairchild Logo

2nd line: Device Name - 4th to 5th characters of the device name.
or 5th to 6th characters for BZXyy series

3rd line: Device Name - 6th to 7th characters of the device name.
or Voltage rating for BZXyy series

General Requirements:

1.0 Cathode Band

2.0 First Line: F - Fairchild Logo

3.0 Second Line: Device name - For 1Nxx series: 4th to 5th characters of the device name.
For BZxx series: 5th to 6th characters of the device name.

4.0 Third Line: Device name - For 1Nxx series: 6th to 7th characters of the device name.
For BZXyy series: Voltage rating

5.0 Devices shall be marked as required in the device specification (PID or FSC Test Spec).

6.0 Maximum no. of marking lines: 3

7.0 Maximum no. of digits per line: 2

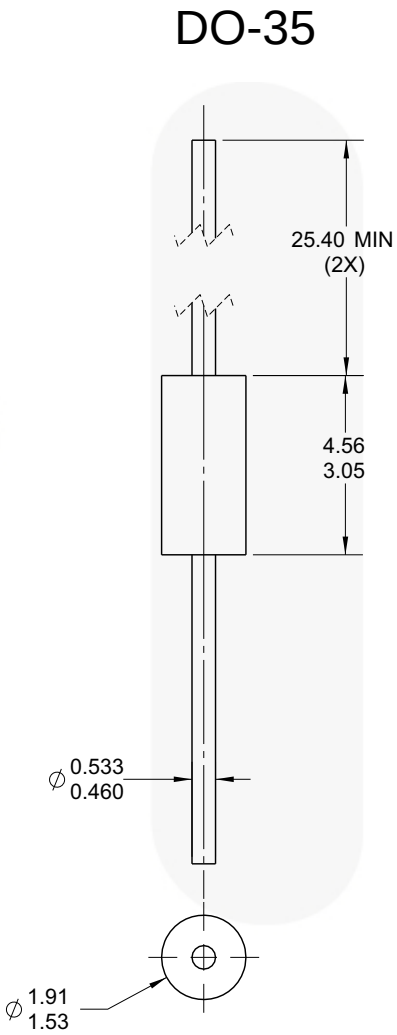
8.0 FSC logo must be 20 % taller than the alphanumeric marking and should occupy the 2 characters of the specified line.

9.0 Marking Font: Arial (Except FSC Logo)

10.0 First character of each marking line must be aligned vertically.

11.0 All device markings must be based on Fairchild device specification.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE:
JEDEC DO-204, VARIATION AH.
B) HERMETICALLY SEALED GLASS PACKAGE.
C) PACKAGE WEIGHT IS 0.137 GRAM.
D) ALL DIMENSIONS ARE IN MILLIMETERS.
E) DRAWING FILE NAME: DO35AREV02

Figure 1. AXIAL LEADED; GLASS; JEDEC DO204; VARIATION AH (ACTIVE)

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64

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January 2016

1N5221B - 1N5263B
Zener Diodes

Tolerance = 5%

DO-35 Glass case
COLOR BAND DENOTES CATHODE

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	500	mW
	Derate above 50°C	4.0	mW°C
T_{STG}	Storage Temperature Range	-65 to +200	°C
T_J	Operating Junction Temperature Range	-65 to +200	°C
	Lead Temperature (1/16 inch from case for 10 s)	+230	°C

Note:

1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
   Non-recurrent square wave Pulse Width = 8.3 ms, T_A = 50°C

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted .

Device	V_Z (V) @ I_Z (2)			Z_Z (Ω) @ I_Z (mA)		Z_{ZK} (Ω) @ I_{ZK}(mA)		I_R (μA) @ V_R (V)		T_C (%/°C)
	Min.	Typ.	Max.							
1N5221B	2.28	2.4	2.52	30	20	1,200	0.25	100	1.0	-0.085
1N5222B	2.375	2.5	2.625	30	20	1,250	0.25	100	1.0	-0.085
1N5223B	2.565	2.7	2.835	30	20	1,300	0.25	75	1.0	-0.080
1N5224B	2.66	2.8	2.94	30	20	1,400	0.25	75	1.0	-0.080
1N5225B	2.85	3	3.15	29	20	1,600	0.25	50	1.0	-0.075
1N5226B	3.135	3.3	3.465	28	20	1,600	0.25	25	1.0	-0.07
1N5227B	3.42	3.6	3.78	24	20	1,700	0.25	15	1.0	-0.065
1N5228B	3.705	3.9	4.095	23	20	1,900	0.25	10	1.0	-0.06
1N5229B	4.085	4.3	4.515	22	20	2,000	0.25	5.0	1.0	+/-0.055
1N5230B	4.465	4.7	4.935	19	20	1,900	0.25	5.0	2.0	+/-0.03
1N5231B	4.845	5.1	5.355	17	20	1,600	0.25	5.0	2.0	+/-0.03
1N5232B	5.32	5.6	5.88	11	20	1,600	0.25	5.0	3.0	0.038
1N5233B	5.7	6	6.3	7.0	20	1,600	0.25	5.0	3.5	0.038
1N5234B	5.89	6.2	6.51	7.0	20	1,000	0.25	5.0	4.0	0.045
1N5235B	6.46	6.8	7.14	5.0	20	750	0.25	3.0	5.0	0.05
1N5236B	7.125	7.5	7.875	6.0	20	500	0.25	3.0	6.0	0.058
1N5237B	7.79	8.2	8.61	8.0	20	500	0.25	3.0	6.5	0.062
1N5238B	8.265	8.7	9.135	8.0	20	600	0.25	3.0	6.5	0.065
1N5239B	8.645	9.1	9.555	10	20	600	0.25	3.0	7.0	0.068
1N5240B	9.5	10	10.5	17	20	600	0.25	3.0	8.0	0.075
1N5241B	10.45	11	11.55	22	20	600	0.25	2.0	8.4	0.076
1N5242B	11.4	12	12.6	30	20	600	0.25	1.0	9.1	0.077
1N5243B	12.35	13	13.65	13	9.5	600	0.25	0.5	9.9	0.079
1N5244B	13.3	14	14.7	15	9.0	600	0.25	0.1	10	0.080
1N5245B	14.25	15	15.75	16	8.5	600	0.25	0.1	11	0.082
1N5246B	15.2	16	16.8	17	7.8	600	0.25	0.1	12	0.083
1N5247B	16.15	17	17.85	19	7.4	600	0.25	0.1	13	0.084
1N5248B	17.1	18	18.9	21	7.0	600	0.25	0.1	14	0.085
1N5249B	18.05	19	19.95	23	6.6	600	0.25	0.1	14	0.085
1N5250B	19	20	21	25	6.2	600	0.25	0.1	15	0.086
1N5251B	20.9	22	23.1	29	5.6	600	0.25	0.1	17	0.087
1N5252B	22.8	24	25.2	33	5.2	600	0.25	0.1	18	0.088
1N5253B	23.75	25	26.25	35	5.0	600	0.25	0.1	19	0.088
1N5254B	25.65	27	28.35	41	4.6	600	0.25	0.1	21	0.089
1N5255B	26.6	28	29.4	44	4.5	600	0.25	0.1	21	0.090
1N5256B	28.5	30	31.5	49	4.2	600	0.25	0.1	23	0.09
1N5257B	31.35	33	34.65	58	3.8	700	0.25	0.1	25	0.092
1N5258B	34.2	36	37.8	70	3.4	700	0.25	0.1	27	0.093
1N5259B	37.05	39	40.95	80	3.2	800	0.25	0.1	30	0.094
1N5260B	40.85	43	45.15	93	3.0	900	0.25	0.1	33	0.095
1N5261B	44.65	47	49.35	105	2.7	1000	0.25	0.1	36	0.095
1N5262B	48.45	51	53.55	125	2.5	1100	0.25	0.1	39	0.096
1N5263B	53.2	56	58.8	150	2.2	1300	0.25	0.1	43	0.096
V_F Forward Voltage = 1.2V Max. @ I_F = 200mA										

Note:

2. Zener Voltage (V_Z)
   The zener voltage is measured with the device junction in the thermal equilibrium at the lead temperature (T_L) at 30°C ± 1°C and 3/8" lead length.

Top Mark Information

Device	Line 1	Line 2	Line 3
1N5221B	LOGO	22	1B
1N5222B	LOGO	22	2B
1N5223B	LOGO	22	3B
1N5224B	LOGO	22	4B
1N5225B	LOGO	22	5B
1N5226B	LOGO	22	6B
1N5227B	LOGO	22	7B
1N5228B	LOGO	22	8B
1N5229B	LOGO	22	9B
1N5230B	LOGO	23	0B
1N5231B	LOGO	23	1B
1N5232B	LOGO	23	2B
1N5233B	LOGO	23	3B
1N5234B	LOGO	23	4B
1N5235B	LOGO	23	5B
1N5236B	LOGO	23	6B
1N5237B	LOGO	23	7B
1N5238B	LOGO	23	8B
1N5239B	LOGO	23	9B
1N5240B	LOGO	24	0B
1N5241B	LOGO	24	1B
1N5242B	LOGO	24	2B
1N5243B	LOGO	24	3B
1N5244B	LOGO	24	4B
1N5245B	LOGO	24	5B
1N5246B	LOGO	24	6B
1N5247B	LOGO	24	7B
1N5248B	LOGO	24	8B
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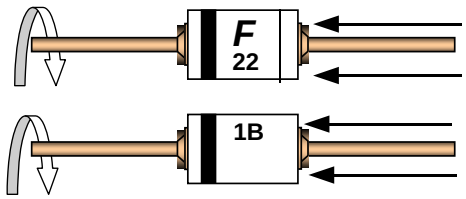
1N5255B	LOGO	25	5B
1N5256B	LOGO	25	6B
1N5257B	LOGO	25	7B
1N5258B	LOGO	25	8B
1N5259B	LOGO	25	9B
1N5260B	LOGO	26	0B
1N5261B	LOGO	26	1B
1N5262B	LOGO	26	2B
1N5263B	LOGO	26	3B

Top Mark Information (Continued)



1st line: F - Fairchild Logo

2nd line: Device Name - 4th to 5th characters of the device name.
or 5th to 6th characters for BZXyy series

3rd line: Device Name - 6th to 7th characters of the device name.
or Voltage rating for BZXyy series

General Requirements:

1.0 Cathode Band

2.0 First Line: F - Fairchild Logo

3.0 Second Line: Device name - For 1Nxx series: 4th to 5th characters of the device name.
For BZxx series: 5th to 6th characters of the device name.

4.0 Third Line: Device name - For 1Nxx series: 6th to 7th characters of the device name.
For BZXyy series: Voltage rating

5.0 Devices shall be marked as required in the device specification (PID or FSC Test Spec).

6.0 Maximum no. of marking lines: 3

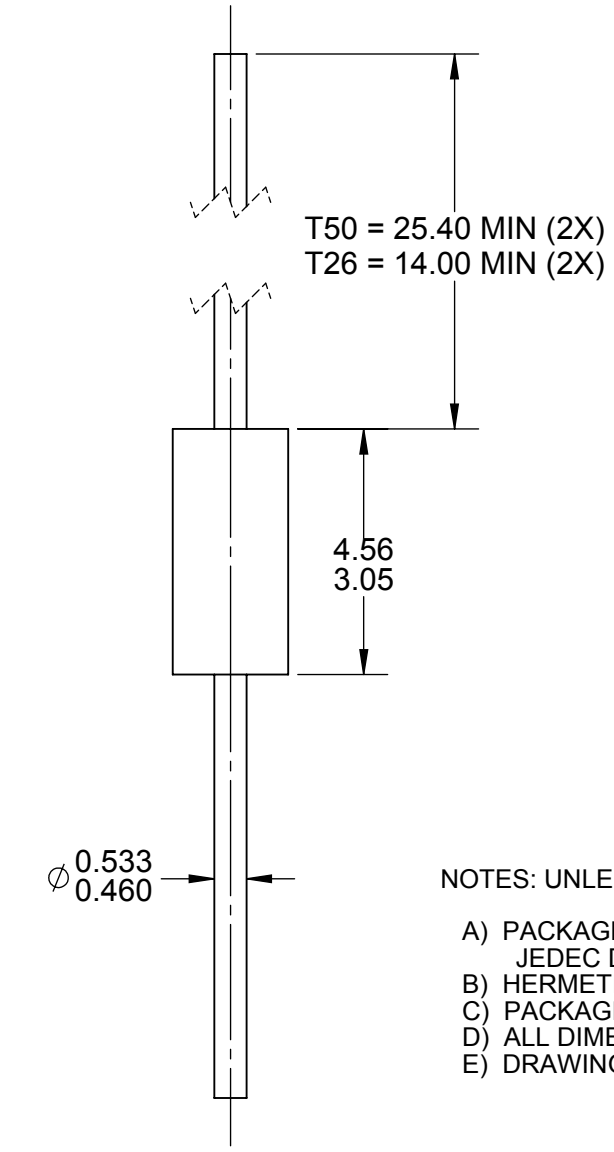
7.0 Maximum no. of digits per line: 2

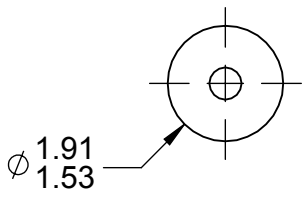
8.0 FSC logo must be 20 % taller than the alphanumeric marking and should occupy the 2 characters of the specified line.

9.0 Marking Font: Arial (Except FSC Logo)

10.0 First character of each marking line must be aligned vertically.

11.0 All device markings must be based on Fairchild device specification.





NOTES: UNLESS OTHERWISE SPECIFIED

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B) HERMETICALLY SEALED GLASS PACKAGE.
C) PACKAGE WEIGHT IS 0.137 GRAM.
D) ALL DIMENSIONS ARE IN MILLIMETERS.
E) DRAWING FILE NAME: DO35AREV03

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- High IMR: 140 dB at 60 Hz
- 0.010% Maximum Nonlinearity
- Bipolar Operation: V_O = ±10 V
- DIP-16 and SO-28
- Ease of Use: Fixed Unity Gain Configuration
- ±4.5-V to ±18-V Supply Range

2 Applications

- Industrial Process Control:
  - Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4-mA to 20-mA Loop Isolation
- Ground Loop Elimination
- Motor and SCR Control
- Power Monitoring
- PC-Based Data Acquisition
- Test Equipment

3 Description

The ISO124 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2-pF differential capacitive barrier. With digital modulation, the barrier characteristics do not affect signal integrity, thus resulting in excellent reliability and good high-frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO124 is easy to use. No external components are required for operation. The key specifications are 0.010% maximum nonlinearity, 50-kHz signal bandwidth, and 200-µV/°C V_{OS} drift. A power supply range of ±4.5 V to ±18 V and quiescent currents of ±5 mA on V_{S1} and ±5.5 mA on V_{S2} make the ISO124 device ideal for a wide range of applications.

The ISO124 is available in SOIC-16 and SOIC-28 plastic surface-mount packages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO124	SOIC (16)	17.90 mm × 7.50 mm
	SOIC (28)	20.01 mm × 6.61 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

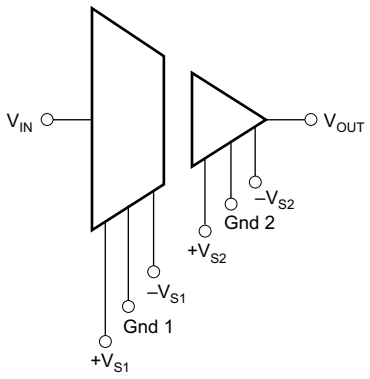


Table of Contents

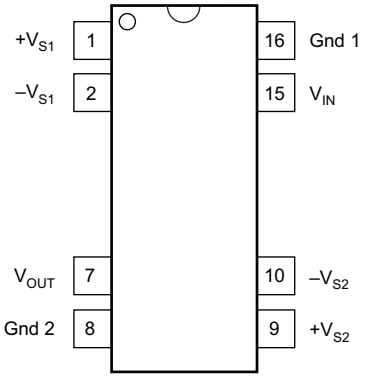
5 Revision History

Changes from Revision C (September 2005) to Revision D **Page**

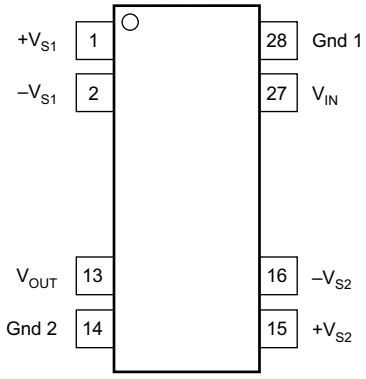
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

6 Pin Configuration and Functions

DVA Package
16 Pins SOIC
Top View



NVF Package
28 Pins SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	SOIC		
GND	8	14	–	Low-side ground reference
	16	28	–	High-side ground reference
V_{IN}	15	27	I	High-side analog input
V_{OUT}	7	13	O	Low-side analog output
$+V_{S1}$	1	1	–	High-side positive analog supply
$–V_{S1}$	2	2	–	High-side negative analog supply
$+V_{S2}$	9	15	–	Low-side positive analog supply
$–V_{S2}$	10	16	–	Low-side negative analog supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage		±18	V
V_{IN}		100	V
Continuous isolation voltage		1500	Vrms
Junction temperature		125	°C
Output short to common		Continuous	
Storage temperature, T_{stg}	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
T_A	–25		85	°C
V_{S1}		±15		V
V_{S2}		±15		V
V_{IN}		±10		V

7.4 Thermal Information

THERMAL METRIC (1)		ISO124		UNIT
		DVA (SOIC)	NVF (SOIC)	
		16 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.8	51.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	32.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	29.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.9	29.0	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.5 Electrical Characteristics

At T_A = +25°C , V_{S1} = V_{S2} = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ISO124P, U			UNIT
			MIN	TYP	MAX	
ISOLATION						
	Rated Voltage, continuous ac 60 Hz		1500			Vac
	100% Test(1)	1s, 5pc PD	2400			Vac
	Isolation Mode Rejection	60 Hz		140		dB
	Barrier Impedance			10^{14} || 2		Ω || pF
	Leakage Current at 60 Hz	V_{ISO} = 240 Vrms		0.18	0.5	µArms
GAIN						
	Nominal Gain	V_O = ±10 V		1		V/V
	Gain Error			±0.05	±0.50	%FSR
	Gain vs Temperature			±10		ppm/°C
	Nonlinearity(2)			±0.005	±0.010	%FSR
INPUT OFFSET VOLTAGE						
	Initial Offset			±20	±50	mV
	vs Temperature			±200		µV/°C
	vs Supply			±2		mV/V
	Noise			4		µV/√Hz
INPUT						
	Voltage Range		±10	±12.5		V
	Resistance			200		kΩ
OUTPUT						
	Voltage Range		±10	±12.5		V
	Current Drive		±5	±15		mA
	Capacitive Load Drive			0.1		µF
	Ripple Voltage(3)			20		mVp-p
FREQUENCY RESPONSE						
	Small-Signal Bandwidth			50		kHz
	Slew Rate			2		V/µs
	Settling Time 0.10%	V_O = ±10 V		50		µs
	Settling Time 0.01%			350		µs
	Overload Recovery Time			150		µs
POWER SUPPLIES						
	Rated Voltage			±15		V
	Voltage Range		±4.5		±18	V
V_{S1}	Quiescent Current			±5.0	±7.0	mA
V_{S2}				±5.5	±7.0	
TEMPERATURE RANGE						
	Specification		–25		85	°C
	Operating		–25		85	°C
	Storage		–40		125	°C
$R_{\theta JA}$	Thermal Resistance			100		°C/W
$R_{\theta JC}$				65		°C/W

(1) Tested at 1.6 X rated, fail on 5 pC partial discharge.
(2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR.
(3) Ripple frequency is at carrier frequency (500 kHz).

7.6 Typical Characteristics

At T_A = +25°C, and V_S = ±15 V, unless otherwise noted.

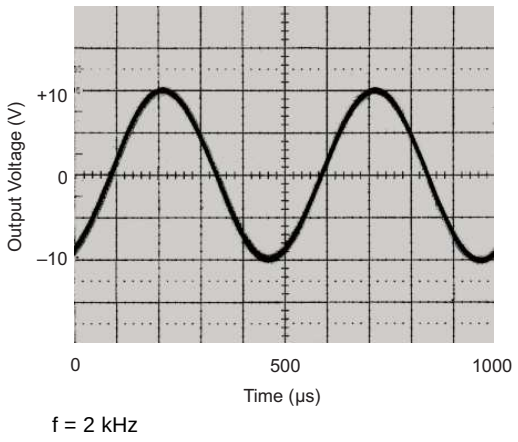


Figure 1. Sine Response

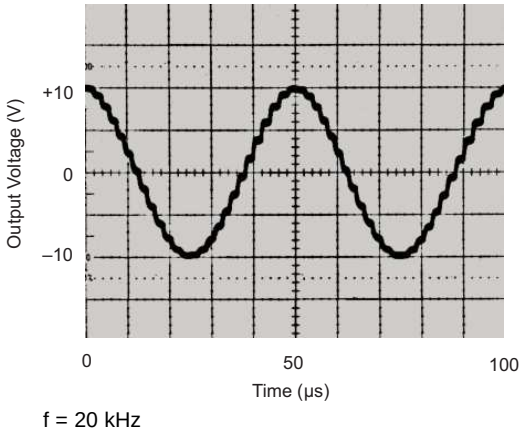


Figure 2. Sine Response

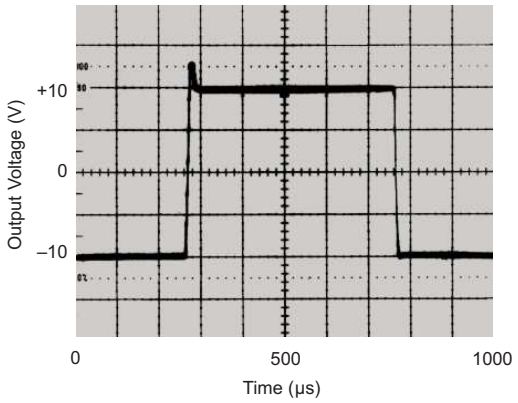


Figure 3. Step Response

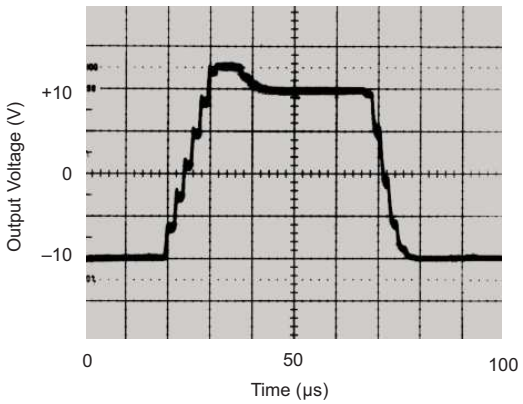


Figure 4. Step Response

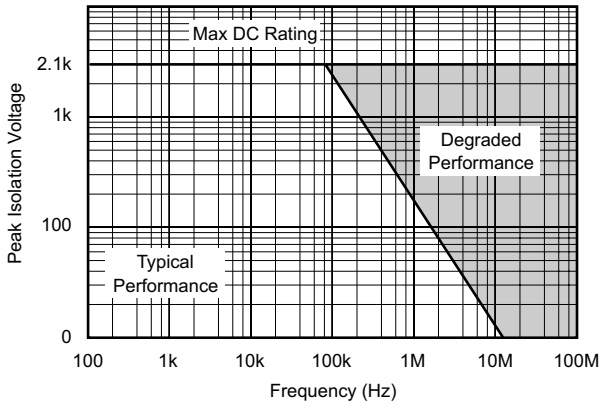


Figure 5. Isolation Voltage vs Frequency

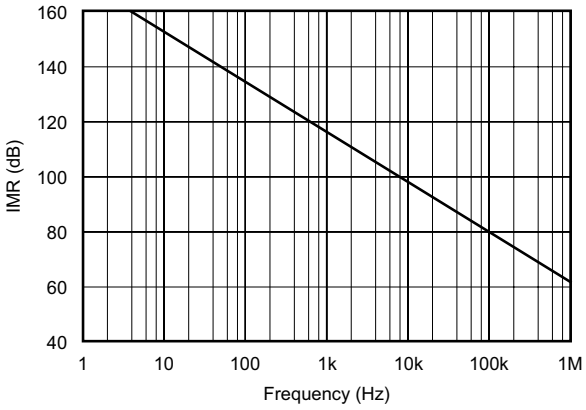


Figure 6. IMR vs Frequency

Typical Characteristics (continued)

At T_A = +25°C, and V_S = ±15 V, unless otherwise noted.

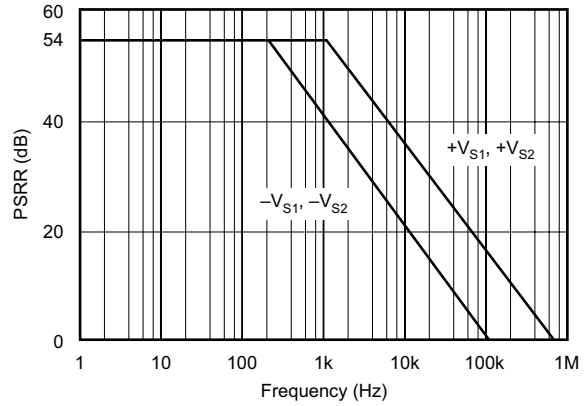


Figure 7. PSRR vs Frequency

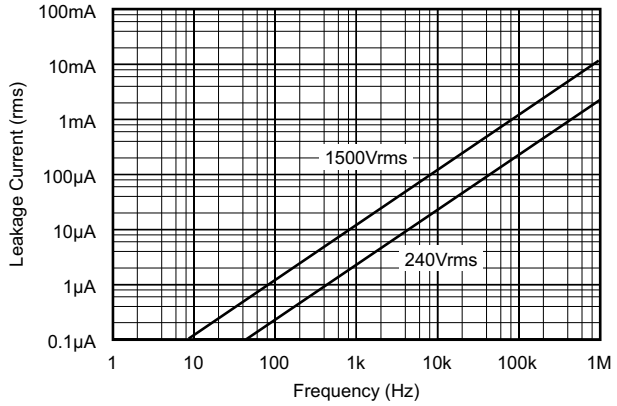
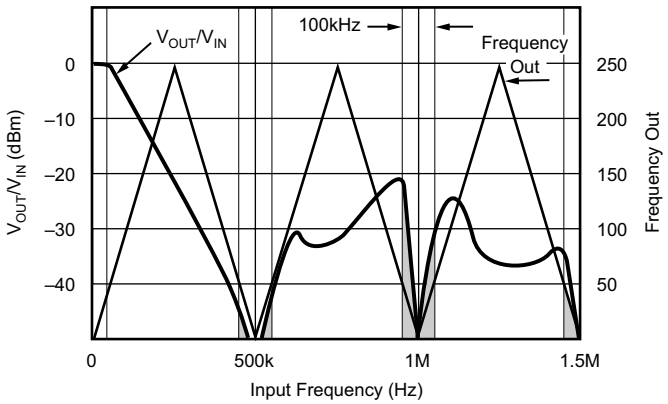


Figure 8. Isolation Leakage Current vs Frequency



NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.

Figure 9. Signal Response to Inputs Greater than 250 kHz

8 Detailed Description

8.1 Overview

The ISO124 isolation amplifier uses an input and an output section galvanically isolated by matched 1-pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections. The ISO124 contains 250 transistors.

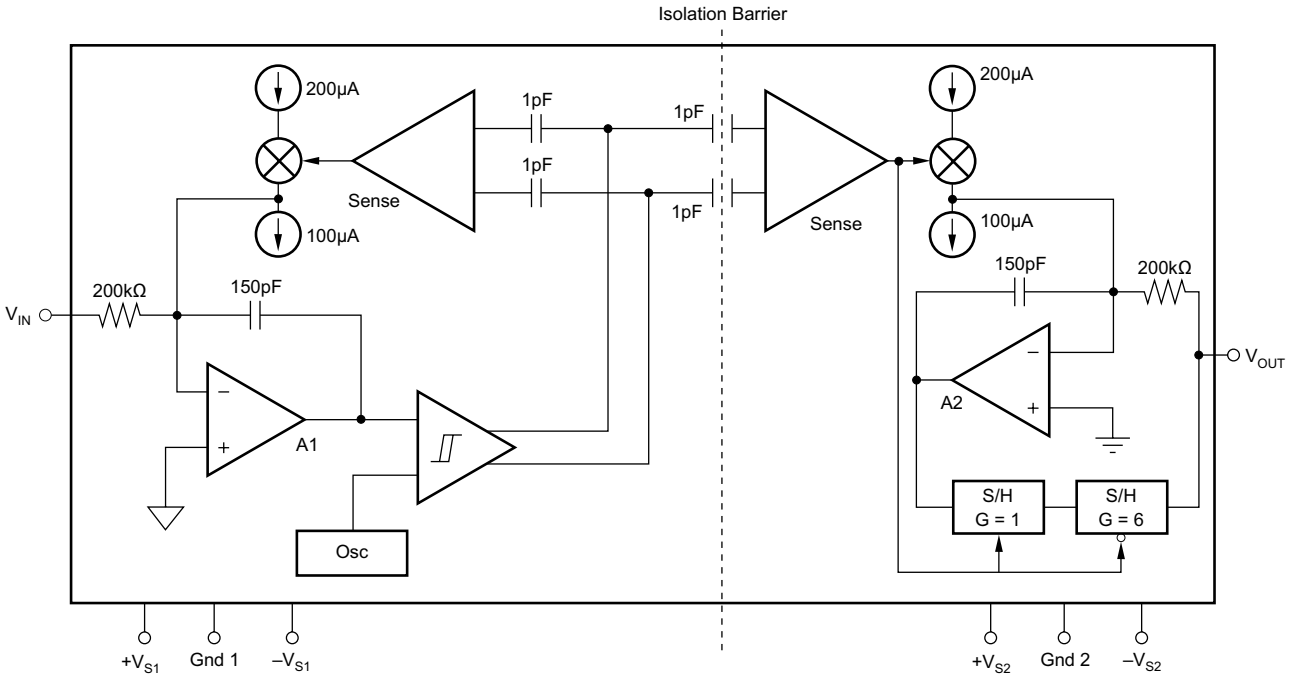
8.1.1 Module

An input amplifier (A1, as shown in *Functional Block Diagram*) integrates the difference between the input current (V_{IN}/200 kΩ) and a switched ±100-µA current source. This current source is implemented by a switchable 200-µA source and a fixed 100-µA current sink. To understand the basic operation of the modulator, assume that V_{IN} = 0 V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500 kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave

8.1.2 Demodulator

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200-kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample-and-hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Isolation Amplifier

The ISO124 is a precision analog isolation amplifier. The input signal is transmitted digitally across a high-voltage differential capacitive barrier. With digital modulation, the barrier characteristics do affect signal integrity, resulting in excellent reliability and high-frequency transient immunity.

8.4 Device Functional Modes

The ISO124 device does not have any additional functional modes.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Carrier Frequency Considerations

The ISO124 amplifier transmits the signal across the isolation barrier by a 500-kHz duty-cycle modulation technique. For input signals having frequencies below 250 kHz, this system works like any linear amplifier. But for frequencies above 250 kHz, the behavior is similar to that of a sampling amplifier. Figure 9 shows this behavior graphically; at input frequencies above 250 kHz, the device generates an output signal component of reduced magnitude at a frequency below 250 kHz. This is the aliasing effect of sampling at frequencies less than two times the signal frequency (the Nyquist frequency). At the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

9.1.2 Isolation Mode Voltage Induced Errors

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250 kHz, the output also will display spurious outputs (aliasing) in a manner similar to that for V_{IN} > 250 kHz and the amplifier response will be identical to that shown in Figure 9.This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in Figure 11 and compute the amplifier response to this input-referred error signal from the data shown in Figure 9. For example, if a 800-kHz 1000-Vrms IMR is present, then a total of [(–60 dB) + (–30 dB)] x (1000 V) = 32-mV error signal at 200 kHz plus a 1-V, 800-kHz error signal will be present at the output.

9.1.3 High IMV dV/dt Errors

As the IMV frequency increases and the dV/dt exceeds 1000 Vμs, the sense amp may start to false trigger, and the output will display spurious errors. The common-mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power-supply voltages below ±15 V may decrease the dV/dt to 500 V/M s for typical performance.

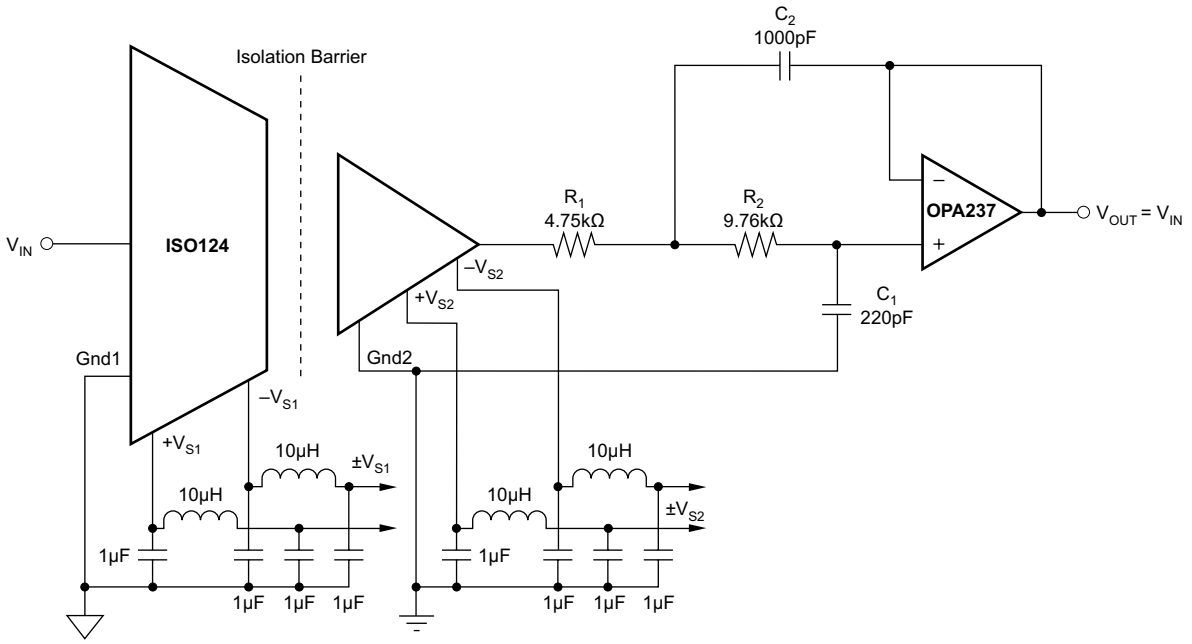
9.1.4 High Voltage Testing

TI has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (< 5 pC) while applying 2400-Vrms, 60-Hz high-voltage stress across every ISO124 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 × 1500 Vrms) protection without damage to the ISO124. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the art" for nondestructive high-voltage reliability testing. It is based on the effects of nonuniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void nonuniformities, electric field stress begins to ionize the void region before bridging the entire high-voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01–0.1-μs current pulses that repeat on each ac voltage cycle. The minimum ac barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." The package insulation processes have been characterized and developed to yield an inception voltage in excess of 2400 Vrms so that transient overvoltages below this level will not damage the ISO124. The extinction voltage is above 1500 Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500-Vrms (rated) level. Older high-voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

9.2 Typical Applications

9.2.1 Output Filters



For more information concerning output filters, see *Simple Output Filter Elminiates ISO Amp Output Ripple and Keeps Full Bandwidth* and *FilterPro™ MFB and Sallen-Key Low-Pass Filter Design Program User Guide*.

Figure 10. ISO124 With Output Filter for Improved Ripple

9.2.1.1 Design Requirements

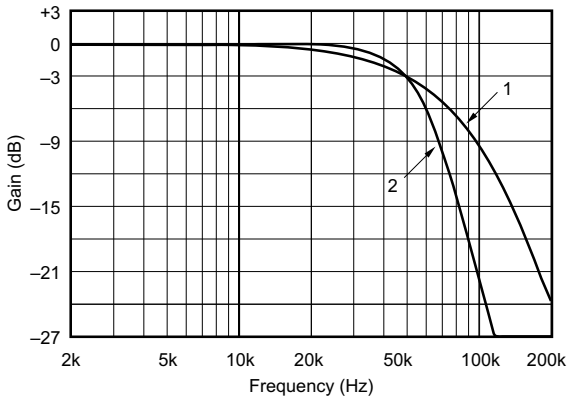
The ISO124 isolation amplifiers (ISO amps) have a small (10 to 20 mVp-p typical) residual demodulator ripple at the output. A simple filter can be added to eliminate the output ripple without decreasing the 50kHz signal bandwidth of the ISO amp.

9.2.1.2 Detailed Design Procedure

The ISO124 device is designed to have a 50-kHz single-pole (Butterworth) signal response. By cascading the ISO amp with a simple 50-kHz, Q = 1, two-pole, low-pass filter, the overall signal response becomes three-pole Butterworth. The result is a maximally flat 50-kHz magnitude response and the output ripple reduced below the noise level. Figure 10 shows the complete circuit. The two-pole filter is a unity-gain Sallen-Key type consisting of A1, R1, R2, C1, and C2. The values shown give Q = 1 and f–3dB bandwidth = 50 kHz. Because the op amp is connected as a unity-gain follower, gain and gain accuracy of the ISO amp are unaffected. Using a precision op amp such as the OPA602 also preserves the DC accuracy of the ISO amp.

Typical Applications (continued)

9.2.1.3 Application Curves



1) Standard ISO124 has 50kHz single-pole (Butterworth) response.

2) ISO124 with cascaded 50kHz, Q = 1, two-pole, low-pass filter has three-pole Butterworth response.

Figure 11. Gain vs. Frequency

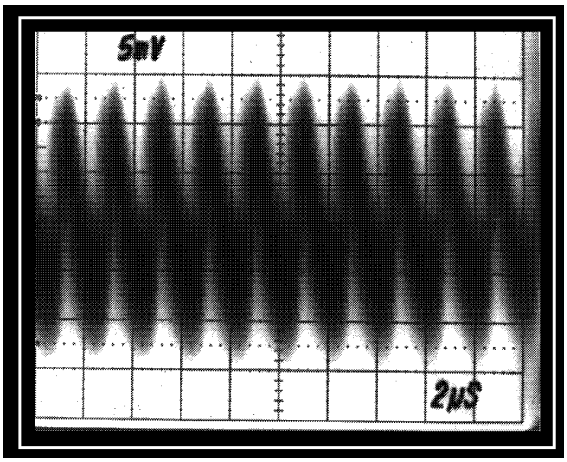


Figure 12. Standard ISO124 (Approximately 20-mVp-p Output Ripple)

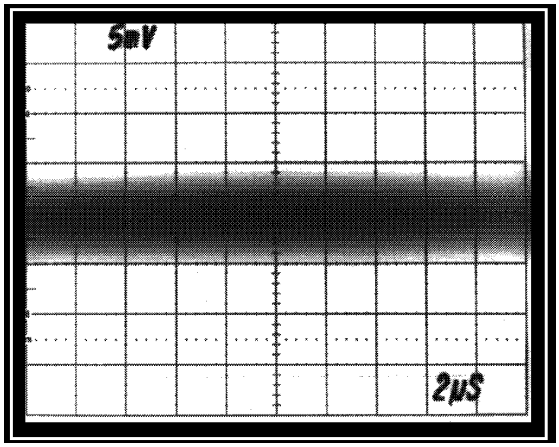


Figure 13. Filtered ISO124 (No Visible Output Ripple)

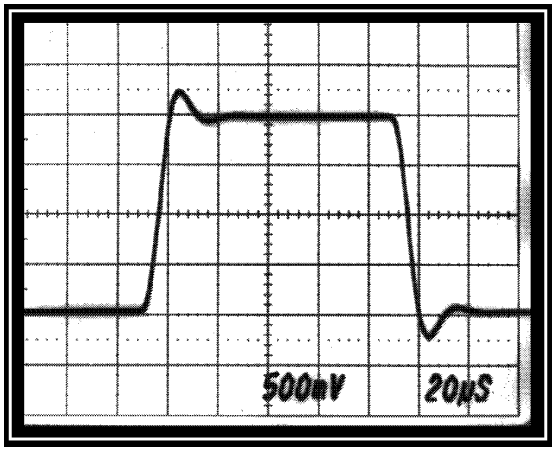


Figure 14. Step Response of Standard ISO124

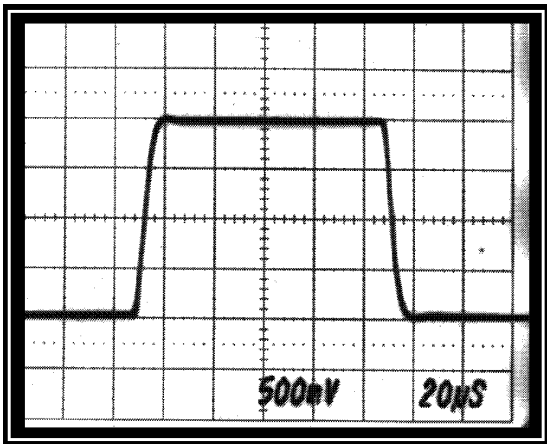


Figure 15. Step Response of ISO124 With Added Twopole Output Filter

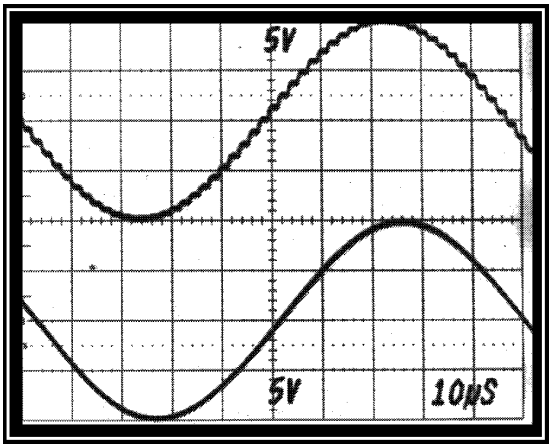
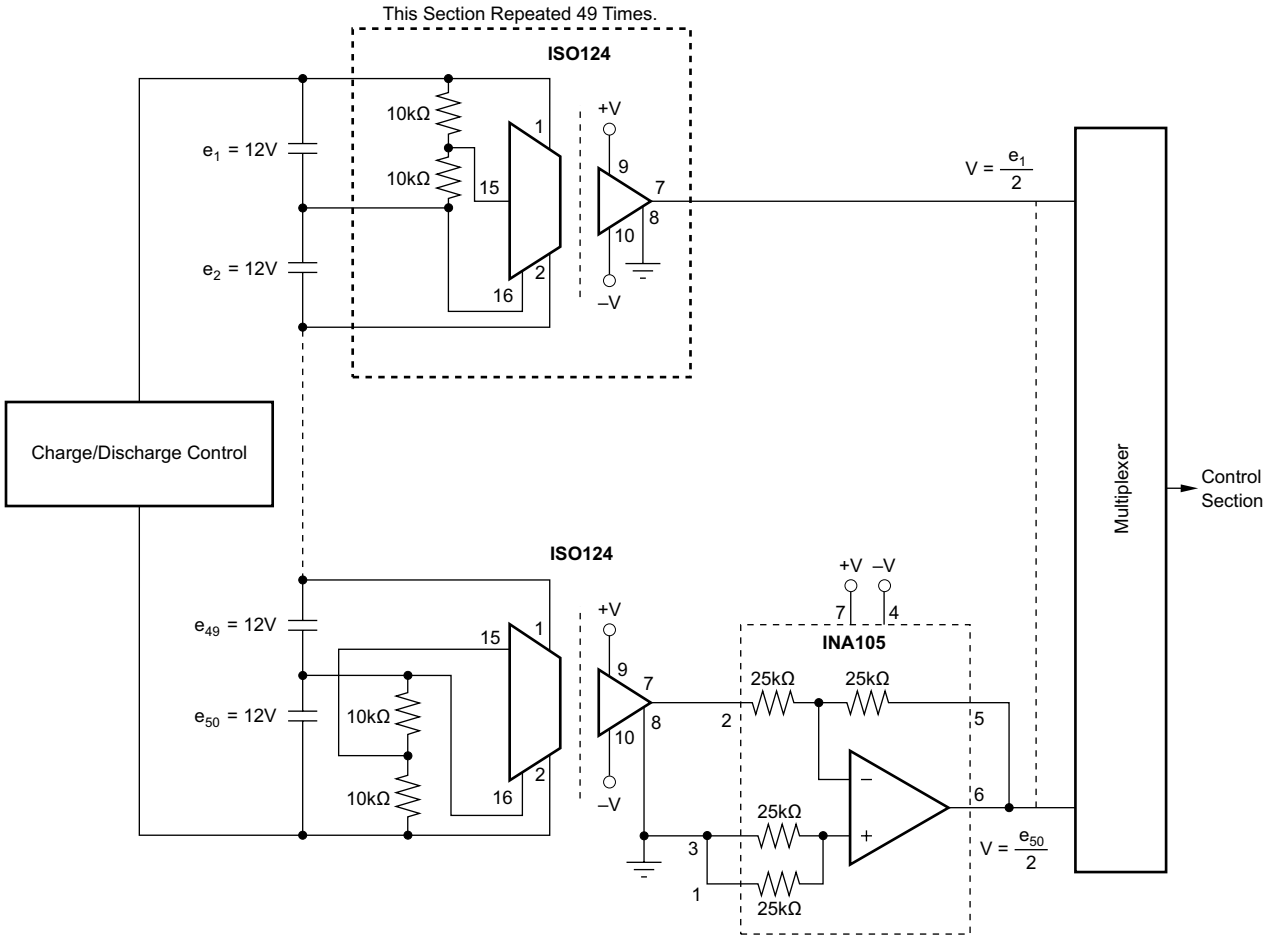


Figure 16. Large-signal, 10-kHz Sine-wave Response of ISO124 With and Without Output Filter

Typical Applications (continued)

9.2.2 Battery Monitor

Figure 17 provides a means to monitor the cell voltage on a 600-V battery stack by using the battery as a power source for the isolated voltage.



(Derives input power from the battery.)

Figure 17. Battery Monitor for a 600-V Battery Power System

Typical Applications (continued)

9.2.3 Programmable Gain Amplifier

In applications where variable gain configurations are required, a programmable gain amplifier like the PGA102 can be used with the ISO124 device. Figure 18 uses an ISO150 device to provide gain pin selection options to the PGA102 device.

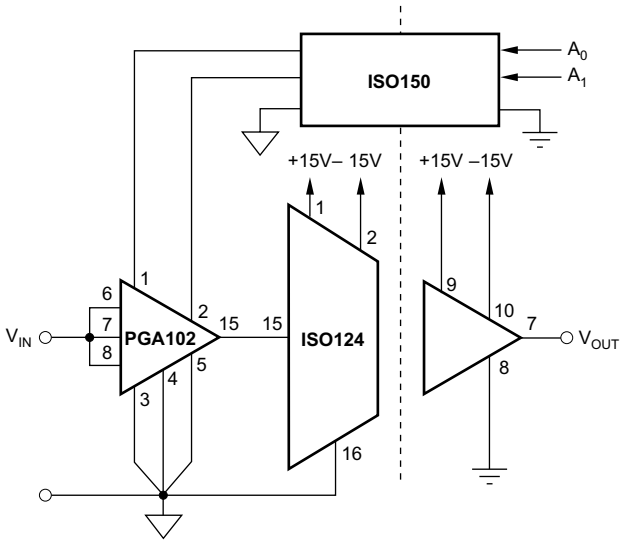
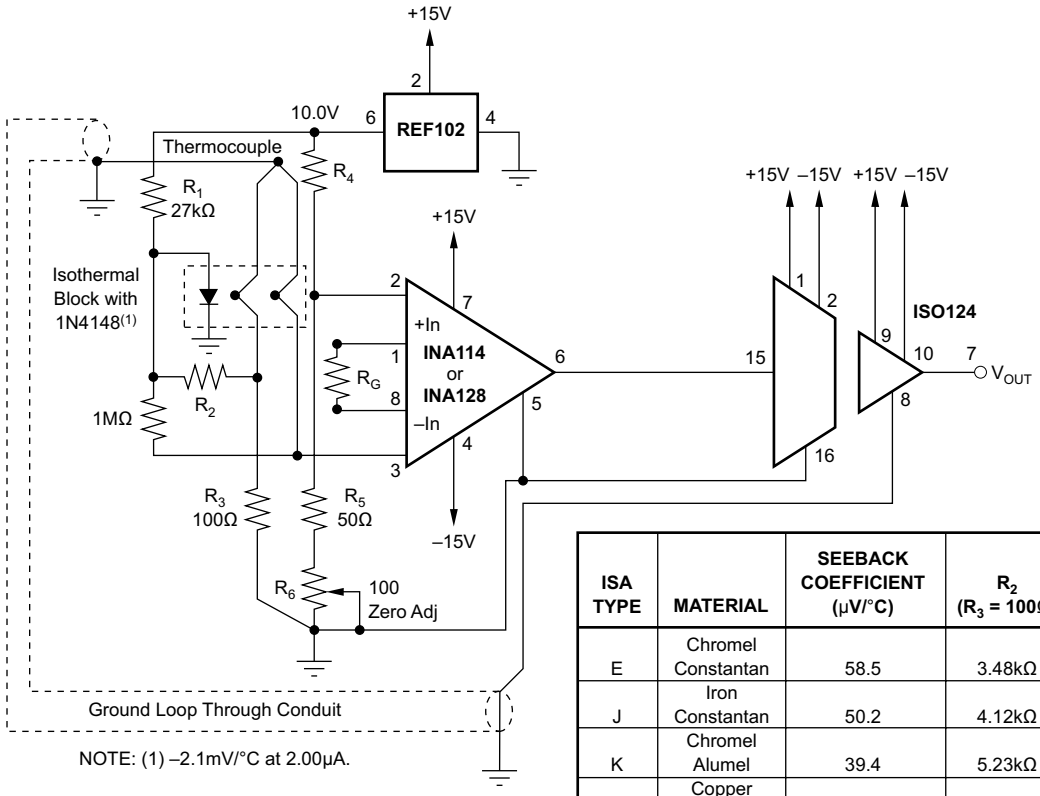


Figure 18. Programmable-Gain Isolation Channel With Gains of 1, 10, and 100

Typical Applications (continued)

9.2.4 Thermocouple Amplifier

For isolated temperature measurements, Figure 19 provides an application solution using the INA114 or INA128 devices, feeding the input stage of the ISO124 device. The table provides suggested resistor values based on the type of thermistor used in the application.



ISA TYPE	MATERIAL	SEEBACK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

Figure 19. Thermocouple Amplifier With Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out

Typical Applications (continued)

9.2.5 Isolated 4- to 20-mA Instrument Loop

For isolated temperature measurements in a 4- to 20-mA loop, Figure 20 provides a solution using the XTR101 and RCV420 devices. A high-performance PT100 resistance temperature detector (RTD) provides the user with an isolated 0- to 5-V representation of the isolated temperature measurement.

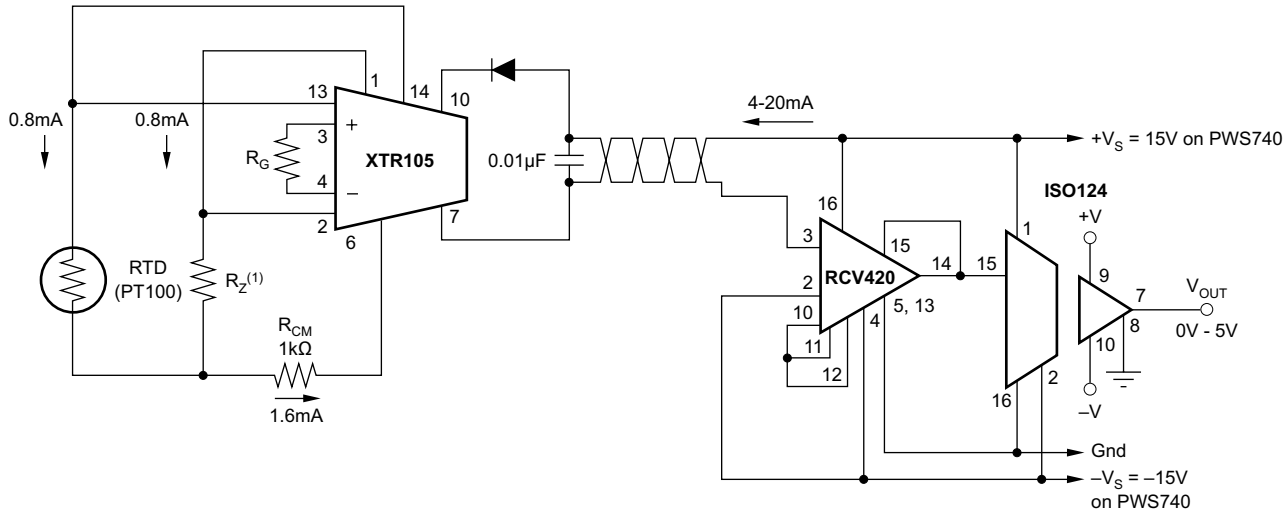
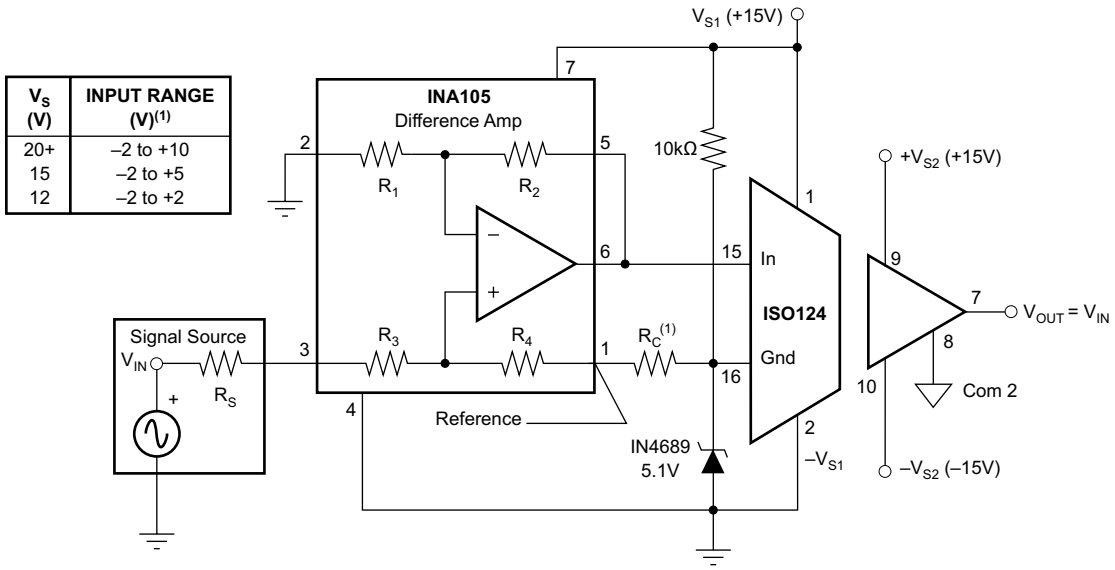


Figure 20. Isolated 4- to 20-mA Instrument Loop (RTD Shown)

9.2.6 Single-Supply Operation of the ISO124 Isolation Amplifier

The circuit shown in Figure 21 uses a 5.1-V Zener diode to generate the negative supply for an ISO12x from a single supply on the high-voltage side of the isolation amplifier. The input measuring range will be dependent on the applied voltage as noted in the accompanying table.

V_S (V)	INPUT RANGE (V)(1)
20+	–2 to +10
15	–2 to +5
12	–2 to +2



NOTE: Because the amplifier is unity gain, the input range is also the output range. The output can go to –2 V because the output section of the ISO amp operates from dual supplies.

For additional information see *Single-Supply Operation of Isolation Amplifiers*.

Figure 21. Single-Supply Operation of the ISO124 Isolation Amplifier Schematic

Typical Applications (continued)

9.2.7 Input-Side Powered ISO Amplifier

The user side of the ISO124 device can be powered from the high voltage side using an isolated DC-DC converter as shown in Figure 22.

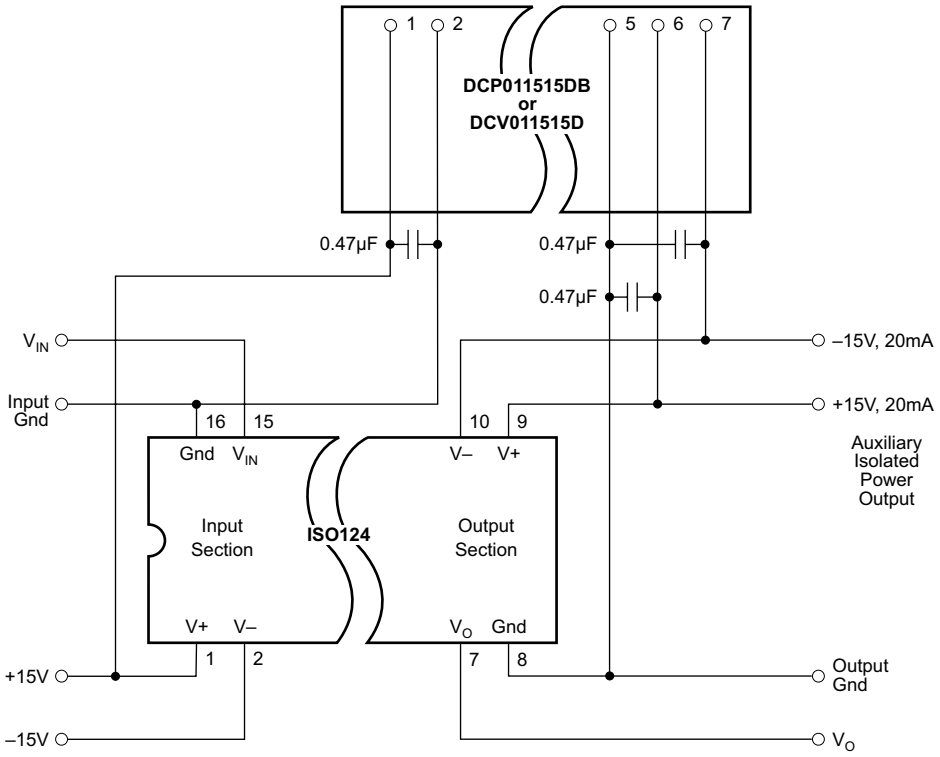


Figure 22. Input-Side Powered ISO Amplifier Schematic

Typical Applications (continued)

9.2.8 Powered ISO Amplifier With Three-Port Isolation

Figure 23 illustrates an application solution that provides isolated power to both the user and high-voltage sides of the ISO124 amplifier.

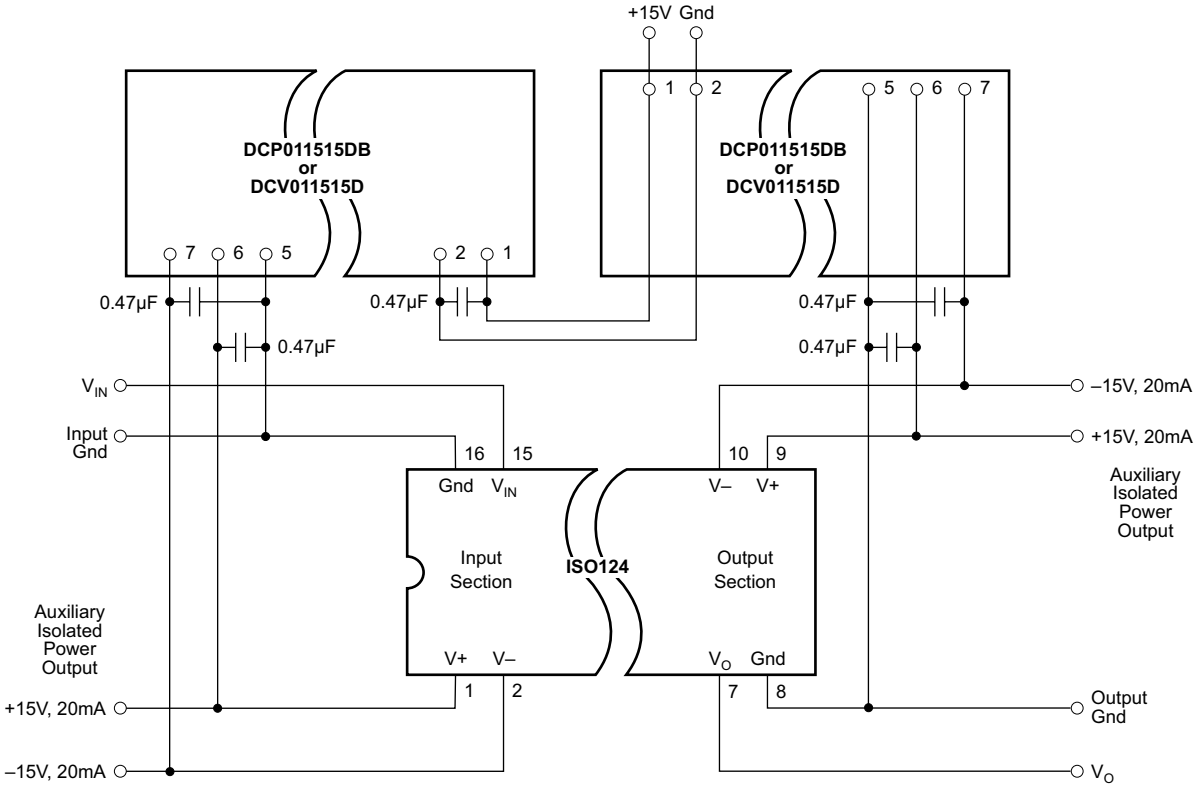


Figure 23. Powered ISO Amplifier With Three-Port Isolation Schematic

10 Power Supply Recommendations

10.1 Signal and Supply Connections

Each power-supply pin should be bypassed with 1-µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500 kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC-DC converter, use a π filter on the supplies (see Figure 10). The ISO124 output has a 500-kHz ripple of 20 mV, which can be removed with a simple 2-pole low-pass filter with a 100-kHz cutoff using a low-cost op amp (see Figure 10).

The input to the modulator is a current (set by the 200-kΩ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least ±15 V. It is therefore possible, when using an unregulated DC-DC converter, to minimize PSR related output errors with ±5-V voltage regulators on the isolated side and still get the full ±10-V input and output swing.

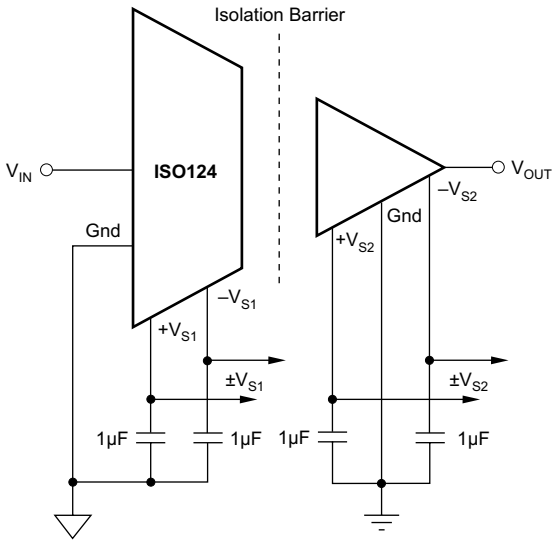


Figure 24. Basic Signal and Power Connections

11 Layout

11.1 Layout Guidelines

To maintain the isolation barrier of the device, the distance between the high-side ground (pin 16 or 28) and the low-side ground (pin 8 or 14) should be kept at maximum; that is, the entire area underneath the device should be kept free of any conducting materials.

11.2 Layout Example

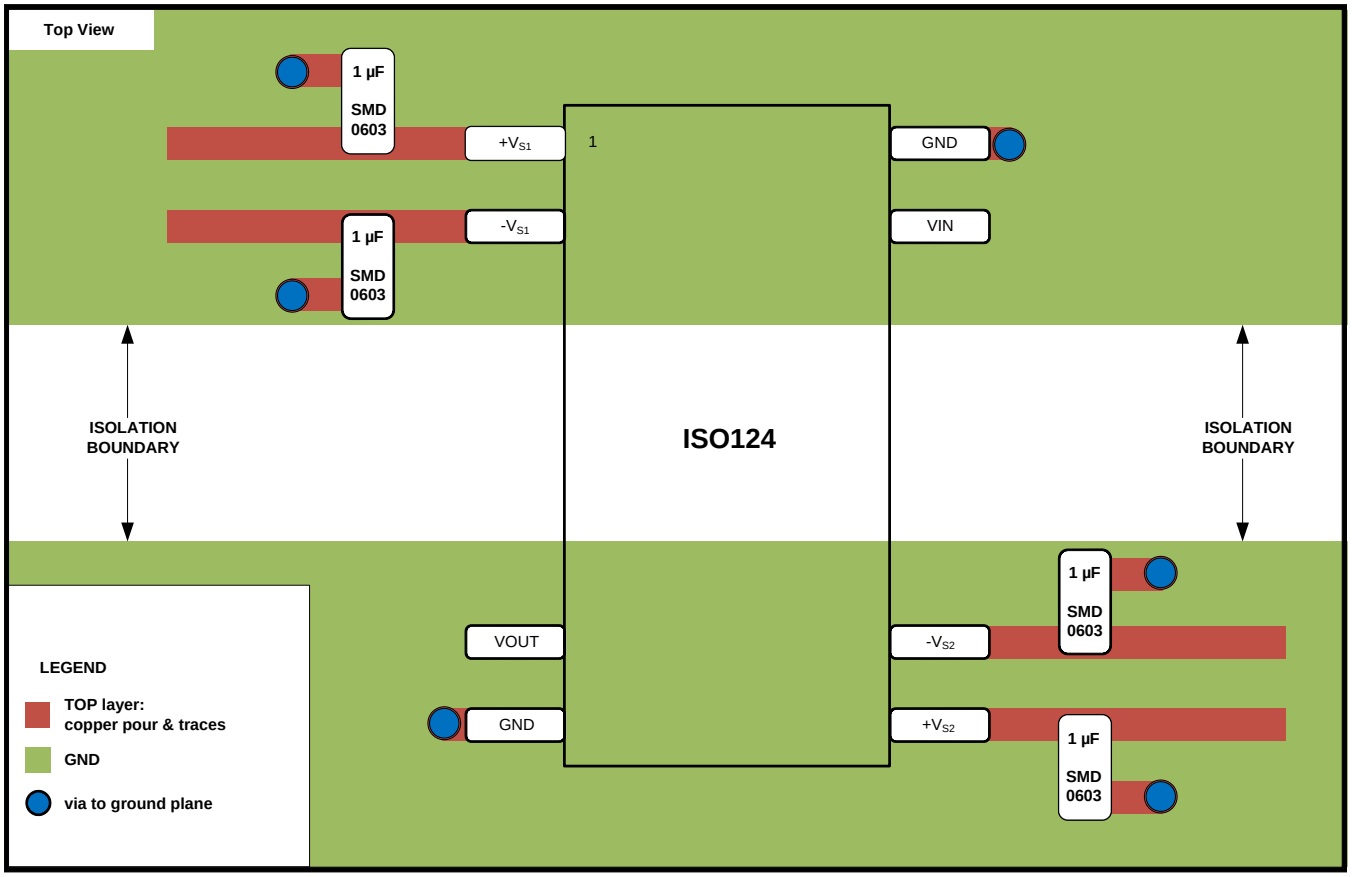


Figure 25. ISO124 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *Single-Supply Operation of Isolation Amplifiers*.
- *Simple Output Filter Eliminates ISO Amp Output Ripple and Keeps Full Bandwidth*.
- *FilterPro™ User's Guide*.

12.2 Trademarks

FilterPro is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO124P	ACTIVE	PDIP	NVF	8	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	ISO124P	Samples
ISO124U	ACTIVE	SOIC	DVA	8	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	Samples
ISO124U/1K	ACTIVE	SOIC	DVA	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	Samples
ISO124U/1KE4	ACTIVE	SOIC	DVA	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	Samples
ISO124UE4	ACTIVE	SOIC	DVA	8	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

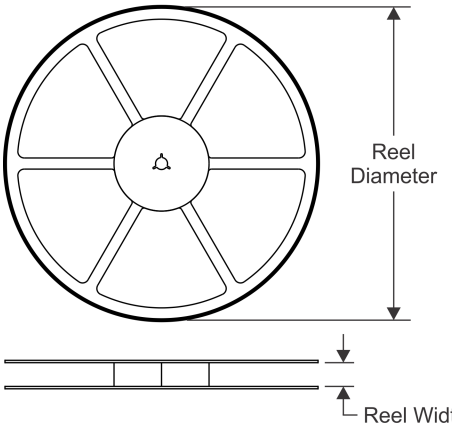
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

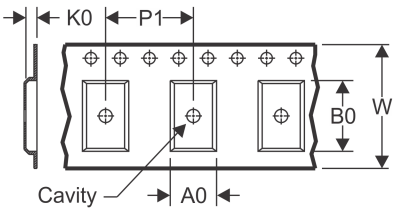
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

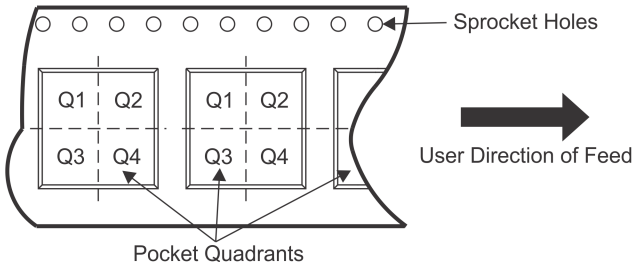


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

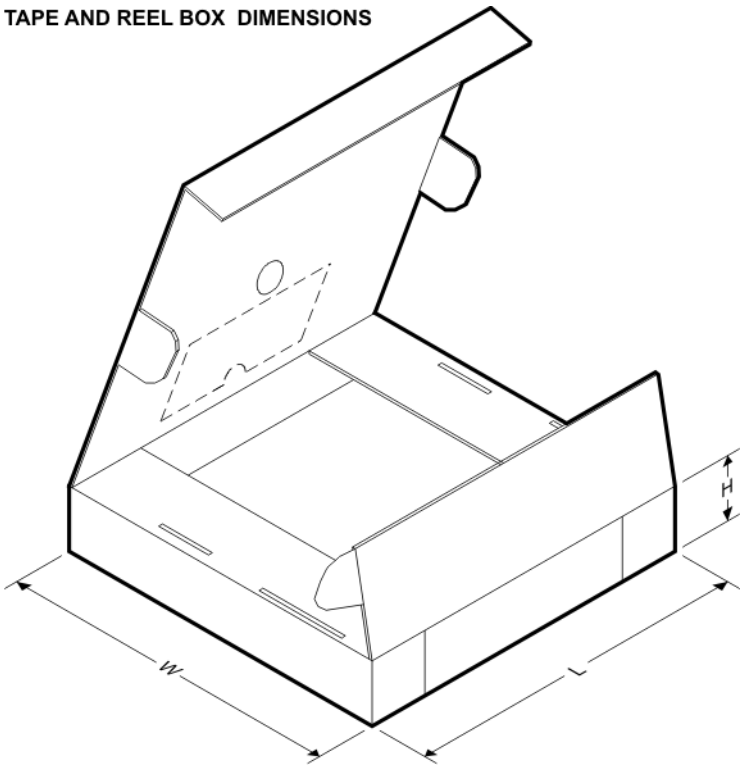
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO124U/1K	SOIC	DVA	8	1000	330.0	24.4	1.11	2.1	0.56	2.0	8.0	Q1

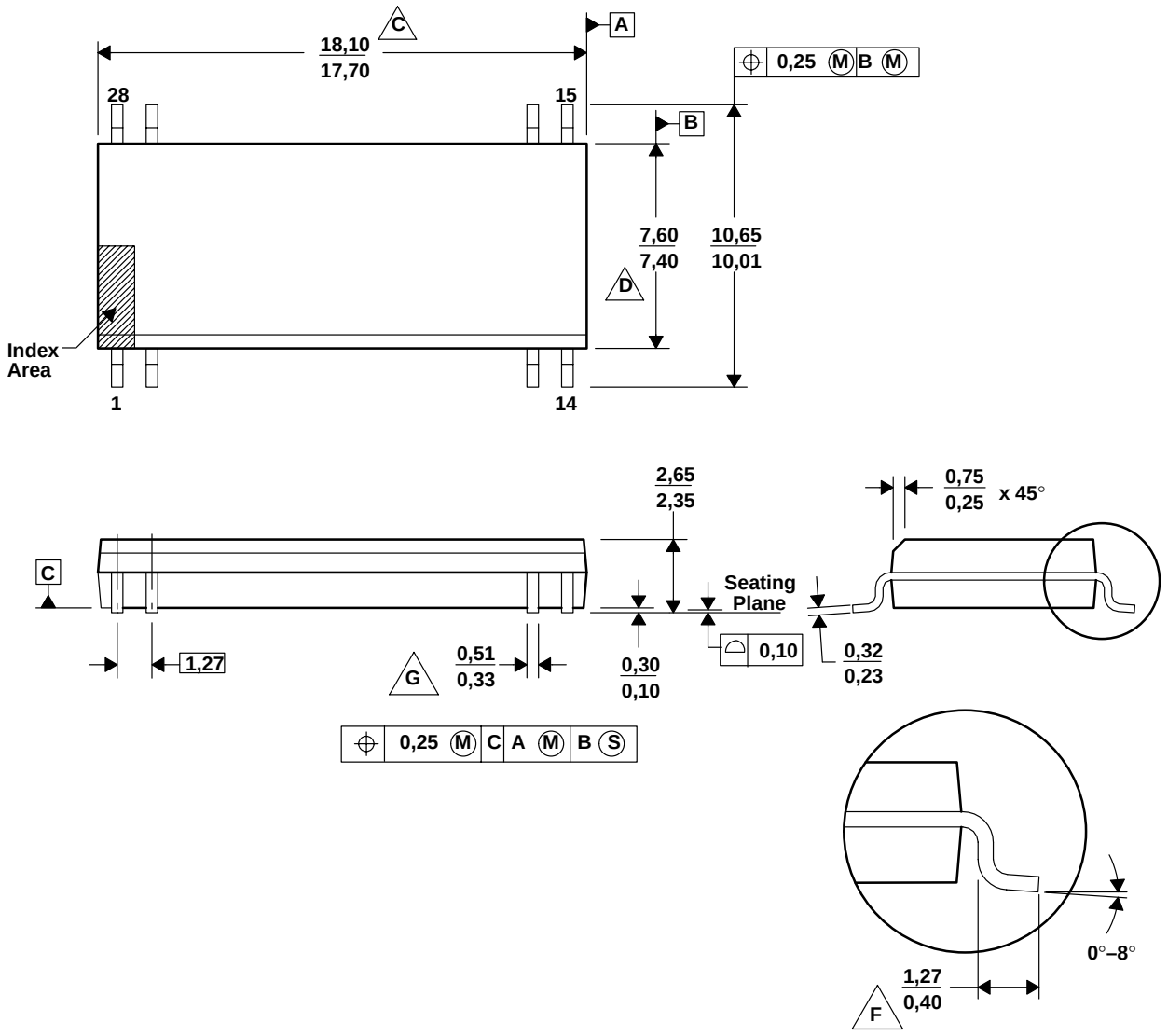
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO124U/1K	SOIC	DVA	8	1000	367.0	367.0	45.0

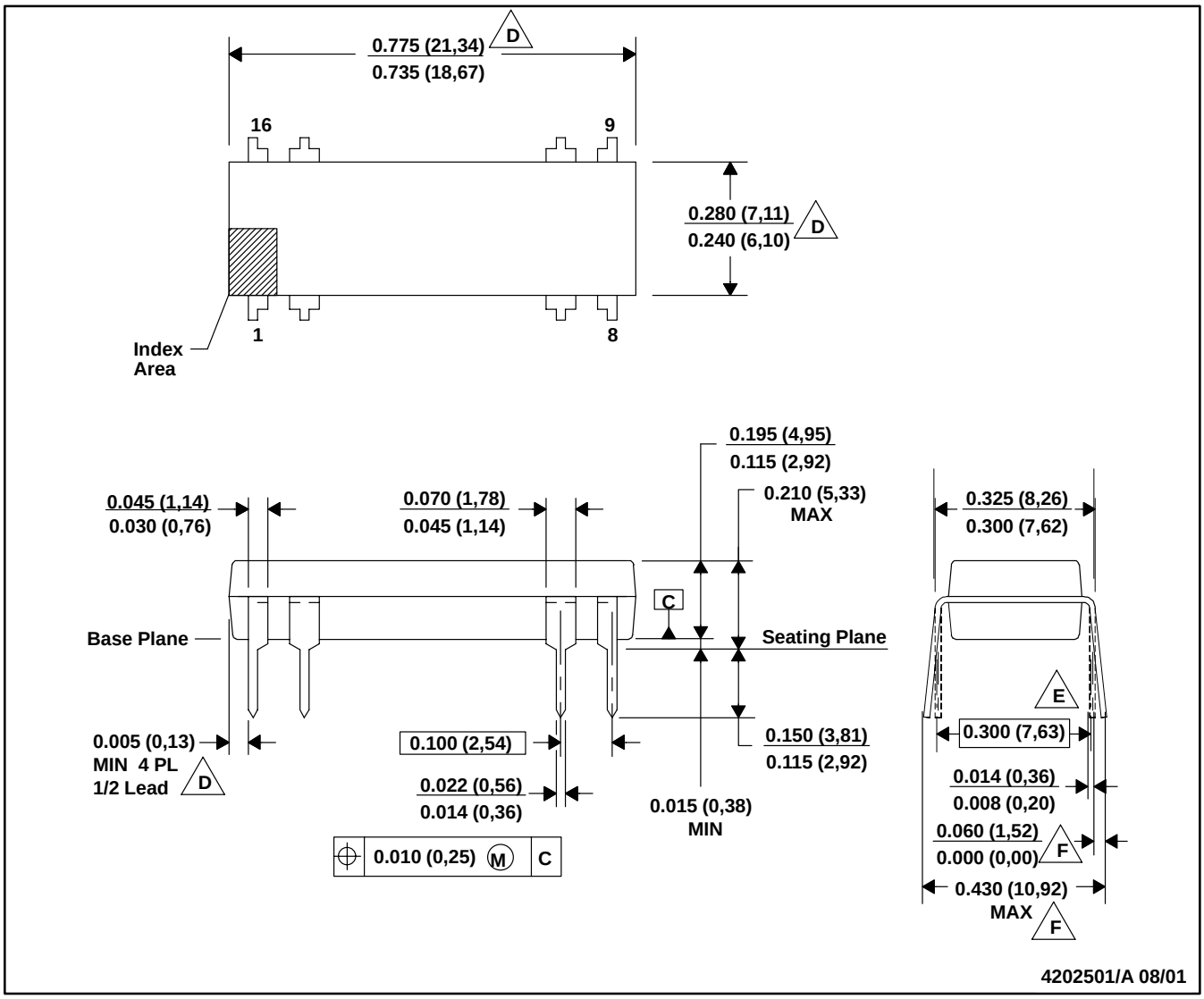
DVA (R-PDSO-G8/28) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

MPDI072 – AUGUST 2001

NVF (R-PDIP-T8/16) **PLASTIC DUAL-IN-LINE**



A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-BB with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

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November 2014

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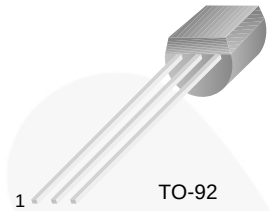
NPN Epitaxial Silicon Transistor

Features

- Switching and Amplifier
- High-Voltage: BC546, V_{CEO} = 65 V
- Low-Noise: BC549, BC550
- Complement to BC556, BC557, BC558, BC559, and BC560



TO-92

1. Collector 2. Base 3. Emitter

Ordering Information

Part Number	Marking	Package	Packing Method
BC546ABU	BC546A	TO-92 3L	Bulk
BC546ATA	BC546A	TO-92 3L	Ammo
BC546BTA	BC546B	TO-92 3L	Ammo
BC546BTF	BC546B	TO-92 3L	Tape and Reel
BC546CTA	BC546C	TO-92 3L	Ammo
BC547ATA	BC547A	TO-92 3L	Ammo
BC547B	BC547B	TO-92 3L	Bulk
BC547BBU	BC547B	TO-92 3L	Bulk
BC547BTA	BC547B	TO-92 3L	Ammo
BC547BTF	BC547B	TO-92 3L	Tape and Reel
BC547CBU	BC547C	TO-92 3L	Bulk
BC547CTA	BC547C	TO-92 3L	Ammo
BC547CTFR	BC547C	TO-92 3L	Tape and Reel
BC548BU	BC548	TO-92 3L	Bulk
BC548BTA	BC548B	TO-92 3L	Ammo
BC548CTA	BC548C	TO-92 3L	Ammo
BC549BTA	BC549B	TO-92 3L	Ammo
BC549BTF	BC549B	TO-92 3L	Tape and Reel
BC549CTA	BC549C	TO-92 3L	Ammo
BC550CBU	BC550C	TO-92 3L	Bulk
BC550CTA	BC550C	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{CBO}	Collector-Base Voltage	BC546	80	V
		BC547 / BC550	50	
		BC548 / BC549	30	
V_{CEO}	Collector-Emitter Voltage	BC546	65	V
		BC547 / BC550	45	
		BC548 / BC549	30	
V_{EBO}	Emitter-Base Voltage	BC546 / BC547	6	V
		BC548 / BC549 / BC550	5	
I_C	Collector Current (DC)		100	mA
P_C	Collector Power Dissipation		500	mW
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-Off Current		V_{CB} = 30 V, I_E = 0			15	nA
h_{FE}	DC Current Gain		V_{CE} = 5 V, I_C = 2 mA	110		800	
V_{CE}(sat)	Collector-Emitter Saturation Voltage		I_C = 10 mA, I_B = 0.5 mA		90	250	mV
			I_C = 100 mA, I_B = 5 mA		250	600	
V_{BE}(sat)	Base-Emitter Saturation Voltage		I_C = 10 mA, I_B = 0.5 mA		700		mV
			I_C = 100 mA, I_B = 5 mA		900		
V_{BE}(on)	Base-Emitter On Voltage		V_{CE} = 5 V, I_C = 2 mA	580	660	700	mV
			V_{CE} = 5 V, I_C = 10 mA			720	
f_T	Current Gain Bandwidth Product		V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		300		MHz
C_{ob}	Output Capacitance		V_{CB} = 10 V, I_E = 0, f = 1 MHz		3.5	6.0	pF
C_{ib}	Input Capacitance		V_{EB} = 0.5 V, I_C = 0, f = 1 MHz		9		pF
NF	Noise Figure	BC546 / BC547 / BC548	V_{CE} = 5 V, I_C = 200 μA, f = 1 kHz, R_G = 2 kΩ		2.0	10.0	dB
		BC549 / BC550			1.2	4.0	
		BC549	V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 30 to 15000 MHz		1.4	4.0	
		BC550			1.4	3.0	

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

Typical Performance Characteristics

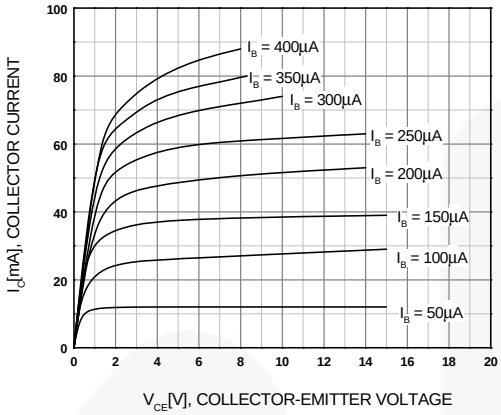


Figure 1. Static Characteristic

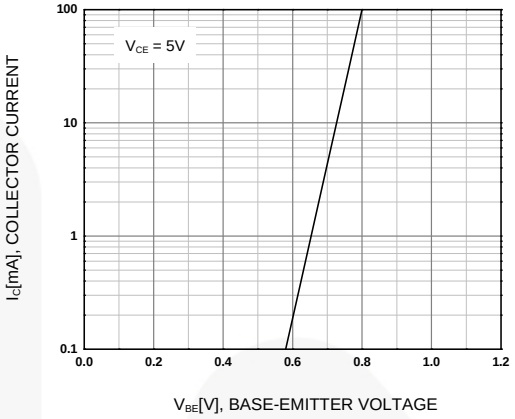


Figure 2. Transfer Characteristic

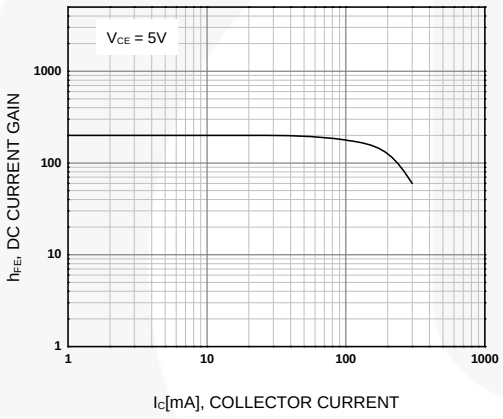


Figure 3. DC Current Gain

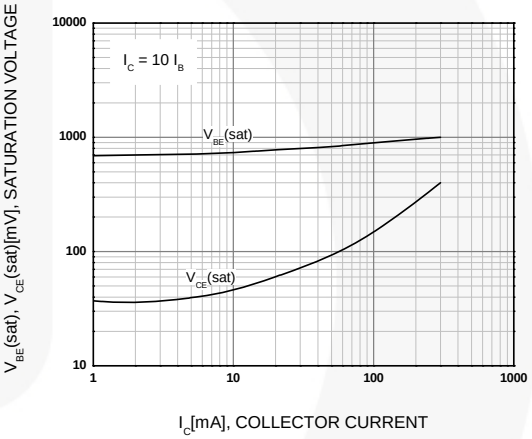


Figure 4. Base-Emitter Saturation Voltage and Collector-Emitter Saturation Voltage

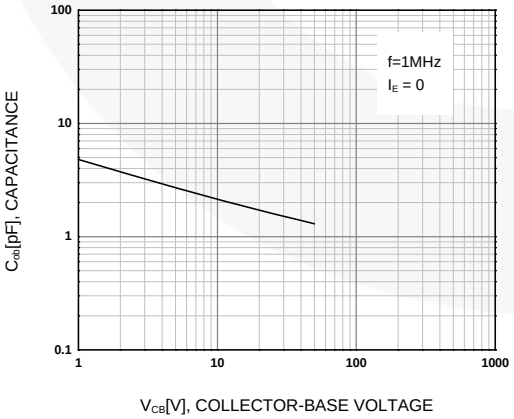


Figure 5. Output Capacitance

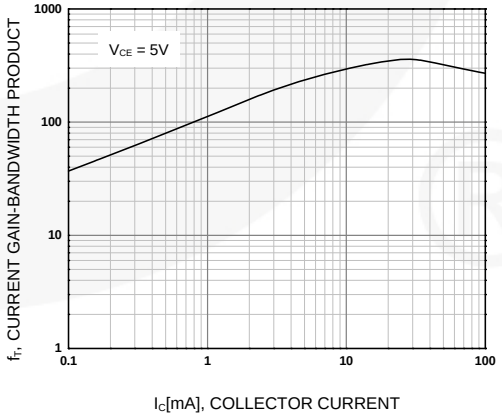
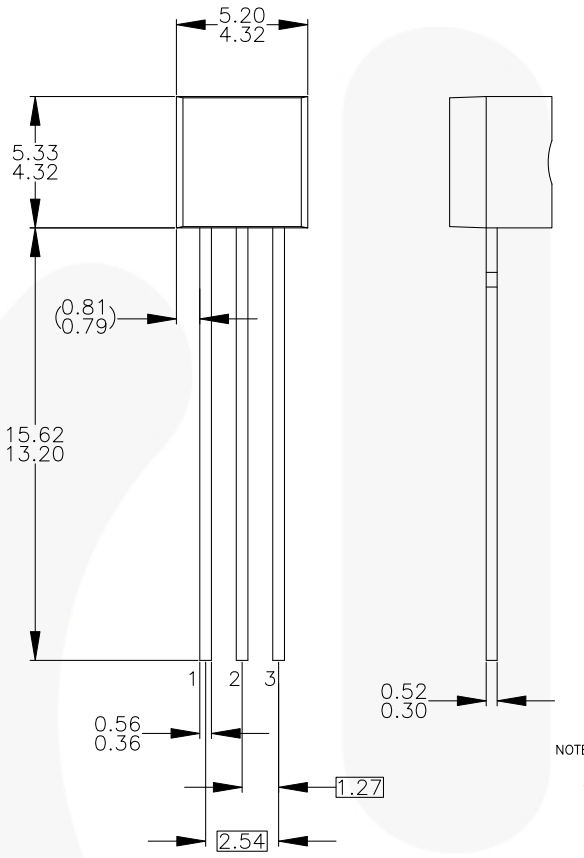


Figure 6. Current Gain Bandwidth Product

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 7. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration, Bulk Type

Physical Dimensions (Continued)

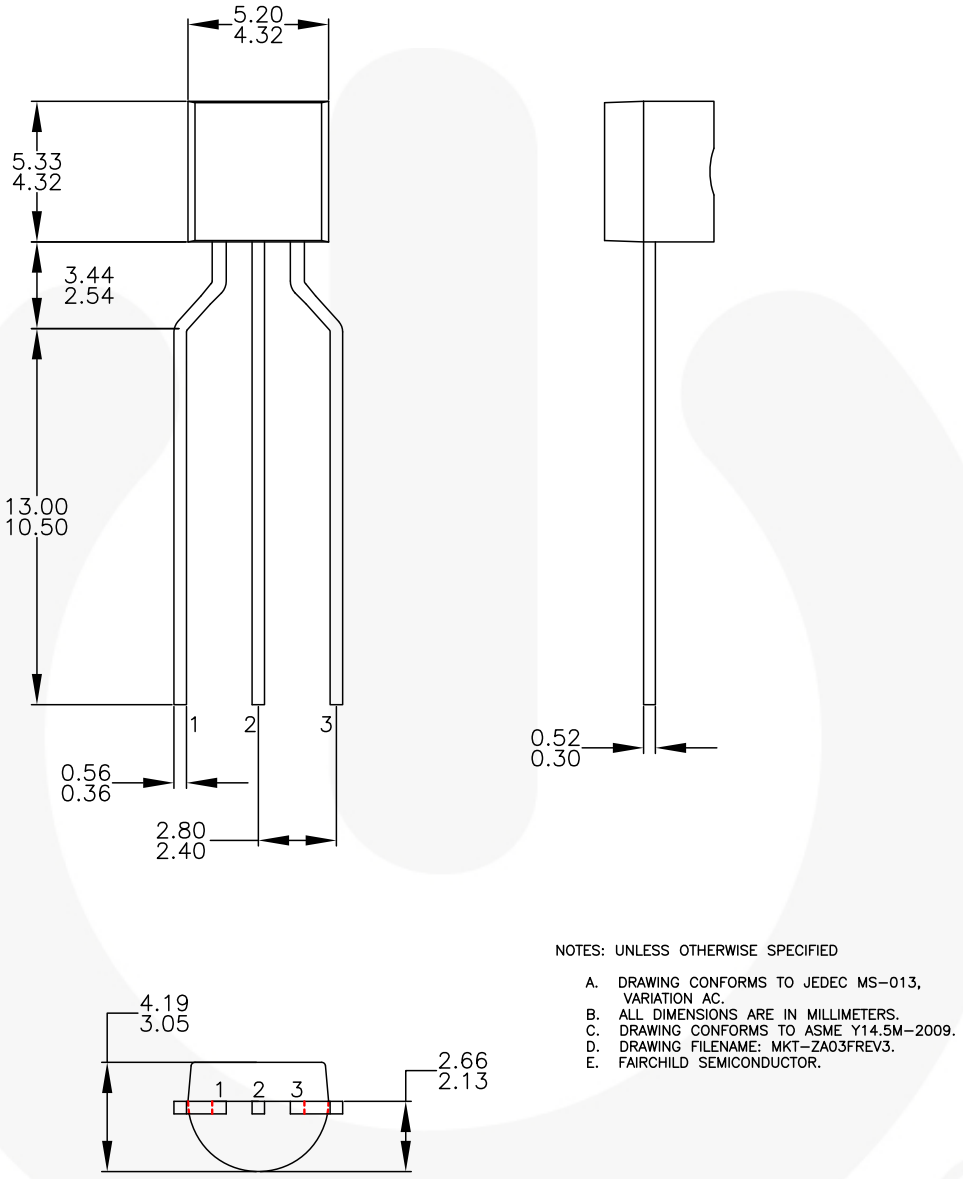


Figure 8. 3-Lead, TO-92, Molded, 0.2 In Line Spacing Lead Form, Ammo, Tape and Reel Type

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I72

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1N4099 THRU 1N4135

SILICON ZENER DIODE
LOW NOISE
6.8 VOLT THRU 100 VOLT
250mW, 5% TOLERANCE

DO-35 CASE

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR 1N4099 series silicon Zener diode is designed for low leakage, low current, and low noise applications.

MARKING: FULL PART NUMBER

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Power Dissipation	P_D	250	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS: (T_A=25°C) V_F=1.1V MAX @ I_F=200mA (for all types)

TYPE	ZENER VOLTAGE V_Z @ I_{ZT}			TEST CURRENT	MAXIMUM ZENER IMPEDANCE	MAXIMUM REVERSE CURRENT		MAXIMUM ZENER CURRENT	MAXIMUM NOISE DENSITY
	MIN	NOM	MAX	I_{ZT}	Z_{ZT} @ I_{ZT}	I_R @ V_R		I_{ZM}	N_D @ 250µA
	V	V	V	µA	Ω	µA	V	mA	µV/√Hz
1N4099	6.460	6.8	7.140	250	200	10	5.2	35.0	40
1N4100	7.125	7.5	7.875	250	200	10	5.7	31.8	40
1N4101	7.790	8.2	8.610	250	200	1.0	6.3	29.0	40
1N4102	8.265	8.7	9.135	250	200	1.0	6.7	27.4	40
1N4103	8.645	9.1	9.555	250	200	1.0	7.0	26.2	40
1N4104	9.50	10	10.50	250	200	1.0	7.6	24.8	40
1N4105	10.45	11	11.55	250	200	0.05	8.5	21.6	40
1N4106	11.40	12	12.60	250	200	0.05	9.2	20.4	40
1N4107	12.35	13	13.65	250	200	0.05	9.9	19.0	40
1N4108	13.30	14	14.70	250	200	0.05	10.7	17.5	40
1N4109	14.25	15	15.75	250	100	0.05	11.4	16.3	40
1N4110	15.20	16	16.80	250	100	0.05	12.2	15.4	40
1N4111	16.15	17	17.85	250	100	0.05	13.0	14.5	40
1N4112	17.10	18	18.90	250	100	0.05	13.7	13.2	40
1N4113	18.05	19	19.95	250	150	0.05	14.5	12.5	40
1N4114	19.00	20	21.00	250	150	0.01	15.2	11.9	40
1N4115	20.90	22	23.10	250	150	0.01	16.8	10.8	40
1N4116	22.80	24	25.20	250	150	0.01	18.3	9.9	40
1N4117	23.75	25	26.25	250	150	0.01	19.0	9.5	40
1N4118	25.65	27	28.35	250	150	0.01	20.5	8.8	40
1N4119	26.60	28	29.40	250	200	0.01	21.3	8.5	40
1N4120	28.50	30	31.50	250	200	0.01	22.8	7.9	40
1N4121	31.35	33	34.65	250	200	0.01	25.1	7.2	40

R1 (4-February 2014)

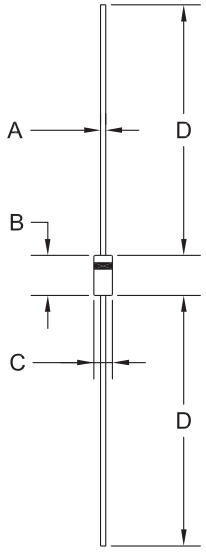
1N4099 THRU 1N4135

SILICON ZENER DIODE
LOW NOISE
6.8 VOLT THRU 100 VOLT
250mW, 5% TOLERANCE

ELECTRICAL CHARACTERISTICS - Continued: (T_A=25°C) V_F=1.1V MAX @ I_F=200mA (for all types)

TYPE	ZENER VOLTAGE V_Z @ I_{ZT}			TEST CURRENT	MAXIMUM ZENER IMPEDANCE	MAXIMUM REVERSE CURRENT		MAXIMUM ZENER CURRENT	MAXIMUM NOISE DENSITY
	MIN	NOM	MAX	I_{ZT}	Z_{ZT} @ I_{ZT}	I_R @ V_R		I_{ZM}	N_D @ 250µA
	V	V	V	µA	Ω	µA	V	mA	µV/√Hz
1N4122	34.20	36	37.80	250	200	0.01	27.4	6.6	40
1N4123	37.05	39	40.95	250	200	0.01	29.7	6.1	40
1N4124	40.85	43	45.15	250	250	0.01	32.7	5.5	40
1N4125	44.65	47	49.35	250	250	0.01	35.8	5.1	40
1N4126	48.45	51	53.55	250	300	0.01	38.8	4.6	40
1N4127	53.20	56	58.80	250	300	0.01	42.6	4.2	40
1N4128	57.00	60	63.00	250	400	0.01	45.6	4.0	40
1N4129	58.90	62	65.10	250	500	0.01	47.1	3.8	40
1N4130	64.60	68	71.40	250	700	0.01	51.7	3.5	40
1N4131	71.25	75	78.75	250	700	0.01	57.0	3.1	40
1N4132	77.90	82	86.10	250	800	0.01	62.4	2.9	40
1N4133	82.65	87	91.35	250	1.0K	0.01	66.2	2.7	40
1N4134	86.45	91	95.55	250	1.2K	0.01	69.2	2.6	40
1N4135	95.00	100	105.0	250	1.5K	0.01	76.0	2.3	40

DO-35 CASE - MECHANICAL OUTLINE



R1

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.018	0.022	0.46	0.56
B	0.120	0.200	3.05	5.08
C	0.060	0.090	1.52	2.29
D	1.000	-	25.40	-

DO-35 (REV: R1)

MARKING: FULL PART NUMBER

R1 (4-February 2014)

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PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
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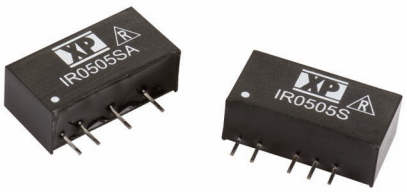
3 Watts
IR Series



- Single & Dual Output
- SIP Package
- 1000 VDC Isolation
- Optional 3000 VDC Isolation
- –40 °C to +85 °C Operation
- Semi–regulated
- 3 Year Warranty

Specification

Input

Input Voltage Range	• Nominal ±10%
Input Reflected Ripple Current	• 20 mA pk-pk, 5 Hz to 20 MHz
Input Reverse Voltage Protection	• None

Output

Output Voltage	• See table
Minimum Load	• None[1]
Line Regulation	• 1.2%/1% Δ Vin
Load Regulation	• See table
Setpoint Accuracy	• +2%, -4%
Ripple & Noise	• 50 mV pk-pk max, 20 MHz bandwidth[2]
Temperature Coefficient	• 0.02%/°C
Maximum Capacitive Load	• See table

General

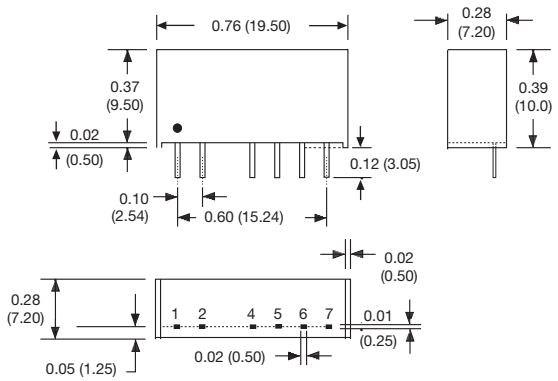
Efficiency	• See table
Isolation Voltage	• 1000 VDC minimum, 3000 VDC option[3]
Isolation Resistance	• $10^9\Omega$
Isolation Capacitance	• 60 pF typical
Switching Frequency	• Variable, 60 kHz - 85 kHz
MTBF	• >1.1 MHrs to MIL-HDBK-217F at 25 °C, GB

Environmental

Operating Temperature	• -40 °C to +85 °C
Storage Temperature	• -40 °C to +125 °C
Case Temperature	• 100 °C max
Cooling	• Convection-cooled

Input Voltage	No Load Input Current	Output Voltage	Output Current	Max Capacitive Load	Efficiency	Load Reg.	Model Number
5 VDC	80 mA	5.0 V	600 mA	220 µF	79%	8.0%	IR0505SA
	70 mA	9.0 V	333 mA	220 µF	84%	7.0%	IR0509SA
	70 mA	12.0 V	250 mA	100 µF	84%	6.0%	IR0512SA
	80 mA	15.0 V	200 mA	100 µF	84%	6.0%	IR0515SA
	80 mA	±5.0 V	±300 mA	±100 µF	82%	7.0%	IR0505S
	70 mA	±9.0 V	±167 mA	±100 µF	85%	6.0%	IR0509S
	70 mA	±12.0 V	±125 mA	±47 µF	85%	6.0%	IR0512S
	70 mA	±15.0 V	±100 mA	±47 µF	86%	5.0%	IR0515S
12 VDC	25 mA	5.0 V	600 mA	220 µF	84%	6.0%	IR1205SA
	25 mA	9.0 V	333 mA	220 µF	87%	4.0%	IR1209SA
	25 mA	12.0 V	250 mA	100 µF	88%	4.0%	IR1212SA
	20 mA	15.0 V	200 mA	100 µF	90%	3.0%	IR1215SA
	25 mA	±5.0 V	±300 mA	±100 µF	85%	5.0%	IR1205S
	25 mA	±9.0 V	±167 mA	±100 µF	88%	4.0%	IR1209S
	25 mA	±12.0 V	±125 mA	±47 µF	89%	3.0%	IR1212S
	20 mA	±15.0 V	±100 mA	±47 µF	90%	3.0%	IR1215S

Mechanical Details



Notes

1. Operation at no load will not damage unit but it may not meet all specifications.
2. Output capacitor of 1 µF required to meet quoted ripple and noise.
3. For optional 3 kV isolation, add suffix '-H' to the model number.
4. All dimensions in inches (mm).
5. Pin pitch tolerance: ±0.014 (±0.35)
6. Case tolerance: ±0.02 (±0.5)
7. Weight: 0.006 lbs (2.8 g)

Pin Connections				
Pin	Single	Dual	Single-H	Dual-H
1	+Vin	+Vin	+Vin	+Vin
2	-Vin	-Vin	-Vin	-Vin
4	-Vout	-Vout	N.P	N.P
5	N.P	Common	-Vout	-Vout
6	+Vout	+Vout	N.P	Common
7	N.P	N.P	+Vout	+Vout

Heatsink

Description:

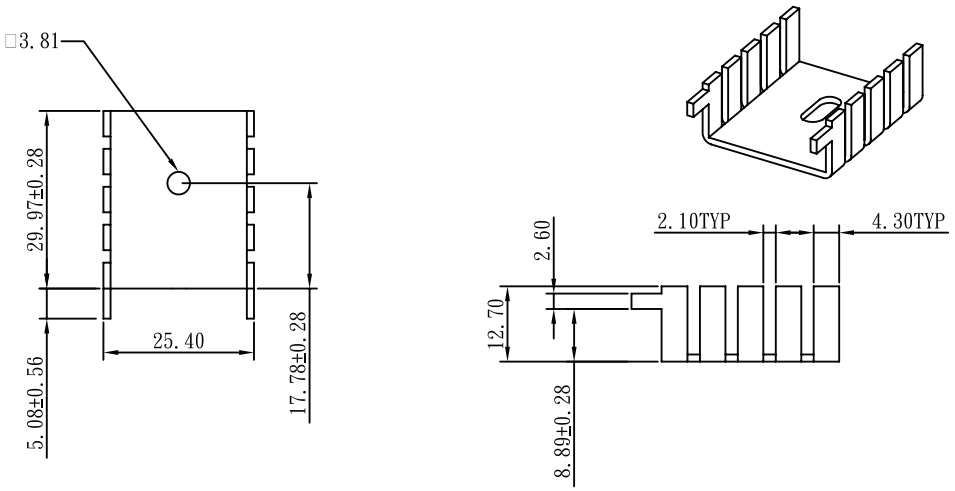
Heatsink with a slotted hole for a single SOT-23/TO-126 package. With integral fixing tags.

Features:

- Low cost stamped heatsink
- Black anodize finish

Specifications:

Thermal Resistance	: 13.6°C/W
External Height	: 12.7mm
External Width	: 25.4mm
External Length	: 30mm
Heat Sink Material	: Aluminium
Mounting Type	: Vert. / Horiz. with slotted mounting hole



Dimensions : Millimetres

Part Number Table

Description	Part Number
Heatsink SOT-23/126 17°C/W	MC33260

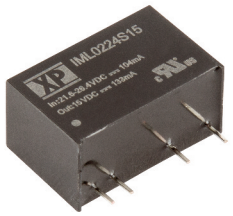
IML02 Series

DC-DC Converter

XP Power

2 Watts

- World Wide Medical Approvals
- Single and Dual Outputs
- SIP7 Package
- -40 °C to +85 °C Operation
- Full Load at 85 °C Ambient
- 4000 VAC Isolation, 1 x MOPP at 250 VAC
- 2 µA Patient Leakage Current
- MTBF 2.5 MHrs
- 3 Year Warranty



Dimensions:

IML02:
0.77 x 0.39 x 0.49" (19.5 x 9.8 x 12.5 mm)

Models & Ratings

Input Voltage	Output Voltage	Output Current	Input current		Max. capacitive load	Efficiency	Model Number
			No Load	Full Load			
4.5-5.5 V	3V3	600 mA	50 mA	533 mA	1000 µF	75%	IML0205S3V3
	5 V	400 mA	60 mA	533 mA	470 µF	78%	IML0205S05
	9 V	222 mA	60 mA	500 mA	470 µF	80%	IML0205S09
	12 V	167 mA	60 mA	482 mA	220 µF	83%	IML0205S12
	15 V	133 mA	60 mA	488 mA	220 µF	82%	IML0205S15
	±3V3	±300 mA	50 mA	519 mA	±470 µF	77%	IML0205D03
	±5 V	±200 mA	60 mA	513 mA	±220 µF	78%	IML0205D05
	±9 V	±111 mA	60 mA	500 mA	±220 µF	80%	IML0205D09
	±12 V	±83 mA	60 mA	482 mA	±100 µF	83%	IML0205D12
	±15 V	±66 mA	60 mA	488 mA	±100 µF	82%	IML0205D15
10.8-13.2 V	3V3	600 mA	25 mA	217 mA	1000 µF	76%	IML0212S3V3
	5 V	400 mA	30 mA	208 mA	470 µF	80%	IML0212S05
	9 V	222 mA	30 mA	208 mA	470 µF	80%	IML0212S09
	12 V	167 mA	30 mA	200 mA	220 µF	83%	IML0212S12
	15 V	133 mA	30 mA	203 mA	220 µF	82%	IML0212S15
	±3V3	±300 mA	25 mA	214 mA	±470 µF	78%	IML0212D03
	±5 V	±200 mA	30 mA	208 mA	±220 µF	80%	IML0212D05
	±9 V	±111 mA	30 mA	208 mA	±220 µF	80%	IML0212D09
	±12 V	±83 mA	30 mA	200 mA	±100 µF	83%	IML0212D12
	±15 V	±66 mA	30 mA	203 mA	±100 µF	82%	IML0212D15
13.5-16.5V	3V3	600 mA	25 mA	174 mA	1000 µF	76%	IML0215S3V3
	5 V	400 mA	30 mA	170 mA	470 µF	78%	IML0215S05
	9 V	222 mA	30 mA	167 mA	470 µF	80%	IML0215S09
	12 V	167 mA	30 mA	167 mA	220 µF	80%	IML0215S12
	15 V	133 mA	30 mA	167 mA	220 µF	80%	IML0215S15
	±3V3	±300 mA	25 mA	170 mA	±470 µF	78%	IML0215D03
	±5 V	±200 mA	30 mA	170 mA	±220 µF	78%	IML0215D05
	±9 V	±111 mA	30 mA	167 mA	±220 µF	80%	IML0215D09
	±12 V	±83 mA	30 mA	167 mA	±100 µF	80%	IML0215D12
	±15 V	±66 mA	30 mA	167 mA	±100 µF	80%	IML0215D15
21.6-26.4V	3V3	600 mA	20 mA	111 mA	1000 µF	75%	IML0224S3V3
	5 V	400 mA	20 mA	106 mA	470 µF	78%	IML0224S05
	9 V	222 mA	20 mA	104 mA	470 µF	80%	IML0224S09
	12 V	167 mA	20 mA	104 mA	220 µF	80%	IML0224S12
	15 V	133 mA	20 mA	104 mA	220 µF	80%	IML0224S15
	±3V3	±300 mA	20 mA	107 mA	±470 µF	77%	IML0224D03
	±5 V	±200 mA	20 mA	106 mA	±220 µF	78%	IML0224D05
	±9 V	±111 mA	20 mA	104 mA	±220 µF	80%	IML0224D09
	±12 V	±83 mA	20 mA	104 mA	±100 µF	80%	IML0224D12
	±15 V	±66 mA	20 mA	104 mA	±100 µF	80%	IML0224D15

Notes

Input currents measured at nominal input voltage.

Input

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Input Voltage Range	4.5		5.5	VDC	5 V nominal
	10.8		13.2		12 V nominal
	13.5		16.5		15 V nominal
	21.6		26.4		24 V nominal
Input Reflected Ripple Current		20		mA pk-pk	Through 12 µH inductor and 47 µF capacitor
Input Surge			5.5	VDC for 100 ms	5 V models
			13.2		12 V models
			16.5		15 V nominal
			26.4		24 V nominal

Output

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Output Voltage	3.3		30	VDC	See Models and Ratings table
Initial Set Accuracy			±5	%	At full load
Minimum Load	10			%	Minimum load required to meet specified regulation
Line Regulation			±1.2	%/1%	Output changes by max of 1.2% for each 1% change in input voltage
Load Regulation			10	%	From 10% to full load, see application note
Cross Regulation		±4		%	On dual output models, when one output is at 25% load and other is varied from 10% load to full load
Ripple & Noise			150	mV pk-pk	20 MHz bandwidth. Measured using 10 µF electrolytic in parallel with 0.1 µF ceramic capacitor
Short Circuit Protection					Continuous
Maximum Capacitive Load					See Models and Ratings table
Temperature Coefficient			0.03	%/°C	

General

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Efficiency		80		%	
Isolation: Input to Output	4000			VAC	1 x MOPP at 250 VAC working voltage, 2 x MOPP at 125 VAC working voltage
Patient Leakage Current			2	µA	
Isolation Resistance	10^9			Ω	
Isolation Capacitance		10	20	pF	
Switching Frequency	50		100	kHz	
Power Density			13.6	W/in^3	
Mean Time Between Failure	2.5			MHrs	MIL-HDBK-217F, +25 °C GB
Weight		0.009 (4.2)		lb (g)	

Environmental

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Operating Temperature	-40		+85	°C	No derating
Storage Temperature	-40		+125	°C	
Case Temperature			+100	°C	
Humidity	2.5		95	%RH	Non-condensing
Cooling					Natural convection

EMC: Emissions

Phenomenon	Standard	Test Level	Notes & Conditions
Conducted	EN55011	Class B	See Application Note
Radiated	EN55011	Class B	

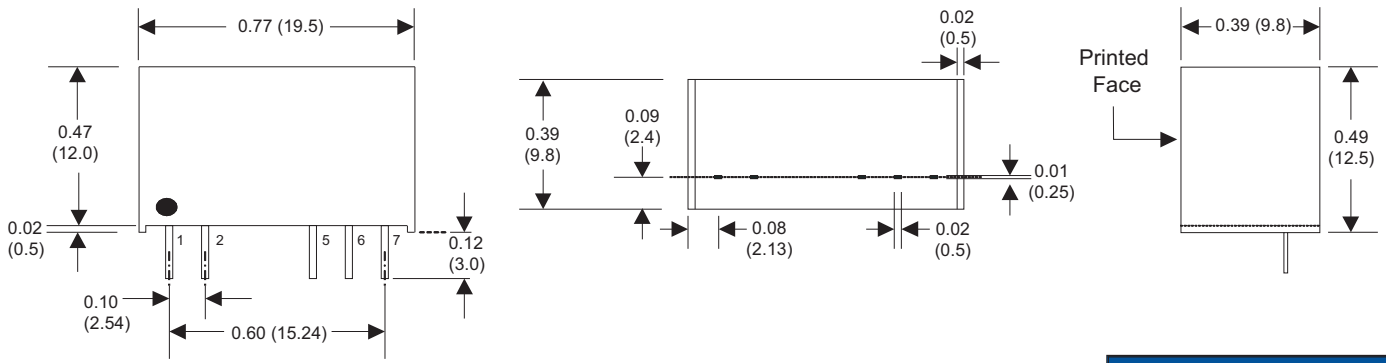
EMC: Immunity

Phenomenon	Standard	Test Level	Criteria	Notes & Conditions
ESD Immunity	EN61000-4-2	±15 kV	A	Air Discharge
Radiated Immunity	EN61000-4-3	10 Vrms	A	
EFT/Burst	EN61000-4-4	2 kV	A	External components required, see application notes
Surge	EN61000-4-5	2 kV	A	External components required, see applications note
Conducted Immunity	EN61000-4-6	10 V rms	A	
Magnetic Fields	EN61000-4-8	30 A/m	A	

Safety Approvals

Safety Agency	Safety Standard	Notes & Conditions
UL	ANSI/AMMI ES60601-1	
CSA	CSA C22.2 No. 60601-1	
TUV	EN60601-1	
CB	IEC60601-1	

Mechanical Details



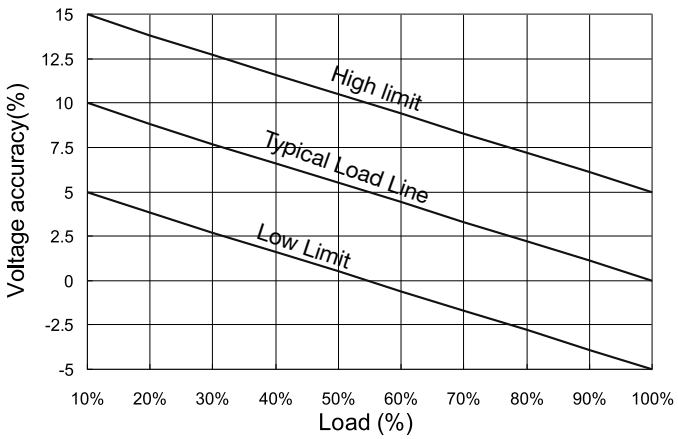
Pin Connections		
Pin	Single	Dual
1	+Vin	+Vin
2	-Vin	-Vin
5	-Vout	-Vout
6	No Pin	Common
7	+Vout	+Vout

Notes

1. All dimensions are in inches (mm)
2. Weight: 0.009 lbs (4.2 g) approx.
3. Pin diameter: 0.02±0.002 (0.5±0.05)
4. Pin pitch tolerance: ±0.014 (±0.35)
5. Case tolerance: ±0.02 (±0.5)

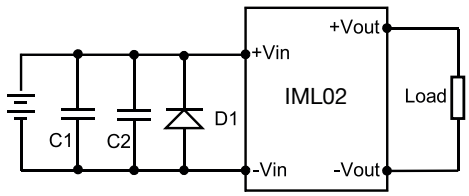
Application Note

Regulation



EFT and Surge Filter

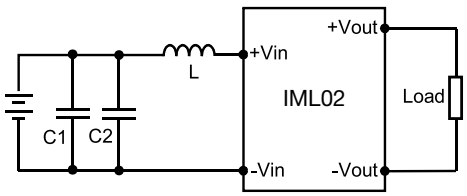
Input components (C1, C2, D1) are used to help meet EFT and surge test requirements for the module.



	C1	C2	D1
IML0205XXXX	1000 µF/35 V	330 µF/50 V	SMDJ9.0A
IML0212XXXX	1000 µF/35 V	330 µF/50 V	SMDJ13A
IML0215XXXX	1000 µF/35 V	330 µF/50 V	SMDJ18A
IML0224XXXX	1000 µF/35 V	330 µF/50 V	SMDJ28A

EMI Filter

Input filter components (C1,C2 and L) are used to help meet conducted emissions requirements for the module. These components should be mounted as close as possible to the module, and all leads should be minimised to decrease radiated noise.



	C1	C2	L
IML0205XXXX	1206, 4.7 µF/ 50 V		6.8 µH
IML0212XXXX	1206, 4.7 µF/ 50 V	1206, 4.7 µF/ 50 V	6.8 µH
IML0215XXXX	1206, 4.7 µF/ 50 V	1206, 4.7 µF/ 50 V	6.8 µH
IML0224XXXX	1206, 4.7 µF/ 50 V	1206, 4.7 µF/ 50 V	6.8 µH

Miniature PCB Relay PCJ

- **1pole 3A/5A, 1 form A (NO) contact**
- **Sensitive coil 200mW**
- **Ambient temperature 85°C**
- **RoHS compliant (Directive 2002/95/EC)**
- **WG version : Product in accordance to IEC60335-1**

F0276-C

Typical applications
Home appliances

Approvals

VDE 40009151, UL E58304, CSA LR48471-211, CQC 03001008593
Technical data of approved types on request

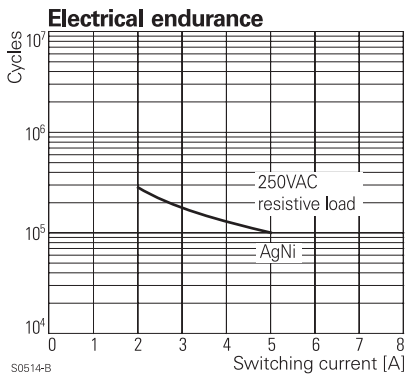
Contact Data

Contact arrangement	1 form A (NO)
Rated voltage	250VAC
Max. switching voltage	30VDC, 250VAC
Rated current	3A/5A
Switching power	1,250VA, 150W
Contact material	AgNi
Min. recommended contact load	100mA, 5VDC
Initial contact resistance	100mΩ at 1A, 6VDC
Frequency of operation, with/without load	1800/18000h^{-1}
Operate/release time max.	10/4ms
Electrical endurance	
3A version: 250VAC, resistive,	100x10^3 ops.
5A version: 250VAC, resistive,	100x10^3 ops.

Contact ratings

Type	Contact	Load	Cycles
IEC 61810			
PCJ	form A (NO)	5A,250VAC, cosφ=1, 85°C	100x10^3
PCJ	form A (NO)	2A,250VAC, cosφ=0.6 85°C	100x10^3
PCJ	form A (NO)	3A,250VAC, cosφ=1, 105°C	100x10^3
UL 508			
PCJ	form A (NO)	5A,250VAC, general use, 85°C	6x10^3
PCJ	form A (NO)	3A,250VAC, cosφ=1, 85°C	100x10^3
PCJ	form A (NO)	3A,250VAC, cosφ=1, 105°C	100x10^3

Mechanical endurance >10x10^6 operations



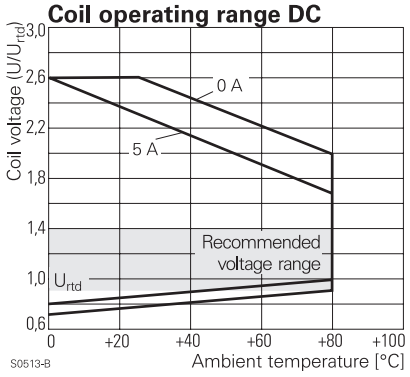
Coil Data

Coil voltage range	3 to 24VDC
Coil insulation system according UL	
Standard Version:	class 105 (A)
WG version:	class 155 (F)

Coil versions, DC coil

Coil code	Rated voltage VDC	Operate voltage VDC	Release voltage VDC	Coil resistance Ω±10%	Rated coil power mW
03	3	2.25	0.15	45	200
05	4	3.75	0.25	125	200
06	6	4.50	0.3	180	200
09	9	6.75	0.45	405	200
12	12	9.00	0.6	720	200
18	18	13.50	0.9	1620	200
24	24	18.00	1.2	2880	200

All figures are given for coil without pre-energization, at ambient temperature +23°C.



Insulation Data

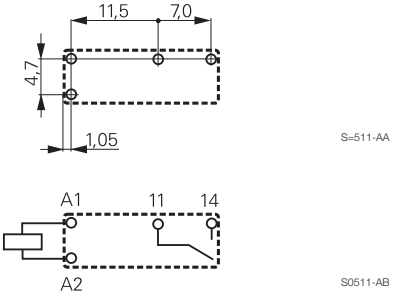
Initial dielectric strength	
between open contacts	750V$_{rms}$
between contact and coil	4000V$_{rms}$
Initial surge withstand voltage	
between contact and coil	10000V$_{rms}$
Initial insulation resistance	1000MΩ
Clearance/creepage	
between contact and coil	≥ 7.5/8mm

Miniature PCB Relay PCJ (Continued)

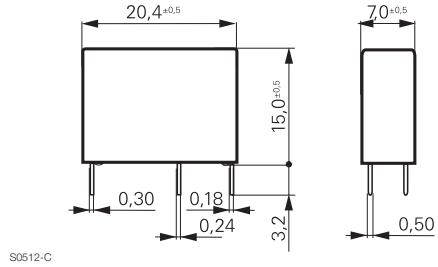
Other Data	
Material compliance: EU RoHS/ELV, China RoHS, REACH, Halogen content refer to the Product Compliance Support Center at www.te.com/customersupport/rohssupportcenter	
Ambient temperature	-40 to 85°C (105°C)
Category of environmental protection	
IEC 61810	RTII - flux proof, RTIII - wash tight
Vibration resistance (functional)	10 to 50Hz, 1.5mm double amplitude
Shock resistance (functional)	
IEC 60068-2-27 (half sine)	98m/s², 11ms
Terminal type	PCB-THT
Weight	4g
Resistance to soldering heat THT	
IEC 60068-2-20	260°C/5s
Packaging/unit	box/1000 pcs.

PCB layout / terminal assignment

Bottom view on solder pins



Dimensions



Product code structure

Typical product code: **PCJ 1 12 D 3 M 301**

Type
- **PCJ** Miniature PCB Relay PCJ

Version
- **1** Single contact

Coil
- Coil code: please refer to coil versions table

Coil power
- **D** Standard 200mW

Contact material
- **3** AgNi

Contact arrangement
- **M** 1 form A (NO) contact

Sealing
- **Blank** Flux proof
- **H** Wash tight*

Suffix
- **301** Standard version
- **WG** Product in accordance with IEC 60335-1 (domestic appliances)*

*) Wash tight WG version on request

Miniature PCB Relay PCJ (Continued)

Product code	Version	Contact	Cont. material	Coil version	Coil	Sealing	Part number
PCJ-103D3M,301	3A	1 form A (NO)	AgNi	200mW	3VDC	Flux proof	1721081-1
PCJ-105D3M,301					5VDC		1721081-2
PCJ-106D3M,301					6VDC		1721081-3
PCJ-109D3M,301					9VDC		1721081-4
PCJ-112D3M,301					12VDC		1721081-5
PCJ-124D3M,301					24VDC		1721081-7
PCJ-103D3MH,301					3VDC	Wash tight	1721081-8
PCJ-105D3MH,301					5VDC		1721081-9
PCJ-106D3MH,301					6VDC		1-1721081-0
PCJ-109D3MH,301					9VDC		1-1721081-1
PCJ-112D3MH,301					12VDC		1-1721081-2
PCJ-124D3MH,301					24VDC		1-1721081-4
PCJ-103D3M-WG	5A				3VDC	Flux proof	1721547-1
PCJ-105D3M-WG					5VDC		1721547-2
PCJ-106D3M-WG					6VDC		1721547-3
PCJ-109D3M-WG					9VDC		1721547-4
PCJ-112D3M-WG					12VDC		1721547-5
PCJ-124D3M-WG					24VDC		1721547-7
PCJ-103D3MH-WG					3VDC	Wash tight	1721547-8
PCJ-105D3MH-WG					5VDC		1721547-9
PCJ-106D3MH-WG					6VDC		1-1721547-0
PCJ-109D3MH-WG					9VDC		1-1721547-1
PCJ-112D3MH-WG					12VDC		1-1721547-2
PCJ-124D3MH-WG					24VDC		1-1721547-4

SR302 THRU SR310

3.0 AMPS. Schottky Barrier Rectifiers

Voltage Range
20 to 100 Volts
Current
3.0 Amperes

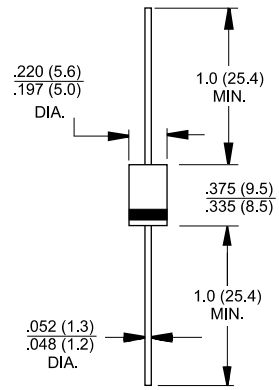
Features

- ✧ Low forward voltage drop
- ✧ High current capability
- ✧ High reliability
- ✧ High surge current capability

Mechanical Data

- ✧ Cases: DO-201AD molded plastic
- ✧ Epoxy: UL 94V-O rate flame retardant
- ✧ Lead: Axial leads, solderable per MIL-STD-202, Method 208 guaranteed
- ✧ Polarity: Color band denotes cathode end
- ✧ High temperature soldering guaranteed: 250°C/10 seconds/.375",(9.5mm) lead lengths at 5 lbs., (2.3kg) tension
- ✧ Weight: 1.1 grams

DO-201AD



Dimensions in inches and (millimeters)

Maximum Ratings and Electrical Characteristics

Rating at 25℃ ambient temperature unless otherwise specified.
Single phase, half wave, 60 Hz, resistive or inductive load.
For capacitive load, derate current by 20%

Type Number	SR302	SR303	SR304	SR305	SR306	SR309	SR310	Units
Maximum Recurrent Peak Reverse Voltage	20	30	40	50	60	90	100	V
Maximum RMS Voltage	14	21	28	35	42	63	70	V
Maximum DC Blocking Voltage	20	30	40	50	60	90	100	V
Maximum Average Forward Rectified Current See Fig. 1	3.0							A
Peak Forward Surge Current, 8.3 ms Single Half Sine-wave Superimposed on Rated Load (JEDEC method)	80					150		A
Maximum Instantaneous Forward Voltage @3.0A	0.55			0.70		0.79		V
Maximum D.C. Reverse Current @ T_A=25℃	0.5					0.6		mA
at Rated DC Blocking Voltage @ T_A=100℃	30					20		mA
Typical Thermal Resistance (Note 1) $R\theta JA$	40							℃/W
Typical Junction Capacitance (Note 2)	300			250		72		pF
Operating Junction Temperature Range T_J	-65 to +125			-65 to +150				℃
Storage Temperature Range T_{STG}	-65 to +150							℃

Notes: 1. Thermal Resistance from Junction to Ambient Vertical P.C. Board Mounting, 0.375"(9.5mm) Lead Length
2. Measured at 1 MHz and Applied Reverse Voltage of 4.0V D.C.

RATINGS AND CHARACTERISTIC CURVES (SR302 THUR SR310)

FIG.1- MAXIMUM FORWARD CURRENT DERATING CURVE

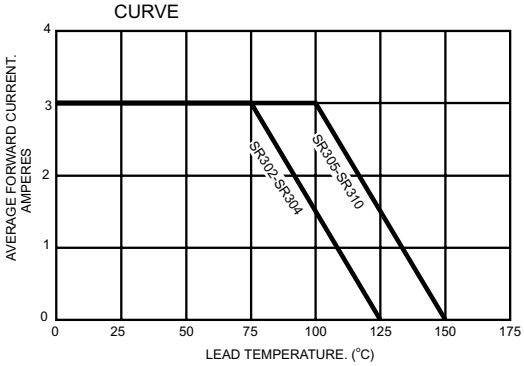


FIG.2- TYPICAL FORWARD CHARACTERISTICS

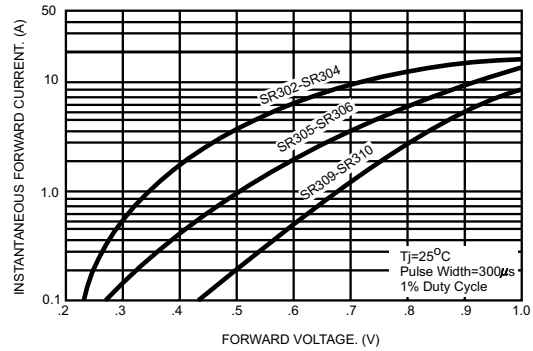


FIG.3- TYPICAL REVERSE CHARACTERISTICS

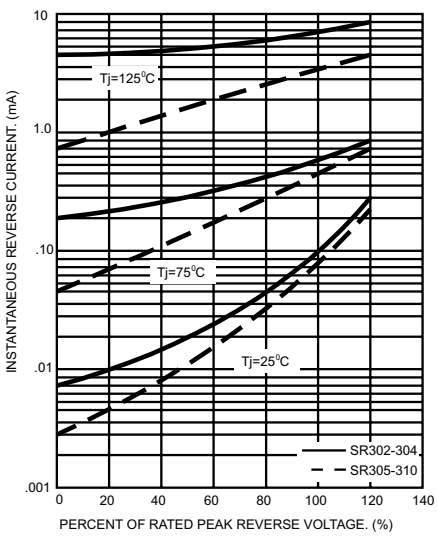


FIG.4- TYPICAL JUNCTION CAPACITANCE

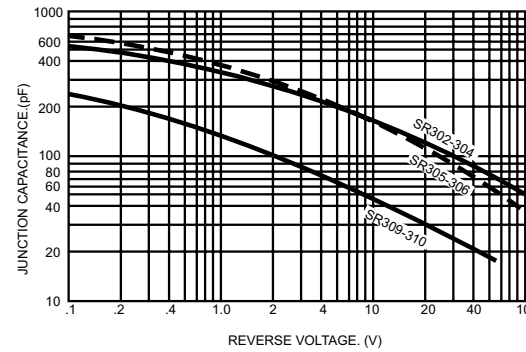
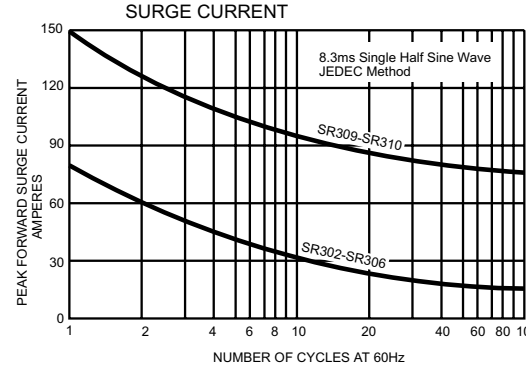


FIG.5- MAXIMUM NON-REPETITIVE FORWARD SURGE CURRENT



TEXAS INSTRUMENTS

TL081, TL081A, TL081B, TL082, TL082A
TL082B, TL084, TL084A, TL084B

SLOS081I – FEBRUARY 1977 – REVISED MAY 2015

TL08xx JFET-Input Operational Amplifiers

1 Features

- Low Power Consumption: 1.4 mA/ch Typical
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias Current: 30 pA Typical
- Low Input Offset Current: 5 pA Typical
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typical
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- High Slew Rate: 13 V/μs Typical
- Common-Mode Input Voltage Range Includes V_{CC+}

2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

3 Description

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

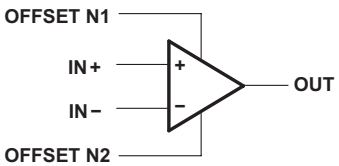
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL084xD	SOIC (14)	8.65 mm × 3.91 mm
TL08xxFK	LCCC (20)	8.89 mm × 8.89 mm
TL084xJ	CDIP (14)	19.56 mm × 6.92 mm
TL084xN	PDIP (14)	19.3 mm × 6.35 mm
TL084xNS	SO (14)	10.3 mm × 5.3 mm
TL084xPW	TSSOP (14)	5.0 mm × 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Symbol

TL081



TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)

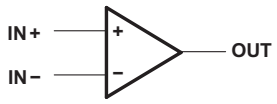


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2014) to Revision I — **Page**

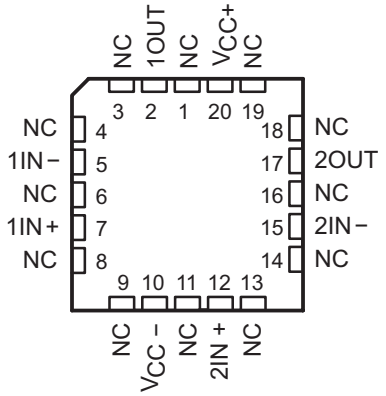
- Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Applications* ... 1
- Moved *Typical Characteristics* into *Specifications* section. ... 9

Changes from Revision G (September 2004) to Revision H — **Page**

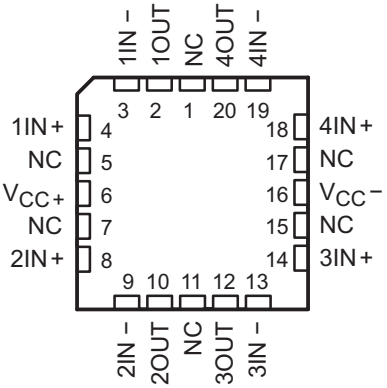
- Updated document to new TI data sheet format - no specification changes. ... 1
- Deleted *Ordering Information* table. ... 1

5 Pin Configuration and Functions

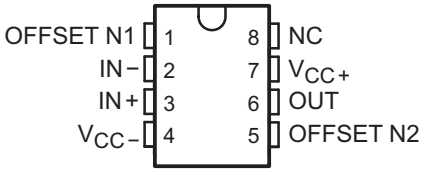
TL082 FK Package
20-Pin LCCC
Top View



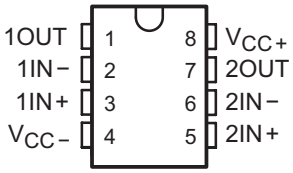
TL084 FK Package
20-Pin LCCC
Top View



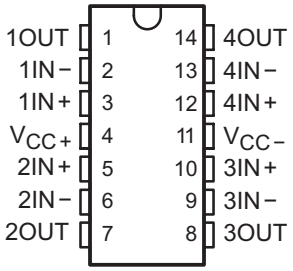
TL081 and TL081x D, P, and PS Package
8-Pin SOIC, PDIP, and SO
Top View



TL082 and TL082x D, JG, P, PS and PW Package
8-Pin SOIC, CDIP, PDIP, SO, and TSSOP
Top View



TL084 and TL084x D, J, N, NS and PW Package
14-Pin SOIC, CDIP, PDIP, SO, and TSSOP
Top View



Pin Functions

PIN						I/O	DESCRIPTION
NAME	TL081	TL082		TL084			
	SOIC, PDIP, SO	SOIC, CDIP, PDIP, SO, TSSOP	LCCC	SOIC, CDIP, PDIP, SO, TSSOP	LCCC		
1IN–	—	2	5	2	3	I	Negative input
1IN+	—	3	7	3	4	I	Positive input
1OUT	—	1	2	1	2	O	Output
2IN–	—	6	15	6	9	I	Negative input
2IN+	—	5	12	5	8	I	Positive input
2OUT	—	7	17	7	10	O	Output
3IN–	—	—	—	9	13	I	Negative input
3IN+	—	—	—	10	14	I	Positive input
3OUT	—	—	—	8	12	O	Output
4IN–	—	—	—	13	19	I	Negative input
4IN+	—	—	—	12	18	I	Positive input
4OUT	—	—	—	14	20	O	Output

Pin Functions (continued)

PIN						I/O	DESCRIPTION
NAME	TL081	TL082		TL084			
	SOIC, PDIP, SO	SOIC, CDIP, PDIP, SO, TSSOP	LCCC	SOIC, CDIP, PDIP, SO, TSSOP	LCCC		
IN–	2	—	—	—	—	I	Negative input
IN+	3	—	—	—	—	I	Positive input
NC	8	—	1	—	1	—	Do not connect
			3				
			4		5		
			6				
			8		7		
			9				
			11		11		
			13				
			14		15		
			16				
			18		17		
OFFSET N1	1	—	—	—	—	—	Input offset adjustment
OFFSET N2	5	—	—	—	—	—	Input offset adjustment
OUT	6	—	—	—	—	O	Output
V_{CC-}	4	4	10	11	16	—	Power supply
V_{CC+}	7	8	20	4	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)				18	V
V_{CC-}					–18	
V_{ID}	Differential input voltage(3)				±30	V
V_I	Input voltage(2)(4)				±15	V
	Duration of output short circuit(5)			Unlimited		
	Continuous total power dissipation			See *Dissipation Rating Table*		
T_A	Operating free-air temperature		TL08_C TL08_AC TL08_BC	0	70	°C
			TL08_I	–40	85	
			TL084Q	–40	125	
			TL08_M	–55	125	
	Operating virtual junction temperature				150	°C
T_C	Case temperature for 60 seconds	FK package	TL08_M		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	J or JG package	TL08_M		300	°C
T_{stg}	Storage temperature			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		V_{CC-} + 4	V_{CC+} – 4	V
T_A	Ambient temperature	TL08xM	–55	125	°C
		TL08xQ	–40	125	
		TL08xI	–40	85	
		TL08xC	0	70	

6.4 Thermal Information

THERMAL METRIC[1]		TL08xx								UNIT
		D (SOIC)		N (PDIP)	NS (SO)	P (PDIP)	PS (SO)	PW (TSSOP)		
		8 PINS	14 PINS	14 PINS	14 PINS	{PIN COUNT} PINS	{PIN COUNT} PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2][3]	97	86	76	80	85	95	149	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI

$V_{CC±}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A[1]	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current[2]	V_O = 0	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current[2]	V_O = 0	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			15			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and –40°C to 85°C for TL08_I.
(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

Electrical Characteristics for TL08xC, TL08xxC, and TL08xI (continued)

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

6.6 Electrical Characteristics for TL08xM and TL084x

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current (2)	V_O = 0	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current (2)	V_O = 0	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		25	200		V/mV
			Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

6.7 Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 19	8 (1)	13		V/µs
		V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, T_A = − 55°C to 125°C, See Figure 19	5 (1)			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Operating Characteristics (continued)

$V_{CC\pm}$ = ±15 V, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise-time	V_I = 20 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 19			0.05		µs
	overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, A_{VD} = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ, f = 1 kHz,			0.003%		

6.8 Dissipation Rating Table

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 m/W	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 m/W	546 mW	210 mW

6.9 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in *Parameter Measurement Information*.

Table 1. Table of Graphs

			Figure
V_{OM}	Maximum peak output voltage	versus Frequency versus Free-air temperature versus Load resistance versus Supply voltage	Figure 1, Figure 2, Figure 3 Figure 4 Figure 5 Figure 6
A_{VD}	Large-signal differential voltage amplification	versus Free-air temperature versus Load resistance	Figure 7 Figure 8
	Differential voltage amplification	versus Frequency with feed-forward compensation	Figure 9
P_D	Total power dissipation	versus Free-air temperature	Figure 10
I_{CC}	Supply current	versus Free-air temperature versus Supply voltage	Figure 11 Figure 12
I_{IB}	Input bias current	versus Free-air temperature	Figure 13
	Large-signal pulse response	versus Time	Figure 14
V_O	Output voltage	versus Elapsed time	Figure 15
CMRR	Common-mode rejection ratio	versus Free-air temperature	Figure 16
V_n	Equivalent input noise voltage	versus Frequency	Figure 17
THD	Total harmonic distortion	versus Frequency	Figure 18

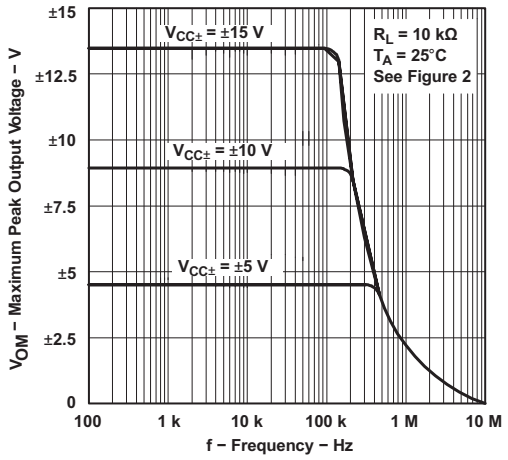


Figure 1. Maximum Peak Output Voltage vs Frequency

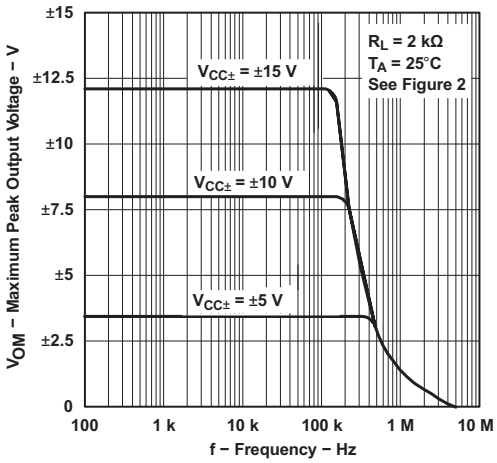


Figure 2. Maximum Peak Output Voltage vs Frequency

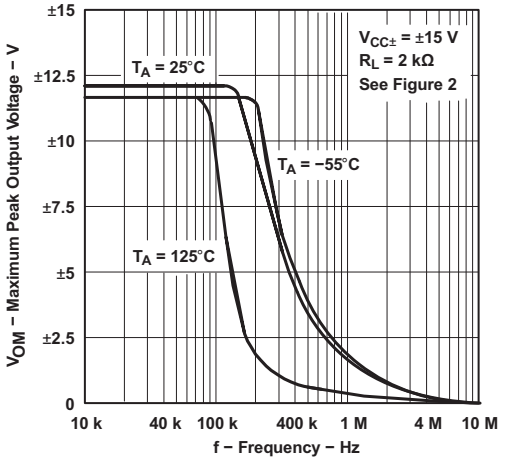


Figure 3. Maximum Peak Voltage vs Frequency

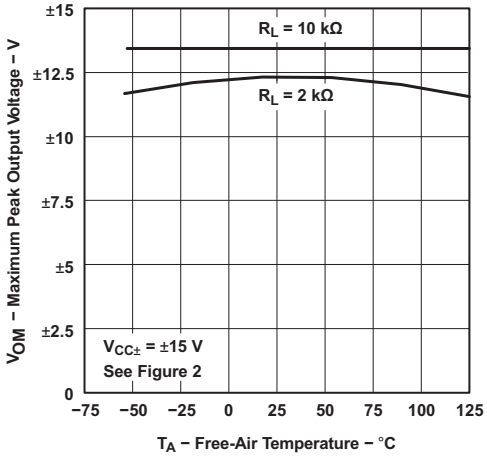


Figure 4. Maximum Peak Output Voltage vs Free-Air Temperature

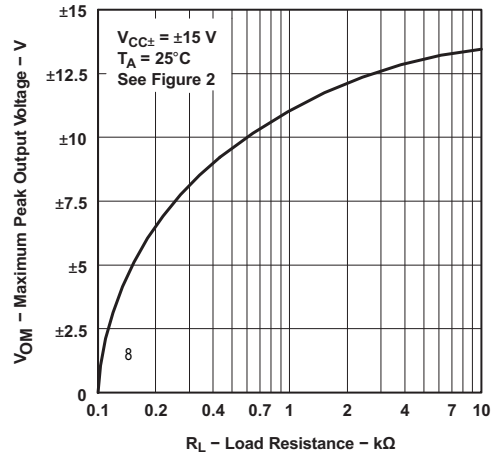


Figure 5. Maximum Peak Output Voltage vs Load Resistance

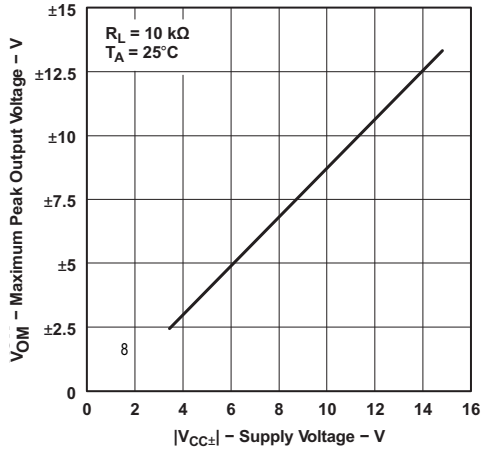


Figure 6. Maximum Peak Output Voltage vs Supply Voltage

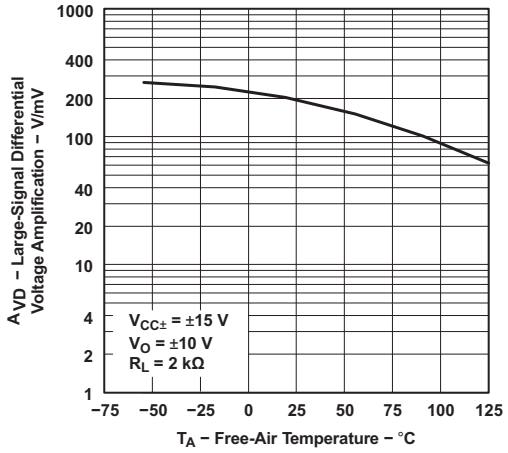


Figure 7. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

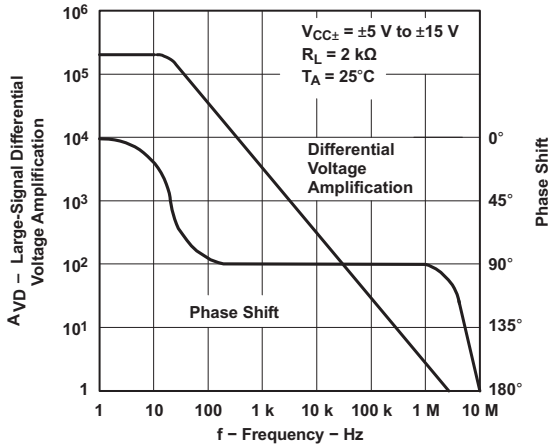


Figure 8. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

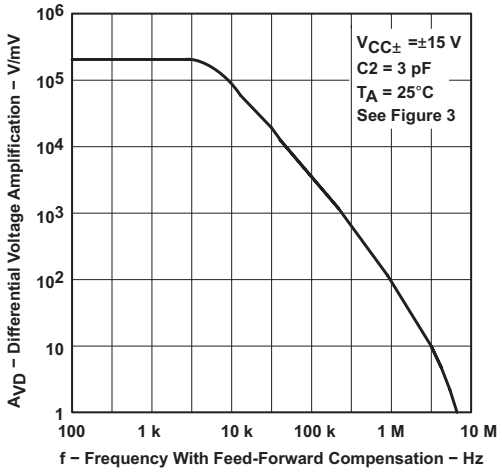


Figure 9. Differential Voltage Amplification vs Frequency with Feed-Forward Compensation

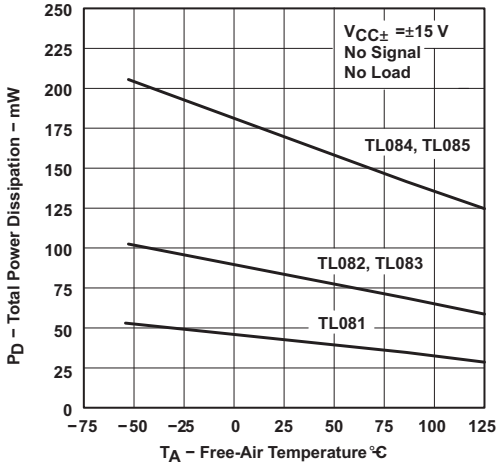


Figure 10. Total Power Dissipation vs Free-Air Temperature

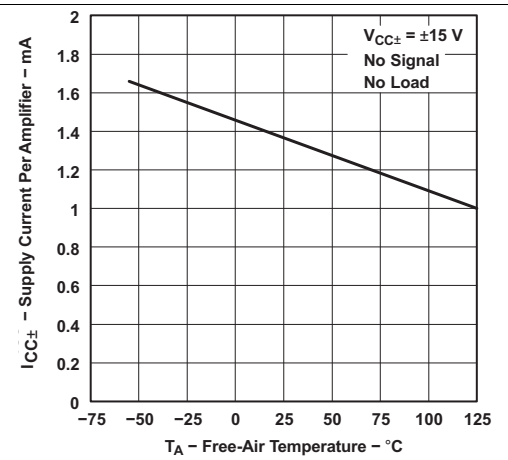


Figure 11. Supply Current per Amplifier vs Free-Air Temperature

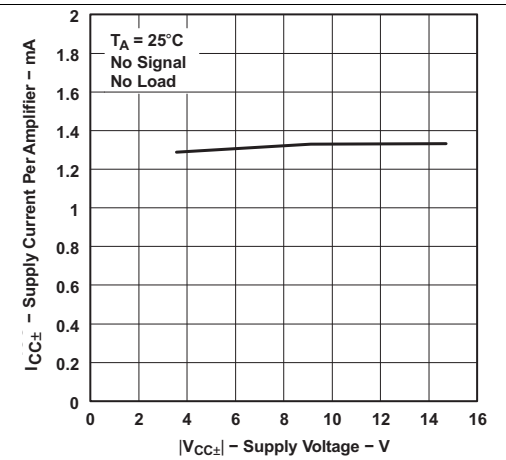


Figure 12. Supply Current per Amplifier vs Supply Voltage

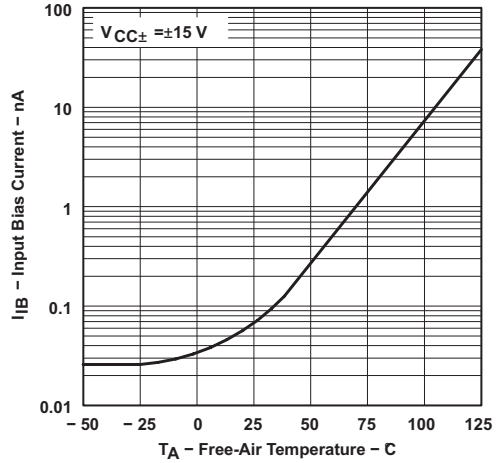


Figure 13. Input Bias Current vs Free-Air Temperature

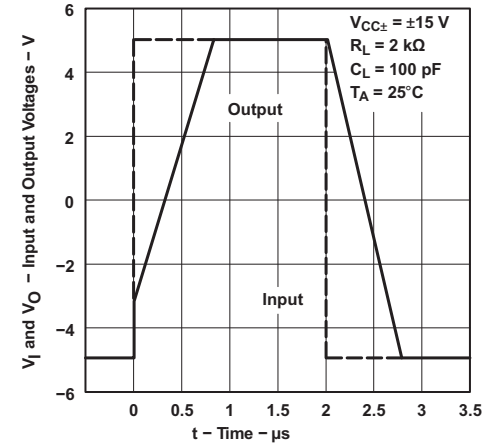


Figure 14. Voltage-Follower Large-Signal Pulse Response

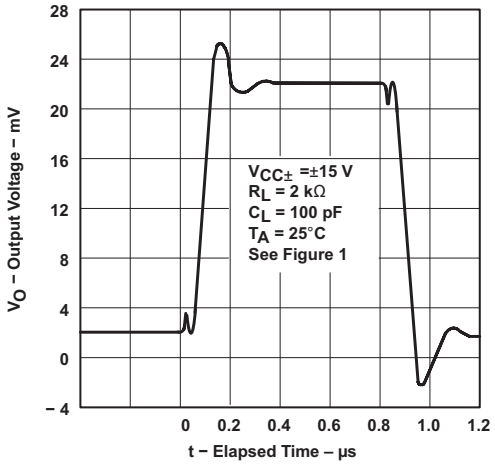


Figure 15. Output Voltage vs Elapsed Time

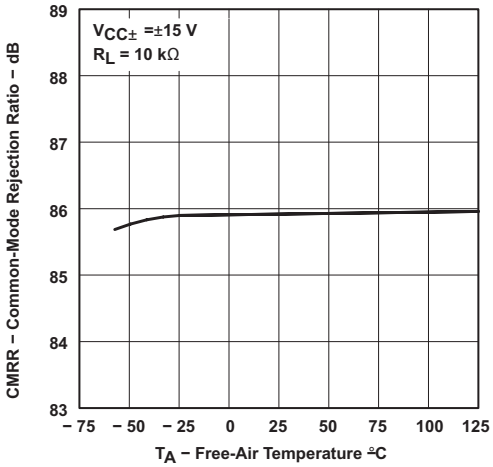


Figure 16. Common-Mode Rejection Ratio vs Free-Air Temperature

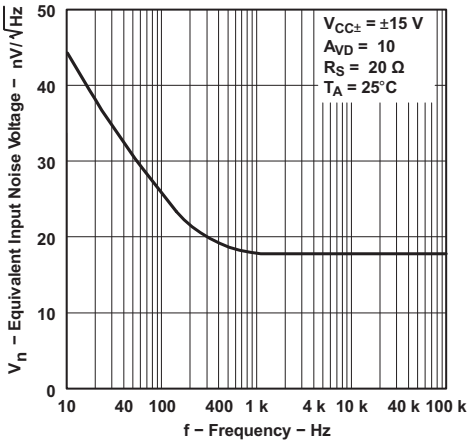


Figure 17. Equivalent Input Noise Voltage vs Frequency

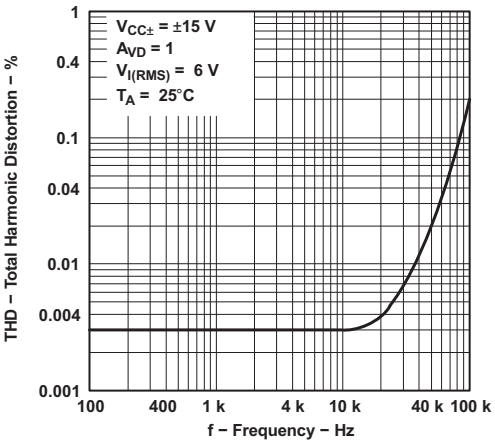


Figure 18. Total Harmonic Distortion vs Frequency

7 Parameter Measurement Information

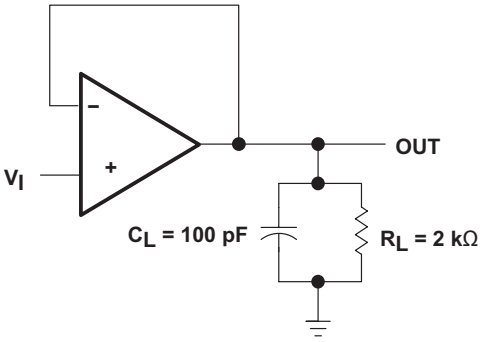


Figure 19. Test Figure 1

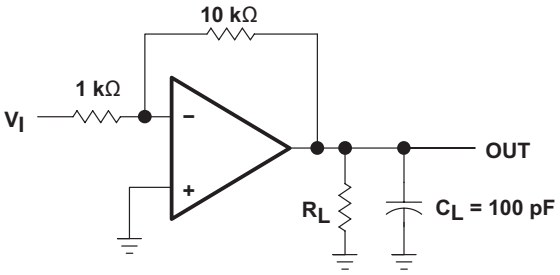


Figure 20. Test Figure 2

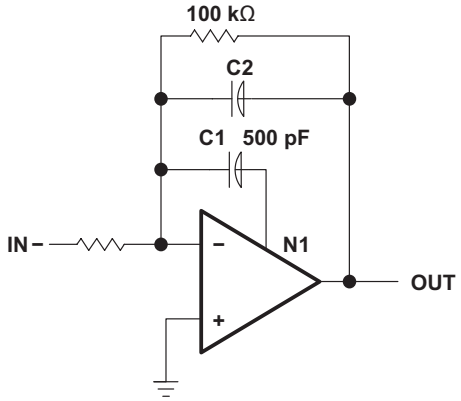


Figure 21. Test Figure 3

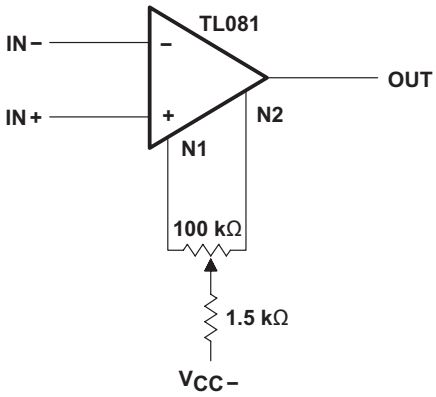


Figure 22. Test Figure 4

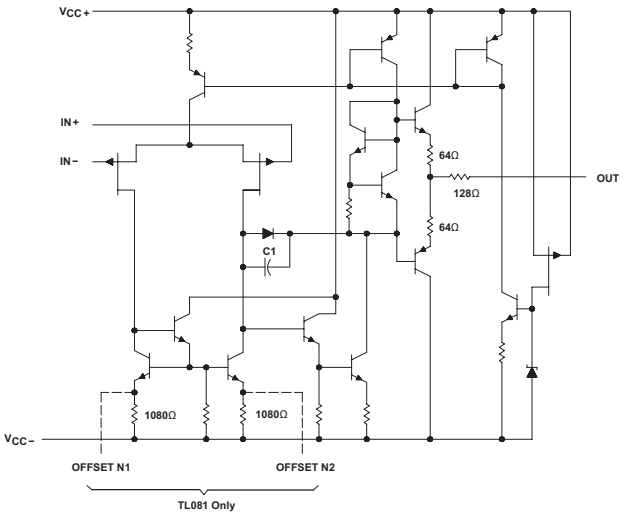
8 Detailed Description

8.1 Overview

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08xx family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to +125°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to +125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices will add little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

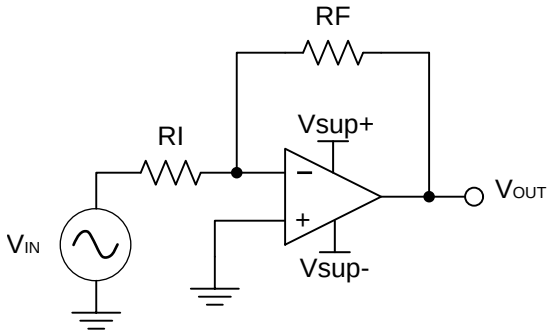


Figure 23. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_v = \frac{VOUT}{VIN} \tag{1}$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_v = -\frac{RF}{RI} \tag{3}$$

Typical Applications (continued)

9.2.1.3 Application Curve

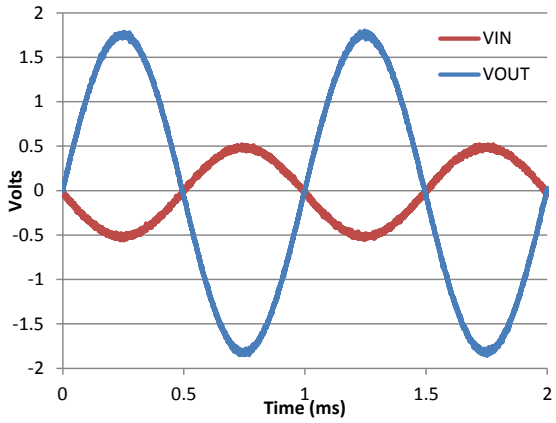


Figure 24. Input and output voltages of the inverting amplifier

9.3 System Examples

9.3.1 General Applications

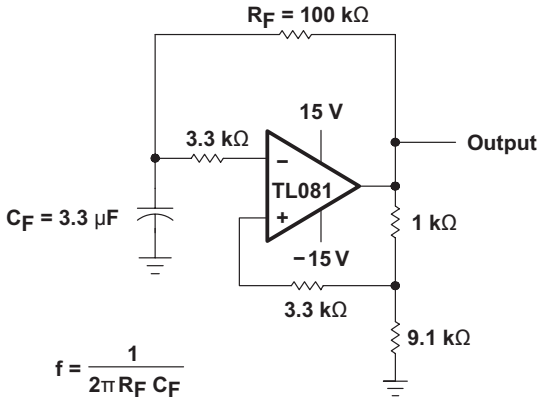


Figure 25. 0.5-Hz Square-Wave Oscillator

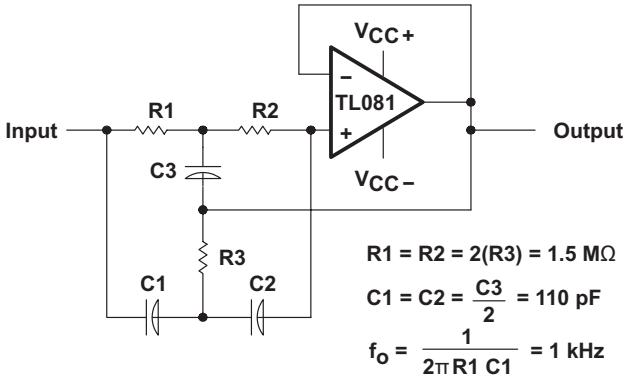


Figure 26. High-Q Notch Filter

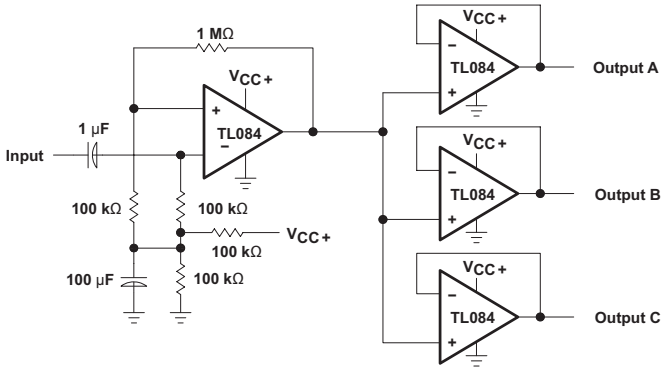
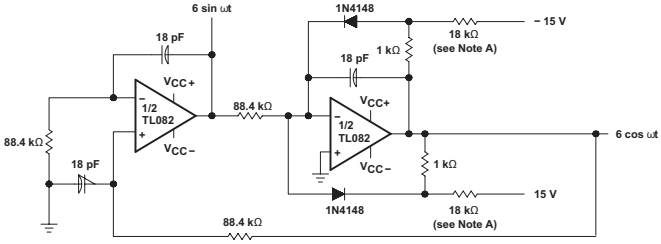


Figure 27. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

Figure 28. 100-kHz Quadrature Oscillator

System Examples (continued)

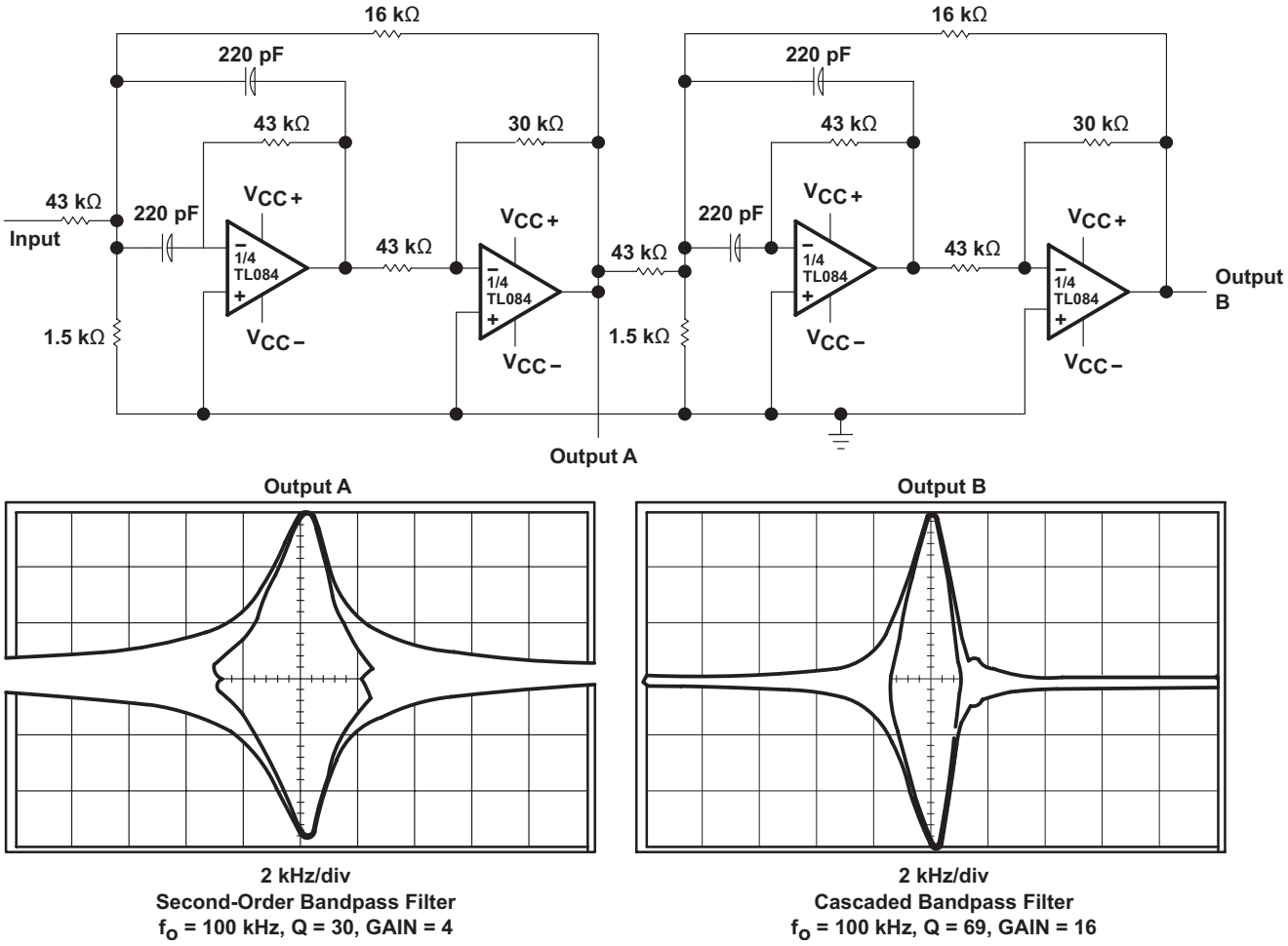


Figure 29. Positive-Feedback Bandpass Filter

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

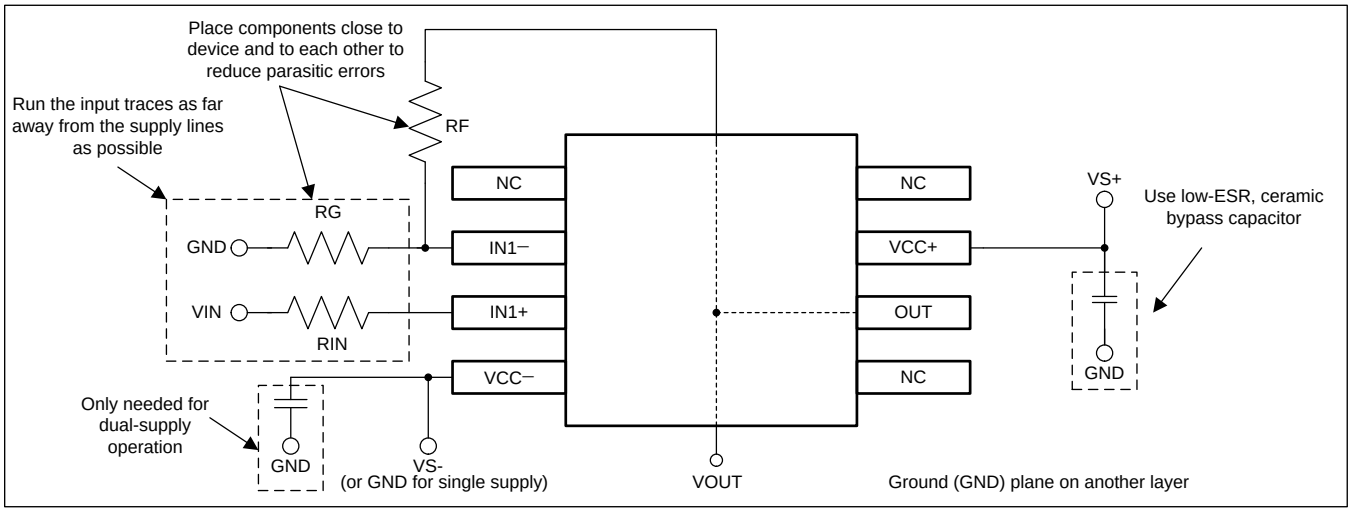


Figure 30. Operational Amplifier Board Layout for Noninverting Configuration

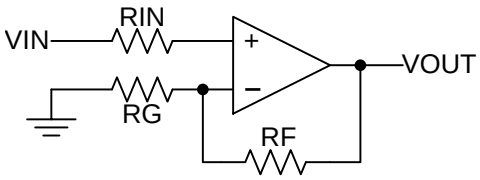


Figure 31. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For more information, see the following:

- *Circuit Board Layout Techniques*, SLOA089.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL081	Click here	Click here	Click here	Click here	Click here
TL081A	Click here	Click here	Click here	Click here	Click here
TL081B	Click here	Click here	Click here	Click here	Click here
TL082	Click here	Click here	Click here	Click here	Click here
TL082A	Click here	Click here	Click here	Click here	Click here
TL082B	Click here	Click here	Click here	Click here	Click here
TL084	Click here	Click here	Click here	Click here	Click here
TL084A	Click here	Click here	Click here	Click here	Click here
TL084B	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
5962-9851501QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
5962-9851503Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	Samples
5962-9851503QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9851503QCA TL084MJB	Samples
TL081ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	Samples
TL081ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	Samples
TL081BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL081CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples
TL081CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	Samples
TL081ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL081IP	Samples
TL082ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	Samples
TL082ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	Samples
TL082ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	Samples
TL082BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	Samples
TL082CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	Samples
TL082CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples
TL082IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
TL082MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL082MJG	Samples
TL082MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
TL084ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084ACN	Samples
TL084ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples
TL084ACNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples
TL084BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	Samples
TL084CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	Samples
TL084CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL084MFK	Samples
TL084MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										MFKB	
TL084MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL084MJ	Samples
TL084MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	Samples
TL084QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

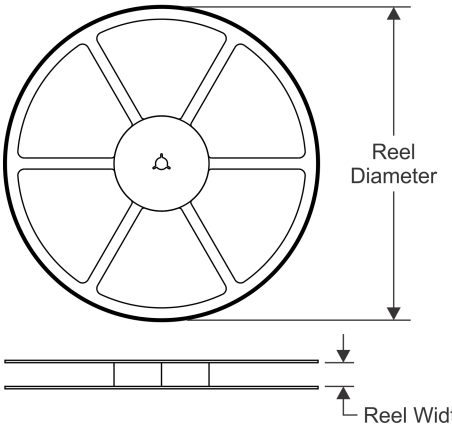
- Catalog: TL082, TL084
- Automotive: TL082-Q1, TL082-Q1
- Military: TL082M, TL084M

NOTE: Qualified Version Definitions:

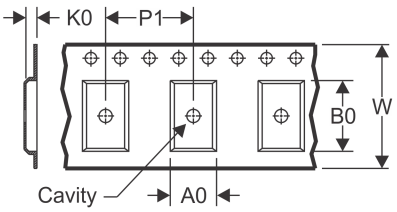
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

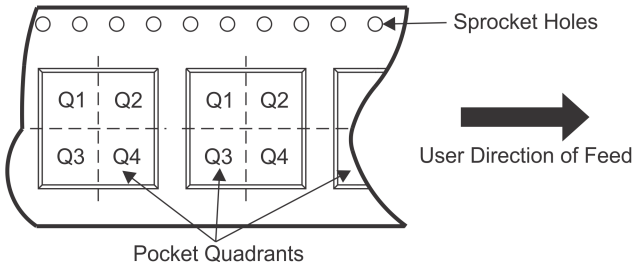


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

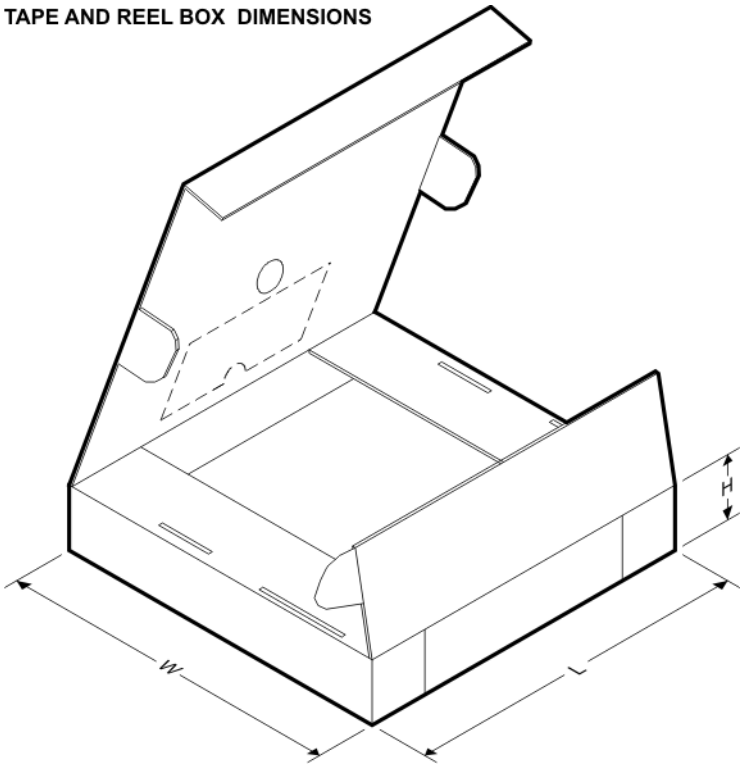


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL084ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



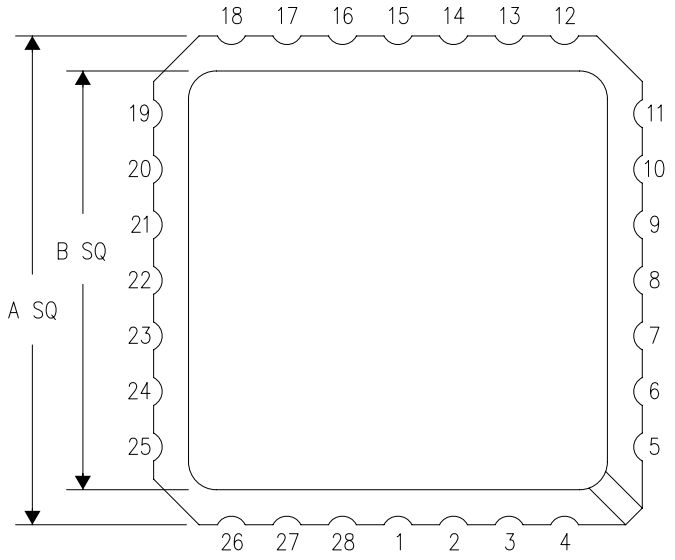
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL081IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACPSR	SO	PS	8	2000	367.0	367.0	38.0

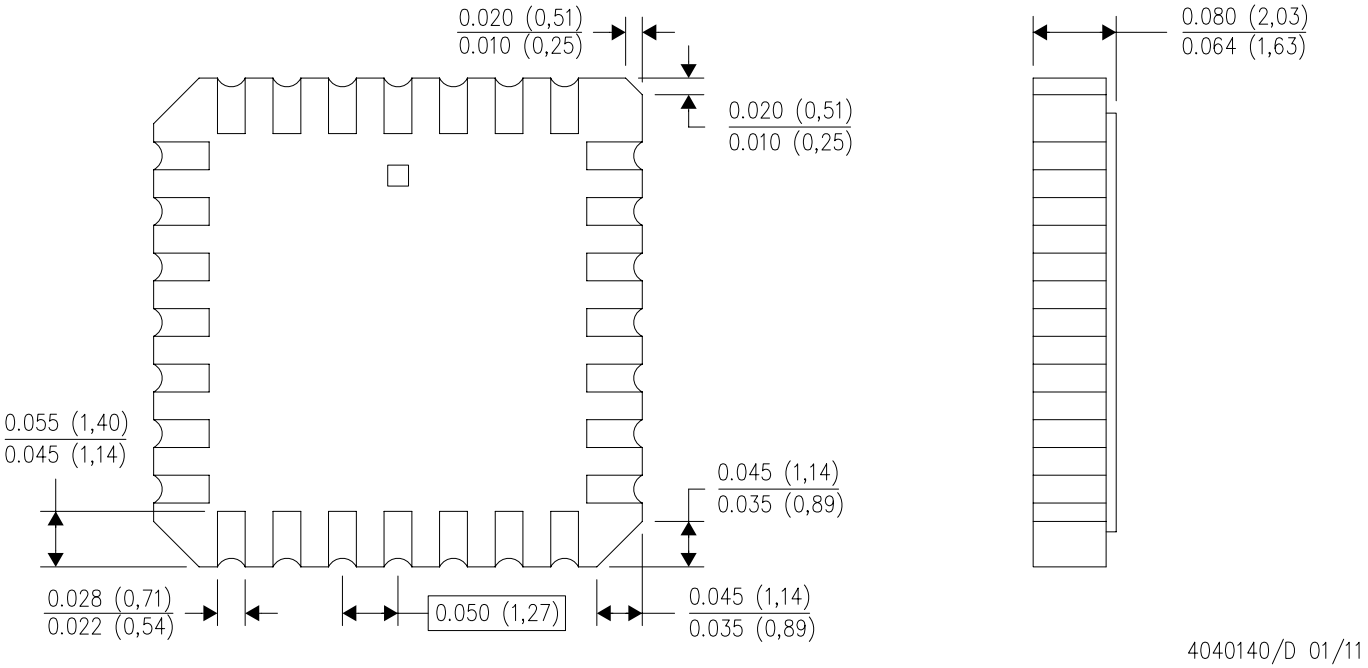
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL082CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL082IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL084ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL084BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL084CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL084IDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084QDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084QDRG4	SOIC	D	14	2500	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



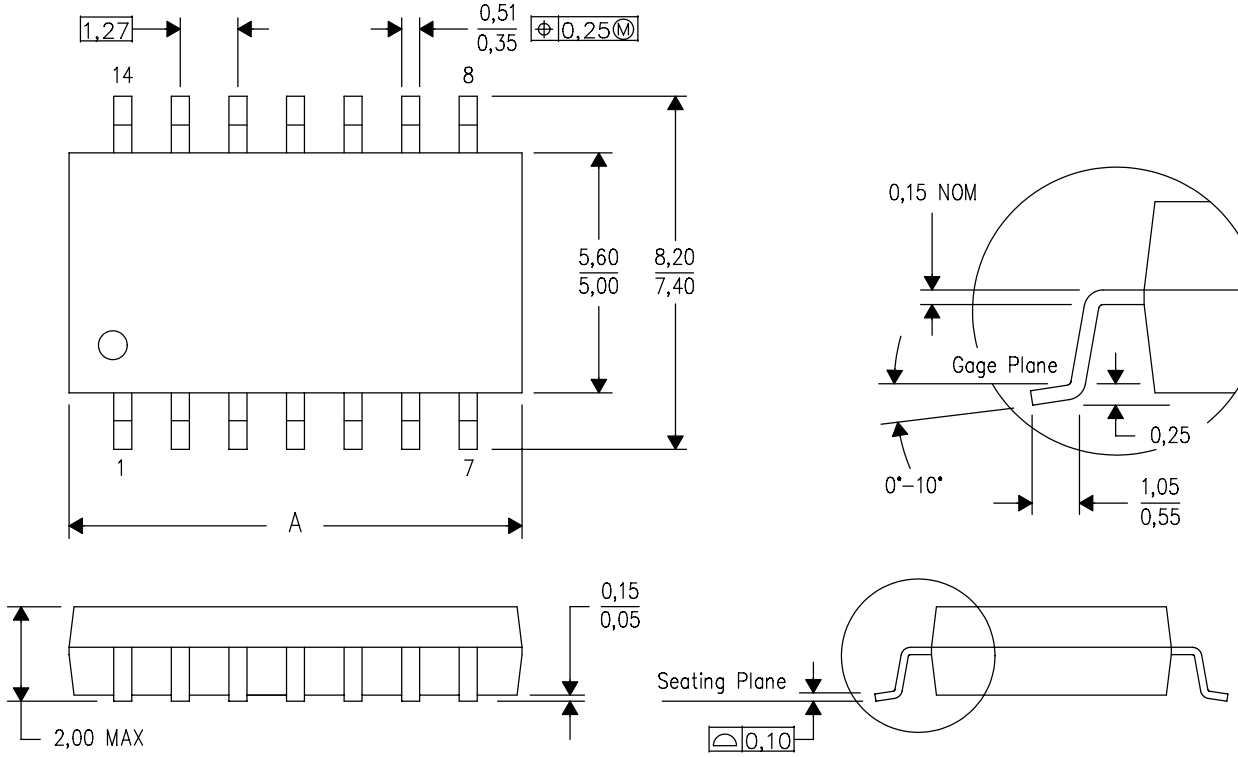
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

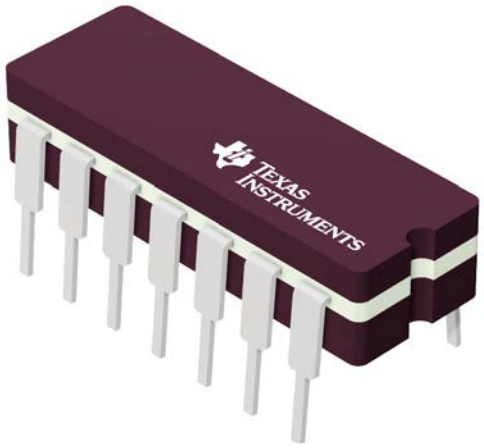
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

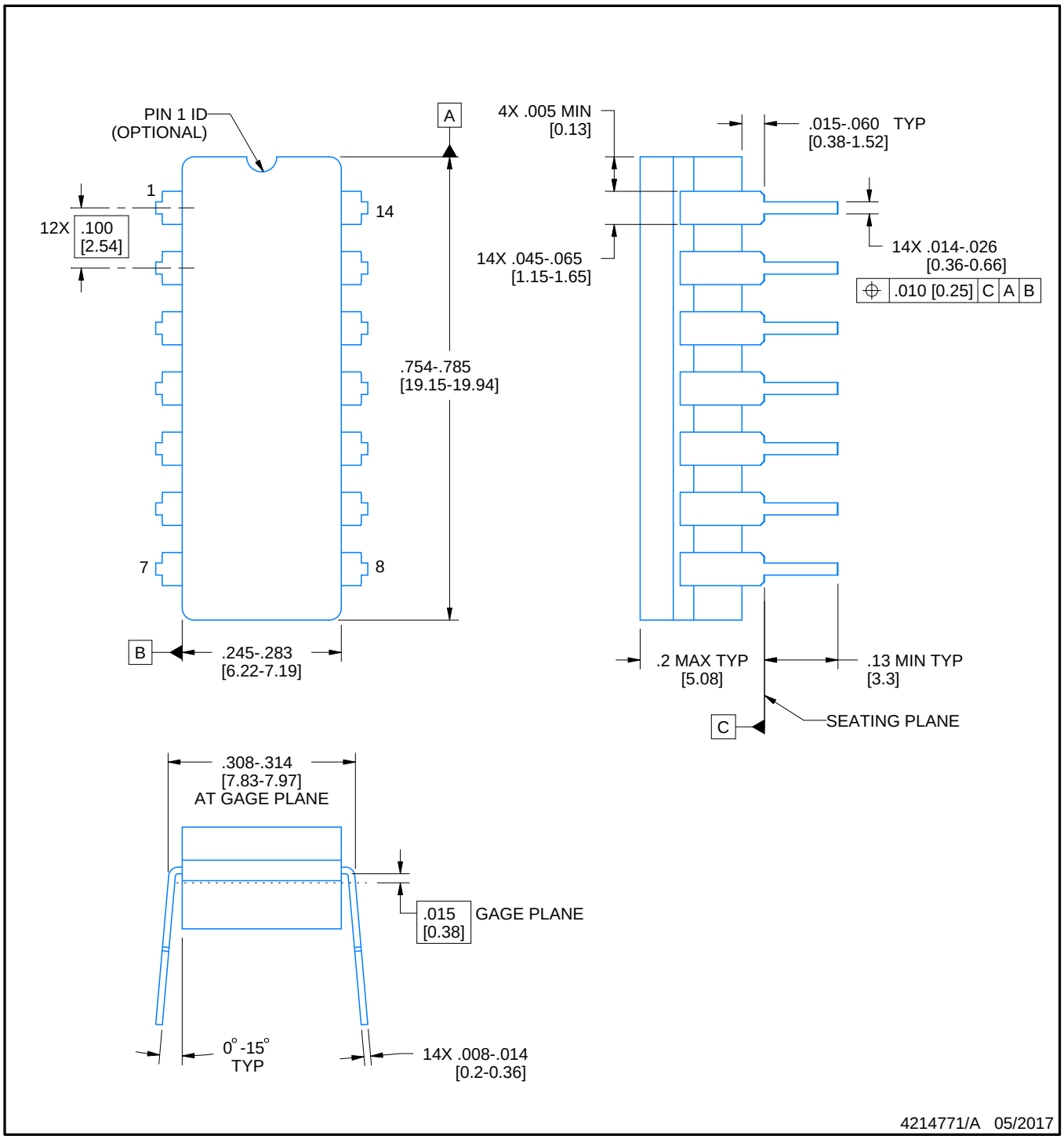
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

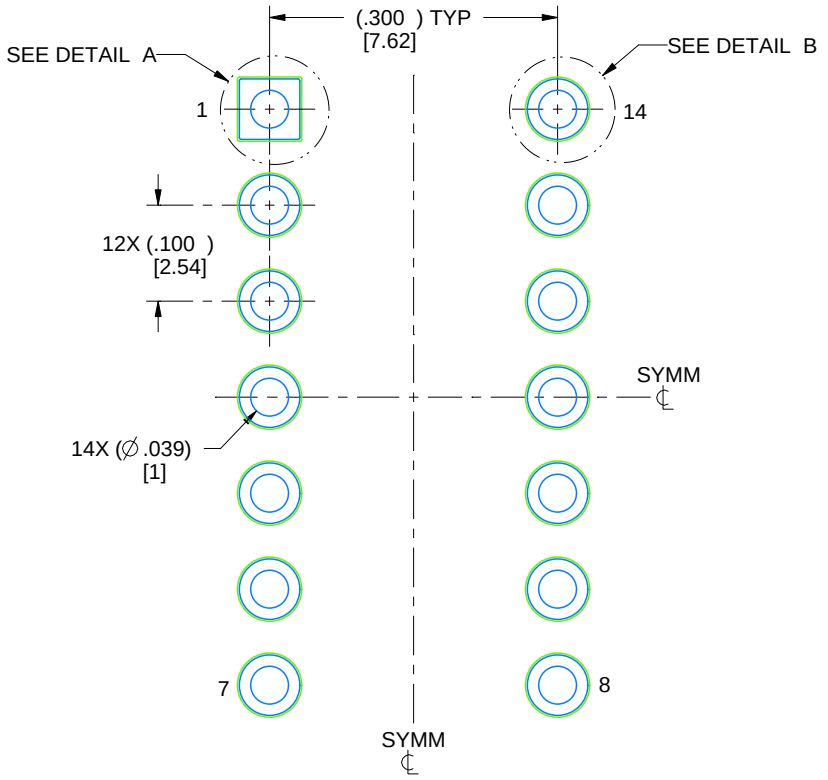
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

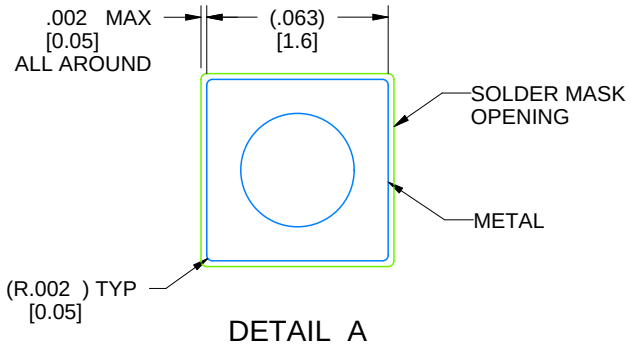
J0014A

CDIP - 5.08 mm max height

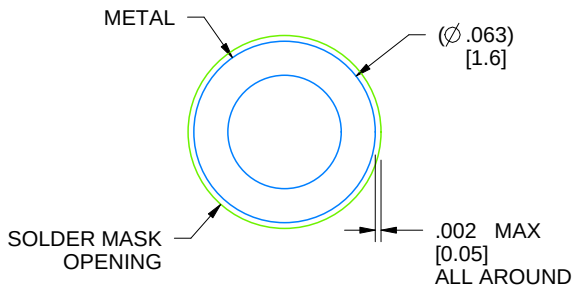
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



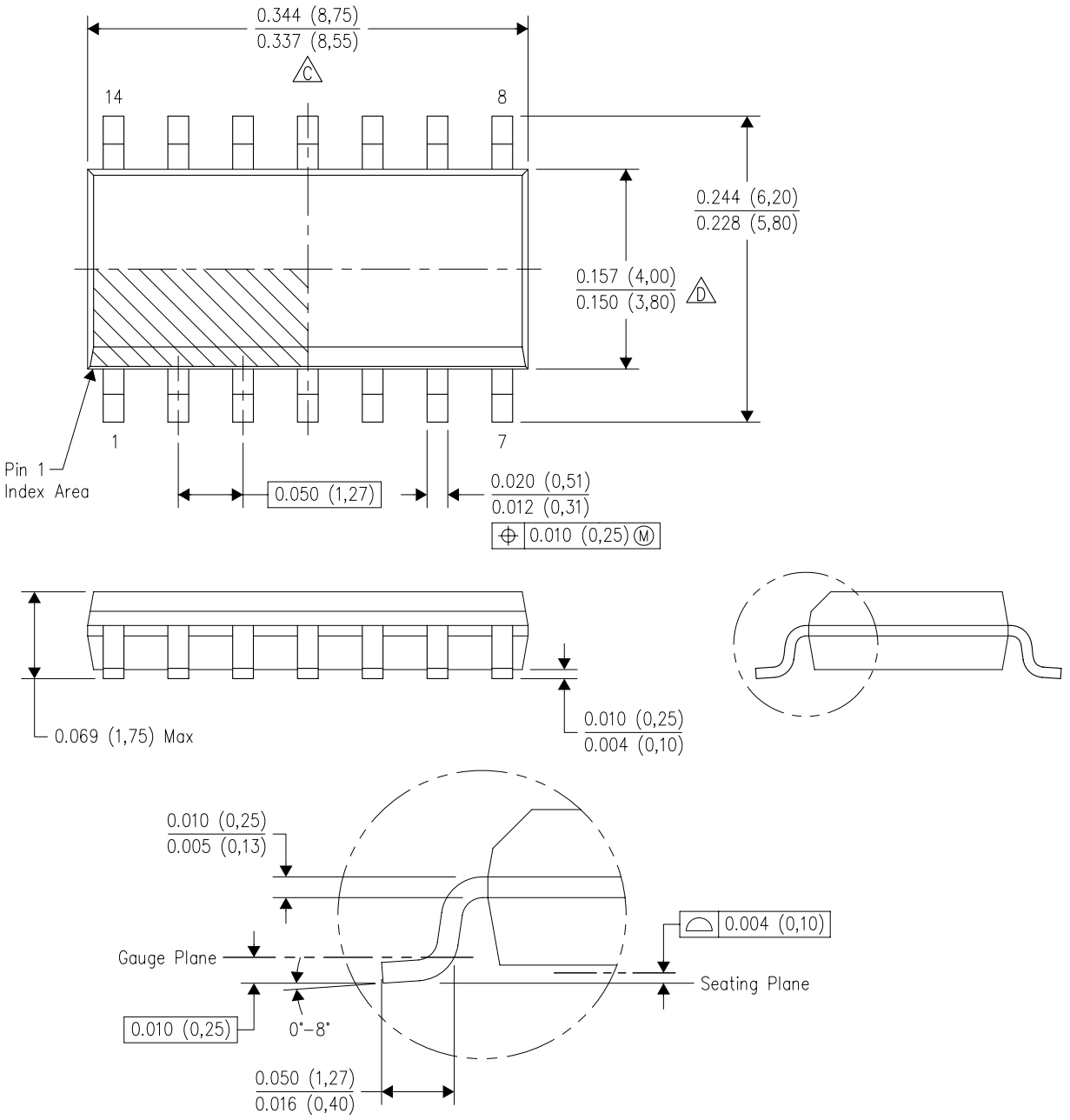
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

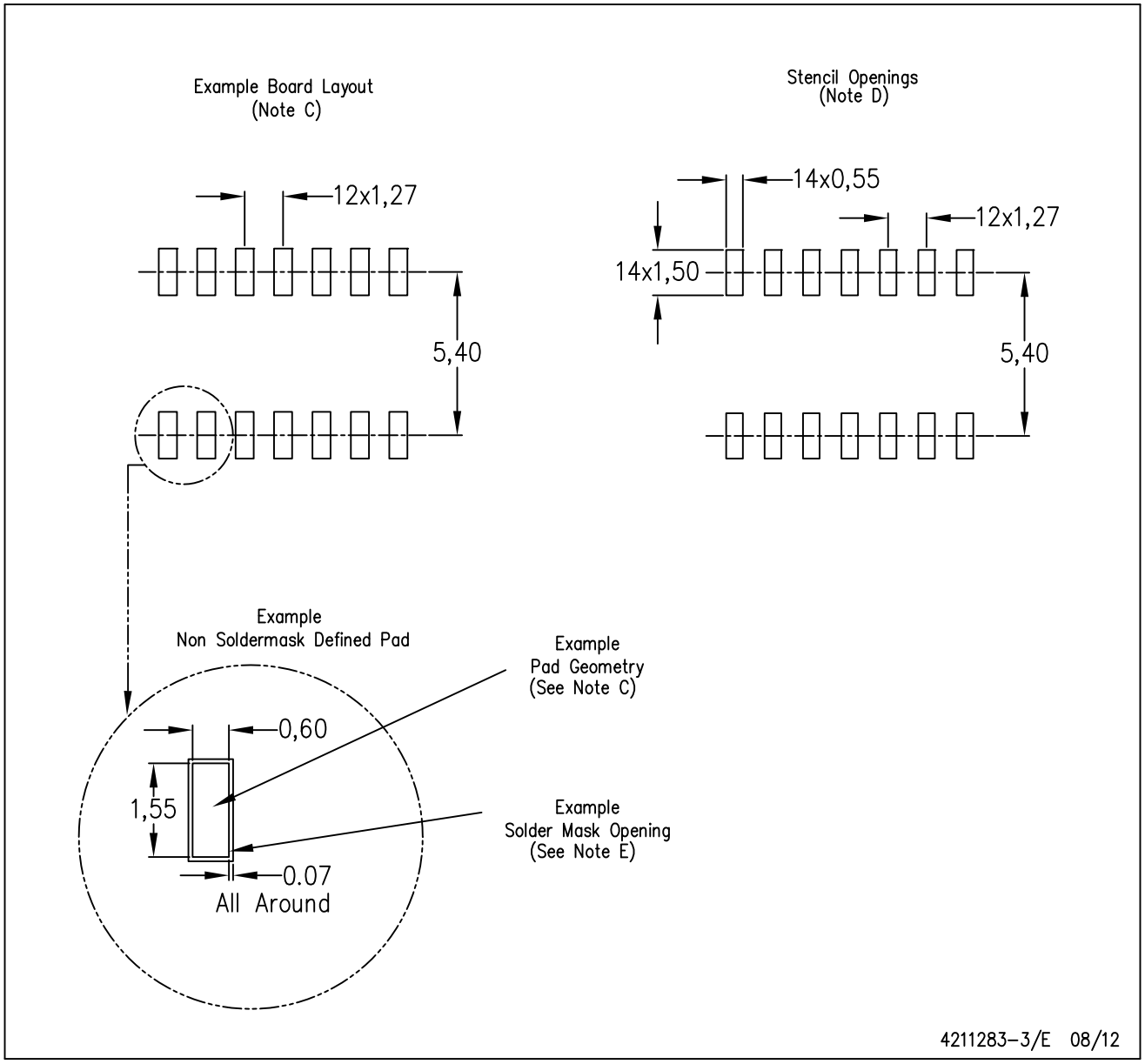
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

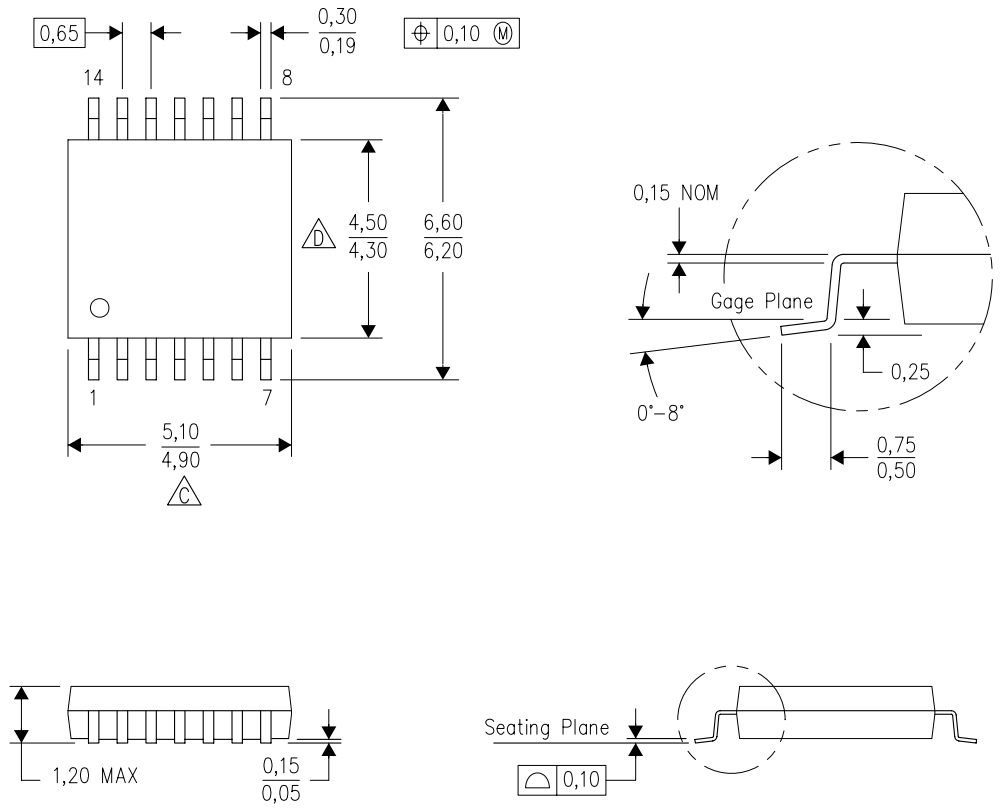
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

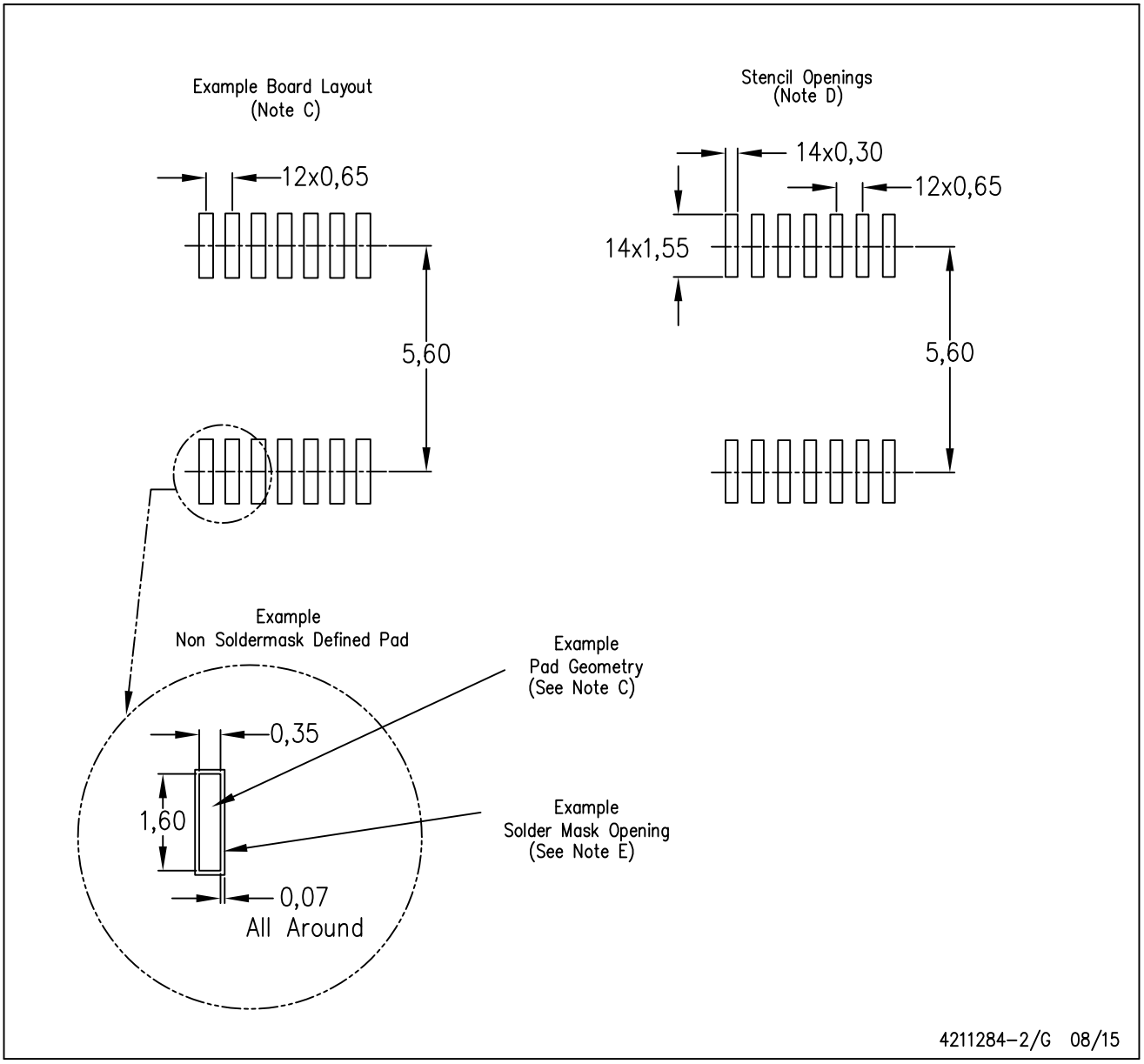
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

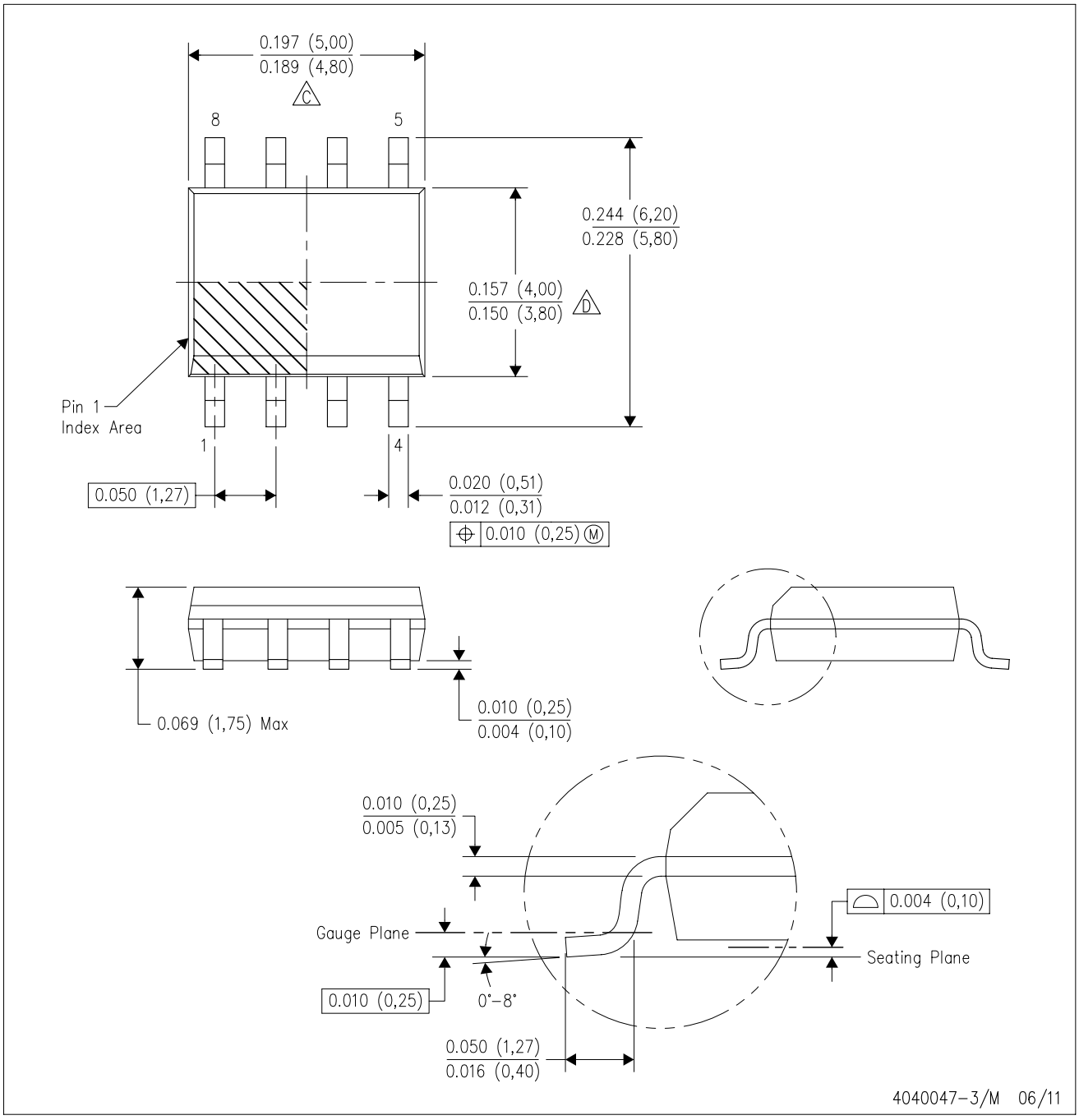
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



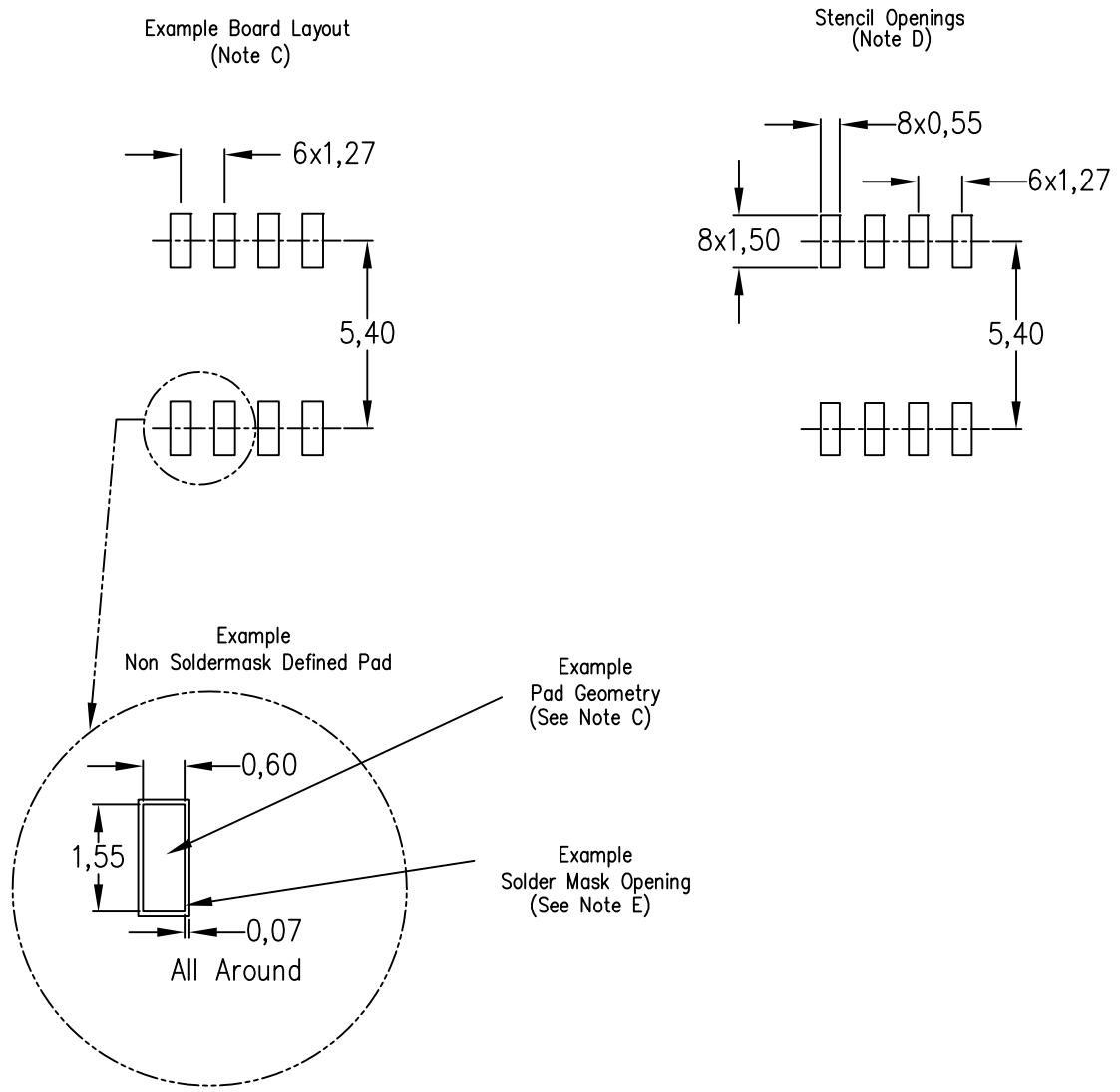
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

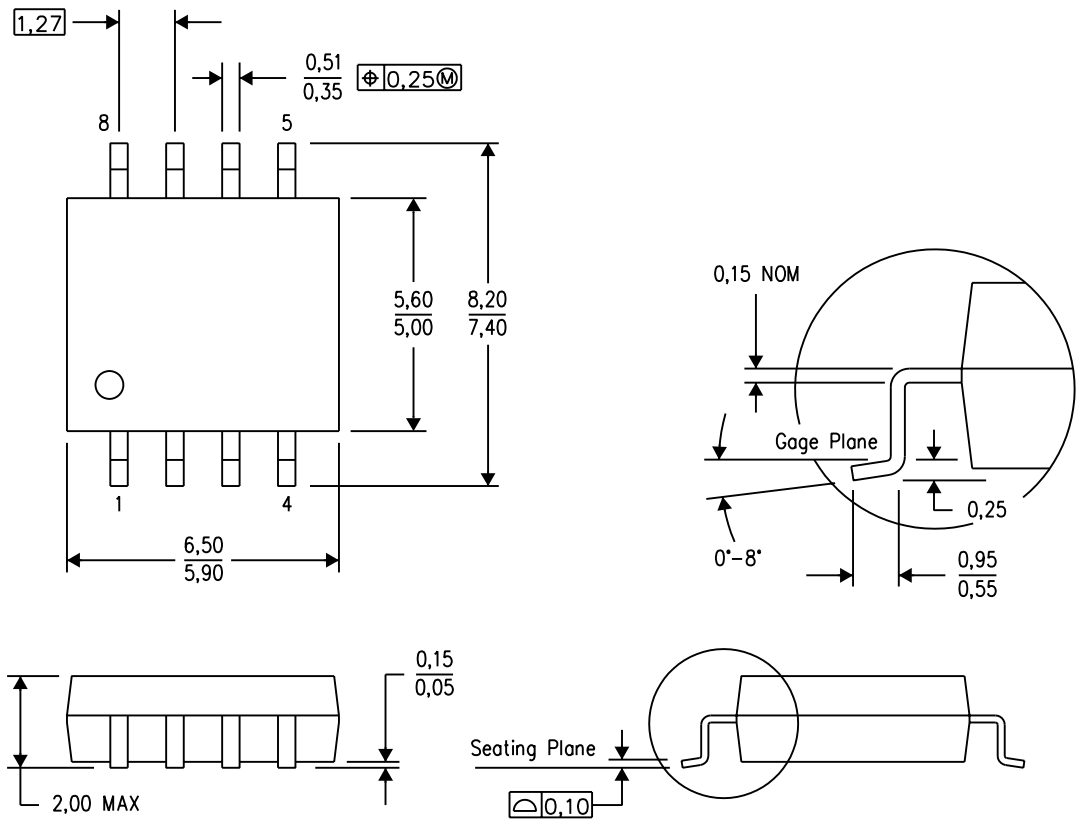
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

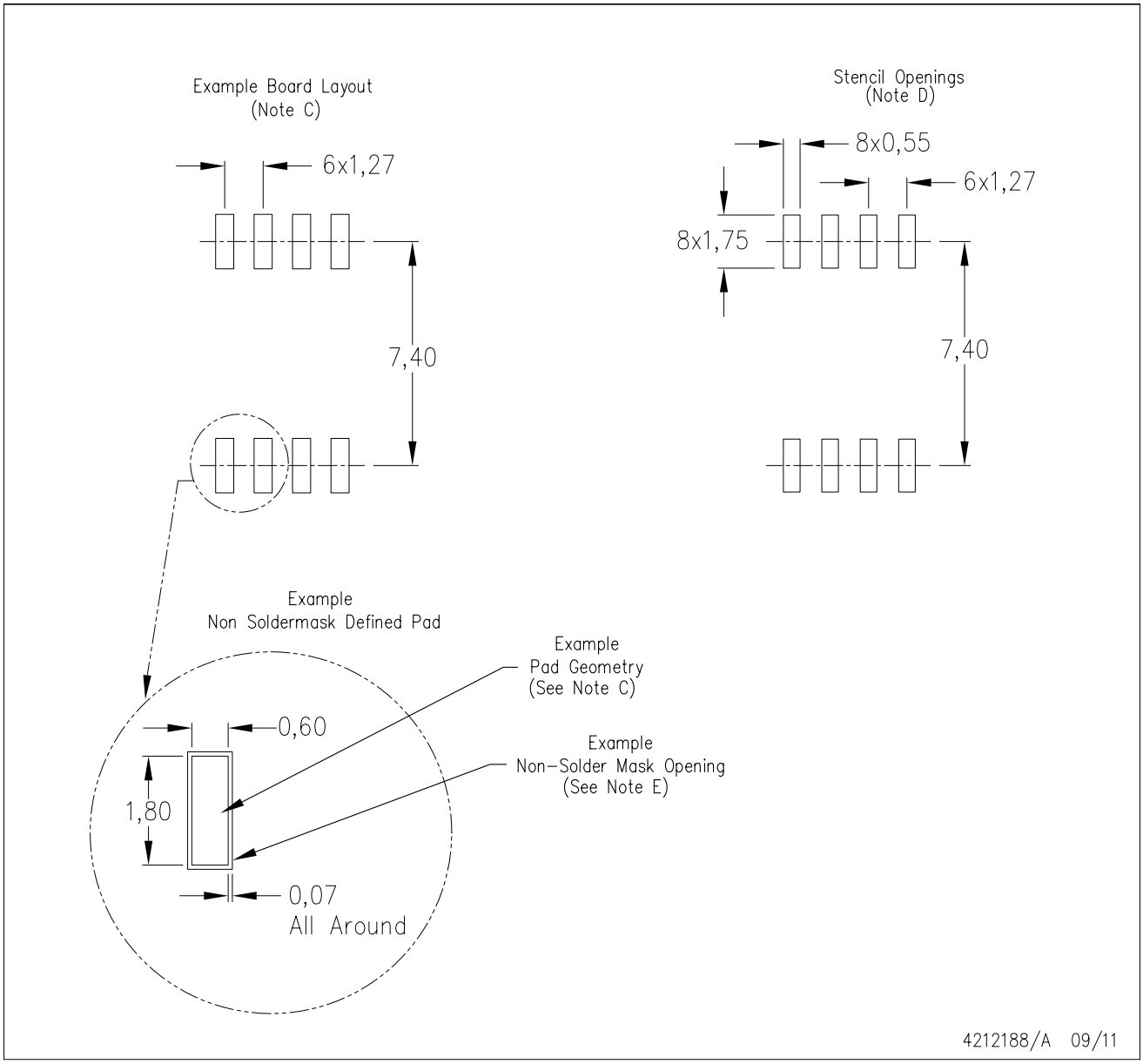
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

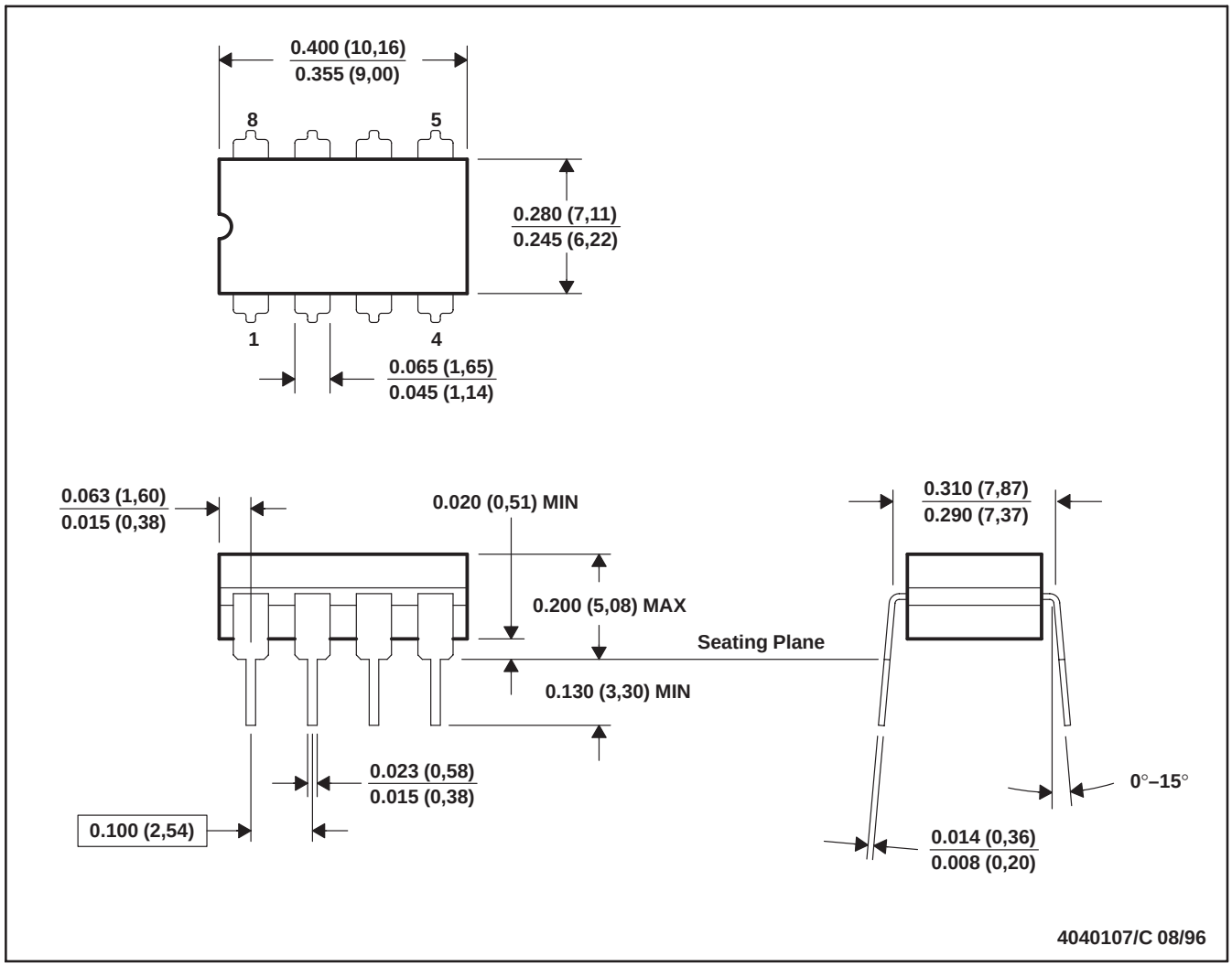
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

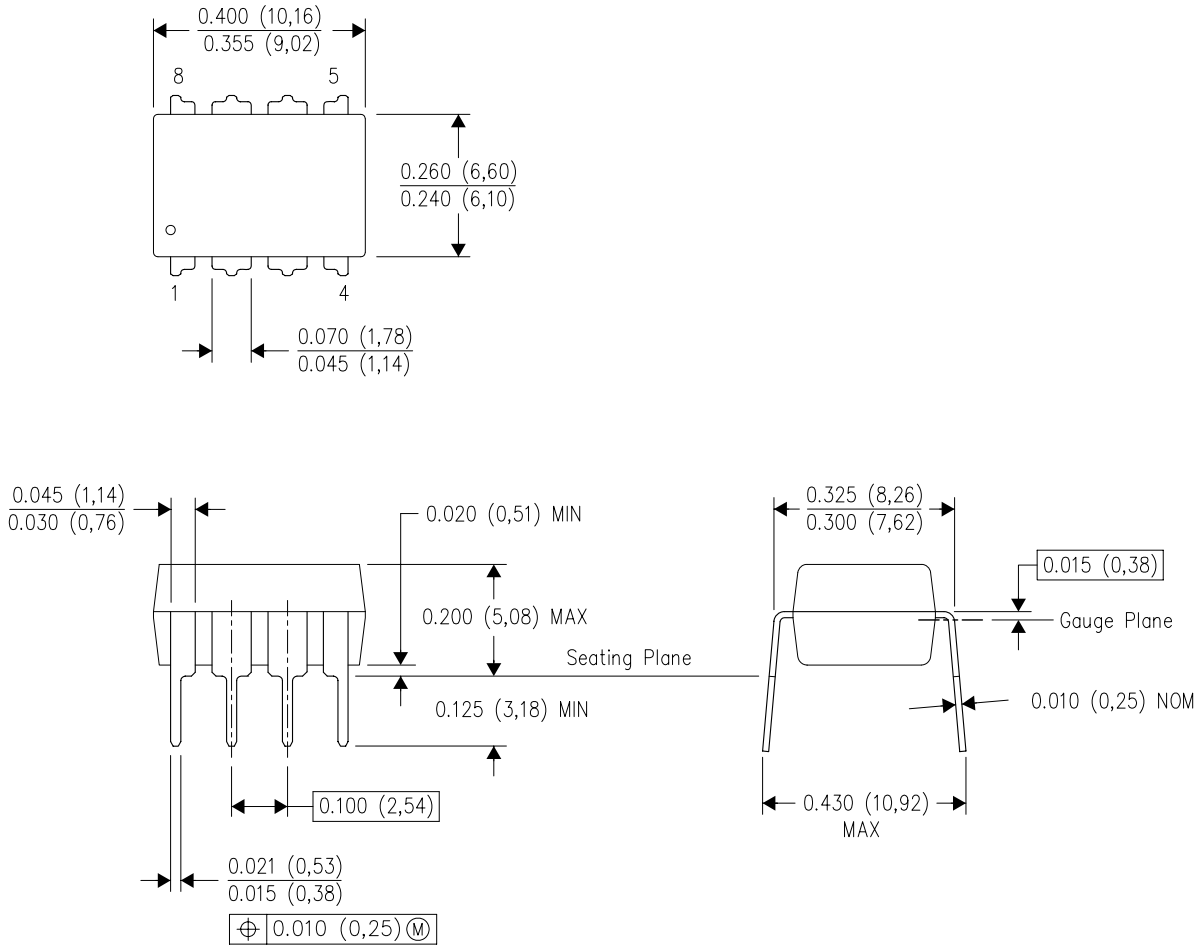
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

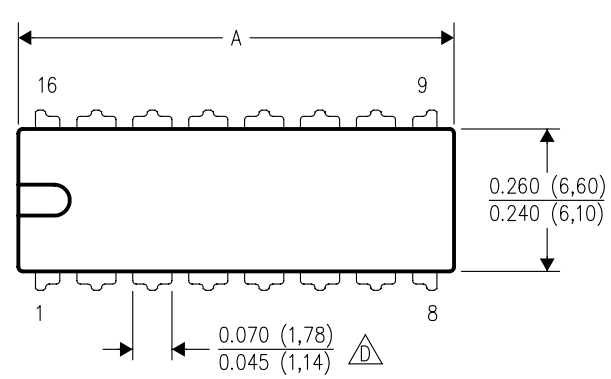


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

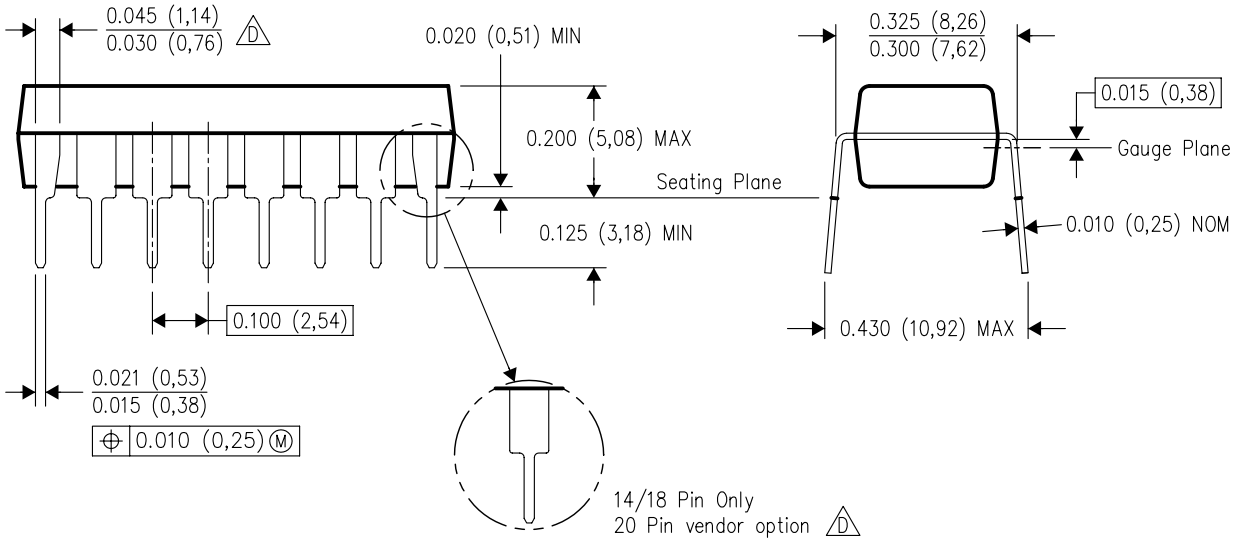
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

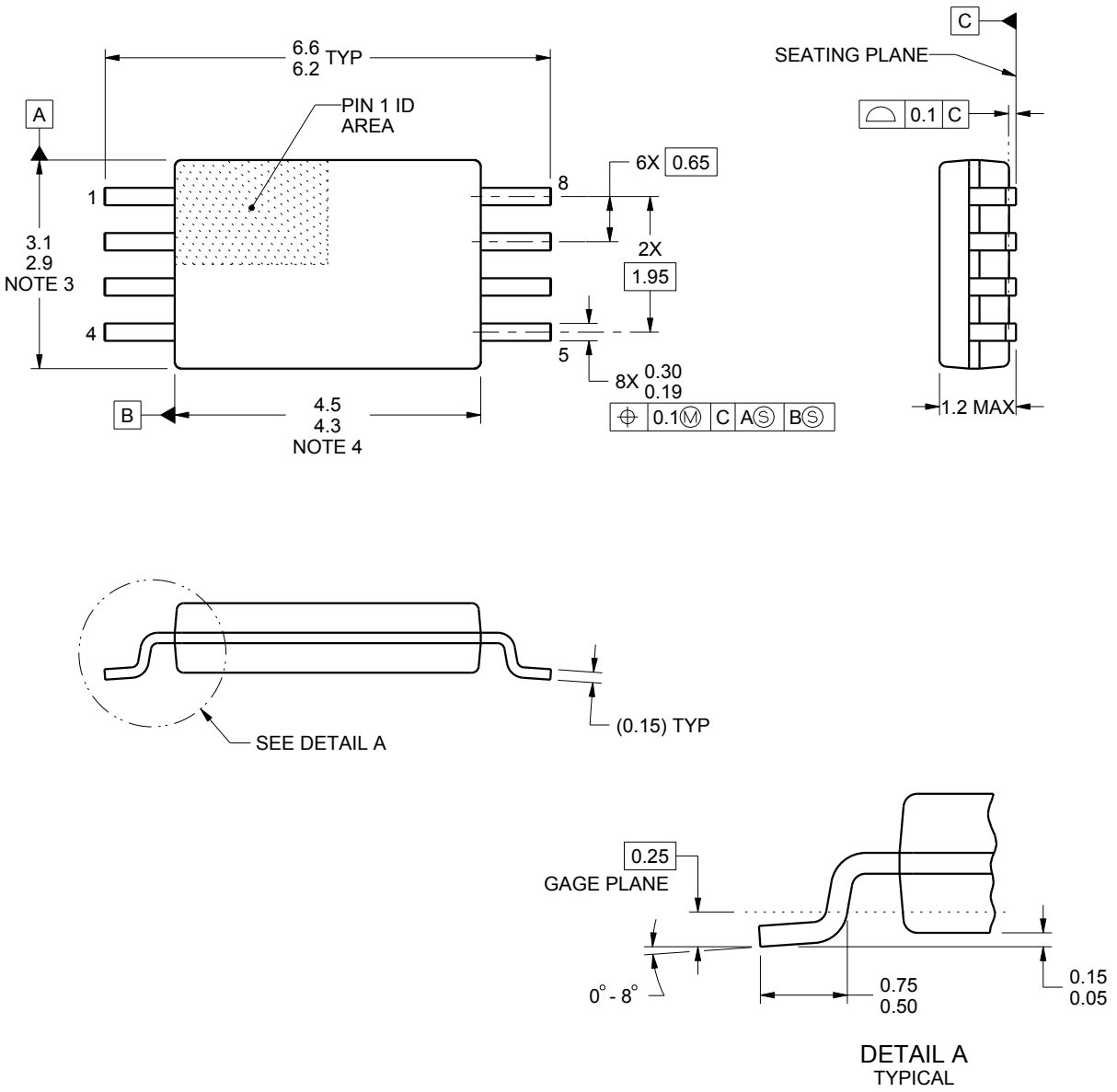
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0008A

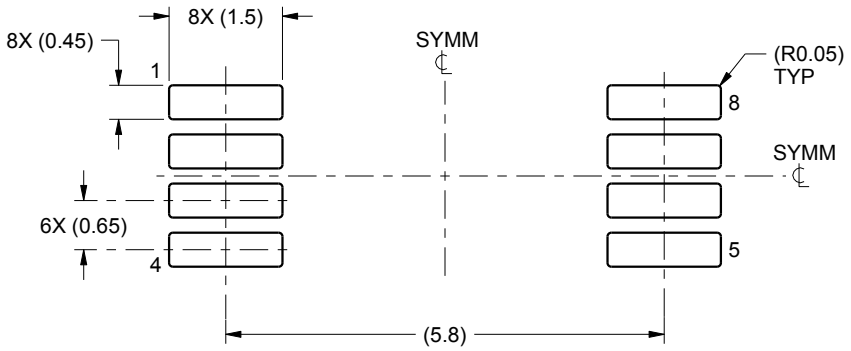
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

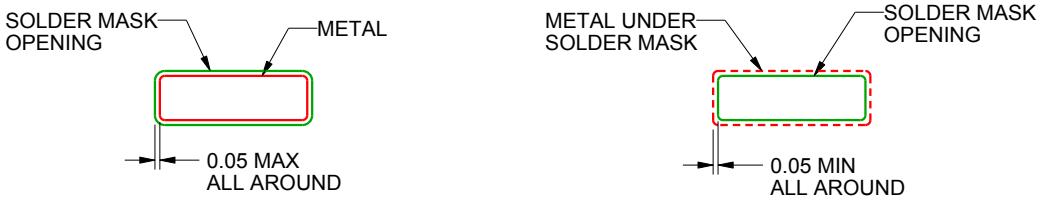


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

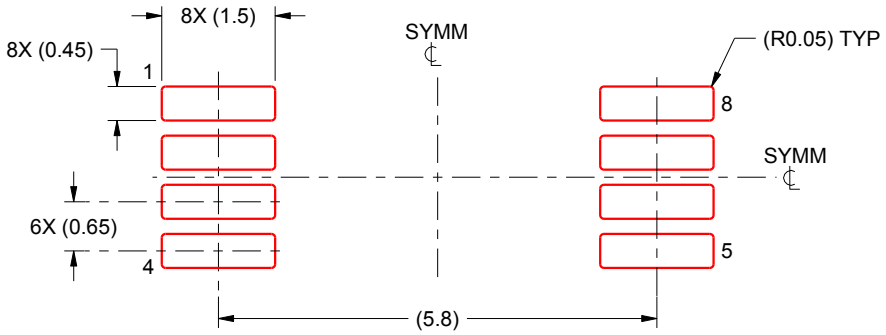


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

MJE15028, MJE15030 (NPN), MJE15029, MJE15031 (PNP)

Complementary Silicon Plastic Power Transistors

These devices are designed for use as high−frequency drivers in audio amplifiers.

Features

- High Current Gain − Bandwidth Product
- TO−220 Compact Package
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage MJE15028G, MJE15029G MJE15030G, MJE15031G	V_{CEO}	 120 150	Vdc
Collector−Base Voltage MJE15028G, MJE15029G MJE15030G, MJE15031G	V_{CB}	 120 150	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous	I_C	8.0	Adc
Collector Current − Peak	I_{CM}	16	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 50 0.40	 W W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

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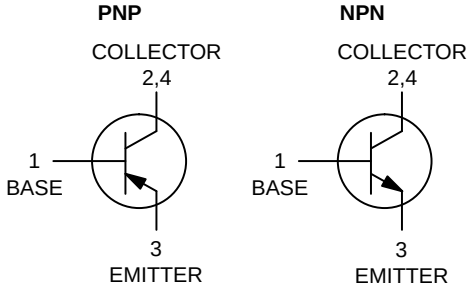
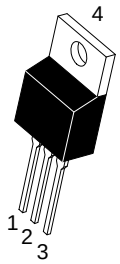
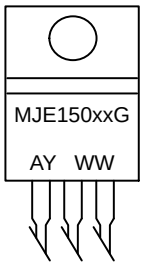
8 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 120−150 VOLTS, 50 WATTS





TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM



MJE150xx = Device Code
x = 28, 29, 30, or 31
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 10 mAdc, I_B = 0) MJE15028, MJE15029 MJE15030, MJE15031	$V_{CEO(sus)}$	 120 150	 − −	Vdc
Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0) MJE15028, MJE15029 (V_{CE} = 150 Vdc, I_B = 0) MJE15030, MJE15031	I_{CEO}	 − −	 0.1 0.1	mAdc
Collector Cutoff Current (V_{CB} = 120 Vdc, I_E = 0) MJE15028, MJE15029 (V_{CB} = 150 Vdc, I_E = 0) MJE15030, MJE15031	I_{CBO}	 − −	 10 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	 −	 10	μAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 2.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 40 40 40 20	 − − − −	−
DC Current Gain Linearity (V_{CE} From 2.0 V to 20 V, I_C From 0.1 A to 3 A) (NPN to PNP)	h_{FE}	**Typ** 2 3		
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	 −	 0.5	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	 −	 1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (Note 2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	 30	 −	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

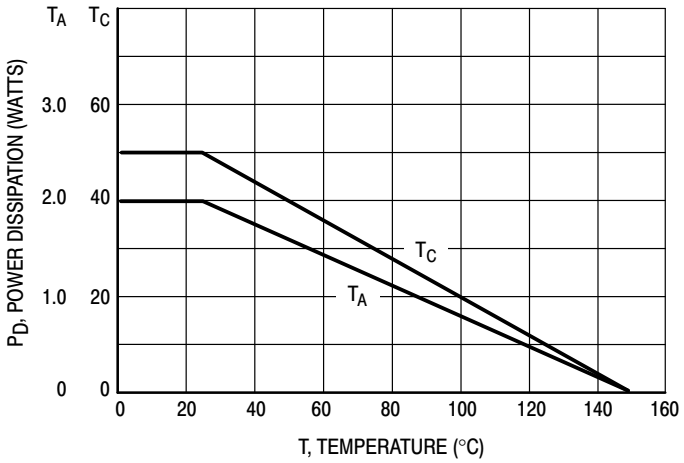


Figure 1. Power Derating

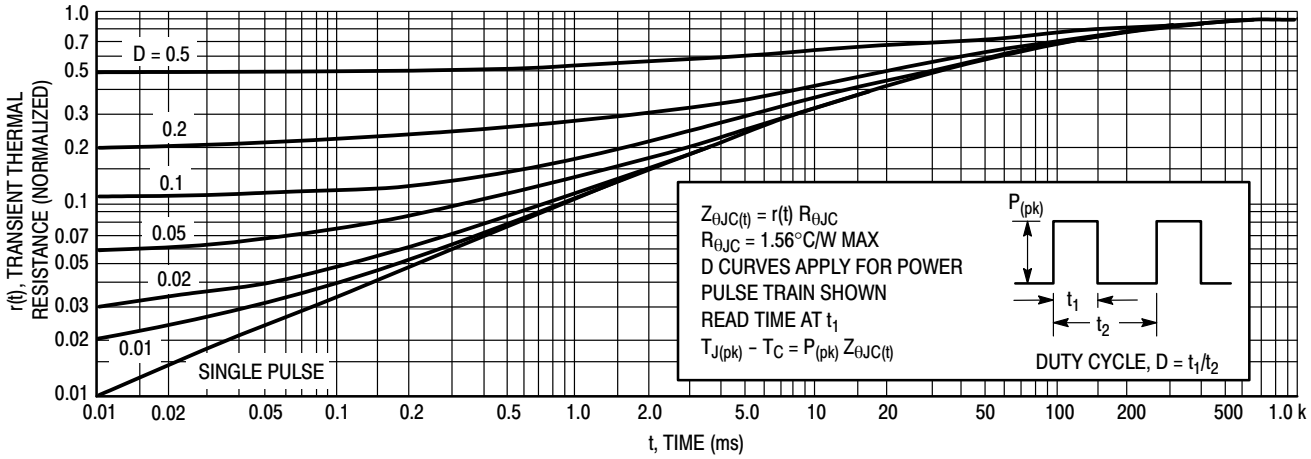


Figure 2. Thermal Response

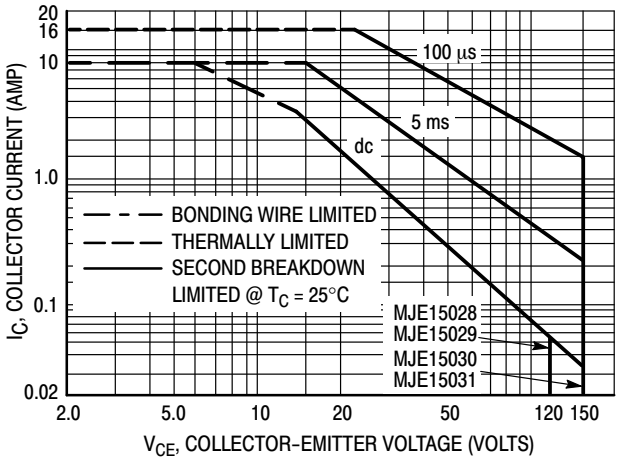


Figure 3. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

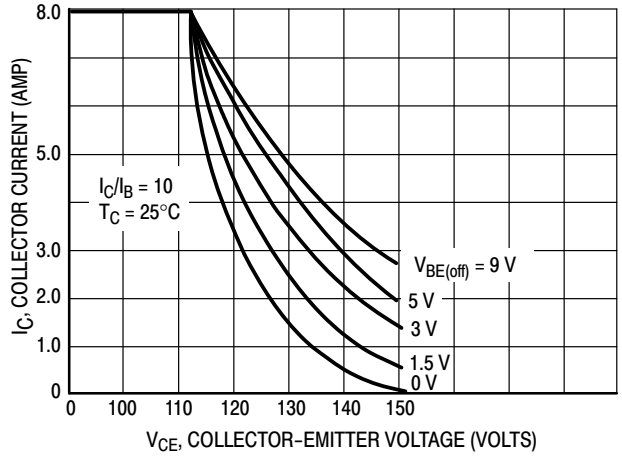


Figure 4. Reverse−Bias Switching Safe Operating Area

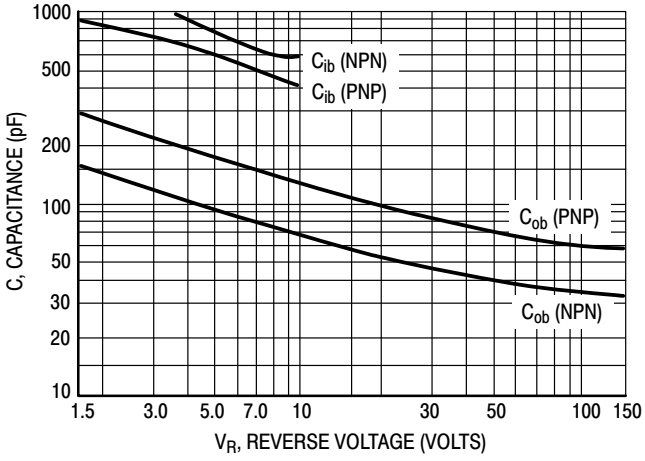


Figure 5. Capacitances

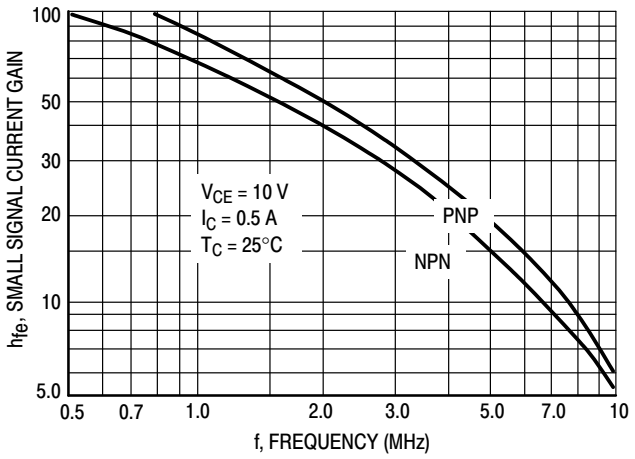


Figure 6. Small−Signal Current Gain

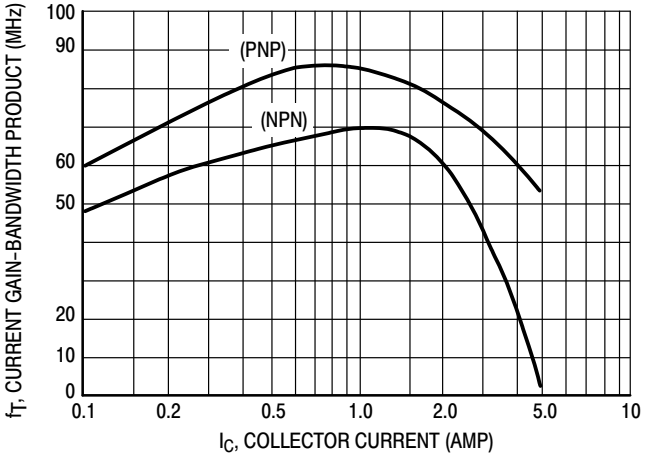


Figure 7. Current Gain−Bandwidth Product

NPN — MJE15028 MJE15030

PNP — MJE15029 MJE15031

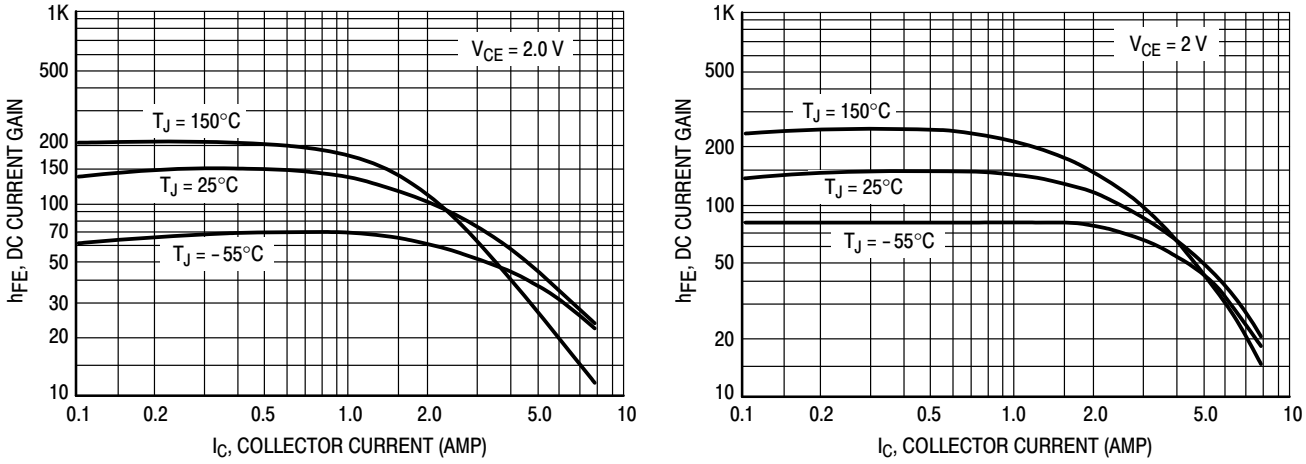


Figure 8. DC Current Gain

NPN

PNP

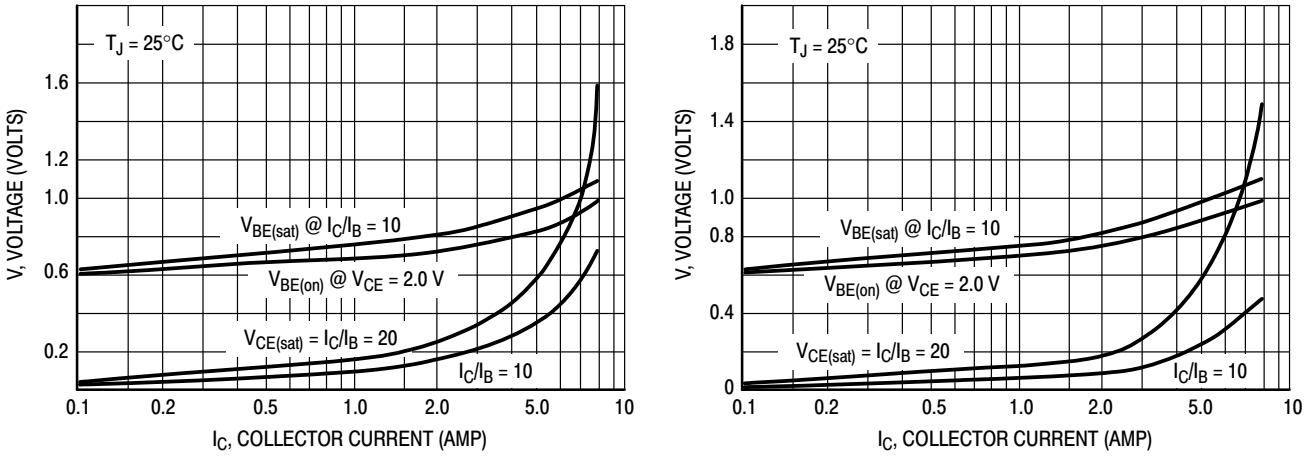


Figure 9. “On” Voltage

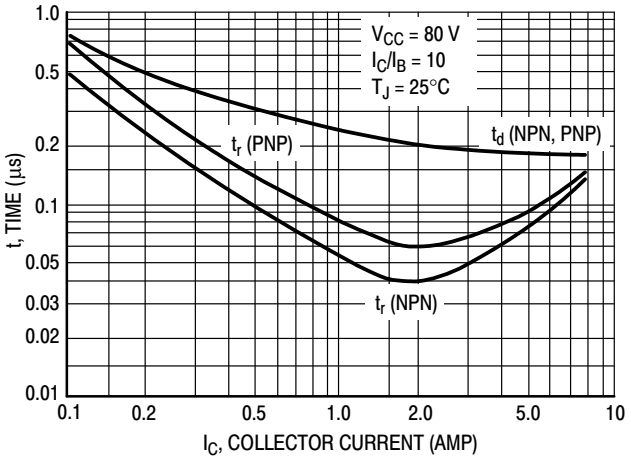


Figure 10. Turn−On Times

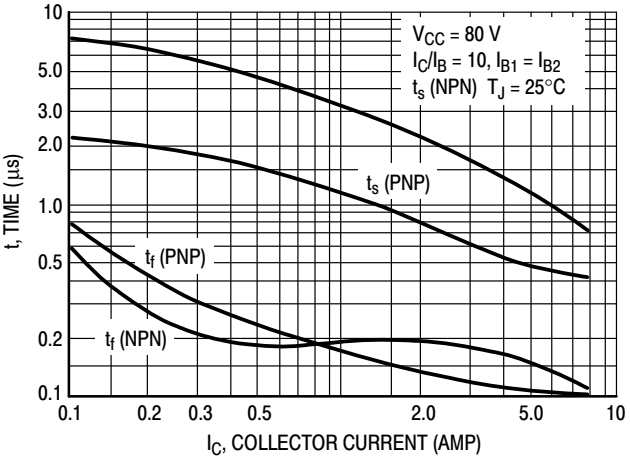


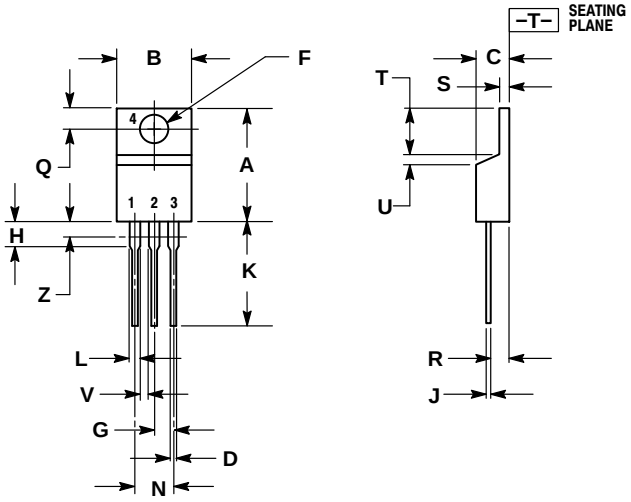
Figure 11. Turn−Off Times

ORDERING INFORMATION

Device	Package	Shipping
MJE15028G	TO−220 (Pb−Free)	50 Units / Rail
MJE15029G	TO−220 (Pb−Free)	50 Units / Rail
MJE15030G	TO−220 (Pb−Free)	50 Units / Rail
MJE15031G	TO−220 (Pb−Free)	50 Units / Rail

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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