30329 - Digital Electronic Systems

Información del Plan Docente

Academic Year	2017/18
Faculty / School	110 - Escuela de Ingeniería y Arquitectura
Degree	438 - Bachelor's Degree in Telecomunications Technology and Services Engineering
ECTS	6.0
Year	
Semester	Second semester
Subject Type	
Module	---

1.General information

1.1.Introduction

1.2.Recommendations to take this course

1.3.Context and importance of this course in the degree

1.4.Activities and key dates

2.Learning goals

2.1.Learning goals

2.2.Importance of learning goals

3.Aims of the course and competences

3.1.Aims of the course

3.2.Competences

4.Assessment (1st and 2nd call)

4.1.Assessment tasks (description of tasks, marking system and assessment criteria)

5.Methodology, learning tasks, syllabus and resources

5.1.Methodological overview

This course covers the systematic design of advanced digital systems using Field programmable gate arrays (FPGAs) and an introduction to ASIC design.

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We will first review in detail the basic building blocks of FPGA programming. Second, we focus on architecture, design methodologies, best design practices, and optimization techniques for performance (frequency, latency, area, power, etc). Finally, we will cover testbench development, simulation for bit-true design verification, and synthesis of complete digital systems.

The emphasis is on FPGA technology, but most of the design techniques can also be applied to ASIC devices.

5.2.Learning tasks

This course includes a combination of lectures, laboratory assignments, and a final exam.

5.3.Syllabus

course topics :

- Advanced VHDL coding

- Fixed point VHDL description.

- FPGA architectures

- High performance FPGA design

- CMOS Technology

- Introduction to ASIC design

- Testbench development

5.4.Course planning and calendar

The schedule of the lectures and lab sessions is posted on the university website.

5.5.Bibliography and recommended resources

- Electrónica digital : aplicaciones y problemas con VHDL / José Ignacio Artigas Maestre, Luis Ángel Barragán Pérez, Carlos Orrite Uruñuela, Isidro Urriza Parroqué Madrid [etc.] : Prentice Hall, D. L. 2002
- Ashenden, Peter J.. VHDL-2008: just the new stuff / Peter J. Ashenden, Jim Lewis Morgan Kaufmann, 2008

recomanded resources:

ISE WebPack **http://www.xilinx.com/support/download/index.htm**