Output voltage estimation of a half-bridge inverter for domestic induction heating applications

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***Abstract*—The power supplied to a vessel by a domestic induction-heating appliance is strongly dependent on several parameters the designer of the system has no control over: the type and the size of the vessel, misalignments between the pot and the inductor, temperatures, etc. A reliable estimation of the power is essential to ensure that the home appliance works under the expected conditions and the user experience is suitable. Furthermore, any reduction of hardware is totally welcome by consumer-electronics manufacturers. In this work, two methods to estimate the output voltage of a half-bridge inverter without digitizing it with an analog-to-digital converter are proposed and the effects that this estimation has on the power calculation are evaluated. Both methods are implemented and experimentally verified in a real prototype with an FPGA (Field-Programmable Gate Array).**

***Index Terms*—Home Appliances, Induction Heating, Digital Signal Processing**

I. Introduction

During the last years, induction hobs have become one of the preferred methods for domestic heating. This is mainly due to its inherent efficiency, cleanness and security compared to the traditional cooking methods [1].

Most of the low-mid cost induction hobs are based on the same topology: the series-resonant half-bridge inverter. The good balance between performance and number/cost of devices of this topology explains its choice [2].

A simplified schematic of the system is shown in Fig. 1. The mains voltage is full-wave rectified and filtered with a small bus capacitor that allows a high ripple, resulting in a power factor close to one [3]. This voltage, called bus voltage, v_{B}, feeds the inverter, which produces the alternating current that flows through the inductor, generating an alternating magnetic field that, due to the induced current losses, heats the bottom of the vessel.

This work was partly supported by the Spanish MINECO under Project TEC2016-78358-R, by the Spanish MICINN and AEI under Project RTC-2017-5965-6, co-funded by EU through FEDER program, by the DGA-FSE, and by the BSH Home Appliances Group.

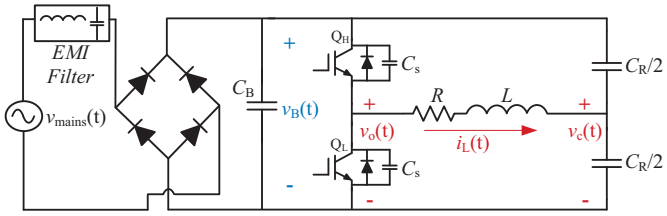

Fig. 1. Simplified schematic of the power electronics of an induction hob.

The equivalent load of the inverter, which represents the electromagnetic interaction between the planar inductor and the ferromagnetic base of the pot, is usually modeled as a series resistive-inductive circuit (R–L) [4]. Besides, in parallel with the semiconductor devices, which switch at frequencies between 35 and 75 kHz, snubber capacitors, C_{s}, are placed to reduce the switching losses and the derivative of the voltage respect to the time, dv/dt [5].

For a given condition (mains voltage and frequency, type of pot, misalignment, temperature...) the power supplied to the load can be controlled by modifying two variables: the switching frequency, f_{sw}, or the duty cycle. The accuracy, in terms of power, required by these applications allows a simplification of the control, maintaining a constant duty cycle of 0.5, and controlling the power by varying only the switching frequency. If the power required by the user is lower than the one supplied at the maximum switching frequency, pulse density modulation (PDM) techniques are used [6].

The most direct non-calorimetric method to calculate the power is to digitize the voltage drop in the load, $v_{\mathrm{L}} = v_{\mathrm{o}} - v_{\mathrm{c}}$, the current that flows through it, i_{L}, and compute the integral of the product during a bus cycle, T_{B}. Assuming that the equivalent series resistance (ESR) of the resonant capacitors is negligible, it could be adequate to measure the output voltage, v_{o}, and the current, i_{L}, with a relatively high bandwidth

(hundreds of kHz). To do so, two high-resolution Nyquist ADCs (analog-to-digital converter) per inverter might be used. Sigma-delta ADCs could also be used, as in [2]. The main drawback of these methods is the cost; for flexible induction surfaces, where a single appliance is made of dozens of small inductors, two ADCs per inverter would lead to unacceptable costs. These costs could be reduced if instead of measuring the power supplied by the inverter, the power supplied by the bus was measured [7]. In this case a lower bandwidth would be required, but unfortunately this method could not be applied to several loads (several inverters connected to the same bus) either. In [8], [9] the output voltage of the inverter is estimated from the bus voltage and the control signals of the semiconductor devices, but the effect of the charging and discharging of the snubber capacitors is not taken into account. An approximation by the first harmonic is proposed in [10], but as it is shown in [11], if the bus voltage is an AC signal, the first harmonic of v_{o} and i_{L} only contains the information of about 80% of the total power, so the error would be too high. Another option would be to use analog circuitry as it is suggested in [12], but this method is very dependable on the temperature and on the ageing of the components.

This work proposes two methods to estimate the output voltage of the inverter without digitizing it. Some parameters, apart from the measurement of the current i_{L} and the voltage v_{B}, are required, but they are known by the designer of the system. Moreover, the effect of the snubber capacitors is taken into account. This method can be specially convenient in induction hobs where more than one inverter is connected to the same bus, so that instead of measuring the output voltage of every inverter, just one ADC is needed to digitize the bus voltage.

The rest of the paper is organized as follows. The methods that estimate the output voltage of the inverter and the theory behind them are detailed in section II. Experimental results of the methods both, offline and in real-time, are reported in section III. Finally, conclusions are drawn in section IV.

II. Estimation Methods

In Fig. 2, the output voltage of the inverter, v_{o}, and the current that flows through the inductor, i_{L}, at peak value of the bus voltage are shown. A switching cycle, assuming zero-voltage switching (ZVS) operating conditions, can be divided into six states (see Fig. 2):

S1) Charging/discharging of snubber capacitors (IGBTs off).
S2) Conduction of upper diode.
S3) Conduction of upper IGBT.
S4) Charging/discharging of snubber capacitors (IGBTs off).
S5) Conduction of lower diode.
S6) Conduction of lower IGBT.

Considering that the collector-to-emitter saturation voltage of the semiconductor devices and the forward polarization voltage of the anti-parallel diode are negligible, it can be assumed that in states S2 and S3 the voltage $v_{\mathrm{o}}(t)$ equals $v_{\mathrm{B}}(t)$ and that in S5 and S6 $v_{\mathrm{o}}(t)$ is 0. In the other states (S1 and S4), the output voltage of the inverter depends on the capacitance

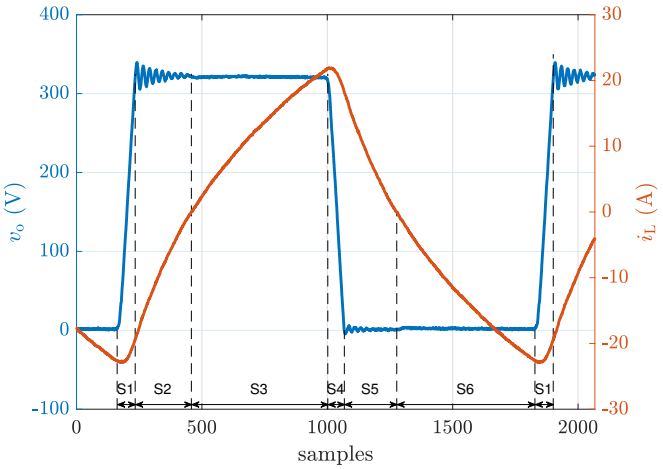

Fig. 2. Output voltage of the inverter, v_{o} (blue), load current, i_{L} (orange), and states of a switching cycle.

of the snubber capacitors and its charging/discharging rate, that is, on $i_{\mathrm{L}}(t)$. From now on, and to ease the reading, the charging and discharging phenomena of the snubber capacitors will be referred just as charging.

The active power supplied to the load can be calculated as the summation of the power supplied by every harmonic:

$$P = \frac{1}{2}\sum_{h=1}^{\infty} \hat{V}_{\mathrm{O}h}\hat{I}_{\mathrm{L}h}\cos(\phi_{vh} - \phi_{ih}), \tag{1}$$

where the amplitude and the phase of the h^{th} harmonic of v_{o} are $\hat{V}_{\mathrm{O}h}$ and ϕ_{vh}, respectively, and the amplitude and the phase of the h^{th} harmonic of i_{L} are $\hat{I}_{\mathrm{L}h}$ and ϕ_{ih}, respectively. From this equation, it can be deduced that any deviation in the phase between v_{o} and i_{L} would introduce an error in the computation of the active power.

The known variables are: the bus voltage, $v_{\mathrm{B}}(t)$, the load current, $i_{\mathrm{L}}(t)$, the control signals of the semiconductor devices, Q_{H} and Q_{L} (generated by a digital modulator), and the propagation delay time of the control signals from the digital modulator to the IGBT (Insulated Gate Bipolar Transistor), t_{prop}, which together with the control signals, is used to know when the IGBTs turn off.

The only difference between the methods is how the output voltage of the inverter is estimated when the snubber capacitors are charging (states S1 and S4), since v_{o} equals v_{B} or 0 in the rest of the states.

A. Integration of the load current

The output voltage of the inverter, during the interval in which the snubber capacitors are charged by the load current, can be approximated as:

$$v_{\mathrm{o}}(t) = v_{\mathrm{o}}(t_0) - \frac{1}{2C_{\mathrm{s}}}\int_{t_0}^{t} i_{\mathrm{L}}(\tau)d\tau \tag{2}$$

where $v_{\mathrm{o}}(t_0)$ can be 0 or $v_{\mathrm{B}}(t_0)$. Applying a rectangular approximation to discretize the integral in (2) with a sampling period of T_{s}, the following equation is obtained:

$$v_{\mathrm{o}}(k) = v_{\mathrm{o}}(k-1) - \frac{T_{\mathrm{s}}}{2C_{\mathrm{s}}} i_{\mathrm{L}}(k). \tag{3}$$

Once (3) is computed, a transition between states S1 and S2 is assumed when $v_{\mathrm{o}}(k) \geq v_{\mathrm{B}}(k)$, moment from which $v_{\mathrm{o}}(k)$ is set to $v_{\mathrm{B}}(k)$. In a similar way, when $v_{\mathrm{o}}(k) \leq 0$, a transition between S4 and S5 is assumed, and $v_{\mathrm{o}}(k)$ is set to 0 from then on.

B. Approximation as a square signal

Given the load current and the value of the snubber capacitors that are normally designed for domestic induction heating, the snubber charging time is relatively small (tens of nanoseconds). This allows approximating the load current as a constant for that interval of time without introducing big errors. Therefore, according to (2), and assuming the load current is constant, $v_{\mathrm{o}}(t)$ would be a linear function of time. Additionally, if the bus voltage is assumed constant (the bus capacitor facilitates this approximation), the output voltage of the inverter can be approximated as a trapezoid signal, like the one shown in 3.(a).

A further simplification would let us to approximate this trapezoid as a square signal. But according to (1), this simplification should not change the phase between the current and the voltage, that means the phase between the square and the trapezoid signal has to be null. To fulfill this requirement it is necessary to calculate the β angle of the square signal as a function of the γ angle of the trapezoid signal (see Fig. 3).

Referring to [12] and using the Fourier series equation, the Fourier coefficients of both signals are obtained:

$$\begin{aligned}
a_{h,\mathrm{tr}} &= -\frac{A\,(\cos(\pi\,h) + \cos(h\,\gamma) - \cos(h\,(\gamma-\pi)) - 1)}{h^2\,\gamma\,\pi} \\
b_{h,\mathrm{tr}} &= -\frac{A\,(\sin(\pi\,h) - \sin(h\,\gamma) + \sin(h\,(\gamma-\pi)))}{h^2\,\gamma\,\pi} \\
a_{h,\mathrm{sq}} &= \frac{A\,(\sin(h\,\beta) - \sin(h\,(\beta-\pi)))}{h\,\pi} \\
b_{h,\mathrm{sq}} &= \frac{A\,(\cos(h\,\beta) - \cos(h\,(\beta-\pi)))}{h\,\pi},
\end{aligned} \tag{4}$$

where subindex tr refers to trapezoid, subindex sq refers to square, h is the harmonic index, and A is the amplitude of the signal. The phase of a function expressed as a Fourier series, for harmonic h is:

$$\phi_h = \arctan\frac{b_h}{a_h}. \tag{5}$$

If the coefficients in (4) are evaluated for the first harmonic, $h = 1$, and the phases are equaled, $\phi_{h,\mathrm{sq}} = \phi_{h,\mathrm{tr}}$, the following equation is obtained:

$$\frac{\cos(\gamma) - \cos(\gamma-\pi) - 2}{\sin(\gamma-\pi) - \sin(\gamma)} = \frac{\sin(\beta) - \sin(\beta-\pi)}{\cos(\beta) - \cos(\beta-\pi)}. \tag{6}$$

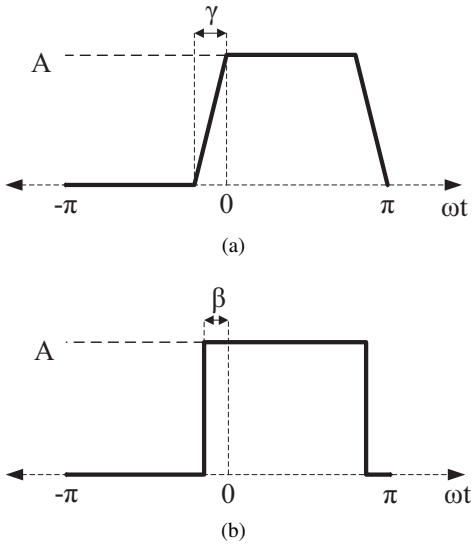

Fig. 3. Output-voltage approximations. (a) Trapezoid signal. (b) Square signal.

Rearranging (6) and applying basic trigonometry:

$$\tan(\beta) = \frac{1-\cos(\gamma)}{\sin(\gamma)}. \tag{7}$$

If (7) is compared to the tangent half-angle trigonometric identity, it can be deduced that it is only fulfilled if $\beta = \gamma/2$. For this value of β, the first-harmonic delay between the trapezoid and the square signals is null, and this will allow approximating the voltage v_{o} as a square signal.

Furthermore, since $v_{\mathrm{o}}(t)$ was considered to be a linear function of time, generating the edge of $v_{\mathrm{o}}(t)$ when $\beta = \gamma/2$ would be equivalent to do so when $v_{\mathrm{o}}(t) = v_{\mathrm{B}}(t)/2$.

If this method performs correctly, it would prove the feasibility of using analog comparators between v_{o} and $v_{\mathrm{B}}/2$. This approach could be considered if the output voltage of the inverter could not be measured or the designer of the system did not want to estimate it as it is suggested in this work.

The proposed methods should be applicable even if comparators are not available, that is why it is necessary to reconstruct the output voltage of the inverter until, at least, $v_{\mathrm{o}}(t)$ equals $v_{\mathrm{B}}(t)/2$. In this case, it is done by integrating the load current, as it is explained in section II-A.

III. Experimental Results

The experimental prototype consists of some essential parts of an induction hob (EMI filter, inductors, ceramic glass...) and the required PCBs (printed circuit board) which were designed to provide it with the appropriate flexibility. The control of the system and the proposed methods were implemented in the System On Chip (SoC) Zynq-7020 of Xilinx.

The active power supplied to the load in a bus cycle, T_{B}, neglecting the ESR term of the resonant capacitor, and

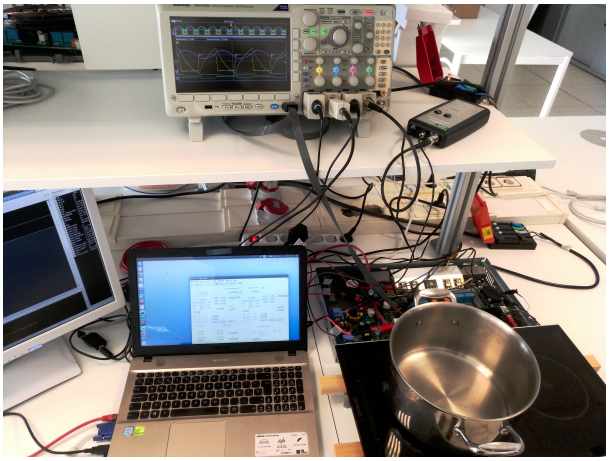

Fig. 4. Experimental setup.

subtracting the potential effect of the voltage and the current offset is:

$$P = \frac{1}{T_{\mathrm{B}}} \int_0^{T_{\mathrm{B}}} v_{\mathrm{o}}(t) i_{\mathrm{L}}(t) dt - \frac{1}{T_{\mathrm{B}}^2} \int_0^{T_{\mathrm{B}}} v_{\mathrm{o}}(t) dt \int_0^{T_{\mathrm{B}}} i_{\mathrm{L}}(t) dt \tag{8}$$

With the aim of evaluating a wide range of powers, these methods have been tested at switching frequencies between 35 and 75 kHz. Given the specific components of the prototype, shown in Table I, these frequencies ensure the system works under ZVS conditions and imply a supplied power between 500 and 2200 W. This power was calculated with raw data captured with a Tektronix MDO3024 oscilloscope sampling at 100 Msps.

Firstly, these methods were implemented offline in MATLAB, using the signals captured with the oscilloscope. Once the methods were tested and validated, they were implemented in real time into the SoC.

A. *Offline Implementation*

A comparison between the measured output voltage of the inverter, and the estimated ones is shown in Fig. 5.

First-order anti-aliasing filters with a cutoff frequency of 360 kHz are used for the acquisition of the signals in the prototype. An equivalent digital IIR (infinite impulse response) filter was designed and applied to the signals captured with the oscilloscope, so that the results were more easily comparable.

TABLE I
PARAMETERS OF THE PROTOTYPE

Symbol	Description	Value
$\hat{V}_{\mathrm{B}}$	Bus voltage (peak value)	325 V
f_{red}	Mains frequency	50 Hz
t_{prop}	Propagation delay time of control signals	330 ns
R	Equivalent resistance	2.7 - 5.3 Ω
L	Equivalent inductance	24.5 - 30.5 µH
C_{B}	Bus capacitor	3.3 µF
C_{R}	Resonant capacitor	1080 nF
C_{s}	Snubber capacitor	15 nF

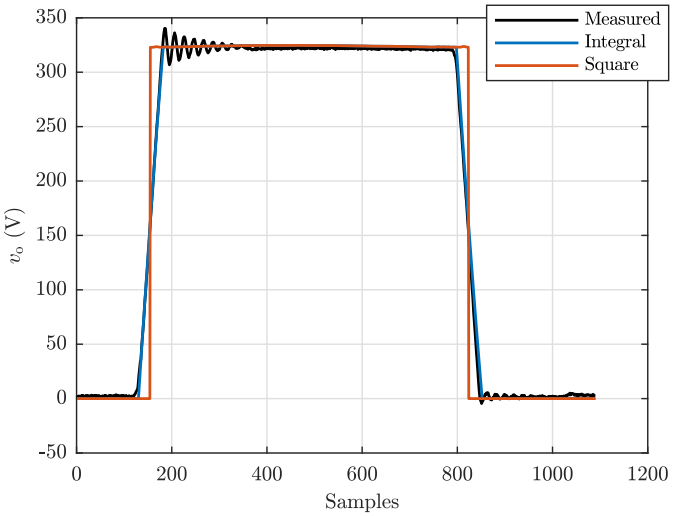

Fig. 5. Output voltage of the inverter: raw data (black), integral approximation (blue), square signal (orange). No digital filter was applied to these signals to ease the visualization.

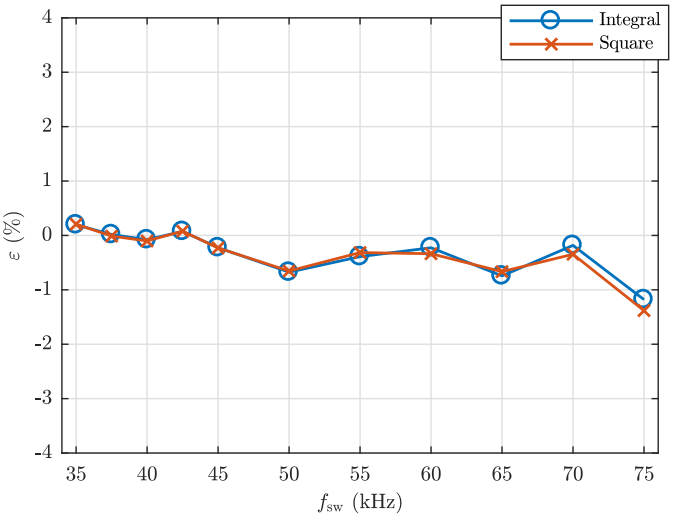

Fig. 6. Relative errors (%) in the computation of the active power for the methods proposed. Raw data from oscilloscope.

The relative errors of the active power calculation are shown in Fig. 6. They have been calculated with (8) and the reference is the active power obtained with the raw data from the oscilloscope.

The errors are below 1.5%, in absolute value, for any tested switching frequency. Besides, both methods show very similar errors, confirming the validity of the assumptions made to estimate the output voltage of the inverter as a square signal.

It is worth mentioning that a small deviation, Δ, in the calculation of the parameter t_{prop}, could introduce some errors in the estimation of the output voltage and, consequently, in the power computation. These errors have been quantized at different Δ values for the first method (integral of current) and are shown in Fig. 7.

With an appropriate t_{prop}, the results seem promising, but

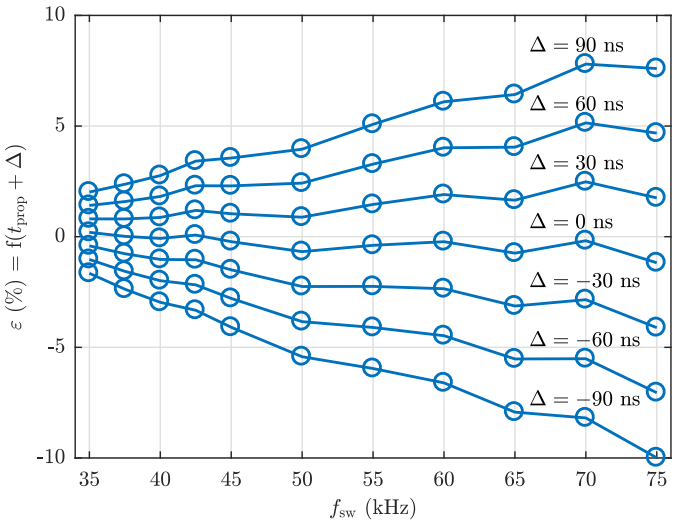

Fig. 7. Influence of Δ on the relative error of the power (integral approximation).

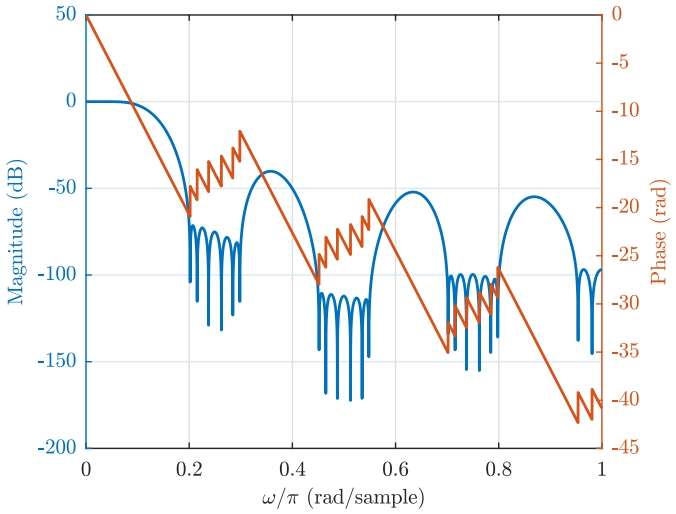

Fig. 8. Frequency response of the half-band interpolation filter.

the sampling frequency of the offline implementation is 100 Msps, which is much higher and therefore less challenging than the sampling frequency available in the prototype.

B. Real-Time Implementation

12-bit SAR (Successive Approximation Register) Nyquist ADCs are mounted in this prototype. The serial peripheral interface (SPI) to control the ADCs, which sample at 2.78 Msps, is implemented in the Zynq device, and the clock frequency of the programmable logic (PL) is set to 100 MHz.

Since the charging rate of the snubber capacitors is in the order of tens of nanoseconds, the current cannot be properly integrated to reconstruct the output voltage with this relatively slow sampling time. That is why the real-time implementation is more challenging and interpolation filters are needed.

Two factors have been considered when selecting the interpolation filter: a low computational complexity and a small

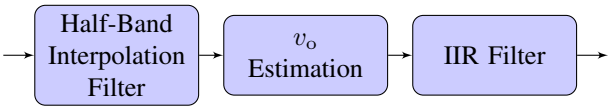

Fig. 9. Block diagram of the real-time implementation.

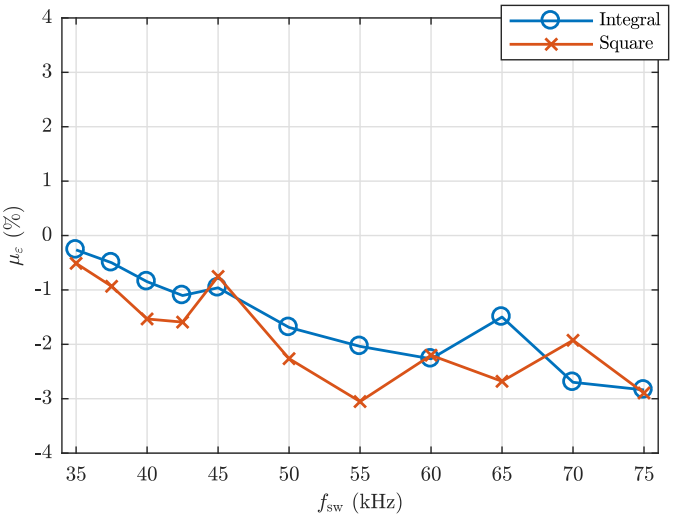

Fig. 10. Mean error (%) in the computation of the active power for the methods proposed. Real time implementation.

group delay. In these terms, the FIR (finite impulse response) half-band filters perform very well [13]. Some of its properties are: every tap reduces the bandwidth of the sampled signal by a factor of approximately two, if the number of coefficients is odd, all the odd coefficients are null, except the central one. Besides, its phase is linear, so the group delay is constant for any frequency, and all its coefficients are symmetric respect to the center. All these characteristics lead to a potentially efficient implementation.

One of the constraints of this type of filters is its upsampling factor, L_{up}: it has to be a power of two. Since a small sampling time is required for the integration of the current, an upsampling factor of 8 was chosen, resulting in a sampling frequency of 22.2 Msps.

The frequency response of the interpolation filter is shown in Fig. 8, where the magnitude appears normalized by L_{up}. This filter consists of three taps, each of them running at a different frequency and increasing the sampling frequency by two respect to the previous one. The first two taps are made of 11 coefficients, while the last one is only made of 7. By sequencing the operations, the number of multipliers used by the PL is optimized, requiring just one multiplier per tap.

A custom IP (Intellectual Property) core was designed to perform the estimation of the output voltage, together with the interpolation filter and the calculation of the active power according to (8). Moreover, the harmonic content of the reconstructed output voltages widely differ from the one of the measured output voltage; that is why a first-order digital IIR filter with a cutoff frequency of 360 kHz was also

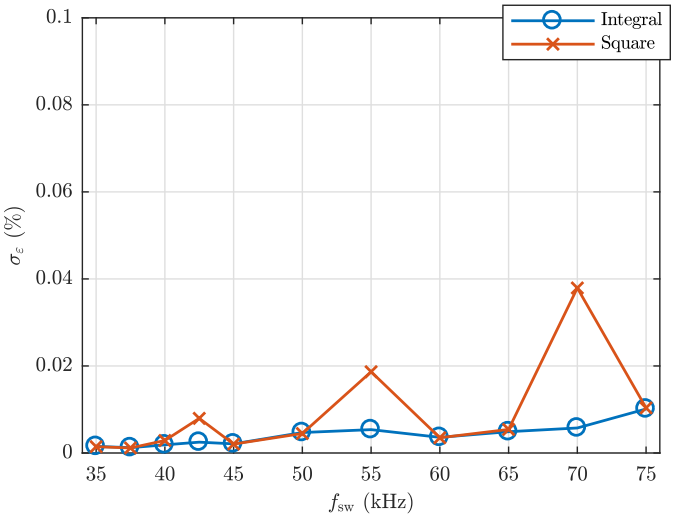

Fig. 11. Standard deviation (%) of the error in the computation of the active power for the methods proposed. Real time implementation.

implemented in the SoC and applied to the integral and square approximation of the signals. A block diagram of the real-time system is shown in Fig. 9.

The active power was calculated for three different cases: v_o digitized with one of the mentioned ADCs and interpolated, v_o approximated by the integral of the current, and v_o approximated as a square signal. The switching frequency was also set to between 35 and 75 kHz, and power supplied to the load per bus cycle was calculated and saved in a RAM memory for 2500 consecutive bus cycles, i.e. 25 seconds.

Fig. 10 shows the average relative error of the active power for the presented methods during these 25 seconds. The reference is the power obtained with the digitized and interpolated output voltage. This error is less than 4% for any frequency.

The standard deviation of these errors can also be observed in Fig. 11. It remains below 0.05%, what shows the robustness and repeatability of the methods. This standard deviation is slightly higher at high switching frequencies. At low switching frequencies, the power supplied to the pot is high enough to keep the water boiling, what helps the stabilization of the temperature and the system. Even taking care to measure the power at a steady state, the change of temperature along the 25 seconds might have had a mentionable impact on the standard deviation.

IV. Conclusion

Two methods to estimate the output voltage of a half-bridge series resonant inverter were proposed and analyzed in this work. The fact of not measuring this voltage with an ADC would potentially reduce the cost that manufacturers have to bear without incurring in big errors.

The presented methods are dependent on the snubber capacitors and the propagation delay time, t_{prop}. Hence, the ageing and the tolerances of the components could affect the performance of the methods. Fortunately, with the development of new technologies, the increasing quality of the components and the drop of its tolerances over the years, the variability of these methods would be less affected. Even though, the effect of a wrong estimation of t_{prop} was also evaluated.

The methods were tested offline and validated in a real-time implementation. For this second case, an interpolation filter, with an upsampling factor of 8, was designed. The errors remain below 4% for any tested switching frequency, which is perfectly acceptable for this application.

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