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1.0 V-0.18 µm CMOS Tunable Low Pass Filters with 73 dB DR for On-Chip Sensing Acquisition Systems

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Abstract: This paper presents a new approach based on the use of a Current Steering (CS) technique for the design of fully integrated G_m–C Low Pass Filters (LPF) with sub-Hz to kHz tunable cut-off frequencies and an enhanced power-area-dynamic range trade-off. The proposed approach has been experimentally validated by two different first-order single-ended LPFs designed in a 0.18 µm CMOS technology powered by a 1.0 V single supply: a folded-OTA based LPF and a mirrored-OTA based LPF. The first one exhibits a constant power consumption of 180 nW at 100 nA bias current with an active area of 0.00135 mm^2 and a tunable cutoff frequency that spans over 4 orders of magnitude (~100 mHz–152 Hz @ C_L = 50 pF) preserving dynamic figures greater than 78 dB. The second one exhibits a power consumption of 1.75 µW at 500 nA with an active area of 0.0137 mm^2 and a tunable cutoff frequency that spans over 5 orders of magnitude (~80 mHz–~1.2 kHz @ C_L = 50 pF) preserving a dynamic range greater than 73 dB. Compared with previously reported filters, this proposal is a competitive solution while satisfying the low-voltage low-power on-chip constraints, becoming a preferable choice for general-purpose reconfigurable front-end sensor interfaces.

Keywords: Analog Low Pass Filter (LPF); CMOS design; sub-Hz cut-off frequencies; low-voltage low-power

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1. Introduction

The achievement of low form factor system-on-chip (SoC) sensing devices with extended battery life or even battery-less systems capable of measuring a great variety of parameters makes the design of every single block within a general-purpose front-end sensor interface a challenge. A front-end sensor interface (Figure 1a) typically includes a transducer to convert the parameter to be measured into an electrical signal; next, a preconditioning stage consisting of a low-noise preamplifier (LNP) amplifies the signal and the low-pass filtering stage (LPF) takes out the out-of-band interferences and noise; finally the digitalization stage (ADC) allows further signal processing by a µC to extract the desired signal information [1–4]. In these acquisition systems, the analog low pass filter (LPF) is required to have a suitable low-cutoff frequency range, which in the case of biosignal front-end interfaces is mainly in the order of tens or hundreds of Hz (Table 1).

Another key application requiring SoC LPFs is an impedance-sensing device. Electrochemical Impedance Spectroscopy (EIS) characterizes a sample by exciting it with a small AC signal, minimizing the probability of damaging the sample, and recovering its impedance over a frequency range. The Frequency Response Analyzer (FRA-EIS) technique is based on dual (0, 90°) synchronous demodulation, that is, it uses a technique known as phase-sensitive detection (PSD) to extract at an excitation frequency f_0 the real and imaginary response. As shown in Figure 1b, the signal is typically amplified by an instrumentation amplifier (IA), then a mixer working at the same frequency f_0 (0, 90°) demodulates the signal, and a low pass filter (LPF) extracts the DC components X-Y, proportional to the real and imaginary response, while noisy signals at other frequencies

are filtered [5–11]. In this case, the LPF is going to be used as a DC magnitude extractor at the last stage of the FRA-EIS read-out system to recover the signal, and it is required to have an adjustable value in the order of sub-Hz to Hz (Table 1) to adjust the accuracy-speed trade-off. Low cutoff frequencies will show better accuracy at the expense of larger acquisition times, while higher cutoff frequencies would speed up the acquisition process reducing the accuracy. This is because the LIAs can be considered as band-pass filters with a quality factor Q = (f0/fc), where f0 is the reference frequency and fc the low-pass filters cutoff frequency. Hence, the smaller the LPF cutoff frequency, the better the noise rejection and the better the recovery accuracy, but compromising related acquisition times.

The implementation of such low-frequency range LPFs in a fully integrated manner is not trivial and becomes especially challenging for portable systems, which require a low voltage design and a reduced area. In fact, Low Pass Filters with sub-Hz cutoff frequencies are generally implemented with external RC elements [12–14].

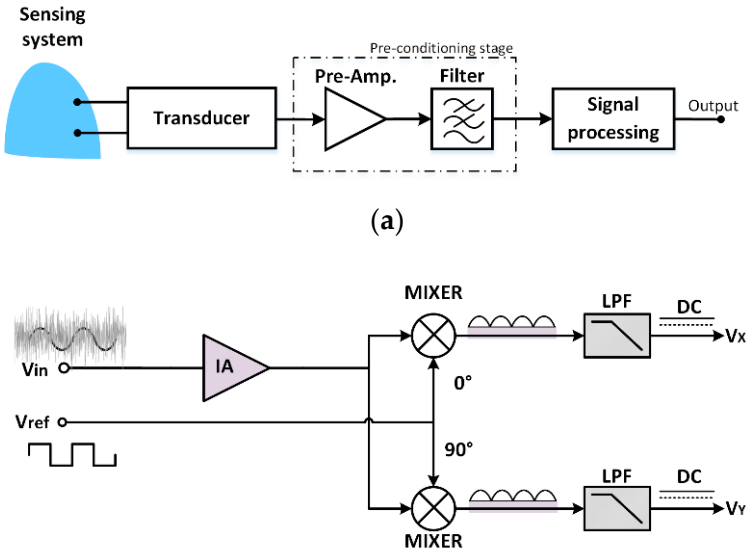


Figure 1. Block diagram of (**a**) general-purpose front-end sensor interface, and (**b**) dual-phase FRA-based electrochemical impedance spectroscopy (FRA-EIS).

Table 1. Review of signals and their range of operation.

Technique	Signal	Frequency Range
Biosignal front-end interface [1,15]	Blood flow	DC–20
	EMG	10–200
	ECG	0.01–250
	Phonocardiography	5–2 k
	Nerve potential	DC–10 k
Impedance Spectroscopy [9,16,17]	Gas detection, Molecular diagnosis, Cell evaluation	Sub-Hz–10

The most common approach to achieve such low cut-off frequencies in a fully integrated way relies on G_m–C structures because of their topological simplicity. The load capacitor is typically a fixed value, which is set around 50 pF as the maximum practical on-chip capacitance preserving an efficient silicon area. To reach sub-Hz cutoff frequencies with these capacitances, G_m~nS are needed, which can be accomplished through bias currents ~pA, benefiting power efficiency. However, the problems for reliably generating such low bias currents on-chip commonly leads to work with higher biasing current values

(~10–100 nA), making it necessary to incorporate transconductance reduction techniques for reliably reaching sub-Hz cut-off frequencies. Among them, in a power-constrained scenario, G_m reduction can be effectively achieved through series-parallel current attenuation to benefit power efficiency [18], but these solutions jeopardize the area to achieve a good matching of transistors. On the other hand, G_m–C topologies exhibit moderate linearity and noise performance so that the power is usually increased to achieve a certain dynamic range (DR), a compromise existing between power, area, and dynamic range (linearity and noise) in LPFs implemented following a G_m–C approach with cutoff frequencies within the ranges of operation shown in Table 1.

Focusing on front-end interfaces, a review of the literature evidence that some of the LPF proposals present power consumptions of several μW not being compatible with portable devices (10 μW [19,20] has a total of 30.4 μW and [21] 233 μW). While those that present power consumption below the μW, either are expensive in terms of area consumption, which is a drawback for portable systems, (0.24 mm^2 [1] and 0.168 mm^2 [2]) or they achieve low power through bias currents too small to be generated on-chip with enough reliability (500 pA [22], from 300 pA to 900 pA [2] or 1 nA [23]). Among those that satisfy the power and area constraints, a high dynamic range (>60 dB) is required to ensure the recovery of the signals, but the reported papers show DR below these value ([24] 54.6 dB, 50 dB [25], 34 dB [26], and 49.9 dB [27]). Moreover, most of the previously reported papers have constant cutoff frequencies (f_c) commonly doing the recovery of a single biomarker. Such is the case of some of the previously mentioned works: [1,25,27] present f_cs of 250 Hz, 50 Hz and 250 Hz for electrocardiogram detection (ECG); [20] implantable devices for nerve-cuff signal recording work at 0.22 Hz and [26] has an f_c of 5.4 kHz for signal processing in neural recording implants. Meanwhile, a review of recent integrated proposals for impedance devices shows that most of the LPFs employed with sub-Hz cutoff frequencies are designed as external passive RC filters [12,28]. As for fully integrated solutions, [29] presents the low pass filter embedded, but it is a second-order RC filter with a fixed 300 Hz cutoff frequency, dominating the 3.6 mm^2 active area consumption of the proposal.

Thus, it is clear that the achievement of a general-purpose high-performance low pass filter (LPF), covering the full frequency range from sub-Hz to hundreds of Hz with a high dynamic range (DR) to enhance the signal resolution while realizing a highly efficient CMOS topology in terms of power and area, still remains a challenge in analog circuit design, demanding new techniques and strategies to meet simultaneously all these required performances into a SoC. The design of such a LP filter is the motivation of this work, with the targeted design specifications: tunable cutoff frequency covering the main signal ranges of Table 1, power consumption below the ~μW; area below ~0.1 mm^2; bias currents greater than ~10–100 nA to be reliably generated on-chip and a dynamic range above 60 dB.

Our proposal is based on a fixed g_m input stage, with a continuously adjustable current steering (CS) technique in the output branch, which allows for G_m–reduction and tunability. This technique has been previously presented in [30] applied to a 1.8 V mirrored Operational Transconductance Amplifier (OTA). This work presents and validates the experimental results of a modified 1.0 V-0.18 μm integrated LPF, also based on a mirrored OTA whose preliminary simulation results were presented in [31]; and a 1.0 V-0.18 μm specifically designed LPF using a folded-cascode core OTA to achieve an ultra-efficient power and area architecture. Both approaches exhibit wide tunable cut-off frequencies (~80 mHz–~1.2 kHz Mirrored, ~100 mHz–152 Hz Folded), low power (1.75 μW@I_{bias} = 500 nA-Mirrored and 180 nW, @I_{bias} = 100 nA-Folded), and reduced size (0.0137 mm^2-Mirrored and 0.0135 mm^2-Folded), while keeping a high dynamic range (>73 dB-Mirrored and >78 dB-Folded), enhancing the state-of-the-art power-area-DR trade-off. In this way, it will be suitable for a wide variety of sensing interfaces, so that it can be modularly used in an array system saving power, area and complexity.

The paper is organized as follows: Section 2 describes the proposed G_m–C topologies with the G_m-reduction strategy followed and in Section 3 the experimental results are summarized. Finally, conclusions are drawn in Section 4.

2. Low Pass Filter Proposed Topology

The proposed topologies for the two first-order single-ended G_m–C integrators based on the CS approach are presented in this section. A fixed integrating capacitor set to 50 pF is used for both of them, implemented by a MOS capacitor to save area, and differ in the core OTA architecture. These core OTAs are firstly presented, followed by the G_m–reduction modifications introduced in each topology, and finally three integrated versions –one based on the Mirrored OTA and two based on the Folded Cascode OTA– of the LPF are introduced.

2.1. Core OTAs

The considered core cells are shown in Figure 2. Figure 2a is the mirrored cascode OTA previously reported on [31], while Figure 2b shows a folded cascode OTA. The latter was chosen to preserve high performance with a 1.0 V voltage supply and because, while the mirrored OTA needs to be cascoded to apply the current steering (CS) technique, with the folded OTA the folding itself is enough to embed the CS technique.

The mirrored OTA is a classic structure with transconductance $G_m = kg_{m1}$, g_{m1} being the transconductance of the differential input pair transistor M1 and k the gain factor of the current mirror. A NMOS-input pair was used with a small g_{m1} in the order of ~µS and unity gain (k = 1) current mirrors to keep the gain, G_m, reduced. This scheme provides the same gain $G_m = g_{m1}$ as a classic differential pair, but uncouples the input and output common-mode range at the cost of doubling the power consumption [30].

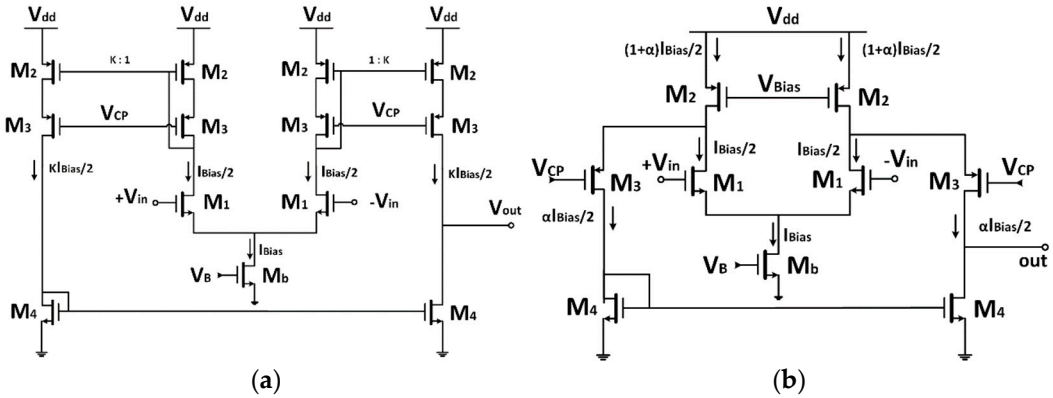


Figure 2. Core: (**a**) Mirrored OTA; and (**b**) Folded Cascode OTA.

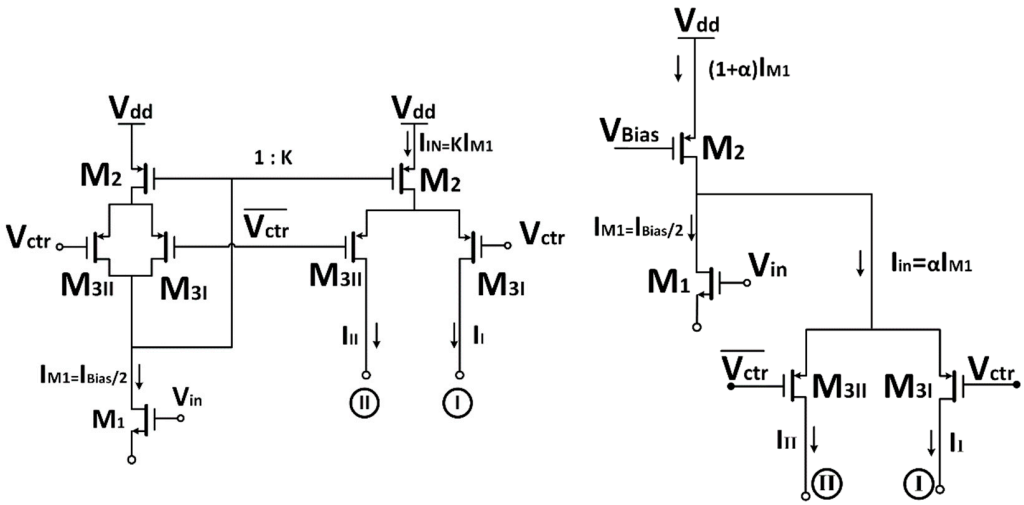
The folded cascode OTA is a single-stage high-gain structure, which requires a lower supply voltage than a typical cascode amplifier. Again, the M1 NMOS-input differential pair is biased at a constant current I_{Bias}, introduced to the circuit through a simple MB 1:1 current mirror. This keeps g_{m1} constant (~µS by design) with transistors M1 in saturation region. The folded branches carry a current $\alpha < 1$ times less than that of the main pair transistors, i.e., $\alpha I_{Bias}/2$, to reduce the power consumption while enhancing the OTA gain and minimizing noise. In this way, through each PMOS M2 biasing transistors the total current is $(1 + \alpha)I_{Bias}/2$. For this scheme, again the overall transconductance gain is $G_m = g_{m1}$.

2.2. Gm Tuning Technique

To achieve a variable transconductance gain, both OTAs keep the input pair transconductance, g_{m1}, constant by keeping the bias current, $I_{Bias,}$ constant (Figure 2), and a current steering transfer section conveys the scaled current to the output. This is done, as shown in Figure 3, by splitting each M3 cascode current mirror transistor into two matched transistors $M3_I$ - $M3_{II}$ with their cascode gate voltage V_{CP} replaced by complementary control voltages $V_{ctr} = V_{CP} + V_{gc}$ and $(\overline{V_{ctr}}) = V_{CP} - V_{gc}$ [32].

Following the current steering applied to the mirrored OTA (Figure 3a), transistors M2 present the same V_{ds} and V_{gs}, as we set unity gain for the current mirrors, having $I_{in} = I_{out} = kI_{M1} = I_I + I_{II}$ with k = 1. The output current is split into two complementary currents $I_I = (1 - \beta)\, I_{in} = (1 - \beta)\, I_{M1}$ and $I_{II} = \beta I_{in} = \beta I_{M1}$, with a value β dependent on V_{gc}, comprehended between 0 and 1, and with $I_{II} > I_I$ when $V_{gc} > 0$; $I_I = I_{II}$ when $V_{gc} = 0$ and $I_{II} < I_I$ when $V_{gc} < 0$. Therefore, the transconductor scheme consists on a fixed gain V-I conversion input stage, followed by a current steering transfer section that conveys the scaled current to the output, so that the overall G_m is $G_{mI} = (1 - \beta)\, g_{m1}$ and $G_{mII} = \beta g_{m1}$, being the output located in branch I.

As for the current steering applied to the folded OTA (Figure 3b), the current $I_{in} = \alpha I_{M1}$ ($\alpha < 1$) is split into complementary currents $I_I = (1 - \beta)\, I_{in} = (1 - \beta)\, \alpha I_{M1}$ and $I_{II} = \beta I_{in} = \beta\alpha I_{M1}$ ($I_{in} = \alpha I_{M1} = I_I + I_{II}$). Each output current has adjustable and complementary gain controlled by V_{gc} with $I_{II} = I_I$ for $V_{gc} = 0$; $I_{II} > I_I$ for $V_{gc} > 0$ and $I_{II} < I_I$ for $V_{gc} < 0$. Since there are now two output branches, I and II, there are also two outputs being, the overall G_m, $G_{mI} = (1 - \beta)\alpha g_{m1}$ and $G_{mII} = \beta\alpha g_{m1}$ with the output located in branch I.



Mirrored ($k = 1$)	**Folded** ($\alpha < 1$)
$I_{in} = kI_{M1} = I_I + I_{II}$	$I_{in} = \alpha I_{M1} = I_I + I_{II}$
$I_I = (1 - \beta) I_{in} = (1 - \beta) k I_{M1}$	$I_I = (1 - \beta) I_{in} = (1 - \beta)\alpha I_{M1}$
$I_{II} = \beta I_{in} = \beta k I_{M1}$	$I_{II} = \beta I_{in} = \beta\alpha I_{M1}$
$G_{mI} = (1 - \beta) g_{m1}$	$G_{mI} = (1 - \beta)\alpha g_{m1}$
$G_{mII} = \beta g_{m1}$	$G_{mII} = \beta\alpha g_{m1}$

Figure 3. Current steering technique applied to (**a**) Mirrored OTA; and (**b**) Folded OTA.

2.3. Integrated Low Pass Filter

The single stage G_m–C integrators in combination with the current steering technique (CS) presented in the previous section, are shown in Figures 4 and 5. A unity-gain feedback structure is used to increase linearity in the passband [33,34]. Current steering is applied over M3 and both NMOS current mirrors (transistors, M4) are used to drive the current to the outputs. Since there are now two branches, there are also two outputs, I and II. Output II is kept at $V_{dd}/2$ to keep the symmetry of the system and ensure linear current division. The other one, output I, is the output of the integrator. This output is connected to V_{in}- achieving unity-gain feedback.

2.3.1. Mirrored-OTA Based Low Pass Filter

The auxiliary output branch, Output II, of the Mirrored-based Low Pass Filter uses a simple M4 current mirror, but for the Output I branch, a gain-boosting technique is used to enhance the current mirror copy and reduce the offset. A simple NMOS-input differential pair operating with a total current consumption of 0.25 µA and a DC gain of 43 dB is used with a Miller compensation network to ensure stability, as shown in Figure 4b.

This proposal has been designed in the low-cost 0.18 µm 1 P–6 M CMOS process from UMC. The maximum on-chip integrating capacitance for this technology is around 50 pF, which is the value set for the output capacitor. Transistor sizes in (µm/µm) are M1 = 7.5/10, M2 = 10/4, M3 = 5/4, M4 = 1/4, MB = 6/4, and for the auxiliary Error Amplifier M1 = 2/4, M2 = 6/4, M3 = 6/4, M3′ = 3/4. Miller compensation is achieved with a 3 kΩ resistance and a 1 pF capacitance. With a 1.0 V voltage supply, V_{dd}, and V_{cm} set to 0.5 V. The external reference current is set to 500 nA introduced through a 1:1 current mirror to the input differential pair and through a 2:1 current mirror to the EA, with a total power consumption of 1.75 µW.

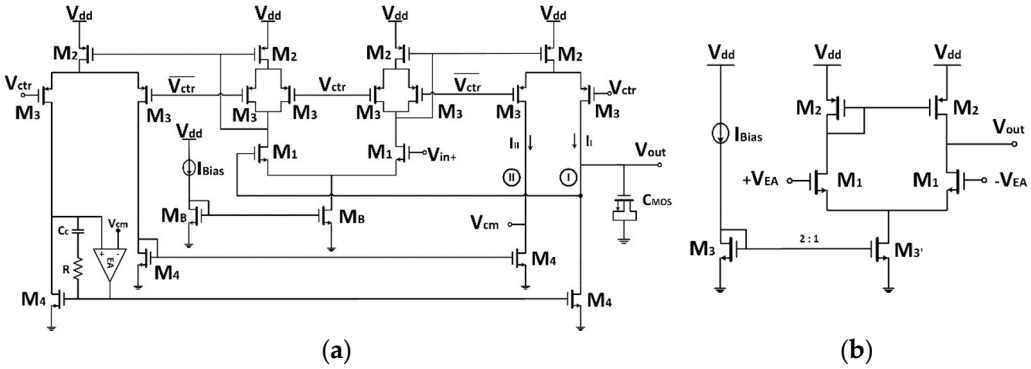


Figure 4. Schematic view of the proposed mirrored-OTA based: (**a**) LPF with Current-Steering and gain-boosting technique; and (**b**) differential pair EA used to reduce the offset.

2.3.2. Folded-OTA Based Low Pass Filter

The transistor sizes of the Folded-based Low Pass Filter in (µm/µm) are M1 = 8/10, M2 = 10/4, M3 = 5/4, M4 = 1/4, MB = 3/4, MB′ = 6/4, MN = 2/4, MP = 10/4. With a 1.0 V voltage supply, V_{dd}, and V_{cm} set to 0.5 V. The external reference current is set to 100 nA introduced through a 1:1 current mirror to the input differential pair, while the bias voltage is generated from another branch, having a total power consumption of 180 nW.

In order to enhance the behavior of the folded OTA, instead of using a classic current mirror, a cascode current mirror would enhance the copy of the current, but using classic cascode current mirrors requires a supply voltage higher than 1.0 V as the number of stacked transistors is too great. That is why a high swing cascode current mirror is chosen with a deviation from its classic topology, which is to connect both gates [35] saving the bias voltage characteristic of the high swing cascode current mirror.

Based on the same G_m–C structure of the low pass filter, two different NMOS current mirrors are used to drive the currents to the output stage in order to generate the complementary outputs II and I. The first integrated filter uses a classic current mirror structure as shown in Figure 5b, while the second proposal makes use of an enhanced version of the current mirror (Figure 5c) with a better copy factor of the currents thanks to the cascode current mirrors. The common voltage of the control gate voltages, V_{CP}, is set to 0.3 V for the first proposal while for the second one is set to 0.4 V. For the two of them, the external reference current is set to 100 nA, having a total power consumption of 180 nW with a 1.0 V voltage supply.

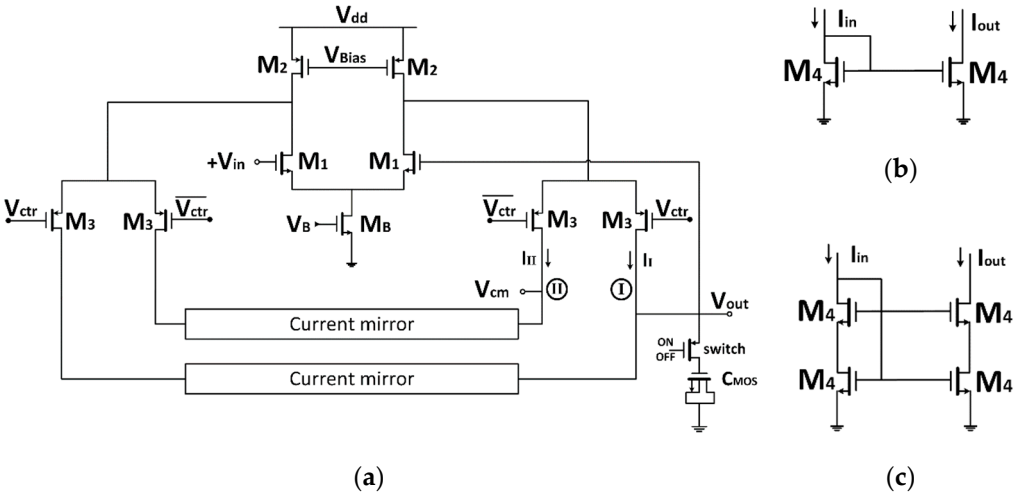


Figure 5. Schematic view of the: (**a**) proposed folded-OTA based LPF, (**b**) classic current mirror and (**c**) self-biased cascode current mirror.

The simulated analysis of the frequency response, shown in Figure 6, shows, with a 500 nA bias current, a constant unity gain with a tunable frequency that ranges from 2.4 kHz down to 70 mHz for Filter-1, from 2.2 kHz down to 100 mHz for Filter-2 and from 2.8 kHz down to 77 mHz for Filter-3.

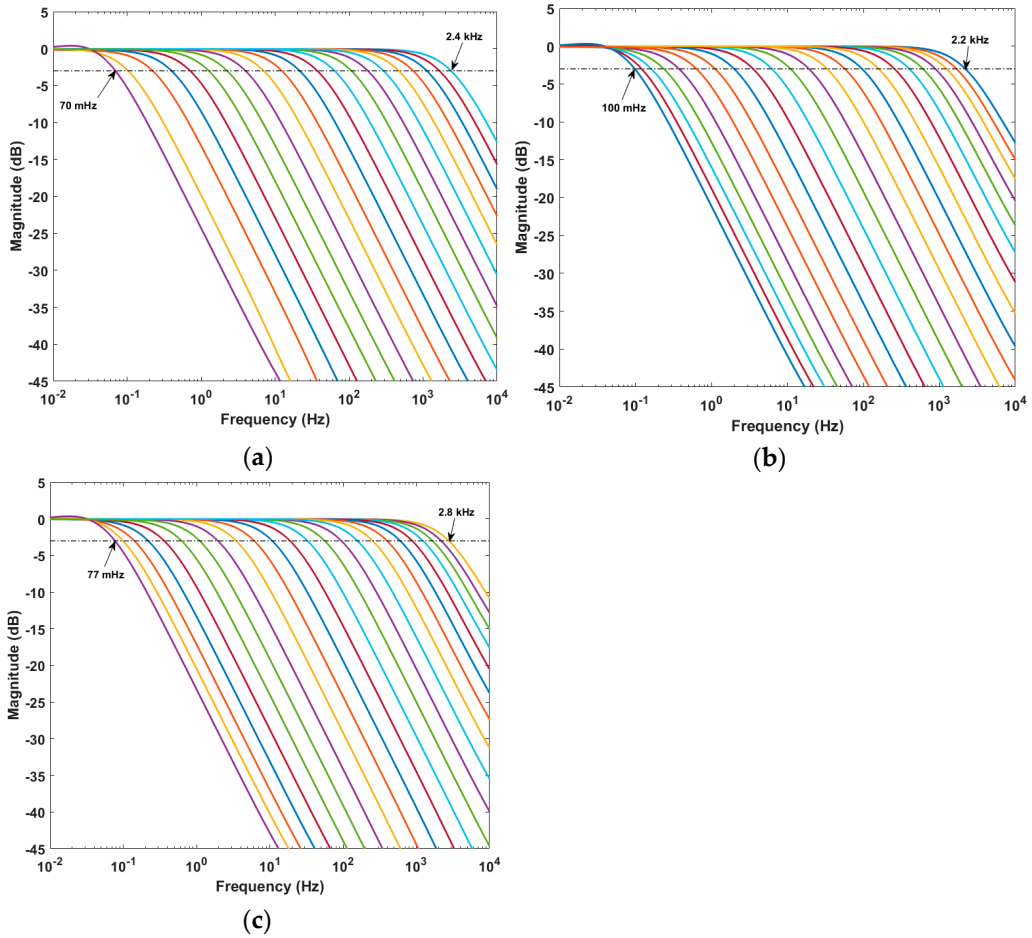


Figure 6. Frequency response vs V_{gc} for 500 nA bias current: (**a**) Filter-1; (**b**) Filter-2; and (**c**) Filter-3.

To validate the proposed architectures, these three topologies, the Mirrored-based LPF and two LPFs with the same core structure, one with a classic current mirror and another with an enhanced version of the current mirror, biased at a 1.0 V power supply, have been fabricated and experimentally characterized. A low cost UMC 0.18 µm 1 P–6 M CMOS process has been used, providing transistors with 1.8 V–3.3 V nominal supplies, MIM (Metal-Insulator-Metal) capacitors (CPOX = 1.0 fF/µm^2), and a high resistive polysilicon (HRP) layer (R_{square} = 1039 Ω/sq.) Figure 7 shows the microphotograph of the implemented filters with the total active area expended. As can be seen, most of the area is consumed by the NMOS capacitor, while no difference between the two implemented folded filters in terms of area consumption is appreciated.

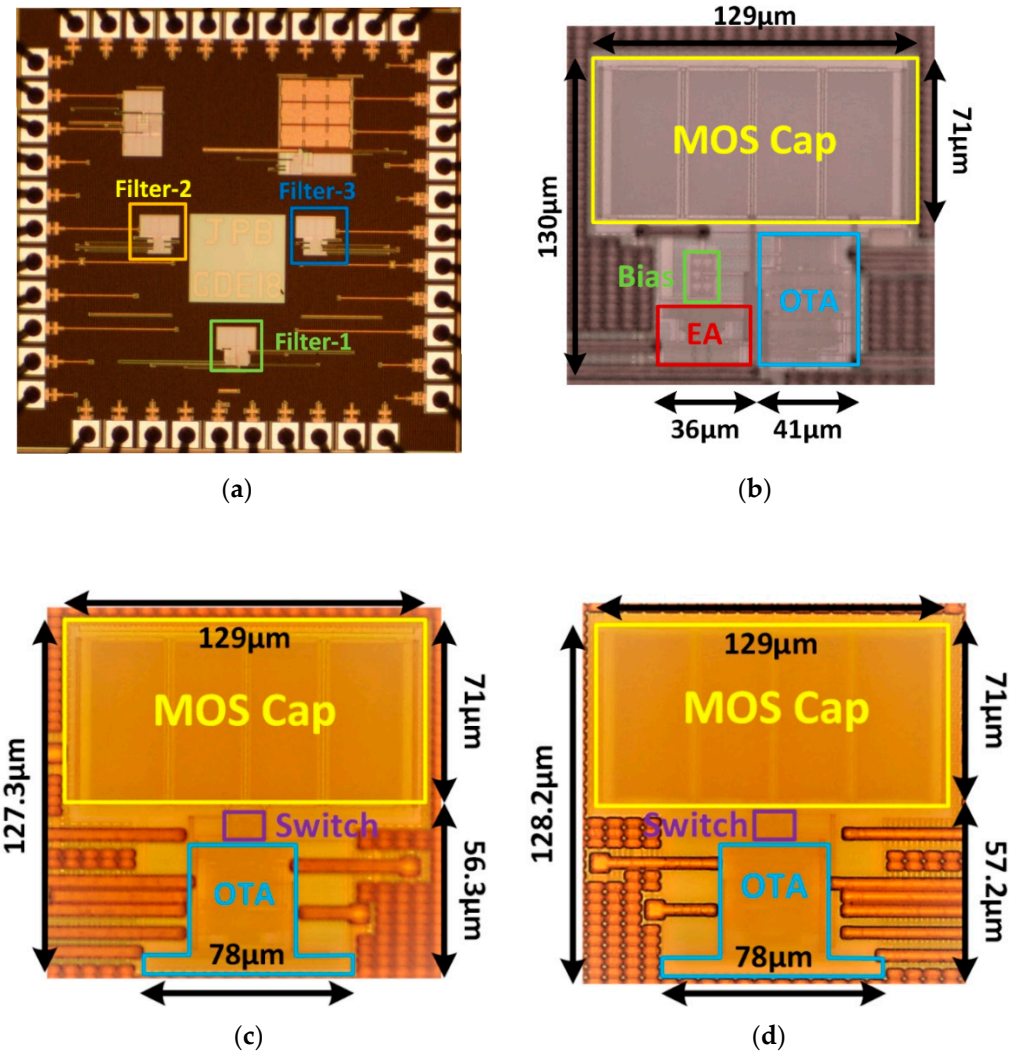


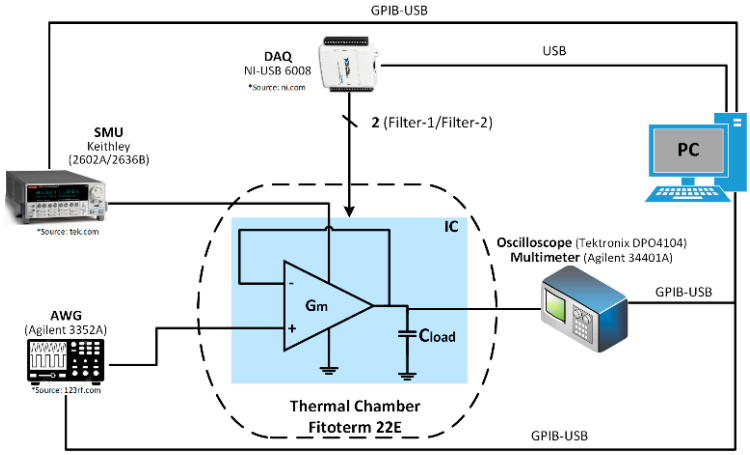
Figure 7. Microphotograph of: (**a**) complete integrated die (1525 µm × 1525 µm); and zoomed image of (**b**) Filter-1; (**c**) Filter-2; and (**d**) Filter-3.

3. Experimental Characterization

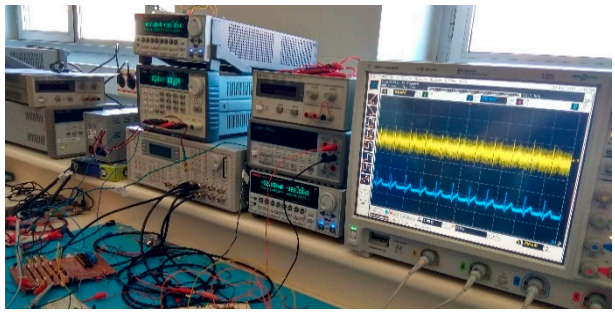
The characterization of the filters main static and dynamic parameters has been done with a Printed Circuit Board (PCB) and the measurement setup shown in Figure 8 (Figure 8a shows the block diagram and Figure 8b a caption of the experimental setup). The active area for Filter-1 (Mirrored) is approximately 77 × 59 µm^2; 78 × 55 µm^2 for Filter-2 (Folded with common CM) and 78 × 56 µm^2 for Filter-3 (Folded with enhanced CM), without the integrated capacitor that has been implemented as a MOS capacitor with an area consumption of 0.0092 mm^2. Thus, total area consumption of 0.0137 mm^2, 0.0135 mm^2, and

0.0136 mm^2 was for Filter-1, Filter-2, and Filter-3, respectively, with the main area expense being due to the capacitor.

The measurement setup has been automatized to characterize the main static and dynamic parameters. It uses a NI-USB 6008 Data Acquisition Card (DAQ) to select between one of the two integrated filters. Two dual channel Source Measurement Units (SMU) controlled through a GPIB-USB are used as sources to generate the biasing of the filter, and at the same time to read: the voltage supply, V_{dd}, and the current reference, I_{ref}, with one of the SMU –Keithley 2636 B–, and with the other one–Keithley 2602 A– to provide (and read) the complementary control voltages and the DC input voltage. While in the dynamic characterization, the input voltage is provided by an Agilent 3352 A arbitrary waveform generator (AWG).



(**a**)



(**b**)

Figure 8. Automatic measurement setup for the two proposed LPFs: (**a**) block diagram and (**b**) experimental setup.

As for the readout, the DC output voltage is acquired with a 34401A Agilent $6\frac{1}{2}$ digital multimeter (DMM), while for the dynamic behavior a DPO4104 Tektronix oscilloscope is used to read the transient input and output signals. Figure 8a shows the instrumentation used for the static and the dynamic characterization.

3.1. Cutoff Frequency Tunable Range

Figure 9 presents how the V_{gc} tuning modifies the G_m value of both outputs when $V_{gc} > 0$. The G_m difference at $V_{gc} = 0$ between the experimental and the simulated behavior appears because the experimental G_m is an indirect value obtained from the measurement of the output currents. The corresponding cutoff frequency at $V_{gc} = 0$ corresponds to the maximum fc achieved, and this maximum cutoff frequency can be extended by using negative values of V_{gc}, $V_{gc} < 0$ or using a smaller value of C_{Load}.

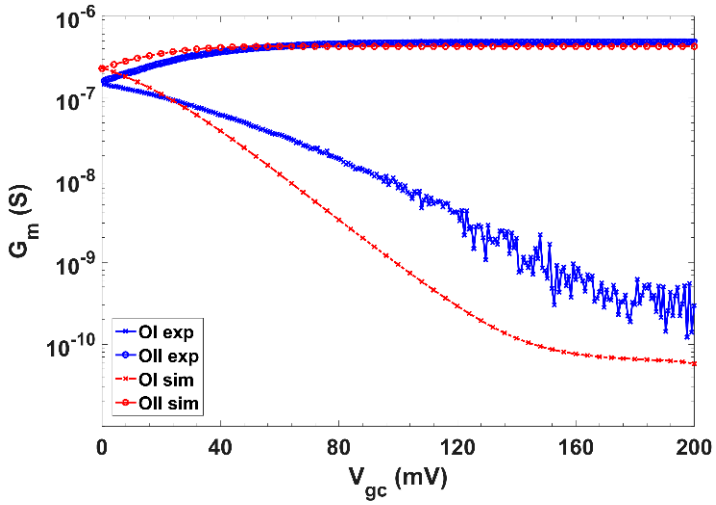


Figure 9. Experimental (blue) and simulated (red) G_m variation over V_{gc} for Filter-3.

Figure 10 presents the cutoff frequencies for the tuning voltage V_{gc} range with a 20 mV step. This V_{gc} range ensures that the maximum offset of the output low pass filters is no greater than 1%. The cutoff frequency, with a 500 nA bias current, can be tuned from 1.179 kHz (V_{gc} = 0 V) down to 82.5 mHz (V_{gc} = 200 mV) for Filter-1 (Figure 10a); from 1.475 kHz (V_{gc} = 0 V) down to 94 mHz (V_{gc} = 200 mV) for Filter-2 (Figure 10b) and for Filter-3 (Figure 10c) from 1.757 kHz (V_{gc} = 0 V) down to 104 mHz (V_{gc} = 200 mV).

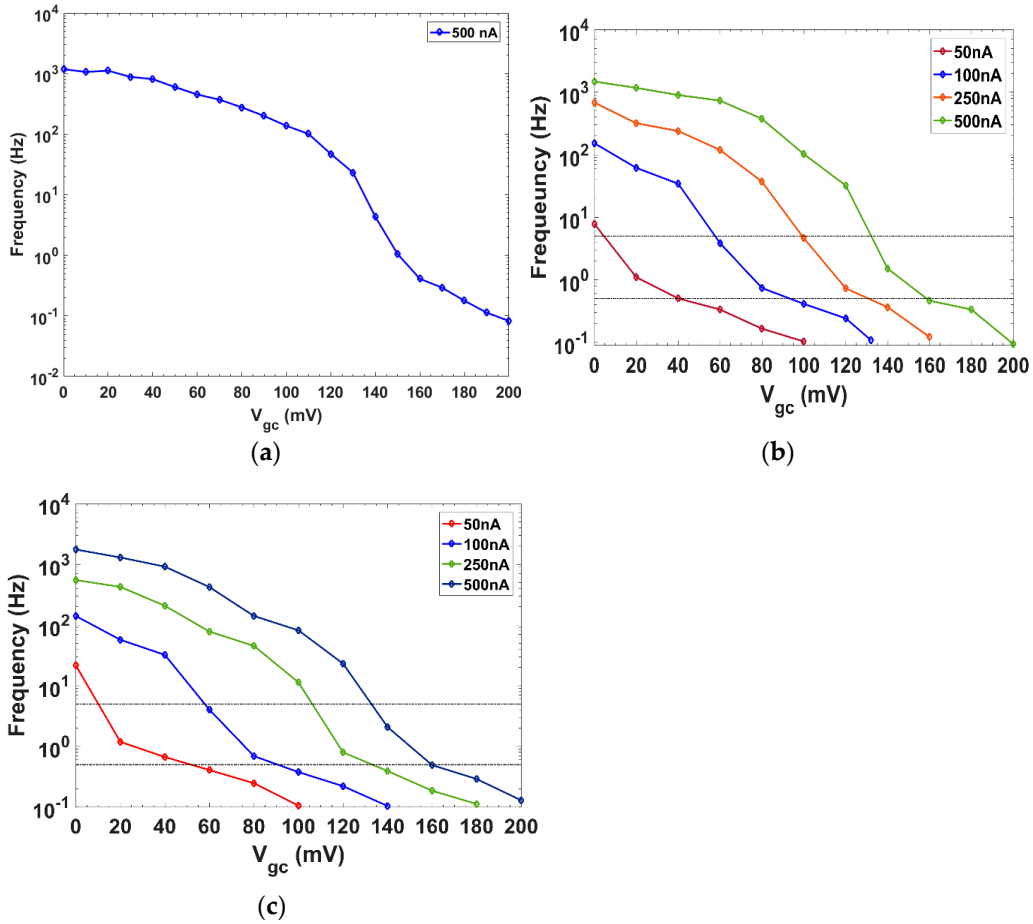


Figure 10. Cutoff frequency vs V_{gc} for different bias currents: (**a**) Filter-1; (**b**) Filter-2; and (**c**) Filter-3.

It is possible to reduce the bias current of Filter-2 and Filter-3 to further reduce the power consumption. This reduction keeps the minimum f_c almost constant while the maximum f_c is reduced so if only low cutoff frequencies are needed, it is possible to save power. The maximum f_c is reduced down to 680 Hz, 152 Hz and 8 Hz for Filter-2 (Figure 10b) and to 551 Hz, 140.6 Hz and 21.7 Hz for Filter-3 (Figure 10c) for bias currents of 250 nA, 100 nA, and 50 nA, respectively.

All the cutoff frequency tuning has been done for $V_{gc} \geq 0$, but it is also possible to extend the f_c range for values $V_{gc} < 0$ increasing the current going through the output branch and increasing the G_m, or using a smaller value of C_{Load}. In this case, as the target frequency range was from 100 mHz to 100 Hz—to cover the frequency ranges of impedance spectroscopy and several biomarkers—an extension of the f_c range, was not required. The corresponding power consumption, for both filters, is 960 nW, 480 nW, 180 nW, and 70 nW for bias currents of 500 nA, 250 nA, 100 nA, and 50 nA, respectively.

Post-layout simulation analysis for PT-variation were performed verifying that the sub-Hz to kHz frequencies were achieved thanks to the CS tuning technique, while V_{dd} is assumed to be provided by a voltage regulator and thus kept constant. Experimentally, Figure 11a,b show the variation of the control voltage, V_{gc}, over temperature needed to keep the filters cutoff frequencies constant at two frequencies: 5 Hz and 0.5 Hz respectively. As can be seen, the V_{gc} values needed are still within the operating range—even though Filter-1 shows higher V_{gc} values—to keep the output offset below ±1% and the DC gain error below 0.5 dB, for a temperature range from −40 °C to 100 °C.

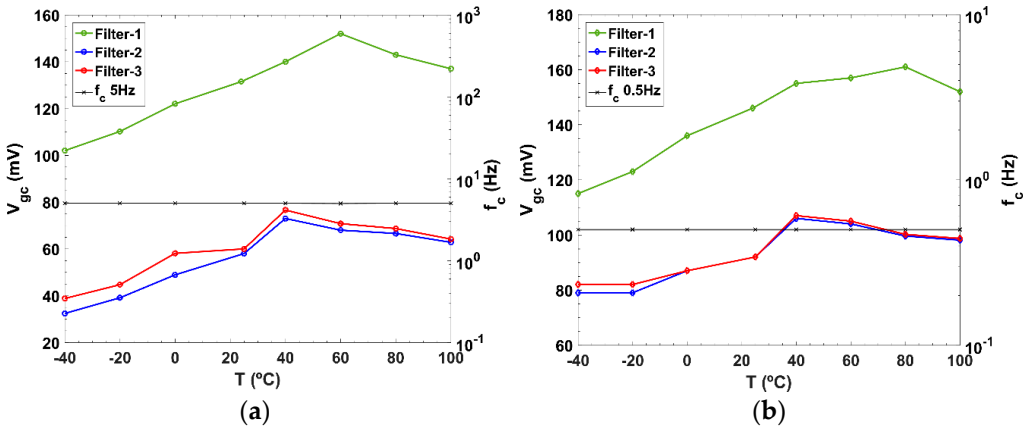


Figure 11. V_{gc} adjusted over T-variations, for the three filters, to keep f_c at: (**a**) 5 Hz and (**b**) 0.5 Hz.

3.2. Input Common Mode Range (ICMR)

The input vs output DC voltage characteristic for the filters at the target frequencies previously set 0.5 Hz and 5 Hz is shown in Figure 12. As we increase the bias current, the input-output characteristic is improved.

Filter-1 (Figure 12a) shows a linear input range of 400 mV–970 mV (f_c = 0.5 Hz) and 350 mV–970 mV (f_c = 5 Hz). For Filter-2 (Figure 12b), the linear input range is 201 mV–743 mV (f_c = 0.5 Hz) and 149 mV–762 mV (f_c = 5 Hz) for a bias current of 100 nA. If the bias current is increased to 500 nA, the linear input range is 310 mV–940 mV (f_c = 0.5 Hz) and 350 mV–950 mV (f_c = 5 Hz). Finally, for Filter-3 (Figure 12c), the linear input range is 153 mV–851 mV (f_c = 0.5 Hz) and 141 mV–870 mV (f_c = 5 Hz) for a bias current of 100 nA. While if the bias current is increased to 500 nA, the linear input range is 190 mV–940 mV (f_c = 0.5 Hz) and 210 mV–950 mV (f_c = 5 Hz) for f_c = 5 Hz.

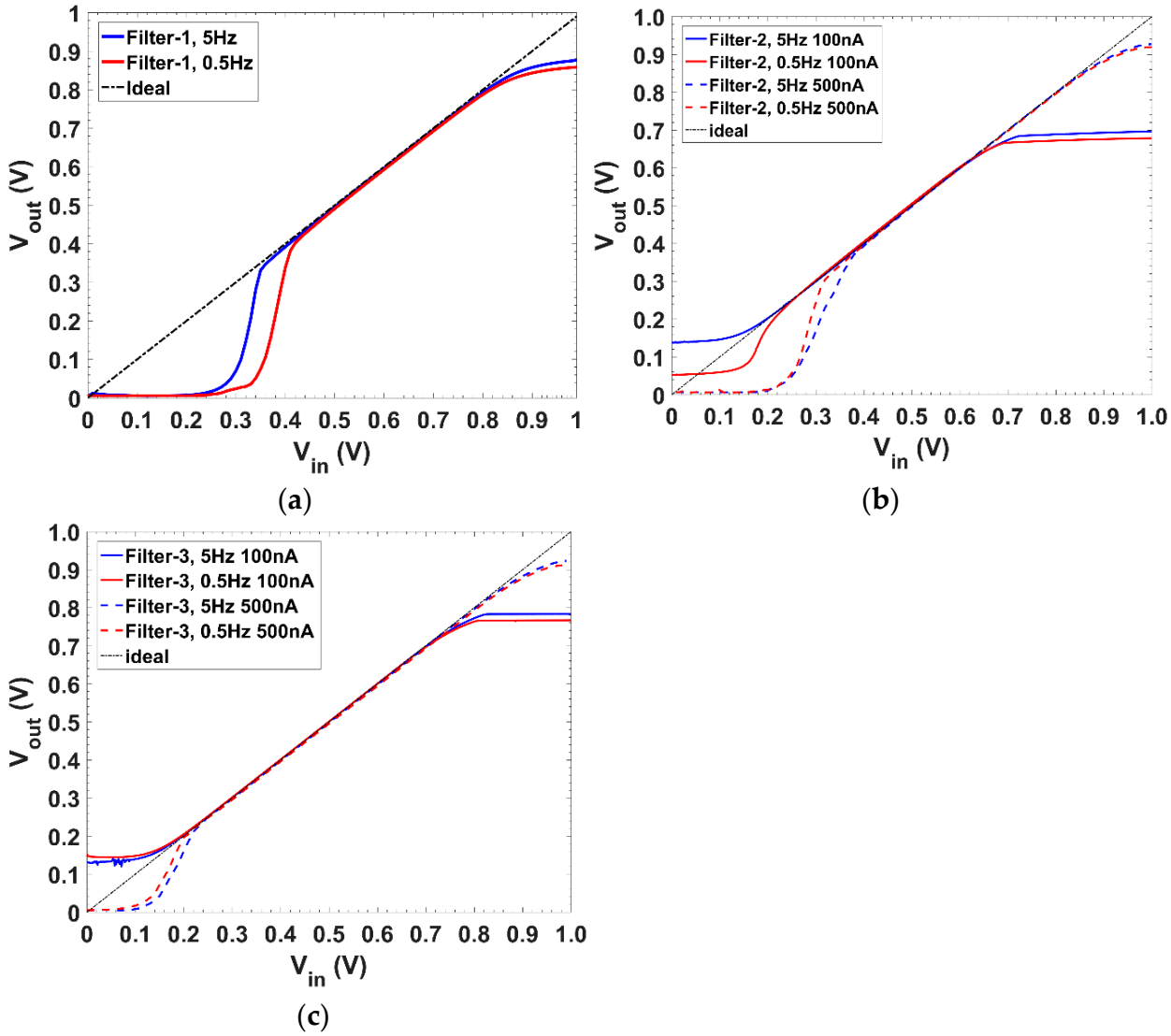


Figure 12. ICMR at fc 5&0.5 Hz for: (**a**) Filter-1; (**b**) Filter-2; and (**c**) Filter-3.

3.3. Linearity (@THD ≤ 1%)

Figure 13 shows the total harmonic distortion (THD) (%) values vs the input voltage (mV_{pp}) for a signal frequency set at $f_c/5$: Figure 13a shows the THD for Filter-1 at 500 nA; Figure 13b,c show the THD for Filter-2 and Filter-3, respectively, and bias currents of 100 nA (straight lines) and 500 nA (dotted lines). Filter-1 has a THD below 1% for input signals up to 280 mV_{pp} and 167 mV_{pp} for f_c 5 Hz and 0.5 Hz, respectively. Filter-2 has a THD below 1% for input signals up to 236 mV_{pp} and 300 mV_{pp} for f_c 5 Hz and 0.5 Hz, respectively, and a bias current of 100 nA, while for a bias current of 500 nA it goes down to 222 mV_{pp} (f_c 5 Hz) and 251 mV_{pp} (f_c 0.5 Hz). Filter-3 has a THD below 1% for input signals up to 205 mV_{pp} and 248 mV_{pp} for f_c 5 Hz and 0.5 Hz, respectively, and a bias current of 100 nA, while for a bias current of 500 nA it goes down to 190 mV_{pp} (f_c 5 Hz) and 222 mV_{pp} (f_c 0.5 Hz).

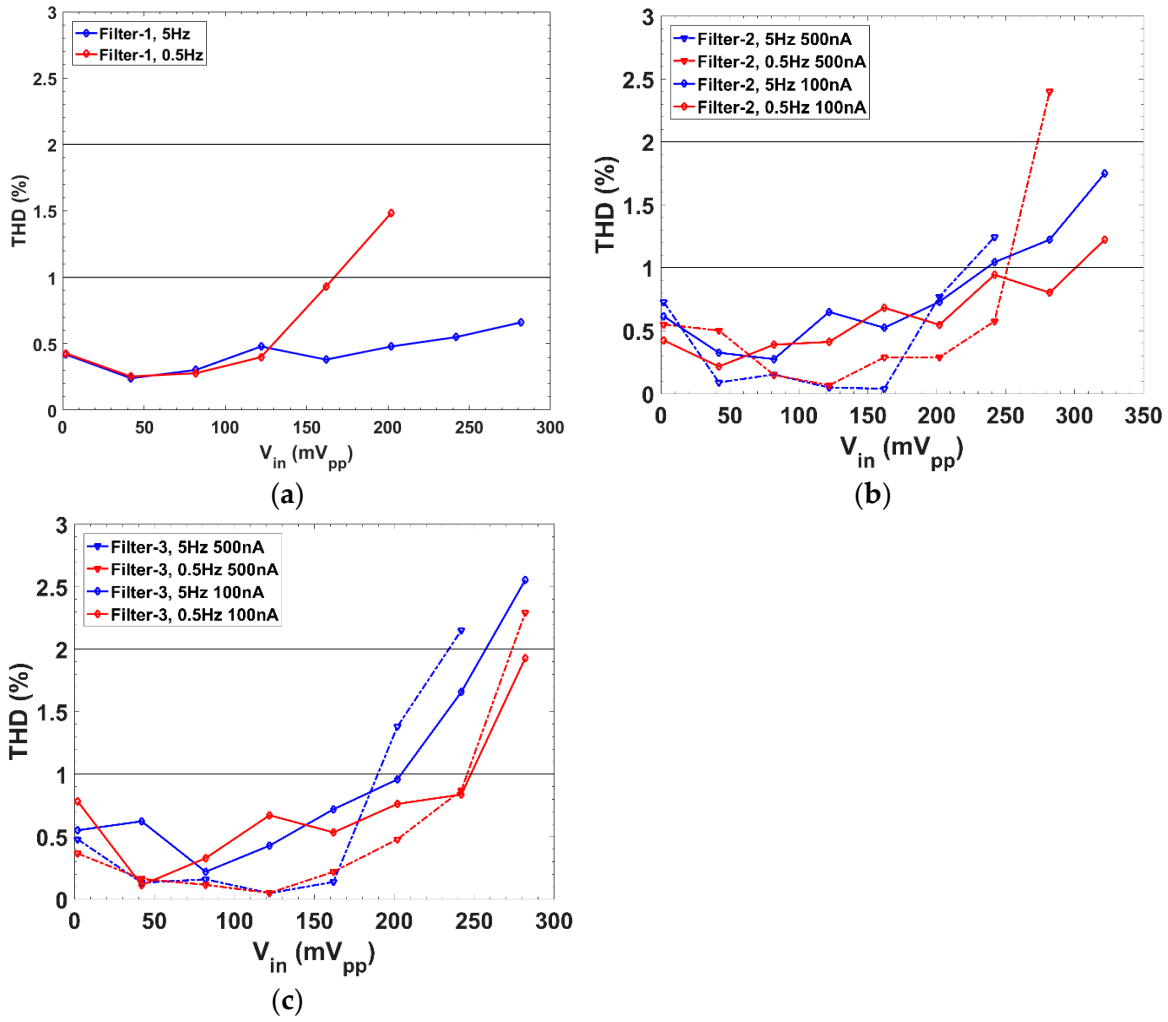


Figure 13. Harmonic distortion vs. different amplitudes for: (**a**) Filter-1; (**b**) Filter-2; and (**c**) Filter-3.

3.4. Dynamic Range (DR)

To evaluate the dynamic range given by

$$DR = 20\log_{10}\left(\frac{THD(V_{pp}/2)/\sqrt{2}}{noise_{rms}}\right) \quad (1)$$

The integrated in-band noise is the simulated value from the extracted view of the designed filters: 8.48 μV_{rms} (f_c = 5 Hz) and 7.75 μV_{rms} (f_c = 0.5 Hz) for Filter-1; 7.33 μV_{rms} (f_c = 5 Hz) and 6.4 μV_{rms} (f_c = 0.5 Hz) for Filter-2 and 15.5 μV_{rms} (f_c = 5 Hz) and 12.2 μV_{rms} (f_c = 0.5 Hz) for Filter-3.

3.5. Figure of Merit (FoM)

To compare different proposed structures with similar characteristics, different FoMs can be found in the literature [1,2,22,27]. The main parameters that are employed to define LPFs are power, dynamic range (DR), order of the filter (n), bandwidth (BW), and area consumption. We are going to use the two introduced in [1,27], as they not only take into account all the previous parameters but also normalize the power (NP) and the area

(NA) consumption to the technology used, so it is believed it holds stronger comparative constraints. These FoMs are given by:

$$FoM_1 = \frac{NP}{n * DR} \quad (2)$$

$$FoM_2 = \frac{Power * BW * NA}{n * DR} \quad (3)$$

where NP = Power*[0.5/($V_{dd} - V_{th}$)]*(1/V_{dd}) and NA = area(mm^2)/Tech(μm^2)^2, with V_{th} = 0.4 V for 0.18 µm CMOS technology.

A comparison between the two proposed structures for active filters with previously reported works of similar voltage supply is presented in Table 2. The reported filters present a tuning frequency range that spans over four orders of magnitude with very low power and area consumption while an important enhancement of the dynamic range is achieved. Besides, they are capable of maintaining the target cutoff frequencies over a temperature range from −40 °C to 100 °C. Therefore, compared with previously reported works, the proposals presented in this paper present a wider frequency range with a better performance trade-off in terms of area/pole consumption.

Table 2. LPF performance comparison with similar G_m–C works.

Parameter	Filt-1	Filt-2	Filt-3	Filt-2	Filt-3	[36] '15	[21] '16[(c)]	[23] '18	[24] '18	[1] '19
Results	Exp.	Exp.	Exp.	Exp.	Exp.	Lay.	Lay.	Sim.	Exp.	Sim.
Tech. (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.35	0.18
Fully-integrated	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
V_{supply} (V)	1.0	1.0	1.0	1.0	1.0	0.5	1.8	1.8	1.8	1
Order	1	1	1	1	1	2	2	2	2	5
Gain offset (dB)	<0.5	<0.5	<0.5	<0.5	<0.5	−0.5	NA	−3.2; −7.2	NA	−7
Area (mm^2)	0.0137	0.0135	0.0136	0.0135	0.0136	NA	0.062	NA	0.12	0.24
T range (°C)	−40–100	−40–100	−40–100	−40–100	−40–100	NA	NA	NA	NA	0–80
I_{Bias} (nA)	500	100	100	500	500	37.5	NA	1	14.9–182.3	NA
Power (nW)	1750	180	180	960	960	250	2.33*10^5	9.5	107.2–1310	41
Tunable	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	No
f_c (Hz)	82.5 m–1.179 k	109 m–152	104 m–141	94 m–1.475 k	129 m–1.757 k	100	34–20 k	4–100	2 k–20 k	250
ICMR (V)	0.4–0.97; 0.35–0.97[(a)]	0.2–0.74; 0.15–0.76[(a)]	0.15–0.85; 0.14–0.87[(a)]	0.31–0.94; 0.35–0.95[(a)]	0.19–0.94; 0.21–0.95[(a)]	NA	NA	NA	NA	NA
noise (μV_{rms})	12.2; 15.5[(a)]	9.48; 10.28[(a)]	8.11; 8.81[(a)]	7.75; 8.48[(a)]	6.40; 7.33[(a)]	NA	91.2	10.24[(d)]	86.3–84.3	134
Linearity (V_{pp})	0.167; 0.28[(a)]	0.3; 0.236[(a)]	0.248; 0.205[(a)]	0.251; 0.222[(a)]	0.246; 0.19[(a)]	0.15	NA	1.03[(d)]	NA	NA
DR (dB)	73.7; 76.1[(a)]	81.0; 78.2[(a)]	80.7; 78.3[(a)]	81.2; 79.3[(a)]	82.7; 79.2[(a)]	74.62[(b)]	NA	91[(d)]	52.7; 54.6[(e)]	61.2
NP (FoM_1) (10^{-9})	1458	150	150	800	800	2500	46230	1.88	22.2; 271.6	34.2
NA (FoM_2)	0.423	0.417	0.420	0.417	0.420	NA	1.914	NA	0.98	7.4
FoM_1 (10^{-12})	301; 228[(a)]	13.4; 18.5[(a)]	13.4; 18.5[(a)]	70; 87[(a)]	59; 88[(a)]	232	NA	0.0265	26; 253	5.96
FoM_2 (10^{-12})	76.4; 580[(a)]	3.34; 46.2[(a)]	3.48; 46[(a)]	17.4; 217[(a)]	14.8; 221[(a)]	NA	NA	NA	245; 23905	13.21

* NA = Not Available; [(a)] for f_c = 0.5&5 Hz; [(b)] f_{in} =30 Hz, f_c = 100 Hz; [(c)] DC_{offset} = 0.6 V; [(d)] at f_c = 100 Hz; [(e)] SFDR.

The two FoMs presented allow comparison of the main performances (cut-off frequencies, DR, power, area) of the different proposals in terms of normalized power consumption (FoM_1) and in terms of normalized area consumption (FoM_2). Considering that the smaller the values of both FoMs the better trade-off the corresponding topology exhibits, note that

as can be seen in Table 2, Filter-1 has the worst performance of our proposed structures as its core OTA was not optimized in terms of power efficiency for this voltage supply. Nonetheless, it shows similar results to [24,36]. As for Filter-2 and Filter-3, their performances achieve competitive values being enhanced for lower bias currents. Reference [1] has better FoM_1 due to its lower power consumption, but a higher FoM_2 and it shows no frequency tuning.

Thus, the proposal presented here is a competitive solution while satisfying the low-voltage low-power on-chip constraints, becoming a preferable choice for general-purpose reconfigurable front-end sensor interfaces.

4. Conclusions

Two active low pass filters based on a G_m–C approach for very low voltage applications have been presented in this paper. Programmability of the cutoff frequencies is achieved through a current steering technique. The integrated LPFs have a 1.0 V voltage supply and a tunable cutoff frequency that spans several orders of magnitude achieving sub-Hz frequencies, with a low power consumption and a high dynamic range. It has been validated for different bias currents showing its adaptability for different frequency ranges.

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