ANEXO

ANEXO 1: Código fuente

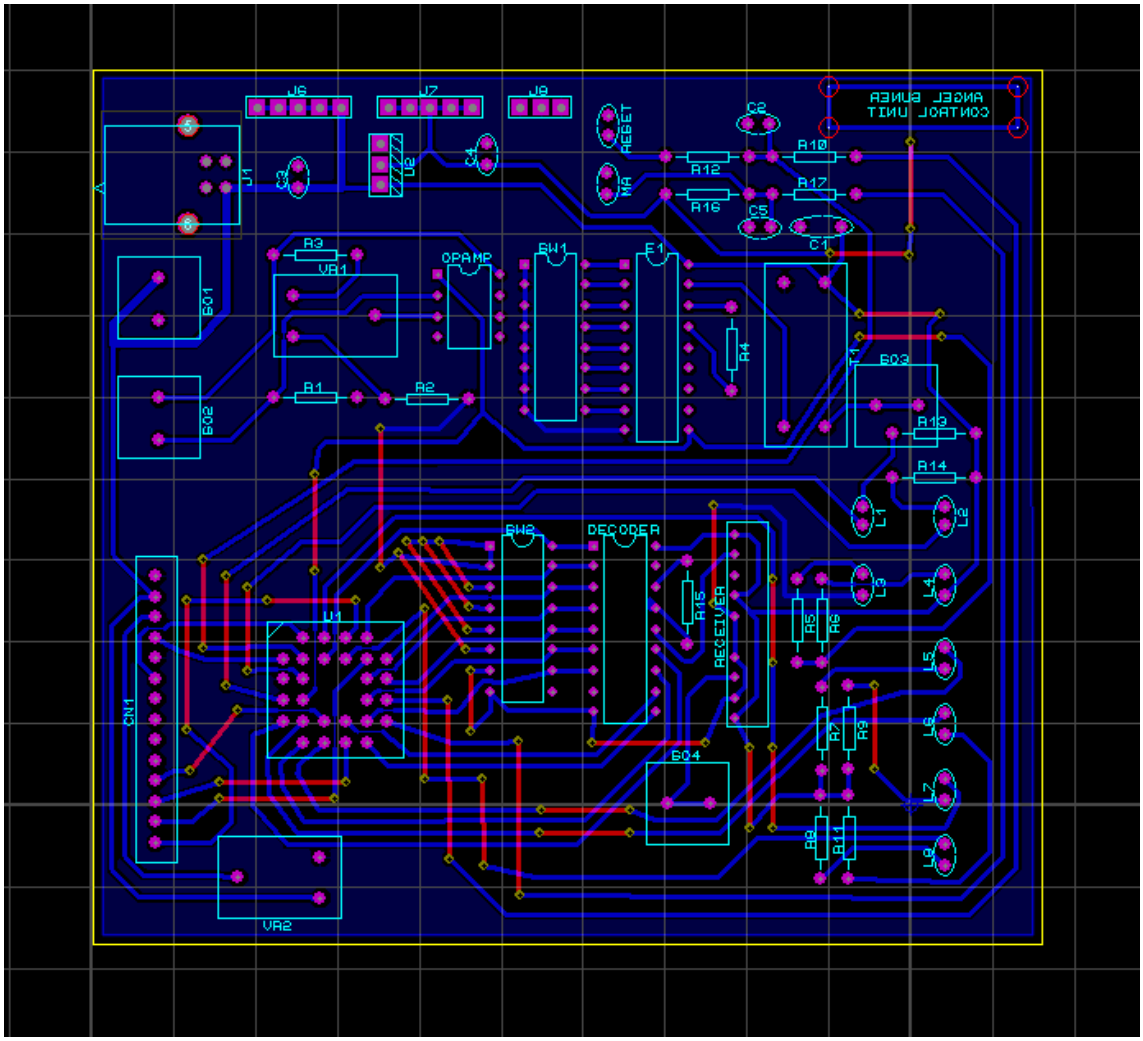
C:\Users\Angel\Desktop\UCLAN UNIVERSITY\PROJECT\KEIL UVISION 4\street lamps.c

```
#include <REG938.H>
unsigned char mode;
unsigned char daynight;
unsigned char lamps;
void delay();
void check(unsigned char lamp, unsigned char i, unsigned char j);

void main()
{
    int counter;

     unsigned char lampcounter=0x01;
     unsigned char icounter=0x07;
     unsigned char jcounter=0x08;


     P0M1 = 0x80;
     P0M2 = 0x00;
     P1M1 = 0xFF;
     P1M2 = 0x00;
     P2M1 = 0x00;
     P2M2 = 0x00;
     P3M1 = 0x00;  P2 = 0x0F;
     P3M2 = 0x00;  P3 = 0x02;

     while(1)
     {
         lamps = P1&0x0F;
         mode = P0&0x80;
         daynight = P1&0x10;


     if ( mode == 0x00)                  // MODO AUTOMÁTICO
                                         // Microprocesador selecciona
     {                                   // automáticamente las direcciones
                                         // de las lámparas
       lampcounter=0x01;
       icounter=0x07;
       jcounter=0x08;

         for(counter=0;counter<4;counter++)
         {

          lamps=P1&0x0F;

         check(lampcounter,icounter,jcounter);
         lampcounter <<=1;
         icounter >>=1;
         icounter += 0x08;
         jcounter>>=1;
         delay();

     }                                   // MODO MANUAL: La dirección de la
     }                                   // lámpara se selecciona manualmente
     else                                // en la Unidad de Control
```

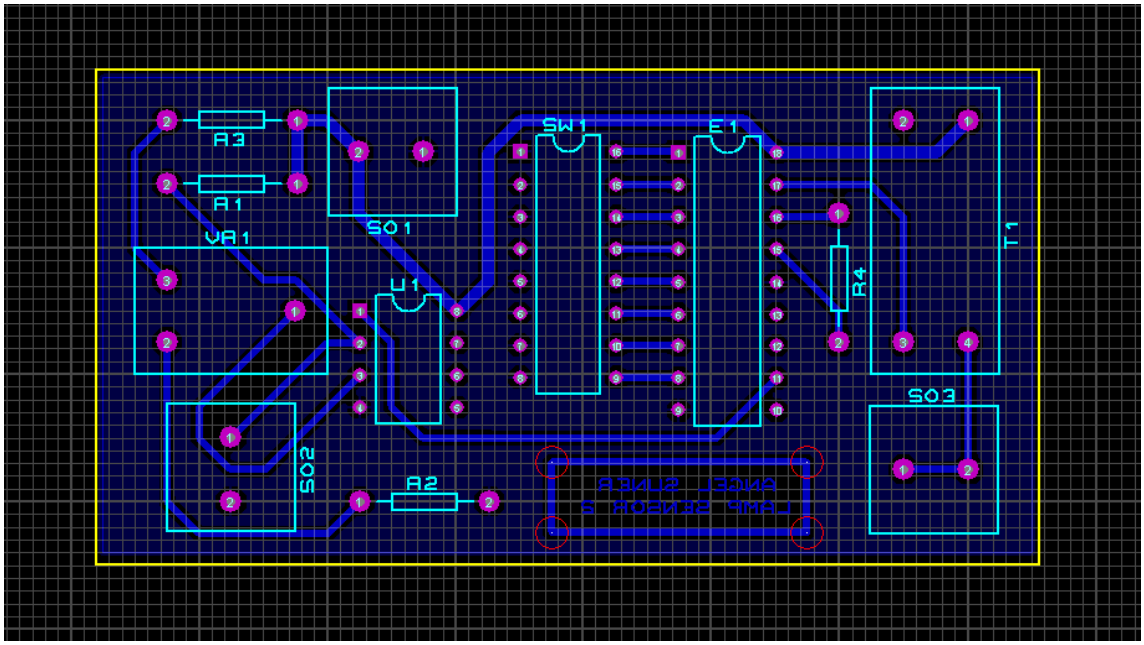
```
    {   if(daynight==0x00)                  // Si salida interruptor crepuscular = "0",
        {                                   // indica que es de DÍA.
        P2= P1&0x0F;                        // Visualiza entradas puerto 1 en puerto 2
        if ((lamps&0x0F)!=0x00)             // Si salidas decodificador no son "0" (lamps on)
        P3=0x00;                            // entonces indicador de fallo ON.
        else P3=0x02;                       // Si salidas decodificador son "0" (lamps off)
                                            // entonces indicador de fallo OFF.
        }
        Else                                // Si salida interruptor crepuscular no es 0,
        {                                   // indica que es de NOCHE.
        P2=P1^0x0F;                         // Visualiza entradas puerto 1 en puerto 2.
        if ((lamps&0x0F)!=0x0F)             // Si salidas decodificador no son "1" (lamps off)
        P3=0x00;                            // entonces indicador de fallo ON.
        else P3 = 0x02;                     // Si salidas decodificador son "1" (lamps on)
        }                                   // entonces indicador de fallo OFF.
    }
}}

void delay()
{
    unsigned long int j;
    for(j=0;j<400000;j++)
     {
      ;
      }
}

void check(unsigned char lamp, unsigned char i, unsigned char j)
{

    P0 = lamp;                              // Selecciona dirección de lámpara

    if (daynight == 0x00)                   // Si salida interruptor crepuscular es "0"→DÍA
    {if ((lamps&lamp) == 0x00)              // Si salida decodificador es "0" (lampara off)
        {P2 = P2 & i;                       // entonces LED de la lámpara ON y el
            P3 = 0x02;                      // indicador de fallo OFF.
        }
        else{
        P2 = P2 | j;                        // Si salida decodificador no es "0" (lampara on)
            P3 = 0x00;                      // entonces LED de la lámpara off (fallo)
        }                                   // e indicador de fallo ON.
        }
      if(daynight == 0x10)
    {if ((lamps&lamp) == 0x00)              // Si salida int. crepuscular es "1"→NOCHE
        {P2 = P2 | j;                       // Si salida decodificador es "0" (lámpara off)
            P3 = 0x00;                      // entonces LED de la lámpara OFF y el
        }                                   // indicador de fallo ON.
        else{
        P2 = P2 & i;                        // Si salida decodificador no es "0" (lámpara on)
            P3= 0x02;}                      // entonces LED de la lámpara ON y el
                                            // indicador de fallo OFF.
    }
}
```

ANEXO 2: Layouts de las PCBs

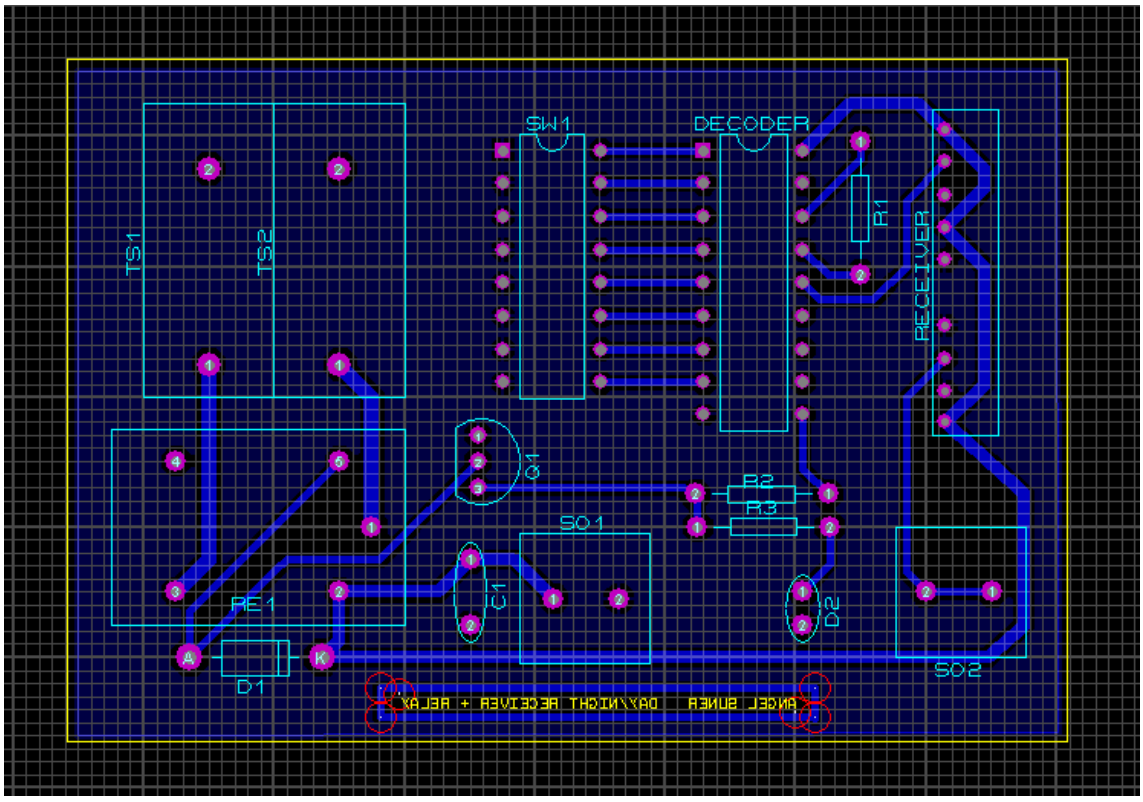
Unidad de Control



Sensor detector de luz



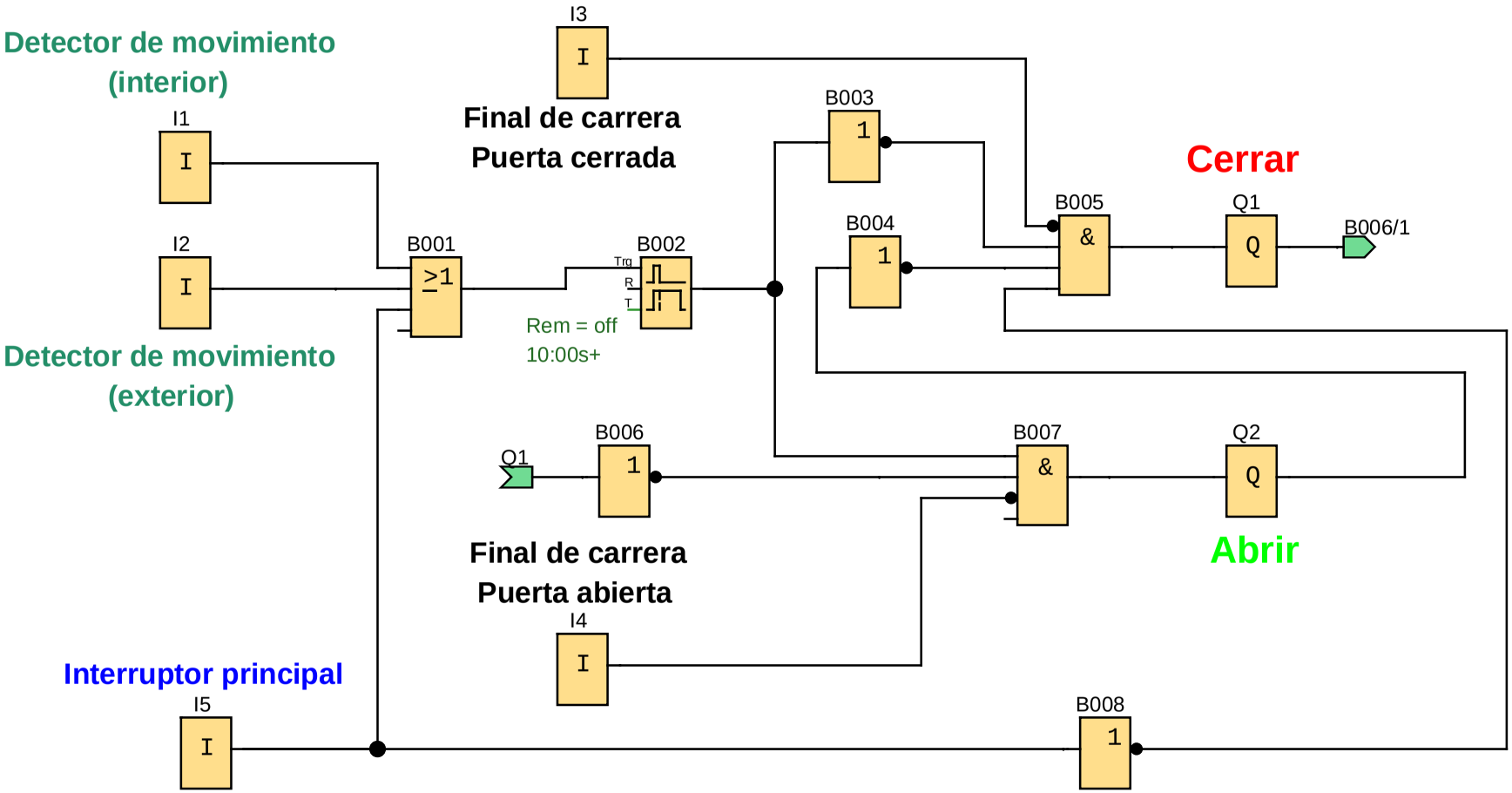
Interruptor crepuscular



ANEXO 3: Esquemas Generales Programas LOGO!

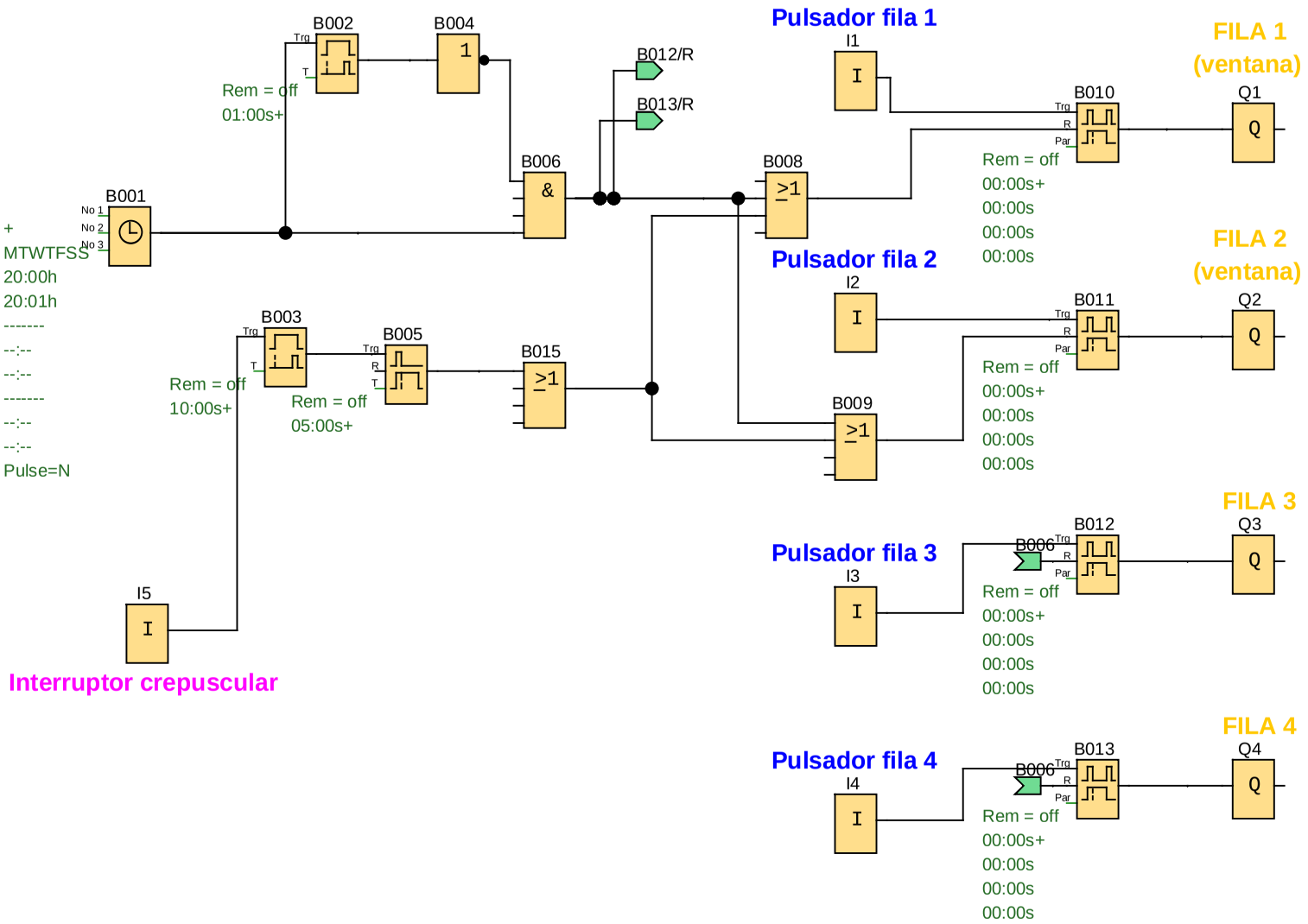
Como se mencionó en el capítulo 6, *Ejemplos de automatización aplicados a un edificio empresarial*, los programas del autómata LOGO! se realizan a través de su software gratuito LOGO!Soft Comfort. Por medio de este software se puede extraer un informe en PDF con el esquema eléctrico general del programa, nombres de los conectores, parámetros, etc. Se adjuntan por tanto los documentos extraídos para los programas realizados:

PUERTA AUTOMÁTICA



Autor:	Angel Súñer de Pedro		Proyecto:	Aplicaciones LOGO!	Cliente:	
Comprobado:			Instalación:	Puerta de acceso	Nº diagrama:	
Fecha de creación/modificación:	5/08/12 16:47/8/09/12 11:12		archivo:	Acceso_puerta.lsc	Página:	1 / 2

Número de bloque (tipo)	Parámetro
B002(Retardo a la desconexión) :	Rem = off 10:00s+
I1(Entrada) : Detector de movimiento (interior)	
I2(Entrada) : Detector de movimiento (exterior)	
I3(Entrada) : Final de carrera Puerta cerrada	
I4(Entrada) : Final de carrera Puerta abierta	
I5(Entrada) : Interruptor principal	
Q1(Salida) : Cerrar	
Q2(Salida) : Abrir	

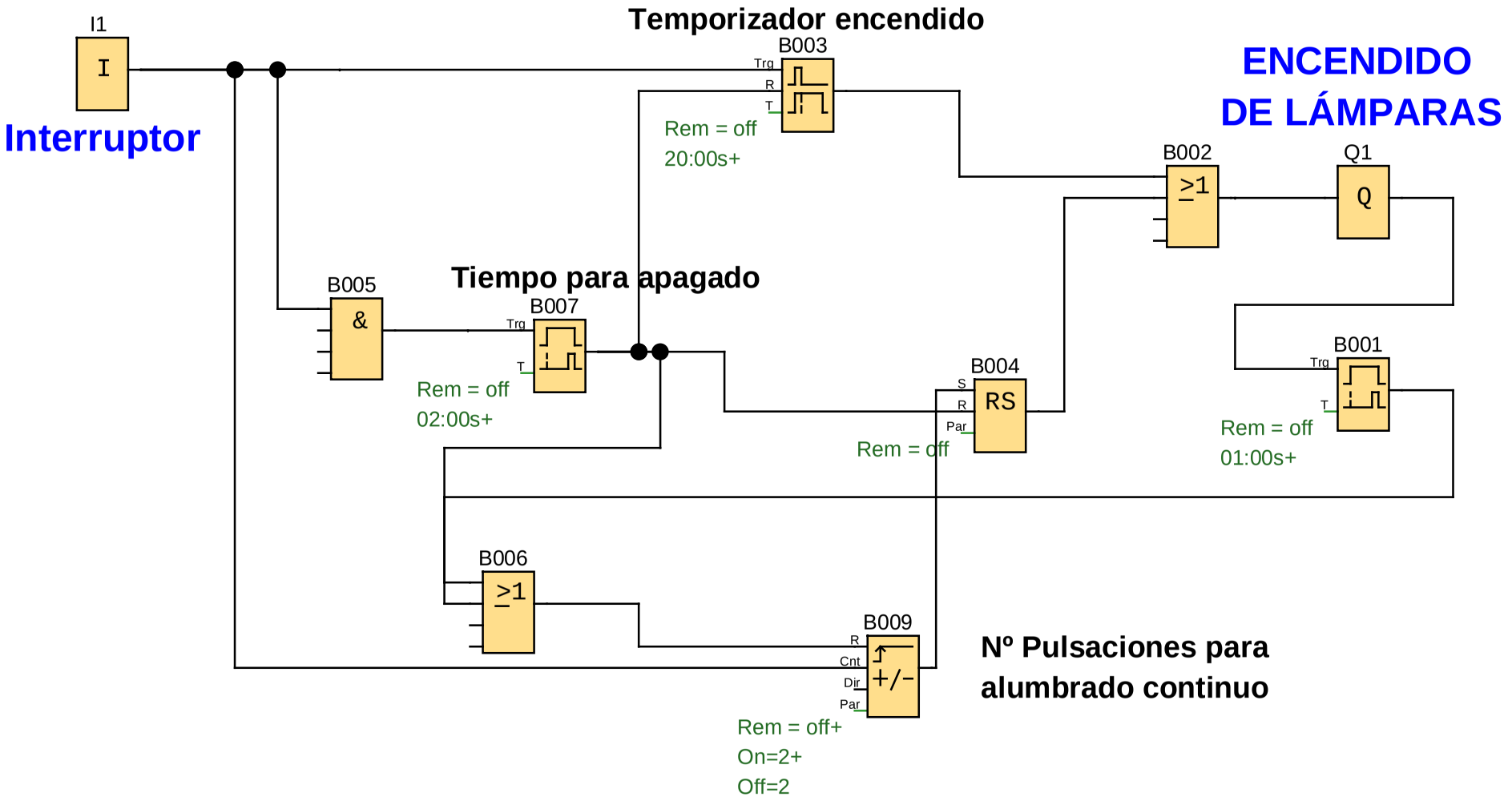


Autor:	Angel Súñer de Pedro		Proyecto:	Aplicaciones LOGO!	Cliente:	
Comprobado:			Instalación:	Iluminación oficina	Nº diagrama:	
Fecha de creación/modificación:	18/08/12 20:02/8/09/12 11:09		archivo:	Luminarias oficina.lsc	Página:	1 / 3

Número de bloque (tipo)	Parámetro
B001(Temporizador semanal) :	+ MTWTFSS 20:00h 20:01h ------- --:-- --:-- ------- --:-- --:-- Pulse=N
B002(Retardo a la conexión) :	Rem = off 01:00s+
B003(Retardo a la conexión) :	Rem = off 10:00s+
B005(Retardo a la desconexión) :	Rem = off 05:00s+
B010(Interruptor bifuncional) :	Rem = off 00:00s+ 00:00s 00:00s 00:00s
B011(Interruptor bifuncional) :	Rem = off 00:00s+ 00:00s 00:00s 00:00s
B012(Interruptor bifuncional) :	Rem = off 00:00s+ 00:00s 00:00s 00:00s
B013(Interruptor bifuncional) :	Rem = off 00:00s+ 00:00s 00:00s 00:00s
I1(Entrada) : Pulsador fila 1	
I2(Entrada) : Pulsador fila 2	
I3(Entrada) : Pulsador fila 3	
I4(Entrada) : Pulsador fila 4	
I5(Entrada) : Interruptor crepuscular	

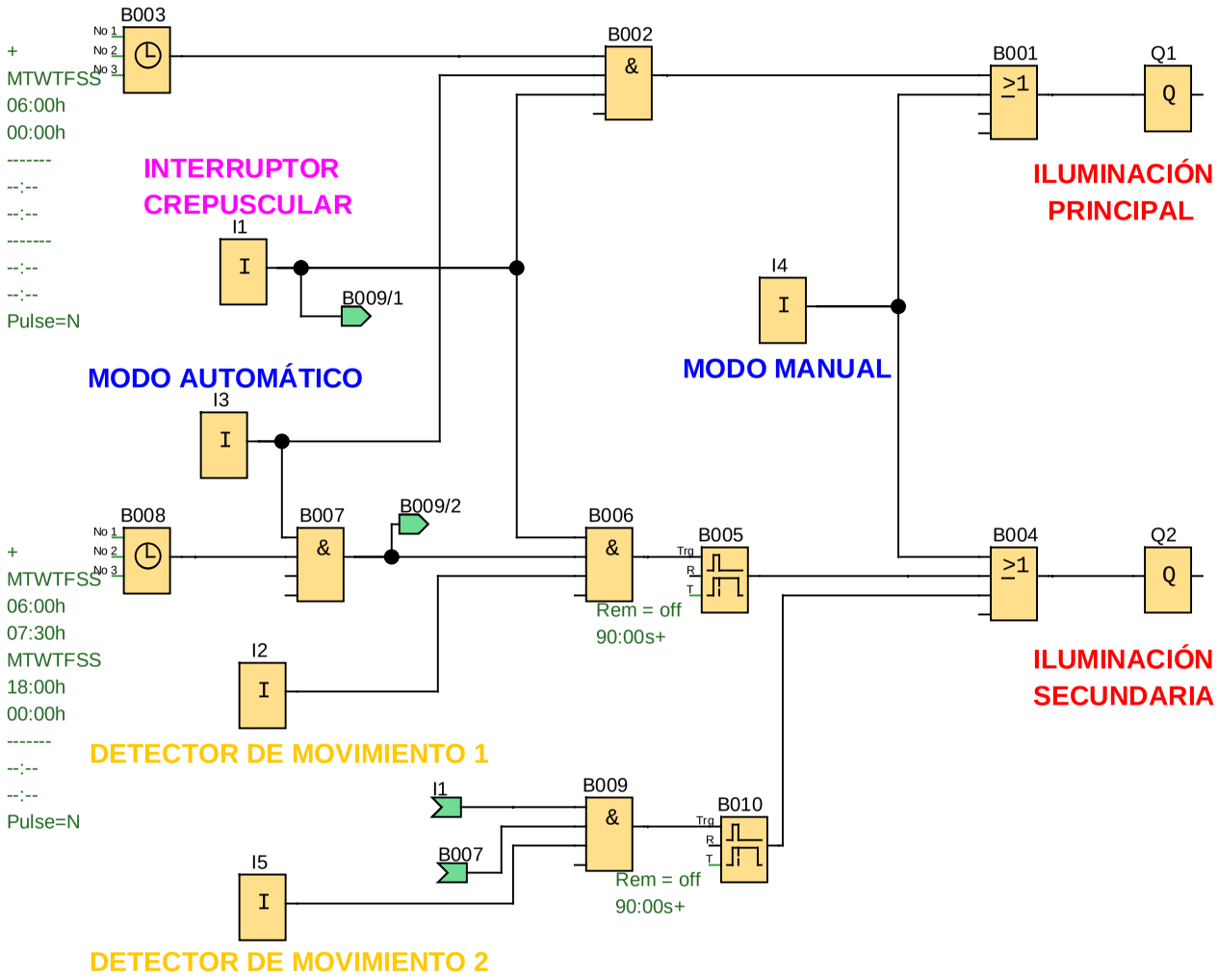
Número de bloque (tipo)	Parámetro
Q1(Salida) : FILA 1 (ventana)	
Q2(Salida) : FILA 2 (ventana)	
Q3(Salida) : FILA 3	
Q4(Salida) : FILA 4	

INTERRUPTOR AUTOMÁTICO PARA ESCALERAS O PASILLOS



Autor:	Angel Súñer de Pedro		Proyecto:	Interruptor automatico para escaleras y pasillos	Cliente:	
Comprobado:			Instalación:		Nº diagrama:	
Fecha de creación/modificación:	5/09/12 17:16/8/09/12 11:17		archivo:	Interruptor automatico de escaleras y pasillos.lsc	Página:	1 / 2

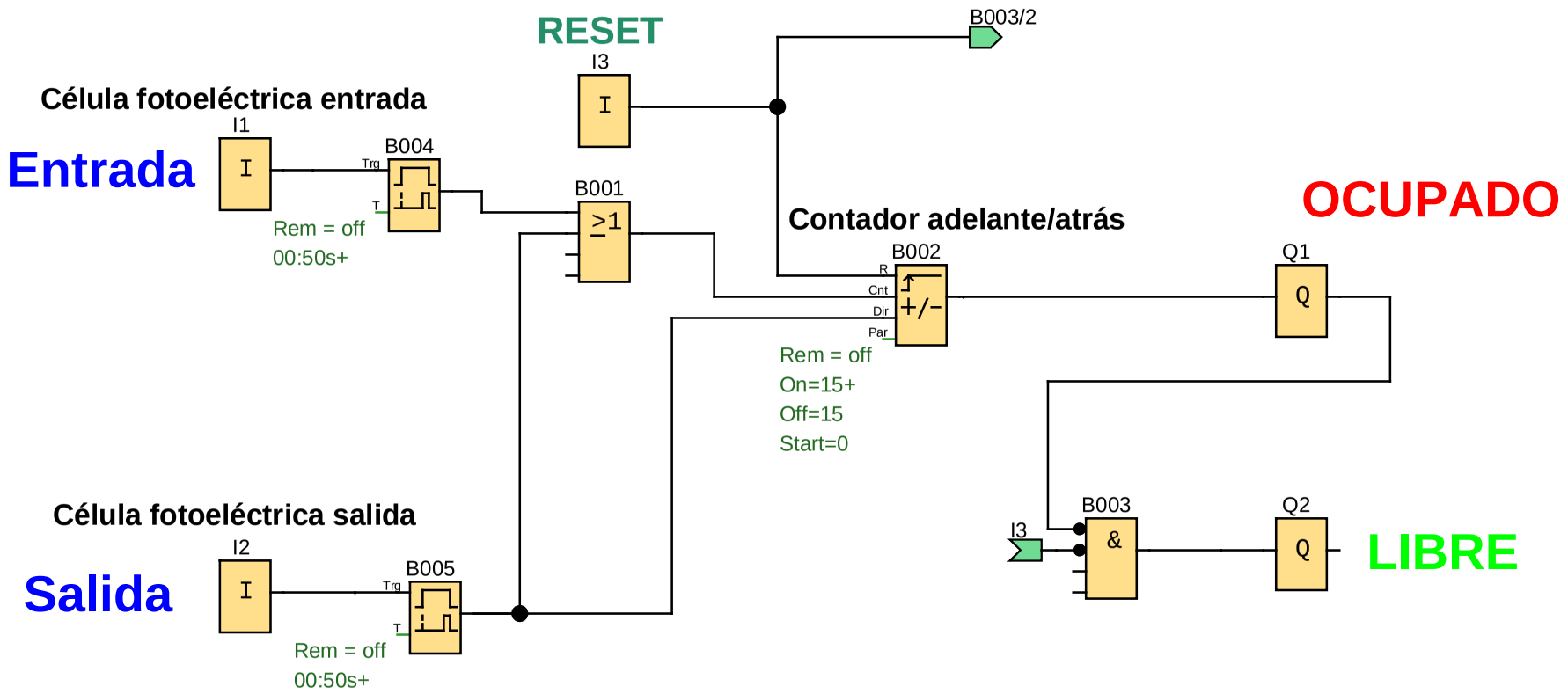
Número de bloque (tipo)	Parámetro
B001(Retardo a la conexión) :	Rem = off 01:00s+
B003(Retardo a la desconexión) : Temporizador encendido	Rem = off 20:00s+
B004(Relé autoenclavador) :	Rem = off
B007(Retardo a la conexión) : Tiempo para apagado	Rem = off 02:00s+
B009(Contador adelante/atrás) : Nº Pulsaciones para alumbrado continuo	Rem = off On=2+ Off=2
I1(Entrada) : Interruptor	
Q1(Salida) : ENCENDIDO DE LÁMPARAS	



Autor:	Ángel Súñer de Pedro		Proyecto:	Aplicaciones LOGO!	Cliente:	
Comprobado:			Instalación:	Iluminación Exterior Edificio	Nº diagrama:	
Fecha de creación/modificación:	9/06/12 18:31/8/09/12 11:14		archivo:	ILUMINACIÓN_EXTERIOR_EDIFICIO.lsc	Página:	1 / 2

Número de bloque (tipo)	Parámetro
B003(Temporizador semanal) :	+ MTWTFSS 06:00h 00:00h ------- --:-- --:-- ------- --:-- --:-- Pulse=N
B005(Retardo a la desconexión) :	Rem = off 90:00s+
B008(Temporizador semanal) :	+ MTWTFSS 06:00h 07:30h MTWTFSS 18:00h 00:00h ------- --:-- --:-- Pulse=N
B010(Retardo a la desconexión) :	Rem = off 90:00s+
I1(Entrada) : INTERRUPTOR CREPUSCULAR	
I2(Entrada) : DETECTOR DE MOVIMIENTO 1	
I3(Entrada) : MODO AUTOMÁTICO	
I4(Entrada) : MODO MANUAL	
I5(Entrada) : DETECTOR DE MOVIMIENTO 2	
Q1(Salida) : ILUMINACIÓN PRINCIPAL	
Q2(Salida) : ILUMINACIÓN SECUNDARIA	

PROGRAMA DE CONTROL DE CADA PLANTA DEL PARKING



Autor:	Angel Súñer de Pedro		Proyecto:	Aplicaciones LOGO!	Cliente:	
Comprobado:			Instalación:	Control parking	Nº diagrama:	
Fecha de creación/modificación:	22/07/12 20:25/8/09/12 11:19		archivo:	Parking_1planta.lsc	Página:	1 / 2

Número de bloque (tipo)	Parámetro
B002(Contador adelante/atrás) :	Rem = off On=15+ Off=15 Start=0
B004(Retardo a la conexión) :	Rem = off 00:50s+
B005(Retardo a la conexión) :	Rem = off 00:50s+
I1(Entrada) : Entrada	
I2(Entrada) : Salida	
I3(Entrada) : RESET	
Q1(Salida) : OCUPADO	
Q2(Salida) : LIBRE	

ANEXO 4: Datasheets

A continuación se incluyen algunas hojas de los datasheets correspondientes a los componentes utilizados en este proyecto.

Remote control & communications

Order code	Manufacturer code	Description
82-4070	HT12D	HT12D-18DIP REMOTE CONTROL DECODER (RC)
82-4074	HT12F	HT12F-18DIP REMOTE CONTROL DECODER (RC)

Sales: 01206 751166
Sales@rapidelec.co.uk
Technical: 01206 835555
Tech@rapidelec.co.uk
Fax: 01206 751188
www.rapidonline.com

2^{12} Series of Decoders

Features

- Operating voltage: 2.4V~12V
- Low power and high noise immunity CMOS technology
- Low standby current
- Capable of decoding 12 bits of information
- Pair with Holtek's 2^{12} series of encoders
- Binary address setting
- Received codes are checked 3 times
- Address/Data number combination
  - HT12D: 8 address bits and 4 data bits
  - HT12F: 12 address bits only
- Built-in oscillator needs only 5% resistor
- Valid transmission indicator
- Easy interface with an RF or an infrared transmission medium
- Minimal external components

Applications

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers
- Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

General Description

The 2^{12} decoders are a series of CMOS LSIs for remote control system applications. They are paired with Holtek's 2^{12} series of encoders (refer to the encoder/decoder cross reference table). For proper operation, a pair of encoder/decoder with the same number of addresses and data format should be chosen.

The decoders receive serial addresses and data from a programmed 2^{12} series of encoders that are transmitted by a carrier using an RF or an IR transmission medium. They compare the serial input data three times continuously with their local addresses. If no error or unmatched codes are found, the input data codes are decoded and then transferred to the output pins. The VT pin also goes high to indicate a valid transmission.

The 2^{12} series of decoders are capable of decoding informations that consist of N bits of address and 12–N bits of data. Of this series, the HT12D is arranged to provide 8 address bits and 4 data bits, and HT12F is used to decode 12 bits of address information.

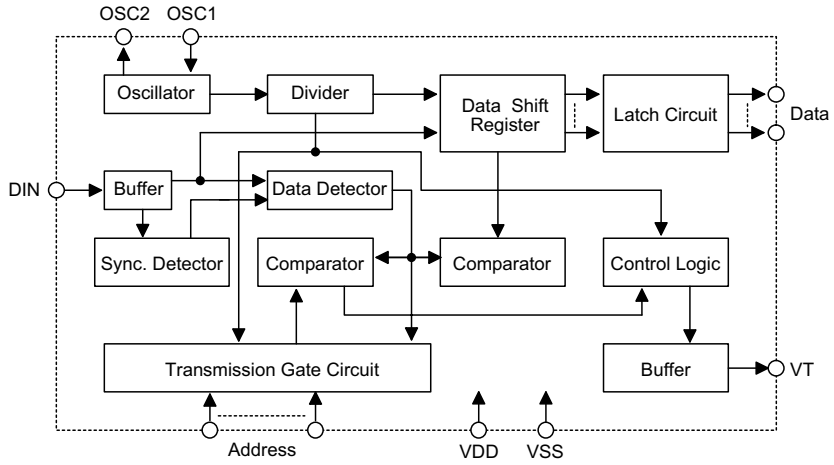
Selection Table

Function / Part No.	Address No.	Data No.	Data Type	VT	Oscillator	Trigger	Package
HT12D	8	4	L	√	RC oscillator	DIN active "Hi"	18 DIP/20 SOP
HT12F	12	0	—	√	RC oscillator	DIN active "Hi"	18 DIP/20 SOP

Notes: Data type: L stands for latch type data output.

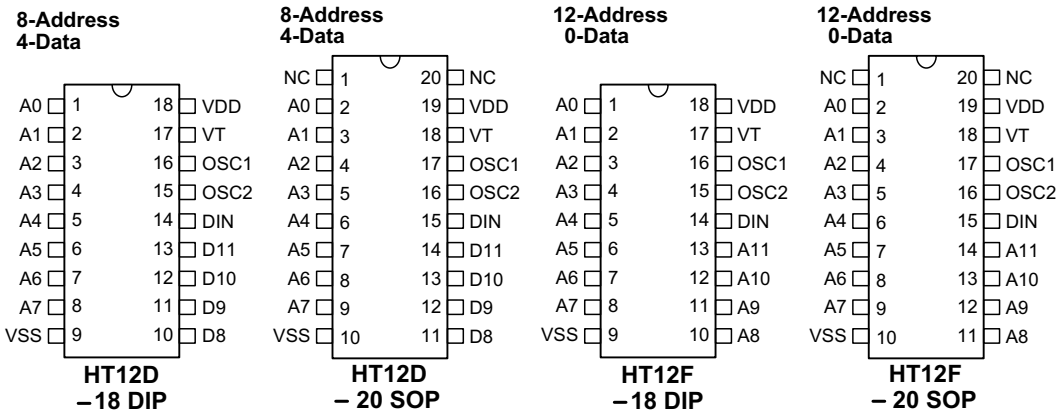
VT can be used as a momentary data output.

Block Diagram



Note: The address/data pins are available in various combinations (see the address/data table).

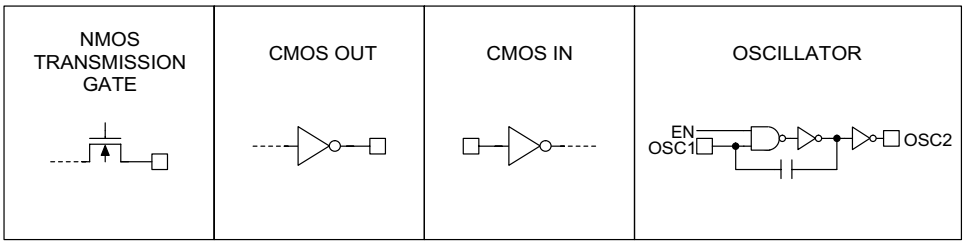
Pin Assignment



Pin Description

Pin Name	I/O	Internal Connection	Description
A0~A11	I	NMOS TRANSMISSION GATE	Input pins for address A0~A11 setting They can be externally set to VDD or VSS.
D8~D11	O	CMOS OUT	Output data pins
DIN	I	CMOS IN	Serial data input pin
VT	O	CMOS OUT	Valid transmission, active high
OSC1	I	OSCILLATOR	Oscillator input pin
OSC2	O	OSCILLATOR	Oscillator output pin
VSS	I	—	Negative power supply (GND)
VDD	I	—	Positive power supply

Approximate internal connection circuits



Absolute Maximum Ratings

Supply Voltage.....–0.3V to 13V
Input Voltage.....V_{SS}–0.3 to V_{DD}+0.3V
Storage Temperature.....–50°C to 125°C
Operating Temperature .....–20°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5	12	V
I_{STB}	Standby Current	5V	Oscillator stops	—	0.1	1	μA
		12V		—	2	4	μA
I_{DD}	Operating Current	5V	No load f_{OSC}=150kHz	—	200	400	μA
I_O	Data Output Source Current (D8~D11)	5V	V_{OH}=4.5V	–1	–1.6	—	mA
	Data Output Sink Current (D8~D11)	5V	V_{OL}=0.5V	1	1.6	—	mA
I_{VT}	VT Output Source Current	5V	V_{OH}=4.5V	–1	–1.6	—	mA
	VT Output Sink Current		V_{OL}=0.5V	1	1.6	—	mA
V_{IH}	″H″ Input Voltage	5V	—	3.5	—	5	V
V_{IL}	″L″ Input Voltage	5V	—	0	—	1	V
f_{OSC}	Oscillator Frequency	5V	R_{OSC}=51kΩ	—	150	—	kHz

Functional Description

Operation

The 2^{12} series of decoders provides various combinations of addresses and data pins in different packages so as to pair with the 2^{12} series of encoders.

The decoders receive data that are transmitted by an encoder and interpret the first N bits of code period as addresses and the last 12–N bits as data, where N is the address code number. A signal on the DIN pin activates the oscillator which in turn decodes the incoming address and data. The decoders will then check the received address three times continuously. If the received address codes all match the contents of the decoder's local address, the 12–N bits of data are decoded to activate the output pins and the VT pin is set high to indicate a valid transmission. This will last unless the address code is incorrect or no signal is received.

The output of the VT pin is high only when the transmission is valid. Otherwise it is always low.

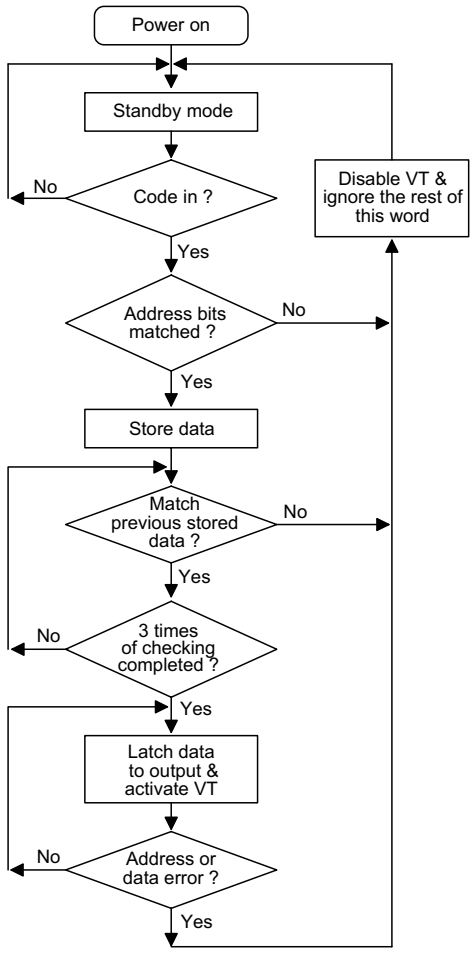
Output type

Of the 2^{12} series of decoders, the HT12F has no data output pin but its VT pin can be used as a momentary data output. The HT12D, on the other hand, provides 4 latch type data pins whose data remain unchanged until new data are received.

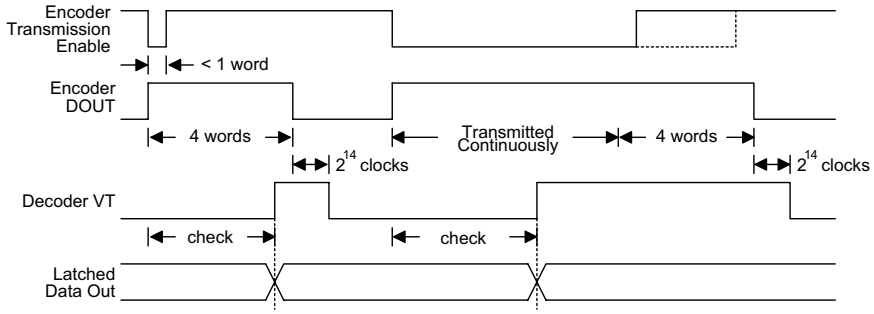
Part No.	Data Pins	Address Pins	Output Type	Operating Voltage
HT12D	4	8	Latch	2.4V~12V
HT12F	0	12	—	2.4V~12V

Flowchart

The oscillator is disabled in the standby state and activated when a logic "high" signal applies to the DIN pin. That is to say, the DIN should be kept low if there is no signal input.



Decoder timing



Encoder/Decoder cross reference table

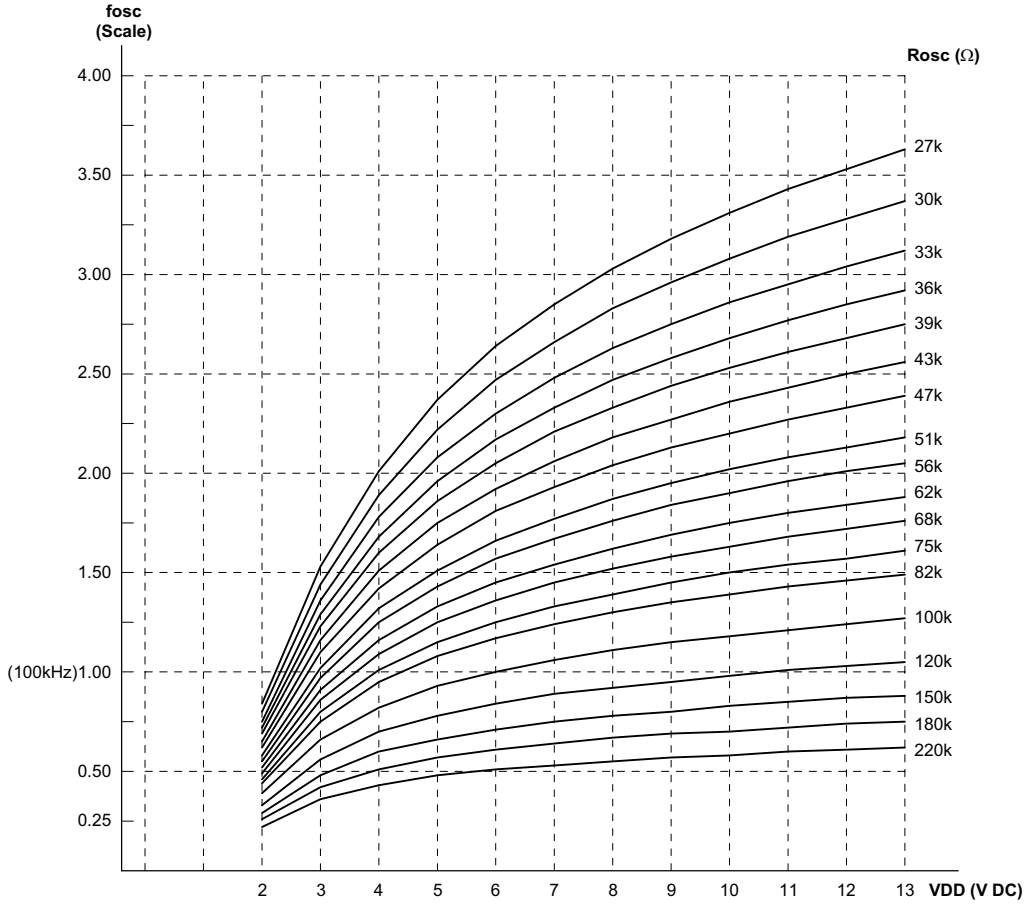
Decoders Part No.	Data Pins	Address Pins	VT	Pair Encoder	Package			
					Encoder		Decoder	
					DIP	SOP	DIP	SOP
HT12D	4	8	√	HT12A	18	20	18	20
				HT12E	18	20		
HT12F	0	12	√	HT12A	18	20	18	20
				HT12E	18	20		

Address/Data sequence

The following table provides address/data sequence for various models of the 2^{12} series of decoders. A correct device should be chosen according to the requirements of the individual addresses and data.

Part No.	Address/Data Bits											
	0	1	2	3	4	5	6	7	8	9	10	11
HT12D	A0	A1	A2	A3	A4	A5	A6	A7	D8	D9	D10	D11
HT12F	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

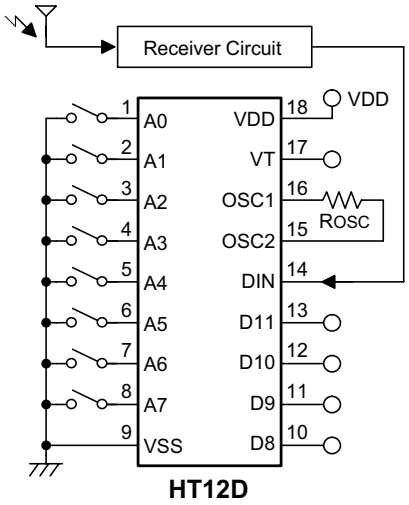
Oscillator frequency vs supply voltage



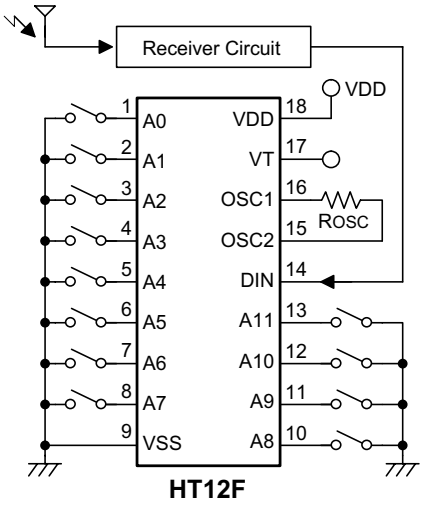
The recommended oscillator frequency is f_{OSCD} (decoder) $\cong 50\ f_{OSCE}$ (HT12E encoder)

$$\cong \frac{1}{3} f_{OSCE} \text{ (HT12A encoder).}$$

Application Circuits



HT12D



HT12F

Holtek Semiconductor Inc. (Headquarters)
No.3 Creation Rd. II, Science-based Industrial Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189

Holtek Semiconductor Inc. (Taipei Office)
11F, No.576, Sec.7 Chung Hsiao E. Rd., Taipei, Taiwan
Tel: 886-2-2782-9635
Fax: 886-2-2782-9636
Fax: 886-2-2782-7128 (International sales hotline)

Holtek Semiconductor (Hong Kong) Ltd.
RM.711, Tower 2, Cheung Sha Wan Plaza, 833 Cheung Sha Wan Rd., Kowloon, Hong Kong
Tel: 852-2-745-8288
Fax: 852-2-742-8657

Holtek Semiconductor (Shanghai) Ltd.
7th Floor, Building 2, No.889, Yi Shan Road, Shanghai, China
Tel:021-6485-5560
Fax:021-6485-0313

Holmate Technology Corp.
48531 Warm Springs Boulevard, Suite 413, Fremont, CA 94539
Tel: 510-252-9880
Fax: 510-252-9885

Remote control & communications

Order code	Manufacturer code	Description
82-4072	HT12A	HT12A-18DIP REMOTE CONTROL DECODER
82-4076	HT12E	HT12E-18DIP REMOTE CONTROL DECODER

Sales: 01206 751166 **Technical: 01206 835555** **Fax: 01206 7551188**
Sales@rapidelec.co.uk **Tech@rapidelec.co.uk** **www.rapidelectronics.co.uk**

HT12A/HT12E
2^{12} Series of Encoders

Features

- Operating voltage
  - 2.4V~5V for the HT12A
  - 2.4V~12V for the HT12E
- Low power and high noise immunity CMOS technology
- Low standby current: 0.1μA (typ.) at V_{DD}=5V
- HT12A with a 38kHz carrier for infrared transmission medium
- Minimum transmission word
  - Four words for the HT12E
  - One word for the HT12A
- Built-in oscillator needs only 5% resistor
- Data code has positive polarity
- Minimal external components
- HT12A/E: 18-pin DIP/20-pin SOP package

Applications

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers
- Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

General Description

The 2^{12} encoders are a series of CMOS LSIs for remote control system applications. They are capable of encoding information which consists of N address bits and 12–N data bits. Each address/data input can be set to one of the two logic states. The programmed addresses/data are transmitted together with the header bits via an RF or an infrared transmission medium upon receipt of a trigger signal. The capability to select a $\overline{TE}$ trigger on the HT12E or a DATA trigger on the HT12A further enhances the application flexibility of the 2^{12} series of encoders. The HT12A additionally provides a 38kHz carrier for infrared systems.

Selection Table

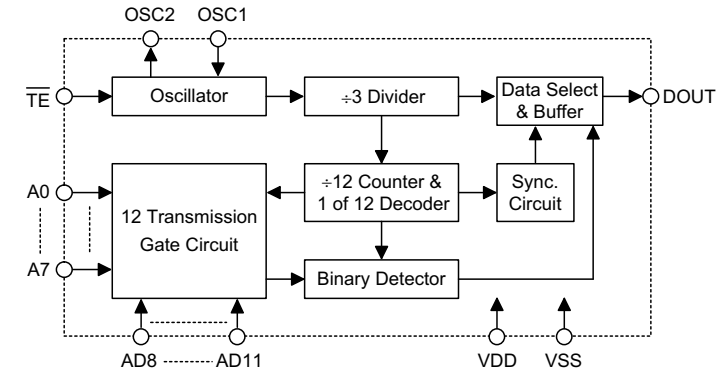
Function / Part No.	Address No.	Address/ Data No.	Data No.	Oscillator	Trigger	Package	Carrier Output	Negative Polarity
HT12A	8	0	4	455kHz resonator	D8~D11	18 DIP 20 SOP	38kHz	No
HT12E	8	4	0	RC oscillator	$\overline{TE}$	18 DIP 20 SOP	No	No

Note: Address/Data represents pins that can be address or data according to the decoder requirement.

Block Diagram

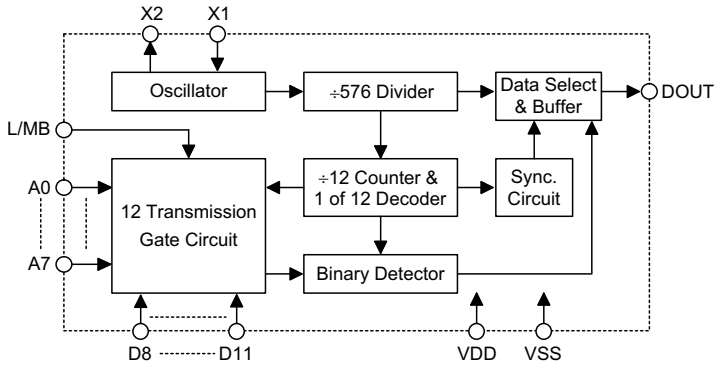
$\overline{TE}$ trigger

HT12E



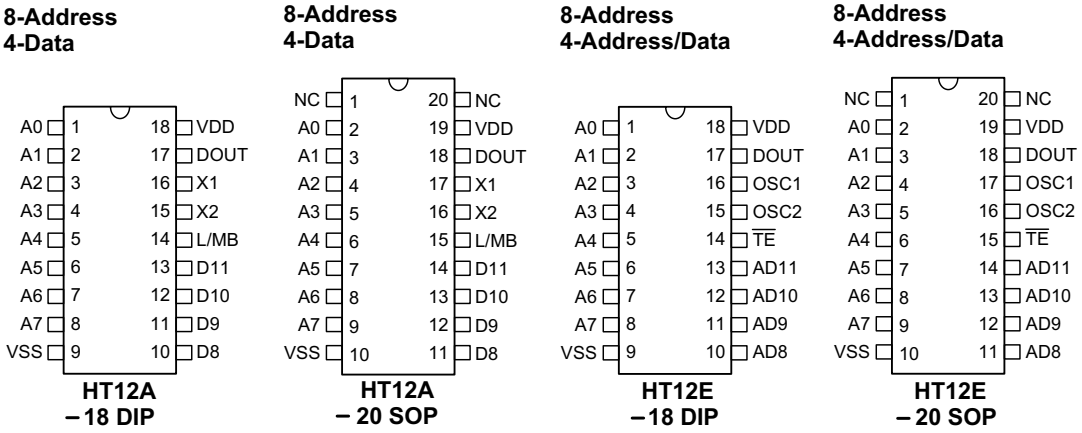
DATA trigger

HT12A



Note: The address data pins are available in various combinations (refer to the address/data table).

Pin Assignment



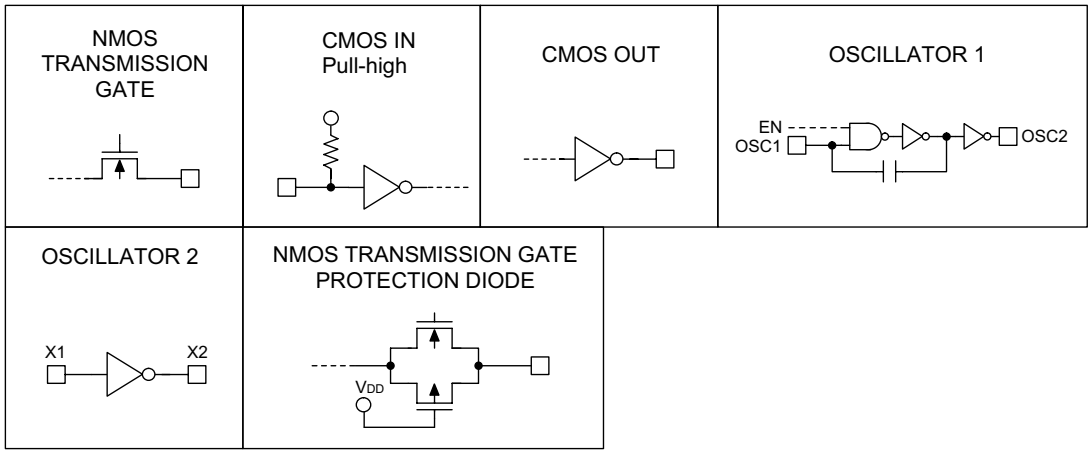
Pin Description

Pin Name	I/O	Internal Connection	Description
A0~A7	I	CMOS IN Pull-high (HT12A) NMOS TRANSMISSION GATE PROTECTION DIODE (HT12E)	Input pins for address A0~A7 setting These pins can be externally set to VSS or left open
AD8~AD11	I	NMOS TRANSMISSION GATE PROTECTION DIODE (HT12E)	Input pins for address/data AD8~AD11 setting These pins can be externally set to VSS or left open
D8~D11	I	CMOS IN Pull-high	Input pins for data D8~D11 setting and transmission enable, active low These pins should be externally set to VSS or left open (see Note)
DOUT	O	CMOS OUT	Encoder data serial transmission output
L/MB	I	CMOS IN Pull-high	Latch/Momentary transmission format selection pin: Latch: Floating or VDD Momentary: VSS

Pin Name	I/O	Internal Connection	Description
$\overline{TE}$	I	CMOS IN Pull-high	Transmission enable, active low (see Note)
OSC1	I	OSCILLATOR 1	Oscillator input pin
OSC2	O	OSCILLATOR 1	Oscillator output pin
X1	I	OSCILLATOR 2	455kHz resonator oscillator input
X2	O	OSCILLATOR 2	455kHz resonator oscillator output
VSS	I	—	Negative power supply, grounds
VDD	I	—	Positive power supply

Note: D8~D11 are all data input and transmission enable pins of the HT12A.
$\overline{TE}$ is a transmission enable pin of the HT12E.

Approximate internal connections



Absolute Maximum Ratings

Supply Voltage (HT12A) .....–0.3V to 5.5V
Input Voltage.....V_{SS}–0.3 to V_{DD}+0.3V
Operating Temperature.....–20°C to 75°C
Supply Voltage (HT12E) .....–0.3V to 13V
Storage Temperature.....–50°C to 125°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

HT12A Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	3	5	V
I_{STB}	Standby Current	3V	Oscillator stops	—	0.1	1	μA
		5V		—	0.1	1	μA
I_{DD}	Operating Current	3V	No load f_{OSC}=455kHz	—	200	400	μA
		5V		—	400	800	μA
I_{DOUT}	Output Drive Current	5V	V_{OH}=0.9V_{DD} (Source)	–1	–1.6	—	mA
			V_{OL}=0.1V_{DD} (Sink)	2	3.2	—	mA
V_{IH}	"H" Input Voltage	—	—	0.8V_{DD}	—	V_{DD}	V
V_{IL}	"L" Input Voltage	—	—	0	—	0.2V_{DD}	V
R_{DATA}	D8~D11 Pull-high Resistance	5V	V_{DATA}=0V	—	150	300	kΩ

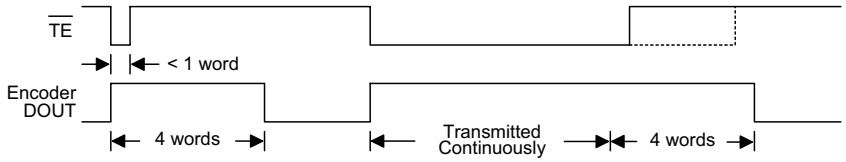
HT12E Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5	12	V
I_{STB}	Standby Current	3V	Oscillator stops	—	0.1	1	μA
		12V		—	2	4	μA
I_{DD}	Operating Current	3V	No load f_{OSC}=3kHz	—	40	80	μA
		12V		—	150	300	μA
I_{DOUT}	Output Drive Current	5V	V_{OH}=0.9V_{DD} (Source)	–1	–1.6	—	mA
			V_{OL}=0.1V_{DD} (Sink)	1	1.6	—	mA
V_{IH}	"H" Input Voltage	—	—	0.8V_{DD}	—	V_{DD}	V
V_{IL}	"L" Input Voltage	—	—	0	—	0.2V_{DD}	V
f_{OSC}	Oscillator Frequency	5V	R_{OSC}=1.1MΩ	—	3	—	kHz
$R_{\overline{TE}}$	$\overline{TE}$ Pull-high Resistance	5V	$V_{\overline{TE}}$=0V	—	1.5	3	MΩ

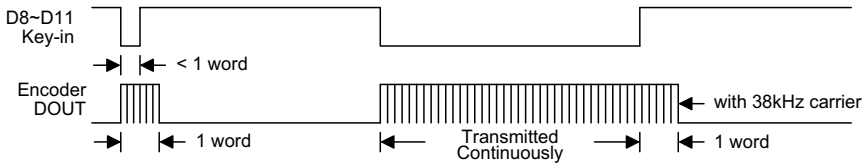
Functional Description

Operation

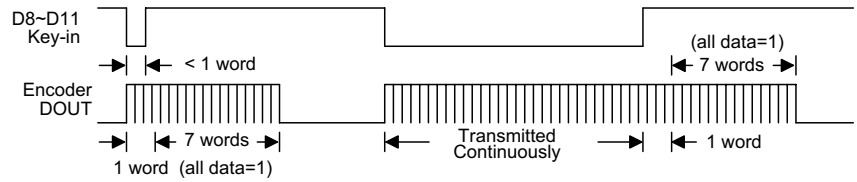
The 2^{12} series of encoders begin a 4-word transmission cycle upon receipt of a transmission enable ($\overline{TE}$ for the HT12E or D8~D11 for the HT12A, active low). This cycle will repeat itself as long as the transmission enable ($\overline{TE}$ or D8~D11) is held low. Once the transmission enable returns high the encoder output completes its final cycle and then stops as shown below.



Transmission timing for the HT12E



Transmission timing for the HT12A (L/MB=Floating or VDD)

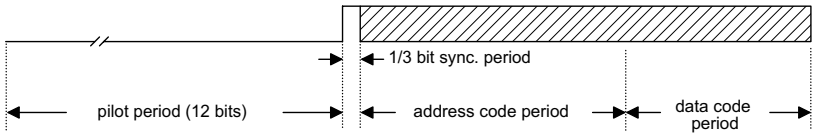


Transmission timing for the HT12A (L/MB=VSS)

Information word

If L/MB=1 the device is in the latch mode (for use with the latch type of data decoders). When the transmission enable is removed during a transmission, the DOUT pin outputs a complete word and then stops. On the other hand, if L/MB=0 the device is in the momentary mode (for use with the momentary type of data decoders). When the transmission enable is removed during a transmission, the DOUT outputs a complete word and then adds 7 words all with the "1" data code.

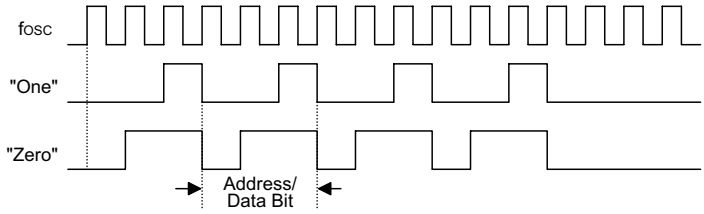
An information word consists of 4 periods as illustrated below.



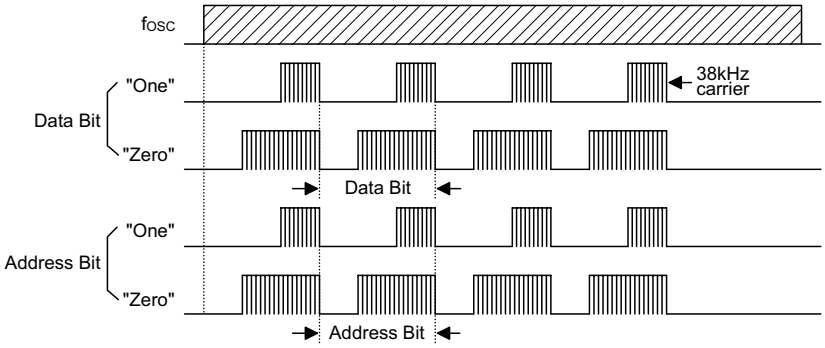
Composition of information

Address/data waveform

Each programmable address/data pin can be externally set to one of the following two logic states as shown below.



Address/Data bit waveform for the HT12E



Address/Data bit waveform for the HT12A

The address/data bits of the HT12A are transmitted with a 38kHz carrier for infrared remote controller flexibility.

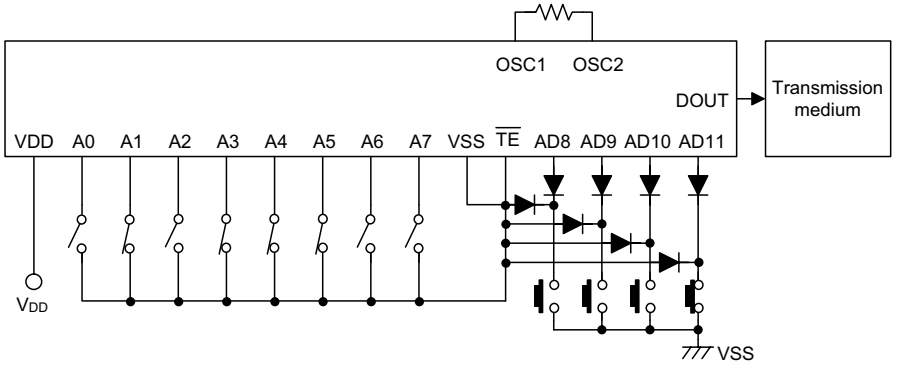
Address/data programming (preset)

The status of each address/data pin can be individually pre-set to logic "high" or "low". If a transmission-enable signal is applied, the encoder scans and transmits the status of the 12 bits of address/data serially in the order A0 to AD11 for the HT12E encoder and A0 to D11 for the HT12A encoder.

During information transmission these bits are transmitted with a preceding synchronization bit. If the trigger signal is not applied, the chip enters the standby mode and consumes a reduced current of less than 1μA for a supply voltage of 5V.

Usual applications preset the address pins with individual security codes using DIP switches or PCB wiring, while the data is selected by push buttons or electronic switches.

The following figure shows an application using the HT12E:



The transmitted information is as shown:

Pilot & Sync.	A0 1	A1 0	A2 1	A3 0	A4 0	A5 0	A6 1	A7 1	AD8 1	AD9 1	AD10 1	AD11 0

Address/Data sequence

The following provides the address/data sequence table for various models of the 2^{12} series of encoders. The correct device should be selected according to the individual address and data requirements.

Part No.	Address/Data Bits											
	0	1	2	3	4	5	6	7	8	9	10	11
HT12A	A0	A1	A2	A3	A4	A5	A6	A7	D8	D9	D10	D11
HT12E	A0	A1	A2	A3	A4	A5	A6	A7	AD8	AD9	AD10	AD11

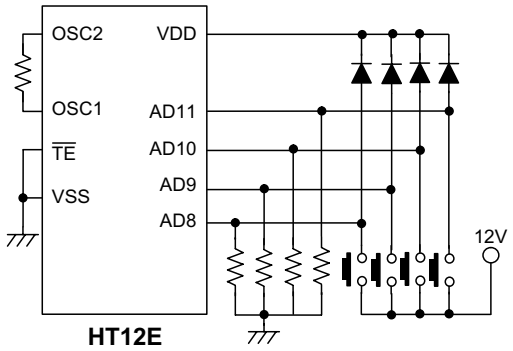
Transmission enable

For the HT12E encoders, transmission is enabled by applying a low signal to the $\overline{TE}$ pin. For the HT12A encoders, transmission is enabled by applying a low signal to one of the data pins D8~D11.

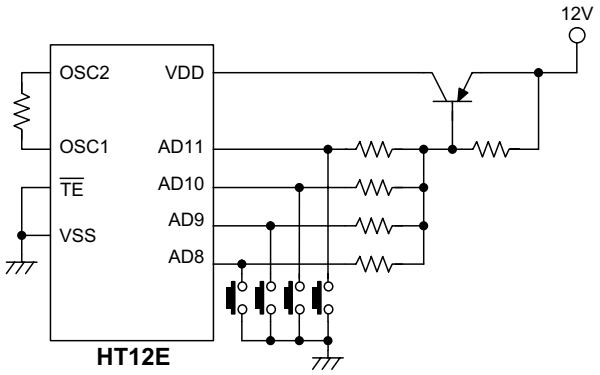
Two erroneous HT12E application circuits

The HT12E must follow closely the application circuits provided by Holtek (see the "Application circuits").

- Error: AD8~AD11 pins input voltage > V_{DD}+0.3V

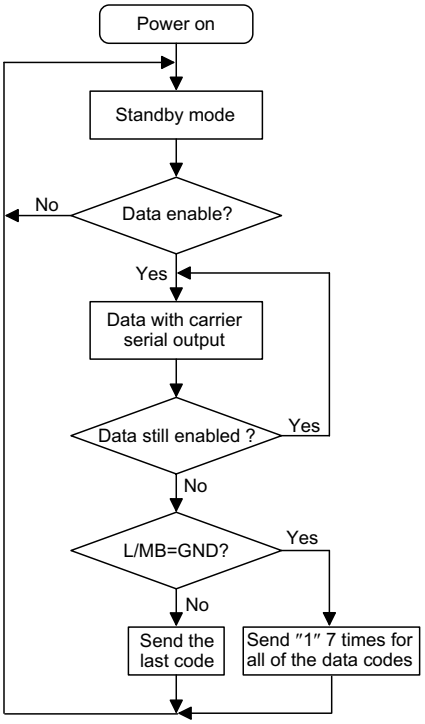


• Error: The IC′s power source is activated by pins AD8~AD11

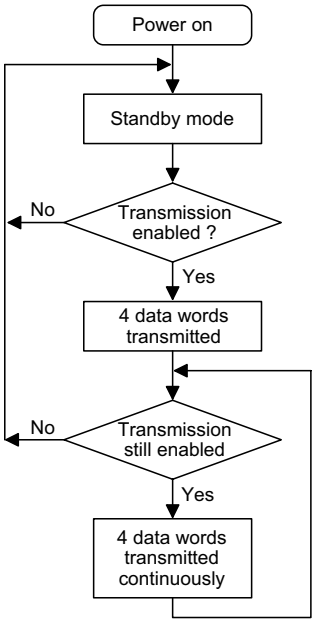


Flowchart

• HT12A

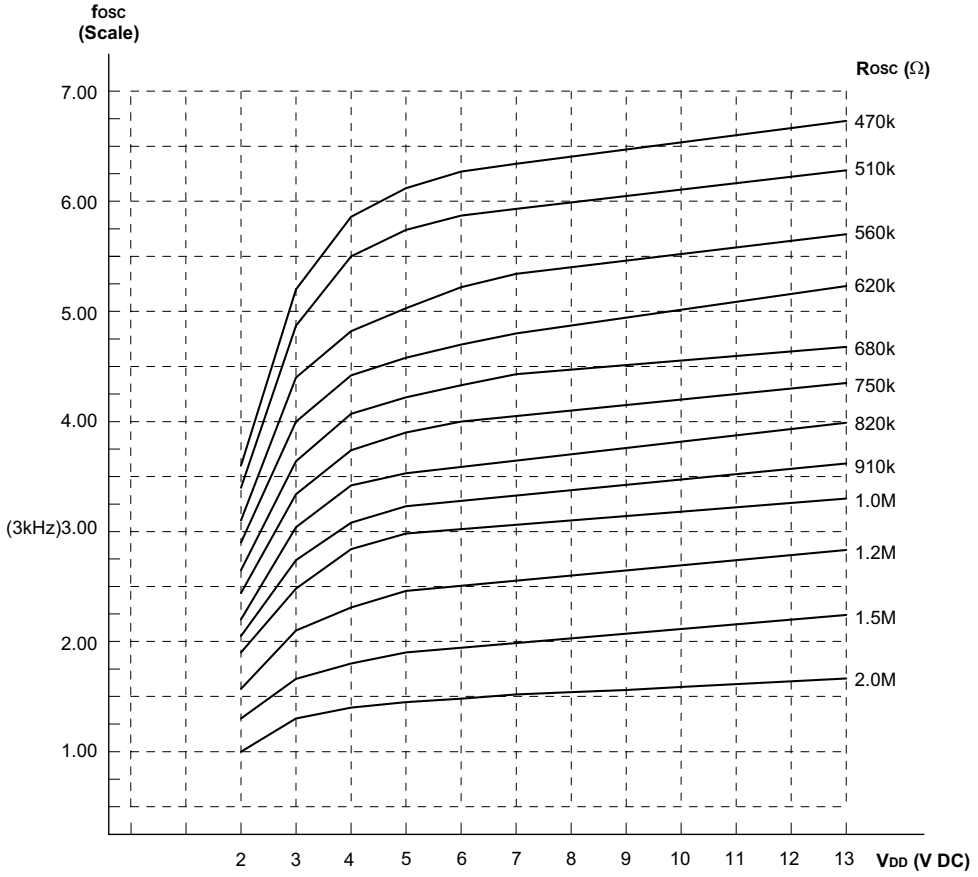


• HT12E



Note: D8~D11 are transmission enables of the HT12A.
$\overline{TE}$ is the transmission enable of the HT12E.

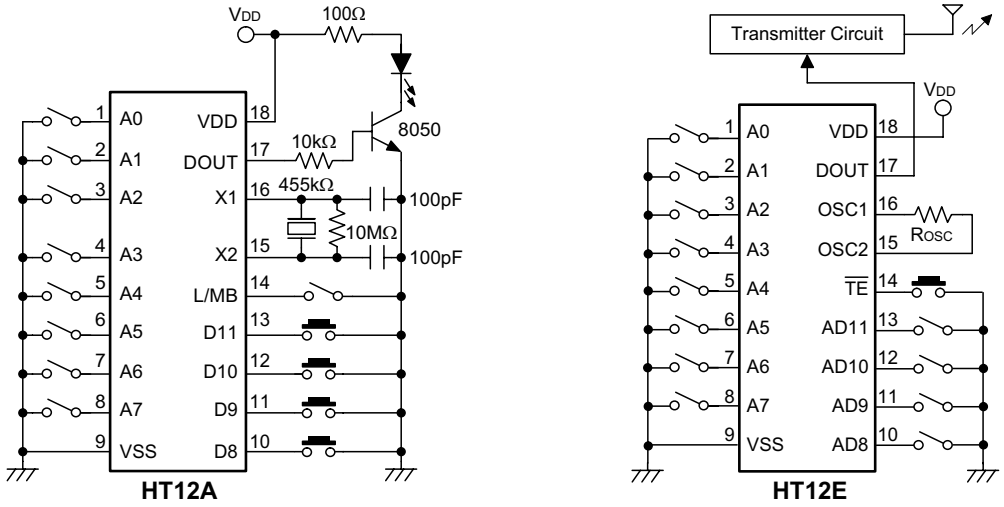
Oscillator frequency vs supply voltage



The recommended oscillator frequency is f_{OSCD} (decoder) $\cong 50\ f_{OSCE}$ (HT12E encoder)

$$\cong \frac{1}{3} f_{OSCE} \text{ (HT12A encoder)}$$

Application Circuits



Note: Typical infrared diode: EL-1L2 (KODENSHI CORP.)
Typical RF transmitter: JR-220 (JUWA CORP.)

Holtek Semiconductor Inc. (Headquarters)
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Fax: 886-2-2782-7128 (International sales hotline)

Holtek Semiconductor (Hong Kong) Ltd.
RM.711, Tower 2, Cheung Sha Wan Plaza, 833 Cheung Sha Wan Rd., Kowloon, Hong Kong
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Holtek Semiconductor (Shanghai) Ltd.
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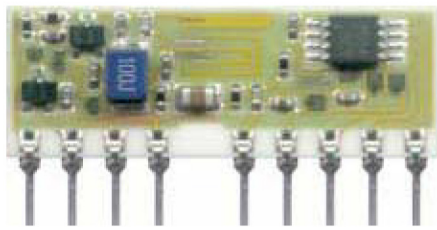
Tel: 021-6485-5560
Fax: 021-6485-0313

Holmate Technology Corp.
48531 Warm Springs Boulevard, Suite 413, Fremont, CA 94539
Tel: 510-252-9880
Fax: 510-252-9885

Order code	Manufacturer code	Description
43-0384	n/a	SUPERREGEN RECEIVER MODULE (RC)

Sales: 01206 751166
Sales@rapidelec.co.uk
Technical: 01206 835555
Tech@rapidelec.co.uk
Fax: 01206 751188
www.rapidonline.com

- 50% smaller than standard hybrid modules.
- Standard Frequencies; 315, 433MHz
- Frequencies Available: 300-450MHz
- Very High Frequency Stability (No Adjustable Components).
- Receiving Range Up To 50 Metres.
- CMOS/TTL Compatible Output.
- Compatible With R.F. Solutions AM Transmitters.
- Patented Laser Trimmed Inductor.
- Compliant To ETSI300-220.
- Requires No Radio Licence To Operate.



Description

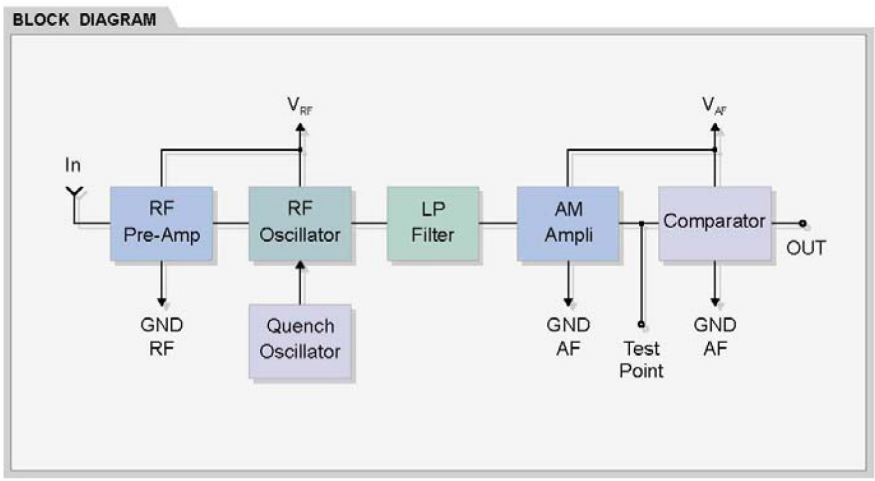
The R.F. Solutions Miniature AM 'Super Regen' Receiver module is an extremely compact hybrid RF receiver, which can be used to capture undecoded data from any AM Transmitter, such as R.F. Solutions AM-RT4 / 5 range of transmitters. (See AM Transmitter datasheet DS013).

These modules show a very high frequency stability over a wide operating temperature even when subjected to mechanical vibrations or manual handling. A unique laser trimming process which has been patented gives a very accurate on board inductor, removing the need for any adjustable components.

All receivers are compatible, producing a CMOS/TTL output, and require connections to power and antenna only.

RF Solutions also offer a range of Super Heterodyne Receivers, for data on these products (please see Datasheet DS017).

Block Diagram

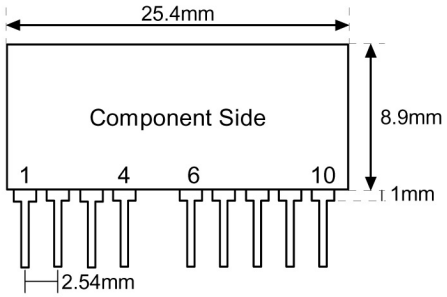


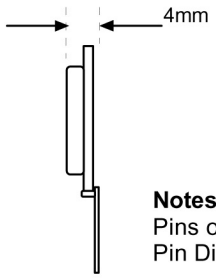
Part Numbers

The following modules are available from stock although any frequency between 300-450MHz is available upon request.

Part Number	Description
AM-HRR30-433	Compact Hybrid Receiver Module, 433MHz
AM-HRR60-433	Compact Hybrid Receiver Module, 433MHz

Mechanical Details





Notes
Pins on 0.1" pitch
Pin Dims :0.25 x 0.50mm

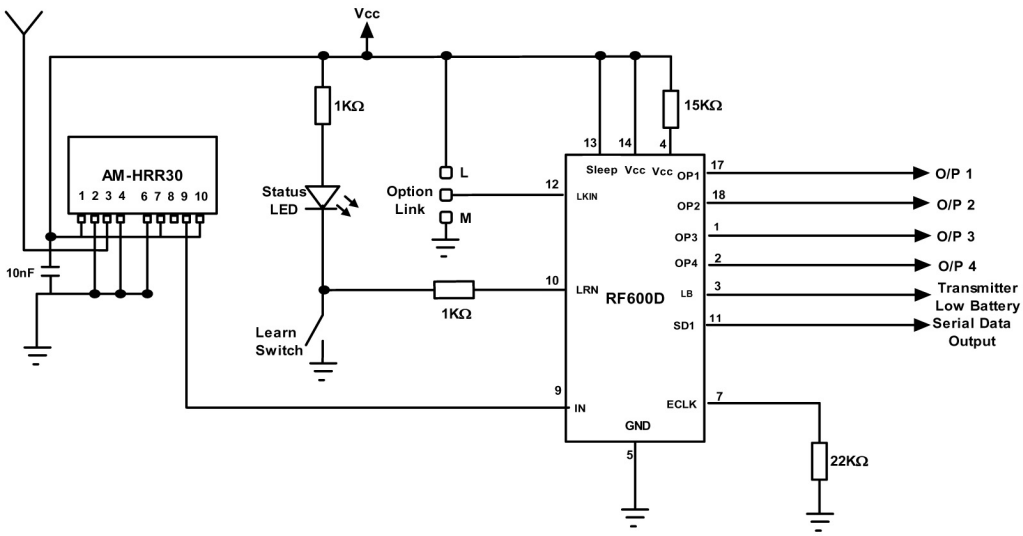
Pin	Pin Name
1	RF +Vcc
2	RF GND
3	DATA IN (Ant)
4	RF GND
6	AF GND
7	AF +VCC
8	TEST POINT
9	DATA OUT
10	AF +VCC

Electrical Characteristics

Ambient temperature = 25° Celsius.

ELECTRICAL CHARACTERISTICS	MIN	TYPICAL	MAX	DIMENSION
Operating Temperature Range	-25		+80	°C
Tuning Tolerance		± 0.2	± 0.5	MHz
Receiver Frequency (315 MHz versions)		315		MHz
Receiver Frequency (433 MHz versions)		433.92		MHz
Supply Voltage	4.5	5	5.5	V
Supply Current		2.5	3	mA
Data Rate	50		4800	bits/Sec
R.F Sensitivity 100% AM	-100	-105		dBm
-3dB Bandwidth		± 2	± 3	MHz
Conducted Spurious Emissions			-60	dBm
High Level Output Voltage	3.6			V
Low Level Output Voltage			0.6	V

Application Circuit

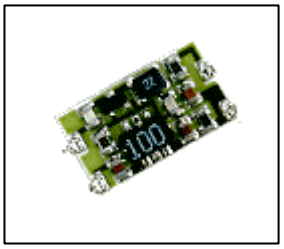


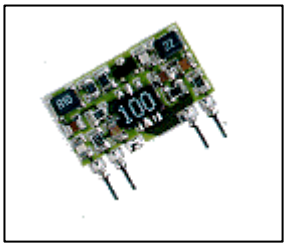
AM Hybrid Transmitter

AM-RTn-XXX

FEATURES

- COMPLETE RF TRANSMITTER
- TRANSMIT RANGE UP TO 70m
- CMOS/TTL INPUT
- AVAILABLE IN DIL OR SIL PACKAGE
- NO ADJUSTABLE COMPONENTS
- VERY STABLE OPERATING FREQUENCY
- LOW CURRENT CONSUMPTION (TYP 4mA)
- LOW SPURIOUS EMISSIONS (-35dBc)
- WIDE OPERATING VOLTAGE (2-14V)
- AVAILABLE AS 315, 418 OR 433 MHz
- COMPATIBLE WITH RF SOLUTIONS RECEIVERS





APPLICATIONS

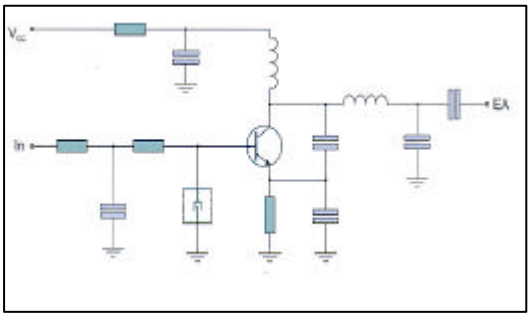
- WIRELESS SECURITY SYSTEMS
- CAR ALARMS
- REMOTE GATE CONTROLS
- REMOTE SENSING
- DATA CAPTURE
- SENSOR REPORTING

DESCRIPTION

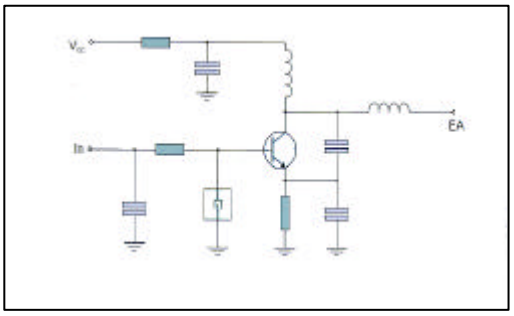
The R F Solutions Ltd. AM hybrid transmitter module provides a complete RF transmitter which can be used to transmit data at up to 4 kHz from any standard CMOS/TTL source.
The module is very simple to operate and offers low current consumption (typ. 4 mA). Data can be supplied directly from a microprocessor or encoding device, thus keeping the component count down and ensuring a low hardware cost.
The module exhibits extremely stable electronic characteristics due to the use of 'Thick-Film' hybrid technology, which uses no adjustable components and ensures very reliable operation.
The modules are compatible with R F solutions Ltd. range of AM receivers to provide a complete solution.

CIRCUIT SCHEMATICS

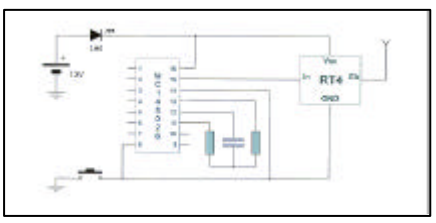
RT4



RT5

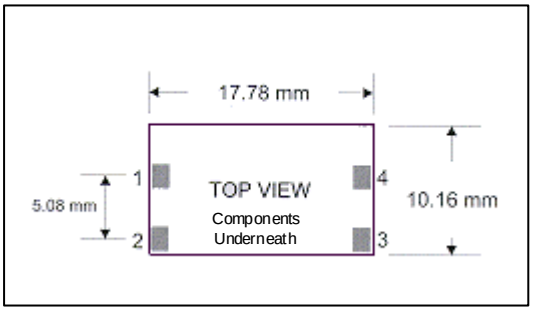


TYPICAL APPLICATION

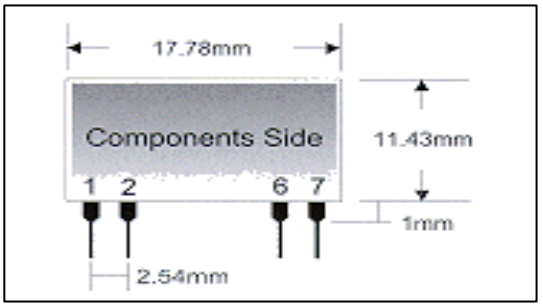


MECHANICAL DIMENSIONS

RT4



RT5



PIN DESCRIPTIONS

RT4 Pin	RT5 Pin	Name	Description
1	7	Vcc	Supply Voltage
2	6	GND	Ground, Connect to RF earth return path
3	2	IN	Data input
4	1	EA	External Antenna

ELECTRICAL CHARACTERISTICS

Ambient temp = 25°C unless otherwise stated.

Characteristic	Min.	Typ.	Max.	Dimensions
Supply Voltage	2		14	Vdc
Supply Current (Vcc=5V IN=1kHz)		4		mA
Supply Current (Vcc=5V IN=DC)		50		nA
Working Frequency	303.8		433.92	MHz
RF Output Power into 50Ω (Vcc=5V)		0		-dBm
Harmonic Spurious Emissions		-30		-dBc
Input Voltage High	2		Vcc	V
Time from Power on to data transmission		10		µSec
Data Rate	50		4000	Hz
Operating Temperature	-25		+80	°C

PART NUMBERING

PART Number	Description
AM-RT4-418	DIL AM Transmitter Module 418 MHz
AM-RT4-433	DIL AM Transmitter Module 433 MHz
AM-RT5-418	SIL AM Transmitter Module 418 MHz
AM-RT5-433	SIL AM Transmitter Module 433 MHz

Should you require further assistance, please call;

R. F. Solutions Ltd.,
Unit 21, Cliffe Industrial Estate,
South Street,
Lewes,
E Sussex, BN8 6JL. England.

Tel +44 (0)1273 898 000. Fax +44 (0)1273 480 661.

Email sales@rfsolutions.co.uk

http://www.rfsolutions.co.uk

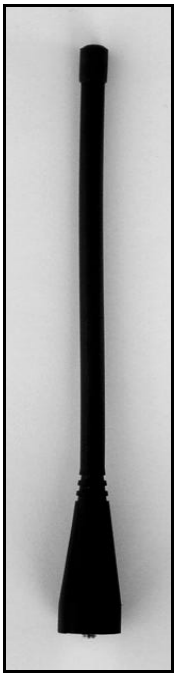
R F Solutions Ltd is a member of the Low Power radio Association

Antenna

A range of high quality antennae designed and manufactured for operation specifically with Low power short range telemetry systems. Using one of the following antennae will give optimum range and reliability to your application.

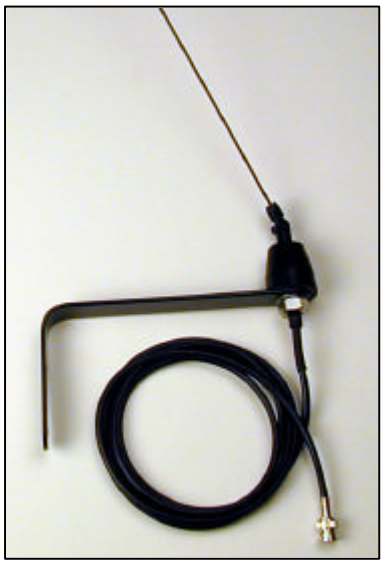
‘STUBBY’ HELICAL ANTENNA

- $^1/_4$ WAVELENGTH **HELICAL** ANTENNA
- RUGGED PLASTIC FINISH, FLEXIBLE ANTENNA



$^1/_4$ WAVE FLEXIBLE ANTENNA

- STANDARD $^1/_4$ WAVELENGTH **WHIP** ANTENNA
- RUGGED PLASTIC FINISH. FLEXIBLE ANTENNA
- BNC CONNECTION AVAILABLE ON REQUEST



+3dB GAIN ANTENNA

- +3dB GAIN $^5/_8$ WAVELENGTH WHIP ANTENNA
- INTEGRAL WALL MOUNTING BRACKET
- SUPPLIED WITH 2 METRES COAX CABLE & BNC (50Ω)

Note: In order to comply with the UK DTI Regulations, a Gain antenna must not be used on any transmitting device.

Dimensions (mm)								
	$^1/_4$ WAVE FLEXI		HELICAL		+3dB GAIN		YAGI	
	Length	Dia	Length	Dia	Length	Dia	Length	Dia
173MHz			88	13				
418 & 433MHz	170	15	43	13	170	13		
458MHz	158	15	66	15				

Part Numbers				
	173MHz	**418MHz**	**433MHz**	**458MHz**
$^1/_4$ WAVE FLEXI ANT (4BA Screw)	FLEXI-4BA-173	FLEXI-4BA-418	FLEXI-4BA-433	
$^1/_4$ WAVE FLEXI ANT (BNC Conn)	FLEXI-BNC-173	FLEXI-BNC-418	FLEXI-BNC-433	
‘HELICAL’ ANTENNA (4BA Screw)	PH-4BA-173	PU-4BA-418	PU-4BA-433	PU-4BA-458
‘HELICAL’ ANTENNA (BNC Conn)	PH-BNC-173	PU-BNC-418	PU-BNC-433	PU-BNC-458
+3dB GAIN ANTENNA	SR150M/TS	MB450-RFS418	MB450-RFS433	MB450-RFS458
YAGI				YAGI-458

Optoelectronic Devices

Order code	Manufacturer code	Description
58-0134	n/a	MINIATURE PHOTORESISTOR NON ROHS

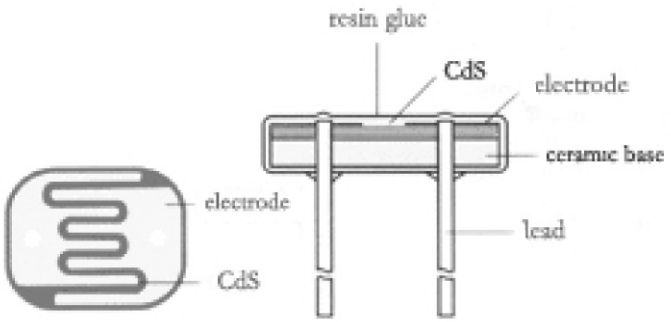
Sales: 01206 751166 **Technical: 01206 835555** **Fax: 01206 751188**
Sales@rapidelec.co.uk **Tech@rapidelec.co.uk** **www.rapidonline.com**

58-0134 Photoresistor

This device consists of a resistor which is made of semiconductor material whose conductance changes with variations in luminance.

The device can be manufactured with different figures and illuminated areas. Photoresistors are widely used in many industries, such as toys, lamps, cameras, etc.

Schematic Drawing



Performance and Features

- Coated with epoxy
- Small volume
- Fast response
- Good reliability
- High sensitivity
- Good spectrum characteristic

Typical Applications

- Camera automatic photometry
- Lighting control
- Industrial control
- Light control lamp
- Photoelectric control
- Annunciator
- Light control switch
- Electronic toy

Types and Specifications

Dark resistance	Voltage max.	Power max.	Environmental temp.	Spectrum peak value
1MΩ	150V	100mW	–30°C to +70°C	540

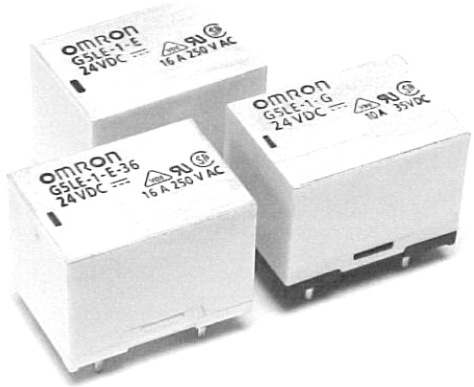
OMRON

PCB Relay | G5LE-E/-G

Single-pole 10A35VDC 0.8mm Contact Gap Power Relay : G5LE-G

Single-pole 16A250VAC Power Relay : G5LE-E

- Sub-miniature 'sugar cube ' relay with universal terminal footprint.
- UL class-F coil insulation system.
- Tracking resistance: CTI>250.
- Withstands impulse of up to 4,500 V.
- RoHS compliant.



VDE
REG.-Nr.6850

Ordering Information

Enclosure Rating	Contact Form	Rated load	
		10A 35VDC	16A 250VAC
Flux protection	SPDT	G5LE-1-G	G5LE-1-E
	SPST-NO	G5LE-1A-G	G5LE-1A-E

Note: When ordering, add the rated coil voltage to the number.
Examples : G5LE-1-E 12 VDC
Rated coil voltage

■ Model Number Legend

G5LE - ☐ ☐ - ☐ - ☐ - ☐ - ☐ - ☐ ☐VDC
1 2 3 4 5 6 7 8

1. Number of Poles
1 : 1 pole

2. Contact Form
None : SPDT
A : SPST-NO

3. Enclosure ratings
None : Flux protection

4. Insulation System
None : Class F (155°C)

8 Rated Coil Voltage
5, 12 & 24 (for suffix-E)
9, 12, 20 & 24 (for suffix-G)

5. Classification
G : 0.8mm contact gap type
E : High capacity type

6. Coil Power Consumption / Coil Characteristics
None : Approx. 400mW (applicable to suffix -E only)
None : Approx. 700mW (applicable to suffix -G only)
36 : Approx. 360mW (applicable to suffix -E only)

7. Packaging
None : Standards Polystyrene tray
SP : Anti-static Tube packing

Specifications

■ Coil Ratings

700-mW Type (G5LE-G)

Rated voltage	9 VDC	12 VDC	20 VDC	24 VDC
Rated current	77.8 mA	58.3 mA	35.0 mA	29.2 mA
Coil resistance	115.7 Ω	205.7 Ω	571.4 Ω	822.9 Ω
Must operate voltage	75% of rated voltage (max.)			
Must release voltage	10% of rated voltage (min.)			
Max. voltage	120% of rated voltage at 85°C, 150% of rated voltage at 23°C			
Power consumption	Approx. 700 mW			

Note: The rated current and coil resistance are measured at a coil temperature of 23°C with a tolerance of ±10%.

400-mW Type (G5LE-E)

Rated voltage	5 VDC	12 VDC	24 VDC
Rated current	80.0 mA	33.3 mA	16.7 mA
Coil resistance	62.5 Ω	360.0 Ω	1440.0 Ω
Must operate voltage	75% of rated voltage (max.)		
Must release voltage	10% of rated voltage (min.)		
Max. voltage	130% of rated voltage at 85°C, 170% of rated voltage at 23°C		
Power consumption	Approx. 400 mW		

Note: The rated current and coil resistance are measured at a coil temperature of 23°C with a tolerance of ±10%.

360-mW Type (G5LE-E-36)

Rated voltage	5 VDC	12 VDC	24 VDC
Rated current	72.0 mA	30.0 mA	15.0 mA
Coil resistance	69.4 Ω	400.0 Ω	1600.0 Ω
Must operate voltage	75% of rated voltage (max.)		
Must release voltage	10% of rated voltage (min.)		
Max. voltage	130% of rated voltage at 85°C, 170% of rated voltage at 23°C		
Power consumption	Approx. 360 mW		

Note: The rated current and coil resistance are measured at a coil temperature of 23°C with a tolerance of ±10%.

■ Contact Ratings

Item	G5LE-G	G5LE-E/-E-36
Load	Resistive load (cos Ø=1)	Resistive load (cos Ø=1)
Rated load	10A at 35VDC	16A at 250VAC
Rated carry current	10A	16A
Max. switching voltage	35VDC	250VAC
Max. switching current	DC : 10A	AC : 16A
Max. switching capacity	350W	4000VA
Min. permissible load	100mA at 5VDC	100mA at 5VDC

■ Characteristics

Contact resistance	100mΩ max.
Operate time	10ms max.
Release time	5ms max.
Bounce time	Operate : Approx. 0.6 ms Release : Approx. 7.2 ms
Max. switching frequency	Mechanical : 18,000 operations/hr Electrical : *1,800 operations/hr
Insulation resistance	100MΩ min. (at 500VDC)
Dielectric strength	750VAC (for suffix -E), 50/60 Hz for 1 min. between contacts of same polarity 1500VAC (for suffix -G), 50/60 Hz for 1 min. between contacts of same polarity 2,000VAC, 50/60 Hz for 1 min. between coil and contacts
Impulse withstand voltage	4,500V between coil and contacts, 1.2 X 50 μsec
Vibration resistance	Destruction : 10 to 55Hz, 1.5mm double amplitude Malfunction : 10 to 55hHz, 1.5mm double amplitude
Shock resistance	Destruction : 1,000m/s^2 (approx. 100G) Malfunction : 100m/s^2 (approx. 10G)
Life expectancy	Mechanical : 10,000,000 operations min. (at 18,000 operations/hr) Electrical : *100,000 operations min. (at 1,800 operations/hr, 12A 250VAC)
Ambient temperature	Operating : -40°C to 85°C
Ambient humidity	Operating : 35% to 85%
Weight	Approx. : 12g

Note : * Applicable for G5LE-1-E normally open contact only.

■ Approved Standards

UL508, UL114, UL478, UL325, UL873, UL1409 (File No. E41643)/CSA C22.2 No. 14, No. 1 (File No. LR31928)

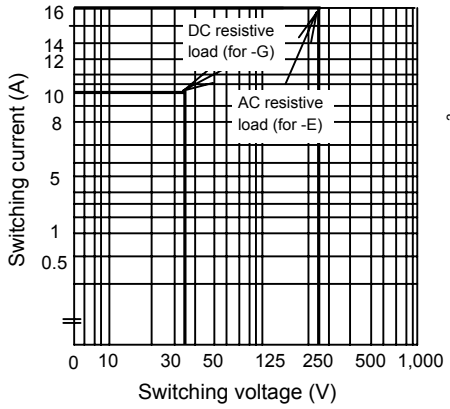
Model	Coil ratings	Contact ratings
G5LE-E/-E-36	5 to 24 VDC	16 A, 250 VAC (general use, normally open contact, 50,000 cycles) 12 A, 250 VAC (general use, normally open contact, 105°C, 100,000 cycles) 12 A, 250 VAC (general use, normally close contact, 30,000 cycles)
G5LE-G	9 to 24 VDC	10 A, 35 VDC (resistive, normally open contact, 100,000 cycles) 10 A, 35 VDC (resistive, normally close contact, 50,000 cycles)

EN61810-1 (2nd Ed) / EN60255-25 (VDE Reg. No. 6850)

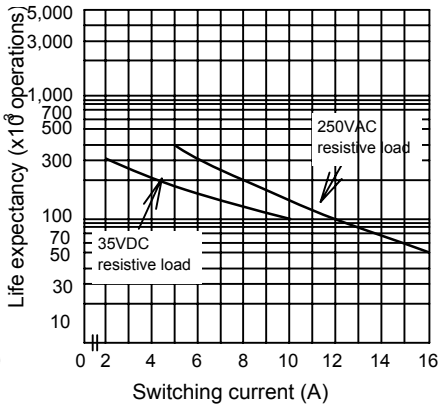
Model	Coil Rating	Contact rating
G5LE-E/-E-36	5 to 24 VDC	16 A, 250 VAC (resistive, normally open contact, 85°C 50,000 cycles) 12 A, 250 VAC (resistive, normally open contact, 105°C, 75,000 cycles)
G5LE-G	9 to 24 VDC	10 A, 35 VDC (resistive, normally open contact, 100,000 cycles) 10 A, 35 VDC (resistive, normally close contact, 50,000 cycles)

Engineering Data

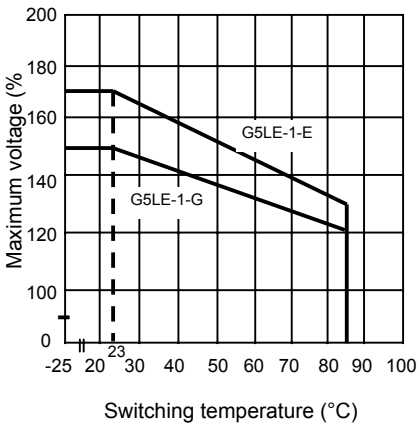
Max. Switching Capacity



Life Expectancy



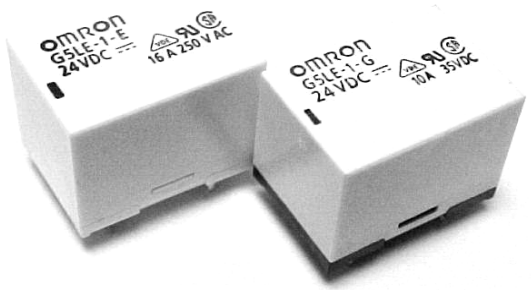
Ambient Temp. Vs Max. Voltage

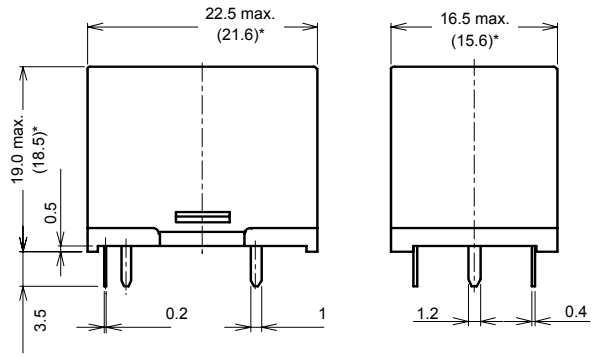


Note: The maximum coil voltage refers to the maximum value in a varyin range of operating power voltage not a continuous voltage

Dimensions

Note: 1. All units are in millimeters unless otherwise indicated.
2. Orientation marks are indicated as follows :

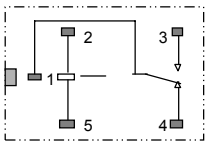




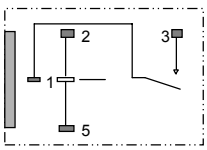
*Average value

Terminal Arrangenement/Internal Connections (Bottom View)

SPDT

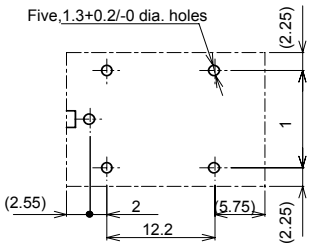


SPST-NO

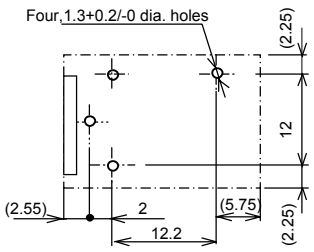


Mounting Holes (Bottom View)
Tolerance: ±0.1 mm unless specified

SPDT



SPST-NO



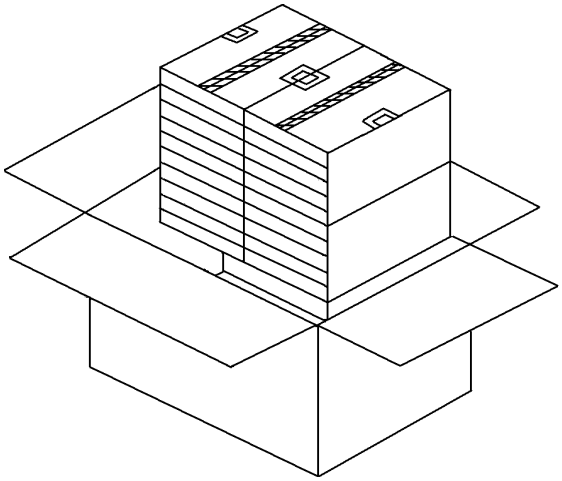
Packaging

Note : 1. All units are millimeters unless otherwise indicated.

■ Polystyrene Trays Packing

1 Polystyrene	=	100	pcs relay
1 Sleeve Packing	=	5	polystyrene tray
1 Carton	=	4	sleeve packing
	=	**2000**	**pcs relay**
Weight	=	Approx. 24 Kg per carton	

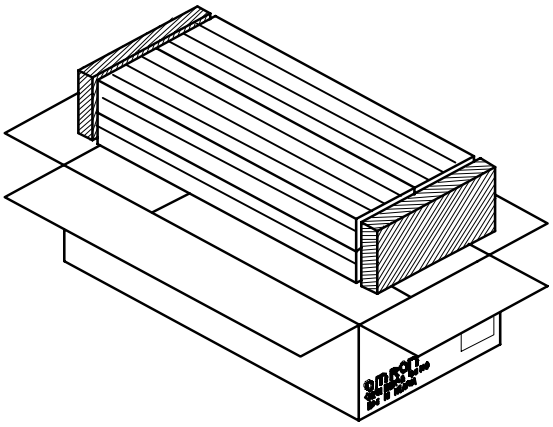
- Size of polystyrene tray: Approx. 311 x 196 x 35mm (L x W xH)
- Size of Carton: Approx. 450 x 316 x 320 mm (L x W xH)



■ Tube Packing

1 Tube	=	25	relays
1 Carton	=	40	tubes
	=	1,000	relays
Weight	=	Approx. 12 Kg per carton	

- Size of Carton: Approx. 512 x 252 x 105 mm (L x W xH)



■ Ordering Information - Packaging

G5LE-1-E-□ DC12 by OMB

KEY		DESCRIPTION
None	:	Standards Polystyrene tray
SP	:	Anti-static Tube packing

G5LE-1-G-□DC20 by OMB

KEY		DESCRIPTION
None	:	Standards Polystyrene tray
SP	:	Anti-static Tube packing

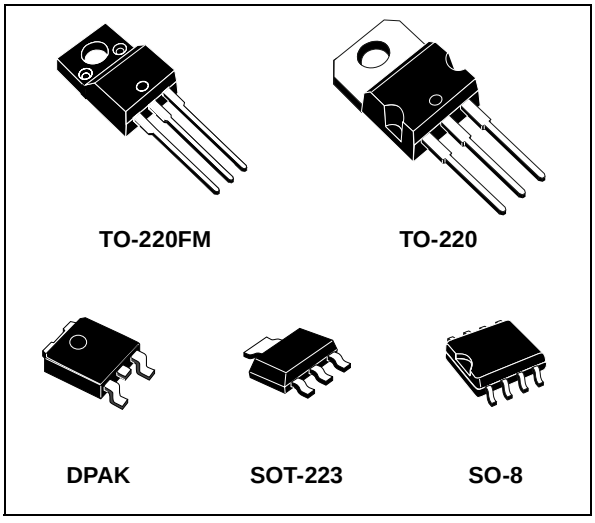
ALL DIMENSION SHOWN ARE IN MILLIMETERS

To convert into inches, multiply by 0.03937, To convert grams into ounces, multiply by 0.03527

LD1117 SERIES

LOW DROP FIXED AND ADJUSTABLE POSITIVE VOLTAGE REGULATORS

- LOW DROPOUT VOLTAGE (1V TYP.)
- 2.85V DEVICE PERFORMANCES ARE SUITABLE FOR SCSI-2 ACTIVE TERMINATION
- OUTPUT CURRENT UP TO 800 mA
- FIXED OUTPUT VOLTAGE OF: 1.2V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- ADJUSTABLE VERSION AVAILABILITY (V_{rel}=1.25V)
- INTERNAL CURRENT AND THERMAL LIMIT
- AVAILABLE IN ± 1% (AT 25°C) AND 2% IN FULL TEMPERATURE RANGE
- SUPPLY VOLTAGE REJECTION: 75dB (TYP.)



DESCRIPTION

The LD1117 is a LOW DROP Voltage Regulator able to provide up to 800mA of Output Current, available even in adjustable version (Vref=1.25V). Concerning fixed versions, are offered the following Output Voltages: 1.2V,1.8V,2.5V,2.85V, 3.0V 3.3V and 5.0V. The 2.85V type is ideal for SCSI-2 lines active termination. The device is supplied in: SOT-223, DPAK, SO-8, TO-220 and TO-220FM. The SOT-223 and DPAK surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. In fact in this case, unlike than PNP one, the Quiescent Current flows mostly into the load. Only a very common 10µF minimum capacitor is needed for stability. On chip trimming allows the regulator to reach a very tight output voltage tolerance, within ± 1% at 25°C. The ADJUSTABLE LD1117 is pin to pin compatible with the other standard. Adjustable voltage regulators maintaining the better performances in terms of Drop and Tolerance.

Figure 1: Block Diagram

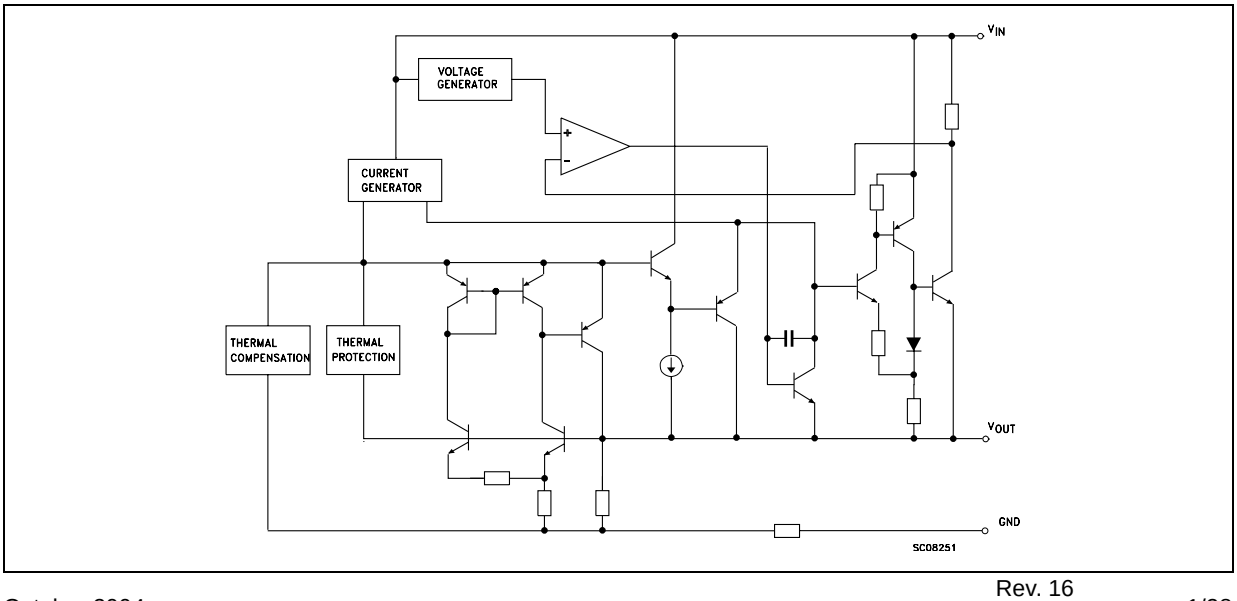
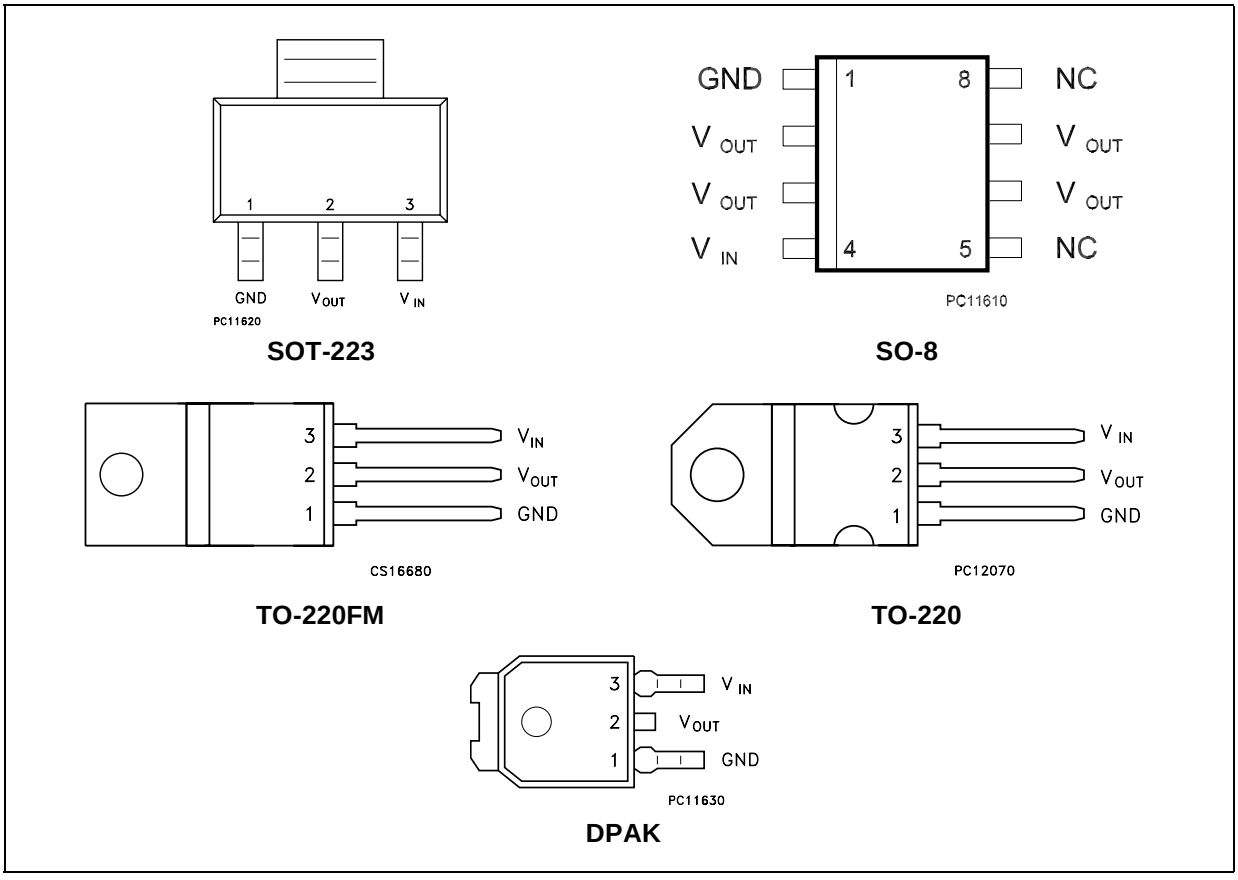


Figure 2: Pin Connection (top view)



NOTE: The TAB is connected to the V_{OUT}.

Table 1: Order Codes

SOT-223	SO-8	DPAK	TO-220	TO-220FM	OUTPUT VOLTAGE
LD1117S12	LD1117D12 (*)	LD1117DT12	LD1117V12 (*)	LD1117F12 (*)	1.2 V
LD1117S12C (*)	LD1117D12C (*)	LD1117DT12C	LD1117V12C (*)	LD1117F12C (*)	1.2 V
LD1117S18	LD1117D18	LD1117DT18	LD1117V18	LD1117F18	1.8 V
LD1117S18C	LD1117D18C	LD1117DT18C	LD1117V18C	LD1117F18C	1.8 V
LD1117S25	LD1117D25	LD1117DT25	LD1117V25	LD1117F25	2.5 V
LD1117S25C	LD1117D25C	LD1117DT25C	LD1117V25C	LD1117F25C	2.5 V
LD1117S28	LD1117D28	LD1117DT28	LD1117V28	LD1117F28	2.85 V
LD1117S30	LD1117D30	LD1117DT30	LD1117V30	LD1117F30	3 V
LD1117S30C	LD1117D30C	LD1117DT30C	LD1117V30C	LD1117F30C	3 V
LD1117S33	LD1117D33	LD1117DT33	LD1117V33	LD1117F33	3.3 V
LD1117S33C	LD1117D33C	LD1117DT33C	LD1117V33C	LD1117F33C	3.3 V
LD1117S50	LD1117D50	LD1117DT50	LD1117V50	LD1117F50	5 V
LD1117S50C	LD1117D50C	LD1117DT50C	LD1117V50C	LD1117F50C	5 V
LD1117S	LD1117D	LD1117DT	LD1117V	LD1117F	ADJ FROM 1.25 TO 15V
LD1117SC	LD1117DC	LD1117DTC	LD1117VC	LD1117FC	ADJ FROM 1.25 TO 15V

(*) Available on request

Table 2: Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{IN}	DC Input Voltage		15	V
P_{tot}	Power Dissipation		12	W
T_{stg}	Storage Temperature Range		-40 to +150	°C
T_{op}	Operating Junction Temperature Range	for C Version	-40 to +125	°C
		for standard Version	0 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied. Over the above suggested Max Power Dissipation a Short Circuit could definitively damage the device.

Table 3: Thermal Data

Symbol	Parameter	SOT-223	SO-8	DPAK	TO-220	TO-220FM	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	15	20	8	3	4	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient				50	60	°C/W

Figure 3: Application Circuit (FOR 1.2 V)

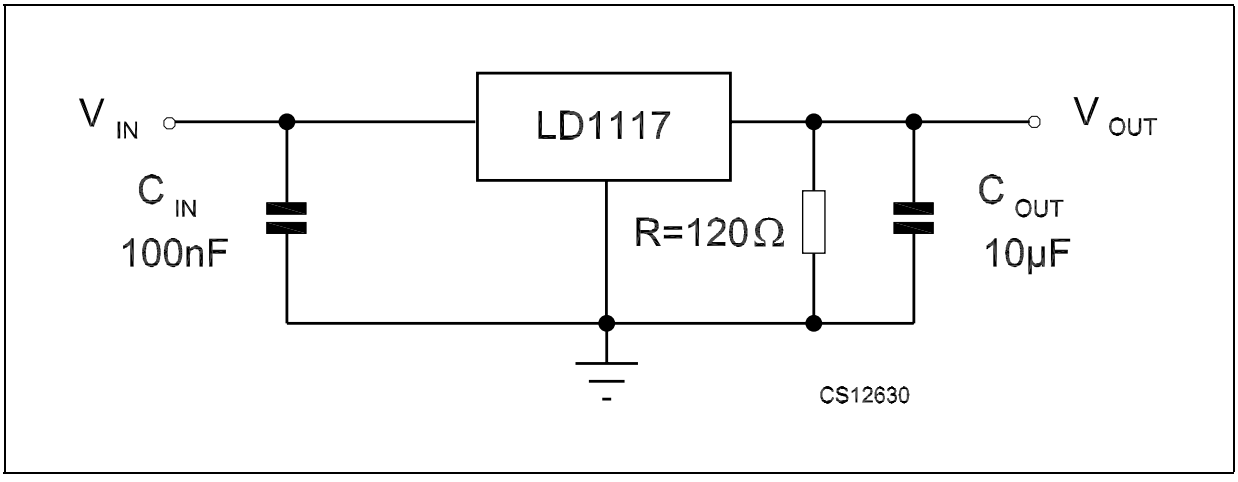


Figure 4: Application Circuit (FOR OTHER FIXED OUTPUT VOLTAGES)

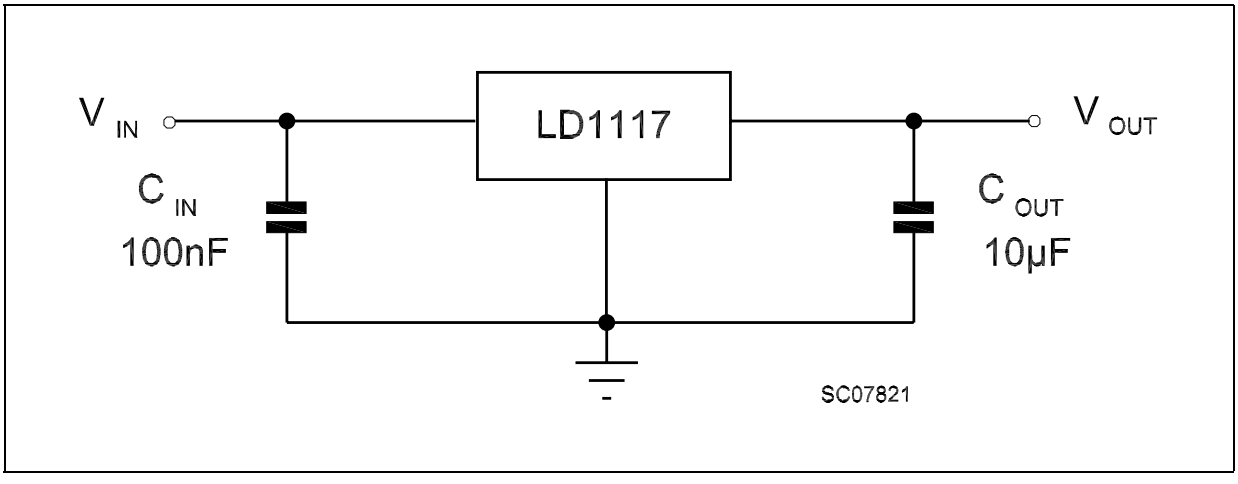


Table 4: Electrical Characteristics Of LD1117#12 (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, R = 120 Ω between GND and OUT pins, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 3.2 V I_O = 10 mA T_J = 25°C	1.188	1.20	1.212	V
V_O	Reference Voltage	I_O = 10 to 800 mA V_{in} - V_O= 1.4 to 10 V	1.140	1.20	1.260	V
ΔV_O	Line Regulation	V_{in} - V_O = 1.5 to 13.75 V I_O = 10 mA		0.035	0.2	%
ΔV_O	Load Regulation	V_{in} - V_O = 3 V I_O = 10 to 800 mA		0.1	0.4	%
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage				15	V
I_{adj}	Adjustment Pin Current	$V_{in} \leq$ 15 V		60	120	µA
ΔI_{adj}	Adjustment Pin Current Change	V_{in} - V_O = 1.4 to 10 V I_O = 10 to 800 mA		1	5	µA
$I_{O(min)}$	Minimum Load Current	V_{in} = 15 V		2	5	mA
I_O	Output Current	V_{in} - V_O = 5 V T_J = 25°C	800	950	1300	mA
eN	Output Noise (%V_O)	B =10Hz to 10KHz T_J = 25°C		0.003		%
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} - V_O = 3 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 5: Electrical Characteristics Of LD1117#18 (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 3.8 V I_O = 10 mA T_J = 25°C	1.78	1.8	1.82	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 3.3 to 8 V	1.76		1.84	V
ΔV_O	Line Regulation	V_{in} = 3.3 to 8 V I_O = 0 mA		1	6	mV
ΔV_O	Load Regulation	V_{in} = 3.3 V I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			10	V
I_d	Quiescent Current	$V_{in} \leq$ 8 V		5	10	mA
I_O	Output Current	V_{in} = 6.8 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 5.5 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 6: Electrical Characteristics Of LD1117#25 (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 4.5 V I_O = 10 mA T_J = 25°C	2.475	2.5	2.525	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 3.9 to 10 V	2.45		2.55	V
ΔV_O	Line Regulation	V_{in} = 3.9 to 10 V I_O = 0 mA		1	6	mV
ΔV_O	Load Regulation	V_{in} = 3.9 V I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 10 V		5	10	mA
I_O	Output Current	V_{in} = 7.5 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 5.5 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 7: Electrical Characteristics Of LD1117#28 (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 4.85 VI_O = 10 mA T_J = 25°C	2.82	2.85	2.88	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 4.25 to 10 V	2.79		2.91	V
ΔV_O	Line Regulation	V_{in} = 4.25 to 10 V I_O = 0 mA		1	6	mV
ΔV_O	Load Regulation	V_{in} = 4.25 V I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 10 V		5	10	mA
I_O	Output Current	V_{in} = 7.85 VT_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 5.85 VV_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 8: Electrical Characteristics Of LD1117#30 (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 5 V I_O = 10 mA T_J = 25°C	2.97	3	3.03	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 4.5 to 10 V	2.94		3.06	V
ΔV_O	Line Regulation	V_{in} = 4.5 to 12 V I_O = 0 mA		1	6	mV
ΔV_O	Load Regulation	V_{in} = 4.5 V I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 12 V		5	10	mA
I_O	Output Current	V_{in} = 8 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 6 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 9: Electrical Characteristics Of LD1117#33 (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 5.3 V I_O = 10 mA T_J = 25°C	3.267	3.3	3.333	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 4.75 to 10 V	3.235		3.365	V
ΔV_O	Line Regulation	V_{in} = 4.75 to 15 V I_O = 0 mA		1	6	mV
ΔV_O	Load Regulation	V_{in} = 4.75 V I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 15 V		5	10	mA
I_O	Output Current	V_{in} = 8.3 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 6.3 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 10: Electrical Characteristics Of LD1117#50 (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 7 V I_O = 10 mA T_J = 25°C	4.95	5	5.05	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 6.5 to 15 V	4.9		5.1	V
ΔV_O	Line Regulation	V_{in} = 6.5 to 15 V I_O = 0 mA		1	10	mV
ΔV_O	Load Regulation	V_{in} = 6.5 V I_O = 0 to 800 mA		1	15	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 15 V		5	10	mA
I_O	Output Current	V_{in} = 10 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 8 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 11: Electrical Characteristics Of LD1117 (ADJUSTABLE) (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ref}	Reference Voltage	V_{in} - V_O = 2 V I_O = 10 mA T_J = 25°C	1.238	1.25	1.262	V
V_{ref}	Reference Voltage	I_O = 10 to 800 mA V_{in} - V_O= 1.4 to 10 V	1.225		1.275	V
ΔV_O	Line Regulation	V_{in} - V_O = 1.5 to 13.75 V I_O = 10 mA		0.035	0.2	%
ΔV_O	Load Regulation	V_{in} - V_O = 3 V I_O = 10 to 800 mA		0.1	0.4	%
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage				15	V
I_{adj}	Adjustment Pin Current	$V_{in} \leq$ 15 V		60	120	µA
ΔI_{adj}	Adjustment Pin Current Change	V_{in} - V_O = 1.4 to 10 V I_O = 10 to 800 mA		1	5	µA
$I_{O(min)}$	Minimum Load Current	V_{in} = 15 V		2	5	mA
I_O	Output Current	V_{in} - V_O = 5 V T_J = 25°C	800	950	1300	mA
eN	Output Noise (%V_O)	B =10Hz to 10KHz T_J = 25°C		0.003		%
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} - V_O = 3 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 12: Electrical Characteristics Of LD1117#12C (refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, R = 120 Ω between GND and OUT pins, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ref}	Reference Voltage	V_{in} - V_O= 2V I_O = 10 mA T_J = 25°C	1.176	1.20	1.224	V
V_{ref}	Reference Voltage	I_O = 10 to 800 mA V_{in} - V_O= 1.4 to 10 V	1.120	1.20	1.280	V
ΔV_O	Line Regulation	V_{in} - V_O = 1.5 to 13.75 V I_O = 10 mA			1	%
ΔV_O	Load Regulation	V_{in} - V_O = 3 V I_O = 10 to 800 mA			1	%
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage				15	V
I_{adj}	Adjustment Pin Current	$V_{in} \leq$ 15 V		60	120	µA
ΔI_{adj}	Adjustment Pin Current Change	V_{in} - V_O = 1.4 to 10 V I_O = 10 to 800 mA		1	5	µA
$I_{O(min)}$	Minimum Load Current	V_{in} = 15 V		2	5	mA
I_O	Output Current	V_{in} - V_O = 5 V T_J = 25°C	800	950	1300	mA
eN	Output Noise (%V_O)	B =10Hz to 10KHz T_J = 25°C		0.003		%
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} - V_O = 3 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA T_J = 0 to 125°C		1.05	1.2	
		I_O = 800 mA T_J = 0 to 125°C		1.10	1.3	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 13: Electrical Characteristics Of LD1117#18C (refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 3.8 V I_O = 10 mA T_J = 25°C	1.76	1.8	1.84	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 3.9 to 10 V	1.73		1.87	V
ΔV_O	Line Regulation	V_{in} = 3.3 to 8 V I_O = 0 mA		1	30	mV
ΔV_O	Load Regulation	V_{in} = 3.3 V I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			10	V
I_d	Quiescent Current	$V_{in} \leq$ 8 V		5	10	mA
I_O	Output Current	V_{in} = 6.8 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 5.5 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout Voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 14: Electrical Characteristics Of LD1117#25C (refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 4.5 V I_O = 10 mA T_J = 25°C	2.45	2.5	2.55	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 3.9 to 10 V	2.4		2.6	V
ΔV_O	Line Regulation	V_{in} = 3.9 to 10 V I_O = 0 mA		1	30	mV
ΔV_O	Load Regulation	V_{in} = 3.9 V I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 10 V		5	10	mA
I_O	Output Current	V_{in} = 7.5 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 5.5 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout Voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 15: Electrical Characteristics Of LD1117#30C (refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 5 V I_O = 10 mA T_J = 25°C	2.94	3	3.06	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 4.5 to 10 V	2.88		3.12	V
ΔV_O	Line Regulation	V_{in} = 4.5 to 12 V I_O = 0 mA		1	30	mV
ΔV_O	Load Regulation	V_{in} = 4.5 V I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 12 V		5	10	mA
I_O	Output Current	V_{in} = 8 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 6 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout Voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 16: Electrical Characteristics Of LD1117#33C (refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 5.3 V I_O = 10 mA T_J = 25°C	3.24	3.3	3.36	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 4.75 to 10 V	3.16		3.44	V
ΔV_O	Line Regulation	V_{in} = 4.75 to 15 V I_O = 0 mA		1	30	mV
ΔV_O	Load Regulation	V_{in} = 4.75 V I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 15 V		5	10	mA
I_O	Output Current	V_{in} = 8.3 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 6.3 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout Voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 17: Electrical Characteristics Of LD1117#50C (refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	V_{in} = 7 V I_O = 10 mA T_J = 25°C	4.9	5	5.1	V
V_O	Output Voltage	I_O = 0 to 800 mA V_{in} = 6.5 to 15 V	4.8		5.2	V
ΔV_O	Line Regulation	V_{in} = 6.5 to 15 V I_O = 0 mA		1	50	mV
ΔV_O	Load Regulation	V_{in} = 6.5 V I_O = 0 to 800 mA		1	50	mV
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage	I_O = 100 mA			15	V
I_d	Quiescent Current	$V_{in} \leq$ 15 V		5	10	mA
I_O	Output Current	V_{in} = 10 V T_J = 25°C	800	950	1300	mA
eN	Output Noise Voltage	B =10Hz to 10KHz T_J = 25°C		100		µV
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} = 8 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout Voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

Table 18: Electrical Characteristics Of LD1117C (ADJUSTABLE) (refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ref}	Reference Voltage	V_{in} - V_O = 2 V I_O = 10 mA T_J = 25°C	1.225	1.25	1.275	V
V_{ref}	Reference Voltage	I_O = 10 to 800 mA V_{in} - V_O= 1.4 to 10 V	1.2		1.3	V
ΔV_O	Line Regulation	V_{in} - V_O = 1.5 to 13.75 V I_O = 10 mA			1	%
ΔV_O	Load Regulation	V_{in} - V_O = 3 V I_O = 10 to 800 mA			1	%
ΔV_O	Temperature Stability			0.5		%
ΔV_O	Long Term Stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating Input Voltage				15	V
I_{adj}	Adjustment Pin Current	$V_{in} \leq$ 15 V		60	120	µA
ΔI_{adj}	Adjustment Pin Current Change	V_{in} - V_O = 1.4 to 10 V I_O = 10 to 800 mA		1	10	µA
$I_{O(min)}$	Minimum Load Current	V_{in} = 15 V		2	5	mA
I_O	Output Current	V_{in} - V_O = 5 V T_J = 25°C	800	950	1300	mA
eN	Output Noise (%V_O)	B =10Hz to 10KHz T_J = 25°C		0.003		%
SVR	Supply Voltage Rejection	I_O = 40 mA f = 120Hz T_J = 25°C V_{in} - V_O = 3 V V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout Voltage	I_O = 100 mA T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout Voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal Regulation	T_a = 25°C 30ms Pulse		0.01	0.1	%/W

TYPICAL APPLICATIONS

Figure 5: Negative Supply

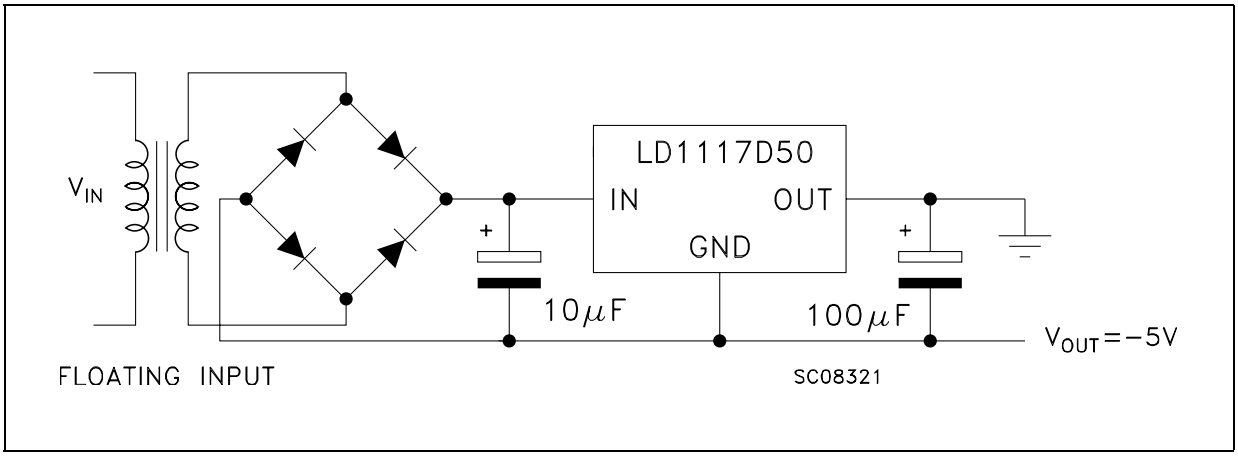


Figure 6: Active Terminator for SCSI-2 BUS

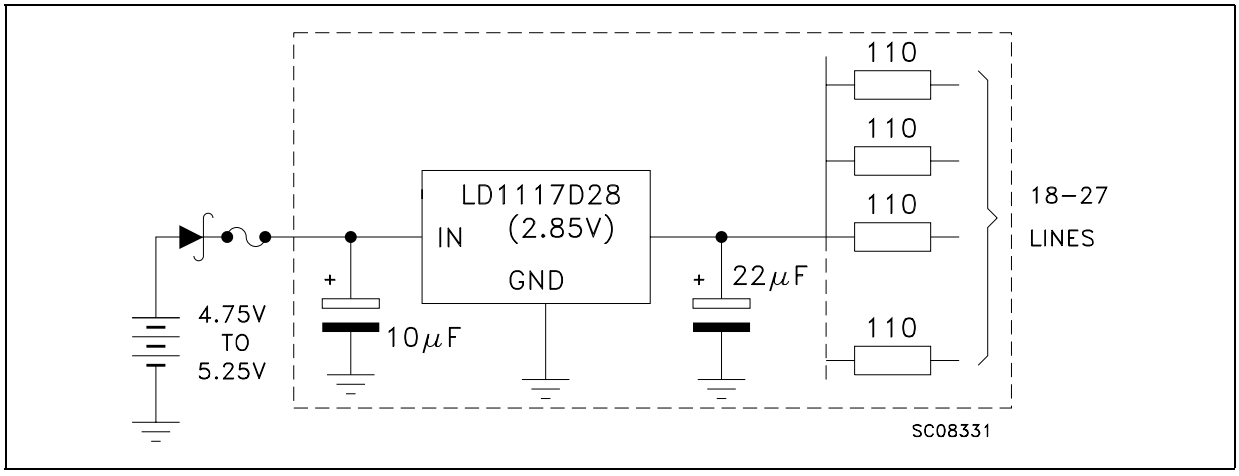


Figure 7: Circuit for Increasing Output Voltage

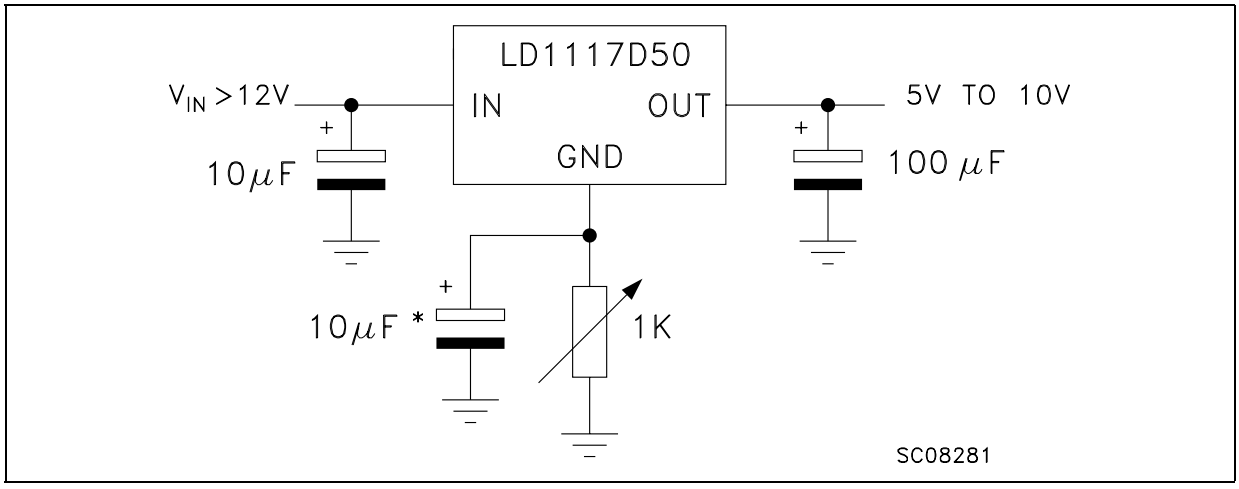


Figure 8: Voltage Regulator With Reference

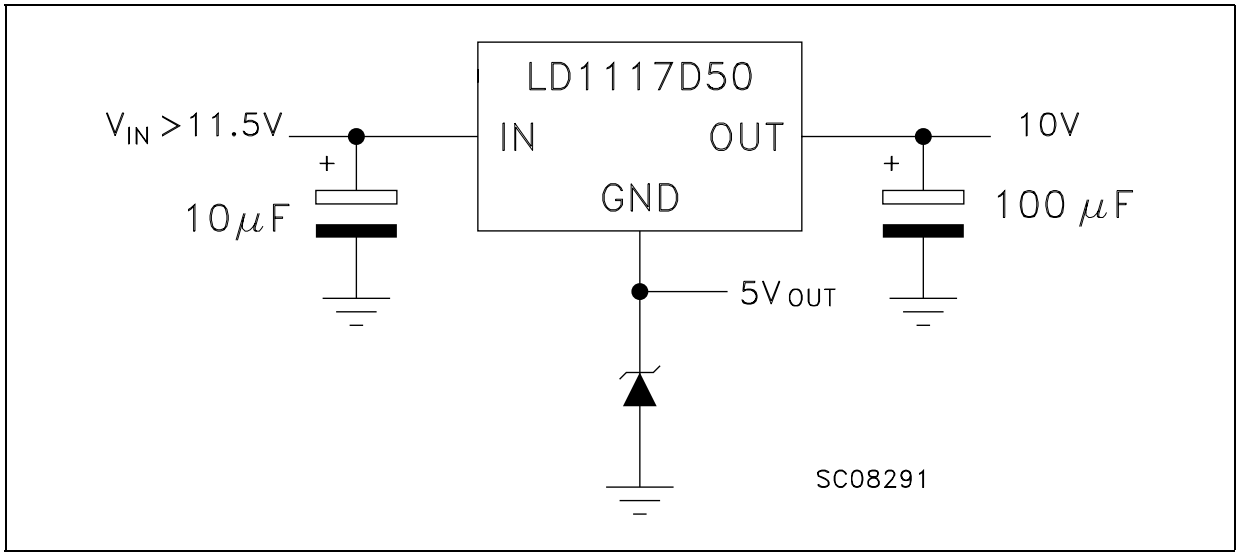


Figure 9: Battery Backed-up Regulated Supply

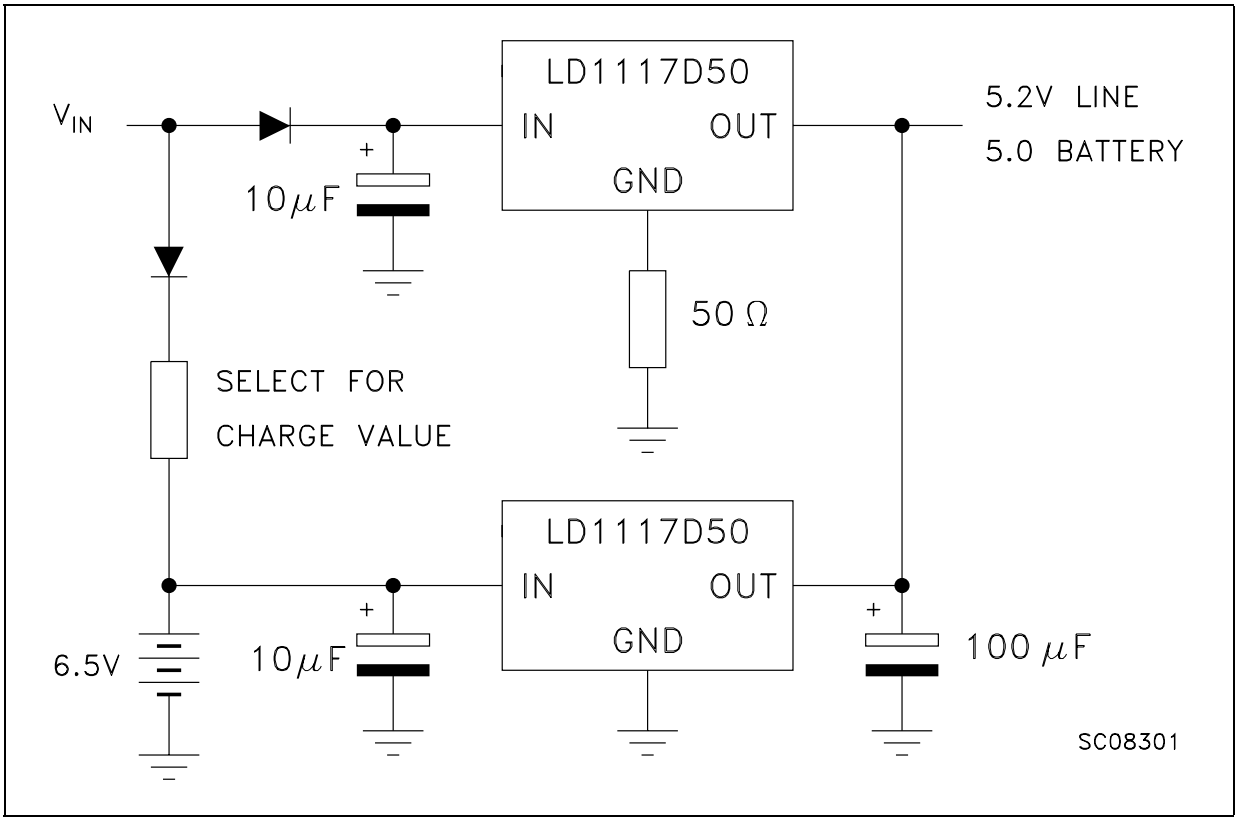
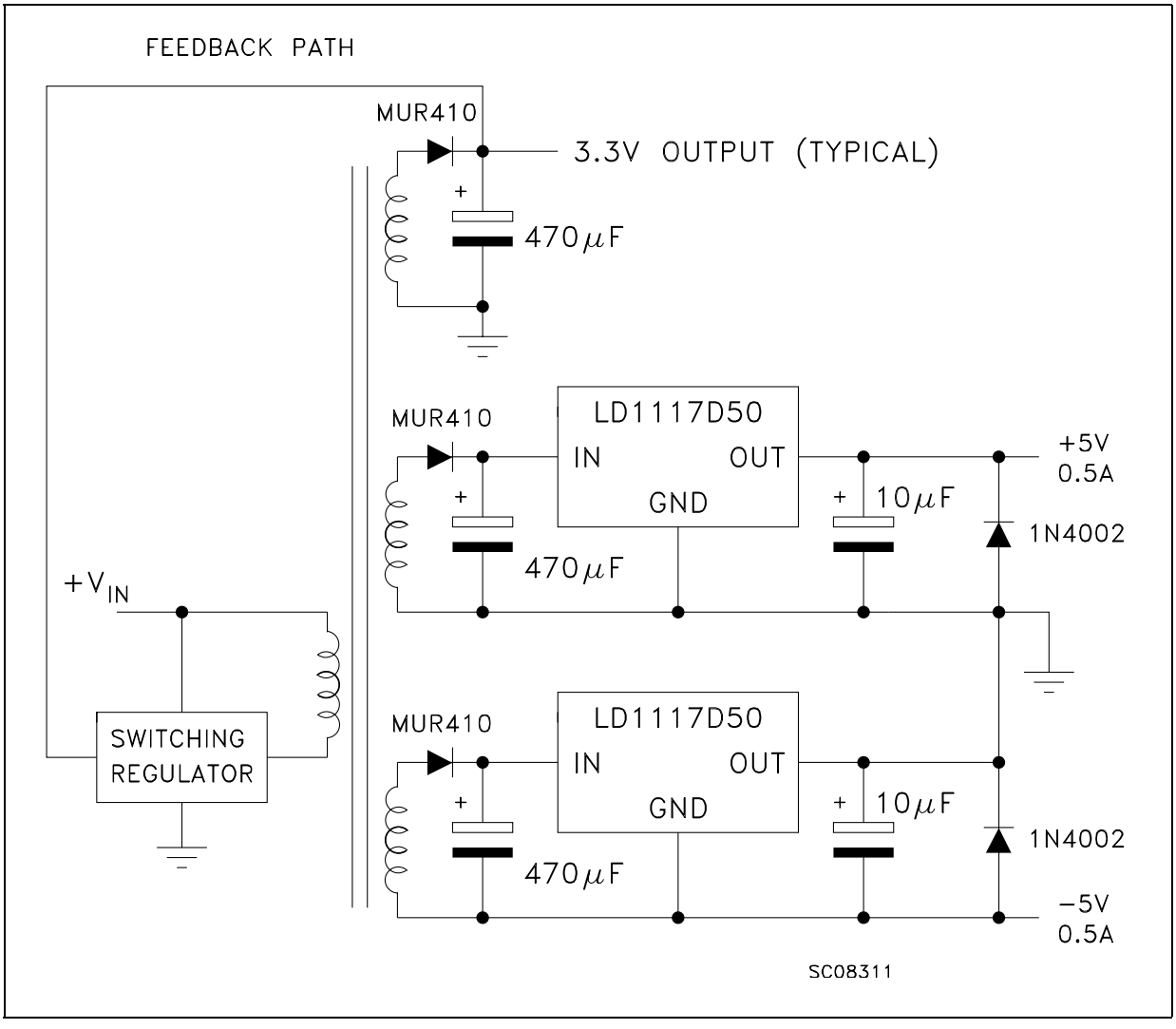


Figure 10: Post-Regulated Dual Supply



LD1117 ADJUSTABLE: APPLICATION NOTE

The LD1117 ADJUSTABLE has a thermal stabilized 1.25±0.012V reference voltage between the OUT and ADJ pins. I_{ADJ} is 60µA typ. (120µA max.) and ΔI_{ADJ} is 1µA typ. (5µA max.).
R1 is normally fixed to 120Ω. From figure 7 we obtain:
$V_{OUT} = V_{REF} + R2 (I_{ADJ} + I_{R1}) = V_{REF} + R2 (I_{ADJ} + V_{REF} / R1) = V_{REF} (1 + R2 / R1) + R2 \times I_{ADJ}$.
In normal application R2 value is in the range of few kohm, so the R2 x I_{DJ} product could not be considered in the V_{OUT} calculation; then the above expression becomes:

$V_{OUT} = V_{REF} (1 + R2 / R1)$.

In order to have the better load regulation it is important to realize a good Kelvin connection of R1 and R2 resistors. In particular R1 connection must be realized very close to OUT and ADJ pin, while R2 ground connection must be placed as near as possible to the negative Load pin. Ripple rejection can be improved by introducing a 10µF electrolytic capacitor placed in parallel to the R2 resistor (see Fig.8).

Figure 11: Adjustable Output Voltage Application

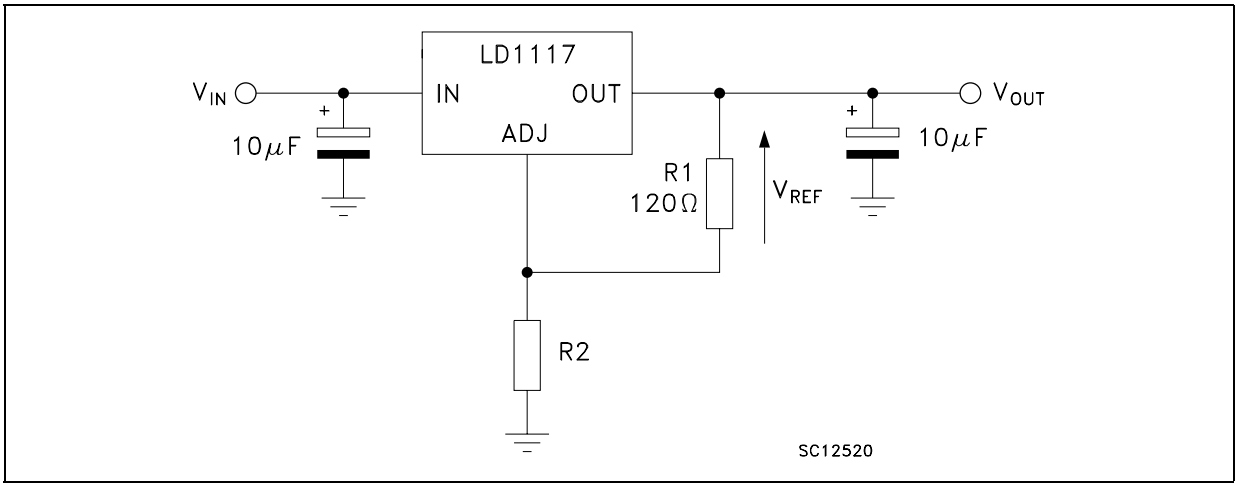
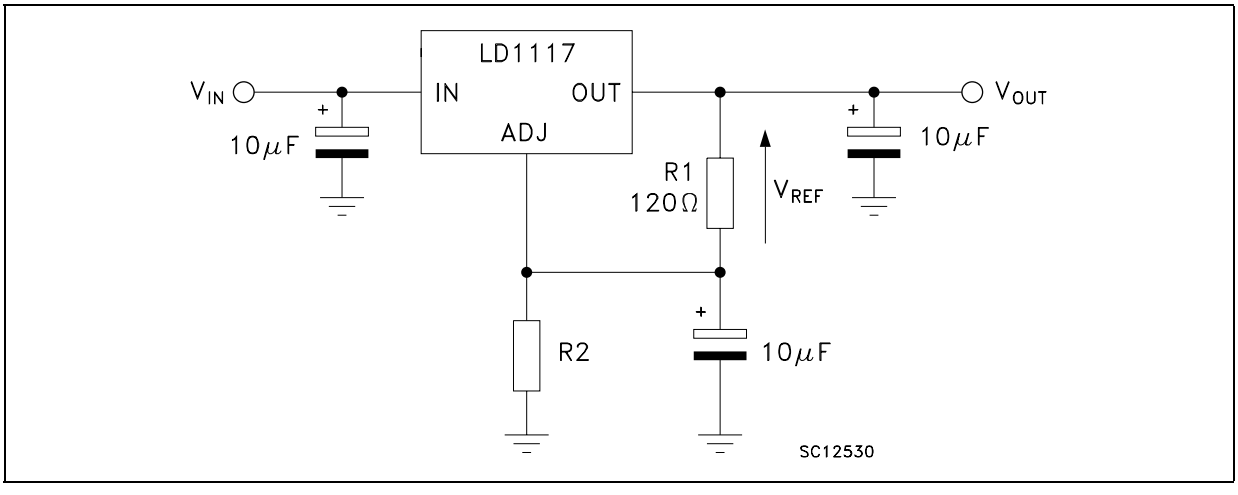
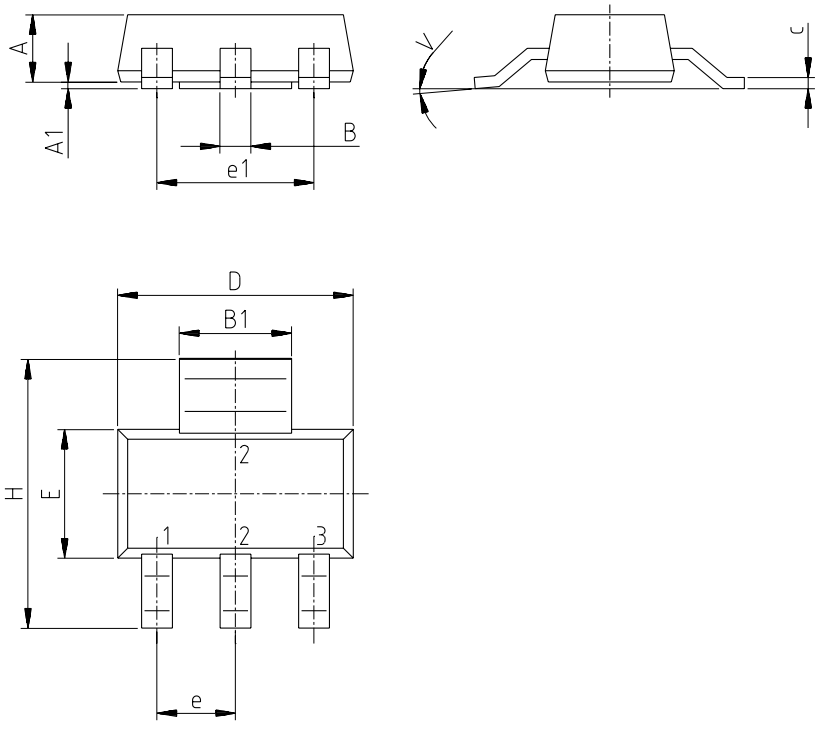


Figure 12: Adjustable Output Voltage Application with improved Ripple Rejection



SOT-223 MECHANICAL DATA

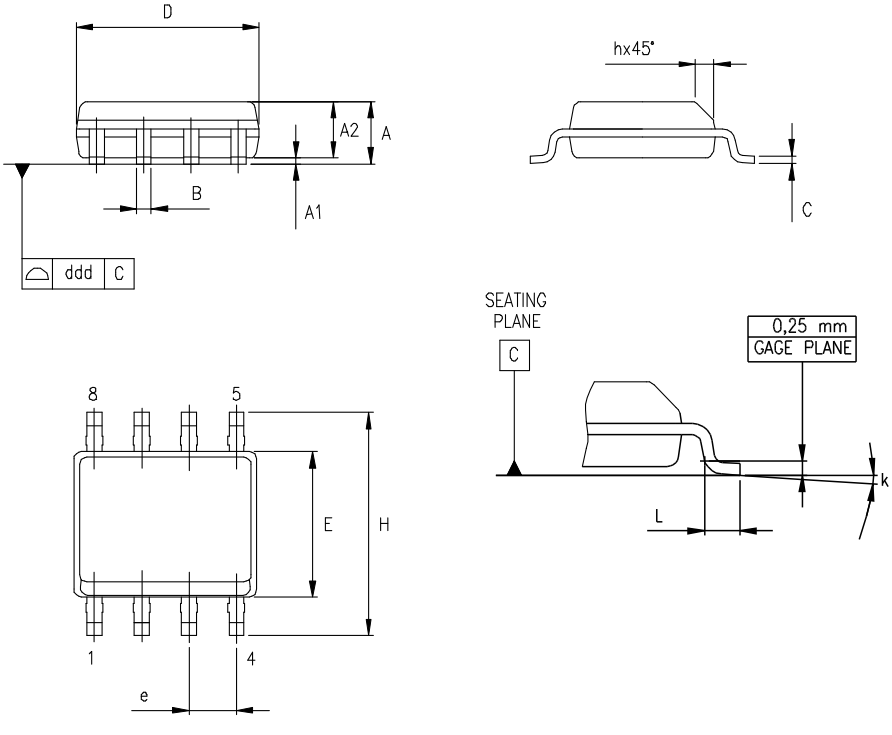
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.8			70.9
A1	0.02		0.1	0.8		3.9
B	0.6	0.7	0.85	23.6	27.6	33.5
B1	2.9	3	3.15	114.2	118.1	124.0
c	0.24	0.26	0.35	9.4	10.2	13.8
D	6.3	6.5	6.7	248.0	255.9	263.8
e		2.3			90.6	
e1		4.6			181.1	
E	3.3	3.5	3.7	129.9	137.8	145.7
H	6.7	7	7.3	129.9	137.8	145.7
V			10°			10°



0046067/H

SO-8 MECHANICAL DATA

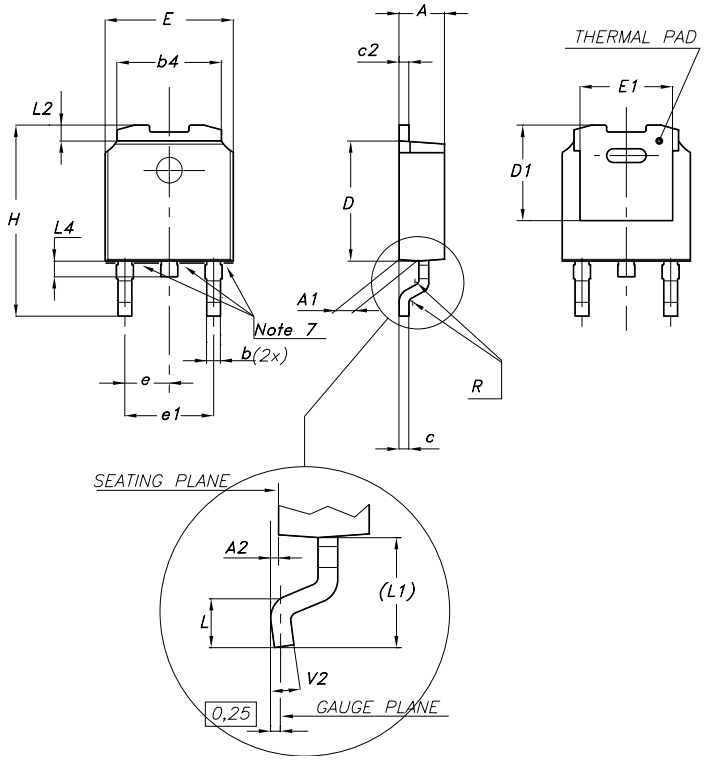
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

DPAK MECHANICAL DATA

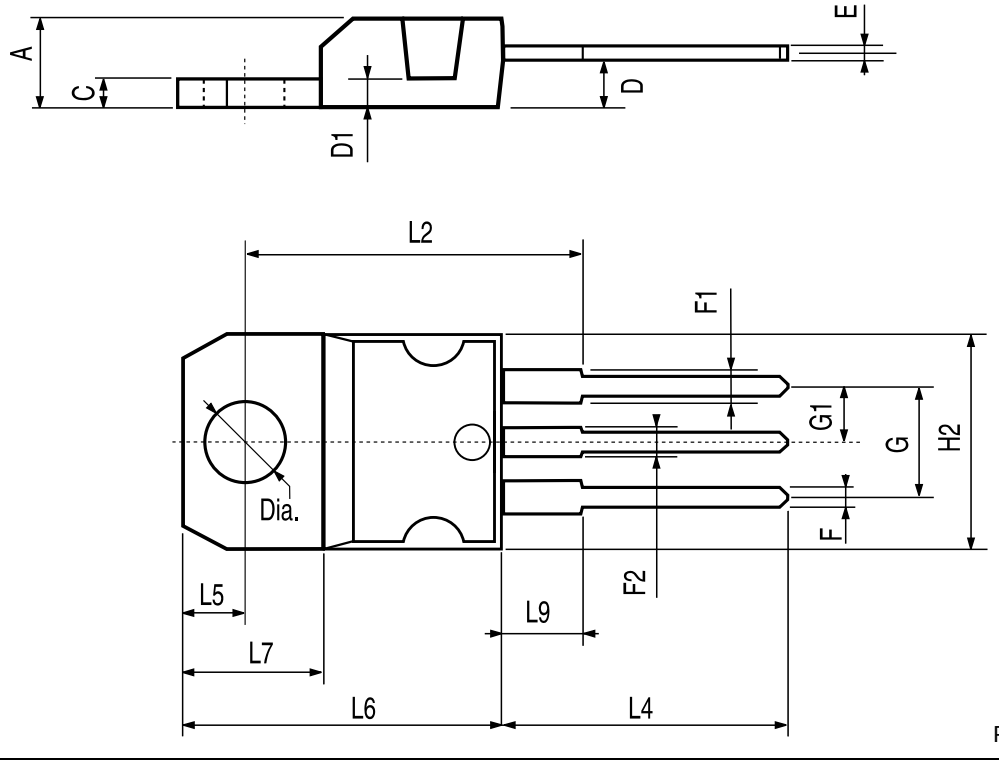
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



0068772-F

TO-220 MECHANICAL DATA

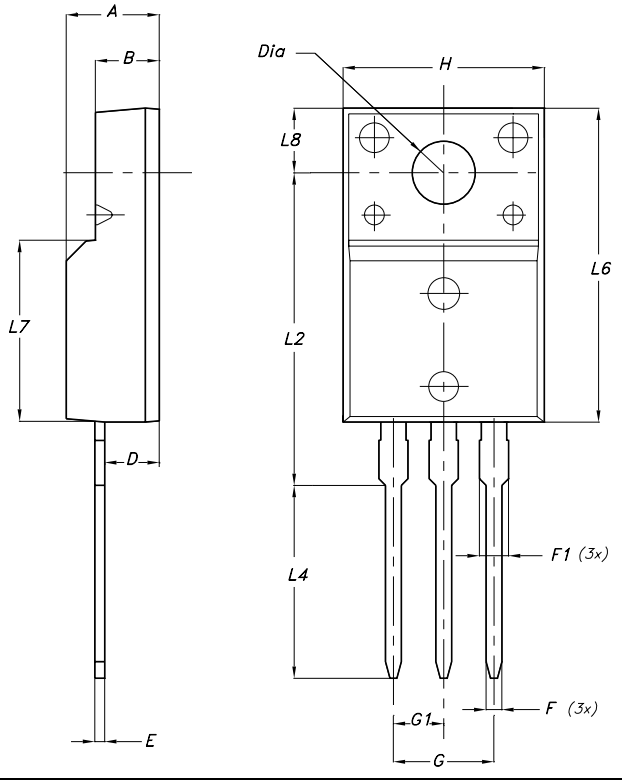
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



P011C

TO-220FM MECHANICAL DATA

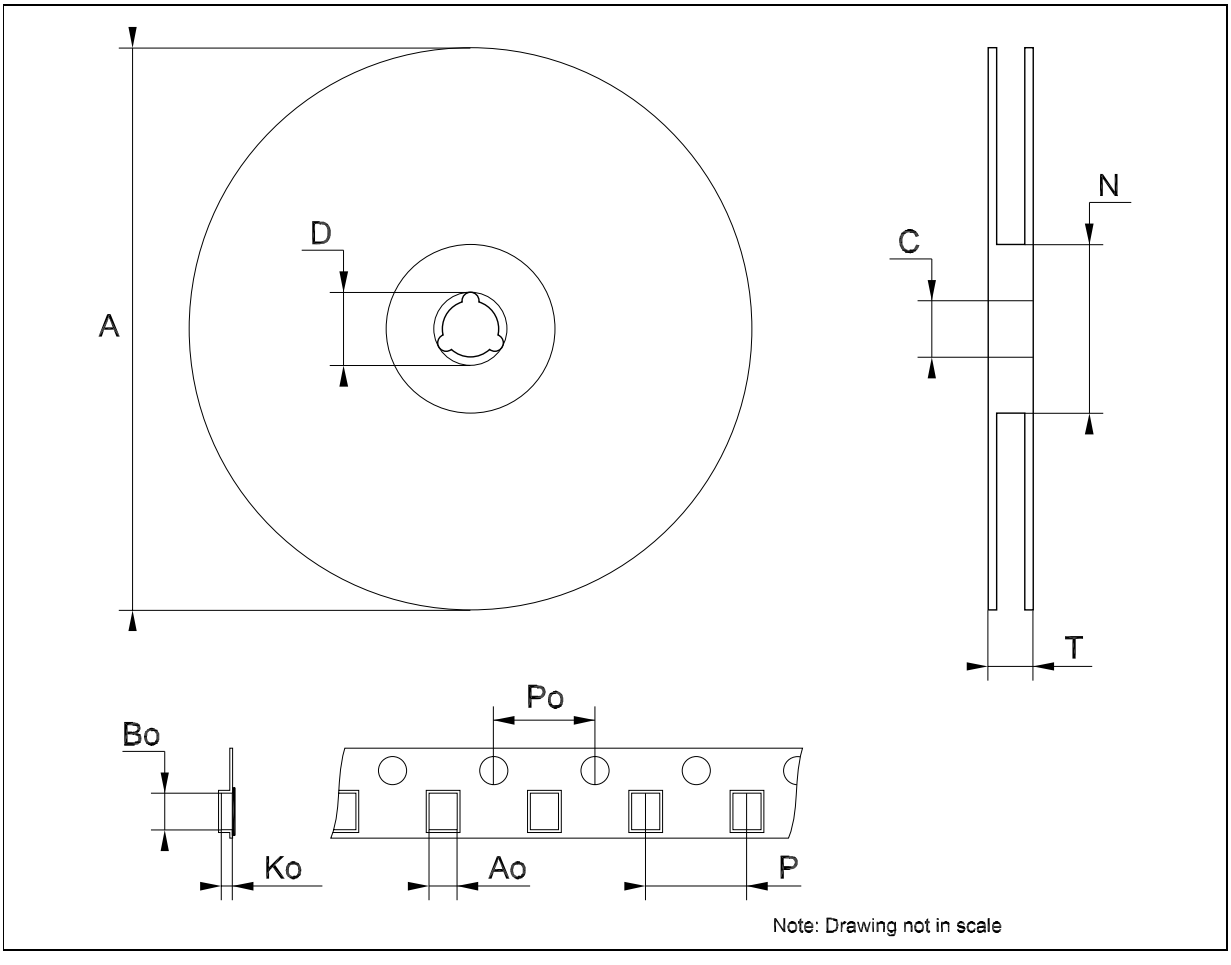
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.50		4.90	0.177		0.193
B	2.34		2.74	0.092		0.108
D	2.56		2.96	0.101		0.117
E	0.45	0.50	0.60	0.018	0.020	0.024
F	0.70		0.90	0.028		0.035
F1			1.47			0.058
G		5.08			0.200	
G1	2.34	2.54	2.74	0.092	0.100	0.108
H	9.96		10.36	0.392		0.408
L2		15.8			0.622	
L4	9.45		10.05	0.372		0.396
L6	15.67		16.07	0.617		0.633
L7	8.99		9.39	0.354		0.370
L8		3.30			0.130	
DIA.	3.08		3.28	0.121		0.129



7012510C-H

Tape & Reel SOT223 MECHANICAL DATA

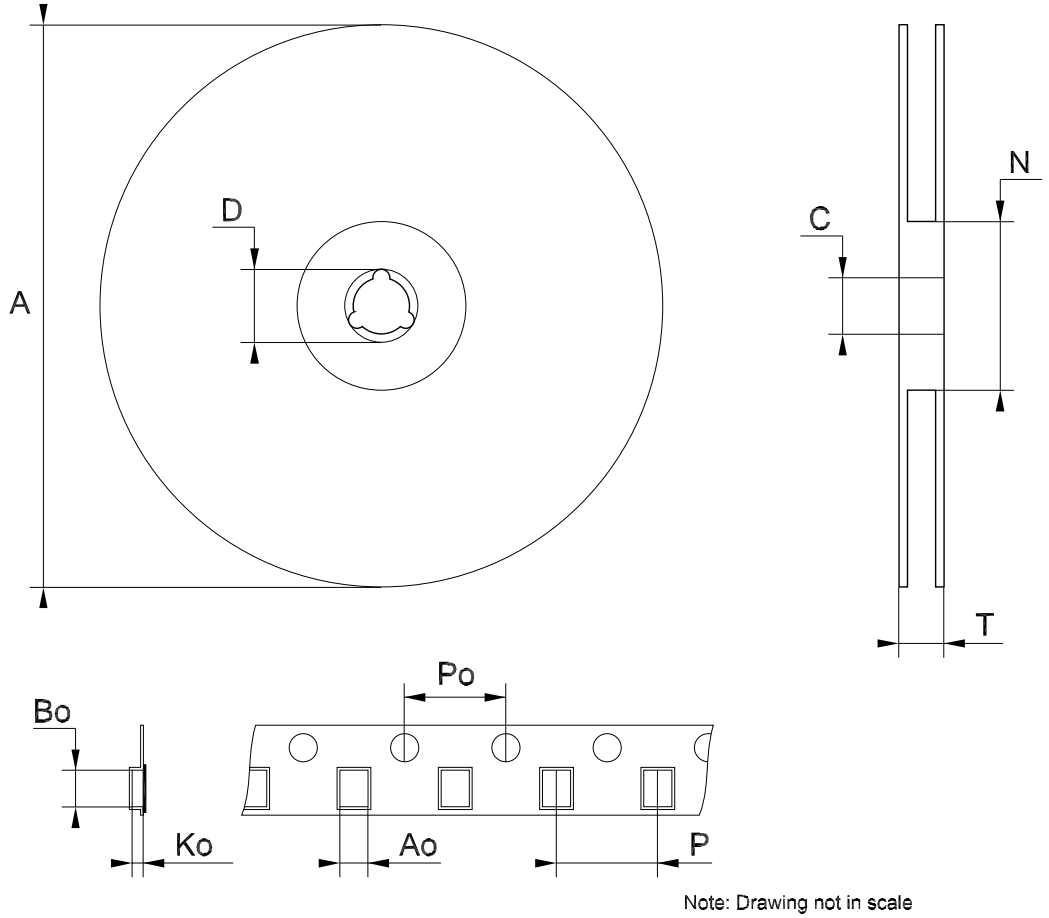
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	6.73	6.83	6.93	0.265	0.269	0.273
Bo	7.32	7.42	7.52	0.288	0.292	0.296
Ko	1.78		2	0.070		0.078
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



Note: Drawing not in scale

Tape & Reel SO-8 MECHANICAL DATA

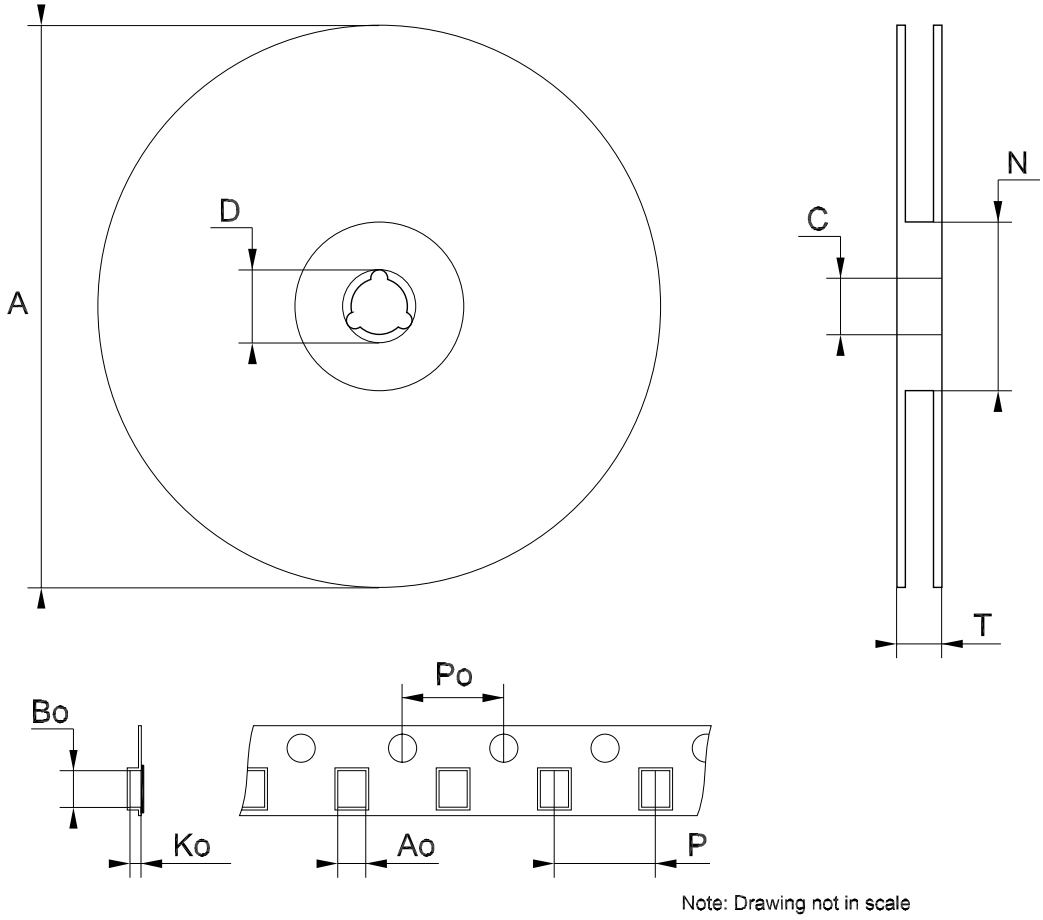
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

Tape & Reel DPAK-PPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.80	6.90	7.00	0.268	0.272	0.2.76
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



Note: Drawing not in scale

Table 19: Revision History

Date	Revision	Description of Changes
22-Sep-2004	15.0	Add new Part Number #12C; Typing Error: Note on table 2.
25-Oct-2004	16.0	Add V_{ref} Reference Voltage on Table 12.

Low power dual operational amplifiers

NE/SA/SE532/ LM158/258/358/A/2904

DESCRIPTION

The 532/358/LM2904 consists of two independent, high gain, internally frequency-compensated operational amplifiers internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature-compensated. The input bias current is also temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain—100dB
- Wide bandwidth (unity gain)—1MHz (temperature-compensated)

PIN CONFIGURATIONS

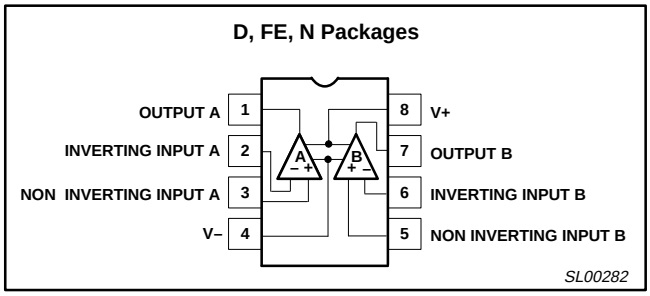


Figure 1. Pin Configuration

- Wide power supply range single supply—$3V_{DC}$ to $30V_{DC}$ or dual supplies—$\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain (400µA)—essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current—$45nA_{DC}$ temperature-compensated
- Low input offset voltage—$2mV_{DC}$ and offset current—$5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage—$0V_{DC}$ to V+ $1.5V_{DC}$ swing

EQUIVALENT CIRCUIT

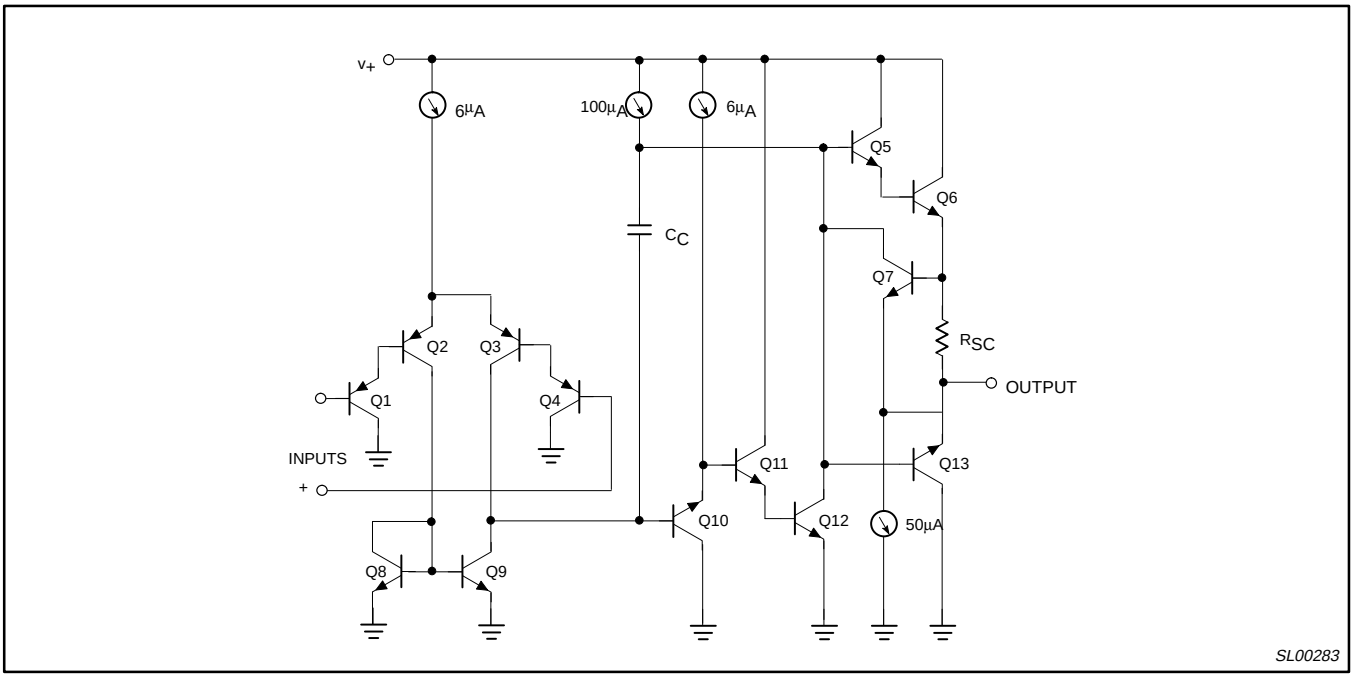


Figure 2. Equivalent Circuit

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE532D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE532N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA532D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA532N	SOT97-1
8-Pin Ceramic Dual In-Line Package (CERDIP)	-40°C to +85°C	SA532FE	0580A
8-Pin Plastic Small Outline (SO) Package	-40°C to +125°C	LM2904D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +125°C	LM2904N	SOT97-1
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	LM158FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	-25°C to +125°C	LM258N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	-25°C to +125°C	LM258D	SOT96-1
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	LM358D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM358N	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM358AN	SOT97-1
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	LM358AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE532N	SOT97-1
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE532FE	0580A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage, V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation T_A=25°C (Still air)[1] FE package N package D package	 780 1160 780	 mW mW mW
	Output short-circuit to GND[5] V+<15 V_{DC} and T_A=25°C	 Continuous	
T_A	Operating ambient temperature range NE532/LM358/LM358A LM258 LM2904 SA532 SE532/LM158	 0 to +70 -25 to +85 -40 to +125 -40 to +85 -55 to +125	 °C °C °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+=+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/ LM358/LM2904			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω R_S=0Ω, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	R_S=0Ω, over temp.		7			7		µV/°C
I_{OS}	Offset current	I_{IN} (+)-I_{IN} (-) Over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift	Over temp.		10			10		pA/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (-) Over temp., I_{IN} (+) or I_{IN} (-)		45 40	150 300		45 40	250 500	nA nA
I_B	Drift	Over temp.		50			50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V Over temp., V+=30V	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V V
CMRR	Common-mode rejection ratio	V+=30V	70	85		65	70		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp. R_L≥10kΩ, V+=30V, over temp.	26 27	28		26 27	28		V V
V_{OL}	Output voltage swing	R_L≥10kΩ, over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V R_L=∞ on all amplifiers, over temp., V+ =30V		0.5 0.6	1.0 1.2		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V (for large V_O swing) over temp.	50 25	100		25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120			-120		dB
I_{OUT}	Output current Source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		20	40		mA
		V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}, over temp.	10	20		10	20		mA
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		12	50		µA
I_{SC}	Short circuit current[5]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V
GBW	Unity gain bandwidth	T_A=25°C		1			1		MHz
SR	Slew rate	T_A=25°C		0.3			0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C, f=1kHz		40			40		nV/√Hz

DC ELECTRICAL CHARACTERISTICS T_A=25°C, V+=+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM358A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω R_S=0Ω, over temp.		±2	±3 ±5	mV mV
V_{OS}	Drift	R_S=0Ω, over temp.		7	20	µV/°C
I_{OS}	Offset current	I_{IN} (+)-I_{IN} (-) Over temp.		5	±30 ±75	nA nA
I_{OS}	Drift	Over temp.		10	300	pA/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (-) Over temp., I_{IN} (+) or I_{IN} (-)		45 40	100 200	nA nA
I_B	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V Over temp., V+=30V	0 0		V+-1.5 V+-2.0	V V
CMRR	Common-mode rejection ratio	V+=30V	65	85		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp. R_L≥10kΩ, V+=30V, over temp.	26 27	 28		V V
V_{OL}	Output voltage swing	R_L≥10kΩ, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V R_L=∞ on all amplifiers, over temp., V+ =30V		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V (for large V_O swing) over temp.	25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120		dB
I_{OUT}	Output current Source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		mA
		V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}, over temp.	10	20		mA
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		µA
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[6]				V+	V
GBW	Unity gain bandwidth	T_A=25°C		1		MHz
SR	Slew rate	T_A=25°C		0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C, f=1kHz		40		nV/√Hz

NOTES:
1. V_O ≈ 1.4V, R_S=0Ω with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V_{DC} without damage.

TYPICAL PERFORMANCE CHARACTERISTICS

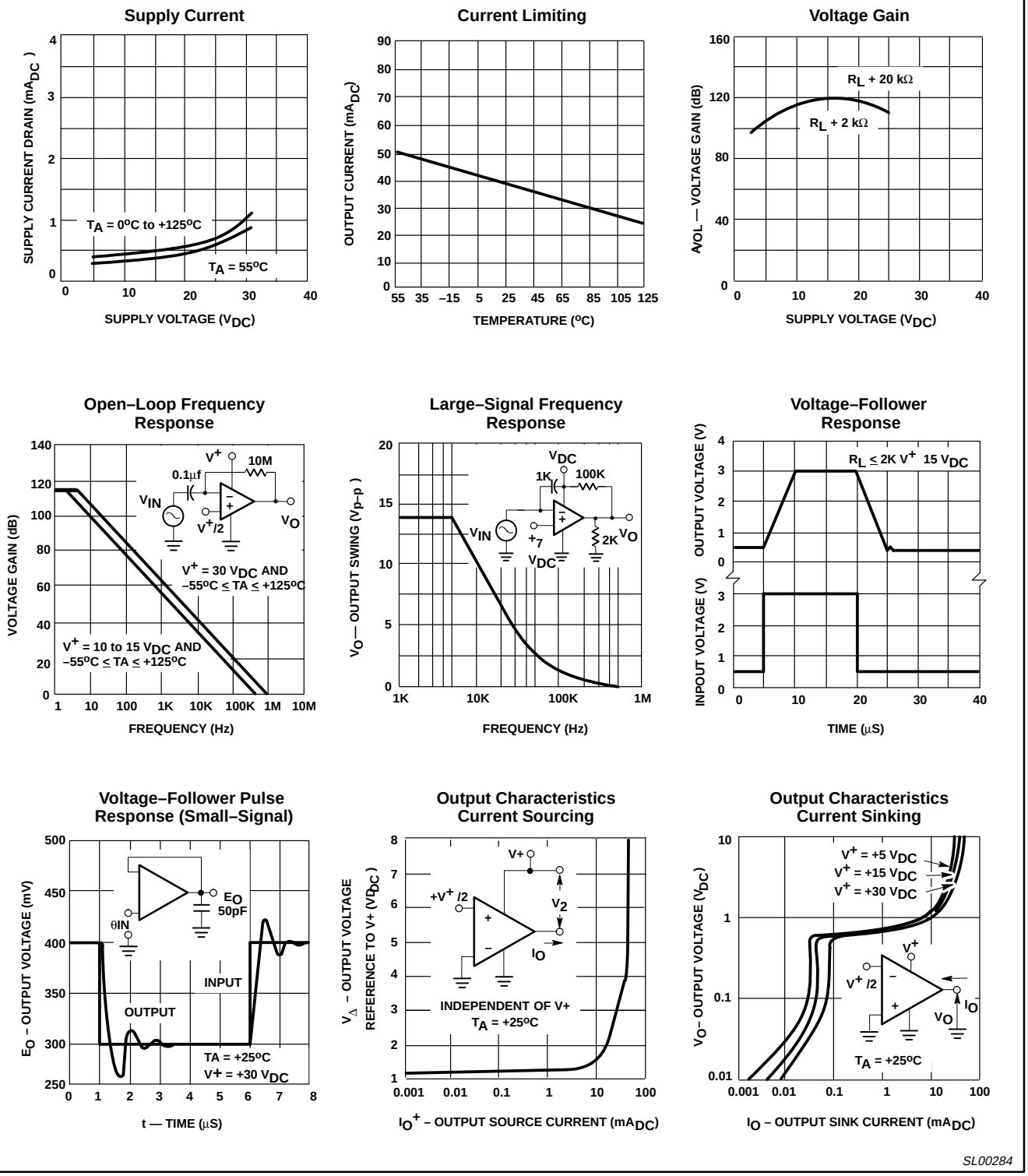


Figure 3. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

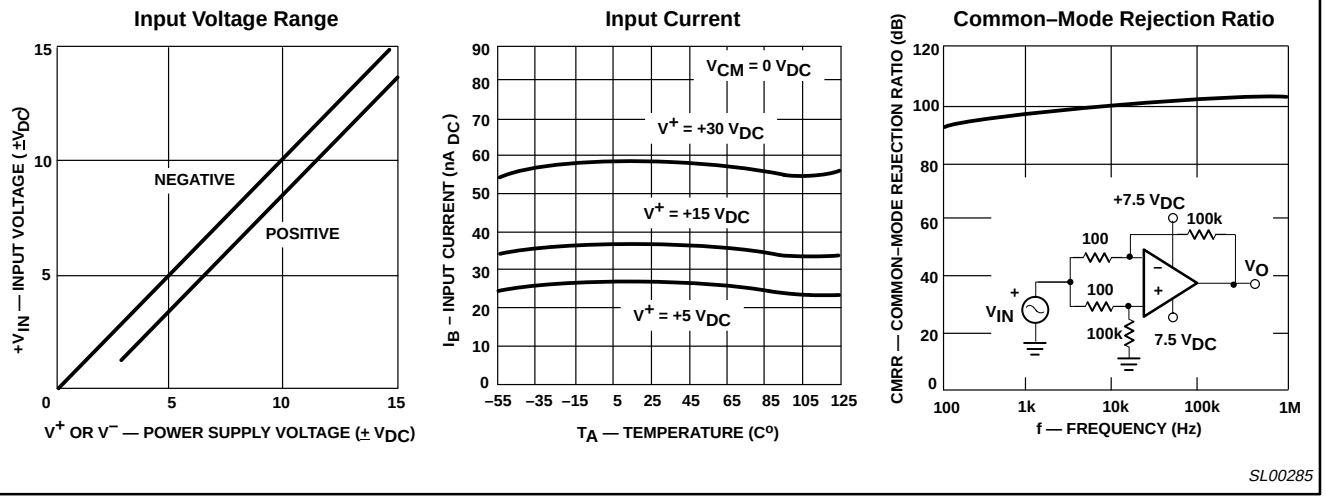


Figure 4. Typical Performance Characteristics (cont.)

TYPICAL APPLICATIONS

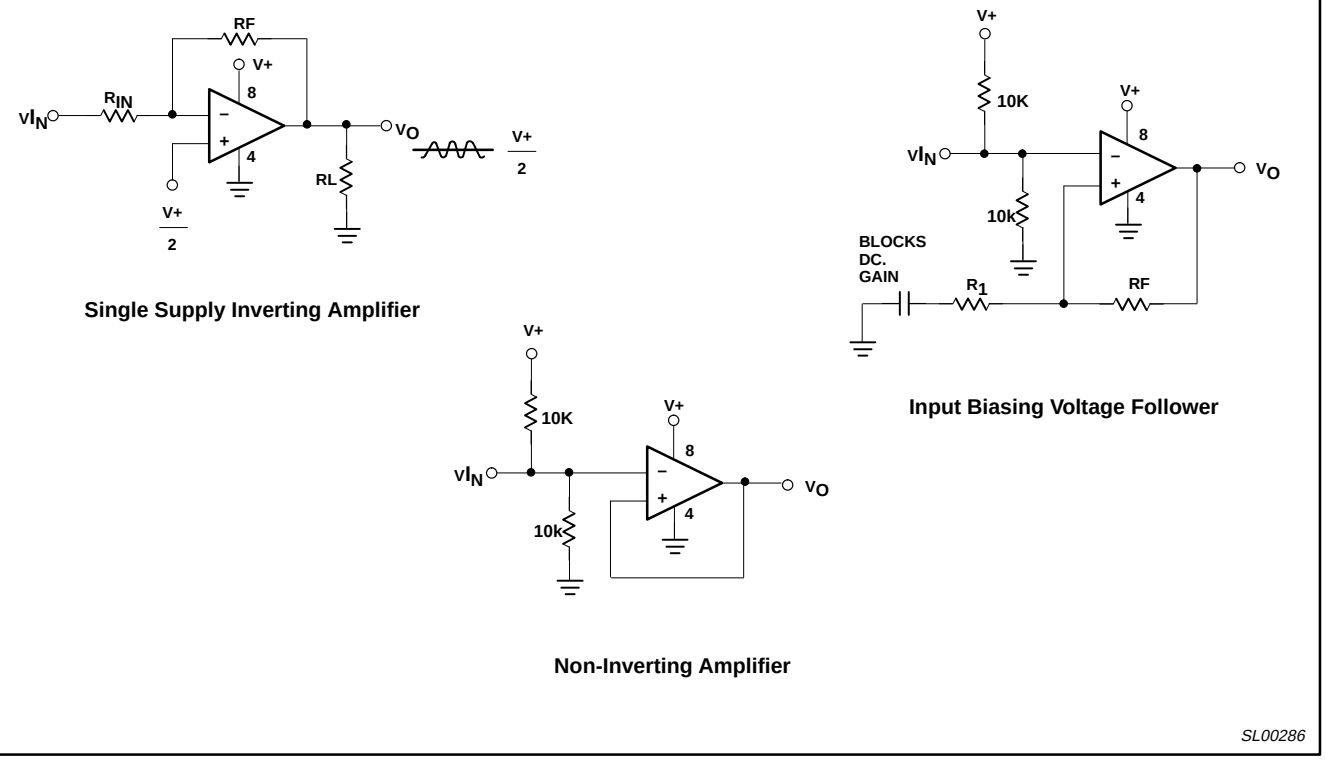


Figure 5. Typical Applications

P89LPC938

8-bit microcontroller with accelerated two-clock 80C51 core 8 kB 3 V byte-erasable Flash with 10-bit A/D converter

Rev. 01 — 25 February 2005 Product data sheet

1. General description

The P89LPC938 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC938 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 8 kB byte-erasable Flash code memory organized into 1 kB sectors and 64-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory and a 512-byte auxiliary on-chip RAM.
- 512-byte customer Data EEPROM on chip allows serialization of devices, storage of set-up parameters, etc.
- 8-input multiplexed 10-bit A/D converter. Two analog comparators with selectable inputs and reference source.
- Two 16-bit counter/timers (each may be configured to toggle a port output upon timer overflow or to become a PWM output) and a 23-bit system timer that can also be used as a RTC.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I^2C-bus communication port and SPI communication port.
- CCU provides PWM, input capture, and output compare functions.
- High-accuracy internal RC oscillator option allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 28-pin TSSOP, PLCC, and HVQFN packages with 23 I/O pins minimum and up to 26 I/O pins while using on-chip oscillator and reset options.

PHILIPS

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial Flash ICP allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial Flash ISP allows coding while the device is mounted in the end application.
- In-Application Programming of the Flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed Flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC938 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC938FA	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2
P89LPC938FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC938FHN	HVQFN28	plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 6 × 6 × 0.85 mm	SOT788-1

3.1 Ordering options

Table 2: Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC938FA	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC938FDH	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC938FHN	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz

4. Block diagram

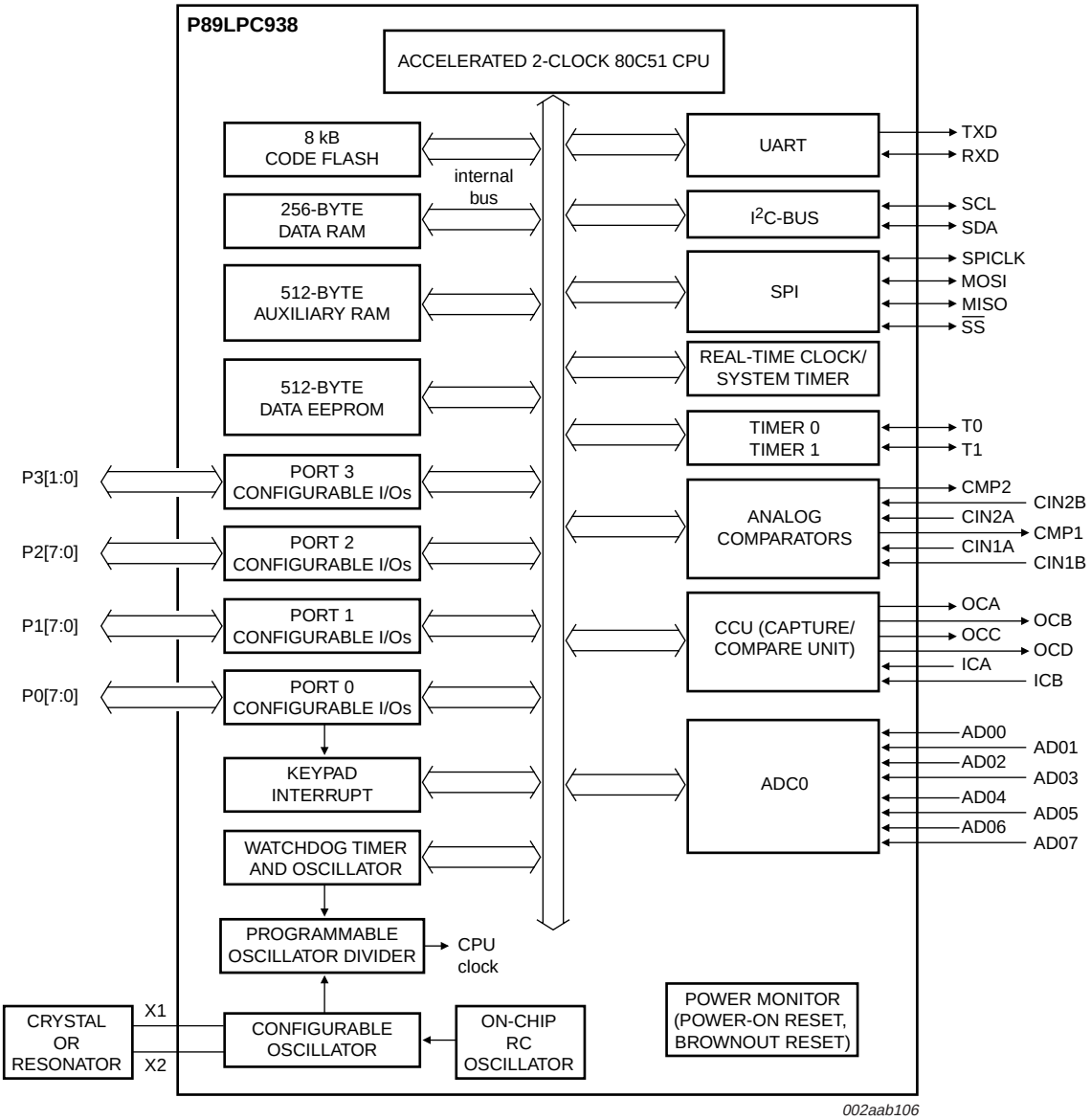


Fig 1. Block diagram.

5. Functional diagram

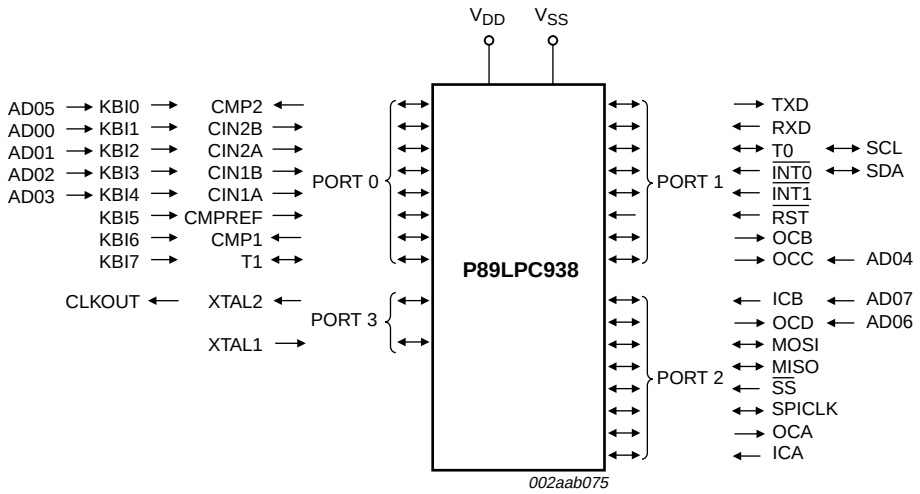


Fig 2. P89LPC938 functional diagram.

6. Pinning information

6.1 Pinning

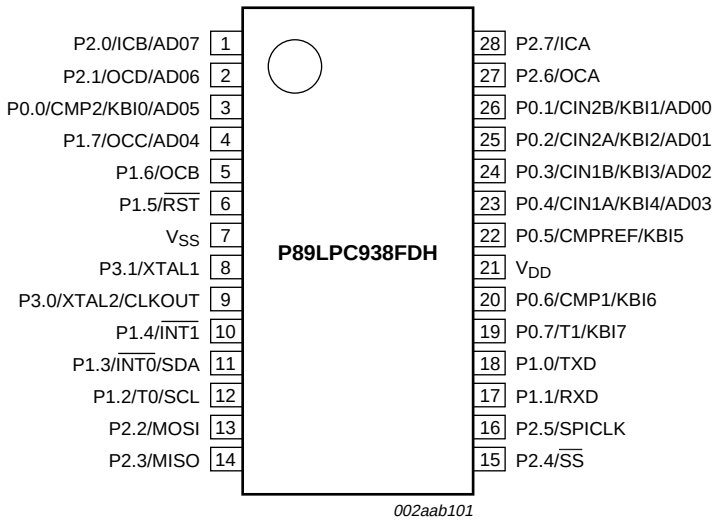


Fig 3. TSSOP28 pin configuration.

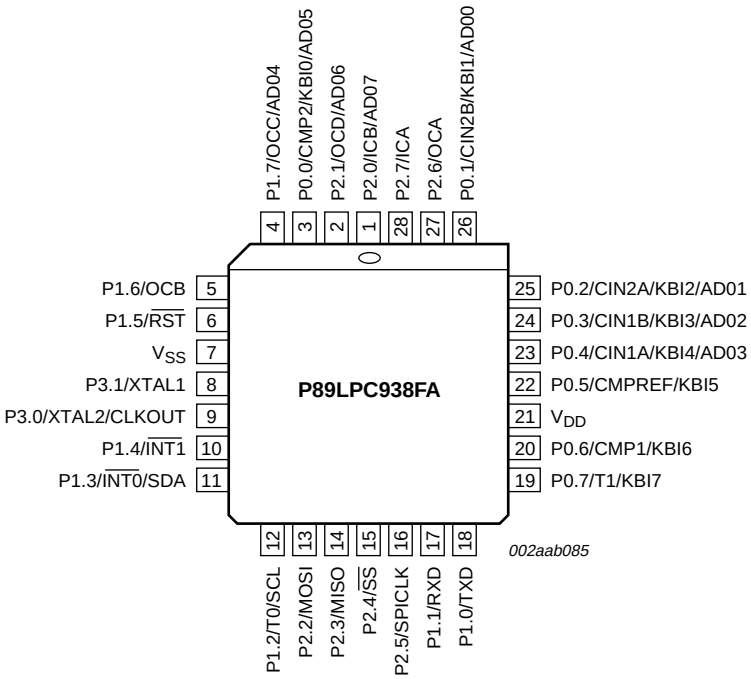


Fig 4. PLCC28 pin configuration.

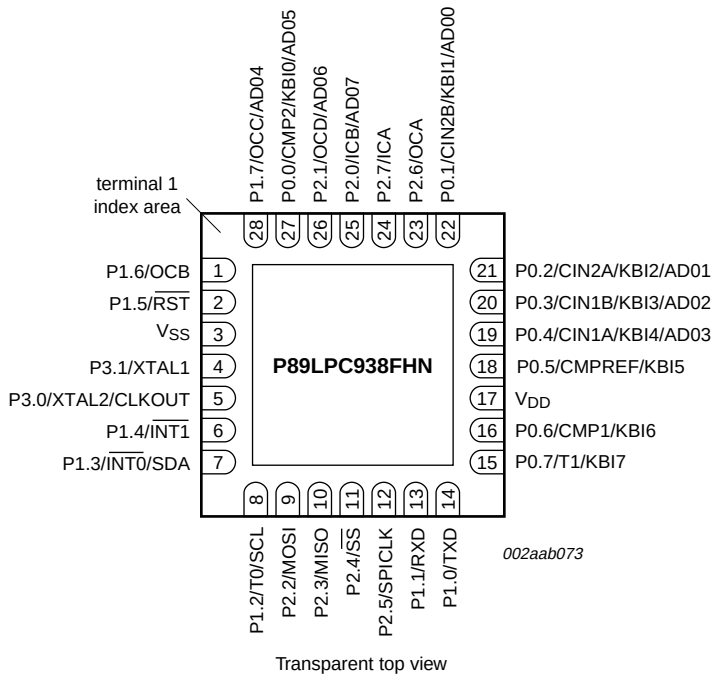


Fig 5. HVQFN28 pin configuration (top view).

6.2 Pin description

Table 3: Pin description

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.0 to P0.7			I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 "Port configurations" and Table 10 "DC electrical characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0/AD05	3	27	I/O	**P0.0 —** Port 0 bit 0.
			O	**CMP2 —** Comparator 2 output.
			I	**KBI0 —** Keyboard input 0.
			I	**AD05 —** ADC0 channel 5 analog input.
P0.1/CIN2B/ KBI1/AD00	26	22	I/O	**P0.1 —** Port 0 bit 1.
			I	**CIN2B —** Comparator 2 positive input B.
			I	**KBI1 —** Keyboard input 1.
			I	**AD00 —** ADC0 channel 0 analog input.

Table 3: Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.2/CIN2A/ KBI2/AD01	25	21	I/O	**P0.2 —** Port 0 bit 2.
			I	**CIN2A —** Comparator 2 positive input A.
			I	**KBI2 —** Keyboard input 2.
			I	**AD01 —** ADC0 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD02	24	20	I/O	**P0.3 —** Port 0 bit 3.
			I	**CIN1B —** Comparator 1 positive input B.
			I	**KBI3 —** Keyboard input 3.
			I	**AD02 —** ADC0 channel 2 analog input.
P0.4/CIN1A/ KBI4/AD03	23	19	I/O	**P0.4 —** Port 0 bit 4.
			I	**CIN1A —** Comparator 1 positive input A.
			I	**KBI4 —** Keyboard input 4.
			I	**AD03 —** ADC0 channel 3 analog input.
P0.5/CMPREF/ KBI5	22	18	I/O	**P0.5 —** Port 0 bit 5.
			I	**CMPREF —** Comparator reference (negative) input.
			I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	20	16	I/O	**P0.6 —** Port 0 bit 6.
			O	**CMP1 —** Comparator 1 output.
			I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	19	15	I/O	**P0.7 —** Port 0 bit 7.
			I/O	**T1 —** Timer/counter 1 external count input or overflow output.
			I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7			I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 “Port configurations” and Table 10 “DC electrical characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	14	I/O	**P1.0 —** Port 1 bit 0.
			O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	17	13	I/O	**P1.1 —** Port 1 bit 1.
			I	**RXD —** Receiver input for the serial port.
P1.2/T0/SCL	12	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
			I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
			I/O	**SCL —** I^2C serial clock input/output.

Table 3: Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P1.3/$\overline{\text{INT0}}$/SDA	11	7	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
			I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
			I/O	**SDA —** I^2C serial data input/output.
P1.4/$\overline{\text{INT1}}$	10	6	I	**P1.4 —** Port 1 bit 4.
			I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P1.5/$\overline{\text{RST}}$	6	2	I	**P1.5 —** Port 1 bit 5 (input only).
			I	**$\overline{\text{RST}}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force In-System Programming mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating range.**
P1.6/OCB	5	1	I/O	**P1.6 —** Port 1 bit 6.
			O	**OCB —** Output Compare B.
P1.7/OCC/ AD04	4	28	I/O	**P1.7 —** Port 1 bit 7.
			O	**OCC —** Output Compare C.
			I	**AD04 —** ADC0 channel 4 analog input.
P2.0 to P2.7			I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 10 “DC electrical characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.0/ICB/AD07	1	25	I/O	**P2.0 —** Port 2 bit 0.
			I	**ICB —** Input Capture B.
			I	**AD07 —** ADC0 channel 7 analog input.
P2.1/OCD/ AD06	2	26	I/O	**P2.1 —** Port 2 bit 1.
			O	**OCD —** Output Compare D.
			I	**AD06 —** ADC0 channel 6 analog input.
P2.2/MOSI	13	9	I/O	**P2.2 —** Port 2 bit 2.
			I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	14	10	I/O	**P2.3 —** Port 2 bit 3.
			I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.

Table 3: Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P2.4/$\overline{SS}$	15	11	I/O	**P2.4 —** Port 2 bit 4.
			I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	16	12	I/O	**P2.5 —** Port 2 bit 5.
			I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6/OCA	27	23	I/O	**P2.6 —** Port 2 bit 6.
			O	**OCA —** Output Compare A.
P2.7/ICA	28	24	I/O	**P2.7 —** Port 2 bit 7.
			I	**ICA —** Input Capture A.
P3.0 to P3.1			I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 10 “DC electrical characteristics” for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	9	5	I/O	**P3.0 —** Port 3 bit 0.
			O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the Flash configuration.
			O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	8	4	I/O	**P3.1 —** Port 3 bit 1.
			I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the Flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	7	3	I	**Ground:** 0 V reference.
V_{DD}	21	17	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/Output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

7. Functional description

Remark: Please refer to the *P89LPC938 User's Manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 4: P89LPC938 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AD0CON	ADC0 control register	97H	ENBI0	ENADCI 0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	00000000
AD0INS	ADC0 input select	A3H	ADI07	ADI06	ADI05	ADI04	ADI03	ADI02	ADI01	ADI00	00	00000000
AD0MOD A	ADC0 mode register A	C0H	BNDI0	BURST0	SCC0	SCAN0	-	-	-	-	00	00000000
AD0MOD B	ADC0 mode register B	A1H	CLK2	CLK1	CLK0	-	-	-	-	-	00	000x0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0 [1]	Baud rate generator rate low	BEH									00	00000000
BRGR1 [1]	Baud rate generator rate high	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00 [1]	xxxxxx00
CCCRA	Capture compare A control register	EAH	ICECA2	ICECA1	ICECA0	ICESA	ICNFA	FCOA	OCMA1	OCMA0	00	00000000
CCCRB	Capture compare B control register	EBH	ICECB2	ICECB1	ICECB0	ICESB	ICNFB	FCOB	OCMB1	OCMB0	00	00000000
CCCRC	Capture compare C control register	ECH	-	-	-	-	-	FCOC	OCMC1	OCMC0	00	xxxxx000
CCCRD	Capture compare D control register	EDH	-	-	-	-	-	FCOD	OCMD1	OCMD0	00	xxxxx000
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00 [2]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00 [2]	xx000000
DEECON	Data EEPROM control register	F1H	EEIF	HVERR	ECTL1	ECTL0	-	-	-	EADR8	0E	00001110
DEEDAT	Data EEPROM data register	F2H									00	00000000
DEEADR	Data EEPROM address register	F3H									00	00000000
DIVM	CPU clock divide-by-M control	95H									00	00000000

Table 4: P89LPC938 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	00000000
DPL	Data pointer low	82H									00	00000000
FMADRH	Program Flash address high	E7H									00	00000000
FMADRL	Program Flash address low	E6H									00	00000000
FMCON	Program Flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
I2ADR	I^2C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	00000000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x00000x0
I2DAT	I^2C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	00000000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	00000000
I2STAT	I^2C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	11111000
ICRAH	Input capture A register high	ABH									00	00000000
ICRAL	Input capture A register low	AAH									00	00000000
ICRBH	Input capture B register high	AFH									00	00000000
ICRBL	Input capture B register low	AEH									00	00000000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	00000000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EIEE	EST	-	ECCU	ESPI	EC	EKBI	EI2C	00 [2]	00x00000
IEN2	Interrupt enable 2	D5H	-	-	-	-	-	-	EADC	-	00 [2]	00x00000
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00 [2]	x0000000

Table 4: P89LPC938 Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00 [2]	x0000000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PADEE	PST	-	PCCU	PSPI	PC	PKBI	PI2C	00 [2]	00x00000
IP1H	Interrupt priority 1 high	F7H	PADEEH	PSTH	-	PCCUH	PSPIH	PCH	PKBIH	PI2CH	00 [2]	00x00000
IP2	Interrupt priority 2	D6H	-	-	-	-	-	-	PADC	-	00 [2]	00x00000
IP2H	Interrupt priority 2 high	D7H	-	-	-	-	-	-	PADCH	-	00 [2]	00x00000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00 [2]	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register										FF	11111111
OCRAH	Output compare A register high	EFH									00	00000000
OCRAL	Output compare A register low	EEH									00	00000000
OCRBH	Output compare B register high	FBH									00	00000000
OCRBL	Output compare B register low	FAH									00	00000000
OCRCH	Output compare C register high	FDH									00	00000000
OCRCL	Output compare C register low	FCH									00	00000000
OCRDH	Output compare D register high	FFH									00	00000000
OCRDL	Output compare D register low	FEH									00	00000000
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H	T1/KB7	CMP1/KB6	CMPREF/KB5	CIN1A/KB4	CIN1B/KB3	CIN2A/KB2	CIN2B/KB1	CMP2/KB0		[2]
		Bit address	97	96	95	94	93	92	91	90		

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Table 4: P89LPC938 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P1*	Port 1	90H	OCC	OCB	$\overline{RST}$	$\overline{INT1}$	$\overline{INT0}$/SDA	T0/SCL	RXD	TXD		[2]
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{SS}$	MISO	MOSI	OCD	ICB		[2]
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2		[2]
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF [2]	11111111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00 [2]	00000000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3 [2]	11x1xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00 [2]	00x0xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF [2]	11111111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00 [2]	00000000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03 [2]	xxxxxx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00 [2]	xxxxxx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD	DEEPD	VCPD	ADPD	I2PD	SPPD	SPD	CCUPD	00 [2]	00000000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[3]
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60 [2] [4]	011xxx00
RTCH	RTC register high	D2H									00 [4]	00000000
RTCL	RTC register low	D3H									00 [4]	00000000
SADDR	Serial port address register	A9H									00	00000000
SADEN	Serial port address enable	B9H									00	00000000
SBUF	Serial Port data buffer register	99H									xx	xxxxxxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	00000000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000

Table 4: P89LPC938 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SP	Stack pointer	81H									07	00000111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	00000100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xxxxxx
SPDAT	SPI data register	E3H									00	00000000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	00000000
TCR20*	CCU control register 0	C8H	PLEEN	HLTRN	HLTEN	ALTCD	ALTAB	TDIR2	TMOD21	TMOD20	00	00000000
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1	PLLDV.0	00	0xxx0000
TH0	Timer 0 high	8CH									00	00000000
TH1	Timer 1 high	8DH									00	00000000
TH2	CCU timer high	CDH									00	00000000
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2D	TOCIE2C	TOCIE2B	TOCIE2A	-	TICIE2B	TICIE2A	00	00000x00
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B	TICF2A	00	00000x00
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT.2	ENCINT.1	ENCINT.0	00	xxxxx000
TL0	Timer 0 low	8AH									00	00000000
TL1	Timer 1 low	8BH									00	00000000
TL2	CCU timer low	CCH									00	00000000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	00000000
TOR2H	CCU reload register high	CFH									00	00000000
TOR2L	CCU reload register low	CEH									00	00000000
TPCR2H	Prescaler control register high	CBH	-	-	-	-	-	-	TPCR2H.1	TPCR2H.0	00	xxxxxx00
TPCR2L	Prescaler control register low	CAH	TPCR2L.7	TPCR2L.6	TPCR2L.5	TPCR2L.4	TPCR2L.3	TPCR2L.2	TPCR2L.1	TPCR2L.0	00	00000000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0		[5] [4]
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK		[6] [4]

Table 4: P89LPC938 Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[2] All ports are in input only (high-impedance) state after power-up.

[3] The RSTSRC register reflects the cause of the P89LPC938 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] The only reset source that affects these SFRs is power-on reset.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

Table 5: P89LPC938 extended special function registers

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
ADC0HBND	ADC0 high _boundary register, left (MSB)	FFEFh			FF	11111111
ADC0LBND	ADC0 low_boundary register (MSB)	FFEEh			00	00000000
AD0DAT0R	ADC0 data register 0, right (LSB)	FFFEh	AD0DAT0[7:0]		00	00000000
AD0DAT0L	ADC0 data register 0, left (MSB)	FFFFh	AD0DAT0[9:2]		00	00000000
AD0DAT1R	ADC0 data register 1, right (LSB)	FFFCh	AD0DAT1[7:0]		00	00000000
AD0DAT1L	ADC0 data register 1, left (MSB)	FFFDh	AD0DAT1[9:2]		00	00000000
AD0DAT2R	ADC0 data register 2, right (LSB)	FFFAh	AD0DAT2[7:0]		00	00000000
AD0DAT2L	ADC0 data register 2, left (MSB)	FFFBh	AD0DAT2[9:2]		00	00000000
AD0DAT3R	ADC0 data register 3, right (LSB)	FFF8h	AD0DAT3[7:0]		00	00000000
AD0DAT3L	ADC0 data register 3, left (MSB)	FFF9h	AD0DAT3[9:2]		00	00000000
AD0DAT4R	ADC0 data register 4, right (LSB)	FFF6h	AD0DAT4[7:0]		00	00000000
AD0DAT4L	ADC0 data register 4, left (MSB)	FFF7h	AD0DAT4[9:2]		00	00000000
AD0DAT5R	ADC0 data register 5, right (LSB)	FFF4h	AD0DAT5[7:0]		00	00000000
AD0DAT5L	ADC0 data register 5, left (MSB)	FFF5h	AD0DAT5[9:2]		00	00000000
AD0DAT6R	ADC0 data register 6, right (LSB)	FFF2h	AD0DAT6[7:0]		00	00000000
AD0DAT6L	ADC0 data register 6, left (MSB)	FFF3h	AD0DAT6[9:2]		00	00000000
AD0DAT7R	ADC0 data register 7, right (LSB)	FFF0h	AD0DAT7[7:0]			
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1h	AD0DAT7[9:2]			
BNDSTA0	ADC0 boundary status register	FFEDh				

7.2 Enhanced CPU

The P89LPC938 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC938 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 6) and can also be optionally divided to a slower frequency (see Section 7.8 “CCLK modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC938 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the Flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz.

7.3.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.3.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.3.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

7.3.6 Clock output

The P89LPC938 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the RTC is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC938. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is ½ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.4 On-chip RC oscillator option

The P89LPC938 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies.

7.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

7.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 18 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

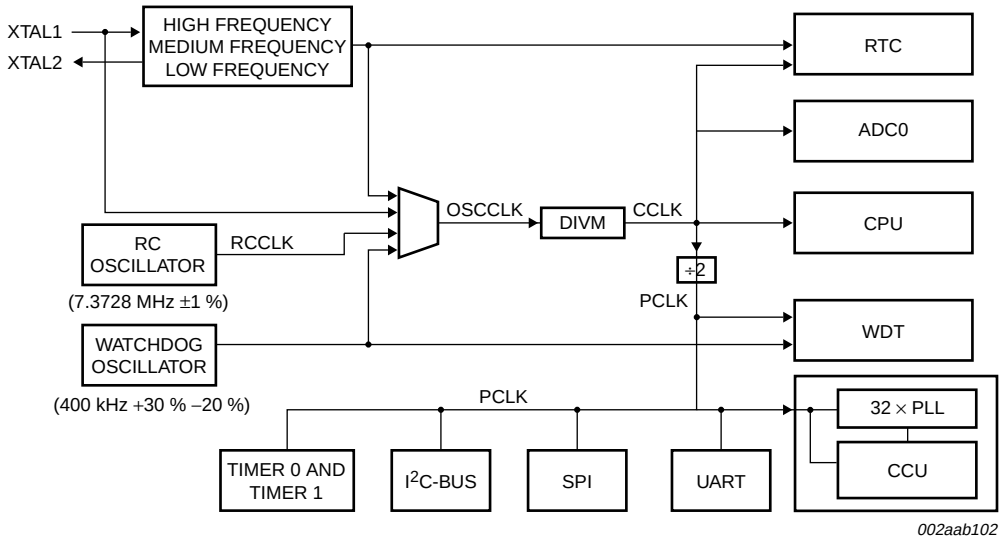


Fig 6. Block diagram of oscillator control.

7.7 CCLK wake-up delay

The P89LPC938 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

7.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.9 Low power select

The P89LPC938 is designed to run at 12 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

7.10 Memory organization

The various P89LPC938 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  ‘External’ Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC938 has 512 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC938 has 8 kB of on-chip Code memory.

The P89LPC938 also has 512 bytes of on-chip Data EEPROM that is accessed via SFRs (see Section 7.27 “Data EEPROM”).

7.11 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 6.

Table 6: On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary (‘External Data’) on-chip memory that is accessed using the MOVX instructions	512

7.12 Interrupts

The P89LPC938 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC938 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/RTC, I^2C, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write/ADC completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

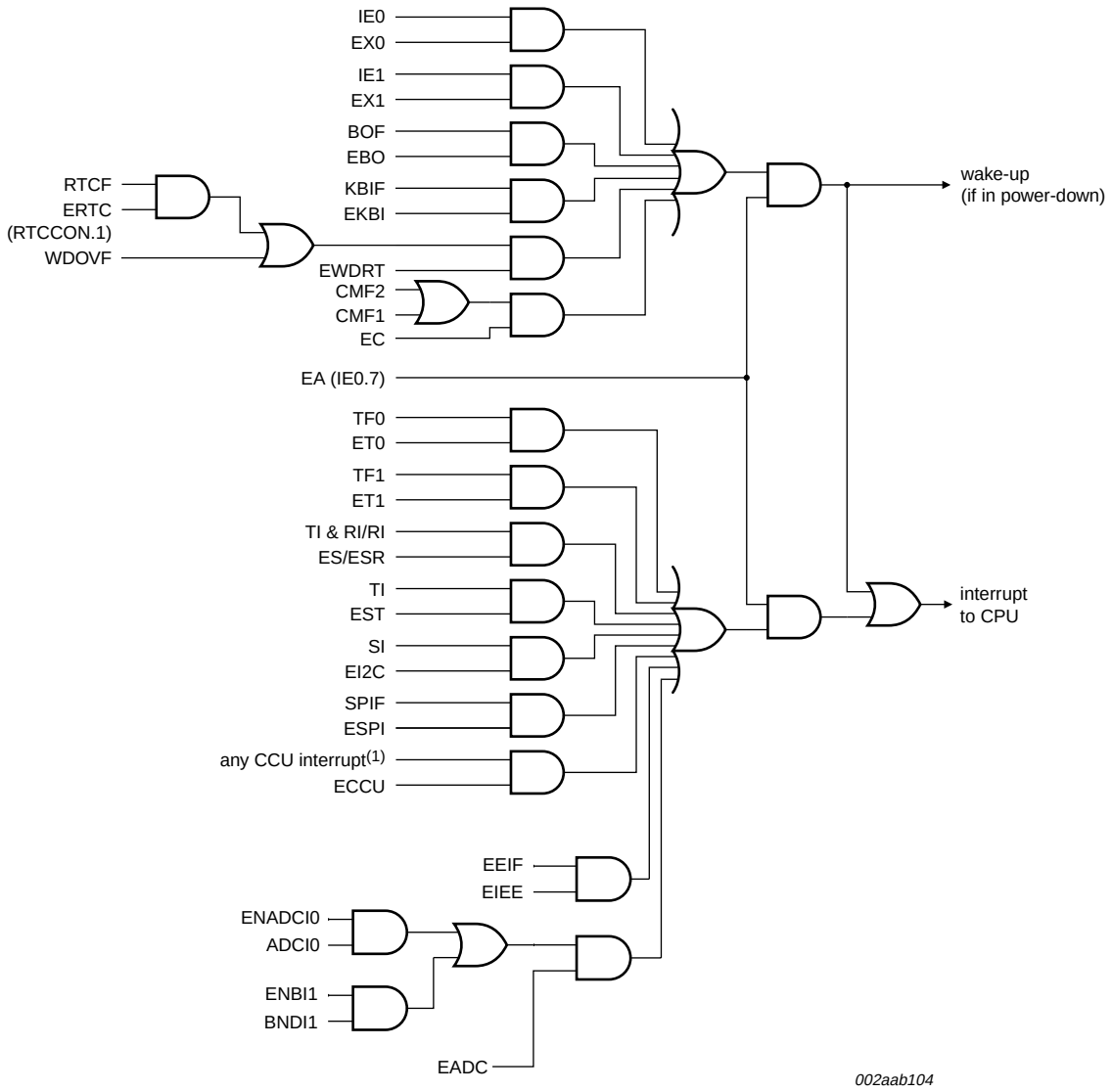
7.12.1 External interrupt inputs

The P89LPC938 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC938 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.15 “Power reduction modes” for details.



(1) See Section 7.19 “CCU”

Fig 7. Interrupt sources, interrupt enables, and power-down wake-up sources.

7.13 I/O ports

The P89LPC938 has four I/O ports: Port 0, Port 1, Port 2, and Port 3. Ports 0, 1and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 7.

Table 7: Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported [1]	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported [1]	23

[1] Required for operation above 12 MHz.

7.13.1 Port configurations

All but three I/O port pins on the P89LPC938 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

7.13.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC938 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.2 Port 0 analog functions

The P89LPC938 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to ‘0’s to enable digital functions.

7.13.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC938 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 10 “DC electrical characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.14 Power monitoring functions

The P89LPC938 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

7.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 10 “DC electrical characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC938 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 10 “DC electrical characteristics” for specifications.

7.14.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.15 Power reduction modes

The P89LPC938 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC938 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention voltage (V_{DDR}). This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: brownout detect, watchdog timer, comparators (note that comparators can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

7.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to '1', enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, The RPE selection is overridden and this pin will always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1);
- Power-on detect;
- Brownout detect;
- Watchdog timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a '0' to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.16.1 Reset vector

Following reset, the P89LPC938 will fetch instructions from either address 0000h or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00h.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC938 User's Manual*). Otherwise, instructions will be fetched from address 0000H.

7.17 Timers/counters 0 and 1

The P89LPC938 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.17.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.17.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.17.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.18 RTC/system timer

The P89LPC938 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all '0's, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as

the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

7.19 CCU

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- Four compare/PWM outputs with selectable polarity
- Symmetrical/Asymmetrical PWM selection
- Two capture inputs with event counter and digital noise rejection filter
- Seven interrupts with common interrupt vector (one Overflow, two Capture, four Compare)
- Safe 16-bit read/write via shadow registers.

7.19.1 CCU Clock (CCUCLK)

The CCU runs on the CCUCLK, which is either PCLK in basic timer mode, or the output of a PLL. The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

7.19.2 CCU clock prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

7.19.3 Basic timer operation

The Timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU Timer may also be used as an 8-bit up/down timer.

7.19.4 Output compare

There are four output compare channels A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

7.19.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input

Capture Noise Filter bit. If set, the capture logic needs to see four consecutive samples of the same value in order to recognize an edge as a capture event. An event counter can be set to delay a capture by a number of capture events.

7.19.6 PWM operation

PWM operation has two main modes, symmetrical and asymmetrical.

In asymmetrical PWM operation the CCU Timer operates in down-counting mode regardless of the direction control bit.

In symmetrical mode, the timer counts up/down alternately. The main difference from basic timer operation is the operation of the compare module, which in PWM mode is used for PWM waveform generation.

As with basic timer operation, when the PWM (compare) pins are connected to the compare logic, their logic state remains unchanged. However, since bit FCO is used to hold the halt value, only a compare event can change the state of the pin.

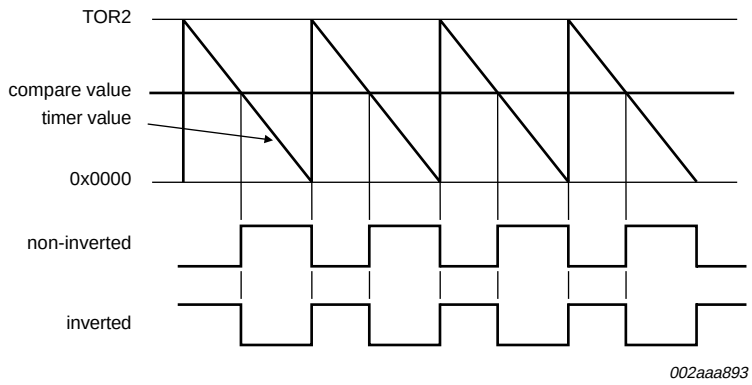


Fig 8. Asymmetrical PWM, down-counting.

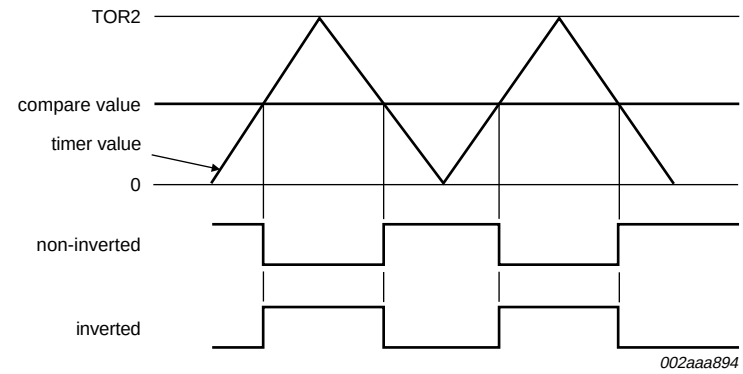


Fig 9. Symmetrical PWM.

7.19.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.

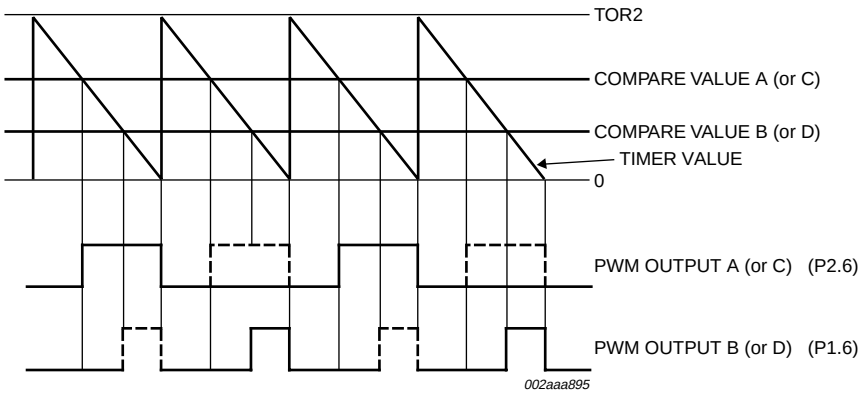


Fig 10. Alternate output mode.

7.19.8 PLL operation

The PWM module features a Phase Locked Loop that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal of 0.5 - 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor of 1-16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in Equation 1.

$$\text{PLL frequency} = \frac{\text{PLCK}}{(N+1)} \quad (1)$$

Where: N is the value of PLLDV3:0.

Since N ranges in 0 - 15, the CCLK frequency can be in the range of PCLK to $^{PCLK}/_{16}$.

7.19.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

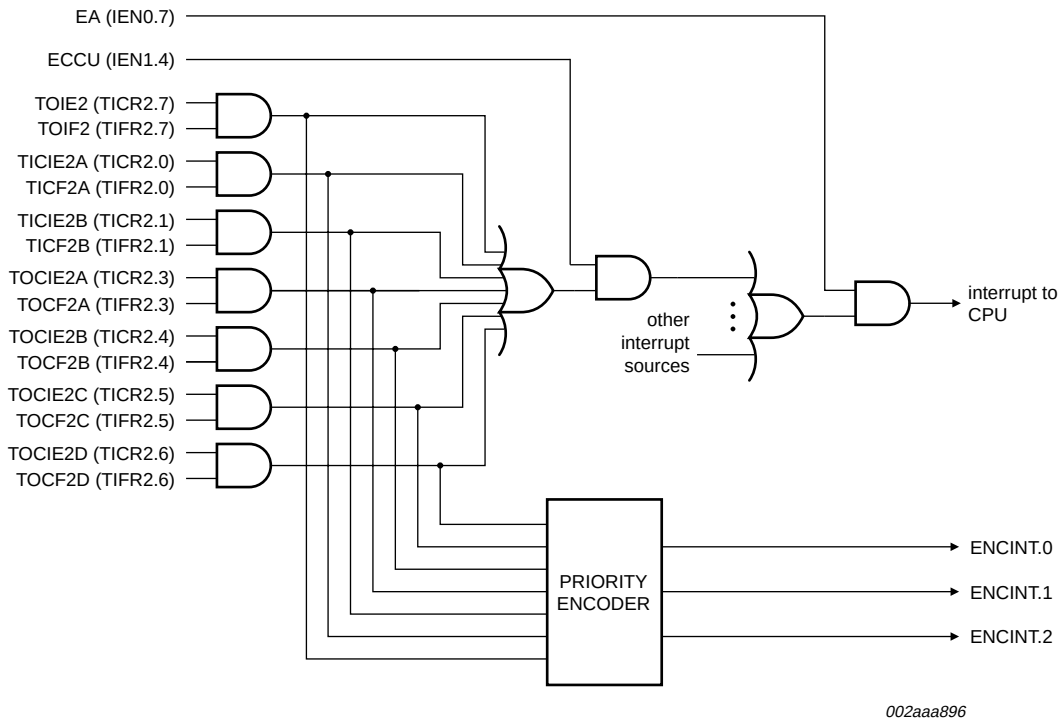


Fig 11. Capture/Compare Unit interrupts.

7.20 UART

The P89LPC938 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC938 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

7.20.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.20.5 “Baud rate generator and selection”).

7.20.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of '0' or '1'. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

7.20.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.20.5 "Baud rate generator and selection").

7.20.5 Baud rate generator and selection

The P89LPC938 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 12). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses OSCCLK.

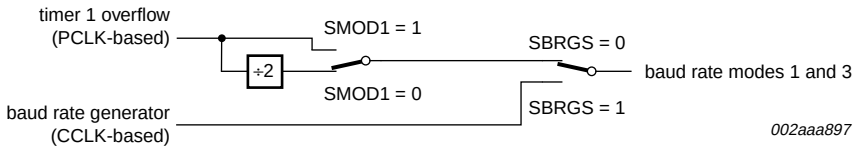


Fig 12. Baud rate sources for UART (Modes 1, 3).

7.20.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is '1', framing errors can be made available in SCON.7 respectively. If SMOD0 is '0', SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is '0'.

7.20.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.20.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.20.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

7.20.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.21 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bi-directional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 13. The P89LPC938 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

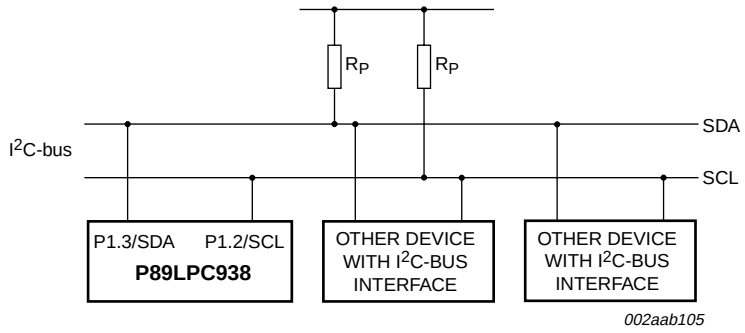


Fig 13. I²C-bus configuration.

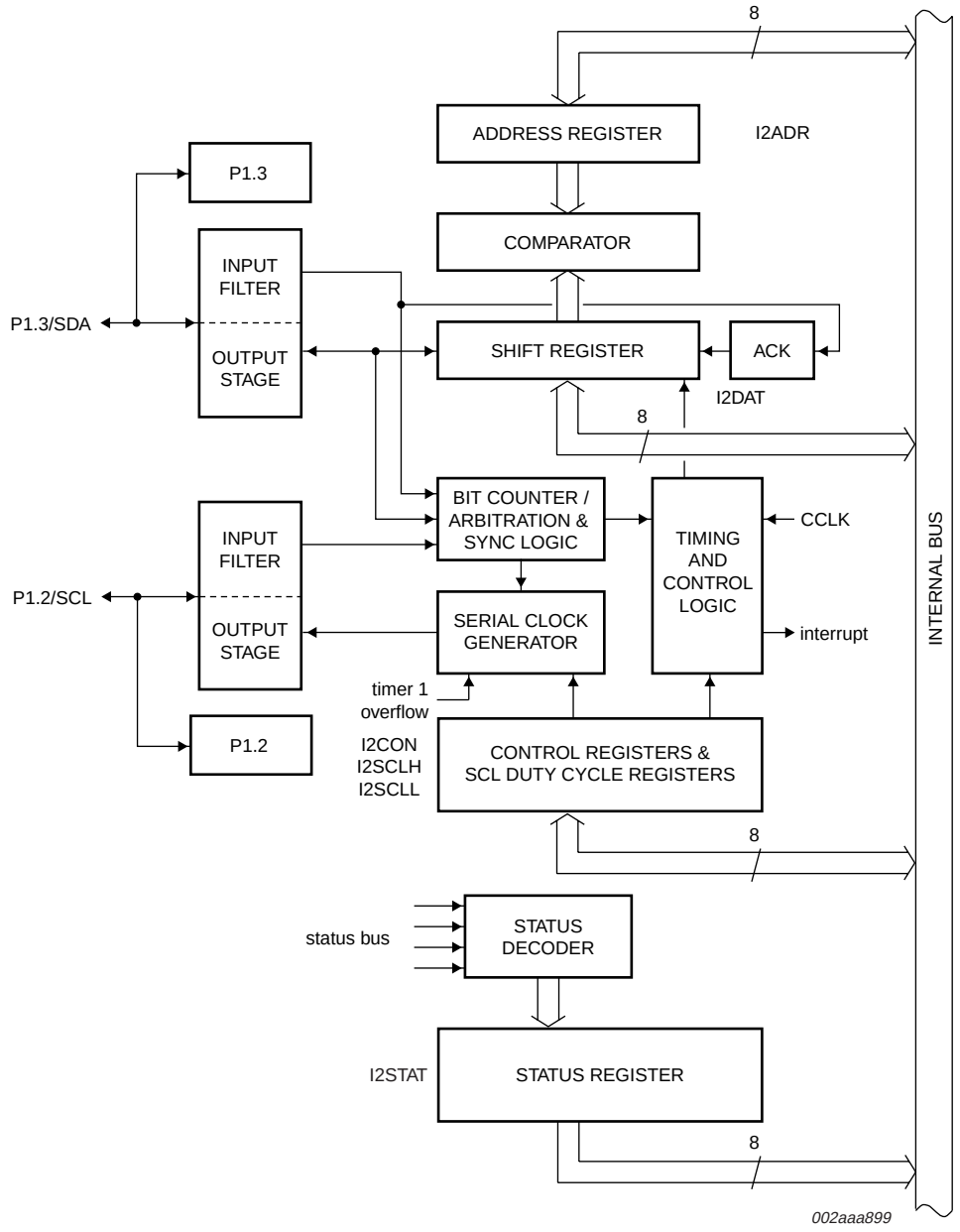


Fig 14. I²C-bus serial interface block diagram.

7.22 SPI

The P89LPC938 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

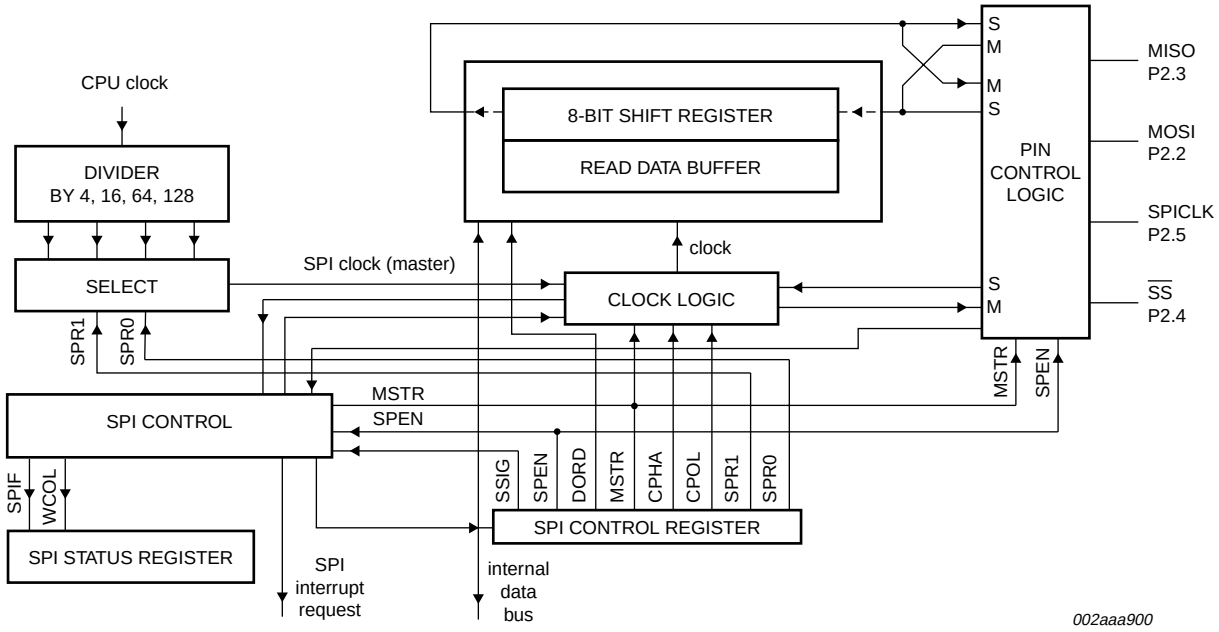


Fig 15. SPI block diagram.

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 16 through Figure 18.

7.22.1 Typical SPI configurations

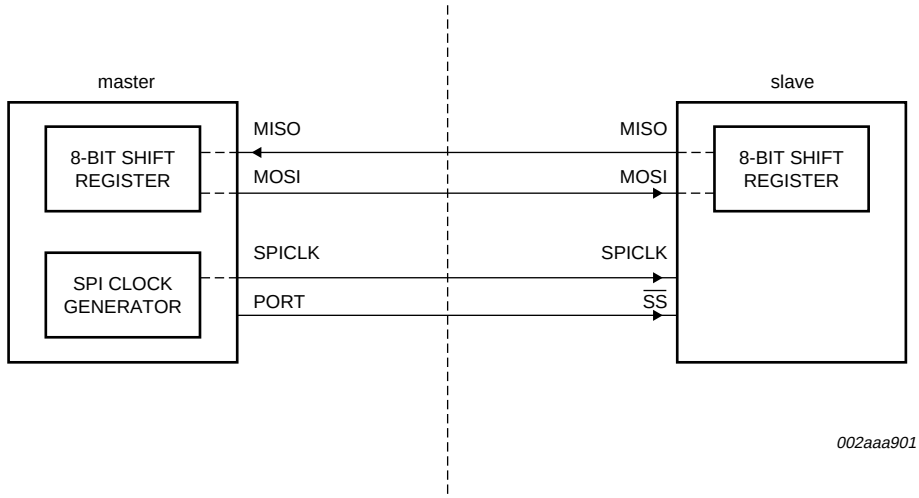


Fig 16. SPI single master single slave configuration.

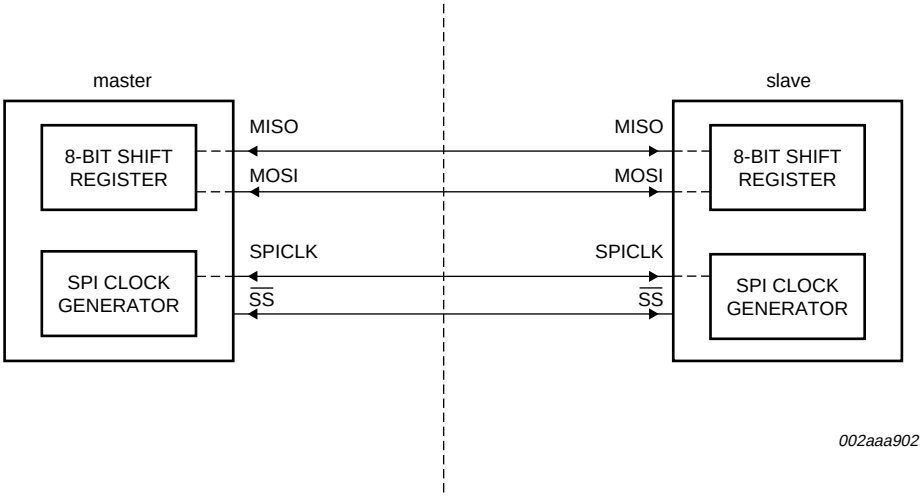


Fig 17. SPI dual device configuration, where either can be a master or a slave.

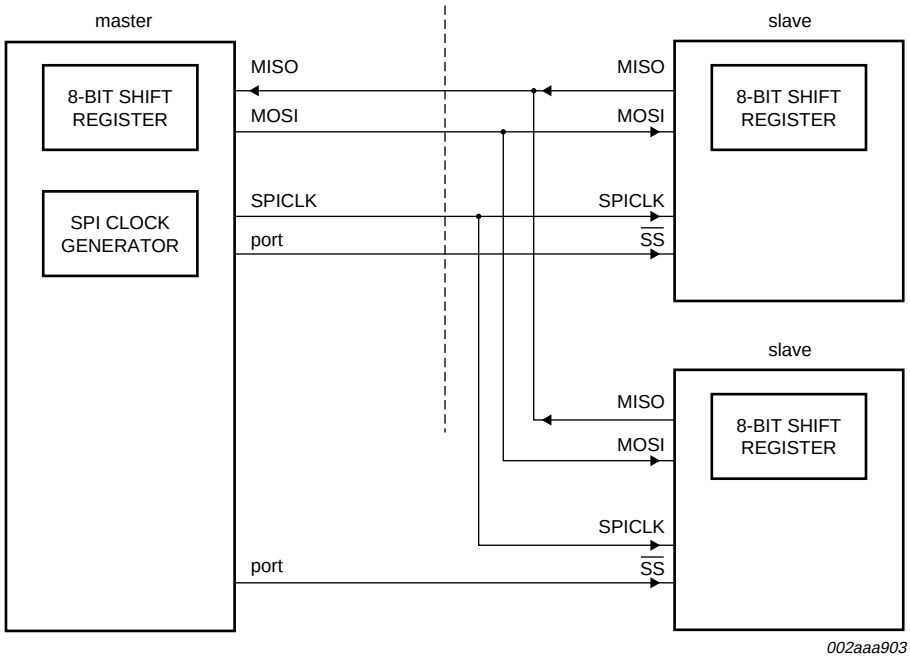


Fig 18. SPI single master multiple slaves configuration.

7.23 Analog comparators

Two analog comparators are provided on the P89LPC938. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 19. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

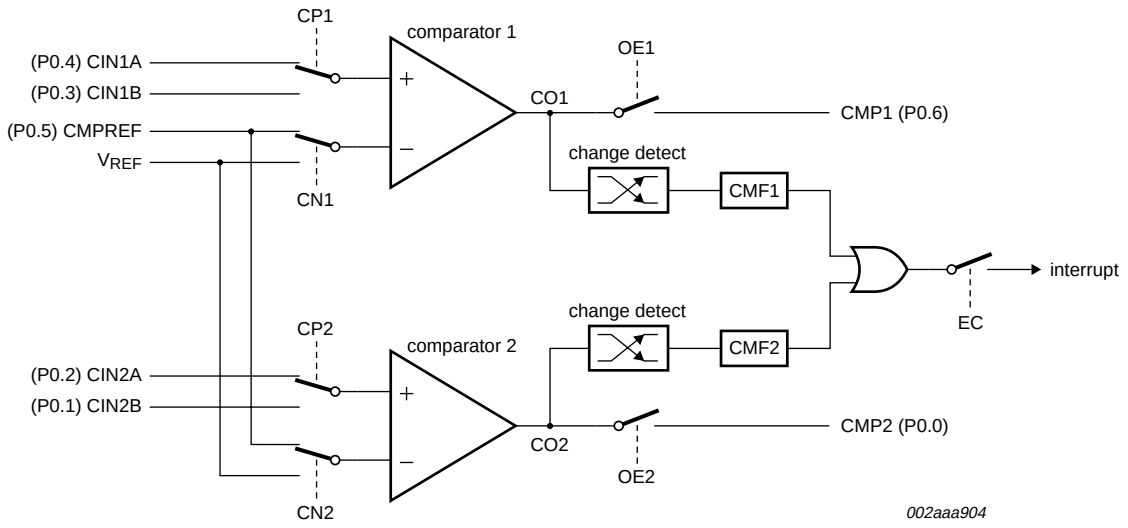


Fig 19. Comparator input and output connections.

7.23.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{REF}, is 1.23 V ± 10 %.

7.23.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

7.23.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

7.24 KBI

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

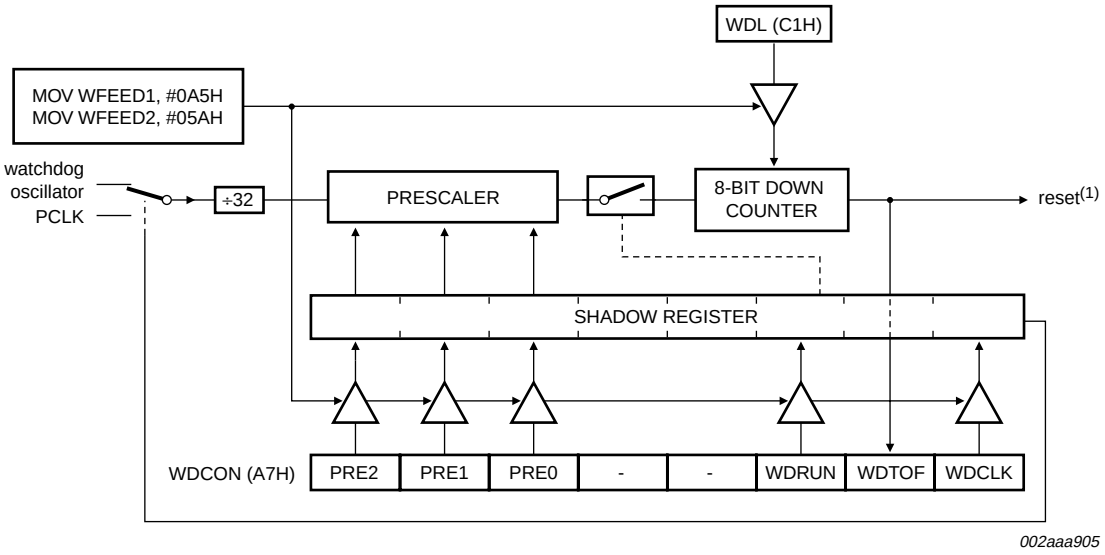
The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

7.25 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 20 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the *P89LPC938 User's Manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 20. Watchdog timer in Watchdog mode (WDTE = '1').

7.26 Additional features

7.26.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.26.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.27 Data EEPROM

The P89LPC938 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- **Byte Mode:** In this mode, data can be read and written one byte at a time.
- **Row Fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00h.
- **Sector Fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00h.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

7.28 Flash program memory

7.28.1 General description

The P89LPC938 Flash memory provides in-circuit electrical erasure and programming. The Flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any Flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. In-Circuit Programming using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC938 Flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC938 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

7.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing In-System Programming via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided Flash loader code to reside anywhere in the Flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the Flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

7.28.3 Flash organization

The program memory consists of eight 1 kB sectors on the P89LPC938 devices. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.28.4 Using Flash as data storage

The Flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

7.28.5 Flash programming and erasing

Four different methods of erasing or programming of the Flash are available. The Flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock/serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The Flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

7.28.6 ICP

In-Circuit Programming is performed without removing the microcontroller from the system. The In-Circuit Programming facility consists of internal hardware resources to facilitate remote programming of the P89LPC938 through a two-wire serial interface. The Philips In-Circuit Programming facility has made in-circuit programming in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC938 User's Manual*.

7.28.7 IAP

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips In-Application Programming has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of Flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00 to FEFF hex, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC938 User's Manual*.

7.28.8 ISP

In-System Programming is performed without removing the microcontroller from the system. The In-System Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC938 through the serial port. This firmware is provided by Philips and embedded within each P89LPC938 device. The Philips In-System Programming facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.28.9 Power-on reset code execution

The P89LPC938 contains two special Flash elements: the Boot Vector and the Boot Status Bit. Following reset, the P89LPC938 examines the contents of the Boot Status Bit. If the Boot Status Bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status Bit is set to a value other than zero, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H.

Table 8 shows the factory default Boot Vector setting for this device. A factory-provided boot loader is pre-programmed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this boot loader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.** A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Table 8: Default Boot Vector values and ISP entry points

Device	Default Boot Vector	Default boot loader entry point	Default boot loader code range	1 kB sector range
P89LPC938	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.28.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC938 User's Manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector (1FH) is changed, it will no longer point to the factory pre-programmed ISP boot loader code. After programming the Flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.29 User configuration bytes

Some user-configurable features of the P89LPC938 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the *P89LPC938 User's Manual* for additional details.

7.30 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC938. Each byte corresponds to one sector. Please see the *P89LPC938 User's Manual* for additional details.

8. A/D converter

8.1 General description

The P89LPC938 has a 10-bit, 8-channel multiplexed successive approximation analog-to-digital converter module. A block diagram of the A/D converter is shown in Figure 21. The A/D consists of an 8-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the SAR drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

8.2 Features

- 10-bit, 8-channel multiplexed input, successive approximation A/D converter.
- Eight result register pairs.
- Six operating modes
  - Fixed channel, single conversion mode
  - Fixed channel, continuous conversion mode
  - Auto scan, single conversion mode
  - Auto scan, continuous conversion mode
  - Dual channel, continuous conversion mode
  - Single step mode
- Three conversion start modes
  - Timer triggered start
  - Start immediately
  - Edge triggered
- 10-bit conversion time of 4 μs at an A/D clock of 9 MHz
- Interrupt or polled operation
- High and Low Boundary limits interrupt; selectable in or out-of-range
- Clock divider
- Power-down mode

8.3 Block diagram

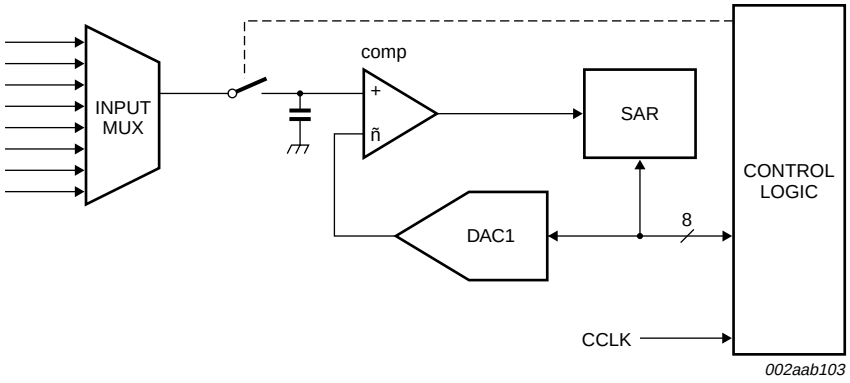


Fig 21. A/D converter block diagram.

8.4 A/D operating modes

8.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register pair which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

8.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the eight result register pairs. The user may select whether an interrupt can be generated after every four or every eight conversions. Additional conversion results will again cycle through the result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

8.4.3 Auto scan, single conversion mode

Any combination of the eight input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel. The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated after the remaining input channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

8.4.4 Auto scan, continuous conversion mode

Any combination of the eight input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel.The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated

after the remaining input channels have been converted. After all selected channels have been converted, the process will repeat starting with the first selected channel. Additional conversion results will again cycle through the eight result register pairs, overwriting the previous results.Continous conversions continue until terminated by the user.

8.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in the result register pair, AD0DAT0R and AD0DAT0L. The result of the conversion of the second channel is placed in result register pair, AD0DAT1R and AD0DAT1L. The first channel is again converted and its result stored in AD0DAT2R and AD0DAT2L. The second channel is again converted and its result placed in AD0DAT3R and AD0DAT3L, etc. An interrupt is generated, if enabled, after every set of four or eight conversions (user selectable).

8.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the eight input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

8.5 Conversion start modes

8.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

8.5.2 Start immediately

Programming this mode immediately starts a conversion.This start mode is available in all A/D operating modes.

8.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

8.6 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

An early detection mechanism exists when the interrupt criteria has been selected to be outside the boundary limits. In this case, after the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion meet the interrupt criteria (i.e., outside the boundary limits) an interrupt will be generated, if enabled. If the four MSBs do not meet the interrupt

criteria, the boundary limits will again be compared after all 8 MSBs have been converted. A boundary status register (BNDSTA0) flags the channels which caused a boundary interrupt.

8.7 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.8 Power-down and Idle mode

In Idle mode the A/D converter, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

9. Limiting values

Table 9: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	operating bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature range		–65	+150	°C
V_{xtal}	voltage on XTAL1, XTAL2 pin to V_{SS}		-	V_{DD} + 0.5	V
$I_{OH(I/O)}$	HIGH-level output current per I/O pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per I/O pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	100	mA
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 9 “Limiting values”

a) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 10 “DC electrical characteristics” and Table 11 “AC characteristics” of this specification are not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

10. Static characteristics

Table 10: DC electrical characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$I_{DD(oper)}$	operating supply current	3.6 V; 12 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	3.6 V; 12 MHz	[2]	-	5	7	mA
$I_{DD(pd)}$	power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[2]	-	55	80	µA
$I_{DD(tpd)}$	total Power-down mode supply current	3.6 V	[3]	-	1	5	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{DDR}	data retention voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	Port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; V_{DD} = 2.4 V – 3.6 V, all ports, all modes except Hi-Z	[4]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V – 3.6 V, all ports, all modes except Hi-Z	[4]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 µA; V_{DD} = 2.4 V – 3.6 V; quasi-bidirectional mode, all ports		V_{DD} – 0.3	V_{DD} – 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V – 3.6 V; push-pull mode, all ports		V_{DD} – 0.7	V_{DD} – 0.4	-	V
		I_{OH} = −20 mA; V_{DD} = 2.4 V – 3.6 V; push-pull mode, all ports		V_{DD} – 1.0	-	-	V
C_{iss}	input capacitance		[5]	-	-	15	pF
I_{IL}	logical 0 input current	V_I = 0.4 V	[6]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}, V_{IH}, V_{th(HL)}$	[7]	-	-	±10	µA
I_{TL}	logical 1-to-0 transition current, all ports	V_I = 1.5 V at V_{DD} = 3.6 V	[8]	−30	-	−450	µA
$R_{RST(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ

Table 10: DC electrical characteristics *...continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, V_{DD} = 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 9 “Limiting values” on page 50 for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] Pin capacitance is characterized but not tested.

[6] Measured with port in quasi-bidirectional mode.

[7] Measured with port in high-impedance mode.

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

11. Dynamic characteristics

Table 11: AC characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified. [1] [2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{OSC(RC)}$	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
$f_{OSC(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(CLK)}$	clock cycle time	see Figure 23	83	-	-	-	ns
f_{CLKLP}	low power select frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 23	33	$T_{cy(CLK)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 23	33	$T_{cy(CLK)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 23	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 23	-	8	-	8	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time	see Figure 22	16 $T_{cy(CLK)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 22	13 $T_{cy(CLK)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 22	-	$T_{cy(CLK)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 22	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 22	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	2.0 MHz (slave)		0	$^{CCLK}/_{6}$	0	2.0	MHz
	3.0 MHz (master)		-	$^{CCLK}/_{4}$	-	3.0	MHz
t_{SPICYC}	SPI cycle time	see Figure 24, 25, 26, 27					
	2.0 MHz (slave)		$^{6}/_{CCLK}$	-	500	-	ns
	3.0 MHz (master)		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 26, 27					
	2.0 MHz (slave)		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 26, 27					
	2.0 MHz (slave)		250	-	250	-	ns

Table 11: AC characteristics *...continued*

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified. [1] [2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 24, 25, 26, 27					
	3.0 MHz (master)		$^{2}/_{CCLK}$	-	165	-	ns
	2.0 MHz (slave)		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 24, 25, 26, 27					
	3.0 MHz (master)		$^{2}/_{CCLK}$	-	165	-	ns
	2.0 MHz (slave)		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 26, 27					
	2.0 MHz (slave)		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 26, 27					
	2.0 MHz (slave)		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 24, 25, 26, 27					
	2.0 MHz (slave)		-	240	-	240	ns
	3.0 MHz (master)		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 24, 25, 26, 27	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Table 12: AC characteristics

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified. [1] [2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{OSC(RC)}$	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
$f_{OSC(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(CLK)}$	clock cycle time	see Figure 23	55	-	-	-	ns
f_{CLKLP}	low power select frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 23	22	$T_{cy(CLK)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 23	22	$T_{cy(CLK)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 23	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 23	-	5	-	5	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time	see Figure 22	$16T_{cy(CLK)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 22	$13T_{cy(CLK)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 22	-	$T_{cy(CLK)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 22	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 22	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	3.0 MHz (slave)		0	$^{CCLK}/_{6}$	0	3.0	MHz
	4.5 MHz (master)		-	$^{CCLK}/_{4}$	-	4.5	MHz
t_{SPICYC}	SPI cycle time	see Figure 24, 25, 26, 27					
	3.0 MHz (slave)		$^{6}/_{CCLK}$	-	333	-	ns
	4.5 MHz (master)		$^{4}/_{CCLK}$	-	222	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 26, 27					
	3.0 MHz (slave)		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 26, 27					
	3.0 MHz (slave)		250	-	250	-	ns

Table 12: AC characteristics *...continued*

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified. [1] [2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 24, 25, 26, 27					
	4.5 MHz (master)		$^{2}/_{CCLK}$	-	111	-	ns
	3.0 MHz (slave)		$^{3}/_{CCLK}$	-	167	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 24, 25, 26, 27					
	4.5 MHz (master)		$^{2}/_{CCLK}$	-	111	-	ns
	3.0 MHz (slave)		$^{3}/_{CCLK}$	-	167	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 26, 27					
	3.0 MHz (slave)		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 26, 27					
	3.0 MHz (slave)		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 24, 25, 26, 27					
	3.0 MHz (slave)		-	160	-	160	ns
	4.5 MHz (master)		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 24, 25, 26, 27	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

11.1 Waveforms

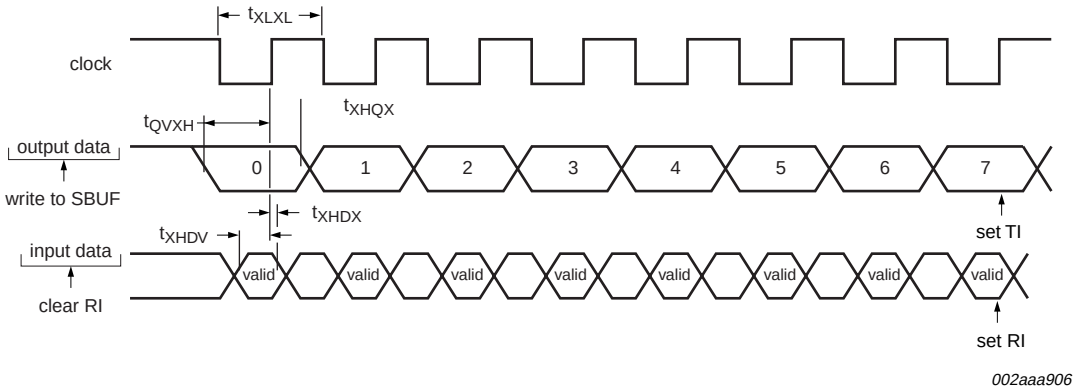


Fig 22. Shift register mode timing.

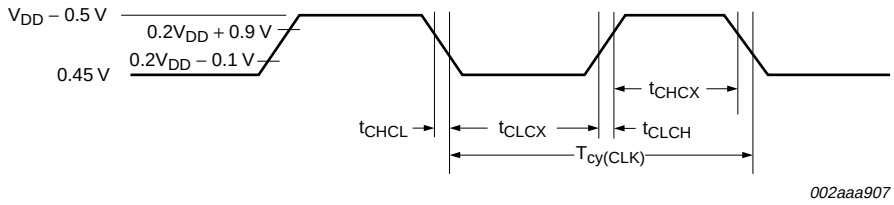


Fig 23. External clock timing.

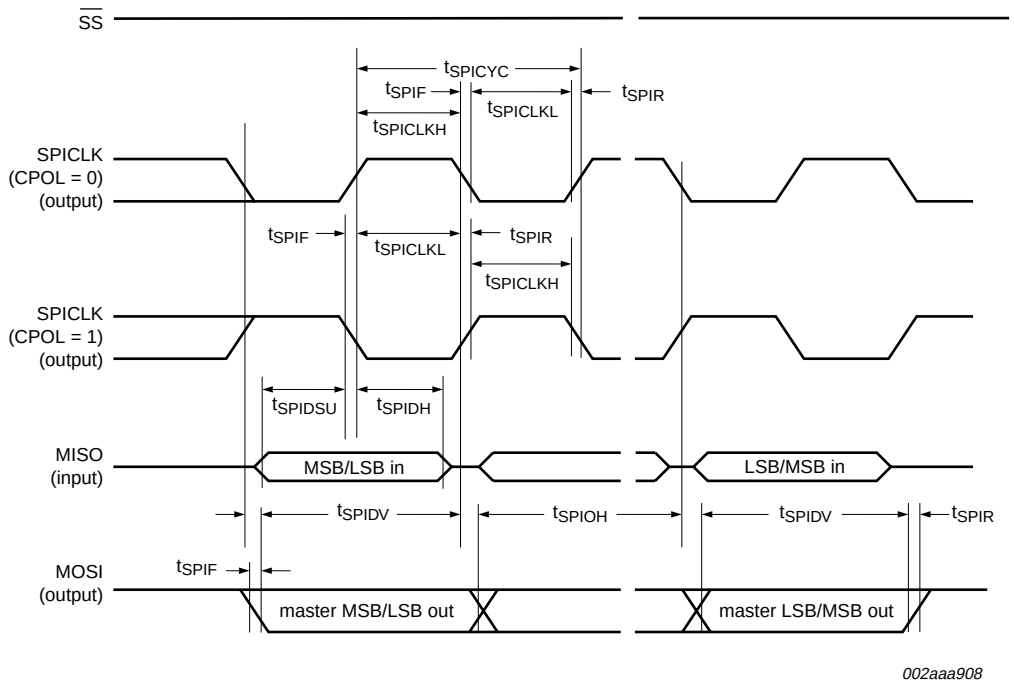


Fig 24. SPI master timing (CPHA = '0').

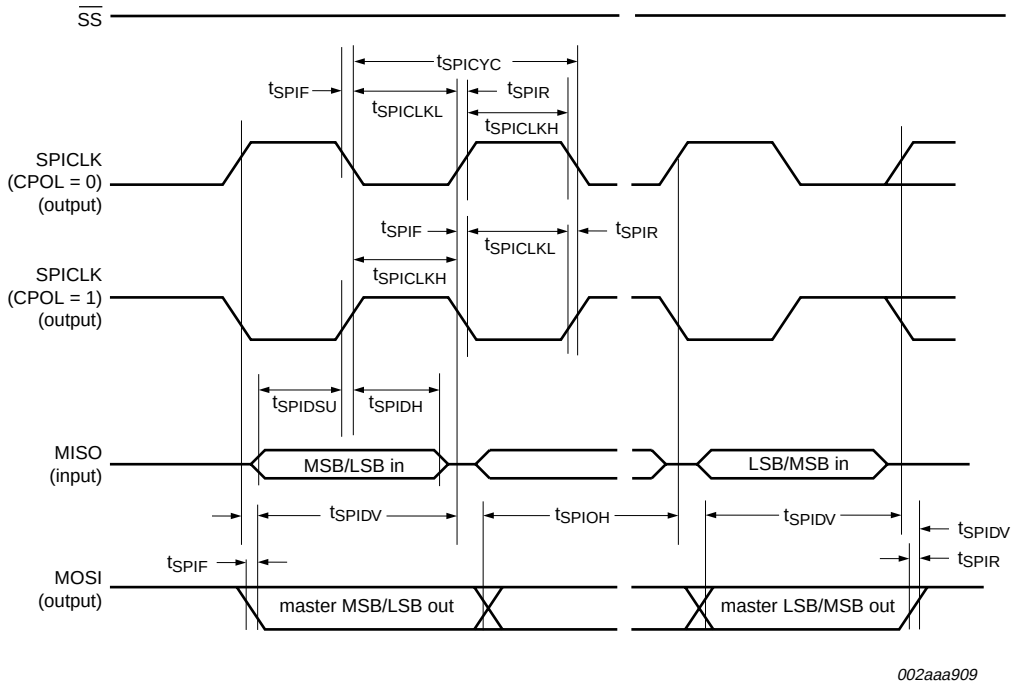


Fig 25. SPI master timing (CPHA = '1').

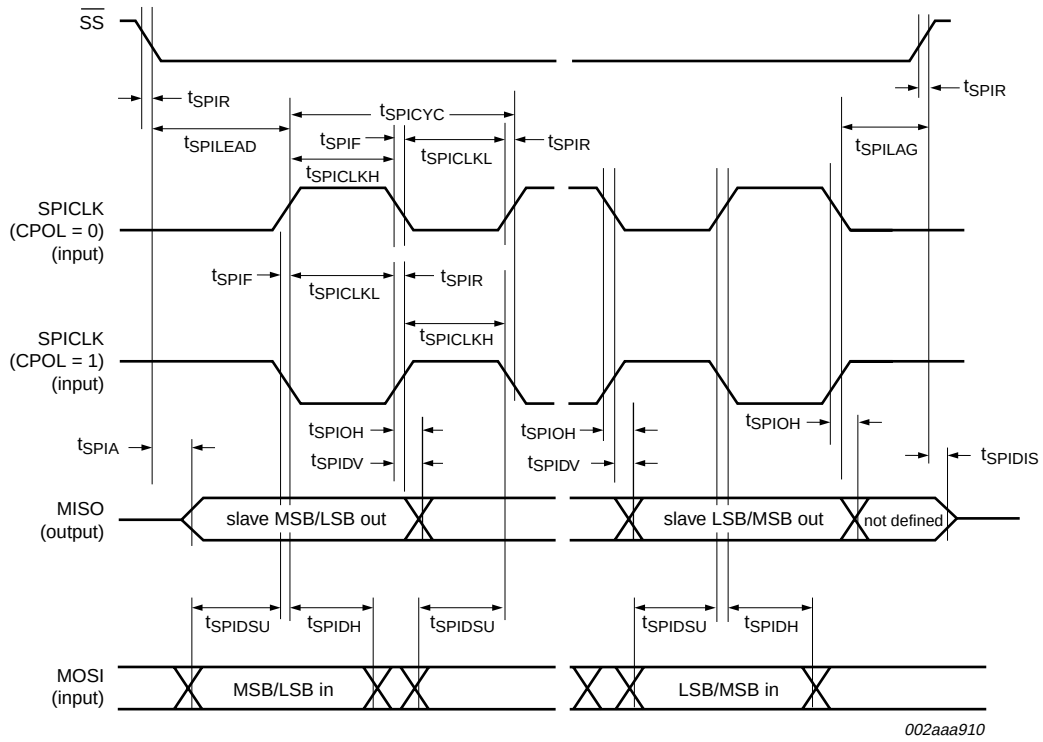


Fig 26. SPI slave timing (CPHA = '0').

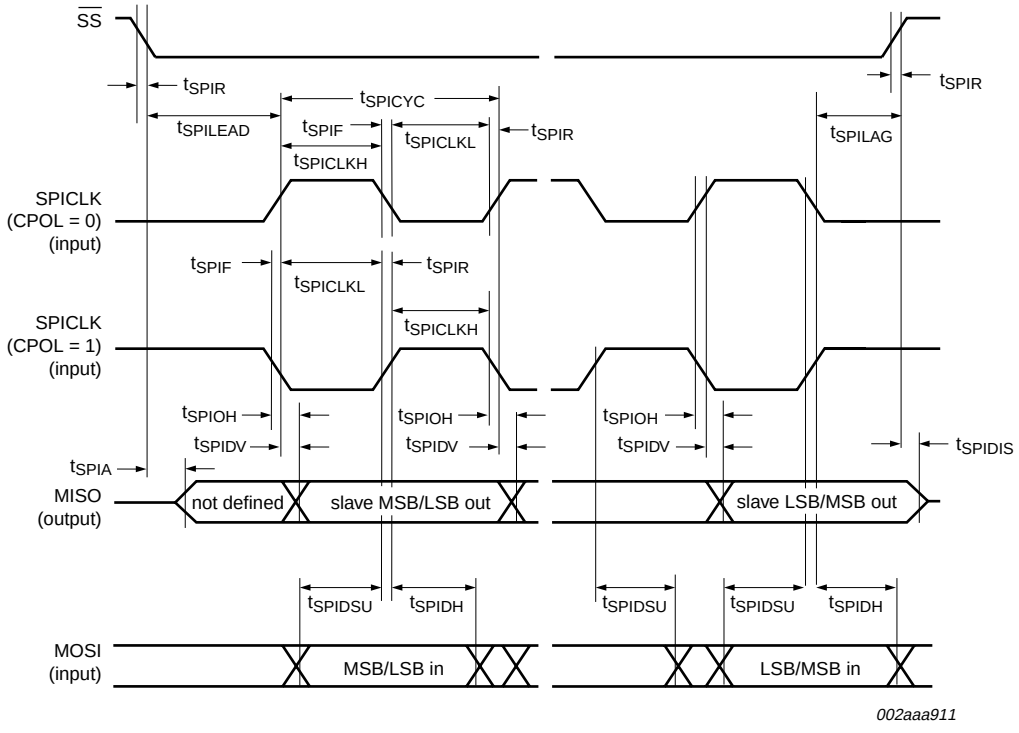


Fig 27. SPI slave timing (CPHA = '1').

11.2 ISP entry mode

Table 13: AC characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{RST}$ delay from V_{DD} active time		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

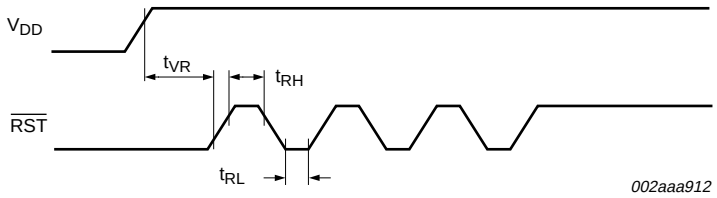


Fig 28. ISP entry waveform.

12. Other characteristics

12.1 Comparator electrical characteristics

Table 14: Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IO}	offset voltage input voltage			-	-	±20	mV
V_{IC}	common mode input voltage			0	-	V_{DD} − 0.3	V
CMRR	common mode rejection ratio		[1]	-	-	−50	dB
$t_{res(tot)}$	total response time			-	250	500	ns
$t_{(CE-OV)}$	comparator enable to output valid time			-	-	10	µs
I_{LI}	input leakage current	$0 < V_I < V_{DD}$		-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

12.2 A/D converter electrical characteristics

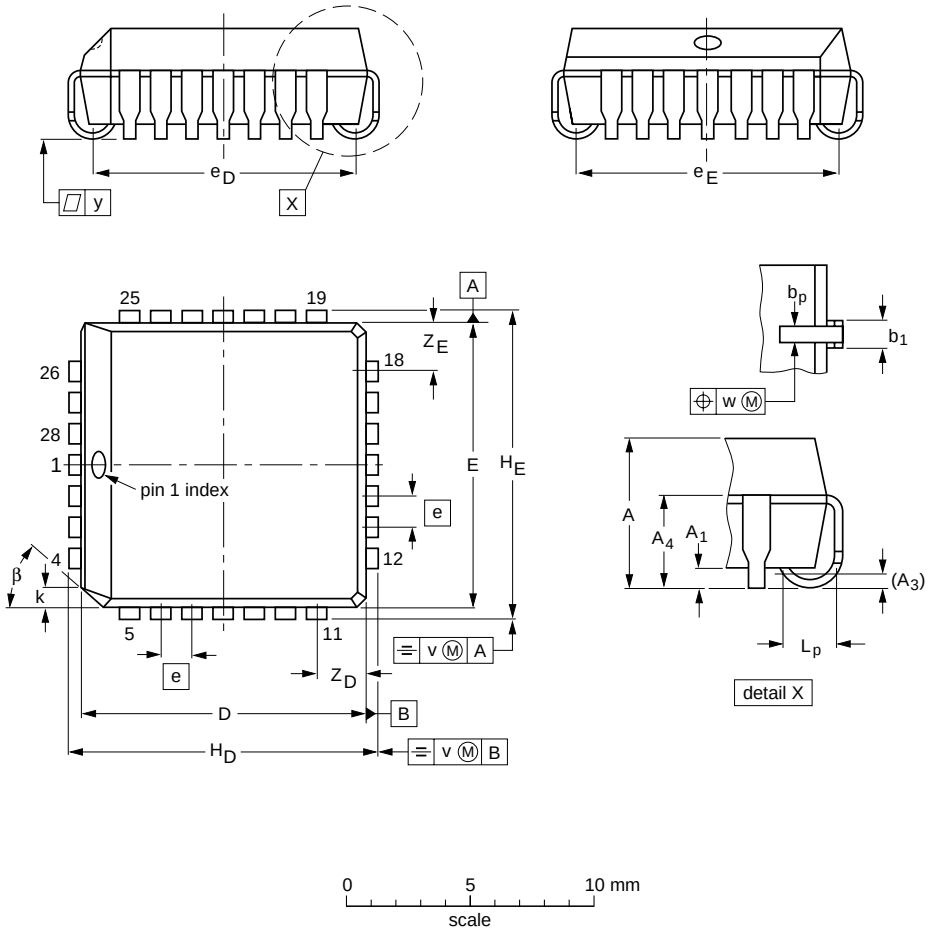
Table 15: A/D converter electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		V_{SS} − 0.2	-	V_{SS} + 0.2	V
C_{iss}	analog input capacitance		-	-	15	pF
E_D	differential non-linearity		-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		-	-	±1	LSB
E_O	offset error		-	-	±2	LSB
E_G	gain error		-	-	±1	%
$E_{u(tot)}$	total unadjusted error		-	-	±2	LSB
M_{CTC}	channel-to-channel matching		-	-	±1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 kHz to 100 kHz	-	-	−60	dB
SR_{in}	input slew rate		-	-	100	V/ms
$T_{cy(ADC)}$	ADC clock cycle		111	-	3125	ns
t_{ADC}	conversion time	A/D enabled	-	-	$36T_{cy(ADC)}$	µs

13. Package outline

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

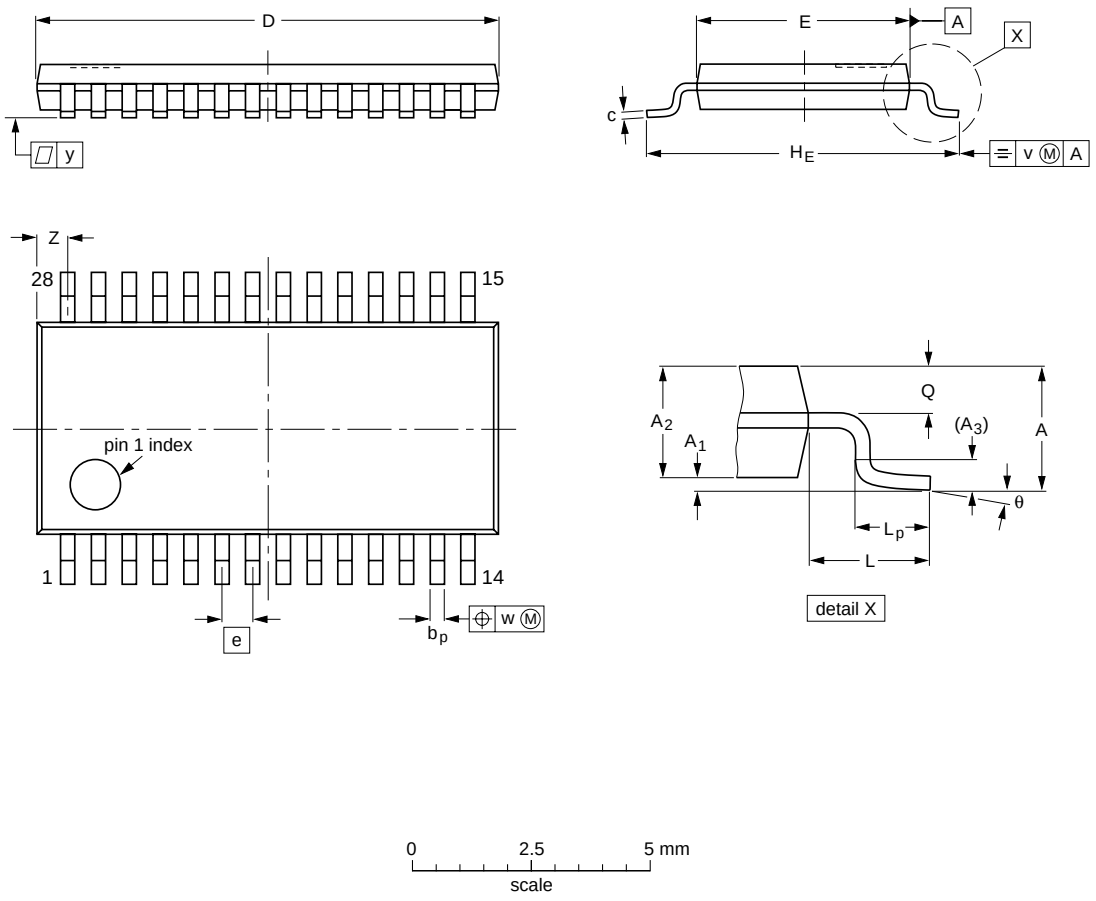
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 29. Package outline SOT261-2 (PLCC28).

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

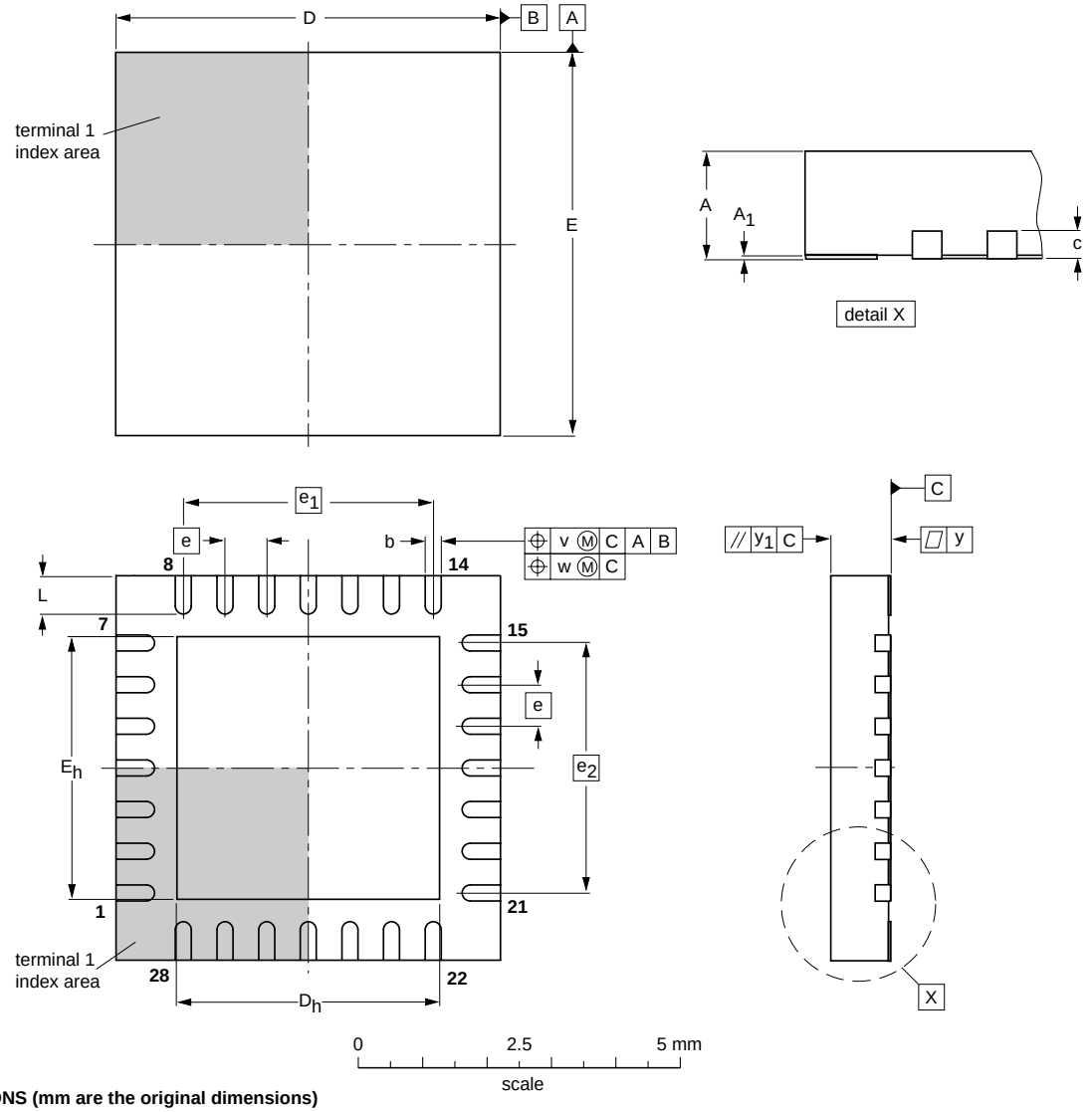
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 30. Package outline SOT361-1 (TSSOP28).

HVQFN28: plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 6 x 6 x 0.85 mm **SOT788-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.35 0.25	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.65	3.9	3.9	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT788-1	- - -	MO-220	- - -			02-10-22

Fig 31. Package outline SOT788-1 (HVQFN28).

14. Abbreviations

Table 16: Acronym list

Acronym	Description
A/D	Analog to Digital
ADC	Analog to Digital Converter
CCU	Capture/Compare Unit
CPU	Central Processing Unit
DAC	Digital to Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
IAP	In-Application Programming
ICP	In-Circuit Programming
ISP	In-System Programming
LED	Light Emitting Diode
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

15. Revision history

Table 17: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
P89LPC938_1	20050225	Product data sheet	-	9397 750 14051	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Contents

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