Universidad Zaragoza

Year : 2020/21

60959 - Advanced digital systems

Syllabus Information

Academic Year: 2020/21
Subject: 60959 - Advanced digital systems
Faculty / School: 110 - Escuela de Ingeniería y Arquitectura
Degree: 623 - Master's Degree in Telecommunications Engineering
ECTS: 6.0
Year: 1
Semester: First semester
Subject Type: Compulsory
Module: ---

1.General information

1.1.Aims of the course

1.2.Context and importance of this course in the degree

1.3.Recommendations to take this course

2.Learning goals

2.1.Competences

2.2.Learning goals

2.3.Importance of learning goals

3.Assessment (1st and 2nd call)

3.1.Assessment tasks (description of tasks, marking system and assessment criteria)

4.Methodology, learning tasks, syllabus and resources

4.1.Methodological overview

Once students finish this course, they should have an in-depth knowledge of digital integrated circuit hardware design. The emphasis is on FPGA technology, but most of the design techniques can also be applied to ASIC devices. The student should be familiar with the latest state-of-the-art system on chip (SoC) design methodologies, including high-level synthesis. Students should be able to learn the benefits and drawbacks of the various design methods for solving a problem. Through practical assignments, experience will be achieved from both using tools as well as designing their own system.

4.2.Learning tasks

The course includes the following learning tasks:

- **Lectures** (30 hours). Students are expected to attend all lectures, pay attention and participate in class discussions.
- **Lab sessions** (25 hours). The course will include 12 lab sessions that allow students to design, implement, test, and evaluate several small communication blocks. Students are expected to work in pairs. It is suggested that students form a group at the beginning of the course and keep in the same group throughout the semester.

4.3.Syllabus

The course will address the following topics:

- Topic 1. Advanced VHDL coding
- Topic 2. High Level Synthesis
- Topic 3. System on Chip design
- Topic 4. ASIC design flow

4.4.Course planning and calendar

Further information concerning the timetable, classroom, office hours, assessment dates and other details regarding this course, will be provided on the first day of class or please refer to the EINA website.

4.5.Bibliography and recommended resources

http://biblos.unizar.es/br/br_citas.php?codigo=60959&year=2020