TESIS DE LA UNIVERSIDAD DE ZARAGOZA

2021

187

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ISSN 2254-7606

Prensas de la Universidad Universidad Zaragoza

ISSN 2254-7606

Universidad Zaragoza
1542

Tesis Doctoral

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UNIVERSIDAD DE ZARAGOZA
Escuela de Doctorado

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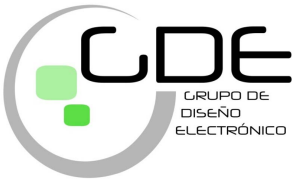

DESIGN OF CMOS TRANSIMPEDANCE AMPLIFIERS FOR REMOTE ANTENNA UNITS IN FIBER-WIRELESS SYSTEMS

A thesis submitted to the University of Zaragoza
in partial fulfillment of the requirements for
the Degree of Doctor of Philosophy in Physics

By
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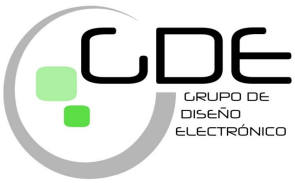

Zaragoza, January 2021

DISEÑO DE AMPLIFICADORES DE TRANSIMPEDANCIA PARA UNIDADES DE ANTENA REMOTA EN SISTEMAS FIBRA-INALÁMBRICO

Tesis presentada a la Universidad de Zaragoza
para optar al grado de
Doctor en Física

Por
Guillermo Royo Calderón

Bajo la dirección de los doctores
Dr. Santiago Celma Pueyo
Dra. Concepción Aldea Chagoyen

Grupo de Diseño Electrónico – I3A
Departamento de Ingeniería Electrónica y Comunicaciones
Facultad de Ciencias – Universidad de Zaragoza

Zaragoza, enero 2021

Publicaciones

La presente tesis doctoral recoge los resultados de trabajos de investigación que han sido previamente publicados en revistas científicas indexadas. A continuación, se listan las cuatro referencias bibliográficas seleccionadas para poder defender la tesis doctoral en la modalidad de compendio de publicaciones.

[ROY20a] Royo, G.; Sánchez-Azqueta, C.; Aldea, C.; Celma, S. High-sensitivity large-area photodiode read-out using a divide-and-conquer technique. *Sensors*, 2020, 20(21), 6316. doi: 10.3390/s20216316
Q1 en Instruments & Instrumentation. Factor de impacto 3.275

[ROY19a] Royo, G.; Martínez-Pérez, A.D.; Sánchez-Azqueta, C.; Aldea, C.; Celma, S. A highly linear low-noise transimpedance amplifier for indoor fiber-wireless remote antenna units. *Electronics*, 2019, 8(4), 437. doi:10.3390/electronics8040437
Q2 en Engineering, Electrical & Electronic. Factor de impacto 2.412

[ROY18a] Royo, G.; Sánchez-Azqueta, C.; Martínez-Pérez, A.D.; Aldea, C.; Celma, S. Fully-differential transimpedance amplifier for reliable wireless communications. *Microelectronics Reliability*, 2018, 83, 25-28. doi: 10.1016/j.microrel.2018.02.007
Q3 en Engineering, Electrical & Electronic. Factor de impacto 1.483

[ROY17a] Royo, G.; Sánchez-Azqueta, C.; Gimeno, C.; Aldea, C.; Celma, S. Programmable low-power low-noise capacitance to voltage converter for MEMS accelerometers. *Sensors*, 2017, 17(1), 67. doi: 10.3390/s17010067
Q2 en Instruments & Instrumentation. Factor de impacto 2.475

El desarrollo de esta tesis se enmarca en el estudio de sistemas mixtos fibra-inalámbrico para su uso en sistemas de antenas distribuidas (DAS). Los DAS se presentan como una solución a las necesidades que van a demandar en un futuro los sistemas de comunicaciones. A lo largo de este manuscrito, se proponen y estudian varias soluciones y aplicaciones de distintos amplificadores de transimpedancia (TIA), partiendo de la base teórica hasta alcanzar el diseño y fabricación de los bloques fundamentales de la unidad de antena remota (RAU) en tecnología CMOS.

El amplio abanico de aplicaciones de los TIAs en comunicaciones y en otros campos ha constituido la motivación del estudio e implementación de este bloque específico en diferentes arquitecturas de RAU, así como de la exploración de su uso para otro tipo de aplicaciones, tales como sensores capacitivos en acelerómetros micro electromecánicos (MEMS).

A mi familia

Agradecimientos

Me gustaría expresar mi agradecimiento a aquellas personas que me han acompañado a lo largo de estos años y que me han dado la fortaleza necesaria para conseguir realizar esta tesis. Todos me habéis ayudado a llegar aquí y con estas palabras os doy las gracias.

En primer lugar, quiero dar las gracias a mis directores, Concha y Santiago. Les agradezco su apoyo incondicional de principio a fin, en especial en los momentos más difíciles, en los que me han ayudado a centrarme, a seguir adelante y a alcanzar objetivos que no habrían sido posibles sin ellos.

A Pedro, que desde primera hora cada día y con un enérgico “buenos días” me ha dado ánimos y consejos más que valiosos. A Pepe, por mantenerme alerta para escuchar sus tonos de llamada religiosamente actualizados. A Nicolás y Belén, por ayudarme cuando les he necesitado, por hacer los días más amenos, gracias por ponerle el punto de humor a las reuniones y gracias Nicolás por tus recomendaciones cinematográficas tan características. A Óscar, Javi, Erick, Cecilia, Dani, Antonio, Guillermo y Carlos, por animar el despacho y compartir vuestro tiempo de descanso conmigo. A Jorge y Alejandro, por mostrarme otra perspectiva y aguantar nuestras penas mutuamente en la cafetería.

Gracias a mis compañeros de despacho, a Miguel por estar siempre disponible para dedicarme cinco minutos cuando los he necesitado, incluso en los momentos más complicados ha sido capaz de sacar tres minutos para poner las cosas en blanco y negro sin sacarnos de nuestras casillas y a Adrián, por ser la élite escribiendo *papers*, por su lucha incesante por buscar la verdad y enseñarnos el camino a sus compañeros de despacho.

A María, que me ha aguantado más que nadie para conseguir centrarme en terminar la tesis cuando más cuesta arriba estaba. Gracias por confiar en mí y no rendirte, gracias por todo lo que hemos vivido y viviremos juntos.

A mi familia, gracias. Gracias a mi padre, Miguel Ángel, que siempre me ha apoyado en mis decisiones y me ha empujado a seguir hacia delante para lograr mis metas. Gracias a mi hermana, Sara, que siempre se ha preocupado por mí, gracias por los buenos ratos que hemos pasado juntos toda la vida.

Por último, agradezco también a todas las instituciones que han financiado este trabajo: Ministerio de Economía y Competitividad del Gobierno de España y Fondo Europeo de Desarrollo Regional a través de los proyectos TEC2014-52840-R, TEC2017-86867-R y BES-2015-073748 y al Grupo de Diseño Electrónico (T26_20R).

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List of Symbols

A	Open-loop gain of an amplifier
A_d	Differential open-loop gain of an amplifier
c	Speed of light $(2.998 \cdot 10^8\ m/s)$
C_{in}	Input-node capacitance
C_{out}	Output-node capacitance
C_{PD}	Intrinsic junction capacitance of a photodiode
f_c	Corner frequency
g_m	MOS transistor transconductance $(\delta I_D/\delta V_{GS})$
h	Plank constant $(6.626 \cdot 10^{-34}\ J \cdot s)$
$\overline{i^2{}_{n,in}}$	Input-referred noise-current spectral density
$\overline{i^2{}_{n,PD}}$	Noise-current spectral density of a PD
$\overline{i^2{}_{n,R}}$	Noise-current spectral density of a resistor
I_{MD}	Monitoring current through a monitor PD
I_{PD}	Current through a photodiode
I_{TH}	Threshold current
g_m	Transconductance of a MOS transistor
k_B	Boltzmann's constant $(1.38 \cdot 10^{-23}\ J/K)$
P_{op}	Optical power
q	Elementary charge $(1.602 \cdot 10^{-19} C)$
Q	Quality factor of a second order response
r_o	Channel-length modulation resistance of a MOS transistor
R_{in}	Input resistance
R_F	Feedback resistance
R_L	Load resistor

R_{PD}	Photodiode's flux responsivity
R_{SH}	Shunt resistance of a photodiode
R_T	DC transimpedance
S	Sensitivity of an optical receiver
S_T	Sensitivity of a capacitive accelerometer sensor
T	Temperature
$\overline{v_{n,A}^2}$	Input-referred voltage noise of an amplifier
Z_T	Transimpedance
γ	Bulk-threshold constant
η	Quantum efficiency of photon-to-electron conversion
η_e	Efficiency of the current to optical power conversion
λ	Wavelength
ω_0	Natural frequency of oscillation
ω_{3dB}	3-dB attenuation frequency
ω_A	Dominant pole frequency of an amplifier
ω_c	Carrier frequency
ω_T	Resonance frequency of a MEMS accelerometer

List of Acronyms

AM	Amplitude modulation
APD	Avalanche photodiode
BBoF	Baseband over fiber
BER	Bit error ratio
BS	Base station
BW	Bandwidth
CAGR	Compound annual growth rate
CATV	Community access television
CG	Common gate
CMOS	Complementary metal-oxide-semiconductor
CNR	Carrier-to-noise ratio
CS	Common source
DAS	Distributed antenna system
DFB	Distributed feedback
DUT	Dispositive under test
EIN	Equivalent input noise
EMI	Electromagnetic interferences
EO	Electro-optical
EVM	Error vector magnitude
FoM	Figure of merit
FP	Fabry-Pérot
GOF	Glass optical fiber
IC	Integrated circuits
IFoF	Intermediate frequency over fiber
IoT	Internet of things

IQ	Quadrature signal
IRR	Image rejection ratio
ISI	Inter-symbol interferences
LED	Light-emitting diode
LNA	Low noise amplifier
LO	Local oscillator
MEMS	Micro electromechanical system
MMF	Multimode fiber
MIMO	Multiple input multiple output
MOS	Metal-oxide-semiconductor
MZM	Max-Zender modulator
NRZ	Non-return-to-zero
OE	Opto-electrical
OFDM	Orthogonal frequency division multiplexation
OLT	Optical line termination
OMI	Optical modulation index
ONT	Optical network terminal
NFC	Near field communication
NRZ	Non-return-to-zero
PA	Power amplifier
PAM	Pulse-amplitude modulation
PCB	Printed-circuit board
PD	Photodiode
PGA	Programmable gain amplifier
PIN	P region – Insulator – N region
PM	Phase modulation
POF	Polymer optical fiber
PON	Passive optical network

PRBS	Pseudo-random bit sequence
PVT	Process, voltage, and temperature
QAM	Quadrature amplitude modulation
RAU	Remote antenna unit
RBS	Random binary sequence
RF	Radio frequency
RFoF	Radio over fiber
SNR	Signal-to-noise ratio
TIA	Transimpedance amplifier
VCSEL	Vertical-cavity surface-emitting LED
VGA	Variable gain amplifier
VSA	Vector signal analyzer
VSG	Vector signal generator
VVA	Variable voltage attenuator
WDM	Wavelength division multiplexation
WiFi	Wireless fidelity
WLAN	Wireless local area network

1 Introduction

The advances in technology and the effort for the development of new communication systems have been constantly growing at the rate of the increasing demand of information in the world over the last decades. Since the Internet took its place in modern society, global data traffic has grown exponentially, and an incredible number of applications and content have been created.

The arrival of fiber optics allowed the achievement of significant advances in communications since the glass optical fiber (GOF) was the key to create broadband long-haul communication networks. The main advantages of fiber-optic communication systems are a very low attenuation and a very high modulation capacity, which means a wide bandwidth (BW) that allows the transmission of data to very long distances at much higher bitrates than any other wire-based communication system [GAG76, KEI03].

The advances in the fabrication of integrated circuits (ICs) and high-speed photonic devices manufacturing has driven the development of high-performance optical systems, increasing communication data rates up to the channel BW limitation. With the need of higher bitrates in the already deployed fiber-optic networks, there has been a recent development of new optical communication systems [ARM09]. These employ more complex signal modulation schemes, which allow higher bitrates within the same BW. These new transmission methods have different and more stringent performance requirements, such as higher dynamic range or linearity. Consequently, high-performance optical front-ends must be available to bring these key characteristics together.

Furthermore, a great increase in demand of information is expected to come in the immediate future [AGR16, SUM15]. Therefore, a great effort must be made in the development of new communication systems for both long-haul and short-distance communications since the demand of this kind of applications is growing at a dizzying pace. Technologies such as 5G or Internet of Things (IoT) are knocking at the door and already starting to be a reality (Fig. 1.1).

Fig. 1.1. Recreation of a Smart City with everyone and everything interconnected.

As global data traffic increases over the last years, simultaneously, wireless technology has been strongly consolidated and the use of wireless and mobile devices is rapidly growing. We live in the era of ubiquitous communication, where high data capacity at high data transmission rates and good accessibility is demanded. Therefore, the new communication scenario will require broadband wireless communication systems, forcing to increase both their transmission capacity and coverage while showing higher immunity to interferences. These improvements will be very challenging, especially in densely populated areas, where many wireless networks concur, and a tremendous amount of high-speed wireless links must share a reduced space.

Wireless data demand has grown exponentially over the last years, along with the enormous proliferation of wireless devices and the unstoppable increase of multimedia content transmission demand. According to the Cisco Annual Internet Report (2018-2023), the global mobile devices and connections will grow to 13.1 billion by 2023 at a compound annual growth rate (CAGR) of 8 percent, while mobile machine-to-machine connections will grow to 4.4 billion at a 30 percent [CIS20].

This immense growth rate entails several difficulties associated with data storage, access, and content preservation. Moreover, the new IoT paradigm is adding an even higher demand in this scenario and consequently, even though there are continuous technological advances in this field, the radiofrequency (RF) spectrum is close to saturating despite the recently introduced normative and restrictions [CIS20]. In addition, there is a huge energy demand associated with data transportation which grows as data traffic increases. Therefore, the development of

highly energy-efficient communication technologies is driving research in this field, being an international priority to reduce the impact of climate change.

The convergence of wireless communications and fiber optic systems has emerged as a promising solution to support the rate of growth of data traffic demand for wireless applications. This approach can be a good candidate either for indoor or outdoor applications, combining the best of these technologies: the mobility of wireless technologies and the low attenuation and high capacity of optical fibers. Therefore, whether it is for long-haul or short-distance connections, fiber-wireless communication systems must evolve and improve their characteristics to lead the development and progress in our increasingly interconnected society.

This first chapter presents an introduction to distributed antenna systems (DAS) and studies its main subsystems and their fundamental design blocks and key devices. After that, a study of the three main DAS communication configurations is made, with the purpose of giving a background and a motivation to the design of the analog front-ends proposed in this thesis. Finally, the motivation and objectives, and a summary of the methodology and thesis organization are provided.

1.1 Distributed Antenna Systems

The upcoming IoT technological frontier arouses enormous interest both in research and in its commercial development. Essentially, its deployment potential depends on the available wireless connectivity, and thus several attempts have been made to adapt the new IoT applications to existing wireless solutions. However, there is a consensus that due to the enormous amount of potential IoT applications (home automation, security, wearables, sensor networks, industrial automation, machine-to-machine, precision agriculture, remote surveillance, or the so-called Smart City among others) there is no single standard capable of satisfying the needs of each one, in terms of complexity, cost, power consumption, and transmission speed [BEC16].

Now, it is still unclear which technologies will take over to meet the increased connectivity demand in the long run, allowing the huge BW consumption of future 5G networks that are already being deployed. Research is underway in different areas because possible solutions will require the concurrence of various technologies [NOR17]. For example, an obvious solution to the saturation of the radio frequency spectrum is to expand its use up to millimeter waves (30 to 300 GHz), a range that has the advantage of being unused and offering channels with enormous capacity. However, a tremendous effort must be made to design and manufacture communication systems at such frequencies, which also suffer a very high attenuation when propagating through air. To solve this limitation, new urban-area networks with high density of base stations (smallcells) must be available. These cells have the advantage of compact sizing, thanks to the very short wavelength of millimetric waves, which facilitates their deployment. Additionally, these cells will work with hundreds of input/output channels in the near future, creating massive multiple-input multiple-output (MIMO) networks. MIMO is one of the most promising approaches to achieve higher data capacity, however, the main challenge is to minimize the antenna interferences. Therefore, techniques such as beamforming, which consists of radiating with high directivity, using algorithms able to determine the optimal transmission path, or technologies such as full duplex must be employed, so that the reachable distance of the millimeter waves transmission can be increased, with higher throughput and interference free [ROH14, HAS17, SOH17].

While the new telecommunications scenario is still being configured, there is no doubt that among the most used standards for the implementation of IoT (WiFi, Bluetooth, ZigBee, Thread, SigFox, NFC ...), the WiFi standard is the preferred option and with greater development potential [AYY16, BEC16, FES15, GAL15, RAP17]. In fact, there are many predictions that coincide in pointing out that the role played by the WiFi standard in IoT systems, currently already relevant, will become

more important over time and will become the dominant option in the medium term [DIG16, PAR17]. Since its introduction in 1997, the 802.11 standard has evolved to become a family of standards operating in the 2.4 GHz (802.11b / g / n) and 5 GHz (802.11a / n / ac) bands, offering data transmission rates exceeding 1 Gb/s (802.11ac) with MIMO systems. This versatility is currently driving the research of new versions within the family of the WiFi standard to adapt it to IoT networks but maintaining a common framework that allows interoperability and facilitates design cycles. The industry forecasts a progressive implementation of the 5 GHz WiFi ac standard until 2021 and subsequently a coexistence with other 60 GHz WiFi versions (802.11ad) with a theoretical speed of 4.6 Gb/s, and of progressive implementation from 2024 [ITR15].

An efficient solution to solve the problem of saturation of the radio spectrum in which WiFi standards operate is the use of low-power access nodes in increasingly higher frequency bands. The reduction in coverage area is compensated by a greater deployment of access points. In other words, instead of using 2.4-GHz base stations with maximum coverage, which is a source of interference in high-density networks, this approach consists of a dense number of low-coverage base stations, preferably working at 5 GHz. Therefore, they show less susceptibility to interference, which is a major problem in densely populated areas, where many wireless networks concur, and it can be very difficult to achieve high data transmission rate [PAR20a]. In this context, the convergence of wireless communications and fiber optic systems can become a promising technique to provide broadband wireless access services, in a range of applications that support the growing demand for wireless data traffic, either indoor or outdoor, combining the best of both technologies: the mobility of wireless systems and the low attenuation and high capacity of optical fibers in a world where high-speed connectivity is required anytime, anywhere [GOM08, KOO08, LIM10, VYA12].

Over the last few years, mixed fiber-wireless communication systems such as DAS fed by multi-mode fibers (MMF) are gaining attention as probably the most promising solution to achieve efficient, cost-effective and high-capacity transmissions in short-range communications [NII04, SAL87, ZHA07]. These systems are flexible and there is a good compromise between data capacity, accessibility, and the overall cost of installation and maintenance, allowing for a good convergence of optical fiber capacity and wireless access flexibility. In this approach, the signal is generated and processed in a base station (BS) and is distributed through MMF to several remote antenna units (RAU), which provide an optical-wireless interface (Fig. 1.2) [LIM10].

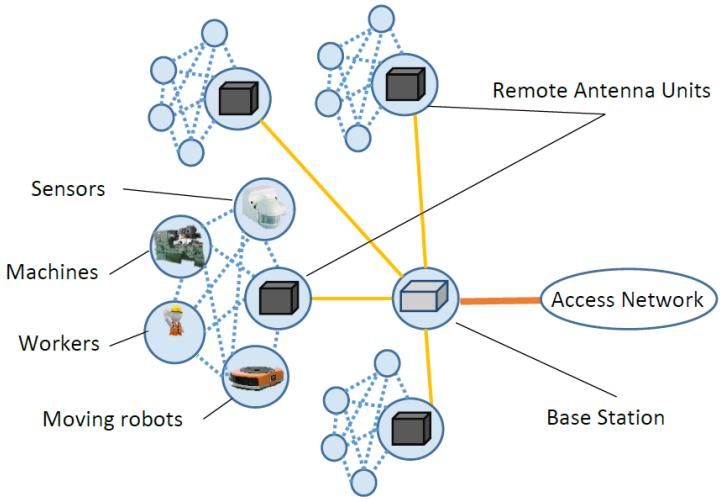

Fig. 1.2. Conceptual scheme of a distributed antenna system in industrial environments.

As Fig. 1.3 shows, the RAU is the link between the BS and the wireless device, and it consists of a downlink and an uplink stream. The downlink receives the optical signal from the BS and the uplink transmits another optical signal in the opposite way, back to the BS. In contrast to traditional wireless networks that consist of broadcasting the signal from a single transmitter, this approach offers much better coverage and data capacity while reducing interferences with other wireless networks [VYA12].

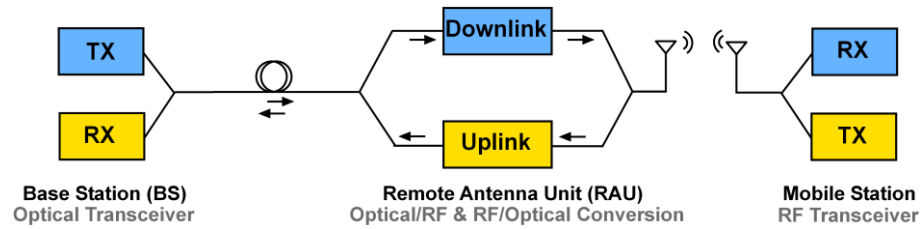

Fig. 1.3. Conceptual scheme of a remote antenna unit (RAU) in a distributed antenna system (DAS).

The key to a DAS is to employ highly energy-efficient and cost-effective components in the three main elements of the communication system. This is achieved with the use of MMF, which presents immunity to electromagnetic interferences (EMI) and offers a large BW, and therefore a very high data capacity, along with cost-effective photonic devices, such as vertical-cavity surface-emitting lasers (VCSEL). However, as mentioned above, to ensure a high data capacity and good coverage, a dense network of RAU is needed, hence a low-cost, low-power fully integrated RAU must be designed with moderate complexity and in digital technologies such as CMOS to obtain a cost-effective DAS.

1.1.1 Uplink Front-End

Now, the principle of operation of electrical-optical and opto-electrical domain converters in a RAU will be presented and its fundamental blocks and key parameters will be described.

The uplink stream of a RAU must receive the wireless signal from different devices and send it towards the BS through the optical fiber. The block that carries out the electro-optical conversion is the uplink front-end. As shown in Fig. 1.4, it consists of a light-emitting photonic device and a driver that provides the electrical signal in a way that it can be correctly transmitted. The design of integrated circuits for optical communications is tightly bounded to the performance and limitations of the photonic devices: maximum transmitted output power, optical modulation index (OMI), or nonlinearities introduced by the light-emitting device and the fiber; among others.

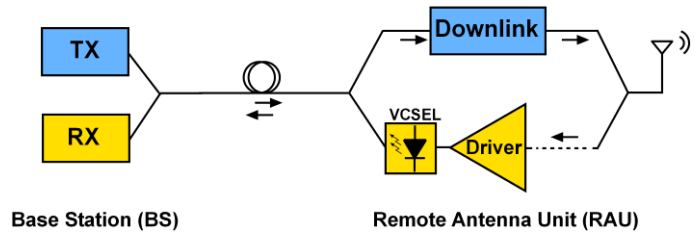

Fig. 1.4. Conceptual scheme of the uplink front-end of a remote antenna unit.

Typically, the photonic device that converts the electrical signal to light is the laser diode. It is a light-amplifying semiconductor device, in which population inversion is performed by forward biasing a heavily doped p-n junction. The position of the Fermi energy levels creates an active region, in which the stimulated emission of light takes place [PET12]. Typically, the generated light beam shows little divergence, which is key to an easy and efficient coupling to the optical fiber. For a current lower than a threshold value, I_{TH}, the population inversion does not occur, thus the device does not work as a laser. If the current is higher than I_{TH}, the stimulated emission begins and the output power rises with an approximately linear relation, where the slope is the efficiency, η_e [HEL16].

In communication systems, the most used laser diodes are the Fabry-Perot (FP) and the distributed feedback (DFB) lasers [MOR13, NAK18]. For long-haul communications, DFB lasers are usually employed because they emit only one wavelength with a very high spectral purity, which is ideal for wavelength-division multiplexing (WDM) to increase the data capacity of the optical fiber. However, in short-reach applications, the cost-efficiency of the system is mandatory, thus several communication systems employ the FP lasers and, most recently, the use of VCSELs is increasing due to their lower cost and ease of integration, test, and packaging [KOT18, LAV17, LU10, MED00, SZC15].

Laser modulation can be carried out either by direct modulation of the laser current or by means of an external modulator. External modulation is typically based on the Mach-Zender modulator (MZM), which increases the transmitter footprint and cost and introduces polarization sensitivity and insertion losses. Direct modulation can be implemented in a more cost-efficient way, avoiding the use of expensive MZMs. However, directly modulated lasers present a resonant peak in the frequency response, beyond which the electro-optical conversion efficiency decreases, thus its use is limited to modulation frequencies up to a few GHz [GHA96].

A correct behavior of a laser diode requires the use of a stable and predictable current source. The overall performance of a laser diode strongly depends on the electronics that drives the required current, the laser driver. In the most ideal form, the laser driver provides a predictable, linear, noiseless, accurate and stable current to the laser diode, preventing power variations due to environmental variables, such as temperature or aging. Moreover, in a direct modulation scheme, the laser driver must be capable of driving not only the bias current, but also the modulation current that contains the transmitted data.

The challenge of reducing the overall cost of the optical communication systems has driven the development of cost-effective laser drivers in a power-efficient way. Over the last few years, the design of VCSEL driver circuits targeting high transmission rate and low power has been enthusiastically investigated in silicon technologies [BEL16, KO18, SED12, SHI15, SZI17].

As shown in Fig. 1.5, in direct modulation, both bias and modulation currents of the laser diode are directly managed by the laser driver. Typically, the aim of the laser driver bias current is to provide a constant output optical power. For this purpose, the bias current is controlled by means of an automatic power control circuit. A monitor photodiode (PD) is typically integrated in the same package as the laser diode and it senses a small fraction of the emitted light. The automatic power control feedbacks the current from the monitor photodiode, I_{MD}, which is proportional to the laser output power, to keep it invariable over time.

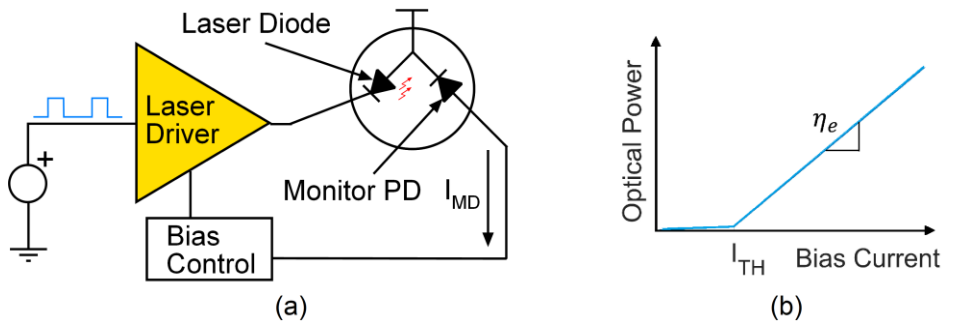

Fig. 1.5. Conceptual scheme of a laser diode driven by a laser driver using direct modulation and automatic power control (a) and typical response of a laser diode (b).

Depending on the modulation scheme or data encoding, the optimum biasing point can be stablished either close to the threshold current, for a digital on/off-switched transmission, or in a highly linear region, for more complex data modulation with high linearity requirements. The modulation current, also provided by the laser diver, contains the message that must be transmitted through the fiber. To achieve a proper, high-quality data transmission, the output optical signal should be a reliable replica of the original signal. Therefore, the output of the transmitter electronics must match the laser load in all the frequency range of interest to prevent nonlinearities and achieve a proper power conversion.

1.1.2 Downlink Front-End

The other half of the RAU is the downlink. The downlink stream of the RAU receives the optical signal from the BS and must perform an opto-electrical conversion to transmit this signal to several wireless devices. This opto-electrical conversion takes place in the downlink front-end, which consists of an optical receiver, generally composed of a photodiode and a transimpedance amplifier (TIA), as shown in Fig. 1.6. The optical receiver translates the incoming signal from the optical domain to the electrical domain.

The key to a high quality data transmission is the combination of good signal-to-noise ratio (SNR), wide BW and high linearity. Depending on the application, the impact of each of these characteristics will be significant and the design of the optical receiver will demand different requirements. All these characteristics, SNR, BW, and linearity depend on the performance of all the communication system elements: the optical fiber, the photodiode and the electronic integrated circuits that compose the receiver.

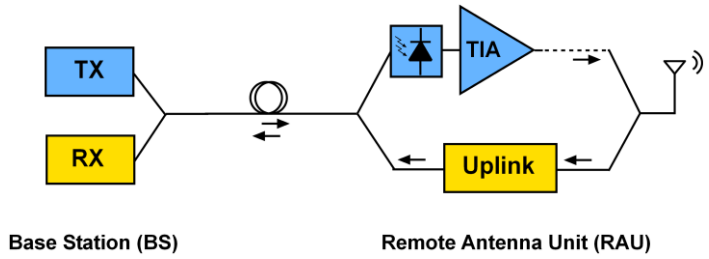

Fig. 1.6. Conceptual scheme of the opto-electrical conversion in a RAU downlink front-end.

The PD is the link between the optical and electrical domains. This device is similar to a regular diode except that a part of it is highly sensitive to light and it generates an electrical current when photons are absorbed. The operating principle of a PD consists of the excitation of the valence band electrons to the conduction band, thus generating electron-hole pairs. An electric field in the depletion layer accelerates these pairs in opposite directions creating an electrical current.

The photo-generated current I_{PD} corresponds directly to the optical power P_{op} and is given by the responsivity of the PD, R_{PD}, as follows

$$I_{PD} = R_{PD} P_{op} \tag{1.1}$$

A simplified electrical small-signal model of a reverse-biased PD using discrete circuit components is shown in Fig. 1.7. The most relevant parasitic elements are included to model the main characteristics of the PD. The model consists of a current source, I_{PD}, which represents the photo-generated signal and a capacitor, C_{PD}, which represents the charge effect of the photodiode junction. It is the main parasitic element that determines the PD performance in most applications. There are several parasitic elements that produce little effects, such as the dark current, I_{DK}, the diode shunt resistance, R_{SH} or the series resistance of the semiconductor material, R_S, which have been included in the model although they can be ignored for most applications [BLA12, STE02, WAN03, YUN12].

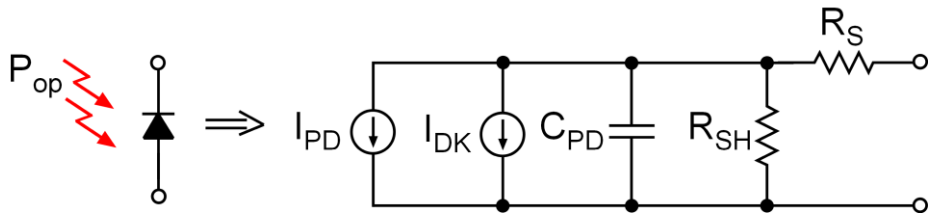

Fig. 1.7. Simplified electrical small-signal model of a reverse-biased photodiode.

The positive-intrinsic-negative (PIN) diode is the most used photodetector for linear wideband applications due to their small response time and excellent linear performance. It is similar to an ordinary P-N diode but including a wide undoped intrinsic region between the P and N regions. PIN diodes are wavelength selective because only the carriers generated within the depletion region or near it contribute to the PD current.

PIN diodes can detect light when they operate in the photovoltaic mode, that is, without a voltage bias. However, when a reverse bias is applied and the electrical field is strong enough to move all the carriers, the linear response is improved. Moreover, a reverse bias is required to ensure that the depletion region extension covers all the way through the intrinsic region to increase the spectral range of response and maximize the responsivity of the PIN diode, which can achieve quantum efficiencies, η[1], of the order of 0.8 [DEN91, MCC04, VAH16].

Silicon-based PIN diodes are sensitive throughout the visible range of the electromagnetic spectrum and in wavelengths near the infrared up to 1 μm. For wavelengths up to 2 μm, extremely fast InGaAs or cheaper alternatives such as

[1] The quantum efficiency, η, is the ratio of the number of charge carriers photo-generated to the number of incident photons.

Germanium PIN PDs are available. Typical spectral responses of several semiconductor materials are shown in Fig. 1.8.

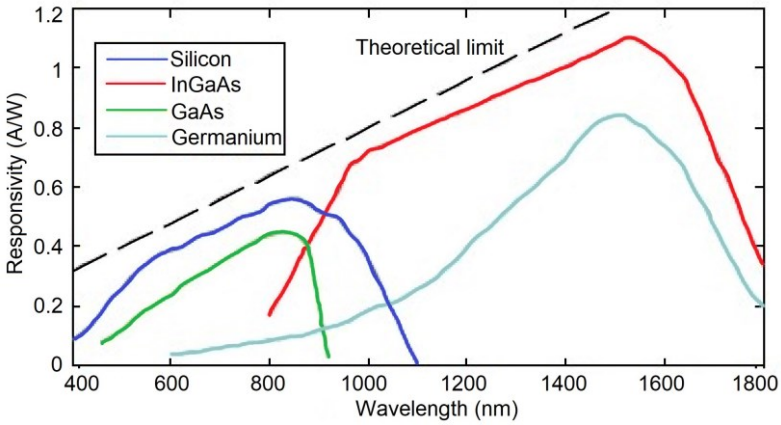

Fig. 1.8. Photodiode responsivity for typical semiconductor materials [AZN11c].

Apart from the wavelength selectivity of the device that determines the quantum efficiency, the maximum responsivity depends on the wavelength-dependent photon energy and it can be derived from (1.1) as

$$R_{PD} = \frac{I_{PD}}{P_{op}} = \eta \frac{\lambda q}{hc}$$
$$R_{PD} \approx 8 \cdot 10^{-4}\, \eta \lambda(nm) \left[\frac{A}{W}\right] \quad (1.2)$$

where η is the quantum efficiency of the PD, λ the wavelength, q the elementary charge, h the Plank constant and c the speed of light.

In addition to the spectral response and frequency response dependence on the device material, the responsivity can be controlled by modifying the dopant concentration and the thickness of the outer P-N layers. It also depends on the inverse voltage, V_{PD}, applied to the PD, which modifies the width of the depletion layer. The PIN PD normally operates under a reverse bias to take full advantage of the intrinsic layer to achieve higher detection BW.

To increase the responsivity, especially for very low signal power conditions, avalanche photodiodes (APDs) are employed. They show certain advantages for high-speed communications, at the expense of higher bias voltage requirements and worse linearity.

The operation of APDs consists of the generation of multiple carriers for each absorbed photon. The photons are absorbed in the very lightly doped π region and the photoelectrons drift towards the P region under the presence of a moderate electrical field. When they reach the PN+ region, the electrical field grows and accelerates the electrons, which gain enough energy to tear several electrons off the material by collision [CAP85, REN06, STI77].

The TIA is the first stage of the electrical domain of an optical receiver and it is the link between the PD and the rest of the analog front-end. This circuit converts the current photogenerated by the PD into an output voltage signal, therefore being the transimpedance, Z_T, its transfer function. It is a fundamental analog block, since most analog signal processing blocks are designed to work in voltage mode, but the PD generates electrical currents. As it is the first stage, its characteristics are critical to determine the overall receiver behavior, especially in terms of noise, which is amplified in the subsequent stages [RAZ03]. Additionally, the performance required by the analog front-end is greatly determined by the characteristics and nature of the transmitted signal.

For high-speed communications, the main requirements of the TIA are low input noise and wide BW. However, depending on certain application variables, such as the communication channel or the modulation scheme, other key parameters such as high transimpedance or highly linear behavior become extremely important [BRI08]. Moreover, the TIA design strongly depends on the characteristic parameters of the PD. Typically, one of the main limitations of a TIA design to achieve a wide BW and a high transimpedance is the intrinsic junction capacitance of the PD, which can vary from a few tens of fF to several pF. High-speed applications require low input impedance to achieve a good matching with the PD and a higher BW, while the tradeoff between BW, noise, linearity and transimpedance can make the design of the TIA very challenging.

The main function of the TIA is the current to voltage conversion. For this target, there are several circuit topologies that can be used for the implementation of a TIA, being the simplest one a passive resistive load directly connected to the PD. This implementation, shown in Fig. 1.9 together with its small signal model, is also easy to study to understand the concepts of the TIA and how its parameters are bounded.

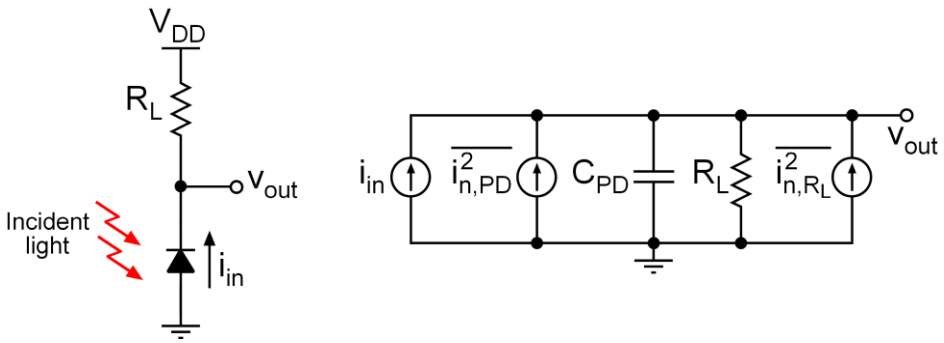

Fig. 1.9. Resistive TIA and its small signal model including noise sources.

Considering the small signal model shown above, being C_{PD} the photodiode capacitance, the main characteristic parameters: transimpedance, bandwidth (ω_{3dB})

and input referred noise[2] $(i_{n,in})$ can be directly derived to arrive at some fundamental limitations of TIAs:

$$Z_T = \frac{v_{out}}{i_{in}} = \frac{R_L}{1 + sR_L C_{PD}} \tag{1.3}$$

$$\omega_{3dB} = \frac{1}{R_L C_{PD}} \tag{1.4}$$

$$\overline{i^2{}_{n,in}} = \overline{i^2{}_{n,PD}} + \overline{i^2{}_{n,R_L}} = \overline{i^2{}_{n,PD}} + \frac{4k_B T}{R_L} \tag{1.5}$$

where k_B is the Boltzmann's constant, T the temperature and $i_{n,PD}$ and $i_{n,RL}$ are the noise contributions of the PD and load resistor, R_L, respectively. Supposing that the noise from the PD is negligible compared to the thermal noise from the resistor, it can be derived that the tradeoff between bandwidth and noise is independent of the transimpedance

$$\frac{\omega_{3dB}}{i^2{}_{n,in}} = \frac{1}{4k_B T C_{PD}} \tag{1.6}$$

This expression shows the poor noise performance of this simple implementation, since the relation between BW and noise can only be improved by reducing the PD capacitance, which is directly related to the PD sensitive area. Larger area PDs will be noisier while smaller area PDs will receive less signal, thus degrading the SNR, or will require a more accurate alignment with the optical fiber [ACH06, LI10, ROY15a].

Moreover, for high-speed applications, a wide BW is needed, therefore with this implementation, a very small resistor should be employed, thus performing very low transimpedance and very high noise, that means a very poor SNR. This suggests that the use of active approaches that provide higher performance and more relaxed trade-offs to implement the TIA is required.

The final requirements of the TIA greatly depend on the characteristics of the transmitted signal. Therefore, to give a background to the TIA design, the next subsection presents the different RAU architectures that define the data transmission format.

[2] The input referred noise is the noise current that, when applied to the input of the noiseless circuit, generates the same output noise as the actual circuit does.

1.1.3 RAU Architectures

Several considerations must be made to accomplish the design of the analog front-ends, from choosing the adequate photonic devices (laser diode, photodiode, fiber) to the design, optimization, and implementation of the different electronic circuits. The key to achieve an adequate DAS is finding a good compromise between performance and cost.

The deployment of distributed antenna systems can have a great impact in several scenarios such as densely populated buildings, hospitals, airports, or office buildings, and in residential areas, where a large, growing number of devices demand a greater interconnectivity. The fiber-wireless combination can bring an enormous increase in wireless data capacity with a fair use of the RF spectrum with a smaller impact in power consumption and radiated power, along with a higher spectral efficiency and reliability.

Mixed fiber-wireless systems offer several optical data transport configurations, which can be classified in three categories: RF over fiber (RFoF), intermediate frequency over fiber (IFoF) and baseband over fiber (BBoF). These schemes are shown in Fig. 1.10 and they are named upon how the data transmission through the fiber is performed.

The BBoF scheme follows the typical configuration of optical communication systems for long-reach applications. With this scheme, very high bit rates, of the order of several Gb/s, can be achieved. However, this scheme requires a complex RAU configuration and design, as it must perform data modulation and demodulation tasks, as well as frequency conversion, which increases power consumption (Fig. 1.10 (a)). Since a high number of RAUs is needed, the cost of a BBoF-based DAS can rise considerably. Despite being the dominant transmission format nowadays, this approach might be unattractive to future low-cost applications.

On the opposite side, the RFoF scheme (Fig. 1.10 (b)), presents the simplest RAU architecture because the RAU only has to perform opto-electrical and electro-optical conversion and signal amplification. RFoF is the most flexible RAU, since it is transparent to the data encoding or the communication standard. The RF signal generation is centralized at the BS and the RAU performs no signal processing, modulation, or frequency conversion. These systems, however, require much higher linearity than BBoF to transmit the signal properly and they show distance limitations when transmitting several WLAN (wireless local area networks) standards at high RF frequencies, due to the high dispersion of the used MMF at such frequencies [LET05]. Several attempts to design RAUs for RFoF have been made in recent years with promising results and performance, transmitting RF at 2.5 GHz [YOO09, KAN09], 5 GHz [KO13] or 12 GHz [DES15].

One of the main disadvantages of RFoF systems is that they require high-speed circuit design and high-performance photonic devices, therefore increasing the

power consumption and the overall cost of the DAS significantly. Moreover, at higher frequencies, there are undesired effects such as power penalty periodically fading and nonlinearities inducing spectrum broadening of the baseband data around the carrier signal [MIY15; QI10; MAE12].

Finally, the intermediate frequency over fiber transmission is a strategy that shows advantages upon both the aforementioned schemes. As in the RFoF approach, RAUs for IFoF do not require the implementation of a modulator/demodulator. Therefore, the complexity in the design of the RAU is much simpler than that in BBoF systems, and the power consumption is significantly lower, Fig. 1.10 (c). The signal is generated at the BS with the same modulation format as the RF signal, but at a lower frequency. Therefore, the flexibility of IFoF RAUs is just a step below RFoF as it is almost transparent to the communication standard, with the only need of tuning the RF carrier frequency. To recover the original RF signal, the RAU now requires a high-speed mixer and a stable local oscillator (LO), which is used in both the downlink and the uplink of the RAU, with an accurately tuned frequency to carry out the frequency up-conversion and down-conversion, respectively. Furthermore, to generate the LO signal, a pilot carrier can be delivered to the RAU optically, allowing a higher flexibility and frequency tuning without the need of quartz crystal or similar devices.

Nevertheless, the IFoF presents major advantages upon RFoF. First, since the optical signal is modulated with a much lower frequency, the use of an IFoF system significantly simplifies the IC design and minimizes the effect of the MMF chromatic dispersion, increasing the achievable fiber length. Moreover, it also drops the overall cost of the system, since lower performance and less expensive photonic devices can be used at both the BS and the RAUs, for both optical-electrical conversion in the downlink and electrical-optical conversion in the uplink.

Furthermore, IFoF is the best solution for the ever-increasing wireless frequencies (60 GHz) due to the deployment of 5G technologies.

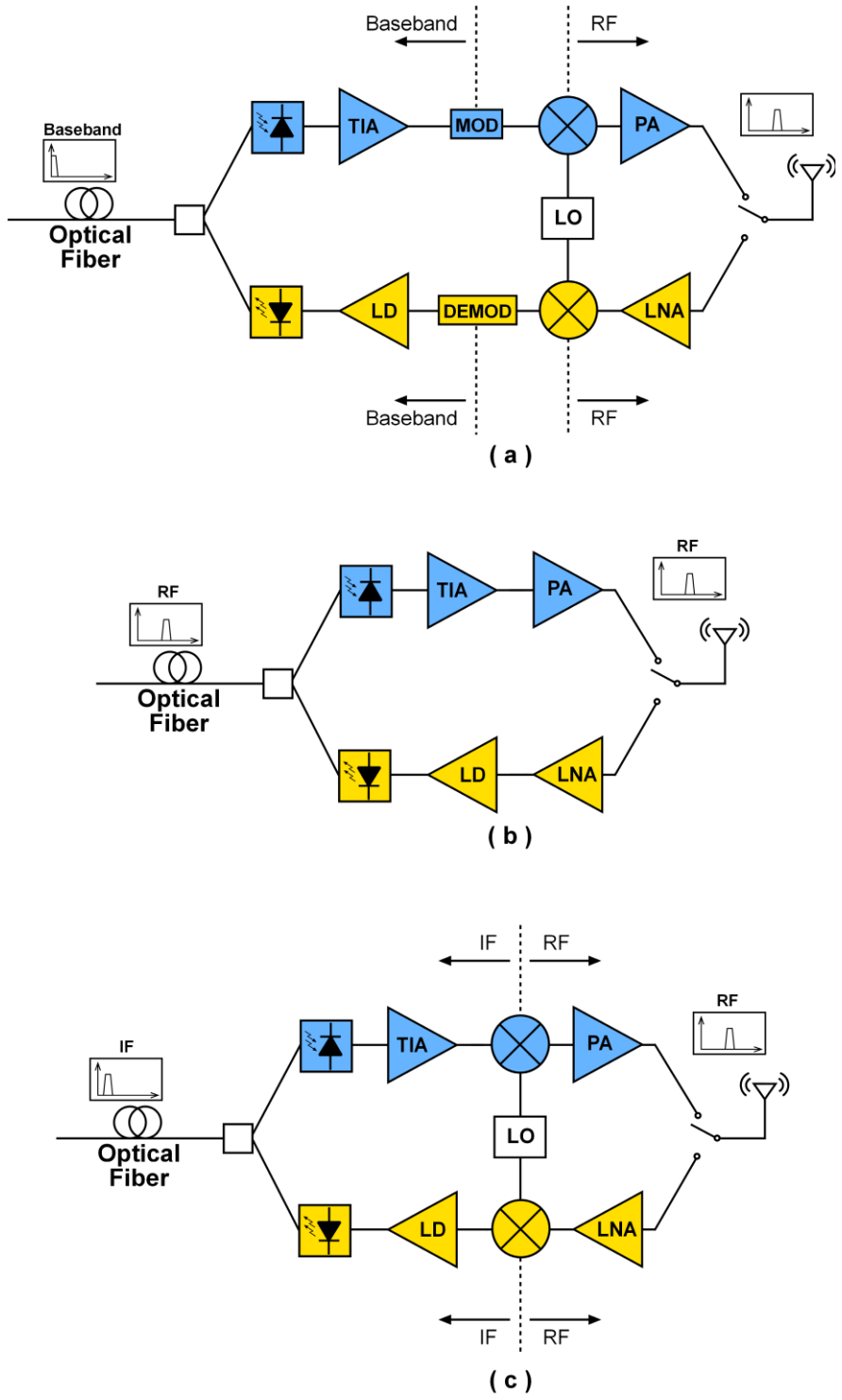

Fig. 1.10. Conceptual scheme of remote antenna units for a) Baseband over fiber, b) Radiofrequency over fiber and c) Intermediate frequency over fiber.

1.2 Motivation and Objectives

Wireless communications development is facing a huge upcoming challenge. The immense growth of data demand over the last years is showing that the capacity of the currently deployed wireless networks must increase considerably in the following years. Otherwise, it will not be possible to satisfy the future needs, which will slow down our development and will probably have a negative impact on the global economy.

Several approaches are tending towards mixed fiber-wireless system configurations, which are the most promising solution to deal with the enormous increase in data demand soon. Nevertheless, there is not an optimal approach among the three proposed DAS schemes, since each scenario and application will present specific requirements. Therefore, scenarios with a very high bitrate need will probably choose the BBoF scheme, despite its higher costs. On the contrary, applications where a high system flexibility and low cost are mandatory, the most preferable approaches will be RFoF and IFoF, while the choice will depend on several factors, such as RF frequency or the maximum budget on each case. In this context, the main objectives of this thesis are the following:

- Develop the design of different alternatives for each RAU configuration: BBoF, RFoF and IFoF. In particular, a proposal of RAU downlink front-ends will be made for each case, with the design of specific TIAs. The BBoF TIA will be aimed for short-reach high-speed communications through polymer optical fiber (POF) using non-return-to-zero (NRZ) encoding, for which high BW and low noise are the main key parameters. The RFoF and IFoF TIAs will target short-reach indoor fiber-wireless communication to transmit signals with different Wi-Fi 802.11 standards, for which a very high linearity and input dynamic range are the main key parameters of the receiver.

- Demonstrate the flexibility and advantages of the proposed TIA topology, migrating it for different applications and technologies.

- Contribute to the development and validation of a complete RAU for IFoF communications with the design of several subcircuits and the design of a printed-circuit board (PCB) to perform the experimental characterization of the RAU after its fabrication and mounting.

The motivation to choose the IFoF scheme for the complete RAU design over the other configurations is driven by the fact that this approach is considered the main candidate to develop high data capacity wireless networks in densely populated areas. These future networks need to be deployed with a very high number of short-reach nodes in a cost-efficient way, which is the reason why IFoF systems are generating an increasing interest over the last years.

1.3 Methodology and Thesis Organization

The development of this thesis is framed on the study of mixed fiber-wireless communication systems using DAS, which are presented as a solution to address the upcoming increase in data demand. Throughout this thesis, several solutions, and applications of different transimpedance amplifier designs are proposed and studied, from the theoretical basis to the design and manufacturing of fundamental blocks of the RAUs, using CMOS (complementary metal-oxide-semiconductor) technological processes. The diverse field of application of this integrated circuit in communications and other applications have driven the motivation to study the implementation of this specific block in different RAU architectures and explore its use for other purposes, such as current sensors in accelerometer applications.

This manuscript-based doctoral thesis consists of three chapters. Chapter 1 has been dedicated to present the upcoming scenario of a highly increasing data demand and to introduce the fiber-wireless DAS and its basic cell unit, the RAU, which is probably the most promising solution to satisfy the future needs.

Chapter 2 is the core of this thesis. In this chapter a review of TIA topologies is provided and the proposal, design, and implementation of several TIAs is performed. A deep study of the electrical noise of the TIA is made and an approach to improve the noise performance is proposed, along with a theoretical study and its implementation in a transistor-level simulation. Three TIA topologies are presented for its use in RAUs for BBoF, RFoF and IFoF, respectively, and an adaptation of one of them is made to demonstrate the versatility and advantages of this circuit structure in other applications, such as readout circuits for micro-electromechanical systems (MEMS) inertial sensors.

An exhaustive experimental verification of the implementation of the TIA in an IFoF RAU is presented in Section 2.4. A complete electrical and optical characterization of the TIA is performed, and the results of the complete chip are obtained.

Finally, Chapter 3 summarizes the conclusions of this work and points out some research lines that could be addressed in near future. The references are summarized at the end of each chapter. At the end of the thesis, a copy of the four publications that conform this thesis is attached and a list of the author's publications is included.

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2 Transimpedance Amplifier Design

The transimpedance amplifier (TIA) is a circuit that converts an input current to a proportional output voltage and presents a low input impedance. In an opto-electronic front-end, the TIA converts the small photocurrent that comes from the PD into a measurable voltage, so that later, the post-amplifier stages can boost such a voltage swing to logical levels, adequate for subsequent digital circuitry, or to achieve enough level amplitude for analog processing.

The design of the TIA is a critical step in the manufacturing of optical receivers since it typically limits and determines the achievable bandwidth and noise performance of the receiver [SAC17]. This chapter presents the study and design of different TIAs optimized for the three possible RAU configurations in a DAS as well as for other applications in communications. Additionally, an adaptation to test the versatility and advantages of this circuit structure in the readout circuits for micro-electromechanical systems (MEMS) inertial sensors is proposed.

2.1 Topologies Review

Overcoming the tradeoff between noise, bandwidth and gain is commonly the main target of a good TIA design. The TIA must present a BW wide enough to avoid inter-symbol interferences (ISI) and a high transimpedance to improve the signal-to-noise ratio (SNR), therefore, the design must seek circuits that present a less stringent tradeoff, which can be very challenging. For each application, a specific BW must be achieved, therefore the focus of the TIA design is the optimization of noise, gain, and linearity.

Noise is one of the most important parameters in all communication systems. It determines not only the smallest signal that can be correctly detected, but also the ratio of bit errors of a data transmission, or bit error ratio (BER) and the maximum link distance is limited by this parameter. Therefore, the TIA design must aim to achieve low input noise performance to maximize the receiver sensitivity and minimize the BER. This critical problem of noise prevents using complex configurations that employ many devices in the signal path, thus restricting the valid CMOS topologies to a few: the common-gate (CG) stage [PAR07], the regulated cascode [ATE13, LI13, LU12, OLI12] and current-feedback amplifiers [LU09, ROY15a, SAN07].

2.1.1 Open-Loop TIA

The open-loop approach is based on the single-stage CMOS amplifier, the CG stage, which exhibits a low input impedance [MAR20a]. The CG-based TIA structure, shown in Fig. 2.1, is also known as a feed-forward TIA, as there is no feedback loop. This circuit topology is typically used as a current buffer [BRI15, PAR07]. It isolates the input capacitance of the PD from the load resistor, R_D, alleviating the speed limitations due to the high value of the parasitic capacitance C_{PD}.

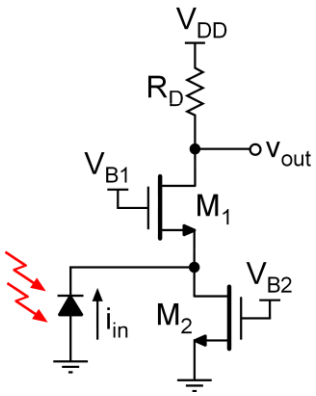

Fig. 2.1. Common-gate based transimpedance amplifier.

Including the channel-length modulation effect of M_1 in the small signal equivalent circuit of Fig. 2.2, and assuming M_2 as an ideal current source, they main TIA

operation key parameters can be derived. The input resistance, R_{in}, obtained from the low-frequency behavior is

$$R_{in} = \frac{r_{o1} + R_D}{1 + g_{m1} r_{o1}} \simeq \frac{1}{g_{m1}} \tag{2.1}$$

where r_{o1} and g_{m1} are the channel-length modulation resistor and transconductance of M_1, respectively. For the high-frequency behavior analysis, the main parasitic capacitances can be grouped in C_{in} and C_{out}.

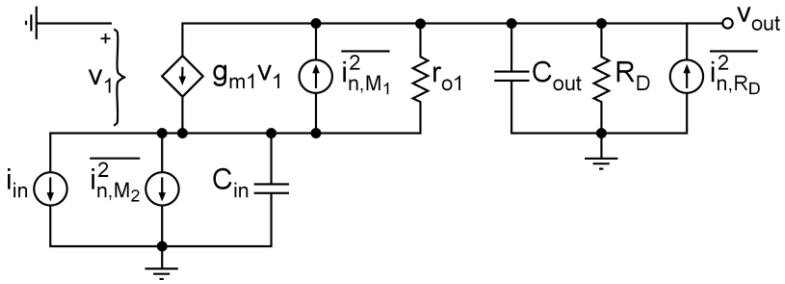

Fig. 2.2. Small signal equivalent circuit of the common-gate TIA including the transistors and resistor noise sources.

Thus, the transimpedance and 3-dB bandwidth, ω_{3dB}, of the TIA are

$$Z_T = \frac{g_{m1} R_D}{(g_{m1} + sC_{in})(sR_D C_{out} + 1)} \tag{2.2}$$

$$\omega_{3dB} = \sqrt{\frac{g_{m1}}{R_D C_{in} C_{out}}} \tag{2.3}$$

Let us now analyze the noise performance at low frequency and study the tradeoffs of this TIA configuration, including the effects of noise of the transistors and the drain resistor. This study depicts the main drawback of this structure, which is that the noise currents of M_2 and R_D are directly referred to the equivalent input noise, $\overline{i^2_{n,in}}$, which can be approximated by

$$\overline{i^2_{n,in}} = \overline{i^2_{n,M_2}} + \overline{i^2_{n,R_D}} \tag{2.4}$$

where

$$\overline{i^2_{n,M_2}} = \gamma 4 k_B T g_{m2} \tag{2.5}$$

$$\overline{i^2_{n,R_D}} = \frac{4 k_B T}{R_D} \tag{2.6}$$

where γ is the bulk-threshold constant, a technology-dependent dimensionless constant with a value smaller than 1. If we rearrange the terms from (2.4)

$$\overline{i^2_{n,in}} = 4 k_B T \left(\gamma g_{m2} + \frac{1}{R_D}\right) \tag{2.7}$$

We arrive at the following tradeoff between BW and noise in this TIA

$$\frac{\omega_{3dB}}{\overline{i^2}_{n,in}} = \frac{1}{4k_BTC_{eq}} \frac{\sqrt{g_{m1}R_D}}{\gamma g_{m2}R_D} \tag{2.8}$$

where C_{in} and C_{out} have been rearranged, being $C_{eq} = \sqrt{C_{in}C_{out}}$ to obtain an equation similar to (1.6). Comparing this expression with (1.6), the BW-noise trade-off is improved with the CG-TIA, being C_{eq} typically much lower than C_{PD} due to the much lower value of C_{out}, as these can be of the order of several pF versus a few hundred of fF, respectively. Moreover, if we design the CG stage so that it achieves high g_{m1} and low g_{m2}, the BW-noise relation can be strongly improved.

With this topology, a proper choice of bias current can provide a low input impedance to maximize the bandwidth. However, there are still several drawbacks related to the BW-noise-transimpedance trade-off. The noise current of the current source and the load resistor are directly referred to the input, which leads to high noise at low supply voltage. Therefore, it is difficult to achieve both high bandwidth and transimpedance without degrading the noise performance.

Another alternative is an improved version of the CG stage that includes a booster amplifier with gain A, as shown in Fig. 2.3. The regulated cascode is a modified CG amplifier composed of a CG with a local feedback and it is designed to overcome the drawback of the low transimpedance at low bias current, while enhancing the frequency response [OLI12, SÄC90].

The regulated cascode amplifier has been widely used for TIA design in high-speed optical communications [PAR04, LI13]. This circuit improves the isolation of the input capacitance and is able to decouple bandwidth and gain, increasing the effective transconductance of the input MOS transistor by *A*, which is the open-loop gain of the booster amplifier. However, a higher noise is expected since more noise sources are added. Therefore, it is very difficult to achieve low noise with this TIA configuration due to its tight trade-offs.

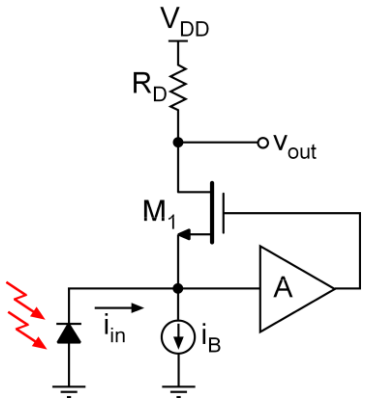

Fig. 2.3. Regulated cascode transimpedance amplifier.

2.1.2 Shunt-Feedback TIA

Compared to feedback topologies, the feedforward TIA is simpler and more stable. However, it tends to be noisier and open-loop topologies typically show a worse linear performance [RAZ12]. Thus, some kind of feedback topology should be used to overcome these trade-offs and limitations.

The most popular TIA configuration is the shunt-feedback topology, which can be represented, as shown in Fig. 2.4, by an inverting voltage amplifier with open-loop gain, $-A$, and a feedback resistor, R_F. This structure lowers both the input and the output impedance, improving the BW and yielding better drive capability while it also provides a high transimpedance [RAZ12, SCH02]. Moreover, the feedback loop enhances the linear behavior, which is critical in several applications.

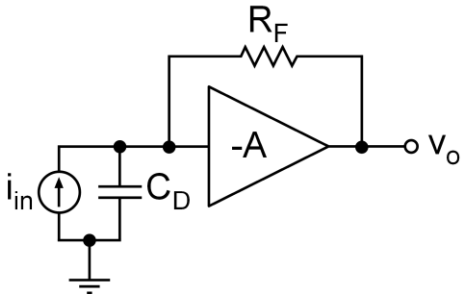

Fig. 2.4. Feedback TIA circuit schematic.

Considering an ideal amplifier behavior with open loop gain $-A$, the transimpedance and BW are obtained

$$Z_T = -\frac{R_F}{1+\frac{1}{A}} \cdot \frac{1}{1+\frac{R_F C_{PD}}{A+1}s} \rightarrow -R_F \tag{2.9}$$

$$\omega_{3dB} = \frac{A+1}{R_F C_{PD}} \rightarrow \frac{A}{R_F C_{PD}} \tag{2.10}$$

If the open-loop gain is much greater than 1, the transimpedance can be approximated by R_F. These expressions resemble those obtained for the resistive TIA in (1.3) and (1.4), being Z_T equal to the feedback resistor, R_F, instead of the load resistor, R_L, and with a much higher BW as there is a multiplication factor that equals the open-loop gain of the voltage amplifier, ideally much higher than 1.

Including the effect of the noise sources that correspond to the feedback resistor and the amplifier, the low frequency expression of the equivalent input noise (EIN) and the BW-to-noise ratio can be obtained

$$\overline{i^2_{n,in}} = \frac{4k_B T}{R_F} + \frac{\overline{v^2_{n,A}}}{R_F^2} \tag{2.11}$$

$$\frac{\omega_{3dB}}{\overline{i^2_{n,in}}} = \frac{A+1}{4k_BTC_{PD} + \frac{C_{PD}}{R_F}\overline{v^2_{n,A}}} \tag{2.12}$$

To compare this BW-noise ratio with (1.6), let us estimate $\overline{v^2_{n,A}}$, considering that the voltage amplifier consists of a common-source (CS) stage, shown in Fig. 2.5.

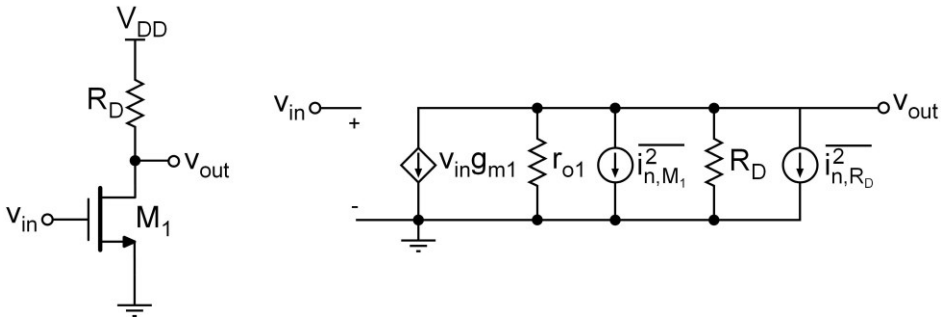

Fig. 2.5. Common-source stage and small signal model.

This stage presents an open-loop gain of

$$A = \frac{v_{out}}{v_{in}} = -g_{m_1}R_D \tag{2.13}$$

Then, calculating the output noise

$$\overline{v^2_{n,out}} = \left(\overline{i^2_{n,M_1}} + \overline{i^2_{n,R_D}}\right) R_D^2 \tag{2.14}$$

where

$$\overline{i^2_{n,M_1}} = 4k_BT\gamma g_{m_1} \tag{2.15}$$

$$\overline{i^2_{n,R_D}} = \frac{4k_BT}{R_D} \tag{2.16}$$

we obtain the input-referred noise of the CS voltage amplifier

$$\overline{v^2_{n,A}} = \frac{4k_BT}{g_{m1}}\left(\frac{1}{g_{m1}R_D} + \gamma\right) \tag{2.17}$$

Then, for a feedback TIA with an input CS stage, the BW to noise trade-off can be approximated by

$$\frac{\omega_{3dB}}{\overline{i^2_{n,in}}} = \frac{A+1}{4k_BTC_{PD}\left[1 + \frac{1}{g_{m_1}R_F}\left(\frac{1}{g_{m_1}R_D} + \gamma\right)\right]} \tag{2.18}$$

and, considering both $g_{m_1}R_F$ and $g_{m_1}R_D$ much greater than 1, then

$$\frac{\omega_{3dB}}{\overline{i^2}_{n,in}} = \frac{A+1}{4k_B T C_{PD}} \tag{2.19}$$

This expression shows a major improvement compared with (1.6), being this ratio A times higher with this TIA topology. Compared to the open-loop CG TIA, the bandwidth to noise tradeoff is also much greater than (2.8), while the design boundaries are less stringent. In feedback TIAs, a much larger transimpedance can be achieved, since Z_T is determined by R_F, which can be much larger than the drain resistor of a CG TIA. Moreover, the feedback resistor does not need to carry a bias current, therefore, its value is not limited by the supply voltage. This is one of the main reasons why many recently published works employ feedback structures for the TIA implementation in optical receivers [CHE16, FUA16, HON18, LAM19].

2.1.3 Second Order Shunt-Feedback TIA

The first order approximation of the shunt-feedback TIA gives us a good understanding of the excellent performance in terms of transimpedance and bandwidth to noise ratio, compared to other TIA configurations [AZN11a, IKE01, PAR03]. Nevertheless, further knowledge about the circuit behavior can be obtained with a more realistic amplifier model. Then, let us consider the core amplifier in Fig. 2.4 a first order amplifier with a single dominant pole, ω_A, and an open-loop gain A, so that

$$A(s) = \frac{A}{1+\frac{s}{\omega_A}} \tag{2.20}$$

given an open-loop gain A much larger than unity and rearranging terms, we can rewrite (2.9) as

$$Z_T = -\frac{R_F}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}} \tag{2.21}$$

which is a second order transfer function with a natural oscillation frequency pole, ω_0, and a quality factor, Q, where their dependence on the circuit variables are

$$\omega_0 = \sqrt{\frac{A\omega_A}{R_F C_{PD}}} \tag{2.22}$$

$$Q = \sqrt{\frac{A}{R_F C_{PD} \omega_A}} \tag{2.23}$$

From (2.21), we obtain the transimpedance module, and analyze the frequency dependence of the denominator of $|Z_T|$

$$|Z_T|^2 = \frac{R_F^2}{\left(1-\frac{\omega^2}{\omega_0^2}\right)^2 + \frac{\omega^2}{Q^2\omega_0^2}} \tag{2.24}$$

$$\frac{d(|Z_T|^2)}{d(\omega^2)} = \frac{1}{\omega_0^2}\left(\frac{1}{Q^2}-2\right) + \frac{2\omega^2}{\omega_0^4} \tag{2.25}$$

If $Q < \sqrt{2}/2$, the derivative of the denominator is greater than zero for all frequencies, therefore the transimpedance is a decreasing function of ω. For $Q = \sqrt{3}/3$, we obtain the Bessel response, which has the smallest group-delay variation, and for $Q = \sqrt{2}/2$ we obtain the Butterworth response, which produces some overshoot but is the highest Q value without peaking and has a maximally flat frequency response. At $Q = \sqrt{2}/2$, where $\omega_0 = \sqrt{2}\omega_A$, the feedback TIA presents a bandwidth of

$$\omega_{3dB} = \sqrt{2}\frac{A}{R_F C_{PD}} \tag{2.26}$$

which is a remarkable result, being $\sqrt{2}$ times the one achieved in (2.10), meaning that the feedback TIA with a finite-bandwidth core amplifier is faster than with an ideal infinite-bandwidth voltage amplifier.

On the contrary, if Q is greater than $\sqrt{2}/2$, the slope of the denominator is negative at low frequencies and becomes positive at higher frequencies, crossing zero at a frequency between zero (when $Q = \sqrt{2}/2$) and ω_0 (when $Q = \infty$), which implies a minimum in the denominator module and means that peaking in the frequency response is present. Fig. 2.6 shows the frequency response as a function of the quality factor. It is clear there is no peaking at low values of Q and that the higher the Q, the higher the peaking, and thus the overshoot, ringing, and system instability.

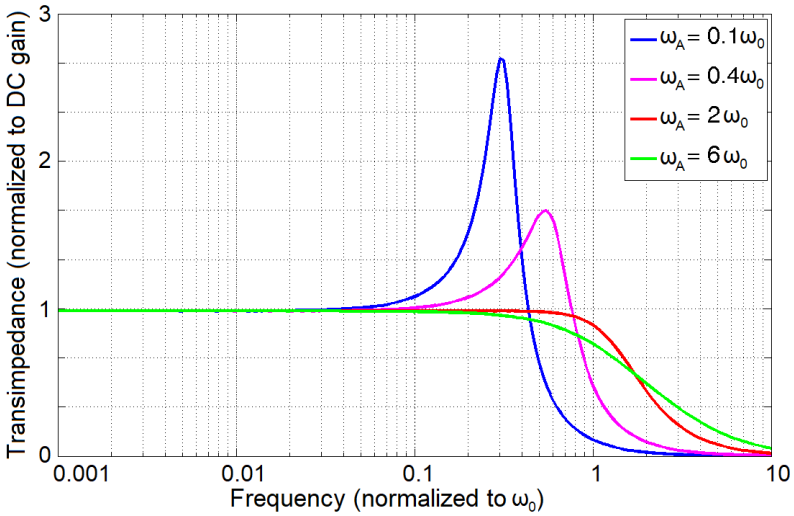

Fig. 2.6. Frequency response as a function of the quality factor.

Applying the requirement that $Q \leq \sqrt{2}/2$ in (2.23) we arrive at the conclusion that

$$\omega_A \geq 2A \frac{1}{R_F C_{PD}} \tag{2.27}$$

$$\omega_A \geq \sqrt{2}\omega_0 \tag{2.28}$$

The open-loop bandwidth must be greater than twice the bandwidth of the one obtained using a first order approximation in (2.10). Additionally, it must be greater than $\sqrt{2}$ times the bandwidth of the second-order TIA, since it can be easily shown in (2.21), that it is bounded by $\omega_{3dB} \leq \omega_0$. This result precludes the use of conventional operational amplifiers in high-speed communication applications since they typically present a relatively low unity gain bandwidth [HUI11].

One last consideration about feedback TIAs, which is also related to the critical drawback of the system stability, is the presence of multiple poles in the core amplifier [PER93, LEU00, LEU01]. Until now, we have considered a second order approximation of the TIA using a first order model of the voltage amplifier, with a dominant frequency pole. This single-pole model is a good approximation that describes very accurately the behavior of feedback TIAs and explains the origin of the frequency response peaking. Nevertheless, in a real situation, the core amplifier in Fig. 2.4 presents additional poles caused by the transistor stages or the parasitic elements. Therefore, actual feedback TIAs present multiple poles, while each pole contributes a certain amount of phase shift to the open-loop frequency response. To obtain a stable TIA and avoid overshoot or ringing issues, we must design the core amplifier with a sufficient open-loop phase margin by placing the poles at frequencies higher than that of (2.27). It is necessary to perform a careful design and detailed simulations at transistor level, along with an accurate parasites approximation to achieve a flat frequency response without peaking, overshoot, or ringing [ESC95, NG99].

2.2 Noise Analysis

Noise is a random phenomenon and as such, it cannot be predicted with a deterministic function. Using probability theory and statistical calculations, we can assume a random noise power, current or voltage, measured by its mean value [RIC44]. When designing an optical receiver, it is common to use the input-referred noise and refer to it as an ideal receiver with zero noise with an input noise source equal to it [RAZ12, SAC05]. To obtain the input-referred noise expression, we must first sum the squares of the noise voltages and currents, since they are uncorrelated random events. All the devices of an analog front-end and their corresponding noise sources contribute to the input-referred noise current and thus degrade the sensitivity of the receiver. Among all, the most relevant to this contribution are the devices present in the input stage of the front-end, the TIA [FUA18, LU09]. According to the results obtained in the previous section, adjusting the TIA response to a Butterworth response with $Q = \sqrt{2}/2$ provides the highest SNR for a given bandwidth. It is also clear that there is an optimum bandwidth depending on the data transmission bitrate since an insufficient BW leads to ISI and a BW too high degrades the SNR because more noise is integrated [AZN11c]. Moreover, in the case of a BW higher than needed, the amount of integrated noise grows much faster due to the f^2 noise contribution, which we will analyze in this section.

At low frequencies, the flicker noise becomes the dominant noise contribution. This is a type of noise with a technology-dependent contribution and a $1/f$ power spectral density [CHA94, HUN90]. Although it can often be troublesome in low frequency applications, it must also be considered in high-speed communications as another noise contribution, which is typically defined by the corner frequency, f_c, shown in Fig. 2.7, where its value equals the white noise. In the previous section we have studied the contribution of noise by different TIA topologies and in this section a deeper study of the noise in a feedback TIA has been done. We must consider not only the contribution of white noise, but also the frequency-dependent noise, for which a high-frequency noise analysis is made. Therefore, if we recalculate the previously obtained input noise expression (2.11), considering the high frequency dependence of the PD capacitance, we arrive at the following equation

$$\overline{i^2_{n,in}} = \frac{4k_B T}{R_F} + \frac{\overline{v^2_{n,A}}}{R_F^2} \cdot (1 + \omega^2 R_F^2 C_{PD}^2) \tag{2.29}$$

If we consider that the first stage of the amplifier is a CS stage and we estimate the amplifier noise with the same approximation of (2.17), including the most relevant noise sources as shown in Fig. 2.8, we can rewrite the noise expression as

$$\overline{i^2_{n,in}} = \frac{4k_B T}{R_F} + \frac{4k_B T}{g_{m_1} R_F^2} \cdot \left(\frac{1}{g_{m_1} R_D} + \gamma \right) (1 + \omega^2 R_F^2 C_{PD}^2) \tag{2.30}$$

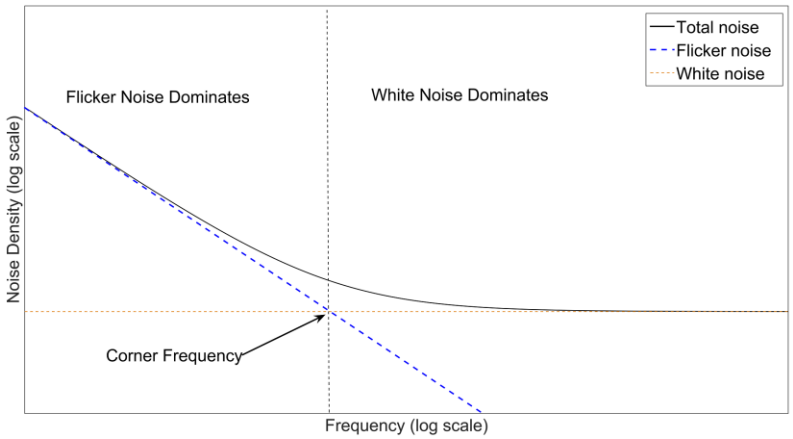

Fig. 2.7. Typical power spectral noise density of a CMOS TIA in presence of both flicker and white noise sources.

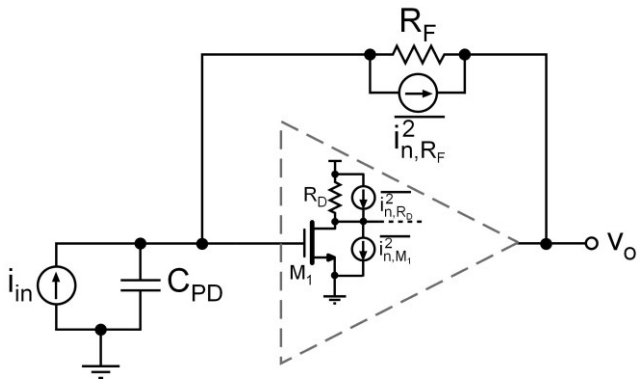

Fig. 2.8. Most significant noise sources in a feedback TIA with CMOS CS input stage.

An interesting result from this expression is that we have obtained an f^2 noise contribution which is proportional to the amplifier voltage noise, $\overline{v_{n,A}^2}$ and to the square of the PD capacitance, C_{PD}^2. If we consider typical values much greater than 1 for $g_{m_1}R_F$ and $g_{m_1}R_D$

$$\frac{4k_BT}{R_F} \gg \frac{4k_BT}{g_{m_1}R_F^2} \cdot \left(\frac{1}{g_{m_1}R_D} + \gamma\right) \tag{2.31}$$

The white noise contribution of the voltage amplifier is negligible, then

$$\overline{i^2_{n,in}} \approx \frac{4k_BT}{R_F} + \cdot \frac{4k_BT}{g_{m_1}} \gamma \omega^2 C_{PD}^2 \tag{2.32}$$

We can now differentiate the white noise contribution of the feedback resistor from the f^2 noise caused by the voltage amplifier, which starts growing at a frequency of $1/R_F C_{PD}$, approximately $\sqrt{2}A$ times lower than the TIA bandwidth in Butterworth

response condition, obtaining the noise response shown in Fig. 2.9. At low frequencies, the noise contribution of the amplifier is much lower than the feedback resistor noise, but the f^2 noise starts rising and we find another corner frequency, f_{c2}, when both noise contributions equal out.

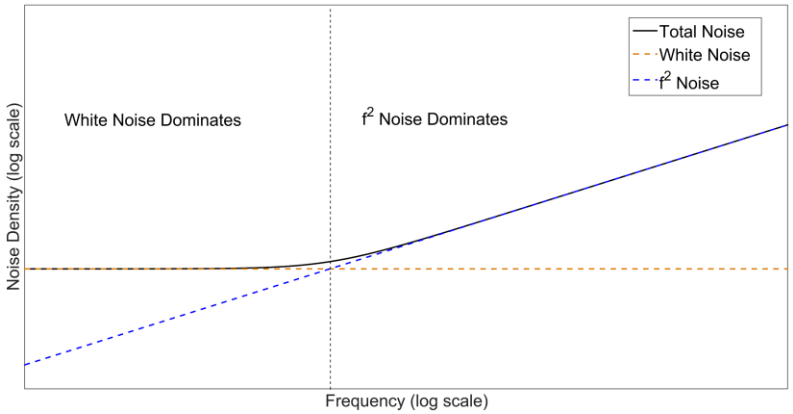

Fig. 2.9. Equivalent input noise spectrum of a CMOS shunt-feedback TIA.

Therefore, at lower frequencies, the flicker noise is dominant and $1/f$ dependent. In the mid-frequency range, the noise equals approximately the white noise contribution of the feedback resistor and at higher frequencies the noise of the voltage amplifier starts rising with an f^2 dependence. The fact that f^2 noise starts rising at a frequency $\sqrt{2}A$ times lower than the TIA bandwidth causes a hump in the output noise frequency response. This happens because typically f_{c2} is also much lower than the TIA BW and the peak of the output noise hump is located near the BW frequency, where the frequency response decays with a steep slope, leading to output noise responses like the one shown in Fig. 2.10.

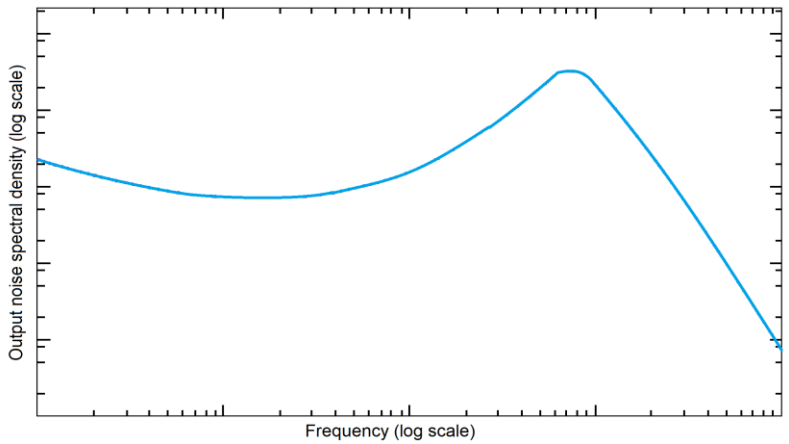

Fig. 2.10. Typical output-referred noise spectrum of a feedback TIA.

2.2.1 Noise Cancellation Techniques

Several techniques can be applied to the TIA design to optimize its noise response. Noise cancellation techniques, which have been employed for low noise amplifiers (LNA) [BRU04, CHE08, WI08, MAR19a, MAR21], can also be used for TIAs under certain conditions and it is possible to cancel specific noise sources in a feedback TIA. Let us consider the CS feedback TIA. The main noise source in the CS stage is the current noise generated by the MOS transistor. This current flows through the feedback resistor and the PD as shown in Fig. 2.11, causing a noise voltage at both output and input nodes, both of which have the same phase. On the other hand, the photogenerated current produces an output voltage that is inverted with respect to the input node voltage. Because of this sign difference between signal and noise, cancelling the noise from the input MOS transistor is possible by subtracting the input from the output signal [BRU04, CHE11].

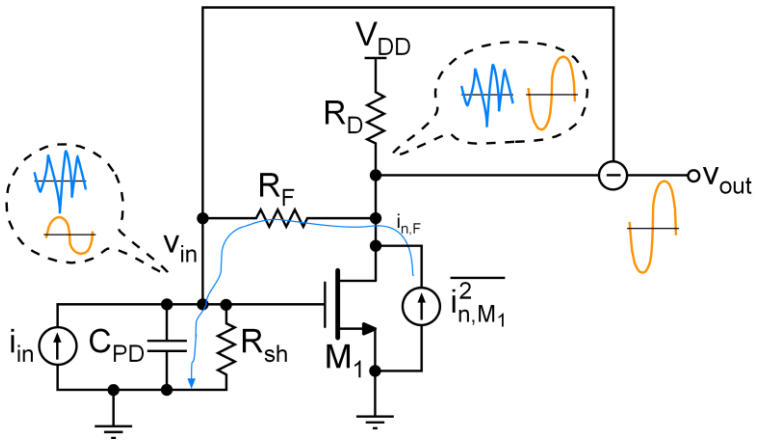

Fig. 2.11. CS feedback TIA using noise cancellation technique.

There have been several attempts to employ this noise cancelation technique [ATE13], however, it might only be valid at low frequencies. Let us see how the noise cancelling technique works at higher frequencies. If we consider the noise current, $i_{n,F}$, flowing through the feedback resistor and the PD, we can calculate the ratio between the noise voltage at the output node and at the input node as

$$v_{n,out} = i_{n,F}\frac{1+sR_FC_{PD}}{sC_{PD}} \tag{2.33}$$

$$v_{n,in} = i_{n,F}\frac{1}{sC_{PD}} \tag{2.34}$$

$$\frac{v_{n,in}}{v_{n,out}} = \frac{1}{1+sR_FC_{PD}} \tag{2.35}$$

According to (2.35), the voltage noise at the input is a replica of the noise at the output at frequencies lower than $1/R_FC_{PD}$, which is the same frequency value as the

one obtained in the input noise expression in (2.30). Therefore, noise components at frequencies lower than $1/R_F C_{PD}$, which are the flicker noise and the white noise contribution of the amplifier, can be cancelled by subtracting $v_{out} - v_{in}$. The noise cancellation degrades and fades out as the frequency increases. However, in addition to the noise cancellation, subtracting $v_o - v_{in}$ results in a higher signal gain, due to the opposite sign of these nodes.

Let us prove this conclusion with a transistor-level simulation of a CS feedback TIA with noise cancellation technique. The circuit parameters employed for this simulation are shown in Table 2-1.

Parameter	W_1	L_1	R_D	R_F	C_{PD}
Value	50 µm	180 µm	150 Ω	150 Ω	3 pF

Table 2-1. Common-source feedback TIA design parameters.

With this circuit design parameters, the TIA achieves a bandwidth of 470 MHz with a power consumption of 11 mW. The EIN response is shown in Fig. 2.12. If we simulate the implementation of an ideal subtraction to combine the input and output voltages as shown in Fig. 2.11, the TIA exhibits the input-referred noise response shown in Fig. 2.13.

As expected from the study above, the noise is cancelled at low frequencies. However, this technique mainly cancels the flicker noise, which has a slight impact on the overall integrated noise. Moreover, at frequencies below $1/R_F C_{PD}$, the white noise and the f^2-noise contribution of the voltage amplifier that is cancelled with this technique is very small, since it is negligible with respect to the white noise of the feedback resistor, as we explained above in (2.31). Therefore, unlike in LNAs, this technique applied to transimpedance amplifiers does not make a relevant noise cancellation and it is only valid to cancel flicker noise of the input stage of the TIA.

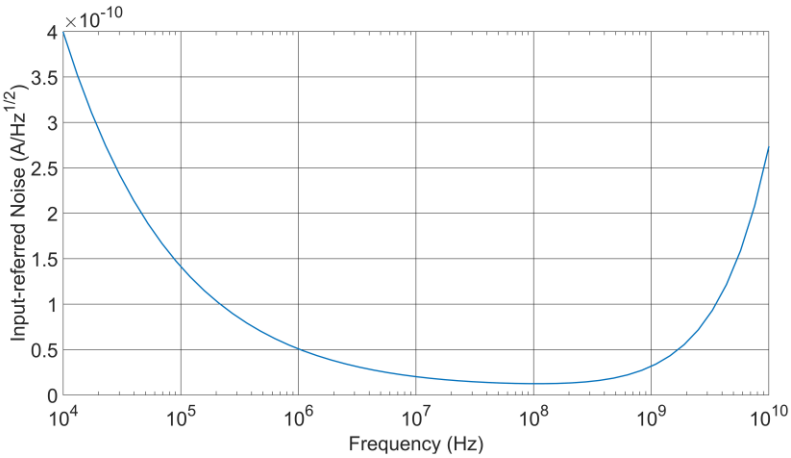

Fig. 2.12. Input-referred noise without noise cancellation.

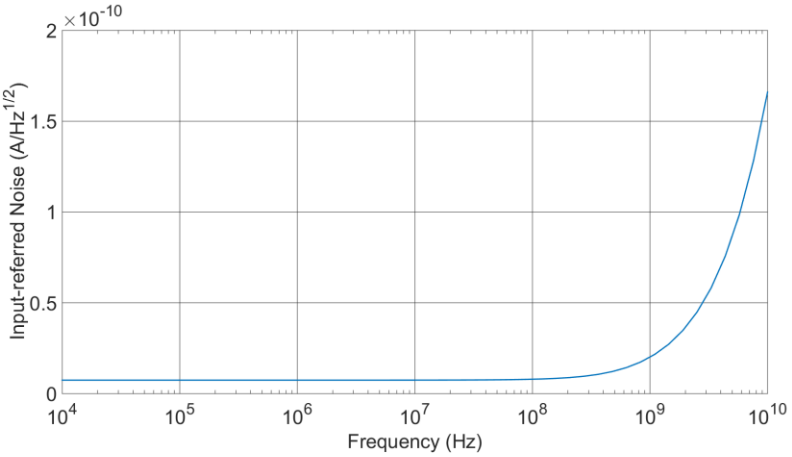

Fig. 2.13. Input-referred noise using the noise cancellation technique.

2.2.2 Sliced Photodiode Proposal

The sliced photodiode is a novel noise-reduction technique, firstly described in [ROY20a]. It consists of slicing the photodiode and manufacturing it in N individual pieces to obtain multiple PDs with smaller parasitic capacitances and connecting a dedicated TIA to each one of them, as shown in Fig. 2.14, with the aim of reducing the equivalent input-referred noise. Slicing the PD also helps reduce the difficulty of designing the TIA, since the parasitic capacitance of each PD piece is smaller and thus the TIA design constraints are relaxed.

To study the effect of this proposal, let us first recall the input-referred noise expression (2.32), including the effect of the parasitic capacitance of the voltage amplifier, C_T, being $C_{in} = C_T + C_{PD}$

$$\overline{i^2}_{n,in} = \frac{4k_B T}{R_F} + \frac{\overline{v_{n,A}^2}}{R_F^2} \cdot (1 + \omega^2 R_F^2 C_{in}^2) \qquad (2.36)$$

According to (2.36), the f^2 term is proportional to the square of the input-node capacitance, which can be approximated to the high intrinsic PD capacitance, especially in designs with large integrated PDs (1-mm diameter or more) used in many instrumentation and communication applications [DON12, TAV10].

Using the proposed technique, which consists of a modification of the integrated PD layout, slicing it in N equal pieces, the intrinsic capacitance of each PD is now divided by N, therefore the f^2 noise contribution should decrease by a factor of N^2. On the other side, each piece of the PD receives an optical power of $1/N$ times the total optical signal power and generates a current, $i'_{in} = i_{in}/N$. As shown in Fig. 2.14, to each PD piece, we connect an independent TIA, and the outputs are combined. In this configuration, a feedback resistor, $R'_F = N \cdot R_F$, is used to keep the $R_F C_{in}$ product approximately constant. Therefore, without the need of modifying the core amplifier

parameters, this approach maintains the same bandwidth and quality factor Q as in the case of a single PD and TIA scheme. The total input noise can be calculated by adding the N contributions, since each PD piece is independent, and the noise sources are uncorrelated

$$\overline{i^2_{n,in}} = \sum_{1}^{N} \frac{4k_B T}{NR_F} + \frac{4k_B T}{g_{m_1}} \gamma \omega^2 \left(\frac{C_{in}}{N}\right)^2 \tag{2.37}$$

$$\overline{i^2_{n,in}} = \frac{4k_B T}{R_F} + \frac{1}{N} \cdot \frac{4k_B T}{g_{m_1}} \gamma \omega^2 C_{in}^2 \tag{2.38}$$

From (2.38) it is clear that the white noise contribution of the feedback resistors does not change, as it is the same as the contribution of a single feedback resistor in a single-piece PD configuration. However, a remarkable result is that the f^2-noise term shows a $1/N$ dependence, which means an improvement of the overall SNR. This approach is valid if $C_{PD}/N \gg C_T$, since for lower values of C_{PD}/N, the rate at which we can reduce the f^2-noise term decreases rapidly due to the higher contribution of C_T to the total C_{in}. Typically, the main contribution to the parasitic capacitance of the voltage amplifier, C_T, is the gate-source capacitance of the input transistor, which can be as large as a few hundreds of femtofarads.

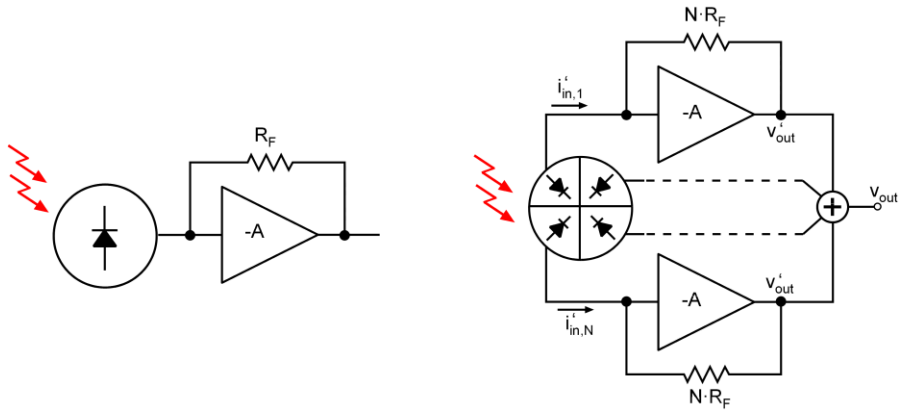

Fig. 2.14. Comparison between the typical configuration of (a) a single PD and (b) the sliced photodiode technique.

Another advantage of using this technique is the higher transimpedance that can be achieved. Each TIA produces the same output voltage v'_{out} as in the case of a single-piece PD, since each TIA senses a $1/N$ input current but presents an N times higher transimpedance, then

$$v'_{out} = i'_{in} R'_F = \frac{i_{in}}{N} \cdot NR_F = i_{in} R_F \tag{2.39}$$

Since all the N signals are synchronized, we can add them as shown in Fig. 2.14 to obtain an overall transimpedance N times higher than with a single-piece PD configuration

$$R_T = \frac{v_{out}}{i_{in}} = \sum_{1}^{N} i_{in} R_F = N R_F \tag{2.40}$$

which is another remarkable result that shows that using this technique it is possible to achieve a higher transimpedance than the expected limit as described in [SAC10]. Obviously, the main drawback of this technique is the increase in power consumption by a factor of N. Nevertheless, this technique strongly reduces the f^2-noise contribution, for which other noise cancellation techniques do not work, and it is possible to overcome the transimpedance limitation, thus allowing the achievement of better figures of merit.

2.3 Proposed TIAs for Communications

The advantage of mobility has placed wireless communication technology above the rest, and the reality of being connected with high data transfer rates, anywhere and anytime is now generally taken for granted by the user. Thanks to the latest advances in the deployment of wireless networks, the chances of losing connection or slowing down the data transfer rate due to a defective coverage is every time smaller. Nevertheless, it is still a highly user-feared fact. Therefore, greater efforts must continuously be carried out to improve the performance of wireless networks, for which actual wireless communication systems must enhance both their coverage and their immunity to interferences. The constant goal is to overcome the limitations of wireless communications, which are stronger in densely populated areas, where many wireless networks concur [DEN17, ORO19]. This can be quite challenging to achieve, since it entails an additional tradeoff that must be overcome, to achieve high data transmission rates that provide a better user experience [ROY18b].

A good candidate to undertake this improvement is the implementation of distributed antenna systems (DAS). With a good distribution of the remote antenna units (RAU), this approach can provide a much better coverage, especially for in-door applications. Moreover, since the emitted power of the RAUs is small, the wireless signal can be more confined within the walls, providing a higher security to the network and lowering the interferences [ROY18c]. However, to achieve a functional DAS, a high number of RAU cells with small coverage is needed. Since the overall cost of the DAS is strongly influenced by RAU costs, a cost-effective design is mandatory.

Of all the analog sub-blocks of an optical front-end, the transimpedance amplifier (TIA) is the most critical one. Its behavior determines the overall performance of the receiver; thus, it must be accurately designed, optimizing its characteristics depending on the application and the key parameters of the transmitted signal. In this chapter, we propose three transimpedance amplifier designs, each of them specifically aimed for use in the downlink optical front-end of each of the available RAU architectures, BBoF, RFoF and IFoF for various applications.

2.3.1 Low-Noise Low-Power TIA for NRZ Transmission (BB-TIA)

Short-range optical communications are a promising approach to achieve multi-gigabit transmission. For this reason, the use of optical communication systems has grown in the last years, due to their capability of transmitting information at very high data rates. However, because of the high cost of installation and maintenance of glass optical fiber (GOF) systems, most of the currently deployed short-range networks are still based on copper, which cannot transmit information as fast as optical fibers.

In this context, a promising solution to overcome the short-range bottleneck is plastic optical fibers (POF). Despite the low bandwidth-length product of POF of around 40 MHz·100 m [GIM15a] that restricts its use to short-reach links, it provides several advantages over other materials, such as mechanical robustness, ease of installation and low cost. POF can provide a higher data rate and are more robust than copper cables, with the additional advantage of their immunity to electromagnetic interferences. They have been recently used in the automotive and aeronautic industry since they are lighter and more flexible than copper cables and show a few advantages over GOF, such as higher stability against vibrations thanks to their much larger core diameter. They are also easier to install and manipulate, thus reducing the costs of installation and maintenance, making POF cost-competitive and an excellent candidate for short-distance applications, such as home networks. On the contrary, POF suffers from high attenuation (0.18 dB/m at 650 nm) and coupling with both the transmitter and the receiver generates even higher losses.

To increase the transmission length, highly sensitive optical receivers with large area photodiodes with a diameter of the order of 1-mm must be used. It is well known that large area photodiodes (PD) have an important parasitic capacitance of the order of several picofarads (pF). Therefore, to interface these photonic devices and overcome the high attenuation of POF, a low-noise TIA with low input impedance must be designed.

Further, the large core cross section of the POF also represents one of its main drawbacks. Due to the size of the fiber diameter, the modal dispersion of POF is very strong and the bandwidth of these fibers is quite low even for a few meters of length. This small BW is quite unusable for long-reach gigabit communications since the data rate is much higher than the BW of the channel. To compensate the dispersion produced by the fiber, equalization techniques must be used. There are several techniques to implement the equalizer circuit [GIM15b, GUE17]. Fig. 2.15 shows the analog equalization scheme, which consists of a filter in the receiver side, right after the TIA to recover the high-frequency signal components. Equalization is a well-known technique which has already been used in long-distance communications through GOF and it can be used to recover the signal integrity even when data rates much higher than the channel BW are employed [GIM14a, GIM15c].

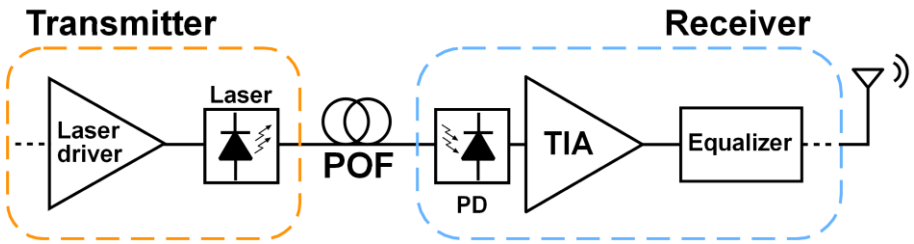

Fig. 2.15. Conceptual scheme of a POF communication system using receiver equalization.

Another disadvantage of the large POF diameter is the need of large area PDs with very high intrinsic capacitances, constraining the design of the optical front-end and making more difficult to achieve high-speed operation. Furthermore, the design of the TIA must overcome the high attenuation of POF of around 0.18 dB/m at 650 nm. The sensitivity of the TIA becomes a critical parameter of the communication system, especially when longer link distances are intended, since it will determine the maximum POF length for which a signal can be distinguished from noise with a low enough BER.

Due to the POF frequency and linearity limitations, transmitting the data in a BBoF transmission scheme is the most adequate approach. BBoF is a very well-known way of transmitting digital signals through optical fiber. It consists of directly transmitting the I-Q bitstream from the BS to the RAUs in the form of light pulses, while the wireless signal processing is carried out entirely at the RAU. This scheme is compatible to already deployed optical networks, in which data is typically transmitted in a digital environment, and it presents the highest simplicity in the optical domain. However, the RAUs for BBoF must be designed including additional hardware to process the wireless signals, thus increasing the design complexity and cost.

Data transmission is carried out using purely digital signals. These signals carry the information as a series of discrete data which can only take a finite number of values. The basic element of a digital communication system is the bit, which is the minimum unit of information and has two possible logical values, “1” and “0”. In a binary modulation, the digital signal can only take these two values on each period. In a typical encoding scheme using binary amplitude modulation and non-return-to-zero (NRZ) codification, each bit period, T_B, carries one bit, where the logical 1 is represented by a fixed-amplitude of the carrier signal and an amplitude value of 0 is used to represent the logical 0, as shown in Fig. 2.16.

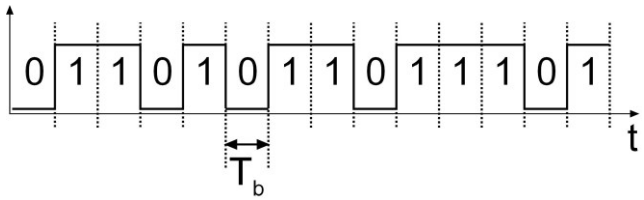

Fig. 2.16. Binary signal with non-return-to-zero codification.

Most optical communication systems are based in a binary amplitude modulation for an easier detection. Typically, encoded data sequences behave as random binary sequences (RBS), being NRZ the data format employed in most high-speed applications, as it is the simplest codification of a bit sequence. In practice, a NRZ signal can be interpreted as a pseudo-random binary sequence (PRBS) with no periodicity. It consists of a binary bit stream where each bit has the same duration of one-bit period, T_B, and is followed by the next bit, without any additional state in between.Following the aforementioned motivations, in this section, a proposal of a 65-nm CMOS TIA architecture for its use in a BBoF DAS using POF is described. It

is based on the TIA presented in [ROY15a], which was previously validated in a 180-nm CMOS technology. This structure is aimed for up to 1.25-Gb/s data transmission using NRZ encoding, thus requiring a TIA bandwidth of 1 GHz when connected to a large area PD. The PD has been modeled with a 14-pF junction capacitance and a responsivity of 0.42 A/W, based on the parameters reported on [DON12], where a large integrated PD for POF is presented. The main target of this proposal is to optimize the sensitivity of the receiver to overcome the huge attenuation of the fiber and thus reach longer link distances.

For the simulations, we will assume the scheme shown in Fig. 2.17. At the transmitter side, a laser generates an optical NRZ signal with a 0-dBm optical power, limited by eye-safety operation requirements. The POF channel is modeled as a linear attenuator with a 0.18 dB/m loss. An additional 1 to 2 dB power loss should be considered because of misalignment of the fiber coupling bot at the transmitter and the receiver side. At the receiver side, the PD is modeled as an optical power-controlled current source with a responsivity of $R_{PD} = 0.42$ A/W and a junction capacitance of 14 pF [DON12], in which a sensitivity[3] of -7.2 dBm for a 1.25 Gb/s transmission with 10^{-12} BER is reported. The PD is connected to the TIA, which is based in a shunt-feedback topology and at its output, the input impedance of the subsequent stage, C_{next}, has been modeled with a 100-fF capacitance.

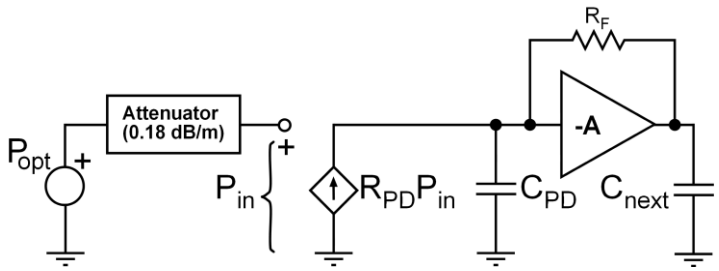

Fig. 2.17. Conceptual scheme of the POF link and schematic diagram for the simulation setup.

The transistor-level schematic of the proposed TIA is shown in Fig. 2.18. It consists of a three cascaded CS stages (M_{iN}, M_{iP}), which are suitable for low-voltage operation, and a feedback resistor, R_F. Three CS stages have been chosen for the following reasons: First, since the CS circuit is an inverting stage, an odd number of stages is required. Secondly, a single stage does not provide enough gain to achieve a high transimpedance. Last, the design complexity using a higher number of stages rises exponentially, since there is a greater number of design variables. Moreover, a higher number of amplifier poles and a larger open-loop gain make it much more difficult to control the system stability.

[3] The sensitivity is defined as the minimum input signal power required to achieve a specific bit error ratio.

To minimize the use of resistive elements that require a large area in the physical implementation, we employ PMOS transistors working in the triode region. These show a similar response, while reducing the area consumption. The TIA has been implemented in a cost-effective 65-nm CMOS technology that supports a 1.2-V supply voltage. To optimize the frequency response, all transistor lengths are set to 65 nm, the minimal length allowed by this technology. A biasing voltage of 0.75 V is kept over the whole signal path, while the transistor widths have been chosen and optimized to minimize the input noise and to achieve a frequency response with a high transimpedance and a 1-GHz bandwidth with a minimal power consumption.

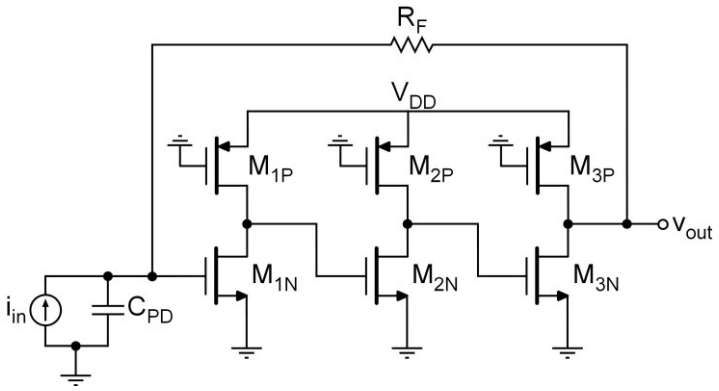

Fig. 2.18. Schematic diagram of the transimpedance amplifier for POF communications.

The main noise sources of the voltage amplifier correspond to the devices of the first CS stage. As studied above (2.17), the way to obtain a lower input noise is to increase the transconductance of M_1. Therefore, a very wide NMOS transistor has been chosen for the first stage. Under this requirement, the second and third stage have been optimized to achieve the highest sensitivity while keeping a low power consumption. In particular, the design variables and main characteristics are summarized in Table 2-2 and Table 2-3.

To obtain these results, simulations have been carried out using Spectre simulator for the TSMC 65-nm CMOS technology. By integrating the output-voltage noise response, which is shown in Fig. 2.19, the sensitivity for a given BER of 10^{-12} has been calculated using the following expression

$$S(\mathrm{dBm}) = 10\log\left(\frac{7 \cdot v_{n,RMS}(\mathrm{V})}{R_T(\Omega) \cdot R_{PD}(\mathrm{A/mW})}\right) \qquad (2.41)$$

where $v_{n,RMS}$ is the total output integrated RMS (root mean square) noise and 7 is the ratio between the signal amplitude and the RMS noise for which, according to the probability theory, a BER of 10^{-12} is obtained [PHO12, RAZ12]. Fig. 2.20 shows the eye diagram of the output signal, corresponding to an optical input signal with -11 dBm and -5 dBm power, which correspond to around 60 and 25 meters of POF, respectively, considering an average loss of 0.18 dB/m. It has been modulated using a PRBS signal with a length of 2^{31}-1 at a bitrate of 1.25 Gb/s with NRZ

encoding. Examining the eye diagram, we can see an RMS deterministic jitter of 1 % and 5.6 % for an optical input power of -11 and -5 dBm, respectively.

W_{N1}	15 µm	W_{N2}	3 µm	W_{N3}	15 µm
W_{P1}	5 µm	W_{P2}	1 µm	W_{P3}	5 µm

Table 2-2 Design parameters for the 65-nm TIA with a feedback resistor, $R_F = 1500\ \Omega$.

Parameter	Value
3-dB Bandwidth	1.02 GHz
Transimpedance	1500 Ω
Sensitivity (BER = 10^{-12})	-11 dBm
Power consumption	2.9 mW

Table 2-3. Summary of the performance of the 65-nm feedback TIA.

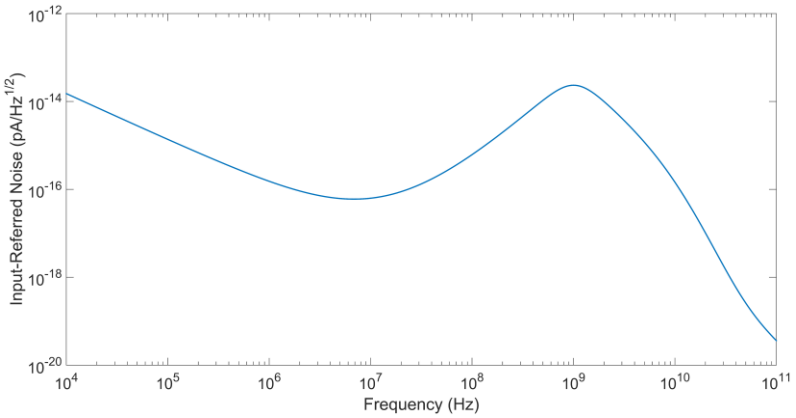

Fig. 2.19. Output noise response of the TIA.

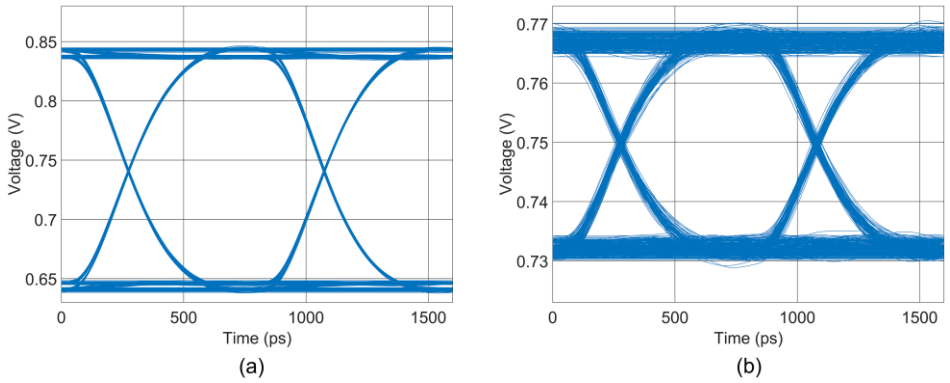

Fig. 2.20. Eye diagram using a PRBS signal at 1.25 Gb/s with (a) -11 dBm and (b) -5 dBm optical power.

2.3.1.1 *Sliced photodiode applied to the BB-TIA*

Let us now apply the sliced photodiode technique to the proposed TIA design. As described in section 2.2.2, we divide the PD in N equal pieces and replicate the TIA N times as shown in Fig. 2.21, modifying the feedback resistor to be N times larger and using the same core voltage amplifier as in the original design. By combining the output signals of each TIA, we should see a decrease of the contribution of all the voltage amplifier noise sources to the input-referred noise, while the contribution of the feedback resistors should remain constant. Therefore, a decrease of the f^2-noise contribution should be achieved, leading to a better SNR and thus a higher sensitivity [ROY21].

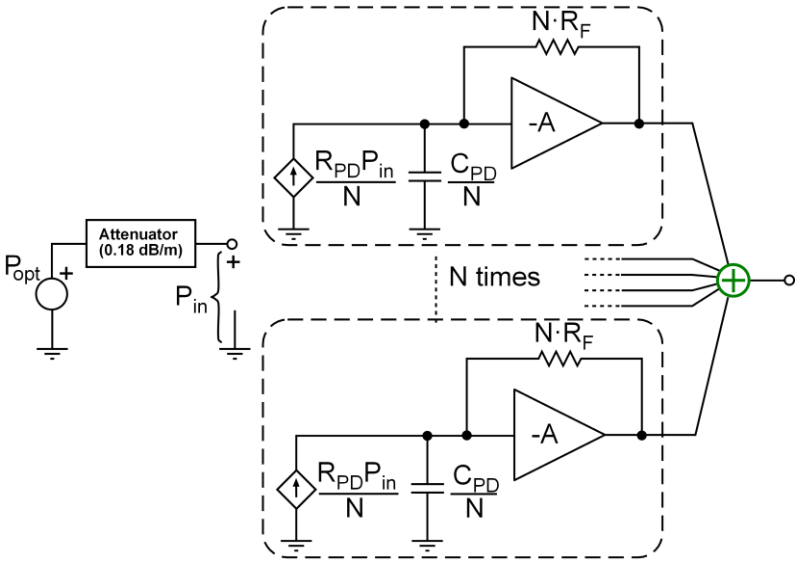

Fig. 2.21. Schematic diagram of the simulation test bench of the sliced PD technique.

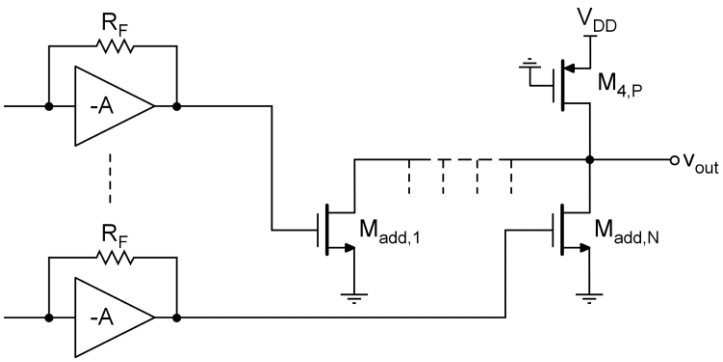

Fig. 2.22. Schematic diagram of the adder based on a common-source stage.

The sliced PD technique has been applied dividing the PD in N pieces, choosing powers of 2 for the values of N, up to 16. As shown in Fig. 2.22, an adder based on

an output buffer using a CS stage has been implemented to combine the output signals of each TIA. As a first approximation, the PD is divided in N equal pieces and the TIA is replicated N times, using a feedback resistor N times larger and the same voltage amplifier as in the original design. By combining the output signals of each TIA, we can increase the SNR by a factor of roughly $\sqrt{N}$. Since the voltage signals are summed linearly and the uncorrelated noise sum is quadratic, the EIN is effectively reduced, thus improving the sensitivity of the PD read-out.

The sliced PD technique has been applied dividing the PD in N pieces, choosing powers of 2 for the values of N, up to 16. To combine the output signals of each TIA, we employ the output buffer, splitting the transistor M_{add}, shown in Fig. 2.22 in N equal transistors to implement a simple signal adder. Since the transconductance of each transistor is now divided by N, the output signal should remain like the single-PD case, but the quadratic sum of the noise contributions should provide an increase in the SNR.

Fig. 2.23 shows the equivalent input-referred noise response, clearly exhibiting a great decrease of the spectral density at high-frequencies for higher N values. A decrease of the f^2-noise contribution is achieved, leading to a better SNR and thus a higher sensitivity.

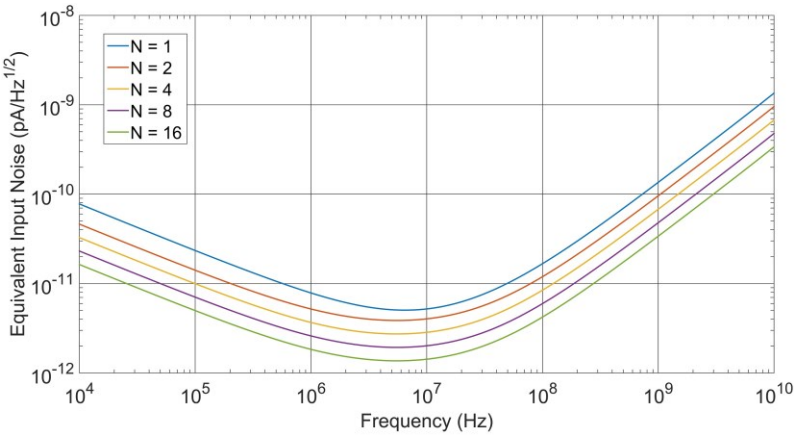

Fig. 2.23. Input-referred current noise applying the sliced photodiode technique for different number of pieces.

Table 2-4 summarizes the key performance parameters of the front-end obtained by slicing the PD in different number of pieces. There is a remarkable increase of the sensitivity, measured for a BER of 10^{-12}, from -11 dBm using the traditional single-PD approach to -15.8 dBm by slicing the PD in 16 pieces. This means that using this technique we obtain an improvement of 4.8 dBm. Notice that the noise will be 3 times lower even though the bandwidth has increased by 32 %. The main drawback is the power consumption, which increases by a factor of N. As mentioned above, the TIA design is bound to the intrinsic capacitance of the PD. After slicing the PD, the capacitance is lowered by a factor of N, therefore, in a second case, we have

optimized the TIA given $N = 16$ to compare the performance of an optimized 16-pieces sliced-PD versus the optimized single-PD approach. Table 2-5 summarizes the design parameters of each optimized design approach for a 1-GHz BW and compares their performances.

Parameter	N=1	2	4	8	16
R_T (dBΩ)	75.7	75.7	75.8	75.8	75.7
BW (GHz)	1.02	1.20	1.31	1.34	1.35
Input RMS Noise (μA)	4.74	3.89	2.57	1.89	1.58
Sensitivity (dBm)	-11.0	-11.8	-13.7	-15.0	-15.8
Power (mW)	2.9	5.8	11.5	23	46

Table 2-4. Summary of the simulation results using the sliced-PD technique with different number of slices.

Parameter	Single PD Fixed BW	Single PD Fixed Power	16 Sliced-PD
R_T (dBΩ)	75.7	80.3	84.4
BW (GHz)	1.02	1.21	1.02
Input RMS Noise (μA)	4.74	1.82	0.78
Sensitivity (dBm)	-11.0	-15.1	-18.9
Power (mW)	2.9	38.8	38.8

Table 2-5. Comparison of the simulation results with optimized parameters for both approaches, the traditional approach and applying the sliced-PD, respectively.

A much higher transimpedance can be achieved after optimizing the TIA for the 16-piece sliced-PD case. Although the increase in power consumption by a factor of 13 cannot be ignored, it is remarkable that the input RMS noise is lowered by a factor of 6, improving the sensitivity by almost 8 dBm.

It is noteworthy that an optimized design with a single PD and the same power budget does not improve performance to the same extent as the proposed technique. This technique is a good candidate to improve the sensitivity of optical receivers with high junction capacitance integrated PDs. It does not depend on the transistor-level architecture of the TIA, which makes it compatible with almost every TIA design.

2.3.2 Highly Linear TIA for RFoF Communications (RF-TIA)

BBoF is the most employed optical transmission methods. However, since it transports a purely digital signal, it requires a complex design of the RAUs. On the opposite side, transmitting analog signals strongly simplifies the design of the RAUs. Among these, the simplest analog signal transport scheme in a fiber-fed DAS is the RFoF scheme, which consists of the direct transmission of the wireless signals through the optical fiber without any further signal processing. The signal is modulated at the wireless carrier frequency onto an optical carrier and it is transported through the optical fiber in an analog format. Signal generation, modulation and processing is centralized at the BS, which enables simple and low-cost design of the RAUs, as both downlink and uplink must only amplify and convert the RF-modulated light to a wireless RF signal and vice versa, without any additional signal processing. Overall, RFoF transmission is a good approach to reduce the cost of installing a DAS, since cost-effective RAUs can be designed [VYA12]. These systems, however, require a much higher linearity of all the devices than BBoF to transmit the signal properly and they show distance limitations when transmitting several WLAN standards. It is well known that the high modal and chromatic dispersion of the fiber at such frequencies degrades the RF power of the optically modulated signals. Therefore, the use of POF is excluded for RFoF at the GHz range, and GOF is the only available technology for these signal transport schemes. Moreover, one of the main drawbacks of RFoF systems is that they require high-speed circuit design and high-performance photonic devices, therefore increasing the power consumption and the overall cost of the DAS.

The main requirements for a RAU downlink using a RFoF scheme are low noise, high linearity, and wide bandwidth to achieve an appropriate opto-electrical conversion. Consequently, an optical front-end must be available to bring these characteristics together, thus both high-speed photodiode and TIA are required in the design [TAL15, YOO09, KO13]. In this section, we propose the design of a low-noise transimpedance amplifier with highly linear performance aimed for use in a RAU downlink for short range communications using a RFoF scheme. It will be designed in a 180-nm RF CMOS technology, which is specifically aimed for high-speed RF design while minimizing electromagnetic interferences to the devices. The TIA design targets the transmission of a wireless Wi-Fi signal, employing the standard 802.11g, which allows for a 54 Mb/s throughput with a wireless quadrature signal (IQ) modulation scheme up to 64-QAM (64-level quadrature amplitude modulation).

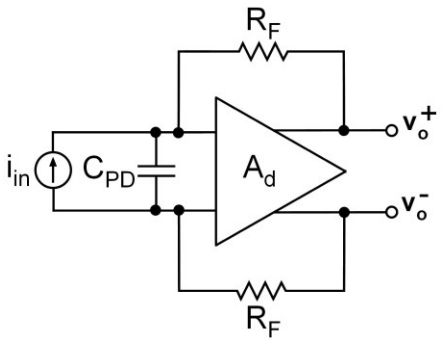

Fig. 2.24. Conceptual scheme of a differential shunt feedback TIA.

A shunt-shunt feedback TIA topology has been chosen, as it shows the best performance for this kind of applications [RAZ12]. To reduce the effect of supply and substrate noise, a fully-differential configuration has been used. This topology reduces second order harmonics and intermodulation products, thus reducing the error vector magnitude (EVM) as it improves the overall linearity [KAZ09, PAL91]. In a differential feedback TIA configuration as shown in Fig. 2.24, the transimpedance, using the second order approximation, can be written as

$$R_T = \frac{v_o^+ - v_o^-}{i_{in}} = -\frac{2R_F}{1 + \frac{2R_F C_{PD}}{A_d} s + \frac{2R_F C_{PD}}{A_d \omega_A} s^2} \qquad (2.42)$$

where A_d and ω_A are the differential open-loop gain and dominant pole frequency of the voltage amplifier, respectively.

Regarding the RF signal, QAM provides several benefits for data transmission [BRI08]. As the QAM order increases, a higher data rate can be achieved. However, for higher orders of QAM the noise margin must be smaller to preserve a low BER. Therefore, a TIA aimed for a high order QAM such as 64-QAM must present a very low noise and a very high linearity [ROY16a]. These restrictions strongly limit the dynamic range of the optical receiver to few dBm. Therefore, to extend the input range, the design of the TIA has been firstly optimized to exhibit the lowest possible equivalent input noise (EIN) and, secondly, the feedback resistor has been substituted by a variable resistor to implement a gain control.

By means of a programmable feedback resistor, the transimpedance can be reduced for larger input signals, thus preventing the amplifier from reaching compression or saturation to maintain low non-linear distortions. However, as explained in Section 2.1.3, when R_F decreases, the quality factor of the second-order response, increases, so that a compensation must be included to perform the transimpedance gain control. According to the Q factor, which, for a differential TIA is written as

$$Q = \sqrt{\frac{A_d}{2R_F C_{PD} \omega_A}} \qquad (2.43)$$

we can maintain Q constant if the reduction of R_F brings with it a simultaneous decrease of the differential open-loop voltage gain, A_d, for which a programmable gain voltage amplifier (PGA) will be employed.

The implementation of the fully-differential TIA with programmable transimpedance consists of three cascaded differential pairs and a negative feedback loop as shown in Fig. 2.25. The design has been optimized for a commercially-available external high-bandwidth InGaAs PIN photodiode with a parasitic junction capacitance of 0.45 pF. The PD is reverse biased with a high reverse voltage to operate in the photoconductive mode, which reduces the response time because the depletion layer width is increased, therefore decreasing the intrinsic junction capacitance [GRA95]. Furthermore, this bias scheme could be used as a signal strength detector for the implementation of a feed-forward gain control of the TIA by monitoring the PD anode voltage. The TIA is AC coupled with 1-nF capacitors, C_C, and the devices have been sized to achieve a 3-dB BW of least 2.5 GHz with high transimpedance and low noise [ROY18a].

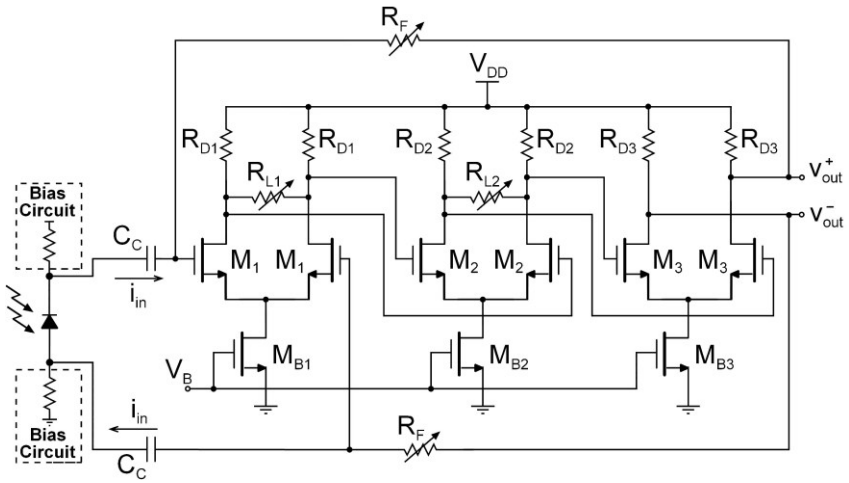

Fig. 2.25. Schematic of the fully differential TIA with programmable transimpedance.

To provide gain programmability to the core voltage amplifier and maintain constant Q against R_F changes, the first two differential pairs have been modified, adding programmable load resistors, $R_{L,i}$ between the outputs. The open-loop gain, of the modified differential pair, shown in Fig. 2.26 follows the approximated expression

$$A_d = g_m \cdot \left(R_D \parallel \frac{R_L}{2}\right) \tag{2.44}$$

and the overall open-loop gain of the TIA core amplifier is estimated by

$$A_d = g_{m1} \cdot \left(R_{D1} \parallel \frac{R_{L1}}{2}\right) g_{m2} \cdot \left(R_{D2} \parallel \frac{R_{L2}}{2}\right) g_{m3} R_{D3} \tag{2.45}$$

This implementation of the variable load resistors is used to accordingly modify the open-loop gain, A_d, of the voltage amplifier with the advantage of maintaining unmodified operating points of the differential pairs and a constant power consumption, independently of the value of R_L.

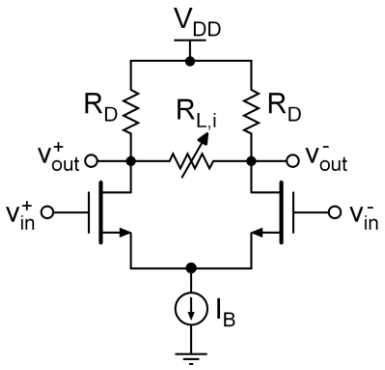

Fig. 2.26. Differential pair including a load resistor.

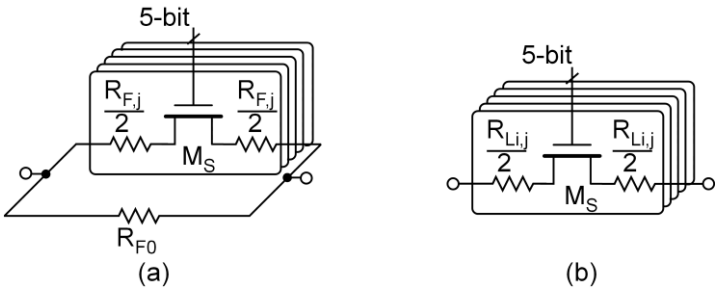

Fig. 2.27. Implementation of the 5-bit programmable resistor arrays (a) feedback resistor, R_F and (b) load resistors, $R_{L(i)}$.

In the proposed design, 5-bit thermometer-coded switched-resistor arrays, $R_{F,j}$, and $R_{L(1,2),j}$, shown in Fig. 2.27, have been included to achieve, respectively, a simultaneous control of the transimpedance and the open-loop gain. The resistors sizing has been adjusted to maintain a constant bandwidth in all the transimpedance configurations. With a linear-in-dB digitally programmability feedback resistor, the input dynamic range can be extended, by reducing the transimpedance for larger input signals to avoid saturation and maintain a low non-linear distortion. The programmable gain also reduces the impact of process, voltage, and temperature (PVT) variations and allows the use of simpler post-amplifying configurations, such as a limiting amplifier instead of a variable-gain amplifier (VGA) [GAR10, AZN11b].

The complete design parameters and transistors sizing is summarized in Table 2-6. The transimpedance can be programmed from 45 dBΩ up to 65 dBΩ and the 5-bit thermometer-coded resistor array has been adjusted to provide a robust linear-in-dB gain control, with 4-dB steps. The double control of the transimpedance and the

open-loop gain guarantees a flat frequency response, independent of the transimpedance value.

Device	Parameter	Value
Differential pair 1	W_1/L_1	250 µm / 180 nm
	W_{B1}/L_{B1}	400 µm / 500 nm
	R_{D1}	200 Ω
Differential pair 2	W_2/L_2	18 µm / 180 nm
	W_{B2}/L_{B2}	400 µm / 500 nm
	R_{D2}	250 Ω
Differential pair 3	W_3/L_3	18 µm / 180 nm
	W_{B3}/L_{B3}	400 µm / 500 nm
	R_{D3}	250 Ω
Load resistors	$R_{L1,1} = R_{L2,1}$	1200 Ω
	$R_{L1,2} = R_{L2,2}$	1000 Ω
	$R_{L1,3} = R_{L2,3}$	1000 Ω
	$R_{L1,4} = R_{L2,4}$	800 Ω
	$R_{L1,5} = R_{L2,5}$	1100 Ω
Feedback resistor	R_{F0}	1000 Ω
	R_{F1}	1750 Ω
	R_{F2}	1200 Ω
	R_{F3}	800 Ω
	R_{F4}	800 Ω
	R_{F5}	800 Ω

Table 2-6. Values of the TIA devices and transistors sizing.

Fig. 2.28 and Fig. 2.29 show the frequency response and the input-referred noise of the TIA, respectively. At 2.5 GHz, the TIA shows an input-referred current spectral density of 10 pA/$\sqrt{\text{Hz}}$, determining the minimum input optical power. To perform linearity measurements, we use the demodulation of an 802.11g 54 Mb/s data transmission at 2.4 GHz, which uses multi-carrier orthogonal frequency-division multiplexation (OFDM) modulated with 64-QAM. Fig. 2.30 shows the normalized constellation diagram of the demodulated signal, where the signal at the output of the proposed TIA exhibits an EVM of 2% to an input signal of -9 dBm optical power

with 20% optical modulation index at the maximum gain configuration of 65 dBΩ. As it is well known, nonlinearities increase for larger signals, however, making use of the 20-dBΩ transimpedance gain control, the input dynamic range is extended, and input signals as large as +1 dBm optical power can be transmitted with an EVM lower than 2%. This is the lowest EVM compared to the ones reported in [YOO09, KO13, DES15], and, more importantly, it is achieved for a wide input dynamic range of 10 dBm optical power, compared to the 3 dBm and 5 dBm ranges reported, respectively, in [YOO09] and [KO13].

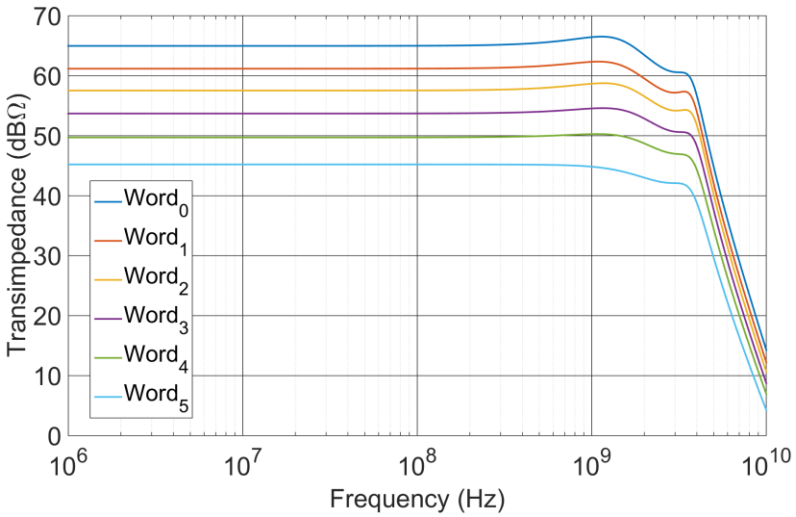

Fig. 2.28. Frequency response of the proposed TIA with double control of transimpedance and open-loop gain.

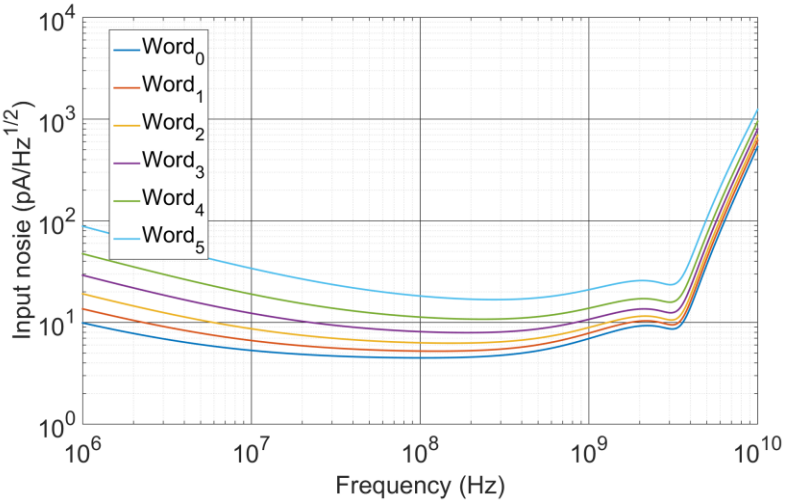

Fig. 2.29. Input-referred noise of the proposed TIA at each transimpedance configuration.

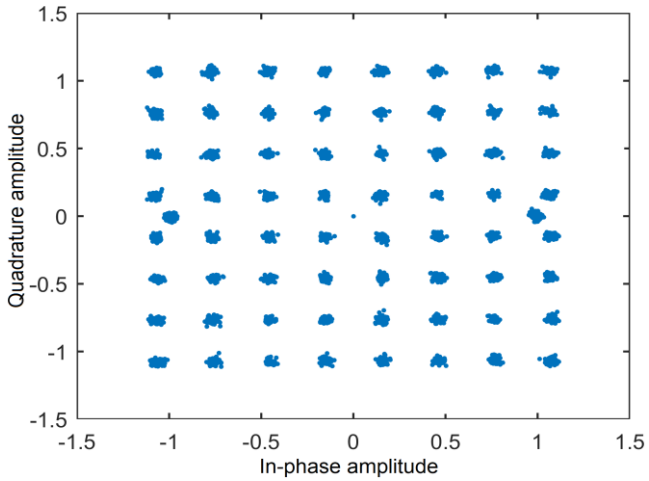

Fig. 2.30. Constellation diagram of the demodulated signal at the maximum transimpedance configuration of 65 dBΩ with -9 dBm optical input power at 20% modulation index.

In Table 2-7, the main parameters and simulation results for our proposal are summarized and compared to recently published TIAs for RFoF applications. Since the integrated noise is not provided, to compare the performance of the proposed TIA with other alternatives, we define the following figure of merit (FoM)

$$FoM = \frac{Transimpedance(\Omega) \cdot BW(GHz)}{Power\ Consumption\ (mW)} \qquad (2.46)$$

Parameter	[YOO09]	[KO13]	[DES15]	This work
Technology	130-nm CMOS	180-nm CMOS	150-nm PHEMT	180-nm RF CMOS
Photodiode Technology	Integrated APD	Integrated APD	External PIN	External PIN
Supply Voltage	1.2 V	1.8 V	5 V	1.8 V
Transimpedance	54 dBΩ	62 dBΩ	46 dBΩ	45-65 dBΩ
Frequency of Operation	2.5 GHz	5.2-5.8 GHz	12 GHz	2.5 GHz
Equivalent Input Noise Current Density	N/A	7 pA/$\sqrt{\text{Hz}}$	21 pA/$\sqrt{\text{Hz}}$	10 pA/$\sqrt{\text{Hz}}$
EVM	3.9 %	2.5 %	3 %	2 %
TIA Power Consumption	18 mW	156 mW	100 mW	26 mW
FoM	70	47	24	171

Table 2-7. Summary of the simulation results and comparison with other RFoF transimpedance amplifiers.

As shown in Table 2-7, the proposed TIA achieves a much better FoM, thanks to the higher transimpedance and the low power consumption of 26 mW for the maximum gain. It is also the only TIA with controllable transimpedance, extending the input dynamic range for which high linearity is achieved. Another advantage of this design

is the compatibility with external PIN photodiodes, which present a much higher junction capacitance, of the order of 0.5 pF, compared to the extremely low 35-fF integrated photodiode presented in [KO13].

The above simulation results obtained high-level models of the devices are usually reliable and accurate. However, to predict the variability of the circuit behavior due to the manufacturing process, statistical simulations must be performed. Therefore, to complete the characterization of the proposed design, Monte Carlo simulations have been carried out. For the test, a total of 2400 simulations have been performed, 400 for each transimpedance state. Results for bandwidth are shown in Fig. 2.31. The transimpedance results, shown in Fig. 2.32 exhibit a worse robustness at low transimpedance configurations, while the standard deviation at high transimpedance configurations is considerably lower, of only 0.5 dBΩ.

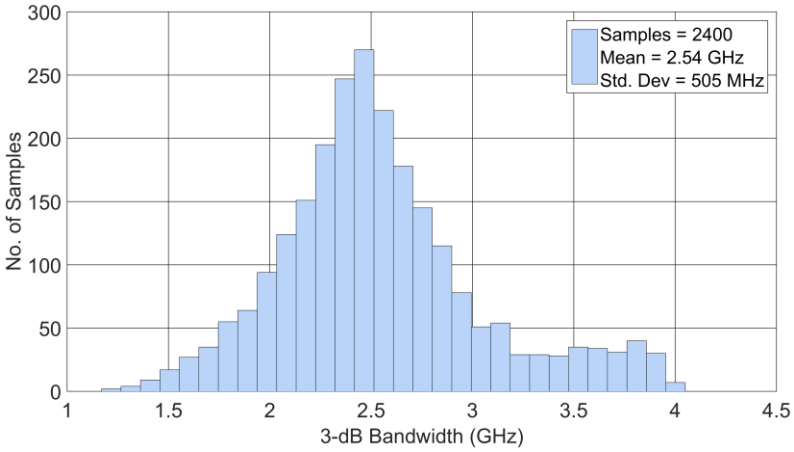

Fig. 2.31. Monte Carlo simulation results for bandwidth at any transimpedance configuration.

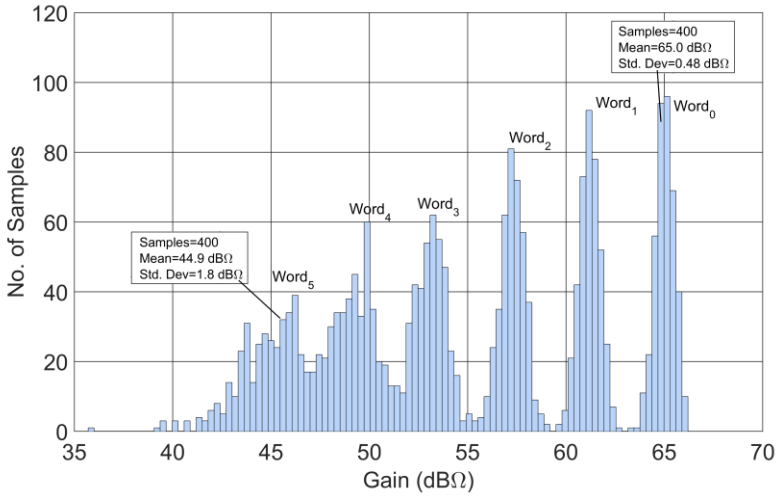

Fig. 2.32. Monte Carlo simulation results for each transimpedance state.

2.3.3 Transimpedance Amplifier for RF Overlay in PON (CATV-TIA)

The use of the RFoF communication scheme is not limited to feeding RAUs in distributed antenna systems. It can also be employed to increase the data capacity in the already deployed long-reach passive optical networks (PON) with small modifications and nearly zero cost, using RF overlay. In this section, we study the implementation of a differential TIA, based on the previous topology, in an RF optical receiver for video broadcasting.

A PON consists of an optical network where all the elements between the optical line termination (OLT) and the optical network terminals (ONT) are passive. This layout, shown in Fig. 2.33, increases the simplicity, reduces power consumption, fiber cable and maintenance needs, therefore the overall cost is minimized, which makes these networks a very cost-effective approach. PON is a point to multipoint network that consists of two main elements: The optical fiber, and optical splitters.

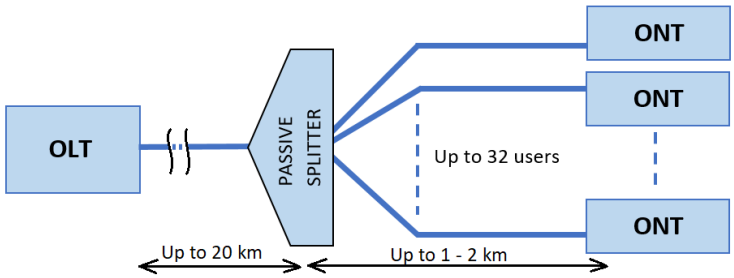

Fig. 2.33. Block diagram of a 1/32 passive optical network (PON).

The light is transmitted with different wavelengths for downstream and upstream, through a single fiber, covering long distances. When it is close enough to the users, an optical splitter divides the power evenly to up to 32 users. This way, the total length of deployed fiber is minimized compared to a point-to-point network, where we would need approximately 32 times the fiber that is needed with this configuration. At the ONT, each user will receive all the transmitted data, and each receiver will only select the data package that corresponds to the user, ignoring the rest of it. This is the main disadvantage of PON: each ONT is receiving a lot of data, but only a small fraction of it, corresponds to the user, which implies a huge limitation in bitrate.

In this context, the RF overlay can be a good approach to increase the downstream data capacity. As shown in Fig. 2.34, it consists of adding a second downstream channel for community access television (CATV) broadcasting, modulated in a different wavelength, the third lambda, typically in the 1550-nm range. The video contents are inserted in the fiber directly modulating a laser with the RF signal. This allows the transmission of over 100 TV channels without any interferences with the IP contents, since they are transmitted in a different wavelength. One of the main advantages of using this second downstream channel is that every user has access to its full BW and not only a fraction of it [BRI08].

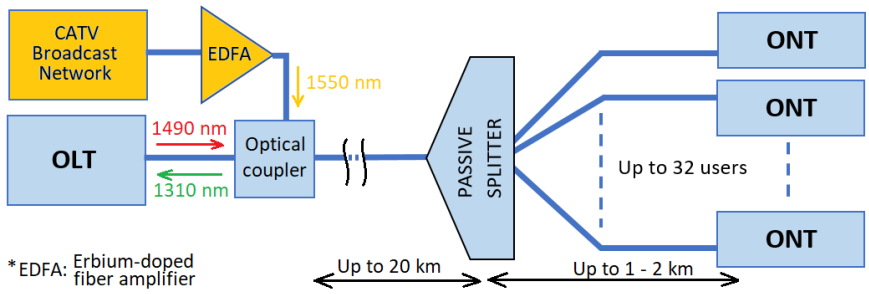

Fig. 2.34. Block diagram of a 1/32 PON using RF Overlay to broadcast CATV.

At the ONT side, the different wavelengths are split using a triplexer, while the receiver consists of two independent optical front-ends, one for each downstream channel. The CATV receiver must feature low noise and high linearity to provide a signal with enough quality for an input range from -6 dBm to +2 dBm [BRI08]. The TIA frequency response must cover the typical bandwidth of CATV communications, which goes from 47 MHz to 870 MHz. Moreover, since different users might receive different signal power, the front-end should be gain-controllable, typically with a variable gain amplifier (VGA) or a variable voltage attenuator (VVA), which can be tuned with the sensed average input power, to ensure a high input range. Additionally, as the output signal is sent through a coaxial cable that is plugged to the TV, an output buffer is needed and the front-end should also feature equalization to deal with the higher attenuation of the transmission channel at higher frequencies [BRI08]. A typical configuration of CATV receiver using VVA is shown in Fig. 2.35.

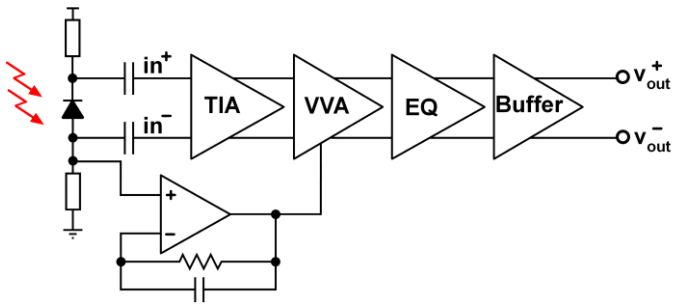

Fig. 2.35. Conceptual block diagram of a typical CATV receiver.

Because of the wide input power range of the CATV signal, using a fixed-transimpedance TIA requires high voltage operation to achieve both low noise (lower than 6 pA/$\sqrt{\text{Hz}}$) at low-power input signals and high linearity for high-power input signals, and these receivers are typically designed in PHEMT or HBT technologies [ZHA11, KAM13]. In this proposal, the VVA functionality is integrated in the TIA with programmable transimpedance. This way, a high transimpedance can be achieved to perform low noise for low-power input signals, while the voltage swing at the output of the TIA for high input power signals does not reach compression or saturation, therefore allowing the TIA to achieve high linearity in a low voltage technology such as 180-nm RF CMOS.

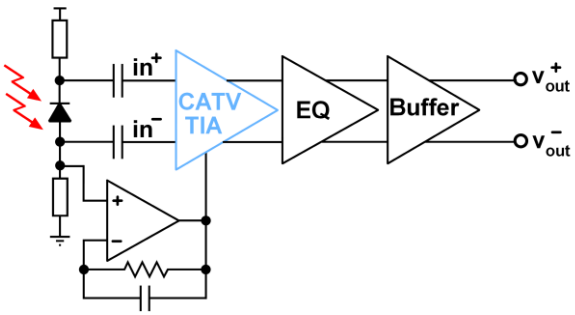

Fig. 2.36. Block diagram of the proposed CATV receiver using a TIA with integrated programmable transimpedance.

The proposed CATV-TIA topology follows the same considerations of the RFoF-TIA. It consists of a differential feedback topology, which shows a better linearity and achieves high transimpedance with low noise level [SAC05, ATE13], and the core voltage is also based in cascaded differential pairs. However, in this case, the goal BW is considerably lower than for RFoF Wi-Fi transmission, therefore, the core voltage consists of only two cascaded differential pairs to lower the open-loop gain and reduce system instability issues.

The implementation of the variable transimpedance is performed with a programmable feedback resistor which consists of a resistor and a digitally-controlled PMOS transistor array, $M_{F,i}$, as shown in Fig. 2.37. The advantage of using a digitally-controlled PMOS array over a single transistor with analog control, is that this way the overdrive voltage is maximized, therefore the transistors work in the ohmic region which leads to a better linear performance, improving the linearity of the TIA [SAN07, RAJ08, AHM15]. Similarly, the open-loop gain control has been implemented with a programmable load resistor in the first differential pair, using a PMOS transistor array, $M_{L,i}$.

The sizing of the transistors has been chosen in order to achieve a fine transimpedance control with steps between 0.3 and 0.9 dB over the entire 18-dB transimpedance control range, thus 6 binary-scaled PMOS transistors have been integrated for each programmable array. The TIA presents a flat frequency response over the frequency range of interest, using a single control voltage, V_{AGC}, for both feedback and load arrays. The control voltage, V_{AGC}, is obtained by sensing the voltage at the PD cathode, which is proportional to the average received input optical power and is then converted to the digital domain with a 6-bit analog to digital converter.

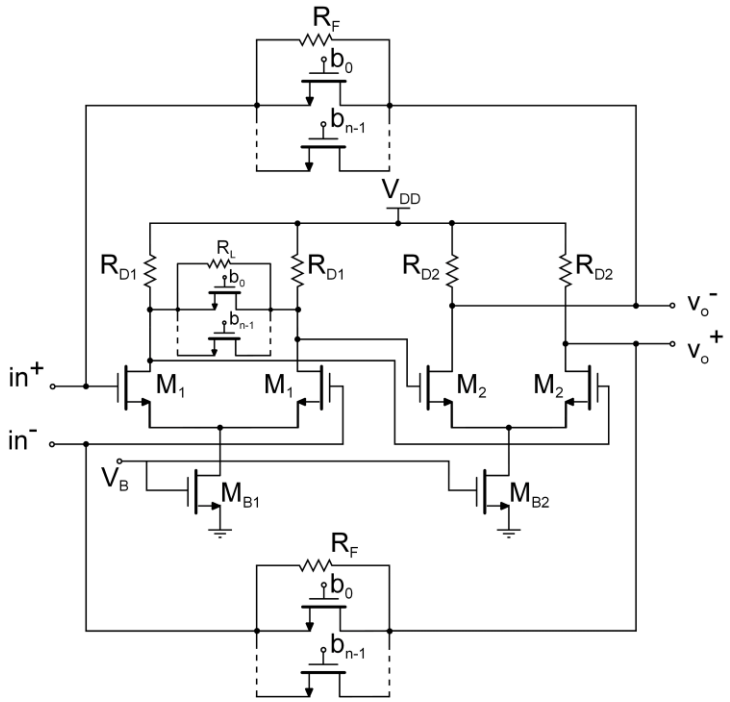

Fig. 2.37. Schematic circuit of the proposed transimpedance amplifier with controllable transimpedance and open-loop gain for CATV.

The CATV TIA has been designed in a 180-nm RF-CMOS technology. The photodiode and its biasing circuitry have been modelled with the parameters of a commercially available PD: A current source with a responsivity of 0.9 A/W at 1550 nm, in parallel with a 0.9-pF capacitor and in series with a 6-nH inductance that represents the parasites of the bonding. The main design parameters and transistors sizing is summarized in Table 2-8.

Device	Parameter	Value
Differential pair 1	W_1/L_1	250 µm / 180 nm
	W_{B1}/L_{B1}	400 µm / 500 nm
	R_{D1}	200 Ω
Differential pair 2	W_2/L_2	18 µm / 180 nm
	W_{B2}/L_{B2}	400 µm / 500 nm
	R_{D2}	250 Ω
Load resistor	R_L	1200 Ω
Feedback resistor	R_{F0}	1000 Ω

Table 2-8. Values of the CATV TIA devices and transistors sizing.

The equivalent input noise response at the maximum transimpedance configuration is shown in Fig. 2.38. For this transimpedance, in the frequency range of operation, the EIN reaches the highest value at 870 MHz with a value of 6 pA/$\sqrt{\text{Hz}}$. As a rule of thumb, this EIN is the required value to achieve a proper carrier-to-noise ratio (CNR) of 53 dB with a 4-MHz-BW TV channel for a -6 dBm input optical signal [BRI08].

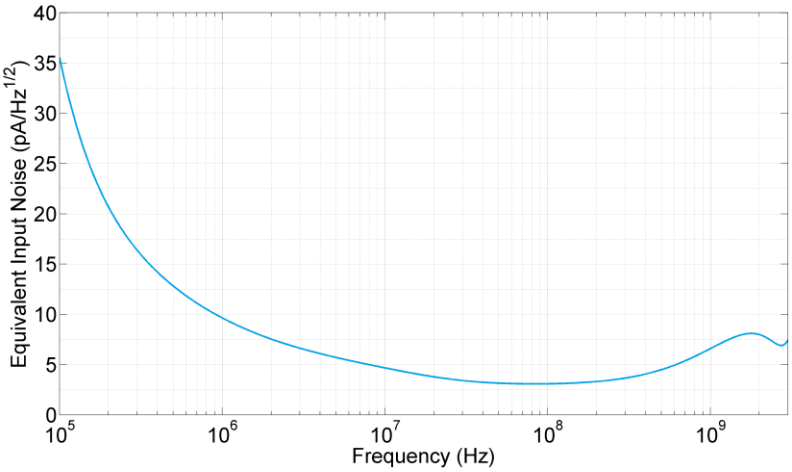

Fig. 2.38. Equivalent input noise of the CATV TIA at the maximum transimpedance configuration.

The frequency response has been measured for each transimpedance configuration, achieving an almost linear-in-dB gain control, as shown in Fig. 2.39. With a power consumption of 27 mW, the TIA achieves a 3-dB bandwidth higher than 1.5 GHz and features a frequency response flatness better than 0.5 dB in the frequency range of interest, from 47 MHz to 870 MHz. Fig. 2.40 exhibits the comparison with a single control of the feedback resistor without open-loop gain compensation. The simulation shows a strong peaking at low transimpedance states as a result of an underdamped system, which entails several stability issues and confirms the need of a simultaneous double gain control. Using the double control of transimpedance and open-loop gain, the TIA achieves a gain control of 18 dBΩ. Therefore, the transimpedance can be reduced to increase the input range to high power signals up to +2 dBm, which is the typical maximum power of CATV transmission.

Lastly, the most relevant parameters of the CATV TIA have been studied in a statistical simulation. These are: (i) The EIN at 870 MHz at the maximum transimpedance configuration, (ii) the 3-dB BW in any transimpedance configuration and (iii) the flatness of the frequency response in the frequency range of operation. The results are shown in Fig. 2.41.

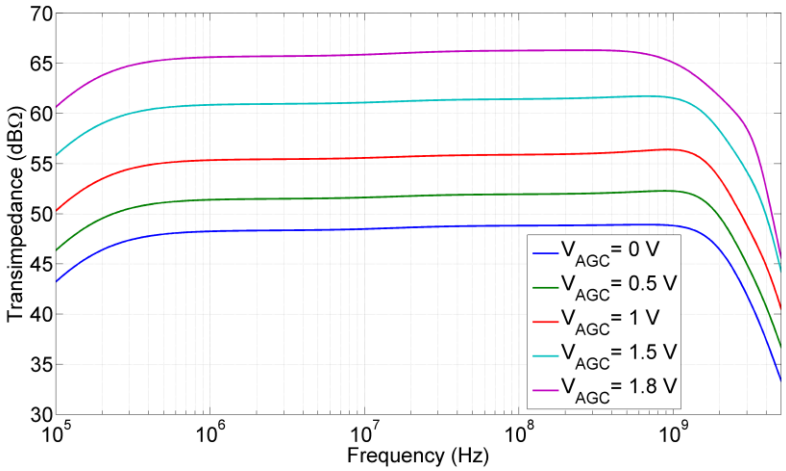

Fig. 2.39. Frequency response of the CATV TIA with double control of transimpedance and open-loop gain.

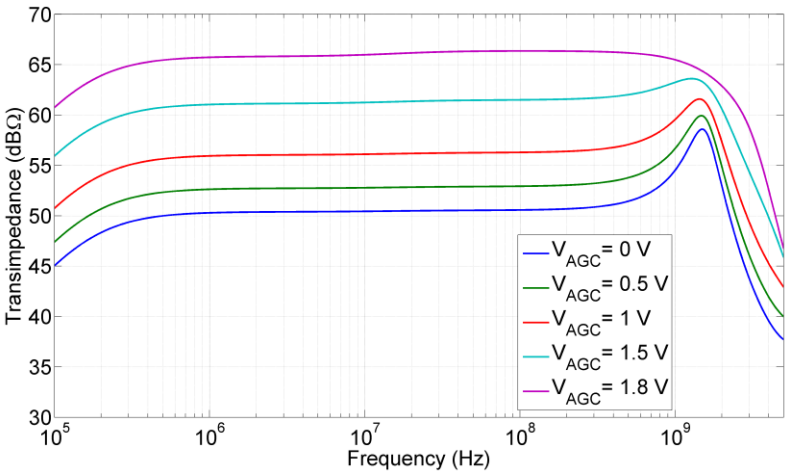

Fig. 2.40. Frequency response of the TIA with a single transimpedance control without open-loop compensation.

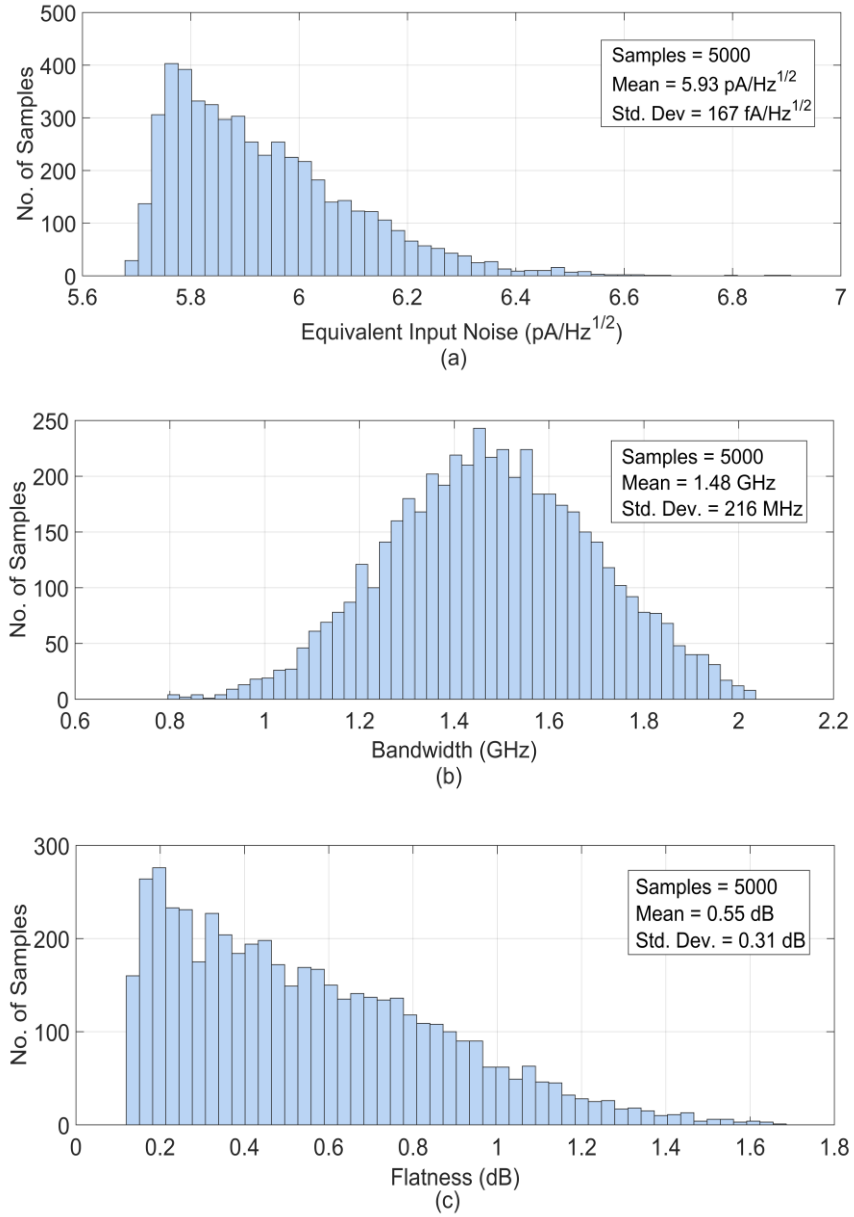

Fig. 2.41. Monte Carlo simulation results for: a) EIN at 870 MHz, b) 3-dB bandwidth and c) flatness of the frequency response from 47 MHz to 870 MHz.

2.3.4 Highly Linear Low-Noise TIA for IFoF Transmission (IF-TIA)

Directly transmitting RF content through optical fiber is conceptually the easiest data transmission format in terms of system complexity. However, as new applications employ higher wireless RF carrier frequencies, the RFoF approach becomes more difficult or even impossible to implement, mainly due to the high-performance requirements on photonic devices, which exponentially increase the overall cost. Upon the scenario of a widespread DAS with a very high number of RAUs deployed, a lower cost alternative is necessary. In this context, the use of an IFoF data transport scheme is gaining attention and it is a good candidate to emerge as a new leading communication standard in wireless signal distribution through optical fiber.

Similar to RFoF, the IFoF scheme present advantages upon BBoF: RAUs for IFoF do not require the implementation of a modulator/demodulator, and therefore, the complexity in the design of the RAU is much simpler than that in BBoF systems, while the power consumption is significantly lower. As in RFoF systems, the signal is generated at the BS with the same modulation format as the RF signal, however in IFoF, a lower carrier frequency is employed, which relaxes the performance requirements of the photonic devices, for both opto-electrical and electro-optical conversion. Moreover, the use of an intermediate frequency minimizes the effect of the fiber dispersion and significantly drops the overall costs, since less expensive fibers such as MMF can be used to transport the signal.

However, the circuitry of the RAU increases with an IFoF scheme with respect to RFoF systems. To recover the original RF signal, the RAU now requires a high-speed mixer with a high image rejection ratio (IRR) and a stable local oscillator (LO). To achieve a high IRR, the mixer typically works with a quadrature signal, which can be obtained with several techniques, such as with hybrid filters or polyphase filters, among others [MAR18a, MAR18b]. The local oscillator is used in both the downlink and the uplink of the RAU, with an accurately tuned frequency to carry out the frequency up-conversion and down-conversion, respectively [SAN17]. To generate the LO signal, a reference signal can be delivered to the RAU optically, allowing a higher flexibility and frequency tuning without the need of implementing quartz crystal oscillators or similar devices in the RAU [SAN17]. As shown in Fig. 2.42, the downlink matching network can be used to isolate data signal from the local oscillator reference.

In this section, we focus on the design of the opto-electrical front-end of the RAU downlink for use in a distributed antenna system using IFoF data transmission. The RAU downlink consists of (1) a photodiode (PD); (2) a transimpedance amplifier; (3) a frequency up-converter to translate the signal from IF to the final RF format, (4) a power amplifier (PA) to provide gain and good matching, and (5) the antenna. In particular, we aim for an optimized design of a fully differential TIA with high linearity and low noise performance. The goal is to show that using an IFoF scheme, the RAU can show better performance, such as lower power consumption and better EVM

than recently published RFoF works. The TIA is based on the topology employed for the proposed RFoF configuration (RF-TIA), it is digitally controllable with a double gain control, maintaining a flat frequency response and constant BW and achieving also a very high input range to enhance the communication system flexibility. The proposed TIA has been fabricated in a 65-nm CMOS process with a 1.2-V voltage supply [ROY19a].

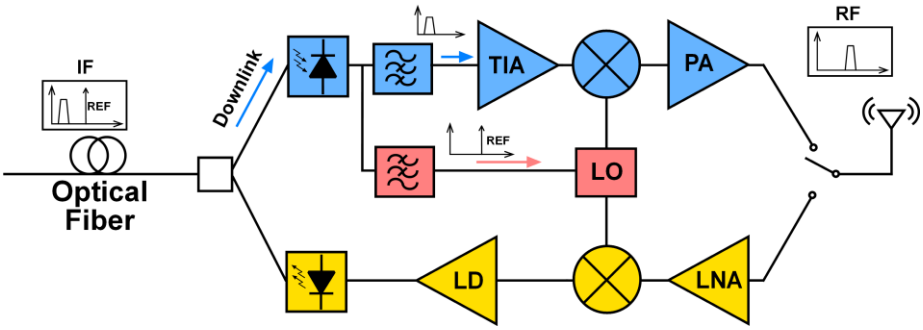

Fig. 2.42. Block diagram of the IFoF RAU using an optical signal to provide the reference to the local oscillator.

One of the main advantages of IFoF is the lower performance requirement of the photonic devices. Nevertheless, the RAU must present low noise and a very high linearity to achieve a low EVM level. Accordingly, the OE front-end must be able to satisfy these performance requirements. The focus of this work is the design of the OE front end, including a low noise TIA with a fully differential implementation to achieve better linearity, using an external 1550 nm PIN photodiode. With the IFoF scheme, the BW requirement and the tradeoff between sensitivity and power consumption is relaxed, so the complexity of the design of the TIA is reduced [ROY19b].

The proposed TIA employs the same transistor configuration as the TIA for RFoF, shown in Fig. 2.25. The transistor sizing and device parameters are sized aiming for short-range wireless transmission with an input IF signal in the range of 100 to 300 MHz. The main purpose of the design is the implementation of the TIA in a RAU downlink capable of performing a reliable transmission of an 802.11a 54 Mb/s WLAN data signal at 5 GHz, which employs a multi-carrier OFDM standard with a 64-QAM modulation.

IFoF communications require a very high linearity, as it has a great impact on the EVM. Therefore, the combination of a differentially-biased PIN PD working in the photoconductive mode and the design of a highly linear TIA is proposed, to achieve a very low EVM for a high input range. The topology employed on the RF TIA has been resized to accomplish with the new requirements of the IFoF front-end. The complete devices parameters are summarized in Table 2-9.

Device	Parameter	Value
Differential pair 1	W_1/L_1	250 µm / 65 nm
	W_{B1}/L_{B1}	400 µm / 65 nm
	R_{D1}	200 Ω
Differential pair 2	W_2/L_2	18 µm / 65 nm
	W_{B2}/L_{B2}	400 µm / 65 nm
	R_{D2}	250 Ω
Differential pair 3	W_3/L_3	18 µm / 65 nm
	W_{B3}/L_{B3}	400 µm / 65 nm
	R_{D3}	250 Ω
Load resistors	$R_{L1,1} = R_{2,1}$	1200 Ω
	$R_{L1,2} = R_{2,2}$	1000 Ω
	$R_{L1,3} = R_{2,3}$	1000 Ω
	$R_{L1,4} = R_{2,4}$	800 Ω
	$R_{L1,5} = R_{2,5}$	1100 Ω
Feedback resistor	R_{F0}	1000 Ω
	R_{F1}	1750 Ω
	R_{F2}	1200 Ω
	R_{F3}	800 Ω
	R_{F4}	800 Ω
	R_{F5}	800 Ω

Table 2-9. Values of the TIA devices and transistors sizing.

To check the functionality of the simultaneous double control, a transistor-level simulation has been carried out with a single control of the feedback resistor to compare it with the frequency response using the double control of both feedback resistor and open-loop gain. As Fig. 2.43 shows, the response without an open-loop gain control shows a frequency peak higher than 4 dB, and the BW increases with lower transimpedance, increasing both the system instability and integrated noise. The solid line shows that, when applying the compensation technique, the frequency response remains flat and the BW is almost constant, which avoids ringing, oscillation, and other instability issues. The complete electrical and optical characterization of the IF TIA will be described in Section 2.4.

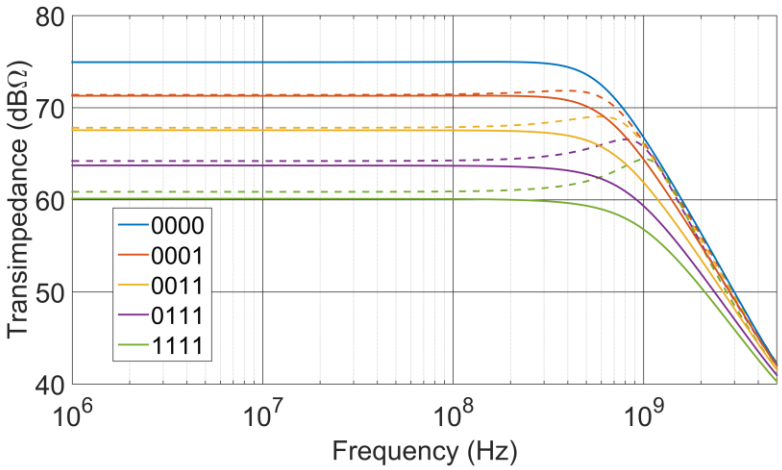

Fig. 2.43. Frequency response of the TIA with simultaneous gain control (solid lines) and single feedback resistor control (dashed lines).

2.4 Experimental Verification of the TIA

In this section, we describe the setup and results of the complete 65-nm IF-TIA experimental characterization. First, we present the chip layout, and we explain the measurement setup, as well as all the components that have been implemented on the chip or externally added to perform the measurements. Then, the measurement methodology and experimental results are presented and discussed. The prototype has been verified both by electrical and optical characterization.

2.4.1 TIA Layout and Fabrication

The correct operation has been tested with post-layout simulations in a 65-nm CMOS technology under the Cadence simulation environment. After checking the proper post-layout performance, the design was sent to fabrication through Europractice-IC. The chip has been fabricated in a 65-nm RF CMOS technology, which operates with a nominal voltage supply of 1.2 V. An output buffer, which we discuss in the following section, has been implemented to provide the output signal. The TIA and buffer are only a single part of the design of an integrated RAU downlink. Fig. 2.44 shows the layout of the downlink and Fig. 2.45 a close-up view on the active area of the TIA+buffer. The dimensions of the full downlink chip are 2 mm x 1.15 mm, whereas the TIA+buffer is placed in a corner of the silicon area and occupy an active area of 115 µm x 130 µm. The output buffer was also fabricated alone in a test cell as shown in Fig. 2.46 with a silicon area of 500 µm x 643 µm, so that its characterization can be performed and de-embedded from the TIA+buffer response.

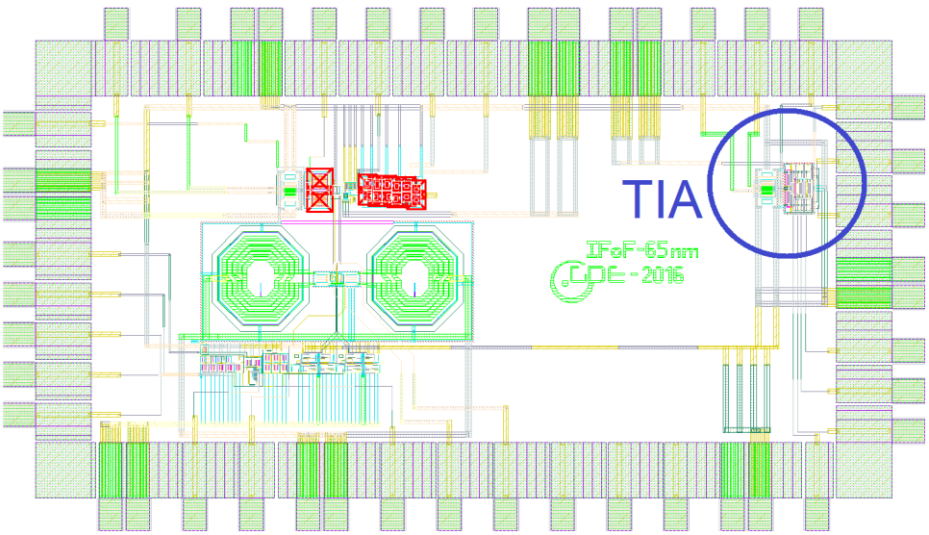

Fig. 2.44. Layout of the RAU downlink.

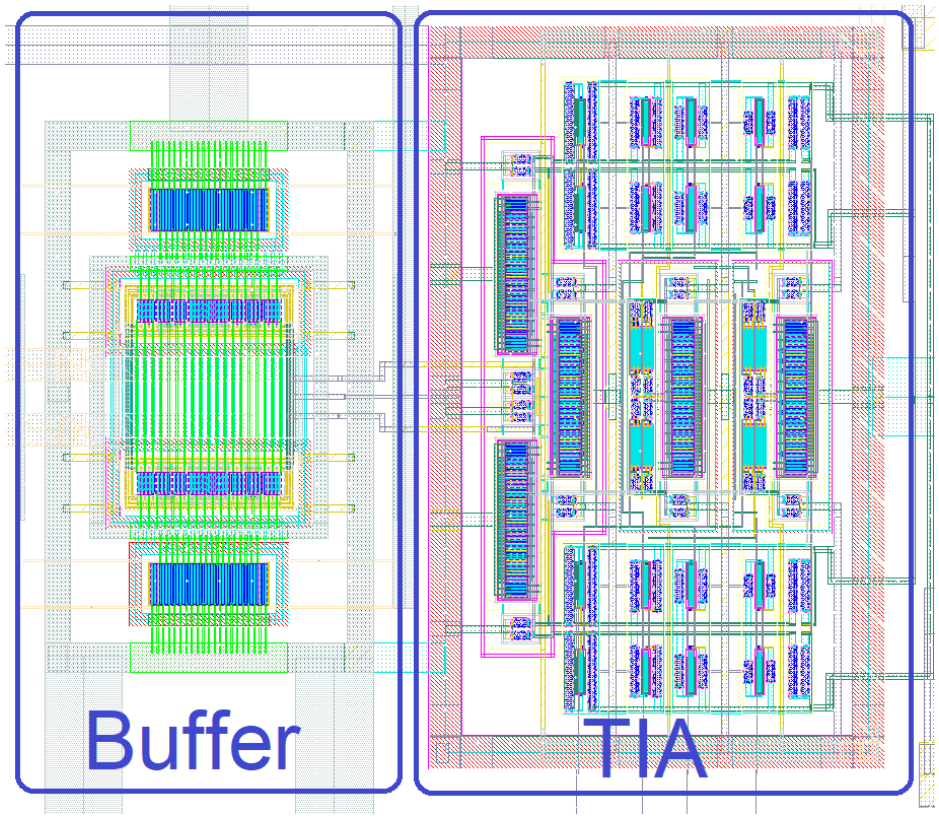

Fig. 2.45. Close-up view of the layout of the TIA and buffer active area.

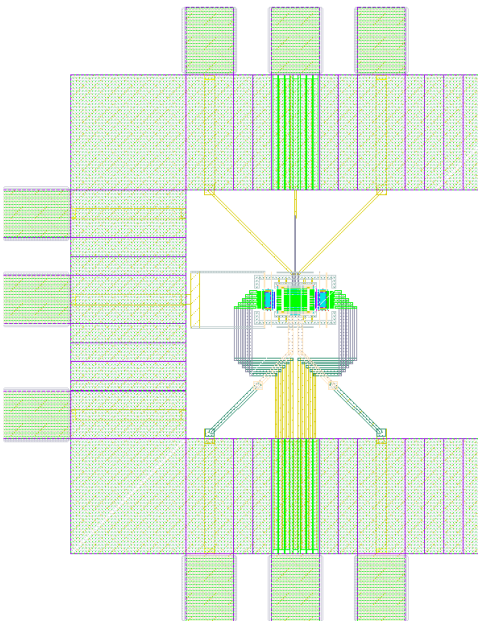

Fig. 2.46. Layout of the output buffer in a test cell.

2.4.2 Output Buffer

To perform the experimental characterization, we need to isolate the TIA output from the measurement devices loads, so that the circuit sees a fixed capacitive load as it will be the case in the fully-integrated receiver. For this purpose, an output buffer as shown in the block diagram of Fig. 2.47 has been implemented. It is described in a transistor-level schematics in Fig. 2.48 and it consists of a differential cascode architecture. To facilitate the design of the output buffer, it has been integrated with open drains and external loads. The bias current is provided using a current mirror and the circuit presents a power consumption of 13 mW from a voltage supply of 1.2 V. In addition to providing circuit isolation between the TIA and the measurement devices, the main target of the buffer is to provide enough driving capability for the 50-Ω input loads.

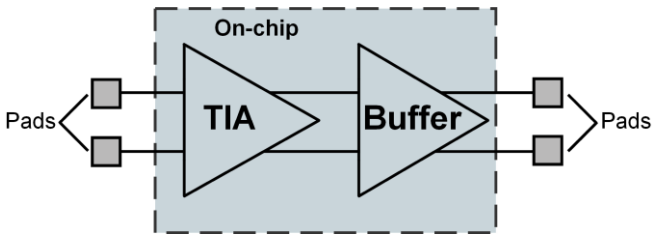

Fig. 2.47. Block diagram of the integrated chip.

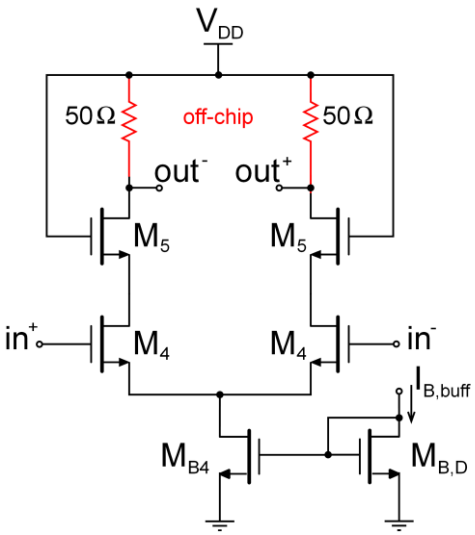

Fig. 2.48. Transistor-level schematic design of the output buffer.

The output buffer has been designed to achieve a very high bandwidth of several GHz and a gain of 0 dB so that it is easier to measure the TIA performance after de-embedding the buffer response. The main design parameters are summarized in Table 2-10.

$\mathbf{M_4}\left(\frac{W}{L}\right)$	$\mathbf{M_5}\left(\frac{W}{L}\right)$	$\mathbf{M_{B4}}\left(\frac{W}{L}\right)$	$\mathbf{M_{BD}}\left(\frac{W}{L}\right)$	$I_{B,buff}$
108 µm / 60 nm	108 µm / 60 nm	432 µm / 240 nm	48 µm / 240 nm	1 mA

Table 2-10. Design parameters for the output buffer.

The test cells of the integrated chip have been encapsulated in their own QFN64 package and a PCB has been designed to carry out the electrical measurements of the output buffer. A picture of the experimental setup is shown in Fig. 2.49 and a detailed picture of the test-cell PCB is shown in Fig. 2.50. The frequency response of the buffer has been obtained using a Rohde & Schwarz ZVL 9 kHz – 6 GHz Network Analyzer by measuring the S-parameters. To convert the output signal of the network analyzer to a differential signal for the buffer input, we employ a passive balun, the PRODYN BIB-100G, with an operation frequency of 250 kHz to 10 GHz [PRO10]. The results of two buffer samples are presented in Fig. 2.51. At low frequencies, up to 3 GHz, the buffer shows a plain gain close to 0 dB and it starts fading at a frequency around 4 GHz, thus it can be considered as an ideal voltage follower for the TIA characterization at the whole frequency range of interest, up to 1 GHz.

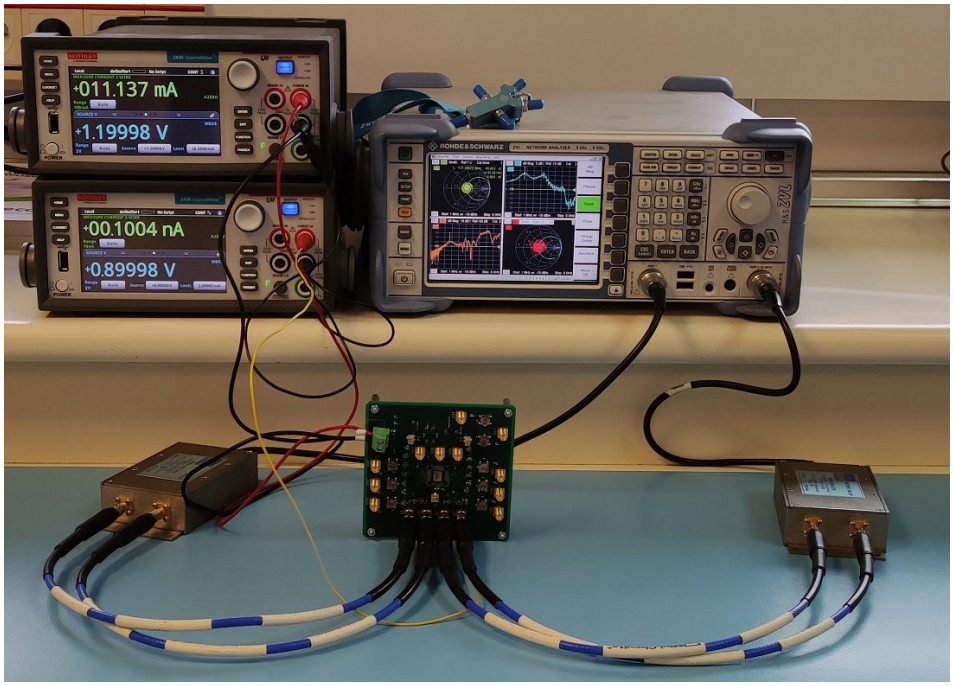

Fig. 2.49. Experimental setup to characterize the S-parameters of the output buffer.

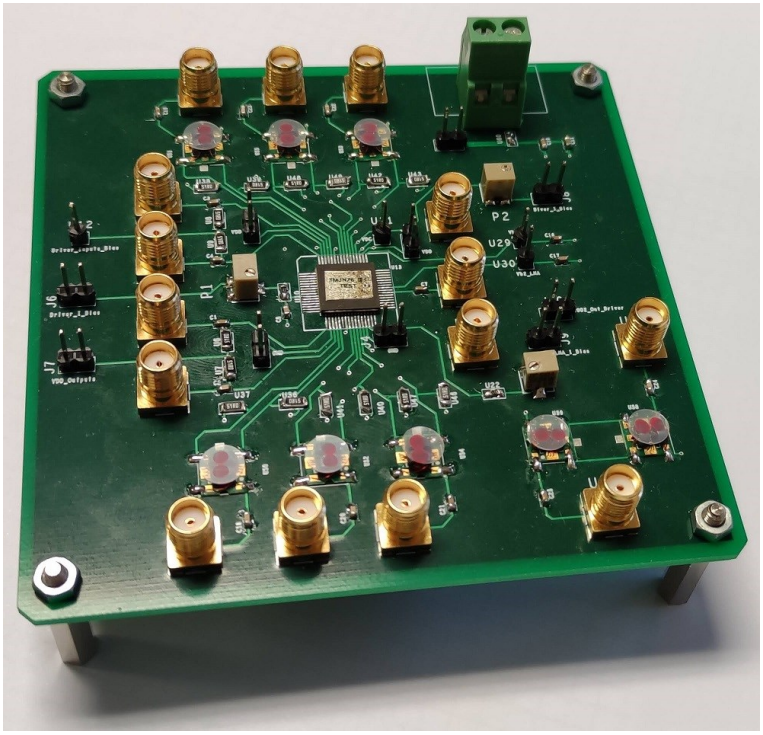

Fig. 2.50. PCB with the prototype test cells, including the output buffer.

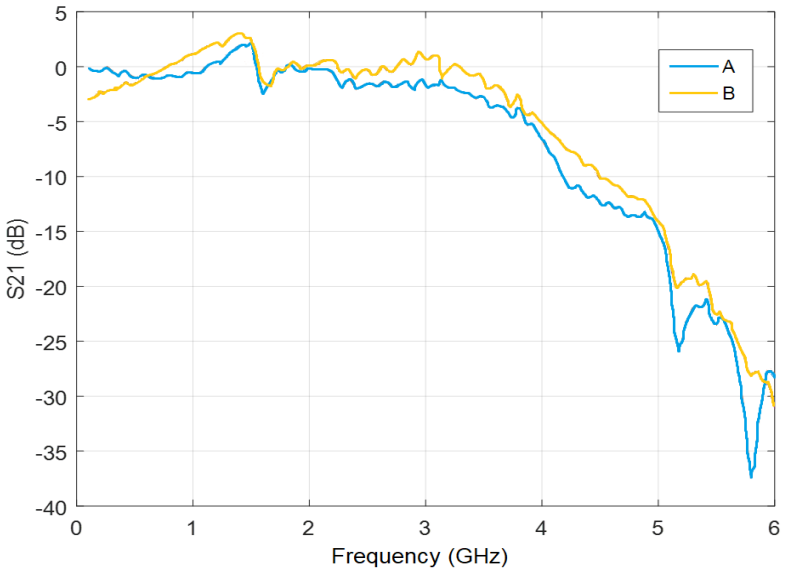

Fig. 2.51. Frequency response of the output buffer for two different samples, A (blue line) and B (orange line).Electrical Characterization

A set of measurements for the electrical characterization of the fabricated TIA has been carried out to check its correct operation before carrying out the optical measurements. The prototypes have been encapsulated in a QFN-64 package and placed on a PCB, which has been designed using the Cadence Suite software Allegro. Fig. 2.52 shows a picture of the PCB, over which the location of the main elements that are connected to the TIA has been superimposed. To obtain the frequency response, we employed a similar setup as the one shown in Fig. 2.49, measuring the S-parameter with the Rohde & Schwarz ZVL 9 kHz – 6 GHz Network Analyzer. To convert the output signal of the network analyzer to a differential signal for the TIA input, we employ a passive balun, and, at the output of the buffer, we use another passive balun to convert the differential output signal to single-ended to connect it to the network analyzer input. Both input and output nodes are AC coupled using 10-nF surface-mounted capacitors. Since the dispositive under test (DUT) contains both the TIA and the buffer, to obtain the response of the TIA alone, we have de-embedded the response of the buffer. The obtained results for the frequency response are shown in Fig. 2.53. The gain programmability of the TIA works correctly, exhibiting a linear-in-dB control from 60 to 76 dBΩ with 5 possible transimpedance levels by using the 4-bit thermometer coded control. Moreover, the 3-dB bandwidth is maintained almost constant independently of the transimpedance configuration, showing a maximum value of 600 MHz at 76 dBΩ and a minimum of 500 MHz at 60 dBΩ.The measured power consumption of the TIA alone is 6 mW, independently of the gain configuration. The input-referred noise of the TIA has been simulated to consider only the circuit noise. At 100 MHz, the TIA exhibits an input-referred noise current of 2 pA/$\sqrt{\text{Hz}}$.

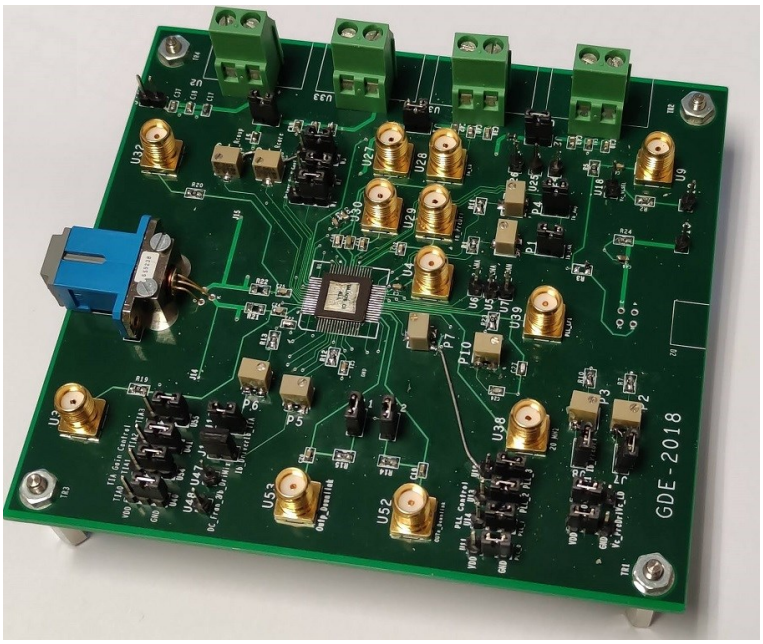

Fig. 2.52. PCB with the prototypes of the RAU, including the TIA with the output buffer.

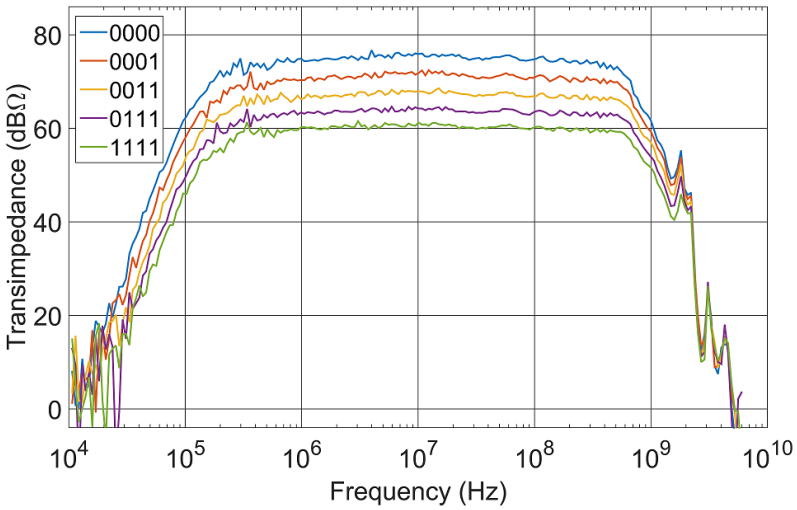

Fig. 2.53. Frequency response of the TIA for each transimpedance configuration.

To carry out linearity measurements, we use the demodulation of a 54 Mb/s 802.11a 64-QAM data transmission with an IF carrier frequency of 100 MHz. To generate and measure the signal we employ the Keysight M9381A vector signal generator (VSG) and the Keysight M9391A vector signal analyzer (VSA) [M9381, M9391]. Using software "N7617B Signal Studio Software for WLAN 802.11", we have generated the waveforms of the IEEE 802.11a standard and, to analyze the measured data, we employ the software "89600 VSA", both from Keysight. The complete evaluation setup configuration is shown in Fig. 2.54.

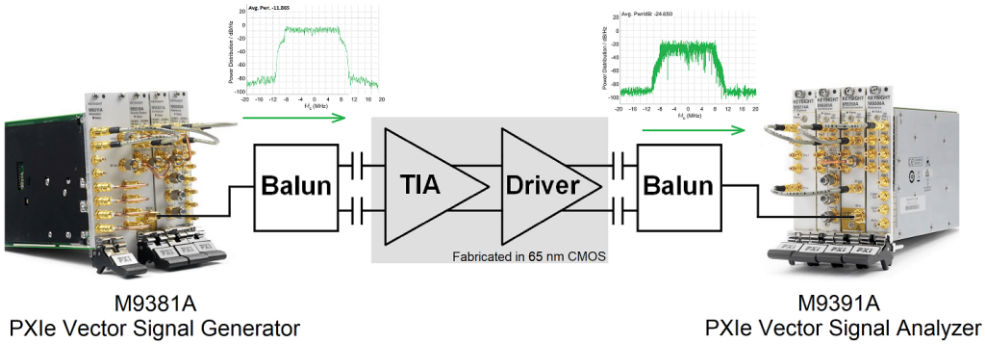

Fig. 2.54. Experimental setup diagram to perform linearity measurements.

Fig. 2.55 shows the measured EVM of the demodulated signal as a function of the input RF power level for the different transimpedance configurations. The TIA exhibits an EVM of less than 2% for a wide input range from -60 dBm to -20 dBm RF power, which corresponds to an optical input dynamic range of -16 dBm to +4 dBm. This is the lowest EVM compared to the values reported in [YOO09, KO13, DES15], and it is achieved for a wide input dynamic range of 20 dBm optical power, compared to the 3 dBm and 5 dBm ranges reported in [YOO09] and [KO13], respectively.

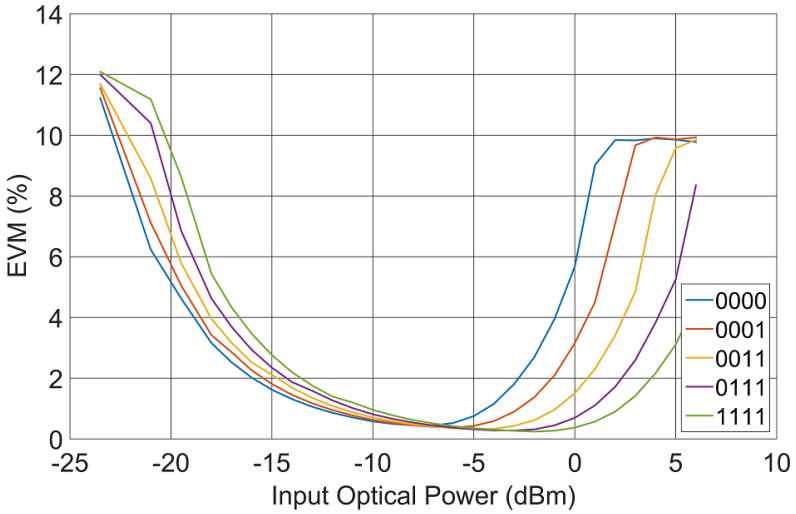

Fig. 2.55. Measured EVM as a function of the equivalent input optical power at different transimpedance configurations.

2.4.3 Optical Characterization

To carry out the optical characterization of the transimpedance amplifier, a commercially available photodiode has been employed. As stated above, the TIA performance is bound to the electrical behavior of the PD and its parasitic components, therefore these must be considered prior to the design of the TIA in the simulation environment. The TIA has been optimized for the PDINCF0705FAA-0-0 SC from PD-LD Inc., which is an external high-bandwidth InGaAs PIN photodiode with a responsivity of 0.85 A/W at 1550 nm and a bandwidth of 3 GHz under 50-Ω load when applying a reverse bias voltage of 5 V [PIN70]. Therefore, during the simulation process, its junction capacitance is modeled by a 0.45-pF capacitor.

To generate the optical signal, a modulated light source is mandatory. In our experimental setup, we employ the Keysight M9403B electro-optical converter. This device is an RF to optical converter, which consists of a constant-power laser with an external modulator as shown in Fig. 2.56. It modulates the RF signal onto a 1550-nm single mode optical signal and it operates over a frequency range of 10 MHz to 50 GHz. Since the lasers' output power is constant at around 15 mW, the optical signal amplitude must be changed by controlling the optical modulation index (OMI), which depends on the RF signal that modulates the laser, or by means of an optical attenuator.

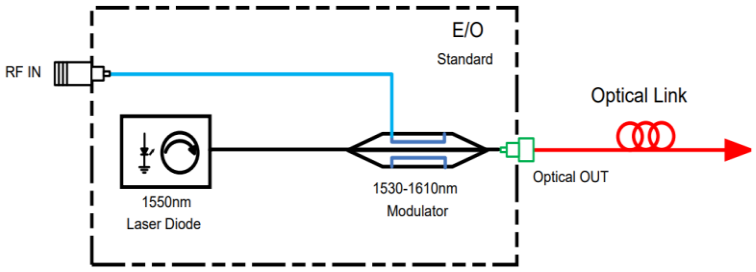

Fig. 2.56. Conceptual scheme of the M9403B electro-optical converter.

The laser output is coupled to a 2-m long MMF, which is also coupled to the PD. Previously, a 10-dB optical attenuator is added to reduce the optical power of the M9403B down to 1.5 mW to avoid damaging the PD due to an excessive optical power. To isolate the DC voltage of the PD biasing circuit, 10-nF coupling capacitors are employed. The TIA output is connected to the measurement devices using a passive balun as in the previous section. A picture of the experimental optical setup is shown in Fig. 2.57.

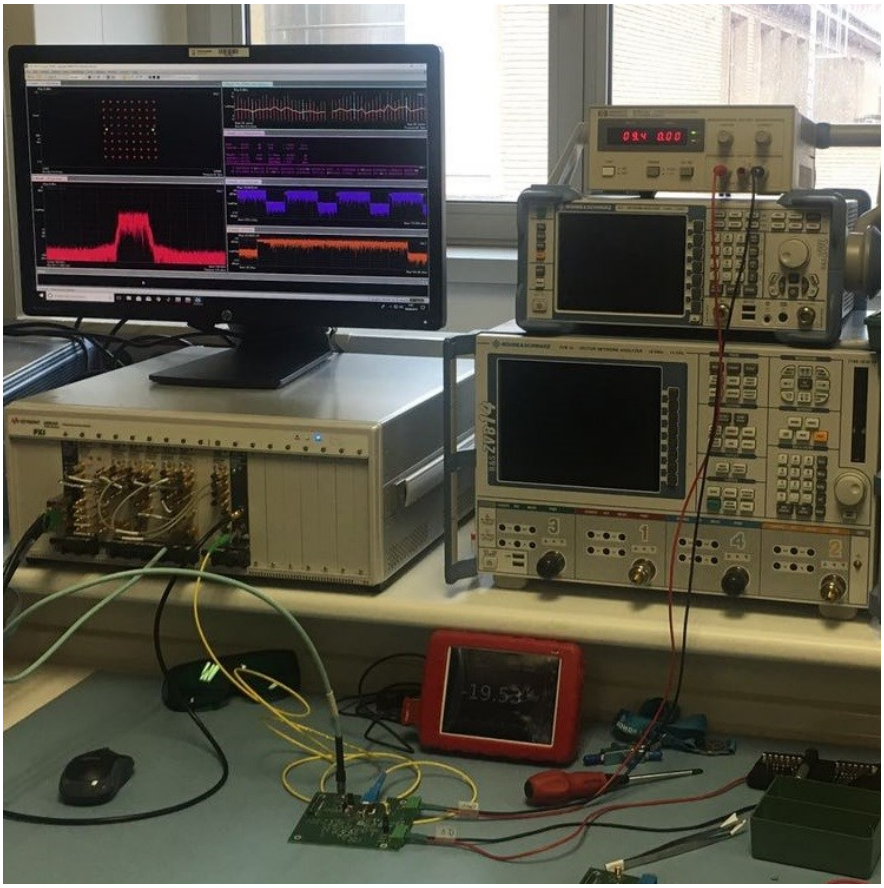

Fig. 2.57. Picture of the experimental setup for optical characterization.

To check the optical characterization and compare the front-end behavior with the electrical measurements, we have set the same verification tests as in the section above. Fig. 2.58 presents the measured frequency response at different transimpedance configurations and Fig. 2.59 shows the measured EVM versus the input signal power at each transimpedance state using the IEEE 802.11a Wi-Fi communication standard at its maximum throughput of 54 Mb/s, using an intermediate frequency of 100 MHz.

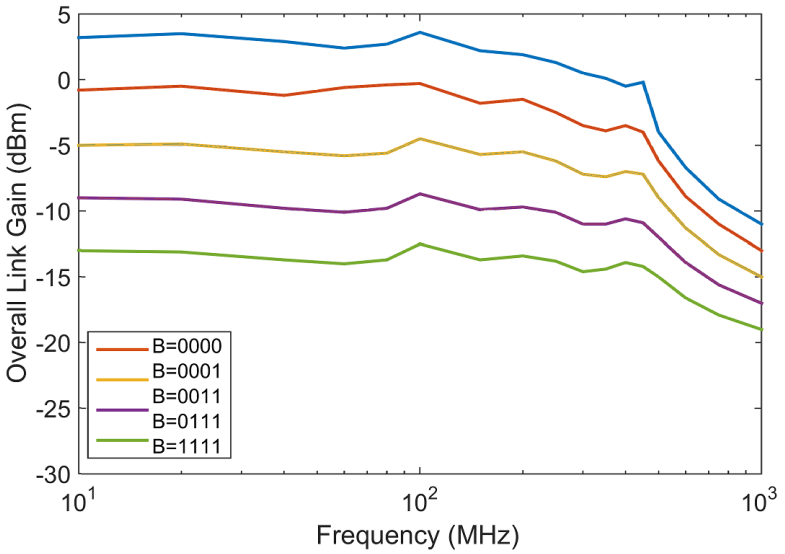

Fig. 2.58. Frequency response of the electro-optical front-end.

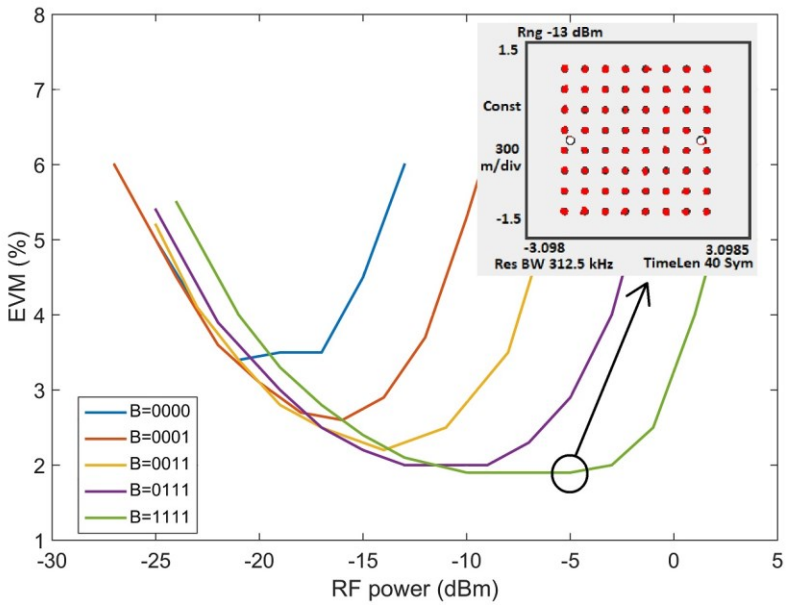

Fig. 2.59. Output signal error vector magnitude using the demodulation of a 54 Mb/s 802.11a WLAN signal.

With respect to the electrical results, the input dynamic range of the optical setup is clearly degraded. As it was expected, the higher difficulty and complexity of the optical setup require additional elements which present non-ideal parasitic effects. Moreover, the electro-optical and optical-electrical conversions, as well as the losses and nonlinearities introduced by the photonic devices and their coupling, can strongly degrade the signal properties. The bandwidth is also substantially reduced with respect to the electrical characterization, mainly due to the high parasitic capacitance of the PD. Nevertheless, the 3-dB bandwidth is maintained almost constant around 300 MHz with a 1-dB attenuation at 100 MHz. Moreover, the 16-dB linear-in-dB transimpedance control is achieved with no frequency peaking present, thanks to the simultaneous control of the feedback resistor and the open-loop gain. The measured EVM results show an EVM lower than 2% for a 10-dB optical power range and lower than 3% for a 20-dB optical power range.

Parameter	**[YOO09]**	**[KO13]**	**[DES15]**	**[AHM15]****	**This work**
RAU architecture	RFoF	RFoF	RFoF	IFoF	IFoF
Technology	130 nm CMOS	180 nm CMOS	150 nm PHEMT	65 nm RF CMOS	65 nm RF CMOS
Photodiode technology	Integrated APD	Integrated APD	External PIN	Integrated PD	External PIN
Supply Voltage	1.2 V	1.8 V	5 V	1.2 V	1.2 V
Transimpedance	54 dBΩ	62 dBΩ	46 dBΩ	51-73 dBΩ	60-76 dBΩ
Frequency of operation	2.5 GHz	5.2-5.8 GHz	12 GHz	550 MHz	300 MHz
Input noise current density	N/A	7.3 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$	26 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$	3.4 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$	2 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$**
EVM	3.89 %	2.5 %	3 %	N/A	2 %
Total power consumption	18 mW	156 mW*	100 mW	4.8 mW	6 mW
FoM (Ω·GHz/mW)	70	47*	24	511	315

* Including output buffer; ** Simulation results

Table 2-11. Summary of experimental measurement results and comparison with other RFoF and IFoF transimpedance amplifiers.

The main measurement results of the optical characterization of the IF-TIA are summarized in Table 2-11, as well as a comparison to recently published TIAs for RFoF and IFoF applications. Despite the differences on the frequency of operation of these applications, to make a fair comparison of the performance, we use the following figure of merit (FoM)

$$FoM = \frac{Transimpedance\ (\Omega) \cdot BW\ (GHz)}{Power\ Consumption\ (mW)} \qquad (2.47)$$

As shown in Table 2-11, the TIAs aimed for IFoF achieve much better FoM than those designed for RFoF applications, mainly due to the higher transimpedance and the lower power consumption. The FoM of the other TIA for IFoF, [AHM15], is slightly higher than the one achieved in this work. However, it shows simulation results and for linearity measurements it only reports the OIP3 at the maximum transimpedance, with no information about the EVM. Moreover, in [AHM15] only the linearity results at the highest transimpedance are reported, thus it does not guarantee good linearity at lower gain configurations.

The proposed IFoF TIA, with a linear-in-dB gain control, is capable to extend the input dynamic range for which high linearity is achieved, and it shows a better linear performance than RFoF receivers. For an 802.11a transmission at 54 Mb/s, our proposal achieves an EVM lower than 2 % through a wider input dynamic range of 10 dB optical power, compared to the 3-dB and 5-dB ranges reported in [YOO09] and [KO13], respectively. Another advantage of this design is the adaptability of its response to higher input capacitances by adjusting the transimpedance and open-loop gain. This design is compatible with commercially available external PIN photodiodes, which can present a much higher junction capacitance, of the order of pF, compared to the greatly low 35-fF and 140-fF capacitances of the integrated PD presented in [KO13] and [DES15], respectively.

The IFoF scheme presents a high potential and several advantages over RFoF, being a good alternative to lower the costs and improve the performance of cost-effective fiber-wireless distributed antenna systems.

2.5 Other TIA Applications

The fully differential shunt-feedback TIA with programmable gain can be implemented in several systems where a high-speed, low-noise, highly-linear and robust current-to-voltage converter is required. Therefore, the versatility of the proposed TIA topology allows its use in a wide variety of applications, since it can be easily resized in order to fit the requirements and specifications of different analog front-ends.

In this section, a version of the TIA for a MEMS (micro electro-mechanical system) capacitive sensor interfacing is proposed. It focuses on the design of a capacitance to voltage converter based on a TIA with programmable gain and bandwidth to improve noise performance and to provide adaptability to different MEMS capacitive sensors [ROY17a].

2.5.1 High-Gain TIA for Capacitive MEMS Sensors

MEMS capacitive sensors are one of the most used accelerometers, since they offer high sensitivity, low power consumption and an excellent noise performance. They are also inexpensive and can be used in a wide range of applications, from the automotive industry, e.g., on assisted stabilization systems, or in videogames and consumer electronics, such as smartphones or tablets, or even to generate seeds for secure cryptosystems [BEL02, EDD98, KAA09, GAR16, GAR17].

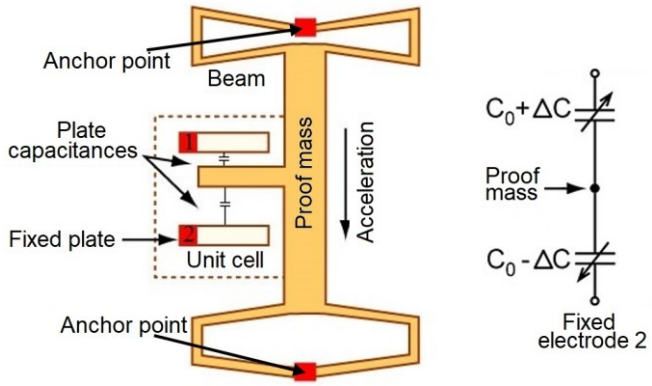

Fig. 2.60. Simplified diagram and schematics of a MEMS capacitive accelerometer.

As Fig. 2.60 shows, the basic operation principle of capacitive accelerometers consists of the combination of a proof mass and fixed electrodes with a small gap between them, effectively creating a capacitor with a capacitance, C_0, ranging from tens to hundreds of femtofarads. The acceleration causes the displacement of the proof mass, changing the gap distance. Therefore, a variation on the capacitance

between the proof mass and the fixed electrodes is generated, and the acceleration is then measured from the capacitance variations. MEMS accelerometers feature very low noise, with values at about 20 μg/$\sqrt{\text{Hz}}$ for bulk micromachined accelerometers and about 300 μg/$\sqrt{\text{Hz}}$ for surface micromachined capacitive structures, which can be fabricated at a significantly lower cost [TEZ15, AYD13, GON11]. Nevertheless, in either case, to take advantage of the extremely low thermal noise of the MEMS accelerometers, an ultra-low noise sensor interface is needed [ROY17b].

However, measuring these capacitances requires a high-sensitivity highly-linear sensor interface, as their variations, ΔC, tend to be extremely small, usually in the femtofarad range. Moreover, the parasitic effects are of great importance, since they can be as large as the sensor capacitance, which greatly affects the sensitivity of the measurement.

Several techniques can help reduce this impact by trying to eliminate the current flow through the parasitic capacitors. One example is the bootstrapping technique, which consists of measuring the voltage at the sense electrode and applying it to a guard electrode to ensure that there is no voltage difference over them [KAA09]. Therefore, this technique virtually eliminates the undesired current flow, and the effect of parasitic capacitances is cancelled. However, a highly accurate unity gain amplifier and a guard electrode surrounding the measurement electrode are needed and, in many cases, manufacturing such guard electrodes is very difficult or even impossible.

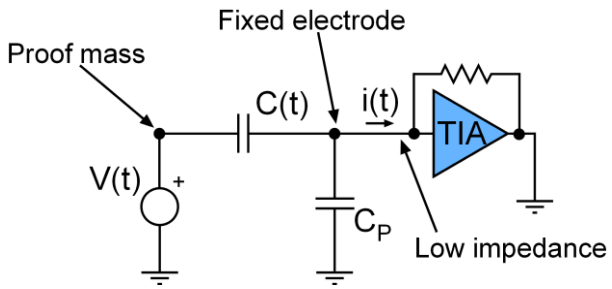

Fig. 2.61. Electrical model of a capacitive MEMS accelerometer using the current measurement technique.

A good alternative to bootstrapping is the current measurement technique, which virtually grounds both sides of the parasitic capacitances with the use of a transimpedance amplifier with very low input impedance. As shown in Fig. 2.61, the TIA measures the current through the capacitor and practically eliminates the voltage variations at the input node, thus minimizing the effect of the parasitic capacitances without needing any guard electrode. The capacitance between the proof mass and the fixed electrodes can be obtained from the expression of the current flow through a capacitor, i, which is given by

$$i = C\frac{\partial V}{\partial t} + V\frac{\partial C}{\partial t} \tag{2.48}$$

where C is the capacitance and V the voltage over the capacitor. The first term is the displacement measurement and the second one is known as the rate-of-change measurement.

Typically, only one of these terms is measured, as it is usually much larger than the other one. The rate-of-change measurement is rarely used for measuring acceleration, as it is only measurable at higher frequencies. The use of the rate-of-change term is common on other applications where this term achieves measurable values, such as in resonators or oscillators that operate at much higher frequencies [SUT15, COL10].

Typically, the displacement measurement is employed for acceleration measurement applications, as the frequency range of the acceleration usually covers the range from 0 to a few hundreds of Hz. This range coincides with the typical linear range of the mechanical response of available MEMS, which must be much lower than the natural mechanical resonance frequency, usually in the range of a few kHz as shown in Fig. 2.62.

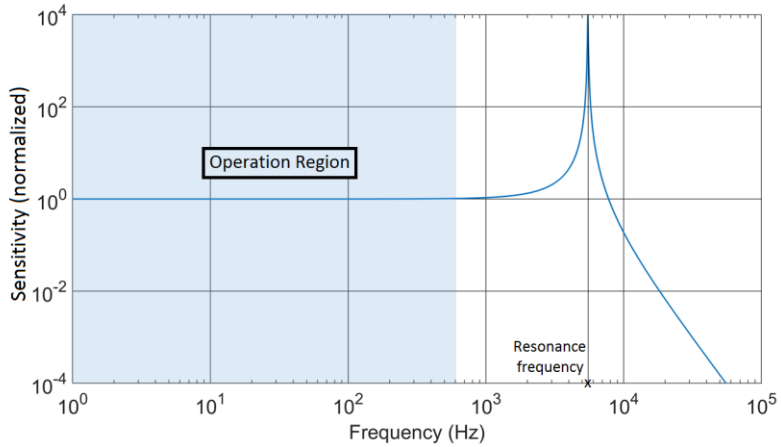

Fig. 2.62. Mechanical frequency response of a MEMS capacitive accelerometer.

Nevertheless, the mechanical response depends on the physical parameters of the MEMS: proof mass, spring constant, damping factor, size, etc. [AYD13, AYD15, MOM16, TAN11]. MEMS have a completely different mechanical response in terms of sensitivity, linear region or resonant frequency depending on their design parameters. Therefore, a sensor interface with a programmable response, adaptive to the mechanical MEMS response can strongly reduce the design costs while it improves the robustness of the MEMS interfacing system to enhance the quality of the measurement, optimizing noise performance and sensitivity [ROY17c].

To adapt the sensor interface, the following considerations must be taken into account. First, this technique consists of applying a high-frequency signal, $v_c(t)$, to the proof mass to make the rate-of-change term negligible. This way, (2.48) can be approximated as

$$i(t) \simeq C(t)\frac{\partial V}{\partial t} \qquad (2.49)$$

That is, the displacement term, which shows a linear dependence with the capacitance. Secondly, the natural oscillation frequency of the MEMS device is of great importance for choosing the signal that must be applied to the proof mass. As explained above, a high-frequency signal is needed. To consider the frequency high enough, we must ensure that it is much higher than the natural resonance frequency of the MEMS, since exciting this frequency would force oscillations and no measurement would be possible. Therefore, choosing an input signal with a frequency at least ten times higher than the MEMS mechanical resonance frequency is desired. Lastly, to recover the original capacitance variations, $C(t)$, the output signal must be demodulated with a frequency downconversion.

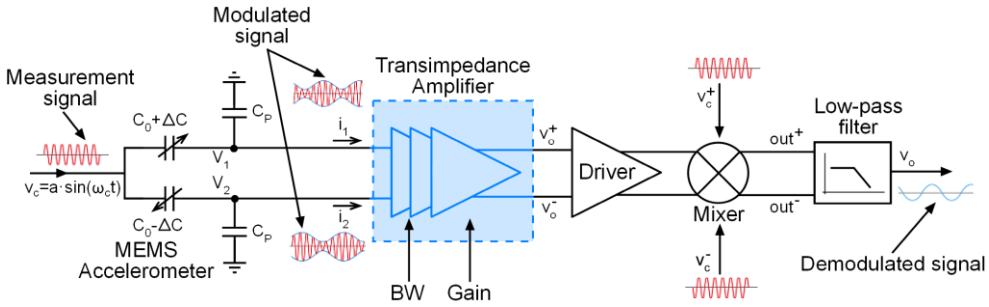

Fig. 2.63. Conceptual scheme of the differential open-loop MEMS capacitive sensor interface using current measurement technique.

The overall scheme of the differential open loop synchronous demodulator is shown in Fig. 2.63. The measurement signal, $v_c(t)$, acts as a carrier signal, while the capacitance of the sensor modulates the amplitude of the current flowing through the capacitor. However, as the capacitance variations tend to be extremely small, of the order of fF, the current flowing through the sensor is as well very small, of the order of few pA. Therefore, to obtain a measurable signal, a high-gain low-noise transimpedance amplifier is required. The TIA must feature low noise and very low input impedance. With a low input impedance and a bandwidth higher than the frequency of v_c, the TIA keeps the input nodes V_1 and V_2 at the ground potential and all the current flows through the TIA, overcoming the bootstrapping technique, as this technique practically eliminates the effect of the parasitic capacitances by suppressing the voltage variations at input nodes without the need of guard electrodes.

To optimize sensitivity, a differential shunt-shunt feedback topology has been chosen to implement the TIA. It is based on the topology employed for communications, but with a completely different sizing to achieve a very high transimpedance and an extremely low power consumption. Using (2.49) we obtain a linear relationship between the TIA transimpedance and the capacitance variations, ΔC,

$$i_{1,2}(t) \simeq (C \pm \Delta C)\frac{\partial v_c}{\partial t} \tag{2.50}$$

$$v_o^+ - v_o^- = R_T(i_1 - i_2)$$

$$v_o^+ - v_o^- = R_T \cdot 2\Delta C \frac{\partial v_c}{\partial t} \tag{2.51}$$

To maximize the sensitivity, the TIA must show high transimpedance, but also a bandwidth wide enough to contain the carrier frequency. Nevertheless, as BW increases, more noise is integrated, hence reducing the signal-to-noise ratio (SNR). The optimum BW is conditioned by the carrier frequency, which should be of the same order. Moreover, since this frequency must be much greater than the MEMS resonance frequency, the optimum BW is a function of the mechanical MEMS response. Therefore, a TIA with programmable gain and BW to optimize sensitivity for a wide range of MEMS has been designed.

As it has been mentioned above, the parasitic capacitive effects must be compensated to maximize the sensitivity of the measurement. For this reason, a low input impedance TIA suppresses the voltage variations at input nodes, and ideally all the current flows through the TIA. Therefore, there is no current flow through the parasitic capacitors and all the current through the sensor can be measured. It is well known that closed loop TIAs show a higher linearity than open-loop approaches [CHE09, LIU12, LU12] and they can achieve a better performance in terms of input noise, being suitable for low-noise sensor applications [HU10, CHU15]. Consequently, the proposed shunt-shunt feedback TIA is based on the topology employed in the TIA for RFoF, shown in Fig. 2.25, which consists of a fully differential voltage amplifier and a negative resistive loop. To control the system stability, transimpedance and bandwidth, a double control of transimpedance and open-loop gain has been implemented [ROY16a, SAN07]. The transimpedance control has been implemented with a variable feedback resistor which consists of an array of four resistors connected in parallel (R_{F0} to R_{F3}), and programmable with a 3-bit thermometer code (b_{F0-2}). In a similar way to the transimpedance gain control, load resistors have been implemented in the first two differential pairs, using an array of three resistors in parallel ($R_{Li,1}$ to $R_{Li,3}$), programmable with a 3-bit thermometer code (b_{L0-2}), providing full programmability to the TIA. The transistors and resistors have been sized with the aim of an extremely low power consumption and a very high transimpedance. The component values and the aspect ratio of the transistors are shown in Table 2-12.

$\mathbf{M_1}\left(\frac{W}{L}\right)$	$\mathbf{M_2}\left(\frac{W}{L}\right)$	$\mathbf{M_3}\left(\frac{W}{L}\right)$	$\mathbf{M_{B1-3}}\left(\frac{W}{L}\right)$	$\mathbf{M_S}\left(\frac{W}{L}\right)$	R_{D1-3}	V_B
20 µm / 1 µm	20 µm / 0.5 µm	10 µm / 1 µm	10.5 µm / 4 µm	20 µm / 0.18 µm	180 kΩ	600 mV
R_{F0}	R_{F1}	R_{F2}	R_{F3}	$R_{Li,1}$	$R_{Li,2}$	$R_{Li,3}$
5 MΩ	1.1 MΩ	380 kΩ	100 kΩ	33 kΩ	48 kΩ	45 kΩ

Table 2-12. Component values and transistor aspect ratios for the proposed TIA.

The transimpedance amplifier has been designed in a standard 0.18-µm CMOS technology with a single 1.8-V voltage supply. For this design, a surface-micromachined comb-finger structure of 2-µm gap and resonance frequency of 5.5 kHz has been employed to model the accelerometer. It shows a nominal capacitance C_0 of 1 pF with parasitic capacitances C_P of around 2 pF. With this model of the MEMS accelerometer, the sensitivity, S_T, provided by the sensor can be obtained from the following expression

$$S_T = \frac{\Delta C}{\Delta \ddot{x}} = \frac{\Delta x}{\Delta \ddot{x}} \cdot \frac{\Delta C}{\Delta x} \tag{2.52}$$

being x the displacement of the proof mass. Considering a linear behavior, and at low frequency operation, it can be approximated by [BEN13]

$$S_T = \frac{1}{\omega_r^2} \cdot \frac{C_0}{x_0} \tag{2.53}$$

with x_0 the gap distance and ω_r the resonance frequency.

From (2.53) we obtain a sensitivity of 4.2 fF/g[4]. The measurement frequency, ω_c, is chosen to be of 50 kHz, so that it is roughly one order of magnitude greater than the resonance frequency.

As shown in Fig. 2.64, the proposed TIA performs a 34-dBΩ transimpedance control range, while maintaining an almost constant bandwidth of around 1.2 MHz. To achieve this gain range keeping a flat frequency response, a simultaneous control of the feedback and load resistors has been made. Moreover, Fig. 2.65 shows that with a single control of the open-loop gain of the voltage amplifier, the transimpedance can be fixed at its maximum value, but the bandwidth can be tuned over more than a decade, from 75 kHz to 1.2 MHz.

With a power consumption of only 54 µW, the TIA achieves a maximum sensitivity of 1 mV/fF, which corresponds to a capacitive sensitivity of 4.2 mV/g and presents a low equivalent input noise of only 42 fA/$\sqrt{\text{Hz}}$, at the maximum transimpedance

[4] The constant g stands for the acceleration of gravity (9.8 m/s^2).

configuration of 10 MΩ and 73-dB open loop gain (Fig. 2.66, $b_F = b_L = 111$), or equivalently 100 μg/$\sqrt{\text{Hz}}$ at 50 kHz. Table 2-13 summarizes the main results and compares with other published capacitance-to-voltage converters [TAN11, SAL09, SHA07, YIN11]. These CVCs are based on current measuring with a sensor interface based on a TIA, excepting [TAN11], where a folded cascode operational amplifier is used configured as voltage amplifier, along with a diode-connected subthreshold NMOS transistor to bias the input nodes. It also requires post-amplifying stages to increase sensitivity, including a variable gain amplifier to achieve a 12-dB gain control, which make of it a power-hungry circuit.

	[TAN11][1]	**[SAL09][2]**	**[SHA07][1]**	**[YIN11][2]**	**This Work[2]**
Technology	0.35 μm CMOS	0.18 μm CMOS	0.6 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Supply Voltage	3.3 V	1.8 V	3 V	5 V	1.8 V
Minimum Input Noise	54 μg/$\sqrt{\text{Hz}}$	65 fA/$\sqrt{\text{Hz}}$	88 fA/$\sqrt{\text{Hz}}$	63 fA/$\sqrt{\text{Hz}}$*	42 fA/$\sqrt{\text{Hz}}$
Capacitive Sensitivity	18 mV/fF	-	25 mV/fF*	3.3 mV/fF	1 mV/fF
Power Consumption	5.1 mW	436 μW	400 μW	-	54 μW
Type of Sensing Interface	Voltage Amplifier	Capacitive TIA	Resistive TIA	Resistive TIA	Resistive TIA
Gain	-9 - +2 dB	56 MΩ	1.6 – 25 MΩ	2 – 22 MΩ	0.15 – 10 MΩ
Bandwidth	8.6 MHz	1.8 MHz	200 kHz*	200 kHz*	75 kHz – 1.2 MHz
Application	Accelerometer	Resonator/ Oscillator	Gyroscope	Gyroscope	Accelerometer

[1]Experimental results; [2]Simulation results; *Calculated from paper

Table 2-13. Summary of the performance and comparison with other published works.

A capacitive TIA is presented in [SAL09], showing a 56-MΩ transimpedance and a 1.8-MHz bandwidth, which features no gain control and exhibits a higher noise level than that reported in this work. Structures reported in [SHA07, YIN11] are both based on resistive TIAs, providing transimpedance gains up to 25 MΩ in [SHA07] and 22 MΩ in [YIN11]. Both perform a transimpedance gain control and implement the feedback resistor using a T-network pattern, which reduces the overall size of the resistor, but can significantly increase noise. Moreover, the bandwidth in [SHA07] decreases with the transimpedance, while an orthogonal gain and bandwidth control is achieved in the TIA proposed in this work. This full programmability of gain and

bandwidth provides a much better adaptability of the frequency response to the mechanical frequency response of different MEMS. Furthermore, Monte Carlo simulations have also been carried out for process variations and mismatch. The Monte Carlo analysis shows a statistical distribution of the chip performance before fabrication, which is of great importance, since the technological parameters can experience strong variations that may considerably deteriorate the overall performance. Fig. 2.67 and Fig. 2.68 present the Monte Carlo histograms for the transimpedance and bandwidth of the TIA, both obtained for the maximum gain configuration. The results obtained confirm the robustness of the design against process variations, with standard deviations of about 5% of the nominal value.

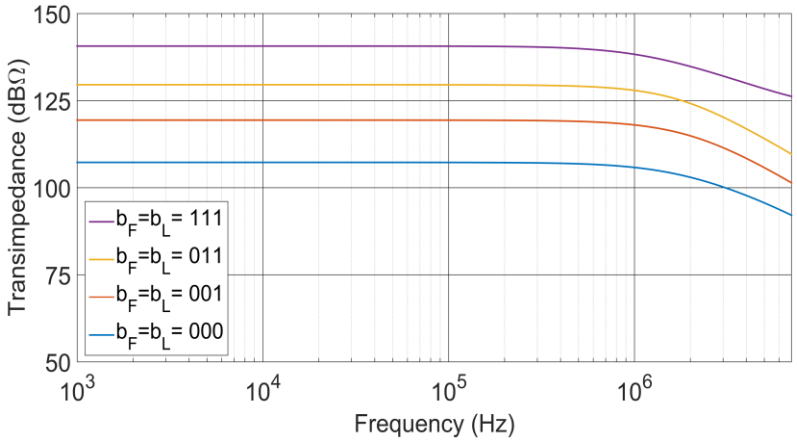

Fig. 2.64. Frequency response of the transimpedance amplifier with a double control of transimpedance (control bits $b_{F(0\text{-}3)}$) and open loop gain (control bits $b_{L(0\text{-}3)}$), showing a nearly constant bandwidth of 1.2 MHz.

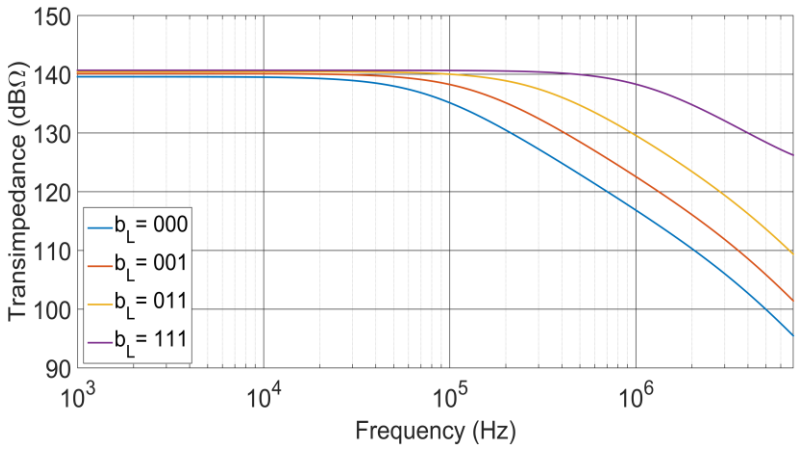

Fig. 2.65. Frequency response with a single control of the open-loop gain. The transimpedance gain is almost constant, 140 dBΩ at the maximum transimpedance configuration $b_F = 111$.

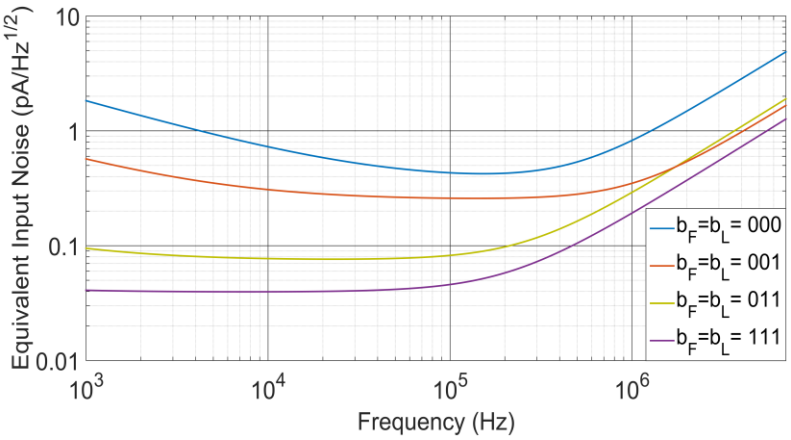

Fig. 2.66. Equivalent input noise response for the four transimpedance configurations with a 1.2 MHz bandwidth. The control bits $b_{F(0\text{-}3)}$ and $b_{L(0\text{-}3)}$ use the same word.

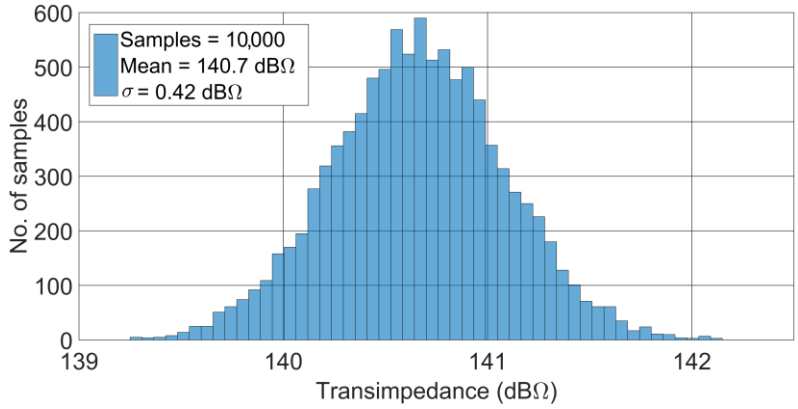

Fig. 2.67. Monte Carlo simulation results for transimpedance gain at the maximum transimpedance configuration.

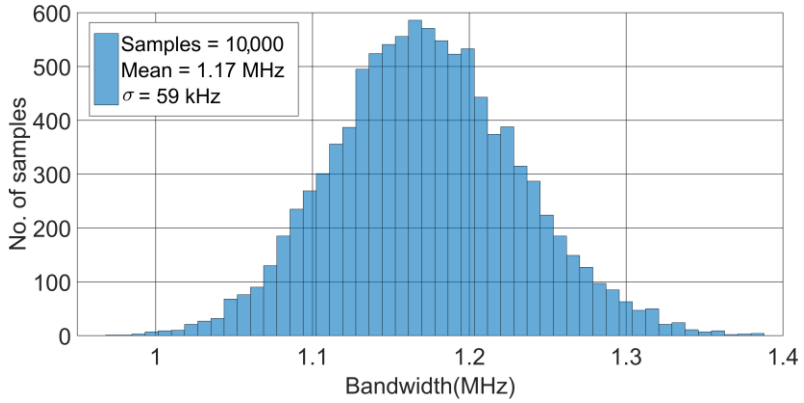

Fig. 2.68. Monte Carlo simulation results for bandwidth at the maximum transimpedance configuration.

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3 Conclusions

Global data traffic demand is growing at a dizzying pace, even faster than it was expected a few years ago. Moreover, recent events, such as the coronavirus crisis, have shown that our dependence on data exchange is extraordinary and that the currently deployed communication systems must evolve to provide even higher capacity if we want our demand to be covered.

To allow the spread of IoT, the available wireless connectivity must be considerably increased, while the costs must decrease to an affordable range. The use of DAS with a vast number of low-power access nodes has proven its effectiveness upon the problem of saturation of the radio spectrum while also being less susceptible to interferences. Mixed fiber-wireless systems are a cost-effective, flexible approach, capable of overcoming the limitations of wireless communication systems at a reasonable cost.

This thesis has been divided into three chapters. Chapter 1 has been employed to introduce the concept of distributed antenna systems to provide an extensive background for the design of remote antenna units, from the basic principles of operation of the photonic and electronic devices to the different DAS architectures. Chapter 2 presents the main body of this thesis, which consists of the design of different TIAs, optimized for different RAU configurations and for other applications. The most relevant results have been summarized in the end of each section, and this final chapter is intended to discuss the main conclusions of this work.

The main goals of this thesis, summarized at the end of Chapter 1, were set before the start of the work leading to this thesis. In the general conclusions section, a verification of the degree of agreement between the initially-set goals and the results is undertaken.

3.1 General Conclusions

Throughout this thesis, several proposals of transimpedance amplifier designs have been presented. These proposals have been mainly developed to suit each of the three main RAU configurations, and versions of these topologies have been adapted for other applications. After the description and comparison of the existing TIA topologies, we arrive at the following conclusions, which lead us to choose the shunt-feedback TIA as the most suitable architecture:

- The trade-off between bandwidth, gain, power consumption, and noise, is less stringent in closed-loop TIAs.
- There is a higher number of degrees of freedom in the design of closed-loop TIAs.
- Closed-loop TIAs exhibit a better linearity, since the negative feedback loop enhances the linear behavior.
- If the frequency response of the core amplifier is properly adjusted, the shunt-feedback TIA can achieve a stable flat frequency response.

In this thesis, a new noise-reduction strategy for optical receivers with large-area photodiodes, has been proposed. This strategy, named as the sliced-PD technique, consists of manufacturing the PD as an array of N sub-PDs occupying the same active area as the original one. The main conclusions, after making a theoretical description and performing a case study with one of the proposed TIA topologies are:

- The integrated input-referred noise is smaller for higher number of slices since the f^2-noise contribution decreases with a $1/N$ dependence.
- Replicating the core amplifier of a feedback TIA N times and using a feedback resistor N times larger than originally, the sensitivity increases with roughly $\sqrt{N}$ dependence with no effects on the system stability.
- When the PD is sliced in several pieces, the intrinsic capacitance of each one is divided by N. Therefore, since it is a much smaller value, the design of the core amplifier can be optimized, achieving a much better sensitivity with this approach than with the traditional one for the same power consumption.

After determining that the shunt-feedback topology is the most suitable one for our purpose, the design and optimization of several TIAs for the different RAU architectures has been carried out. Moreover, for the RFoF and the IFoF designs, a differential TIA topology has been chosen to achieve a better linearity, which is a key parameter of these transmission schemes. The main characteristics and the most relevant results of these two structures are summarized as follows:

- **BB-TIA**
    - The proposed 2.9-mW TIA with a 1-GHz bandwidth achieves a sensitivity of -11 dBm, which is higher than previous works with similar conditions of technology, PD capacitance and transmission rate, where a regulated cascode is employed.
    - The sliced-PD technique has been applied to this circuit, achieving an improvement of 7.9 dBm in sensitivity for an optimized design with 16 PD pieces, proving that the proposed technique works, in a transistor-level simulation.

- **RF-TIA**
    - A better figure of merit than previous works is achieved with our proposal, thanks to the combination of low power consumption and high transimpedance.
    - Moreover, while many of the previous works do not perform an integrated gain control in the TIA, in this work the transimpedance can be programmed from 45 dBΩ up to 65 dBΩ. A 5-bit thermometer-coded resistor array has been adjusted to provide a robust linear-in-dB gain control, with 4-dB steps, and a double control of the transimpedance and the open-loop gain guarantees a flat frequency response, independent of the transimpedance. This programmability provides a higher versatility and flexibility to the system.

- **CATV-TIA**
    - A version of the RF-TIA has been made to show its capabilities for the implementation if a CATV receiver with an almost linear-in-dB transimpedance control with 18-dB control range.
    - With the implementation of the gain control in the TIA, there is no need to use a variable voltage attenuator in the CATV receiver, therefore reducing the number of stages in the system.
    - Thanks to the transimpedance control, the TIA can achieve an input range similar to that of recently published works based on a much more expensive GaAs PHEMT technology.

- **IF-TIA**

    - The chip has been fabricated in a 65-nm RF CMOS technology, which operates with a nominal voltage supply of 1.2 V and a set of measurements for the electrical and optical characterization of the fabricated TIA has been carried out.
    - The gain programmability of the TIA works correctly, exhibiting a linear-in-dB control from 60 dBΩ to 76 dBΩ using a 4-bit thermometer coded control.
    - The 3-dB bandwidth is maintained almost constant independently of the transimpedance configuration, showing a maximum value of 600 MHz at 76 dBΩ and a minimum of 500 MHz at 60 dBΩ. At 100 MHz, the TIA exhibits an input-referred noise current spectral density of 2 pA/√Hz.

As a general conclusion after comparing the performance of the TIAs for the different RAU configurations, is worth mentioning that the IF-TIA achieves a figure of merit much higher than previous works using the RFoF approach. This is mainly due to the much higher transimpedance and the very low power consumption. Moreover, a better linearity is achieved, as, for an 802.11a transmission at 54 Mb/s, our proposal achieves an EVM lower than 2 % through a wide input dynamic range of 10 dB optical power, compared to the 3-dB and 5-dB ranges reported in previous works. The IFoF scheme presents a high potential and several advantages over RFoF, being a good alternative to lower the costs and improve the performance of cost-effective fiber-wireless distributed antenna systems.

Finally, it is worth mentioning that the proposed and manufactured TIA for IFoF greatly contributes to the development and validation of the complete RAU. We have demonstrated the capabilities of the proposed structures to achieve low noise, high linearity, ease of programmability of the transimpedance, and adaptability of the topology to different requirements, which are of great interest to the design of optical receivers.

A version of the TIA for a MEMS capacitive sensor interfacing has been proposed and studied. It consists of a capacitance to voltage converter based on a version of the RFoF-TIA and it aims to improve noise performance and to provide adaptability to different MEMS capacitive sensors. The most significant results and conclusions of this design are the following:

- A transimpedance control has been implemented with a variable feedback resistor, programmable with a 3-bit thermometer code. In a similar way to the transimpedance gain control, an open-loop gain control, programmable with a 3-bit thermometer code, independent to the transimpedance control code.

- The TIA performs a 34-dBΩ transimpedance control range with constant bandwidth of around 1.2 MHz, and a bandwidth control from 75 kHz to 1.2 MHz when the transimpedance is fixed at its maximum value.
- With a power consumption of only 54 μW, the TIA achieves a maximum sensitivity of 1 mV/fF, which corresponds to a capacitive sensitivity of 4.2 mV/g and presents a low equivalent input noise of only 100 μg/$\sqrt{\text{Hz}}$ at 50 kHz for the maximum transimpedance configuration of 10 MΩ.

As a main conclusion, it should be noted that the most relevant contribution of the proposed MEMS acceleration sensor interface is the system flexibility and versatility. The proposed capacitance-to-voltage converter based on a transimpedance amplifier can be easily reprogrammed to match many commercially available MEMS acceleration sensors. While the programmable bandwidth can be used to match sensors with different resonance frequency, the programmable transimpedance can be used to adjust the interface sensitivity to provide the TIA a full adaptability.

3.2 Future Research Lines

The convergence of wireless communications and fiber optic systems has emerged as a promising solution to enable the deployment of new technologies such as 5G and IoT. This approach can be a good candidate to support the rate of growth of data traffic demand for wireless applications, either for indoor or outdoor applications, combining the best of these technologies: the mobility of wireless technologies and the low attenuation and high capacity of optical fibers. The development of ICs capable of transmitting such amount of data is mandatory to achieve the desired high-speed environment in the near future.

In this work, a versatile TIA topology has been proposed, providing several solutions to different data transport configurations in fiber-fed DAS. One of the objectives and motivation of the design of the proposed TIAs was to contribute to the development and validation of a complete RAU for IFoF communications with the design of several subcircuits and the design of a PCB to perform the experimental characterization of the RAU after its fabrication and mounting. The development of such RAU is still ongoing, and the TIA structure might be modified to suit different needs of the RAU, such as its programmability or input dynamic range to provide an even higher flexibility to the overall system.

APPENDIX A
Copy of the Papers Presented in the Thesis

sensors

MDPI

Letter

High-Sensitivity Large-Area Photodiode Read-Out Using a Divide-and-Conquer Technique

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Received: 6 October 2020; Accepted: 3 November 2020; Published: 5 November 2020

Abstract: In this letter, we present a novel technique to increase the sensitivity of optical read-out with large integrated photodiodes (PD). It consists of manufacturing the PD in several pieces, instead of a single device, and connecting a dedicated transimpedance amplifier (TIA) to each of these pieces. The output signals of the TIAs are combined, achieving a higher signal-to-noise ratio than with the traditional approach. This work shows a remarkable improvement in the sensitivity and transimpedance without the need for additional modifications or compensation techniques. As a result, an increase in sensitivity of 7.9 dBm and transimpedance of 8.7 dBΩ for the same bandwidth is achieved when dividing the photodiode read-out into 16 parallel paths. The proposed divide-and-conquer technique can be applied to any TIA design, and it is also independent of the core amplifier structure and fabrication process, which means it is compatible with every technology allowing the integration of PDs.

Keywords: integrated photodiode; low-noise amplifier; noise reduction techniques; photodiode read-out; transimpedance amplifier

1. Introduction

Large area photodiodes (1-mm diameter or more) are used in many instrumentation and communication applications. For example, plastic optical fiber (POF) sensors are a new class of fiber sensors used in oil, gas, biotechnology, and energy fields. Thanks to the POF's large diameter and the inexpensive peripheral components and low installation costs, many electronic pieces of instrumentation are built based on POF and photodiodes with a large active area, such as a sensor for oil trucker valve monitoring, a monitoring system for high voltage substation switch, an oil leaking sensor for offshore platforms, and a solar tracker for illumination [1]

On the other hand, transmitting data at a high transmission rate is crucial in today's world. We are constantly connected and demanding more and more information. The demand is continuously growing, and communication networks must be prepared for this evolving scenario. This need has driven the use and development of optical communication systems over the last years due to their capability to transmit information at very high data rates. However, because of the high cost of installation and maintenance of glass optical fiber (GOF) systems, the vast majority of the currently deployed short-range networks are still based on copper, which cannot transmit information as fast as optical fibers.

In this context, a promising solution to overcome the short-range bottleneck is plastic optical fibers (POF), which can provide a higher data rate and are more robust than copper cables, with the additional advantage of their immunity to electromagnetic interferences. They have been recently used in the automotive industry since they are lighter and more flexible than copper cables and also show a

few advantages over GOF, such as higher stability against vibrations thanks to their much larger core diameter [2]. They are also easier to install and manipulate, thus reducing the costs of installation and maintenance, making POF cost-competitive and an excellent candidate for short-distance applications, such as home networks.

On the contrary, POF suffers from high attenuation (0.2 dB/m at 650 nm), and coupling with both the transmitter and the receiver generates even higher losses. Over the last few years, great efforts have been made to increase the range and throughput of these systems by improving the performance of the photonic devices and the electronic sensor interfaces [2–5]. In addition, since the core of a step index POF (SI-POF) has a 1-mm diameter, large-area optical sensors are required to achieve high-efficiency light coupling [6]. It is well known that large area photodiodes (PD) have an important parasitic capacitance of the order of several picofarads (pF) [7]. Therefore, to interface these photonic devices and overcome the high attenuation of POF, a low-noise transimpedance amplifier (TIA) with low input impedance must be designed.

To increase the transmission length, highly sensitive optical receivers with large area photodiodes with a diameter of the order of 1-mm must be used. Several TIAs have already been proposed for POF applications, the shunt-feedback topology, shown in Figure 1, being the most commonly employed due to its more linear performance and ease of design. Moreover, there are several noise reduction techniques described in the literature to increase receiver sensitivity [8,9]. However, it is still very challenging to fulfill the requirements of sensitivity and bandwidth (BW) needed for the low-cost applications mentioned above simultaneously due to the high capacitance of the photodiodes and their small responsivity. Improving these characteristics is critical to allow the possibility of reaching longer distances and achieving higher data transmission rates.

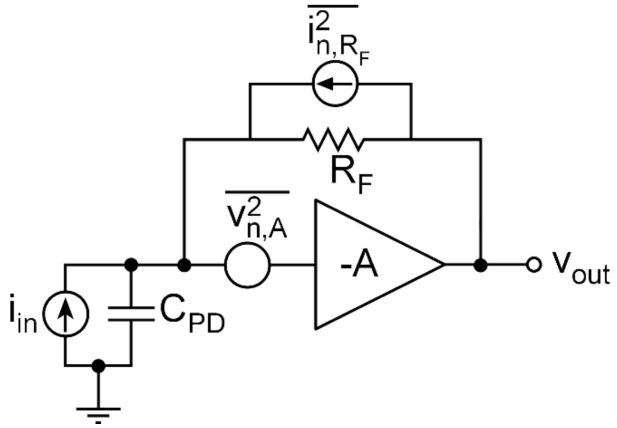

Figure 1. Schematic diagram of a shunt-feedback transimpedance amplifier (TIA), including noise sources.

In this letter, we present a novel technique to increase the sensitivity of optical read-outs based on a feedback TIA with a large integrated photodiode since this topology is the most commonly employed in photodiode read-out designs [10]. Nevertheless, the proposed technique can be applied independently of the TIA core amplifier topology, and, thus, it can be used in any silicon photonics technology. In Section 1, a background is given to introduce the context and provide motivation for this work. Section 2 describes the proposed noise reduction technique with a theoretical analysis, and in Section 3, the technique is applied to a transistor-level simulation of a shunt-feedback TIA to show post-layout results of this study. Finally, Section 4 summarizes the conclusions of this work.

2. Technique Description

One of the main challenges of the TIA design is to overcome the large parasitic capacitance of the PD to achieve wide bandwidth and low noise. In the technique described in this letter, we propose slicing the photodiode and manufacturing it in N individual pieces, connecting a TIA to each one of them, as shown in Figure 2, with the aim of reducing the equivalent input-referred noise. Slicing the PD helps reduce the difficulty of designing the TIA since the parasitic capacitance of each PD piece is smaller, and, thus, the TIA design constraints are relaxed.

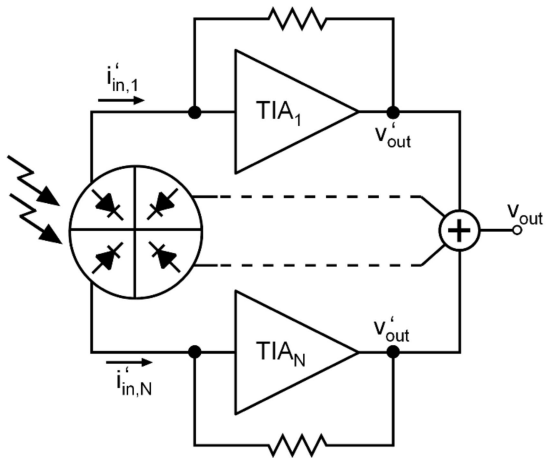

Figure 2. Conceptual scheme of a photodiode read-out using the sliced- photodiode (PD) technique with N TIAs.

To understand the operating principle of this technique, we must first recall the approximate modulus of the complex transimpedance, Z_T, and the input-referred noise, $\overline{i^2_{n,IN}}$, of a shunt-feedback TIA as a function of the angular frequency, ω:

$$|Z_T| = \left| \frac{R_F}{1 + j\frac{R_F C_{in}}{A}\omega} \right| \tag{1}$$

$$\overline{i^2_{n,\,IN}} \approx \frac{K^2}{\omega R_F^2} + \frac{4K_B T}{R_F} + \frac{\overline{v^2_{n,A}}}{R_F^2} + \overline{v^2_{n,A}}\omega^2 C_{in}^2 \tag{2}$$

where K is a constant relative to the $1/f$-dependent Flicker noise contribution, K_B, is the Boltzmann's constant, T the absolute temperature, R_F the feedback resistor, A and $\overline{v^2_{n,A}}$ the open-loop gain and input voltage noise of the core amplifier, respectively, and C_{in} the equivalent input capacitance, which includes the PD capacitance, C_{PD} and the input capacitance of the core amplifier.

It is well known that the tradeoff between bandwidth, transimpedance, input capacitance, and the technological transition frequency limitation, f_T, leads to the transimpedance limit described in [11]:

$$R_T \leq \frac{A_0 \omega_A}{C_{in} BW^2} \tag{3}$$

where R_T is the transimpedance at zero frequency and $A_0\omega_A$ is the gain-bandwidth product of the voltage amplifier, roughly proportional to the technology parameter f_T. Therefore, from (3), it is clear that, for a target BW, the maximum achievable transimpedance is bound to the capacitance at the input node. Despite the intrinsic capacitance of the PD being lower when biased at high reverse voltage, this parameter should be treated as constant. Thus, to reduce C_{in}. The only possible way is to

make a greater effort in the TIA design to minimize its input capacitance. Moreover, according to (2), the input-referred noise is strongly dependent on the input-node capacitance, since the third term, the f^2-noise is proportional to C_{in}^2. Therefore, if a lower value of the input capacitance is achieved, not only a greater transimpedance can be reached, but also lower noise and, thus, better sensitivity. In the proposed technique, we explore the possibility of dividing the PD into N pieces to obtain a $1/N$ parasitic capacitance for each one. To do that, the PD should be manufactured in N slices, and each of them should be connected to an individual TIA, as shown in Figure 2. PDs in silicon photonics are implemented as an array of multiple fingers, which facilitates their division [12,13].

The first and immediate advantage of this technique is a much easier design of the TIA since the parasitic capacitance of the PD that it is attached to is now N times smaller so that achieving wide BW should be much simpler.

Moreover, according to (2), since the input capacitance is approximately divided by N, the f^2-noise contribution decreases by a factor of N^2. Since the signal power received by each PD piece is reduced linearly with the number of slices, the equivalent input-referred noise should decrease. Let us explore this hypothesis and compare it with the traditional approach: After slicing the PD into N pieces, each piece now receives an optical power of $1/N$ times the total optical signal power, and, therefore, it generates a current $i'_{in} = i_{in}/N$. The capacitance of each input node is now $C'_{in} \simeq C_{in}/N$, since the area of each PD piece is N times smaller than the total PD area and C_{PD} is the major contribution to C_{in}. This technique works as long as $C_{PD} \simeq C_{in}$, that is, it can be applied to TIA designs using large integrated PDs with high intrinsic capacitance, such as the ones employed in [14] and [15], where large PD capacitances of 14 pF and 64 pF are reported, respectively.

Regarding the topology, design parameters and transistor sizing of the core amplifier, we can use the same values to compare both approaches. However, to keep a constant BW and quality factor, each TIA must keep a constant $R_F C_{in}$ product, thus a feedback resistor $R'_F = N{\cdot}R_F$ will be used on the sliced-PD with multiple-TIA design [16]. Therefore, after slicing the PD into N equal pieces, each TIA achieves the same bandwidth as before and generates the same output voltage:

$$v'_{out} = i'_{in} R'_F = \frac{i_{in}}{N}{\cdot}NR_F = i_{in}R_F \tag{4}$$

and the input-referred noise of each TIA, $\overline{i^2_{n,IN}}'$ will be:

$$\overline{i^2_{n,\,IN}}' \approx \frac{K^2}{\omega N^2 R_F^2} + \frac{4K_BT}{NR_F} + \frac{\overline{v^2_{n,A}}}{N^2R_F^2} + \frac{\overline{v^2_{n,A}}\omega^2 C_{in}^2}{N^2} \tag{5}$$

which shows a reduction in the input noise by a factor close to $1/N$.

Since all the N signals are synchronized, we can combine the outputs to obtain a higher transimpedance, R_T, than with a single-piece PD configuration, so that:

$$R_T = \frac{v_{out}}{i_{in}} = \sum_1^N i_{in}R_F = NR_F \tag{6}$$

Moreover, since each path from each PD slice is independent of each other, the electrical noise of each TIA is uncorrelated. Therefore, we can calculate the total input noise with a quadratic sum of the N noise contributions as:

$$\begin{aligned} \overline{i^2_{n,IN}} &= \sum_1^N \frac{K^2}{\omega N^2 R_F^2} + \frac{4K_BT}{NR_F} + \frac{\overline{v^2_{n,A}}}{N^2R_F^2} + \frac{\overline{v^2_{n,A}}\omega^2 C_{in}^2}{N^2} \\ &= \frac{K^2}{\omega N R_F^2} + \frac{4K_BT}{R_F} + \frac{\overline{v^2_{n,A}}}{NR_F^2} + \frac{\overline{v^2_{n,A}}\omega^2 C_{in}^2}{N} \end{aligned} \tag{7}$$

This is a remarkable result, since the f^2-noise term, which is the dominant contribution to the bandwidth-integrated noise, shows an inverse dependence with N, a better signal-to-noise ratio (SNR) can be achieved.

3. Results

Let us now apply the sliced photodiode technique to an actual feedback TIA design. Since the technique can be employed with the independence of the core-amplifier design, in this work, the configuration employed to perform the simulation was a TIA consisting of three cascaded common-source stages with a negative resistive loop, as shown in Figure 3. An output common-source buffer was included to employ it as a simple signal adder. The circuit was implemented in 65-nm CMOS technology with a single 1.2-V voltage supply. To model the PD, we used the PD parameters reported in [14], that is $C_{PD} = 14$ pF and a responsivity of 0.42 A/W at 850 nm. As the main purpose of this letter is to demonstrate the feasibility, the proposed divide-and-conquer technique, we chose a BW of 1 GHz, for which we optimized the TIA design, achieving a maximum sensitivity of −11.0 dBm. All simulations were performed using the Cadence Spectre Simulation Platform with a BSIM3v3.2 level 53 transistor model for the TSMC 65-nm CMOS technology.

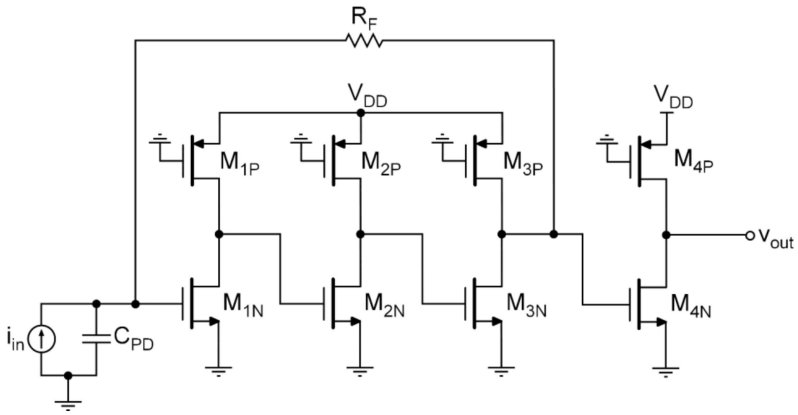

Figure 3. Transistor-level topology of the transimpedance amplifier employed in the simulations to test the proposed noise-reduction technique.

Next, as a first approximation, we divided the PD into N equal pieces and replicated the TIA N times, using a feedback resistor N times larger and the same voltage amplifier as in the original design. By combining the output signals of each TIA, we increased the SNR by a factor of roughly $\sqrt{N}$. Since the voltage signals are summed linearly, and the uncorrelated noise sum is quadratic, we ended up obtaining the equivalent input-referred noise expression (7), effectively reducing it and improving the sensitivity of the read-out.

In this work, the sliced PD technique was applied, dividing the PD into N pieces, choosing powers of 2 for the values of N, up to 16. To combine the output signals of each TIA, we employed the output buffer, splitting the transistor M_{4N} shown in Figure 3 into N equal transistors to implement a simple signal adder. Since the transconductance of each transistor was now divided by N, the output signal should remain similar to the single-PD case, but the quadratic sum of the noise contributions should provide an increase in the SNR. Figure 4 shows the equivalent input-referred noise response, clearly exhibiting a greater decrease in the spectral density at high-frequencies for higher N values. It is clear that a decrease in the f^2-noise contribution was achieved, leading to a better SNR and, thus, higher sensitivity. To calculate the sensitivity of the TIA, we considered a 1.25 Gb/s pseudo-random bit sequence (PRBS) non-return-zero binary data transmission with a bit error ratio (BER) better than 10^{-12}.

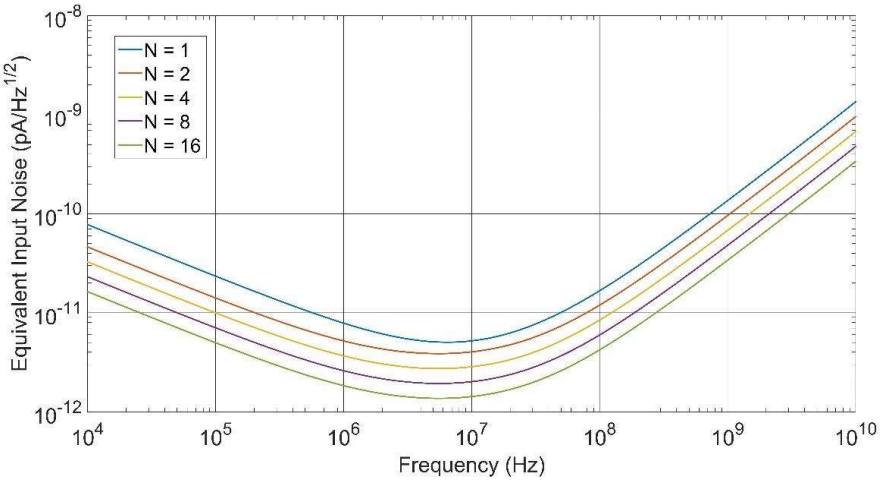

Figure 4. Input-referred noise of the front-end using the divide-and-conquer technique for different numbers of pieces.

Table 1 summarizes the key performance parameters of the front-end obtained by slicing the PD into different numbers of pieces. There was a remarkable increase in the sensitivity, measured for a BER of 10^{-12}, from −11.0 dBm using the traditional single-PD approach to −15.8 dBm by slicing the PD into 16 pieces. This means that using this technique, we obtained an improvement of 4.2 dBm. Notice that the noise was three times lower even though the bandwidth increased by 32%. The main drawback is power consumption, which increases by a factor of N.

Table 1. Summary of the simulation results using the sliced-PD technique with different numbers of slices.

Parameter	N = 1	2	4	8	16
R_T (dBΩ)	75.7	75.7	75.8	75.8	75.7
BW [1] (GHz)	1.02	1.20	1.31	1.34	1.35
Input RMS Noise (μA)	4.74	3.89	2.57	1.89	1.58
Sensitivity *	−11.0	−11.8	−13.7	−15.0	−15.8
Power ** (mW)	2.9	5.8	11.5	23	46

[1] 3-dB bandwidth (BW); * Measured sensitivity for the transmission of a 1.25 Gb/s pseudo-random bit sequence (PRBS) with non-return to zero (NRZ) encoding with a bit error ratio (BER) of 10^{-12}; ** Total electrical power consumption of the transimpedance amplifier.

As mentioned above, the TIA design was bonded to the intrinsic capacitance of the PD. After slicing the PD, the capacitance was lowered by a factor of N. Therefore, in a second case, we optimized the TIA with $N = 16$ to compare the performance of an optimized 16-pieces sliced-PD versus the optimized single-PD approach. Table 2 summarizes the design parameters of each optimized design approach for a 1-GHz BW and compares their performances.

A much higher transimpedance was achieved after optimizing the TIA for the 16-piece sliced-PD case. Although the increase in power consumption by a factor of 13 cannot be ignored, it is remarkable that the input RMS noise was lowered by a factor of 6, improving the sensitivity by almost 8 dBm.

Finally, it is noteworthy that an optimized design with a single PD and the same power budget did not improve performance to the same extent as the proposed technique.

Table 2. Comparison of the simulation results with optimized parameters for both approaches, the traditional approach, and applying the sliced-PD, respectively.

Parameter	Single PD Fixed BW	Single PD Fixed Power	16 Sliced-PD
R_T (dBΩ)	75.7	80.3	84.4
BW (GHz)	1.02	1.21	1.02
Input RMS Noise (μA)	4.74	1.82	0.78
Sensitivity (dBm@BER = 10^{-12})	−11.0	−15.1	−18.9
Power (mW)	2.9	38.8	38.8

4. Conclusions

A novel photodiode read-out design technique to use with large active area photodiodes has been presented in this letter. It consisted of slicing the photodiode area and connecting a TIA to each piece, instead of the conventional single-PD approach. The simulation post-layout results showed that the sensitivity was improved while maintaining the bandwidth and also that the achieved transimpedance could be much higher when the technique was applied, dividing the PD into a large number of pieces. In this letter, we have shown that the proposed divide-and-conquer technique is a good candidate to improve the sensitivity of POF equipment with high junction capacitance integrated PDs, and it can potentially be employed in a vast amount of applications where optical sensors with large-area photodiodes are required. Moreover, it does not depend on the transistor-level architecture of the TIA, which makes it compatible with almost every TIA design.

Author Contributions: G.R. proposed the study of the divide-and-conquer technique and performed the theoretical analysis and first approach simulations. S.C. contributed to the system design and the simulations; G.R., C.S.-A., C.A. and S.C. contributed to the data analysis and the writing of the paper. All authors have read and agreed to the published version of the manuscript.

Funding: This work has been partially supported by MINECO-FEDER TEC2017-86867-R and MINECO fellowship program to Guillermo Royo (BES-2015-073748).

Conflicts of Interest: The authors declare no conflict of interest.

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Article

A Highly Linear Low-Noise Transimpedance Amplifier for Indoor Fiber-Wireless Remote Antenna Units

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Received: 15 March 2019; Accepted: 12 April 2019; Published: 16 April 2019

Abstract: This article presents an optimized design of a low-noise transimpedance amplifier (TIA) with high linearity for use in the downlink receiver of a remote antenna unit (RAU). The aim of this design is to be used in a cost-effective indoor distributed antenna system (DAS) for WLAN transmission using a mixed fiber-wireless system. The circuit topology consists of a fully differential shunt–shunt feedback TIA with digitally programmable transimpedance. An open-loop gain compensation technique is used to maintain stability and constant bandwidth (BW). The TIA has been fabricated in 65 nm CMOS technology with a 1.2 V voltage supply. The total power consumption of the TIA is 6 mW. A complete electrical and optical characterization with a 1550 nm PIN photodiode has been performed to demonstrate the reliable 54 Mb/s 802.11a WLAN transmission achieved with an error vector magnitude (EVM) lower than 3% for a 20 dB optical input range.

Keywords: intermediate frequency over fiber; multi-mode fiber; programmable gain; remote antenna unit; transimpedance amplifier

1. Introduction

The increase in demand for mobile devices has driven the development of wireless systems over the last few years. The main requirements of these new communication systems are good accessibility and robustness, achieving high data capacity. Actual short-range indoor wireless networks must enhance their coverage and show a higher immunity to interferences with neighboring networks with a signal distribution that is better confined in the volume of interest.

In this context, the integration of fiber-wireless networks has emerged as a promising solution to support the rate of growth of data traffic demand for wireless applications, either indoor or outdoor, combining the best of these technologies: the mobility of wireless technologies and the low attenuation and large bandwidth (BW) of optical fibers.

The interest in mixed fiber-wireless systems has grown in recent years, especially for short-range indoor applications, which can benefit from radio-over-fiber (RoF) distributions, as is the case with distributed antenna systems (DASs) [1,2]. These systems are flexible and there is a good compromise between data capacity, accessibility, and the overall cost of installation and maintenance, allowing for a good convergence of optical fiber capacity and wireless access flexibility [3]. The system operation consists of distributing the signal through multi-mode fiber (MMF) from a base station (BS) to distributed remote antenna units (RAUs), which provide an optical-wireless interface (see Figure 1). To decrease the effects of fiber chromatic dispersion, the wireless signals can be down-converted before the optical transmission, employing an intermediate frequency (IF) communication scheme [4].

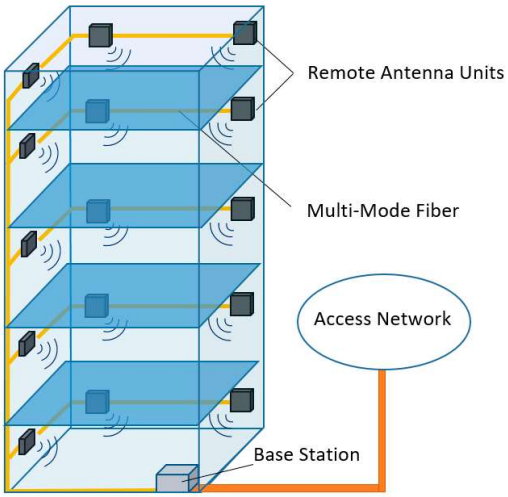


Figure 1. Scheme of a distributed antenna system (DAS) fed by multi-mode fiber (MMF) for indoor networks.

The key of a DAS is to employ cost-effective components in the three main elements of the communication system. This is achieved with the use of MMF, which presents immunity to electromagnetic interferences and offers a large BW, and therefore a very high data capacity, along with cost-effective photonic devices, such as vertical-cavity surface-emitting lasers (VCSEL), and a low-cost, low-power design of the RAUs, with low-cost transceivers and a design of moderate complexity. Figure 2 shows three different downlink RAU configurations, depending on how the data transmission is performed: (a) baseband over fiber (BBoF), (b) radio over fiber, and (c) intermediate-frequency over fiber (IFoF).

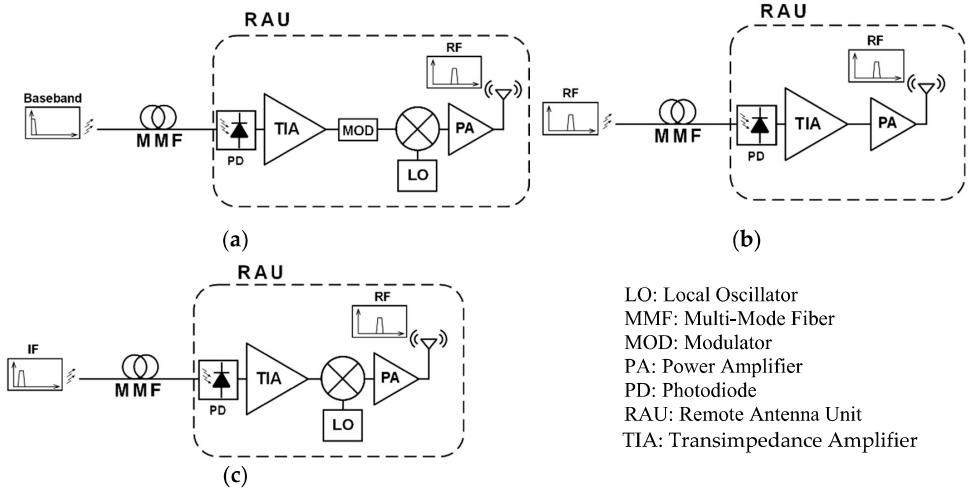


Figure 2. Conceptual scheme of the downlink of remote antenna units for (**a**) baseband over fiber, (**b**) radio over fiber, and (**c**) intermediate-frequency over fiber.

The BBoF scheme is the typical configuration of optical receivers for long-reach fiber communications. With this scheme, very high bit rates of the order of several Gb/s can be achieved. However, it requires the most complex design of the RAU, as it must perform data modulation and

demodulation as well as frequency conversion, also increasing the power consumption. Therefore, the overall cost of the BBoF-based DAS can rise considerably since a high number of RAUs is needed.

On the opposite side, the RoF scheme presents the simplest RAU architecture, because the RAU only has to perform opto/electrical (O/E) and electro/optical (E/O) conversion and signal amplification. The RF signal generation is centralized at the BS, increasing its flexibility. These systems, however, require much higher linearity than BBoF to transmit the signal properly and they show distance limitations when transmitting several WLAN standards due to the high chromatic dispersion of the fiber at such frequencies [5]. Several attempts to design RAUs for RoF have been made in recent years with promising results and performance, transmitting RF at 2.5 GHz [6,7], 5 GHz [8], or 12 GHz [9]. However, RoF systems require high-speed circuit design and high-performance photonic devices, therefore increasing the power consumption and the overall cost of the DAS significantly. Moreover, at higher frequencies, there are undesired effects such as power penalty periodically fading and nonlinearities inducing spectrum broadening of the baseband data around the carrier signal [10–13].

IFoF systems present advantages upon both BBoF and RoF. RAUs for IFoF do not require the implementation of a modulator/demodulator as in BBoF. Therefore, the complexity in the design of the RAU is much simpler than that in BBoF systems, and the power consumption is significantly lower.

Similar to RoF, the signal is generated at the BS with the same modulation format as the RF signal, but at a lower frequency. Nevertheless, since the optical signal is modulated with a much lower frequency, the use of an IFoF system minimizes the effect of the MMF chromatic dispersion and significantly drops the overall cost since lower performance and less expensive photonic devices can be used, at the BS but more importantly at the RAU, for both O/E conversion in the downlink and E/O conversion in the uplink.

However, the complexity of the RAU increases with an IFoF scheme with respect to an RoF system. To recover the original RF signal, the RAU now requires a high speed mixer and a stable local oscillator, which is used in both the downlink and the uplink of the RAU, with an accurately tuned frequency to carry out the frequency up-conversion and down-conversion, respectively. Furthermore, to generate the LO signal, a pilot carrier can be delivered to the RAU optically, allowing a higher flexibility and frequency tuning without the need of quartz crystal or similar devices.

In this work, we focus on the design of the RAU downlink for use in a distributed antenna system using IFoF data transmission. The RAU downlink consists of (1) a photodiode (PD); (2) a transimpedance amplifier (TIA); (3) a frequency up-converter to translate the signal from IF to the final RF, (4) a power amplifier (PA) to provide gain and good matching, and (5) the antenna. In particular, we aim for an optimized design of a new fully differential TIA with high linearity and low noise performance that shows a better error vector magnitude (EVM) than recently published RoF works. The TIA is digitally controllable with a double gain control, maintaining a flat frequency response and constant BW and achieving also a very high input range to enhance the communication system flexibility. The proposed TIA has been fabricated in a 65 nm CMOS process with a 1.2 V voltage supply. This paper is an extended version of the work presented at conferences [14,15], where a preliminary electrical characterization of the device was presented. This work includes unpublished evidence of the validity of the proposed optical receiver by the complete optical characterization of the RAU downlink front end for an IFoF communications system.

The paper is structured as follows: Section 2 provides detailed descriptions of the design of the RAU downlink and the TIA topology and of the design of the RAU for IFoF; Section 3 summarizes the experimental characterization with both electrical and optical measurement results, and Section 4 presents the main conclusions of this work.

2. Design of the Transimpedance Amplifier

One of the main advantages of IFoF is the lower performance requirement of the photonic devices. Nevertheless, the RAU must present low noise and a very high linearity to achieve a low EVM level. Accordingly, the O/E front-end must be able to satisfy these performance requirements. The main focus

of this work is the design of the O/E front end, including a new low-noise transimpedance amplifier with a fully differential implementation to achieve better linearity, using an external 1550 nm PIN photodiode. With the IFoF scheme, the BW requirement and the tradeoff between sensitivity and power consumption is relaxed, so the complexity of the design of the TIA is reduced.

The proposed TIA, shown in Figure 3, is aimed for short-range wireless transmission with an input IF signal at 100 MHz, and it has been designed and fabricated with 65 nm RF CMOS technology. The main purpose of the design is to achieve a reliable transmission of an 802.11a 54 Mb/s WLAN data signal at 5 GHz, which is a multi-carrier OFDM standard that uses 64 QAM modulation.

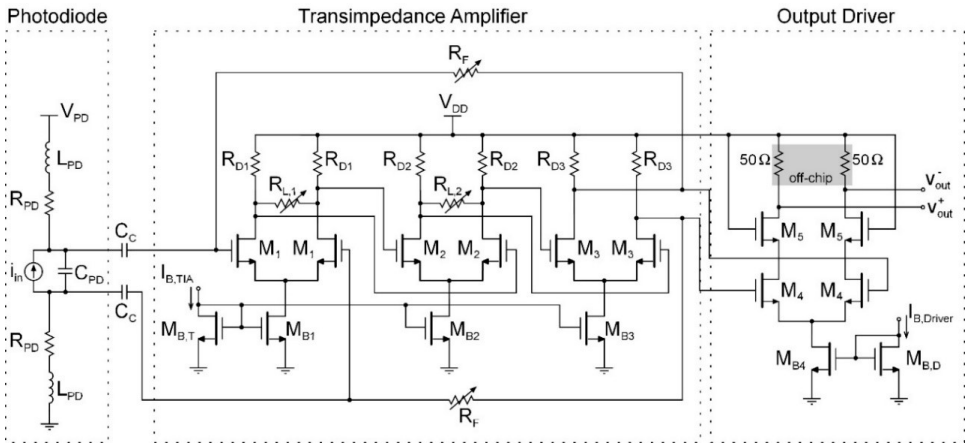


Figure 3. Transistor-level topology of the proposed low-noise transimpedance amplifier (TIA) for the remote antenna unit (RAU) downlink. An output driver is included for measurement purposes.

The PD receives the input optical signal and generates an electrical current, which must be converted to voltage by the transimpedance amplifier, which is the first stage of the analog front end. The TIA is typically one of the most critical modules in an optical receiver. Firstly, since the photogenerated current signal is small, the TIA must show a very low equivalent input noise (EIN) level, as it determines the overall noise of the system. Therefore, the sensitivity of the receiver is mainly determined by the EIN of the TIA.

The TIA must provide a good matching with the PD, which typically presents high parasitics due to the intrinsic junction capacitance, which can be as high as some pF. Therefore, the design of the TIA requires a low input impedance in order to compensate the high PD capacitance to exhibit a wide BW to amplify the incoming signal accordingly. Recent publications report the use of integrated avalanche photodiodes (APDs), which show very low junction capacitances [6,8]. However, these PDs are lacking in linear performance in comparison with PIN PDs. IFoF communications require a very high linearity, as it has a great impact on the EVM. Therefore, in this work, a PIN PD combined with the design of a highly linear TIA are proposed, so that the EVM of the RAU can be maintained at a very low level. The regulated cascode and other open-loop TIA structures based on the common-gate stage have been widely employed in high-speed optical receivers, since they can achieve a high BW with low noise performance. Nevertheless, these topologies show a worse linear behavior, typically not enough for IFoF communications, where linearity is critical to properly transmit the signal. On the other side, closed-loop TIAs, which have been widely used in high-speed optical receivers, can also achieve a wide BW while they present a low EIN and a much better linearity than open-loop configurations [16]. These last two characteristics are mandatory to increase the input dynamic range of the analog front end.

In this work, a shunt–shunt feedback TIA configuration has been employed, as this topology shows a low input impedance and a high linearity, which is the most important characteristic to achieve the best performance for IFoF applications. To improve the system linearity, a differential topology

has been chosen, so that second order intermodulation products as well as the effect of supply and substrate noise are strongly reduced [17].

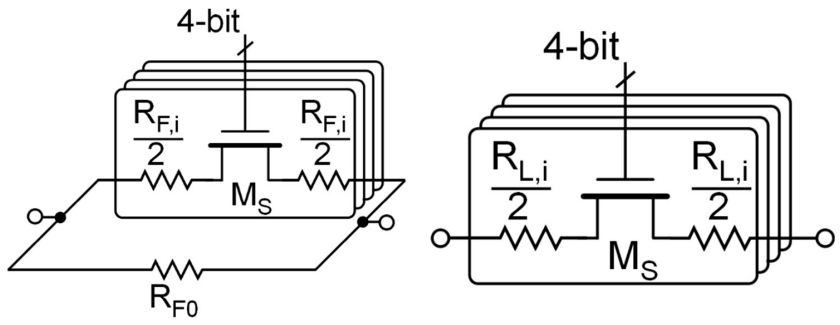
The proposed TIA consists of a differential voltage amplifier and a negative feedback loop. The implementation of the voltage amplifier consists of three cascaded differential pairs and two resistor arrays are employed for the feedback loop. These arrays are digitally programmable to include a gain control of the TIA to increase the input dynamic range of the RAU downlink by varying the transimpedance, R_T, which, in a second-order transfer function approximation can be written as:

$$R_T = \frac{v_{out}^{+} - v_{out}^{-}}{i_{in}} \approx -\frac{2R_F}{1 + \frac{2R_F C_{in}}{A} s + \frac{2R_F C_{in}}{A\omega_A} s^2} \tag{1}$$

where R_F is the feedback resistor, C_{in} the total input capacitance, which is dominated by the parasitic capacitance of the photodiode, C_{PD}, and A and ω_A are the gain and dominant pole frequency of the core amplifier, respectively. It is a rough approximation, but it is useful to illustrate the proposed frequency compensation mechanism. To achieve high sensitivity, considerably high feedback resistors of the order of several kΩ should be employed to maximize transimpedance. Higher transimpedance results both in higher signal amplification and lower EIN. The dependence of the equivalent input current noise density on the feedback resistor in a differential shunt–shunt feedback TIA can be approximated by the following equation:

$$EIN^2 \approx \frac{2K_B T}{R_F} + \frac{\overline{v_{n,A}^2}}{2R_F^2}\left(1 + 4\omega^2 C_{in}^2 R_F^2\right) \tag{2}$$

where K_B is the Boltzmann constant, T the temperature, and $\left(\overline{v_{n,A}^2}\right)$ the equivalent input noise of the voltage amplifier. It is clear that, according to Equation (2), the higher the R_F, the lower the input noise. However, there is an important tradeoff between this parameter and linearity. As the output voltage swing increases, the saturation and the inherent nonlinearities of the CMOS devices start to distort the signal, therefore raising the EVM and shrinking the input dynamic range. As mentioned above, with a digitally programmable feedback resistor, R_F (see Figure 4a), the transimpedance can be reduced for large input signals, avoiding saturation as well as nonlinear distortion due to a large output voltage swing, thus extending the input dynamic range.



(**a**) (**b**)

Figure 4. Implementation of the 4-bit programmable resistor arrays (**a**) feedback resistor, R_F, and (**b**) load resistors, $R_{L,i}$.

However, it is well known that the quality factor of the transfer function, Q, which can be derived from Equation (1), depends on the feedback resistor and increases for lower R_F values [16]. This might significantly impact the circuit stability as the system becomes underdamped for high Q values, so another control needs to be implemented to keep this factor at lower values. The Q factor, derived from Equation (1) can be approximated by

$$Q \approx \sqrt{\frac{A}{2R_F C_{in} \omega_A}}. \tag{3}$$

Thus, the most direct way to keep Q constant against R_F changes is to modify the open-loop gain A proportionally. This gain control is made with the implementation of variable load resistors in the first two differential pairs, $R_{L,i}$. These resistors, as shown in Figure 4b, consist of a resistor array that is digitally programmable with a 4-bit thermometer-coded digital word, B. Therefore, a simultaneous control of the feedback and the load resistors is made to control both transimpedance and open-loop gain accordingly.

A transistor-level simulation has been carried out with a single control of the feedback resistor to compare the frequency response of the TIA using the double control of both feedback resistor and open-loop gain. As Figure 5 shows, the response without an open-loop gain control shows a frequency peak higher than 4 dB, and the BW increases with lower transimpedance. However, applying the compensation technique, the frequency response is always flat and the BW is almost constant.

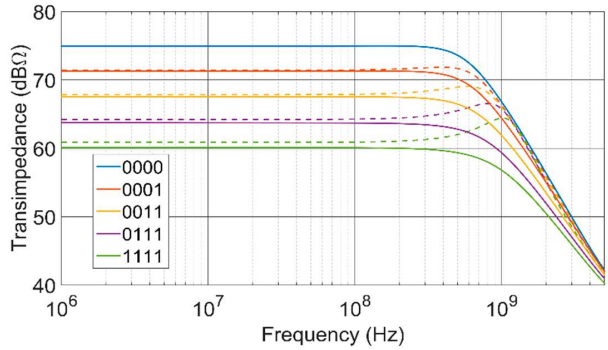


Figure 5. Frequency response of the TIA with simultaneous gain control (solid line) and single feedback resistor control (dashed line).

3. Experimental Characterization

The proposed circuit has been fabricated in 65 nm CMOS technology using a single voltage supply of 1.2 V. The downlink front end has been designed for an external InGaAs PIN PD, which presents a junction capacitance of approximately 0.45 pF and a 0.85 A/W responsivity at 1550 nm. For measurement purposes, an output driver with 50 Ω output resistance has been implemented to provide a good matching with the measurement instrumentation.

The total RAU downlink area including pads is 2000 × 1150 µm, and the active area of the TIA and the driver is of 115 × 130 µm (see Figure 6).

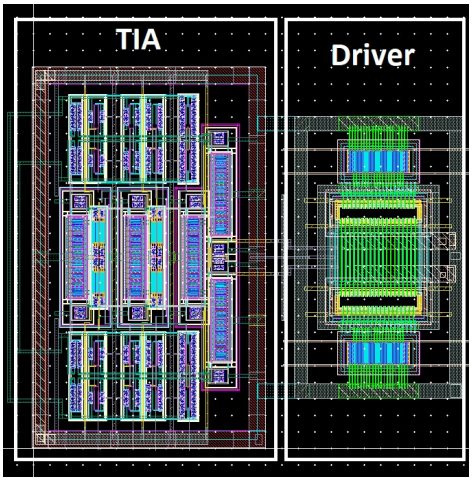
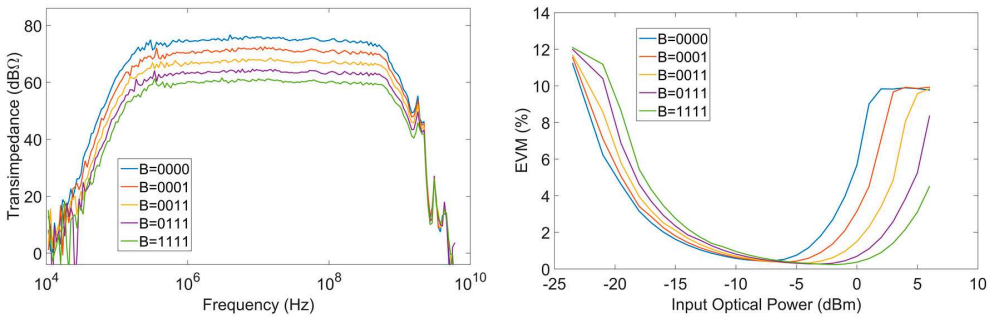


Figure 6. Layout of the active area of the transimpedance amplifier and the output driver.

3.1. Electrical Measurements

To obtain the TIA frequency response, we measure the S21 parameter using a network analyzer (Rohde & Schwarz ZVL 9 kHz-6 GHz). As shown in Figure 7a, the range of programmability with the integrated 4-bit thermometer-coded control of the transimpedance covers up to a 16 dB variation, with a linear-in-dB control from 60 to 76 dBΩ in 4 dB steps. The simultaneous double control avoids frequency response peaking at low transimpedance. Linearity measurements have been carried out using the demodulation of a 54 Mb/s 64 QAM signal at 100 MHz.

Figure 7b shows the measured EVM versus the equivalent input optical power of the signal, at each transimpedance state. The electrical measurements have been performed using a vector signal generator (VSG, Rohde & Schwarz SMW200A) and analyzer (VSA, Keysight M9391A). The TIA presents an EVM lower than 2% for an input RF power range of 40 dB, from −60 to −20 dB, which corresponds to an optical input of −16 to +4 dBm. Noise simulations have been made to take into account only the TIA noise, which exhibits an EIN of 2 pA/$\sqrt{\text{Hz}}$. The power consumption of TIA alone is 6 mW.



(**a**) (**b**)

Figure 7. (**a**) Overall link frequency response and transimpedance of the TIA and (**b**) measured error vector magnitude (EVM) as a function of the input RF power for each transimpedance configuration. Data from [14].

3.2. Optical Characterization

The experimental set-up for optical data transmission is shown in Figure 8. At the transmitter side, the VSG generates the 54 Mb/s 802.11a WLAN signal at 100 MHz, whose spectrum is shown in Figure 9a. The electrical IF signal is then converted to an optical signal by an electro-optical modulator (Keysight M9403B). This latter module consists of a laser diode with a 1550 nm wavelength, externally modulated by the input IF signal and provides an optical signal with an optical power of 5 mW. The laser is then directly coupled to a 2 m MMF. The MMF is coupled to the InGaAs PD (PDINCF070SC21 M 0), which is connected to the TIA input. To avoid damages to the PD due to the high output power of the laser, a 10 dB optical attenuator is added to the set-up. Finally, a balun is used at the output to convert the differential signal into single-ended for the VSA input, where the output signal, shown in Figure 9b, is received.

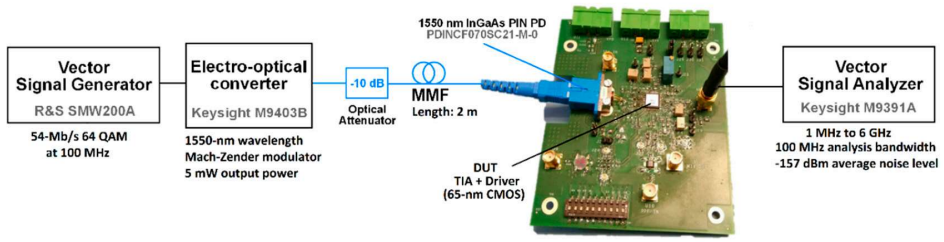
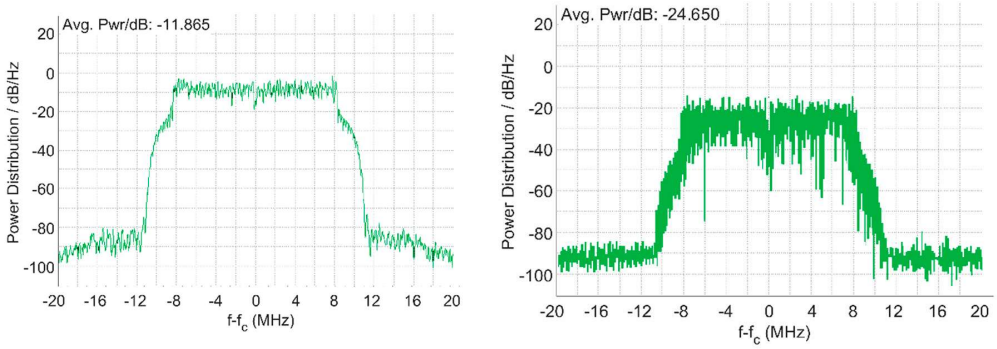


Figure 8. Schematic diagram of the experimental set-up for optical data transmission.



(**a**) (**b**)

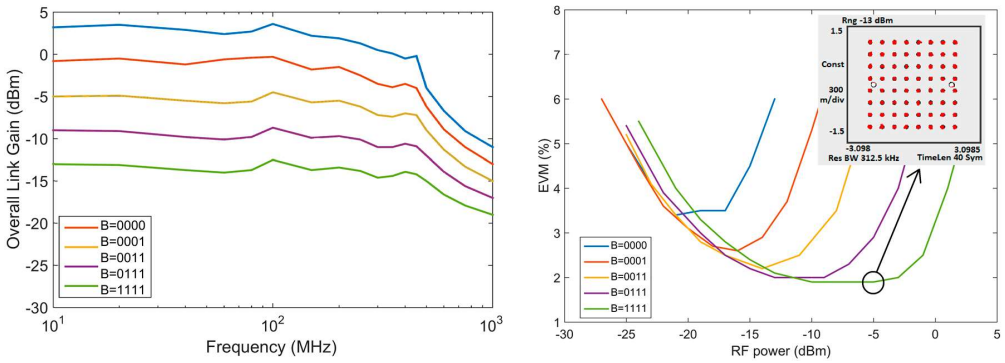
Figure 9. (**a**) Input spectrum of the integrated optical receiver with f_c = 100 MHz. (**b**) Output spectrum of the integrated transimpedance amplifier.

The frequency response is measured using the transmission of a continuous wave. The overall link gain from the VSG to the VSA is shown in Figure 10a for each gain configuration. The BW is substantially reduced with respect to the electrical characterization, mainly due to the high parasitic capacitance of the PD. Nevertheless, it is almost constant around 300 MHz with an attenuation lower than 1 dB at 100 MHz and the 16 dB linear in dB transimpedance control is achieved with no frequency peaking, thanks to the simultaneous control of the feedback resistor and the open loop gain. Linearity measurements are carried out using the demodulation of an 802.11a 54 Mb/s transmission using 64 QAM modulation at 100 MHz. The measured EVM results are shown in Figure 10b as a function of the RF power at the output of the VSG, for each transimpedance configuration. The results show an EVM lower than 2% for a 10 dB optical power range and lower than 3% for a 20 dB optical power range.

The main measurement results for the proposed IFoF RAU are summarized in Table 1 with a comparison to recently published TIAs for RoF and IFoF applications. Despite the differences on the

frequency of operation of these applications, to make a fair comparison of the performance, we define a figure of merit (FoM):

$$\text{FoM} = \frac{\text{Transimpedance } (\Omega) \cdot \text{BW (GHz)}}{\text{Power Consumption (mW)}}. \quad (4)$$



(**a**) (**b**)

Figure 10. (**a**) Frequency response of the electro-optical front end. The BW is maintained almost constant at around 300 MHz and (**b**) output signal error vector magnitude using the demodulation of a 54 Mb/s 802.11a WLAN signal.

Table 1. Summary of measurement results and comparison with RF transimpedance amplifiers.

Parameter	[6]	[8]	[9]	[18] **	This Work
RAU Architecture	RoF	RoF	RoF	IFoF	IFoF
Technology	130 nm CMOS	180 nm CMOS	150 nm PHEMT	65 nm RF CMOS	65 nm RF CMOS
Photodiode Technology	Integrated APD	Integrated APD	External PIN	Integrated PD	External PIN
Supply Voltage	1.2 V	1.8 V	5 V	1.2 V	1.2 V
Transimpedance	54 dBΩ	62 dBΩ	46 dBΩ	51–73 dBΩ	60–76 dBΩ Linear-in-dB
Frequency of operation	2.5 GHz	5.2–5.8 GHz	12 GHz	550 MHz	300 MHz
Input Noise Current Density	N/A	7.3 pA/ $\sqrt{\text{Hz}}$	26 pA/ $\sqrt{\text{Hz}}$	3.4 pA/ $\sqrt{\text{Hz}}$	2 pA/ $\sqrt{\text{Hz}}$ **
EVM	3.89%	2.5%	3%	N/A	2%
Total Power Consumption	18 mW	156 mW *	100 mW	4.8 mW	6 mW
FoM (Ω·GHz/mW)	70	47 *	24	511	315

* Including output buffer; ** Simulation results.

As shown in Table 1, the TIAs aimed for IFoF achieve a much better FoM than those designed for RoF applications, mainly due to the higher transimpedance and the lower power consumption. The FoM of the other TIA for IFoF [18] is slightly higher than the one achieved in this work. However, it shows simulation results and for linearity measurements it only reports the OIP3 at the maximum transimpedance, with no information about the EVM. Moreover, in [18], only the linearity results at the highest transimpedance are reported, so it does not guarantee good linearity at lower gain configurations. In this work, we present the first IFoF TIA with a linear in dB gain control that is able to extend the input dynamic range for which high linearity is achieved. It shows a better linear performance than RoF receivers, as our proposal achieves an EVM lower than 2% through a wider

input dynamic range of 10 dB optical power, compared to the 3 and 5 dB ranges reported in [6] and [8], respectively. Another advantage of this design is the adaptability of its response to higher input capacitances by adjusting the transimpedance and open-loop gain. This design is compatible with commercially available external PIN photodiodes, which can present a much higher junction capacitance, of the order of pF, compared to the greatly low 35 fF and 140 fF capacitances of the integrated PD presented in [8] and [9], respectively.

4. Conclusions

A highly linear low-noise differential TIA to be used in IFoF RAUs has been presented in this paper. The front end has been designed in 65 nm RF CMOS technology with a 1.2 V voltage supply. The proposed design performs a 16 dB linear-in-dB gain control using a method through which the stability is ensured with a simultaneous control of transimpedance and open-loop gain. The TIA achieves an almost constant −3 dB cut-off frequency of 300 MHz and attenuation lower than 1 dB at 100 MHz in all gain configurations. The proposed TIA achieves a 20 dB and 10 dB input optical range with an EVM lower than 3% and 2%, respectively. The lower input noise current density and EVM of the proposed TIA are superior to those reported in recently published works, also with a much lower power consumption achieved with the proposed design. The IFoF scheme presents a high potential and several advantages over RoF, being a good alternative to lower the costs and improve the performance of cost-effective fiber-wireless distributed antenna systems.

Author Contributions: G.R., C.A., and S.C. contributed to the design of the proposed topology; G.R. performed the simulations, the layout design, and the complete experimental characterization of the system; all authors contributed to the data analysis and the writing of the paper.

Acknowledgments: This work has been partially supported by MINECO-FEDER (TEC2014-52840-R and TEC2017-85867-R) and the MINECO fellowship program to Guillermo Royo (BES-2015-073748).

Conflicts of Interest: The authors declare no conflict of interest.

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Microelectronics Reliability 83 (2018) 25–28

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Fully-differential transimpedance amplifier for reliable wireless communications

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ARTICLE INFO

Keywords:
Transimpedance amplifier
Radio-over-fiber
Programmable gain
High linearity

ABSTRACT

The demand of mobile and wireless devices has been continuously growing over the last years, driving the development of new wireless communication systems to provide high data capacity and good accessibility at high data transmission rates. Wireless communication systems must also show high immunity to interference, and in this context distributed systems formed by several remote antenna units (RAU) fed by multi-mode fibers are becoming the preferred solution. At high transmission data rate increases, issues brought by the variability in the fabrication of the circuits and ambient conditions (PVT variations) become more important, and it is necessary to design the systems to minimize their effect. In this work, a fully-differential transimpedance amplifier (TIA) for the receiver in a RAU is presented. The TIA has been designed in a 180-nm RF CMOS technology with a 1.8-V voltage supply and it achieves a bandwidth of 2.5 GHz with a power consumption of 26 mW. To overcome the effect of PVT variations, the TIA features a programmable transimpedance of 20-dB linear-in-dB programmable transimpedance, also increasing the input dynamic range to improve the overall linear range of operation.

1. Introduction

In recent years, there is a growing interest in distributed antenna systems (DAS) fed by multi-mode fibers (MMF), especially for in-door applications. In this context, transmitting radio over fiber (RoF) can be a good alternative to enhance the performance of short-range wireless networks. In a RoF communication system (see Fig. 1), the RF signal is generated in a central station (CS), directly modulating a vertical-cavity surface-emitting laser (VCSEL) with low optical modulation index (typically around 10%–30%) and is then sent to several remote antenna units (RAU) through MMF, which presents very low attenuation, wide bandwidth and immunity to electromagnetic interferences. Delivering the RF signal from the CS to the downlink of several low-power RAUs, instead of using a single high-power emitter offers a more reliable distribution of the wireless signal, which results in very good coverage while reducing interferences with other networks [1].

However, to ensure a high data capacity and good coverage, a dense network of RAUs is needed. To reduce the cost of installing a distributed antenna system, cost-effective fully-integrated RAUs must be designed. RoF systems provide simpler and cost-effective RAU configurations, as both downlink and uplink must only amplify and convert the RF-modulated light to a wireless RF signal and vice versa, respectively, while the RF signal generation and processing is centralized in the CS.

As shown in Fig. 2, the design of the downlink consists of five main elements: (i) a photodiode (PD) that converts the RF-modulated light into current; (ii) a transimpedance amplifier (TIA) to recover the RF signal in voltage; (iii) a variable-gain amplifier (VGA) to provide enough gain, (iv) a power amplifier (PA) and (v) the antenna. The main requirements for RAUs are low noise and high linearity to properly process the RF signal. Consequently, an optical front-end must be available to bring these characteristics together.

In this work, we propose the design of a new fully-differential, low-noise transimpedance amplifier with highly linear performance aimed for use in a RAU for short-range RoF communications. It achieves a bandwidth up to 2.5 GHz and a controllable gain to increase the input dynamic range. The proposed TIA has been designed in a 180-nm RF CMOS technology.

The paper is organized as follows: Section 2 provides a detailed description of the proposed transimpedance amplifier; Section 3 presents the simulation results and Section 4 presents the main conclusions of this work.

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https://doi.org/10.1016/j.microrel.2018.02.007
Received 18 November 2017; Received in revised form 16 January 2018; Accepted 11 February 2018

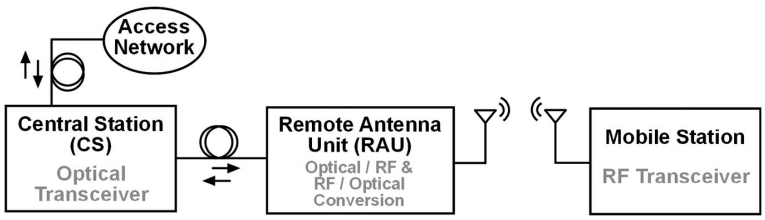

Fig. 1. Block diagram of a radio-over-fiber communication system.

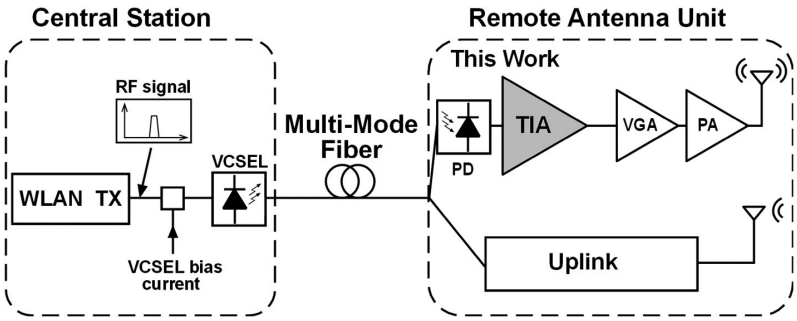

Fig. 2. Block diagram of a radio-over-fiber downlink.

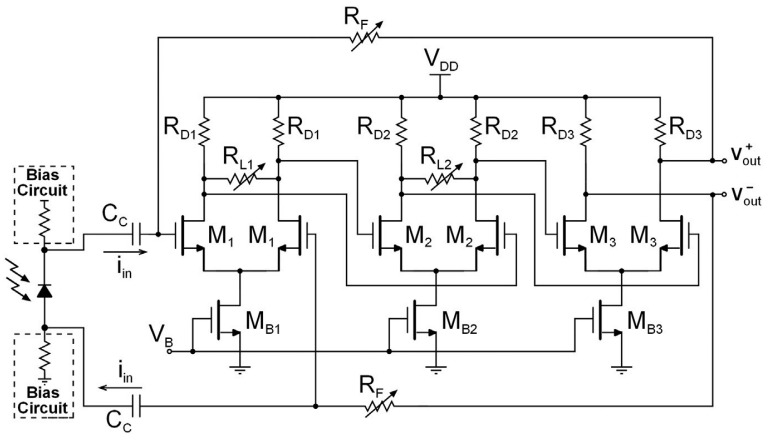

Fig. 3. Transistor-level topology of the proposed TIA.

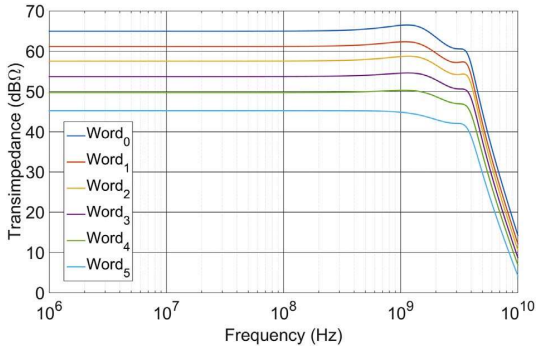

Fig. 4. Frequency response of the TIA with double control of transimpedance and open-loop gain.

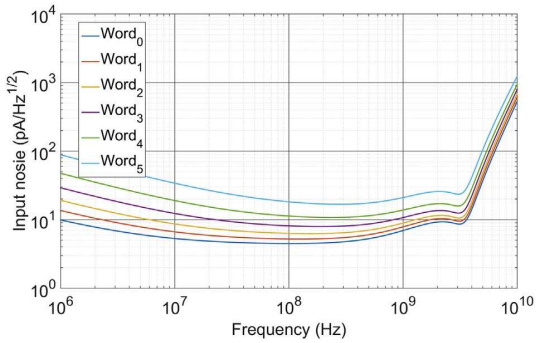

Fig. 5. Input-referred noise of the TIA.

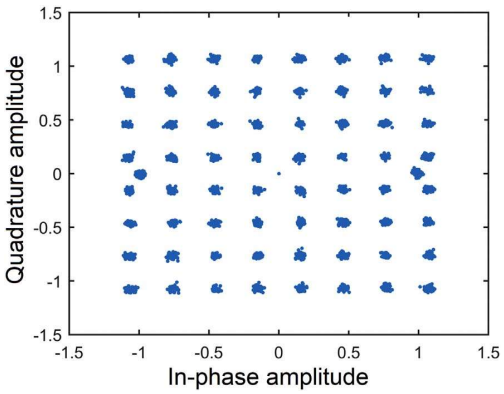

Fig. 6. Constellation diagram of demodulated signal at the maximum transimpedance configuration of 65 dBΩ with −9 dBm optical input power at 20% optical modulation index.

Table 1
Summary of the simulation results and comparison with other RF transimpedance amplifiers.

Parameter	[3]	[4]	[10]	This Work
Technology	130-nm CMOS	180-nm CMOS	150-nm PHEMT	180-nm RF CMOS
Photodiode technology	Integrated APD	Integrated APD	External PIN	External PIN
Supply voltage	1.2 V	1.8 V	5 V	1.8 V
Transimpedance	54 dBΩ	62 dBΩ	46 dBΩ	45–65 dBΩ
Bandwidth	2.5 GHz	5.2–5.8 GHz	12 GHz	2.5 GHz
Input noise current Density	N/A	7.3 pA/$\sqrt{\text{Hz}}$	21 pA/$\sqrt{\text{Hz}}$	10 pA/$\sqrt{\text{Hz}}$
EVM	3.89%	2.5%	3%	2%
Power consumption	18 mW	156 mW	100 mW	26 mW
FoM (Ω·GHz/mW)	70	47	24	171

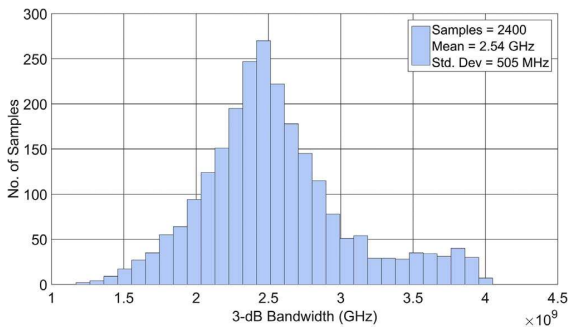

Fig. 7. Monte Carlo simulation results for bandwidth at any transimpedance configuration.

2. Circuit description

The transimpedance amplifier that converts the RF photocurrent to a measurable voltage signal is, together with the photodiode, the most critical block in an optical receiver. It is mandatory that the TIA present a very low noise level, as the equivalent input noise (EIN) of the TIA will determine the overall noise of the system and, therefore, the design must be optimized to achieve a high sensitivity [2].

The bandwidth depends greatly on the frequency response of the PD-TIA block. In some recently published works, integrated avalanche photodiodes (APD) with very low junction capacitance are employed

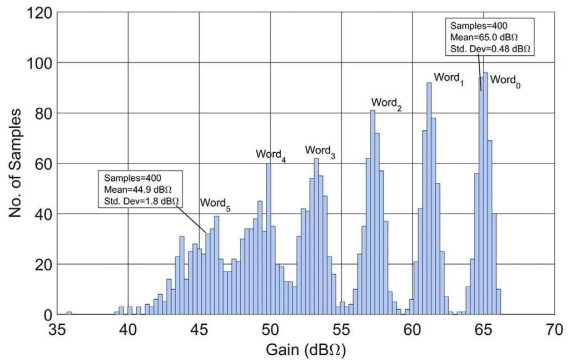

Fig. 8. Monte Carlo simulation results for transimpedance.

[3,4]. However, these photodiodes show a worse linear performance than PIN photodiodes, while RoF communication requires a high linearity to minimize the error vector magnitude (EVM).

High linearity is also a requisite of the TIA, which also critically determines the reliability of the receiver. An inherent problem of conventional differential TIA wigh single-ended photodiode input is that the signal swings are pseudo-differential. For an improved linear behavior, the external photodiode is symmetrically biased with a voltage supply depending on the specific photodiode characteristics and desired frequency response, using a bias circuit that consists of a series-connected resistor and inductor to filter out noise [5].

The topology of the TIA can be fully-differential, both inputs are balanced, leading to balanced differential outputs. Furthermore, this bias scheme could be used as a signal strength detector for the implementation of a feed-forward gain control of the TIA by monitoring the anode voltage.

In CMOS technology, open-loop TIA configurations based on the common gate stage, such as the regulated cascode, can offer high bandwidth and low noise, but they show a bad linear behaviour, so they are not very suitable for RoF applications. Closed-loop TIAs show much better linearity and lower noise level, therefore increasing the input dynamic range, while they can also achieve wide bandwidth [6].

In this work, a fully-differential shunt-shunt feedback TIA topology has been chosen, as it shows the best performance for RoF applications. A differential configuration has been used, reducing the effect of supply and substrate noise, and eliminating second order harmonics and intermodulation products, thus improving the overall linearity. The proposed TIA, shown in Fig. 3, improves linearity and bandwidth to meet the stringent requirements of RoF applications.

In this work, the authors propose a TIA based on an open-loop voltage amplifier implemented with three cascaded differential pairs and a negative resistive feedback loop. The transimpedance of the TIA, R_T, can be approximated by:

$$R_T = \frac{(v_{out}^+ - v_{out}^-)}{i_{in}} \approx -\frac{2R_F}{1 + \frac{2R_F C_{in}}{A}s + \frac{2R_F C_{in}}{A\omega_A}s^2} \quad (1)$$

where R_F is the feedback resistor, C_{in} the equivalent input capacitance, mainly determined by the photodiode capacitance, and A and ω_A the open-loop gain and the dominant pole frequency of the voltage amplifier, respectively.

With a linear-in-dB digitally programmable feedback resistor, R_F, the input dynamic range can be extended, by reducing the transimpedance for larger input signals to avoid saturation and maintain a low non-linear distortion. A programmable gain also reduces the impact of PVT variations and allows the use of simpler post-amplifying configurations, such as a limiting amplifier instead of a VGA [7,8]. However, it is well known that, as the transimpedance decreases, the quality factor, Q, increases [9]. This has a significant impact on the system

stability, as it should be kept at low values; otherwise, the system becomes underdamped, high-frequency peaking appears and the system could start to oscillate. From (1), the Q factor can be approximated by:

$$Q \approx \sqrt{\frac{A}{2R_F C_{in} \omega_A}} \quad (2)$$

In order to maintain constant Q against R_F changes, the first two differential pairs have been modified, implementing variable load resistors to accordingly modify the gain, A, of the open-loop voltage amplifier. In this work, 5-bit thermometer-coded resistor arrays, R_F (from 100 Ω to 1 kΩ) and $R_{L1,\ 2}$ (from 200 Ω to 1.2 kΩ), have been implemented to simultaneously control the transimpedance and the open-loop gain, using the same digital word (from $Word_0$ = 00000 to $Word_5$ = 11,111).

3. Results

The proposed TIA has been designed in a 180-nm RF CMOS technology with a single voltage supply of 1.8 V. The parameters of a high-bandwidth InGaAs PIN photodiode have been used to model the PD: responsivity of 0.85 A/W at 1550 nm, a 0.45 pF junction capacitance and a bandwidth of 3 GHz under 50 Ω-load. The parasitic components of the wiring between the PD and the chip have been modeled with a 5 nH inductance and a 100 fF capacitor in each terminal, and the VGA input impedance has been simulated with 200 fF capacitors.

The transimpedance can be programmed from 45 dBΩ up to 65 dBΩ and the 5-bit thermometer-coded resistor array has been adjusted to provide a robust linear-in-dB gain control, with 4-dB steps. The double control of the transimpedance and the open-loop gain guarantees a flat frequency response, independent of the transimpedance. Figs. 4 and 5 show the frequency response and the input-referred noise of the TIA, respectively. At 2.5 GHz, the TIA shows an input-referred current spectral density of 10 pA/$\sqrt{\text{Hz}}$, determining the minimum input optical power.

To perform linearity measurements, we use the demodulation of an 802.11a 54 Mb/s data transmission at 2.4 GHz, which uses multi-carrier OFDM modulated with 64 QAM. Fig. 6 shows the normalized constellation diagram of the demodulated signal, where the signal at the output of the TIA exhibits an EVM of 2% to an input signal of −9 dBm optical power with 20% optical modulation index at the maximum gain configuration of 65 dBΩ.

As it is well known, nonlinearities increase for larger signals, however, making use of the 20-dBΩ transimpedance gain control, the input dynamic range is extended, and input signals as large as +1 dBm optical power can be transmitted with an EVM lower than 2%. This is the lowest EVM compared to the ones reported in [3,4,10], and, more importantly, it is achieved for a wide input dynamic range of 10 dBm optical power, compared to the 3 dBm and 5 dBm ranges reported, respectively, in [3,4].

In Table 1, the main parameters and simulation results for our proposal are summarized and compared to recently published TIAs for RoF applications. To better compare the performance of the proposed TIA with other alternatives, we define the following figure of merit (FoM):

$$FoM = \frac{\text{Transimpedance (Ω)}\cdot\text{BW (GHz)}}{\text{Power Consumption (mW)}} \quad (3)$$

As shown in Table 1, the proposed TIA achieves a much better FoM, thanks to the higher transimpedance and the low power consumption of 26 mW for the maximum gain. It is also the only TIA with controllable transimpedance, extending the input dynamic range for which high linearity is achieved. Another advantage of this design is the compatibility with external PIN photodiodes, which present a much higher junction capacitance, of the order of 0.5 pF, compared to the extremely low 35-fF integrated photodiode presented in [4].

Simulation results obtained by physically extracted models from the layout of the circuit are usually reliable and accurate. However, in order to predict the variability of the circuit behavior due to the manufacturing process, statistical simulations must be performed. Therefore, to complete the characterization of the proposed design, Monte Carlo simulations have been carried out. Results for bandwidth at any transimpedance configuration are shown in Fig. 7. The transimpedance results, shown in Fig. 8 exhibit a worse robustness at low transimpedance configurations, while the standard deviation at high transimpedance configurations is considerably lower, of only 0.5 dBΩ.

4. Conclusion

A low-noise differential TIA for use in a downlink receiver in RAUs for RoF communications has been presented in this work. The TIA performs a 20-dB linear-in-dB range of gain with a 5-bit thermometer-coded resistor array to achieve a wide input dynamic range from −9 dBm up to +1 dBm optical power. The stability is ensured with an open-loop gain of the core amplifier using programmable load resistors, and the TIA overcomes the high intrinsic capacitance of an external PIN photodiode, achieving a 2.5-GHz bandwidth with a maximum transimpedance of 65 dBΩ. Designed in a 180-nm RF CMOS technology with a 1.8-V voltage supply consuming only 26 mW, the proposed TIA exhibits a very high linearity, achieving a better EVM than recently published works, improving the overall performance of the RAU, which makes it a reliable candidate to be used in robust, cost-effective distributed antenna systems using RoF.

Acknowledgements

This work has been partially supported by MINECO-FEDER (TEC2014-52840-R and TEC2017-85867-R) and MINECO fellowship program to G. Royo (BES-2015-073748).

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Article

Programmable Low-Power Low-Noise Capacitance to Voltage Converter for MEMS Accelerometers

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Academic Editors: Mustafa Yavuz and Stefano Mariani

Received: 30 November 2016; Accepted: 23 December 2016; Published: 30 December 2016

Abstract: In this work, we present a capacitance-to-voltage converter (CVC) for capacitive accelerometers based on microelectromechanical systems (MEMS). Based on a fully-differential transimpedance amplifier (TIA), it features a 34-dB transimpedance gain control and over one decade programmable bandwidth, from 75 kHz to 1.2 MHz. The TIA is aimed for low-cost low-power capacitive sensor applications. It has been designed in a standard 0.18-µm CMOS technology and its power consumption is only 54 µW. At the maximum transimpedance configuration, the TIA shows an equivalent input noise of 42 fA/$\sqrt{\text{Hz}}$ at 50 kHz, which corresponds to 100 µg/$\sqrt{\text{Hz}}$.

Keywords: accelerometer; capacitive sensing; microelectromechanical systems (MEMS); synchronous demodulation; transimpedance amplifier

1. Introduction

Capacitive sensors based on microelectromechanical systems (MEMS) are one of the most used accelerometers, since they offer high sensitivity, low power consumption and an excellent noise performance. They are also inexpensive and can be used in a wide range of applications, from the automotive industry, e.g., on assisted stabilization systems, to videogames and consumer electronics, such as smartphones or tablets [1–3].

The basic operational principle of capacitive accelerometers consists of a proof mass and fixed electrodes with a small gap between them, effectively creating a capacitor, with a capacitance, C_0, ranging from 100 fF, up to a few pF. The acceleration causes the displacement of the proof mass, changing the gap distance. Therefore, a variation on the capacitance between the proof mass and the fixed electrodes is generated, and the acceleration is then measured from the capacitance variations. However, measuring these capacitances requires a high-sensitivity, highly-linear sensor interface, as their variations, ΔC, tend to be extremely small, usually less than 1 fF. Moreover, the parasitic effects are of great importance, since they can be as large as the sensor capacitance, which greatly affects the sensitivity of the measurement. MEMS accelerometers feature very low noise, with values at about 20 µg/$\sqrt{\text{Hz}}$ for bulk micromachined accelerometers and about 300 µg/$\sqrt{\text{Hz}}$ for surface micromachined capacitive structures, which can be fabricated at a significantly lower cost [4–7]. Nevertheless, in either case, in order to take advantage of the extremely low thermal noise of the MEMS accelerometers, an ultra-low noise sensor interface is needed.

Several techniques can help reduce the impact of the parasitic capacitances. For example, the bootstrapping one, where the current flow through the parasitic capacitors is virtually eliminated by ensuring that there is no voltage difference over them [1]. However, a highly accurate unity

gain amplifier and a guard electrode surrounding the measurement electrode are needed. In many cases, manufacturing such guard electrodes is very difficult or even impossible. A good alternative to bootstrapping is the use of a transimpedance amplifier with a very low input impedance. The transimpedance amplifier (TIA) measures the current through the capacitor and practically eliminates the voltage variations at the input node, thus minimizing the effect of the parasitic capacitances without needing any guard electrode. Open loop TIAs based on the common gate or the regulated cascode input stage can show a very low input impedance, which makes them suitable for high speed applications [8–10]. However, closed loop TIAs can achieve a much higher transimpedance and perform a better performance in terms of input noise, being more suitable for low-noise sensor applications [11,12].

This work focuses on the design of the capacitance to voltage converter to improve its noise performance and to provide frequency response adaptability. The capacitance-to-voltage converter (CVC) is based on a transimpedance amplifier which features programmable gain and bandwidth, so that it can be adapted to different capacitive accelerometers.

The paper is organized as follows: Section 2 provides a general description of the proposed CVC and the blocks that it consists of, as well as the techniques that have been employed to perform the acceleration measurement. It also introduces the topology selected for the design of the TIA and the implementation of a programmability of the gain and bandwidth. Finally, Section 3 presents the results of this work and Section 4 provides the main conclusions.

2. Capacitance to Voltage Converter

Figure 1 shows a simplified electrical model of a MEMS capacitive sensor. Measuring the current flow through the sensor is needed to measure the capacitance between the proof mass and the fixed electrodes. The current flow through a capacitor, i, is given by:

$$i = C\frac{\partial V}{\partial t} + V\frac{\partial C}{\partial t} \tag{1}$$

where C is the capacitance and V the voltage over the capacitor. The first term is the displacement measurement and the second one is known as the rate-of-change measurement.

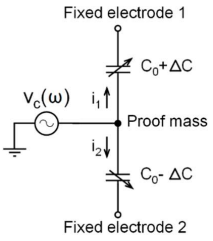

Figure 1. Electrical model of a capacitive accelerometer based on a microelectromechanical system (MEMS).

Typically, only one of these terms is measured, as it is usually much larger than the other one, depending on the application. The rate-of-change measurement is rarely used for measuring acceleration, as it is only measurable at higher frequencies. However, it can be used for other applications, such as resonators, that operate at higher frequencies. In [13] a capacitive readout interface for gravimetric chemical gas sensors based on a MEMS resonator is presented. This measurement mode can also be used to design oscillators, as in [14], where a 100-MHz oscillator based on a MEMS resonator is presented.

For acceleration measurement applications, the displacement measurement is employed, as the frequency range of the acceleration usually covers the range from 0 to a few hundreds of Hz, which coincides with the typical linear range of the mechanical response of a MEMS (Figure 2). This response depends on the physical parameters of the MEMS: proof mass, spring constant, damping factor,

size, etc. [5,15–17]. Different MEMS will have a completely different mechanical response in terms of sensitivity, linear region or resonant frequency. Therefore, a sensor interface with a programmable response, adaptive to the mechanical MEMS response enhances the quality of the measurement, optimizing noise performance and sensitivity.

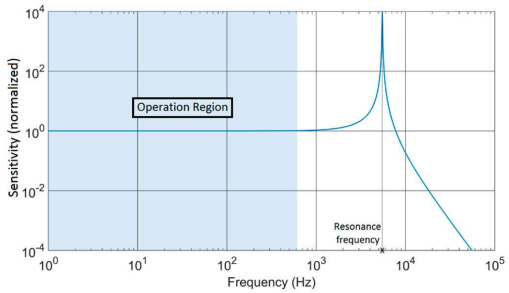

Figure 2. Mechanical frequency response of a capacitive MEMS accelerometer.

Measuring the displacement of the proof mass, that is, the first term in Equation (1), requires a high frequency measurement signal, $v_c = a \cdot \sin(\omega_c t)$, for several reasons. Firstly, for higher frequencies, the current flow through the capacitive sensor will be higher, thus increasing the overall sensitivity. Secondly, this frequency cannot be close to the mechanical resonance frequency of the MEMS, since it could begin to oscillate. Finally, if this signal frequency is much higher than the frequency of the capacitive variations, the second term in Equation (1) can be neglected.

Figure 3 shows the overall scheme of the open loop synchronous demodulator. The measurement signal, v_c, acts as a carrier signal, while the capacitance of the sensor modulates the amplitude of the current flowing through the capacitor. However, as the capacitance variations tend to be extremely small, of the order of fF, the current flowing through the sensor is as well very small, of the order of few pA. Therefore, to obtain a measurable signal, a high-gain low-noise transimpedance amplifier is required. The TIA must feature low noise and low input impedance. With a low input impedance the TIA keeps the input nodes V_1 and V_2 at the ground potential, improving the effect of the bootstrapping technique, as the TIA practically eliminates the effect of the parasitic capacitances by suppressing the voltage variations at the input nodes. In this work, the CVC has been proposed to be used in an open loop synchronous demodulator for capacitive sensor interfaces, however, it could be used in closed loop counterparts based on the force-feedback technique. In this way, more precision can be achieved if a suitable controller is included to steer an actuation mechanism that forces the proof mass back to its rest position.

To demodulate the high frequency measurement signal and transfer it back to the baseband, a double-balanced Gilbert cell has been employed. The Gilbert cell shows high conversion gain, high linearity, and achieves good port-to-port isolation with wide bandwidth and low power consumption. In the last stage, the high frequency components are filtered, employing a low-pass filter that isolates the baseband, to properly measure the capacitance variations.

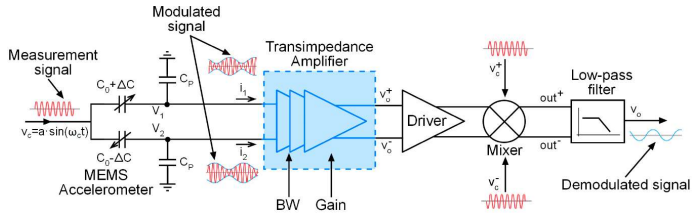

Figure 3. Conceptual scheme of the open loop synchronous demodulator.

Transimpedance Amplifier Design

In this work a differential shunt-shunt feedback topology, shown in Figure 4, has been chosen to implement the TIA. It consists of a high-gain voltage amplifier with a negative feedback loop and it can achieve a high transimpedance, low input impedance, and low equivalent input noise (EIN). Using Equation (1) we obtain that the TIA amplifies the current and provides a measurable voltage signal, proportional to the capacitance variation:

$$i_{1,2} \simeq (C_0 \pm \Delta C)\frac{\partial v_C}{\partial t} \tag{2}$$

$$\begin{aligned} v_o^+ - v_o^- &= R_T \cdot (i_1 - i_2) \\ v_o^+ - v_o^- &= 2\Delta C \cdot R_T \frac{\partial v_c}{\partial t} \end{aligned} \tag{3}$$

where R_T is the transimpedance of the TIA.

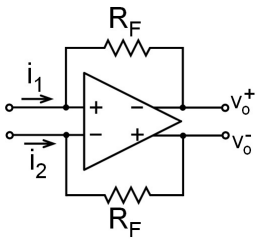

Figure 4. Differential shunt-shunt feedback transimpedance amplifier.

The amplitude of the signal $v_o^+ - v_o^-$ carries the information of the measured acceleration. In order to maximize the sensitivity, the TIA must show high transimpedance, but also a bandwidth wide enough to contain the frequency of the carrier, so that the signal will not suffer attenuation. Nevertheless, as the bandwidth increases, more noise is integrated, thus reducing the signal-to-noise ratio (SNR). This tradeoff indicates that there is an optimum bandwidth, for which the sensitivity and SNR are optimized. This bandwidth is conditioned by the measurement signal frequency. Moreover, since this frequency is chosen depending on the MEMS resonance frequency, the optimum bandwidth will be a function of the mechanical MEMS response. In this work, we propose a TIA with programmable gain and bandwidth to optimize the sensitivity and the SNR for a wide range of mechanical MEMS responses.

As has been mentioned above, the parasitic capacitive effects must be compensated to maximize the sensitivity of the measurement. For this reason a transimpedance amplifier that suppresses the voltage variations at the input nodes is used, so that, ideally, there is no current flow through the parasitic capacitors. Therefore, all of the current through the sensor can be measured. The shunt-shunt feedback topology is the most used TIA configuration, as it achieves better linearity than common-gate based configurations, which also tend to be noisier. The proposed shunt-shunt feedback TIA consists of a fully differential voltage amplifier and a negative resistive loop. In a second-order approximation, where the differential voltage amplifier presents a DC gain, A_d, and a dominant pole frequency, ω_A, the transfer function of the feedback TIA is given by:

$$R_T = -\frac{2R_F}{1 + \frac{2R_F C_{in}}{A_d}s + \frac{2R_F C_{in}}{A_d \omega_A}s^2} \tag{4}$$

where C_{in} is the total input capacitance. To better describe the behavior of this second-order response, we study the quality factor, Q, which from Equation (4), can be calculated as:

$$Q = \sqrt{\frac{A_d}{2R_F C_{in} \omega_A}} \tag{5}$$

According to Equation (4), the DC transimpedance is determined by R_F. With variable feedback resistors, the transimpedance can be programmed to optimize the sensitivity and SNR of the CVC. Nevertheless, the quality factor must also be considered when implementing a transimpedance gain control, as Q depends on the feedback resistance, and its value is restricted to certain values to maintain stability. It is well known that if $Q > 1/\sqrt{2}$ there will be peaking in the frequency response, thus increasing the distortion of the signal and, more critically, the system could start to oscillate. Therefore, in order to maintain $Q < 1/\sqrt{2}$, the open loop differential voltage gain, A_d, and the feedback resistor, R_F, have to be simultaneously controlled [18,19]. The proposed TIA, shown in Figure 5, performs the simultaneous control of both the feedback resistance and the open loop voltage gain. The transimpedance control has been implemented with a variable feedback resistor which consists of an array of four resistors connected in parallel, and programmable with a three-bit thermometer code, $b_{F,i}$ (Figure 6a).

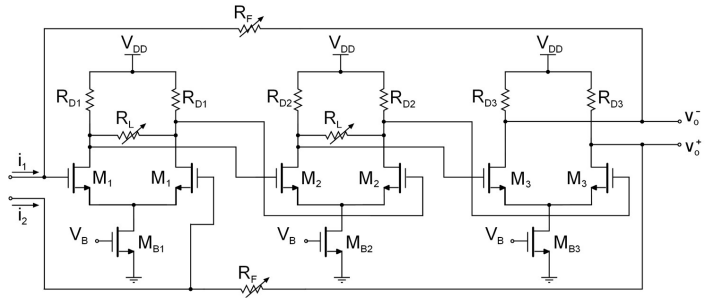

Figure 5. Simplified schematic circuit of the proposed transimpedance amplifier.

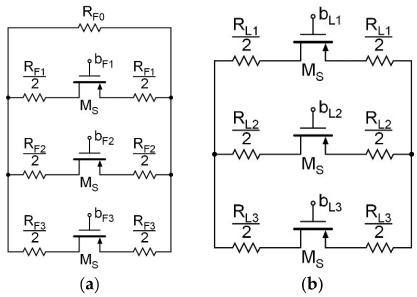

Figure 6. Implementation of (**a**) the feedback resistors, R_F, and (**b**) the load resistors, R_L.

In order to implement the variable open loop gain, a voltage amplifier that allows an open loop gain control has been designed. It consists of three cascaded differential pairs with variable load resistors added to the first two pairs. The voltage gain, A_p of a differential pair can be written as:

$$A_p = g_m \left(R_D \parallel \frac{R_L}{2} \right) \tag{6}$$

where g_m is the pair transonductance, and R_D and R_L the drain and load resistors, respectively. PMOS (p-type metal-oxide-semiconductor) transistors are commonly used to implement the drain resistors, as they require smaller area and can be externally controlled. However, active PMOS loads need a common mode feedback (CMFB) loop to stabilize the voltage at the output of the differential pair,

thus demanding a higher power consumption, and triode PMOS loads exhibit a poor linear behavior, which highly degrades the overall linearity. In this work, inspired by high-frequency amplifiers, where CMFB loops are hard to implement due to stability issues, high-resistivity polysilicon resistors have been employed to achieve better linearity and lower power consumption.

In a similar way to the transimpedance gain control, the load resistors have been implemented using an array of three resistors in parallel, programmable with a three-bit thermometer code, $b_{L,i}$ (Figure 6b), providing full programmability to the TIA, without modifying the common mode output voltage, as there is no DC current flow through these resistors. The component values and the aspect ratio of the transistors are shown in Table 1.

Table 1. Component values and transistor aspect ratios for the proposed transimpedance amplifier.

$M_1\left(\frac{W}{L}\right)$	$M_2\left(\frac{W}{L}\right)$	$M_3\left(\frac{W}{L}\right)$	$M_{B1-3}\left(\frac{W}{L}\right)$	$M_S\left(\frac{W}{L}\right)$	R_{D1-3}	V_B
20 µm/1 µm	20 µm/0.5 µm	10 µm/1 µm	10.5 µm/4 µm	20 µm/0.18 µm	180 kΩ	600 mV
R_{F0}	R_{F1}	R_{F2}	R_{F3}	R_{L1}	R_{L2}	R_{L3}
5 MΩ	1.1 MΩ	380 kΩ	100 kΩ	33 kΩ	48 kΩ	45 kΩ

3. Discussion

The transimpedance amplifier has been designed in a standard 0.18-µm CMOS technology with a single 1.8-V voltage supply. For this work, we have used the model of a surface-micromachined comb-finger structure of 2-µm gap and resonance frequency of 5.5 kHz, with a nominal capacitance C_0 of 1 pF with parasitic capacitances C_P of 2 pF. With this model of the MEMS accelerometer, the sensitivity provided by the sensor can be obtained from the following expression:

$$S_T = \frac{\Delta C}{\Delta \ddot{x}} = \frac{\Delta x}{\Delta \ddot{x}} \cdot \frac{\Delta C}{\Delta x} \tag{7}$$

with x being the displacement of the proof mass. Considering a linear behavior, and at low frequency operation, it can be approximated by [20]:

$$S_T = \frac{1}{\omega_r^2} \cdot \frac{C_0}{x_0} \tag{8}$$

with x_0 being the gap distance and ω_r the resonance frequency. From Equation (8) we obtain a sensitivity of 4.2 fF/g. The measurement frequency, ω_c, is chosen to be of 50 kHz, so that it is roughly one order of magnitude greater than the resonance frequency.

As shown in Figure 7, the proposed TIA performs a 34-dBΩ transimpedance control range, while maintaining an almost constant bandwidth of around 1.2 MHz. To achieve this gain range keeping a flat frequency response, a simultaneous control of the feedback and load resistors has been made. Moreover, Figure 8 shows that with a single control of the open loop gain of the voltage amplifier, the transimpedance can be fixed at its maximum value, but the bandwidth can be tuned over more than a decade, from 75 kHz to 1.2 MHz.

With a power consumption of only 54 µW, the TIA achieves a maximum sensitivity of 1 mV/fF, which corresponds to a capacitive sensitivity of 4.2 mV/g and presents a low equivalent input noise of only 42 fA/$\sqrt{\text{Hz}}$, at the maximum transimpedance configuration of 10 MΩ and 73-dB open loop gain (Figure 9, $b_F = b_L = 111$), or equivalently 100 µg/$\sqrt{\text{Hz}}$ at 50 kHz. Table 2 summarizes the main results and compares with recent published capacitance to voltage converters [17,21–23]. These CVCs are based on current measuring with a sensor interface based on a TIA, excepting [17], where a folded cascade operational amplifier is used configured as voltage amplifier, along with a diode-connected sub-threshold NMOS transistor to bias the input nodes. It also requires post-amplifying stages to increase sensitivity, including a variable gain amplifier to achieve a 12-dB gain control, which makes it a power-hungry circuit. A capacitive TIA is presented in [21], showing a 56-MΩ transimpedance

and a 1.8-MHz bandwidth, which features no gain control and exhibits a higher noise level than that reported in this work. Structures reported in [22,23] are both based on resistive TIAs, providing transimpedance gains up to 25 MΩ in [22] and 22 MΩ in [23]. Both perform a transimpedance gain control and implement the feedback resistor using a T-network pattern, which reduces the overall size of the resistor, but can significantly increase noise. Moreover, the bandwidth in [22] decreases with the transimpedance, while an orthogonal gain and bandwidth control is achieved in the TIA proposed in this work. This full programmability of gain and bandwidth provides a much better adaptability of the frequency response to the mechanical frequency response of different MEMS.

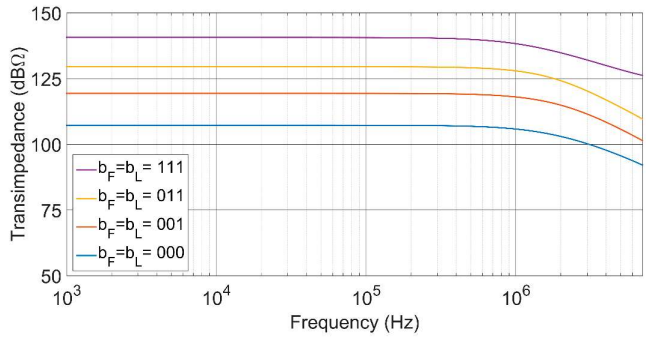

Figure 7. Frequency response showing the transimpedance gain programmability with a double control of the feedback resistor and the open loop gain. The bandwidth is almost constant at 1.2 MHz.

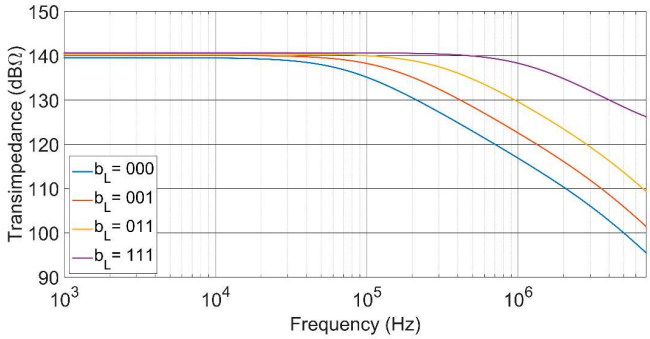

Figure 8. Frequency response with a single control of the open loop gain. The transimpedance gain is almost constant, at 140 dBΩ with feedback control word, b_F = 111.

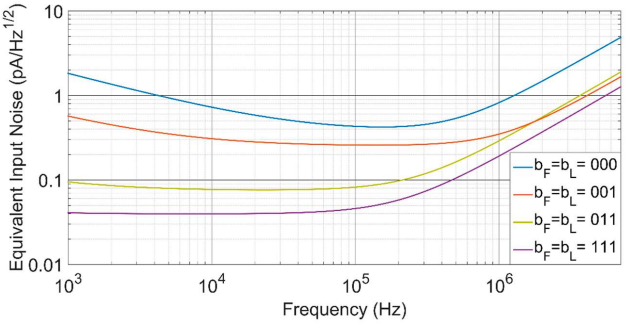

Figure 9. Equivalent input noise figure for the four gain configurations with 1.2 MHz bandwidth.

Table 2. Summary of the performance and comparison with recently published works.

	[17] [1]	[21] [2]	[22] [1]	[23] [2]	**This Work** [2]
Technology	0.35 µm CMOS	0.18 µm CMOS	0.6 µm CMOS	0.35 µm CMOS	0.18 µm CMOS
Supply Voltage	3.3 V	1.8 V	3 V	5 V	1.8 V
Minimum Input Noise	54 µg/$\sqrt{\text{Hz}}$	65 fA/$\sqrt{\text{Hz}}$	88 fA/$\sqrt{\text{Hz}}$	63 fA/$\sqrt{\text{Hz}}$ *	42 fA/$\sqrt{\text{Hz}}$
Capacitive Sensitivity	1450 mV/fF* (18 mV/fF without PA)	-	25 mV/fF *	3.3 mV/fF	1 mV/fF
Power Consumption	5.1 mW	436 µW	400 µW	-	54 µW
Type of Sensing Interface	Voltage Amplifier	Capacitive TIA	Resistive TIA	Resistive TIA	Resistive TIA
Gain	−9 to +2 dB	56 MΩ	1.6–25 MΩ	2–22 MΩ	0.15–10 MΩ
Bandwidth	8.6 MHz	1.8 MHz	200 kHz *	200 kHz *	75 kHz–1.2 MHz
Application	Accelerometer	Resonator/Oscillator	Gyroscope	Gyroscope	Accelerometer

[1] Experimental results; [2] Simulation results; * Calculated from paper.

Furthermore, Monte Carlo simulations have also been carried out for process variations and mismatch. The Monte Carlo analysis shows a statistical distribution of the chip performance before fabrication, which is of great importance, since the technological parameters can experience strong variations that may considerably deteriorate the overall performance. Figures 10 and 11 present the Monte Carlo histograms for the transimpedance and bandwidth of the TIA, both of them obtained for the maximum gain configuration. The results obtained confirm the robustness of the design against process variations, with standard deviations of about 5% of the nominal value.

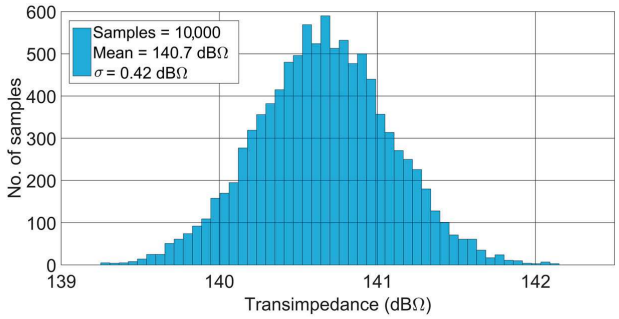

Figure 10. Monte Carlo simulation results for transimpedance gain for the maximum transimpedance configuration, 140 dBΩ, showing a standard deviation, σ, of 0.42 dBΩ.

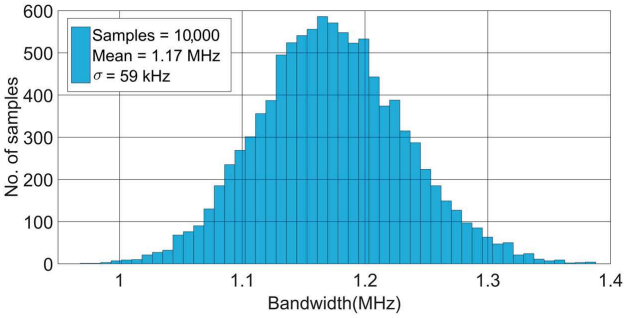

Figure 11. Monte Carlo simulation results for bandwidth for the maximum transimpedance configuration, 140 dBΩ.

4. Conclusions

In this work, a capacitance-to-voltage converter for MEMS accelerometers has been presented. It is based on a new concept of a fully-differential transimpedance amplifier and achieves a 34-dB programmable gain range and over one decade programmable bandwidth. It has been designed in a standard 0.18-μm CMOS technology, and it is aimed for a differential surface-micromachined comb-finger capacitive accelerometer. The TIA achieves an equivalent input noise of 42 $fA/\sqrt{Hz}$ (100 $\mu g/\sqrt{Hz}$) at 50 kHz at the maximum transimpedance configuration. Its programmability allows its use in a wide range of capacitive MEMS devices, adapting the frequency response to the mechanical MEMS response. The presented TIA is compatible with low-power applications, with a power consumption of only 54 μW, and is robust against process variations, with a 5% standard deviation in gain and bandwidth.

Acknowledgments: This work has been partially supported by the Spanish Economy and Competitiveness Ministry under grants from the European Regional Development Fund (MINECO-FEDER) (TEC2014-52840-R) and MINECO fellowship program to G. Royo (BES-2015-073748).

Author Contributions: Guillermo Royo, Concepción Aldea and Santiago Celma contributed to the design of the proposed topology; Guillermo Royo performed the simulations and the complete characterization of the system; all authors contributed to the data analysis and the writing of the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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APPENDIX B
Impact Factors of the Journals and Subject Areas of the Presented Papers

In the following list, the impact factors of the journals in which each of the works were presented are listed.

Publication	Impact Factor	Subject Area
Royo, G.; Sánchez-Azqueta, C.; Aldea, C.; Celma, S. High-sensitivity large-area photodiode read-out using a divide-and-conquer technique. *Sensors*, 2020, 20(21), 6316. doi: 10.3390/s20216316	3.275 (Q1)*	Instruments & Instrumentation
Royo, G.; Martínez-Pérez, A.D.; Sánchez-Azqueta, C.; Aldea, C.; Celma, S. A highly linear low-noise transimpedance amplifier for indoor fiber-wireless remote antenna units. *Electronics*, 2019, 8(4) 437. doi:10.3390/electronics8040437	2.412 (Q2)	Engineering, Electrical & Electronic
Royo, G.; Sánchez-Azqueta, C.; Martínez-Pérez, A.D.; Aldea, C.; Celma, S. Fully-differential transimpedance amplifier for reliable wireless communications. *Microelectronics Reliability*, 2018, 83, 25-28. doi: 10.1016/j.microrel.2018.02.007	1.483 (Q3)	Engineering, Electrical & Electronic
Royo, G.; Sánchez-Azqueta, C.; Gimeno, C.; Aldea, C.; Celma, S. Programmable low-power low-noise capacitance to voltage converter for MEMS accelerometers. *Sensors*, 2017, 17(1), 67. doi: 10.3390/s17010067	2.475 (Q2)	Instruments & Instrumentation

*Data from 2020 is not available, therefore data from the last available year (2019) is presented.

APPENDIX C
Publication List

Publications in Journals

[ROY20a] Royo, G.; Sánchez-Azqueta, C.; Aldea, C.; Celma, S. High-Sensitivity Large-Area Photodiode Read-Out Using a Divide-and-Conquer Technique. *Sensors*, 2020, 20(21), 6316.
doi: 10.3390/s20216316

[ROY19a] Royo, G.; Sánchez-Azqueta, C.; Martínez-Pérez, A.D.; Aldea, C.; Celma, S. A highly linear low-noise transimpedance amplifier for indoor fiber-wireless remote antenna units. *Electronics*, 2019, 8(4) 437.
doi:10.3390/electronics8040437

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doi: 10.3390/s17010067

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doi 10.1002/cta.2505

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doi: 10.3390/electronics9111785

Publications in International Conferences

[GAR17] García-Bosque, M.; Pérez, A.; Sánchez-Azqueta, C.; Royo, G.; Celma, S. MEMS-based seed generator applied to a chaotic stream cipher. In Smart Sensors, Actuators, and MEMS VIII. International Society for Optics and Photonics, 2017, 1024618.

[GAR16] García-Bosque, M.; Sánchez-Azqueta, C.; Royo, G.; Celma, S. Lightweight ciphers based on chaotic map-LFSR architectures. In 2016 12th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME), 2016.

[GIM15b] Gimeno, C.; Guerrero, E.; Sánchez-Azqueta, C.; Royo, G.; Aldea, C.; Celma, S. 1-V continuous-time linear equalizer for up to 2 Gb/s over 50-m SI-POF. In 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, 1818-1821.

[GIM15c] Gimeno, C.; Guerrero, E.; Sánchez-Azqueta, C.; Royo, G.; Aldea, C.; Celma, S. A new equalizer for 2 Gb/s short-reach SI-POF links. In Integrated Photonics: Materials, Devices, and Applications III. International Society for Optics and Photonics, 2015, 95200U.

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[ROY17c] Royo, G.; García-Bosque, M.; Sánchez-Azqueta, C.; Aldea, C.; Celma, S.; Gimeno, C. Transimpedance amplifier with programmable gain and bandwidth for capacitive MEMS accelerometers. In 2017 IEEE International Instrumentation and Measurement Technology Conference (I2MTC), 2017.

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Publications in National Conferences

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