TESIS DE LA UNIVERSIDAD DE ZARAGOZA

2022 79

Jorge Pérez Bailón

CMOS Design of Reconfigurable SoC Systems for Impedance Sensor Devices

Director/es
Calvo López, Belén Teresa
Medrano Marqués, Nicolás Jesús

http://zaguan.unizar.es/collection/Tesis

ISSN 2254-7606

Prensas de la Universidad
Universidad Zaragoza

© Universidad de Zaragoza
Servicio de Publicaciones

ISSN 2254-7606

Universidad Zaragoza
1542

Tesis Doctoral

CMOS DESIGN OF RECONFIGURABLE SOC SYSTEMS FOR IMPEDANCE SENSOR DEVICES

Autor

Jorge Pérez Bailón

Director/es

Calvo López, Belén Teresa
Medrano Marqués, Nicolás Jesús

UNIVERSIDAD DE ZARAGOZA
Escuela de Doctorado

Programa de Doctorado en Física

2022

Repositorio de la Universidad de Zaragoza – Zaguan http://zaguan.unizar.es

CMOS Design of Reconfigurable SoC Systems for Impedance Sensor Devices

A thesis submitted to the University of Zaragoza
in partial fulfilment of the requirements for
the Degree of Doctor of Philosophy in Physics

By

Jorge Pérez Bailón

Thesis Supervisors

Dr. Belén Calvo López
Dr. Nicolás Medrano Marqués

Electronic Design Group (GDE-I3A)
Department of Electronic Engineering and Communications
Faculty of Sciences – University of Zaragoza

Universidad Zaragoza

In Zaragoza, january 22, 2022

Diseño CMOS de Sistemas SoC Reconfigurables Para Dispositivos Sensores de Impedancia

Tesis presentada a la Universidad de Zaragoza
para optar al grado de Doctor

por

Jorge Pérez Bailón

Bajo la dirección de

Dra. Belén Calvo López
Dr. Nicolás Medrano Marqués

Grupo de Diseño Electrónico (GDE-I3A)
Departamento de Ingeniería Electrónica y Comunicaciones
Facultad de Ciencias – Universidad de Zaragoza

Universidad Zaragoza

En Zaragoza, a 22 de enero de 2022

A mis abuelos

Alicia, Gene, Jesús y Pedro

¿Qué es la vida? Un frenesí
¿Qué es la vida? Una ilusión,
una sombra, una ficción,
y el mayor bien es pequeño;
que toda la vida es sueño,
y los sueños, sueños son.

La vida es sueño.
Calderón de la Barca.

Abstract

The fast evolution from basic to intelligent electronic sensors, together with the progress made in computation and communication technologies, is creating a revolution in how we gather and analyse data from the physical world in order to take decisions, facilitating new solutions and accomplishing tasks that were previously thought to be impossible to achieve.

The inclusion in the same silicon die of all the elements required for a monitoring and actuation process has been possible thanks to the advances in micro (and nano) electronics. At the same time, the improvement in the processing technologies and surface micromachining of silicon and other complementary materials has given rise to the development of advanced CMOS-compatible integrated sensors on silicon chips, allowing for high-density sensor arrays supporting large parallelization processes. Moreover, the combination of a System on Chip sensor-processing package, together with a microprocessor as digital core, where signal digitization, data processing and data communication can be executed, provides additional features as reduced cost and compactness, portability, battery power, ease of use and intelligent data sharing, increasing the potential number of applications.

This thesis intends to deepen in the design of a truly portable battery-operated low-power wide frequency impedance spectroscopy measurement system, based on CMOS microelectronic technologies, so that it can be embedded in the sensor package, providing a parallelizable implementation at no significant cost of size or power consumption, but keeping the main reliability and sensibility characteristics of a laboratory instrument. This requires the development of the different cells conforming the IS interface, featuring high performance while satisfying the demanding minimum size and low-power consumption constraints required in portable characterization and monitoring, characteristics that become even more critical when sensors array are considered, making also necessary the design of a suitable power management stage.

At the cell level, different circuits are proposed in a 180 nm CMOS process: A low-dropout voltage regulator as the core of the power management unit providing a stable, low-noise, accurate and load-independent 1.8 V power supply voltage for the whole IS system; Instrumentation Amplifiers with a fully differential approach, including a configurable voltage/current input stage, programmable gain and adjustable bandwidth, both at the low and high cutoff frequencies; A multiplyier to conform the dual synchronous demodulation, which is embedded in the amplifier saving power and area; and fully integrated Low Pass Filters, acting as DC magnitude extractors, with tunable cutoff frequencies from sub-Hz to hundreds of Hz.

.

Resumen

La rápida evolución de los sensores electrónicos, junto con los avances en las tecnologías de la computación y la comunicación, está revolucionando la forma en que recopilamos y analizamos datos del mundo físico para tomar decisiones, facilitando nuevas soluciones y cumplir tareas que antes eran inconcebibles de lograr.

La inclusión en un mismo dado de silicio de todos los elementos necesarios para un proceso de monitorización y actuación ha sido posible gracias a los avances en micro (y nano) electrónica. Al mismo tiempo, la mejora en las tecnologías de procesamiento y micromecanizado de superficies de silicio y otros materiales complementarios ha dado lugar al desarrollo de sensores integrados avanzados compatibles con CMOS en chips de silicio, lo que permite matrices de sensores de alta densidad que admiten grandes procesos de paralelización. Además, la combinación de un sistema de procesamiento de sensores on-Chip, junto con un microprocesador programable como núcleo digital, donde se puede ejecutar la digitalización de señales, el procesamiento y la comunicación de datos, proporciona características adicionales como reducción del coste, compacticidad, portabilidad, alimentación por batería, facilidad de uso e intercambio inteligente de datos, aumentando el potencial número de aplicaciones.

Esta tesis pretende profundizar en el diseño de un sistema portátil de medición de espectroscopía de impedancia de baja potencia operado por batería, basado en tecnologías microelectrónicas CMOS, que pueda integrarse con el sensor, proporcionando una implementación paralelizable sin incrementar significativamente el tamaño o el consumo, pero manteniendo las principales características de fiabilidad y sensibilidad de un instrumento de laboratorio. Esto requiere el desarrollo de las diferentes celdas que conforman la interfaz IS, logrando un alto rendimiento a la par que satisfaciendo las exigentes restricciones de tamaño mínimo y bajo consumo requeridas en la caracterización y monitorización portátil, características que son aún más críticas al considerar cadenas de sensores, lo que también hace necesario el diseño de una etapa de gestión de la alimentación adecuada.

A nivel de celdas, se proponen diferentes circuitos en un proceso CMOS de 180 nm: un regulador de baja caída de voltaje como unidad de gestión de energía que proporciona una alimentación de 1.8 V estable, de bajo ruido, precisa e independiente de la carga para todo el sistema IS; amplificadores de instrumentación con una aproximación completamente diferencial, que incluyen una etapa de entrada de voltaje/corriente configurable, ganancia programable y ancho de banda ajustable, tanto en las frecuencias de corte bajas como altas; un multiplicador para conformar la demodulación síncrona dual, que está integrado en el amplificador ahorrando energía y área; y filtros pasa baja totalmente integrados, que actúan como extractores de magnitude de DC, con frecuencias de corte ajustables desde sub-Hz hasta cientos de Hz.

Agradecimientos

Me gustaría empezar dando las gracias a Belén y Nicolás, mis directores de tesis, siempre con la puerta abierta para comentar cualquier cosa. Sin su dirección y supervisión durante todos estos años esta tesis no habría sido posible.

Agradecer también a todos los miembros del tribunal, revisores externos y todas aquellas personas que han participado durante la elaboración y defensa de estas tesis.

A todos los que durante este periodo han formado parte del GDE, que de un modo u otro me han ayudado con su conocimiento, opinión o su conversación. En particular me gustaría agradecer a Alejandro con el que inicié esta odisea, a Pedro que siempre dispuesto me ha sacado de más de un apuro tratando de entender el porqué de los resultados y a Óscar por su ayuda diaria y su optimismo.

No quiero olvidarme de mis supervisores durante mis estancias. Jaime Ramírez-Angulo durante la estancia en *New Mexico State University* (New Mexico, Estados Unidos) y de todos sus estudiantes que estuvieron siempre disponibles y me acogieron como a uno más; y María Teresa Sanz-Pascual durante la estancia en el *Instituto Nacional de Astrofísica, Óptica y Electrónica* (Puebla, México), por sus consejos e indicaciones y por permitir adaptar la estancia a la situación de pandemia en la que nos vimos inmersos.

Mi familia y por extensión mis amigos se merecen un agradecimiento aparte. A mis abuelos, a mis tíos, a mis padres Jesús y Encarna, a mi hermano Ignacio y a Silvia, gracias. Ellos han estado allí desde el primer día, apoyándome y aguantándome durante lo bueno y lo malo. A mis amigos de Jaca, del Liceo y a los Tarzanes, que se han encargado de recordarme que hay otra vida además del doctorado y han aguantado estoicamente mis largos monólogos sobre mi trabajo.

A Jose Ángel Guedea y Carlos García, mis maestros de Judo y de mucho más, me gustaría agradecerles especialmente todo lo que me han aportado en esas breves horas a la semana que nos vemos. Todo lo que me han transmitido a través del Judo es algo que no puedo poner en palabras y que seguramente muchos no entiendan, pero desde luego es parte esencial de que esta tesis haya llegado hasta aquí. Es por ello que quiero hacer extensible este agradecimiento, al Club de Judo Las Fuentes, a los matutinos y a todos aquellos con los que alguna vez he compartido un randori, un uchi-komi o simplemente, un tatami.

Tengo que dar gracias a Sara, compañera en este viaje y verdadera sufridora de todo este proceso, que ha aguantado todo conmigo siempre con una sonrisa. Siempre dispuesta a dar un paseo, a planear un viaje o un fin de semana cuando yo estaba demasiado inmerso en la tesis como para pensar en otra cosa.

Gracias a Bowie, es quien consigue que me levante de la cama, siempre me recibe con una sonrisa llena de felicidad, gracias a él salgo a pasear todos los días, y nunca tiene una palabra mala o una queja.

Gracias también a todos aquellos que no he nombrado, compañeros de trabajo, investigadores que han realizado estancias y con los que he coincidido, toda la gente que he conocido durante las estancias y congresos que han ampliado mis horizontes y a ti que estás leyendo esta tesis.

Por último, agradezco a todas las instituciones que han hecho posible este trabajo mediante la financiación de los diversos proyectos en los que he participado y contratos de investigación que he recibido:

- Ministerio de Economía y Competitividad (TEC2015-65750-R)
- Universidad de Zaragoza (UZ2019-TEC-08)
- Agencia Estatal de Investigación (PID2019-106570RB-I00)
- Gobierno de Aragón (subvención para la contratación de personal investigador predoctoral en formación)

Table of contents

List of Figures

List of Tables

Acronyms

AC	Alternate Current
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
AWG	Arbitrary Waveform Generator
BD	Bulk Driven
BW	Bandwidth
CBBC	Current Boosting Bias Circuit
CC	Current Cancellation
CD	Current Division
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common Mode Rejection Ratio
COTS	Commercial Off The Shelf
CS	Current Steering
DAQ	Data Acquisition Card
DC	Direct Current
DIL	Dual In-Line
DMM	Digital Multimeter
DNA	Deoxyribonucleic Acid
DR	Dynamic Range
DSP	Digital Signal Processor
DUT	Device Under Test
EA	Error Amplifier
FE	Front End
FFT	Fast Fourier Transform
FoM	Figure of Merit
FRA	Frequency Response Analyzer
FVF	Flipped Voltage Follower
GBW	Gain Bandwidth Product
HPF	High Pass Filter
IC	Integrated Circuit
IS	Impedance Spectroscopy
LDO	Low Dropout
LDR	Load Regulation
LF	Low Frequency
LIA	Lock-In Amplifier
LNA	Low Noise Amplifier
LNR	Line Regulation
LPF	Low Pass Filter
LVLP	Low Voltage Low Power
MEMS	Microelectromechanical System
MIM	Metal-Isolator-Metal

NA	Normalized Area factor
NEF	Noise Efficiency Factor
NMOS	Negative-Channel Metal-Oxide-Semiconductor
NP	Normalized Power factor
O1F	Order-1 Filter
O2F	Order-2 Filter
OS	Overshoot
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PM	Phase Margin
PMOS	Positive-Channel Metal-Oxide-Semiconductor
PMU	Power Management Unit
PSD	Phase Sensitive Detection
PSR	Power Supply Rejection
QFG	Quasi-Floating Gate
RADAR	Radio Detection and Ranging
RF	Radio Frequency
RMS	Root Mean Square
SD	Synchronous Demodulation
SiP	System in Package
SMU	Source Measurement Unit
SNR	Signal-to-Noise Ratio
SoC	System on Chip
TC	Transconductance
THD	Total Harmonic Distortion
TI	Transimpedance
UGF	Unity Gain Frequency
US	Undershoot
VGA	Variable Gain Amplifier
VNA	Vector Network Analyser
VOC	Volatile Organic Compounds

Parameter Glossary

A_{EA}	Errors amplifier gain
A_{fb}	Loop feedback gain
C_c	Cascode compensation capacitance
c_{gd}	Gate-drain capacitance
C_{gs}	gate-source capacitance
C_{Load}	Load capacitor
C_{oa}	OTAs output capacitance
C_{OX}	Gate oxide capacitance per unit area
C_P	Parallel capacitor
C_S	Series capacitor
f_c	cutoff frequency
$f_{c,H}$	Highpass cutoff frequency
$f_{c,L}$	Lowpass cutoff frequency
$f_{c,BW}$	Bandwidth defined as ($f_{c,L}$ - $f_{c,H}$)
f_{in}	input frequency
f_o	excitation signal
G_I	Current gain
g_m	Transconductance of a transistor
g_{mb}	Bulk transconductance
G_V	Voltage gain
I	In-phase signal
I_D, I_{DS}/ I_{SD}	Drain-source/ source-drain current
I_{exc}	excitation signal (current)
I_{fb}	Feedback current
I_{Load}	Load current
I_q	quiescent current
κ_B	Boltzmann's constant
L	Channel length of a MOS transistor
M_P, M_{PASS}	Pass transistor
n	slope in saturation weak inversion
P_{EA}	Error amplifier pole
P_{Load}	Power demanded
P_{OUT}	Output pole
P_{source}	Power supplied
Q	Quadrature signal
R	Resistance
R_{deg}	degeneration resistance

R_{eq}	Equivalent resistance
R_{large}	High resistance
R_{Load}	Load resistor
R_{MOS}	MOS resistance
R_{oa}	OTA output resistance
R_P	Parallel resistance
R_{POLY}	Polysilicon resistance
R_S	Series resistance
T	temperature
t_s	settling time
V_{BAT}	Battery voltage
V_{cm}	common mode voltage
V_{ctrl}	Control voltage
V_{dd}	Positive supply voltage
V_{do}	dropout voltage
V_{ds}	Drain-source voltage
$V_{ds,sat}$ / $V_{sd,sat}$	Saturation voltage
V_{exc}	excitation signal (voltage)
V_{fb}	feedback voltage
V_g	Gate voltage
V_{gc}	control gate voltage
V_{gs}	Gate-source voltage
V_{in}	input voltage
V_{out}	output voltage
V_{ref}	reference voltage
V_{sens}	sensed signal
V_{sq}	Squared signal
V_{ss}	Negative supply voltage
V_T	Thermal voltage
V_{th}	threshold voltage
V_x	DC level of recovered inphase signal
V_y	DC level of recovered quadrature signal
W	Channel width of a MOS transistor
X	Reactance
Z	impedance
η	Efficiency
ω	angular frequency

Chapter 1
Introduction

The fast evolution from basic to intelligent electronic sensors, together with the progress made in computation and communication technologies, is creating a revolution in how we gather and analyse data from the physical world in order to take decisions, facilitating new solutions and accomplishing tasks that were previously thought to be impossible to achieve.

It was in 1980 when Middlehoek and Angell firstly introduced the concept of intelligent electronic sensor as a microelectromechanical system (MEMS) connected to an analog-to-digital converter (ADC) [1]. Even though at this time both MEMS and Complementary Metal-Oxide-Semiconductor (CMOS) technologies were not mature enough Figure 1.1a and Figure 1.1b) for the joint development of what was later known as smart sensors, currently the unceasing technological advances have resulted in countless applications and devices that have become daily commodities in our lives, as it is clearly shown in (Figure 1.1, where past revenue and the forecasted growth of the silicon wafer market (Figure 1.1c) and the MEMS market (Figure 1.1d) is reported.

The inclusion in the same silicon die of all the elements required for a complete monitoring and actuation process has been possible thanks to the advances in micro (and nano) electronics, which results in a constant downscaling of the dimensions of basic CMOS electronics components, enabling the integration of additional components in the same area and with limited power consumption. At the same time, the improvement in the processing technologies and surface micromachining of silicon and other complementary materials has allowed the development of advanced CMOS-compatible integrated sensors on silicon chips.

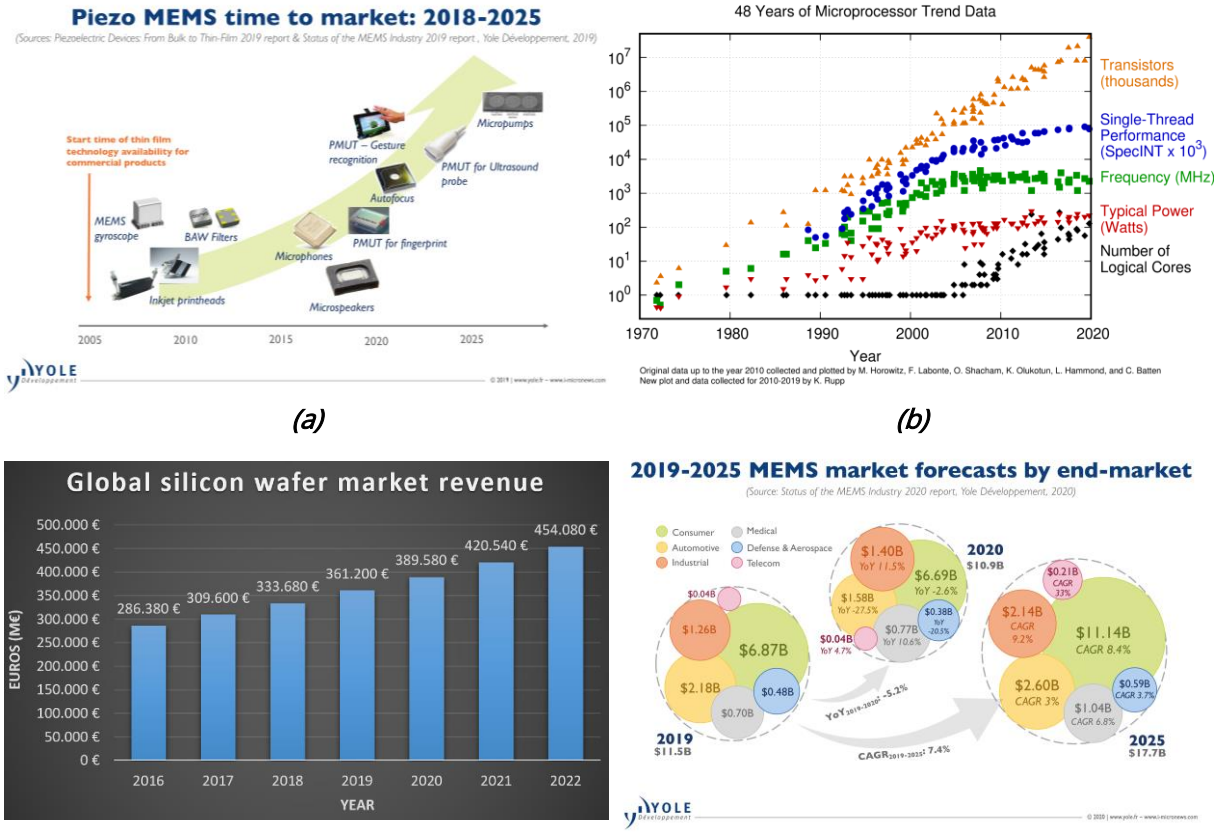


Figure 1.1. Evolution of a) piezo MEMS devices as MEMS example [2] and b) CMOS technologies over time (48-year trend) [3]; and past revenue and forecasted growth of c) global silicon wafer market [data extracted from 4], and d) MEMS market [5].

Compared with the classical counterparts, CMOS sensors present lower cost and power consumption at a smaller size. This allows the creation of high-density sensor arrays supporting large parallelization processes, highly suitable to be applied in different fields, e.g., genomic, proteomic, analytical chemistry, environmental monitoring or biohazards detection [6]. These emergent fields mainly rely on CMOS impedance sensors to accomplish detection, since this approach exhibit one key advantage in terms of performance and utility: they permit label-free detection, eliminating the time, cost and complexity associated to label-based techniques. Impedance evaluation of the sample under test over a specific frequency range of interest is performed through a technique named as Impedance Spectroscopy (IS), which requires a small stimulus signal compared to DC-based methods, reducing the damage or the disturbance risks for the analysed samples.

A review of the state of the art related to the design and implementation of processing systems for impedance measurement evidences that efforts have been mainly focused on using the current nanotechnologies matured over the last decades to develop accurate, highly-selective sensors, leaving the acquisition, signal processing and digitization tasks to commercial benchtop instruments. Figure 1.2 shows a graph of different commercial instruments used for impedance spectroscopy and their frequency ranges. The highly processing power of these external instruments eases the

characterization processes, but at the cost of having expensive, heavyweight, high-power, hardly portable systems, limiting their application only to large laboratories and facilities.

Alternatively, the combination of a System on Chip (SoC) sensor-processing package, together with the use of a microprocessor as digital core, where signal digitization, data processing and data communication can be executed, will provide features as reduced cost and compactness, portability, battery power, ease of use and intelligent data sharing, increasing the potential number of applications and users of these techniques.

This thesis intends to deepen in the design of a truly portable battery-operated low-power wide frequency impedance spectroscopy measurement system, based on CMOS microelectronic technologies. This requires the development of the different microelectronic cells conforming the IS interface, satisfying the demanding high performance constraints required for this application in portable characterization and monitoring. A detailed analysis of the electronic components involved in the excitation and signal recovery of IS systems shows similar characteristics to those required for the processing of low-level electronic signals coming from highly noisy environments. Namely, amplifiers featuring high signal to noise ratio with low noise floor together with wide and adjustable gain and wide bandwidth to fit the specific requirements for different applications. In addition, to ensure portability in order to broaden their application scenario, minimum size and low-power consumption are also compulsory, characteristics that become even more critical when sensors array are considered, while making also necessary to accomplish the design of suitable low-dropout voltage regulators to conform the power management stage.

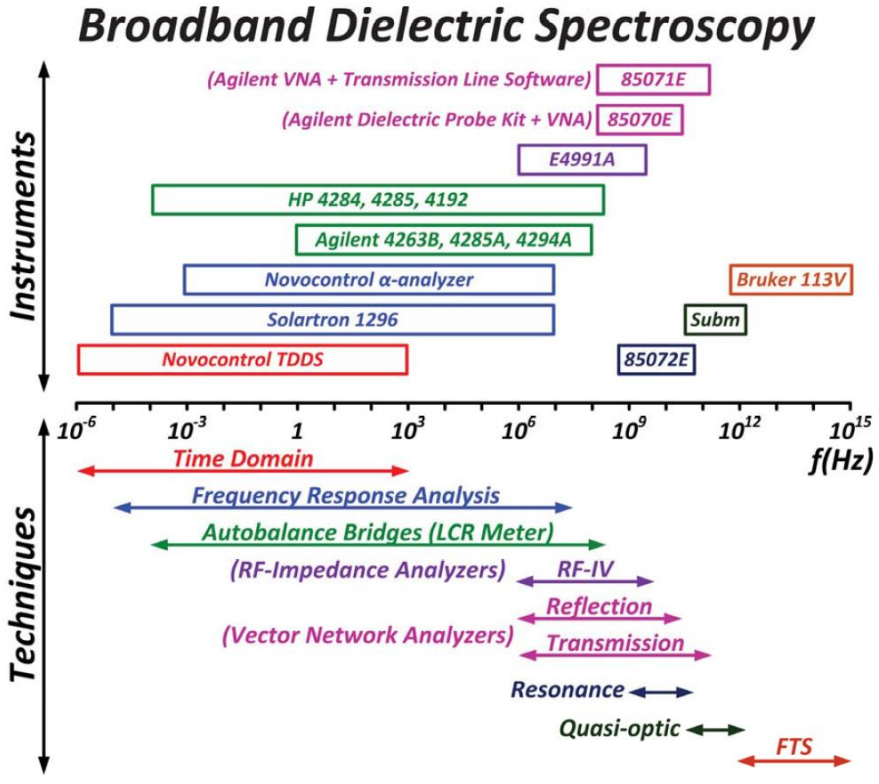


Figure 1.2. Commercial equipment and impedance spectroscopy techniques with their frequency operating range [7].

1.1. IMPEDANCE SPECTROSCOPY

Impedance spectroscopy dates back to the end of the XIX century. However, despite its simple concept -measuring the electrical current passing through a sample at various frequencies of an excitation voltage- and its early conception, it was not until the end of the XX century when its true potential was showed. In fact, the interest in IS grew substantially thanks to digital instrumentation controlled by computers, which allows quick and easy measurements as well as complex data processing and analysis. Thus, it has evolved into a powerful experimental technique widely used in a broad range of applications such as microbiological analysis; food control; human body analysis; planetary surface research; rapid detection of foodborne pathogenic bacteria; real-time detection of milk adulteration; characterization of fast ion transport in solid electrolytes; diagnosis of diseases, including cancer and virus detection; as a testing technique for modern electronic devices or electro-ceramics characterization (technological materials used in actuators and sensors, computer memories, electrically controlled microwave tuning devices for RADAR, etc.) [8-31].

In most of these IS applications only the sensing probes and microfluidic packaging are integrated in the so-called lab-on-chip (LoC) devices, taking the advantage of the CMOS processes to implement the required MEMS [6], but leaving the rest of components that conform the data acquisition chain (excitation signal generators, conditioning, pre-processing and digitization electronics) to benchtop instruments. According to this, IS-based measurement and characterization instruments are considered almost exclusively as external equipment for chemical, biological or quality control laboratories, hindering its use closer to the sampling sources as portable laboratories for on-site tests exploiting the advantages that full miniaturization by means of an Application Specific Integrated Circuit (ASIC) can provide to the measurement system.

1.1.1. Impedance

The sensor equivalent electrical model used in Impedance Spectroscopy is an impedance, denoted by Z. Table 1.1 lists some Z model examples, showing the component values, frequency operating ranges and target applications. A generic impedance $Z=Z(\omega)$ is a complex quantity defined as

$$Z = R + jX \tag{1.1}$$

with $Re(Z) = R$ the resistance, $Im(Z) = X$ the reactance, both measured in Ohms (Ω). Alternatively, (1.1) can be expressed into polar coordinates according to

$$Z = |Z|(cos\theta + jsin\theta) = |Z|e^{j\theta} \tag{1.2}$$

with $|Z|$ the magnitude and θ the phase.

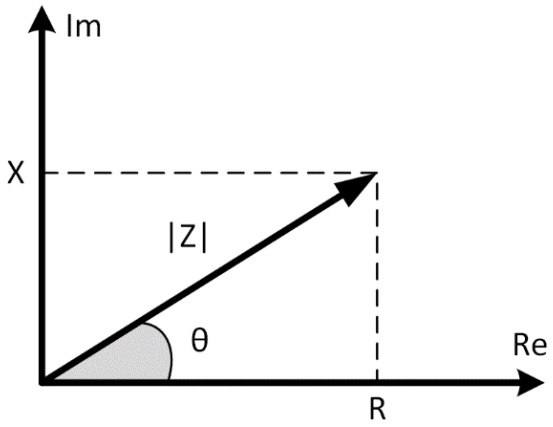


Figure 1.3. Complex impedance plane.

Table 1.1. List of different electric models and their applications [32].

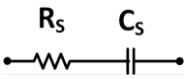
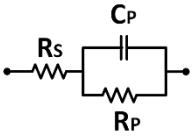
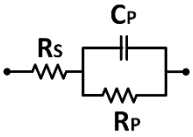
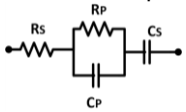
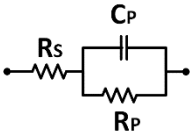
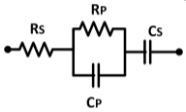
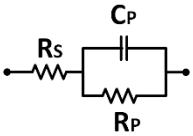
Reference paper	Model	Model values	Application
[1]	Coating 	R_S=500 Ω, C_S=200 pF, f_o{0.1-1 MHz}	Damage over the capacitive coating of a metal
[33]	Electrode 	R_s=1 kΩ, R_P=4 MΩ-20 MΩ C_P=50 nF f_o{1-20 kHz}	Tissue impedance measurement for myocardial ischemia detection
[34]	Electrochemical cell 	R_s=10 kΩ, R_P=4.4 MΩ C_P=400 pF f_o{0.1-10 kHz}	DNA electrochemical detection systems (Potassium Ferricyanide)
[35]	R-C biosensor impedance 	R_s=1 GΩ, R_P=1 MΩ C_P=500 pF, C_S=300 pF f_o{0.1-10 kHz}	Prostate cancer DNA detection
[36]	Human pacemaker 	R_S=664 Ω, R_P=284.8 Ω C_P=48.42 μF f_o{188-5.8 kHz}	Pacemaker-Induced Fibrosis Detection
[37]	Electrode-Electrolyte 	R_S=422 kΩ, R_P=149 kΩ C_P=55 pF, C_S=75 pF f_o{10-50 MHz}	Detection of various biological analytes, such as DNA and proteins
[38]	Protein 	R_S=431 kΩ, R_P=149.1 kΩ C_P=57 pF f_o{34-337 kHz}	Protein detection

Figure 1.3 shows the complex impedance plane, relating R, X and $|Z|, \theta$. The real and imaginary components can be obtained from $|Z|, \theta$ as

$$R = |Z| cos\theta \tag{1.3}$$

$$X = |Z| sin\theta \tag{1.4}$$

while the magnitude and phase can be derived from R, X as follows

$$|Z| = \sqrt{X^2 + R^2} \tag{1.5}$$

$$\theta = arctan\left(\frac{X}{R}\right) \tag{1.6}$$

For IS measurement the ultimate objective is to recover the impedance Z; therefore, the measurement system must recover both the real and imaginary components or, equivalently, both the magnitude and phase.

1.1.2. IS Read-Out Systems

There are several impedance extraction algorithms, which can be classified into two main groups, digital or analog, depending on their operating domain. In the digital domain, the most used extraction method is the Fast Fourier Transform (FFT) [17] or its fast version, the logarithmic FFT [39]. The FFT algorithm computes, from a composite signal, the impedance spectrum result at all frequencies simultaneously. This method requires the use of a Digital Signal Processor (DSP) with extensive computational resources to generate the composite signal and derive the FFT [39], not being suitable for the typical low-cost microcontrollers embedded in portable applications.

Alternatively, in the analog domain, the extraction technique typically used is the Frequency Response Analyzer (FRA) method. It recovers the real and imaginary components of one frequency signal at a time, sweeping over the frequency range where the Device Under Test (DUT) has demonstrated a reliable response. Compared to the FFT method, the FRA method is a simpler algorithm that can be fulfilled with a simple and compact analog circuit architecture, making it the most suitable choice to obtain a low-voltage low-power (LVLP) compact size solution for sensor array systems [39].

On the other hand, reviewing the literature, although there have been certain attempts towards the integration of commercial instrumentation, only partial success has been made in this direction, being the most used the Discrete Fourier Transform based AD5933 integrated circuit from Analog Devices [40]. However, it presents the inherent constraints of a digital implementation, with a typical power consumption of 33-93.5 mW not compatible with battery-powered devices, and a frequency range up to 100 kHz.

Others solutions rely on commercial off the shelf (COTS) components [41-43] jeopardizing size and consumption, finding only very few fully integrated impedance measurement systems in the literature [44-51]. Among those, [42, 46, 48] are single-channel, not being capable of recovering the real and imaginary components of the impedance under test.

Focusing on dual-channel systems, and taking into account that the trend towards the integration of sensor arrays to permit multi-parameter sensor fusion imposes even more demanding design restrictions, while increasing operating frequencies up to the 100 MHz rage are required to widen the application scenarios, [44-47, 52, 53] still present high power (9.6 mW/ch, 24 mW/ch, 1.9 mW/ch and ~1.2 mW/ch respectively) and area consumption (2 mm^2/ch, 1.75 mm^2/ch, 0.36 mm^2/ch and 0.21 mm^2/ch). Low-power proposals (<1mW/ch) such as [49, 50, 51, 54, 55, 56] exhibit operating frequencies below 10 MHz. Table 1.2 shows a comparison of some of these integrated IS read-out systems and their main performances.

In addition, the trend towards the integration of sensor arrays to permit multi-parameter sensor fusion imposes even more demanding design restrictions, with increasing operating frequencies to widen the application scenarios. Therefore, proposals such as [49] with a 2 MHz bandwidth or [50] are no longer suitable for multichannel portable IS read-out devices. Within the multichannel CMOS IS read-out approaches [35, 52, 54], the analog lock-in-based FRA technique seems an appropriate solution potentially featuring the required LVLP high frequency constraints. It is based on synchronous demodulation to extract the response of low signal-to-noise ratio (SNR) sensor signals at a reference frequency f_o.

Therefore, the design of a IS front-end, able to recover the values of the real and imaginary components of the equivalent impedance of a sample under study (or its magnitude and phase, alternatively) over the frequency range of interest, complying with the main features of a commercial impedance analyser in terms of accuracy, while simultaneously preserving LVLP and compact size –critical requirements for a multichannel approach– is still an open challenge, specially when operating at very high frequency, that is, up to hundreds of MHz. This range is aimed to characterize biological systems, cells and molecules [11, 12, 43] by facilitating the advance of new technological tools for the study and detection of diseases [57, 8-10]. To achieve this goal, the analog lock-in-based FRA technique seems the most suitable solution potentially featuring the required LVLP high frequency constraints. It is based on dual synchronous demodulation to extract the magnitude and phase response of low SNR sensor signals at a reference frequency f_o.

Table 1.2. Comparison of previously reported integrated IS read-out systems [58].

Parameter	[52]'13	[53]'13	[59]'15	[54]'16	[55]'20	[56]'20	[51]'21	[44]'21
Results	Exp	Sim	Exp	Sim	Sim	Exp	Sim	Exp
CMOS (µm)	0.18	0.18	Arduino-based	0.18	0.18	0.18	0.18	0.065
Supply (V)	1.8	±0.9	N/A	1.8	1.8	1.8	1.8	1.8, 3.3
Power (W)	37m	28m	N/A	482µ	36.1µ	311.4µ	544µ	9.6m
Gain (dB)	N/A	N/A	N/A	39-59	0-20	N/A	7-48	24
Freq. range (Hz)	15M-20M	100-580k	0.01-100k	1.1M	0.1–1M	DC-100k	100-10M	1k-10M
Area (mm^2)	5	0.4	N/A	0.03	N/A	0.208	1.95	16 (die, 8ch)

1.2. DUAL SYNCHRONOUS DEMODULATION

Dual Synchronous demodulation (DSD), also known as dual phase sensitive detection (DPSD), singles out the components (magnitude and phase) of an AC signal at a specific frequency, calculated by multiplication with two quadrature reference signals that are locked in frequency with the original signal, while signals/noise at frequencies apart from the reference frequency are rejected [60-63].

The general scheme of a DSD read-out is shown in Figure 1.4. Consider an impedance sensor (DUT) excited with a sinusoidal signal V_{exc} of known amplitude A_o and frequency f_o, providing a response V_{sens} of identical frequency but with unknown amplitude (A_s) and phase shift (θ) with respect to this excitation signal

$$V_{sens} = A_s \sin(2\pi f_o t + \theta) \tag{1.7}$$

The sensor output signal V_{sens} is then multiplied by two quadrature $V_{ref,I}$, $V_{ref,Q}$ reference signals of the same frequency f_o as the excitation signal. Assuming that the quadrature reference signals are sinusoidal,

$$V_{ref,I} = A_{ref} \sin(2\pi f_o t) \tag{1.8}$$

$$V_{ref,Q} = A_{ref} \sin(2\pi f_o t + \pi/2) = A_{ref} \cos(2\pi f_o t) \tag{1.9}$$

The product of $V_{ref,I}$ with V_{sens} results in

$$V_{sens} V_{ref,I} = \frac{A_s A_{ref}}{2} [-\cos(2\pi f_o t + \theta) + \cos(\theta)] \tag{1.10}$$

Where the first term operates a two times the frequency f_0, and the second term is a DC component. A Low Pass Filter is used to filter out the first component extracting the DC level.

$$V_x(I) = V_{sens} V_{ref,I} = \frac{A_s A_{ref}}{2} \cos(\theta) \tag{1.11}$$

As for the $V_{ref,Q} V_{sens}$ product,

$$V_y(Q) = V_{sens} V_{ref,Q} = \frac{A_s A_{ref}}{2} \sin(\theta) \tag{1.12}$$

The use of a sinusoidal signal introduces less harmonics in the mixer operation [60]. However, this requires the implementation of quadrature sinousoidal oscillators with constant amplitude and an adjustable wide frequency range, not trivial in portable systems with low power constraints. Alternatively, and taking into account that the technique itself rejects signals at frequencies different from f_0, squared quadrature signals are often used for simplicity [64].

In this case, the signals are easily implemented by a digital port of the embedded microcontroller. In this case, the mixer operation results in

$$V_{sens}V_{sq} = 2A_{sens}A_{sq}\left\{\cos\left[\left(\omega_0 t + \omega_{sq}t\right) + \theta\right] + \cos\left[\left(\omega_0 t - \omega_{sq}t\right) + \theta\right] - \frac{1}{3}\cos\left[\left(\omega_0 t + 3\omega_{sq}t\right) + \theta\right] - \frac{1}{3}\cos\left[\left(\omega_0 t - 3\omega_{sq}t\right) + \theta\right] + \frac{1}{5}\right\} \quad (1.13)$$

Since $\omega_o = \omega_{sq}$, the resulting equations after the low pass filter, are a DC component

$$V_x(I) = \frac{2A_s A_{ref}}{\pi}\cos(\theta) \quad (1.14)$$

$$V_x(Q) = \frac{2A_s A_{ref}}{\pi}\sin(\theta) \quad (1.15)$$

The recovered DC voltage values -namely V_x and V_y- are proportional to the real and imaginary components of the impedance sensor of interest. From these last equations, we can derive the amplitude and phase

$$A_s = \frac{\pi}{2}\sqrt{(V_x)^2 + \left(V_y\right)^2} \quad (1.16)$$

$$\theta = \arctan\left(\frac{V_y}{V_x}\right) \quad (1.17)$$

Finally, note that the proposed read-out in this thesis is due to operate in portable devices powered by batteries. Therefore, a Low Dropout Regulator (LDO) is needed to provide a stable, low-noise and accurate single supply V_{dd} from the battery power. The magnitude/phase recover algorithms must then take into account that the signals being processed are centered over a common mode voltage $V_{cm} = V_{dd}/2$. In this way, the DC levels obtained at the output of the low pass filters, V_x and V_y, will be respectively:

$$V_x = \frac{Vdd}{2} - 2A_S\cos(\theta) \quad (1.18)$$

$$V_y = \frac{Vdd}{2} + 2A_S\cos(\theta) \quad (1.19)$$

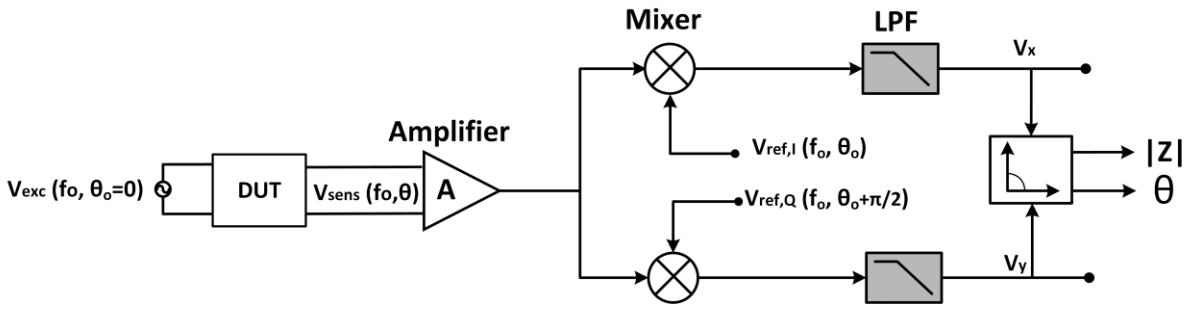


Figure 1.4. Classic dual-phase PSD structure.

and therefore the sensor magnitude and phase will be given by

$$A_S = \frac{\pi}{2}\sqrt{\left(V_x - {Vdd}/{2}\right)^2 + \left(V_y - {Vdd}/{2}\right)^2} \tag{1.20}$$

$$\theta = \frac{\left(V_y - {Vdd}/{2}\right)}{\left(V_x - {Vdd}/{2}\right)} \tag{1.21}$$

1.3. OBJECTIVES

The core purpose of this thesis is the advance in the design of microelectronic cells based on CMOS technologies to conformn an IS interface featuring the characteristics of portable devices (Figure 1.5), so that the analog front-end can be embedded in the sensor package, providing a parallelizable implementation at no significant cost of size or power consumption, but keeping the main reliability and sensibility characteristics of a laboratory instrument.

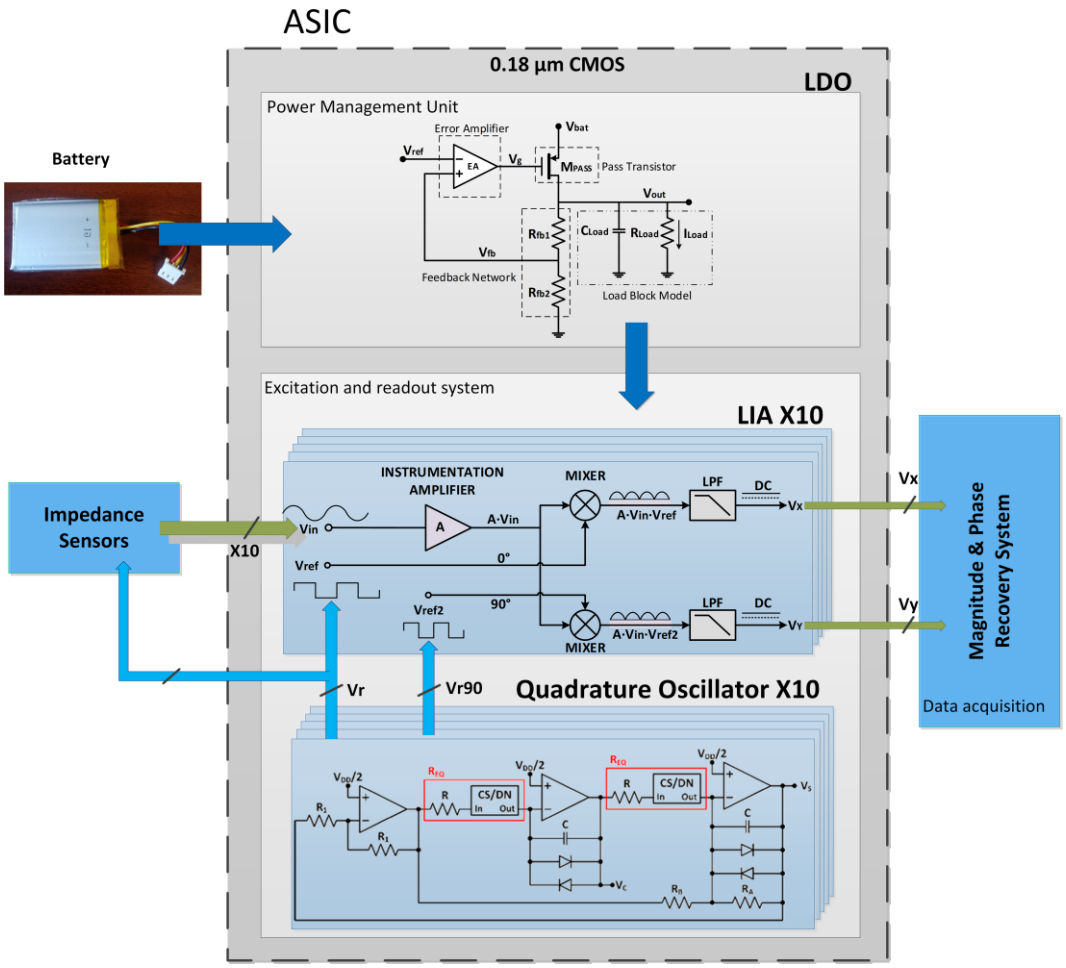


Figure 1.5. Proposed portable Impedance Spectroscopy interface.

A 1.8 V–0.18 μm CMOS process based on general P-Sub structure with 1 layer of poly and 6 layers of metal is used for all designs of this thesis. The IS front-end must comply the following general specifications: power supply at a 1.8 V regulated voltage coming from a LDO, with a 20 dB to 40 dB gain range and a programmable frequency range up tp ~100 MHz to obtain a versatile topology suitable for different applications, all fully integrated –including the output DC extractors- to minimize size and with low-power (<500 μW/channel). The integrated system should be able to provide connectivity for at least 10 biosensing elements per chip.

A detailed view of the main aspects developed in this thesis are:

- Review and analysis of the main available impedance spectrometry techniques, focusing on IS methodologies suitable for sensor arrays. This study concludes that the FRA-lock-in technique seems the most suitable choice for a LVLP high frequency implementation.
- Design and implementation of a reliable power management stage, based on linear LDOs. Assuming the IS electronics will work under restricted energy conditions, the goal is to develop an efficient fully integrated LDO with good static-dynamic trade-off performance.
- Design and implementation of the preconditioning stage for low-level input signals. Because the excitation signals for impedance measurement present low amplitudes, responses are expected in the order of few mV. Therefore, the preamplifiers must comply with strict noise specifications. Thus, besides low-noise design, a fully differential approach is adopted, while to attain a versatile solution the design includes a configurable voltage/current input stage, with programmable bandwidth, both at the low and high cut-off frequencies.
- Design and implementation of variable/programmable gain amplifiers (VGA/PGAs), to adjust the gain of the processing stage, thus achieving on the overall -by cascading the low-noise preamplifier and a PGA- a low-noise programmable gain programmable bandwidth instrumentation amplifier.
- Design and implementation of a mixer or multiplying circuit to conform the core Synchronous Demodulation (SD) stage.
- Design and implementation of fully integrated Low Pass Filters (LPF) used as DC magnitude extractors, with programmable sub-Hz to hundreds of Hzs cutoff frequencies, to adjust the compromise between the recovery accuracy and the acquisition time.
- Fully integrated CMOS implementation of a complete readout circuit for impedance characterization based on the aforementioned basic proposed cells, compatible with the requirements of low-voltage (nominal 1.8 V) and low power. Validation of the proposal by characterization of the electrical behaviour and the recovered Z of a given impedance sensor. Comparison with state-of-art proposals to situate the contribution of the work.

1.4. THESIS ORGANIZATION

This thesis is organized in five chapters and four appendixes, being the first chapter this introductory one while the last chapter is reserved for conclusions and future research. To ease its reading, the contents, list of figures, list of tables, glossary and acronyms can be found at the beginning. In addition, at the end of each chapter, a section is reserved for the bibliography employed along the chapter.

In this first chapter, the motivation of this work has been presented, along with an introduction to electrical sensing and more specifically to Impedance Spectroscopy. The different IS approaches have been reviewed and current state-of-the-art in read-out systems has been presented, explaining in detail the Dual Synchronous Demodulation technique used in this thesis. Finally, the main objectives of this thesis and its organization have been presented.

Chapter 2 to Chapter 4 are the core of the thesis. They all have an introduction, design and characterization of the different cells presented and conclusions.

Chapter 2 is reserved for the power management unit required in battery-powered portable devices. Firstly, the necessity of power management units is explained, presenting the different possible structures. Secondly, the main LDO CMOS topology and characteristic parameters are introduced. Then, the design of a fully integrated 1.8 V low dropout regulator is presented and its experimental characterization is shown, as well as its functionality within the power management unit for a microinstrument application.

In Chapter 3, the different stages that compose a dual synchronous demodulator are studied. The input amplification stage, multiplication stage and output filtering stage are analysed, designed and characterized. Common to all of them, it is firstly introduced the function and the main design characteristics of each stage; then the proposed structures are described, presenting the different design techniques applied, and finally they are validated. In the first section, a pre-amplifier with fixed gain, low noise, capable of sensing current and voltage inputs is presented and validated, followed by a variable gain amplifier to adjust the total amplifier gain depending on the input signal amplitude. The second section presents a technique to embed the multiplying stage within the last stage of the amplifier to minimize size and power. Finally, considering the output filtering stage different structures of tuneable low pass filters are presented, to act as the DC magnitude extractors to recover the real and imaginary parts of the target impedance Z.

Chapter 4 presents the complete front-end structure for a dual-phase synchronous demodulator based on the blocks introduced in the previous chapter. Besides, a compact version -at the cost of jeopardized performance parameters- is introduced.

To conclude, Chapter 5 summarizes the general conclusions of this thesis and its main contributions. In addition, future research lines are given.

The appendixes are placed at the end of this work. Appendix I summarizes the process parameters of the 180 nm CMOS technology from UMC used for the designed proposals. Appendix II collects the detailed analysis in small signal (AC), low frequency (LF) of the line

regulation factor, LNR, and the load regulation factor, LDR, of a low dropout regulator. Appendix III is dedicated to the frequency analysis of a Low Dropout Regulator without compensation, determining its characteristic equation. Appendix IV presents a Variable Gain Amplifier designed in the 180 nm CMOS technology from TSMC.

1.5. REFERENCES

1. Lebsack, G. Sensors are fundamental to new intelligent systems. White paper, *Menthor*, 2018.
2. Piezoelectric Devices: From bulk to Thin-Film 2019 report & Status of the MEMS Industry 2019 report, *YOLE Développement*, 2019.
3. Rupp, K. 48 years of Microprocessor Trend Data, 2020. Last accessed: 05th November 2021. https://github.com/karlrupp/microprocessor-trend-data
4. Silicon Wafer Manufacturers Market Share. *T4,* 2020. Last accessed: 05th November 2021. https://www.t4.ai/industry/silicon-wafer-manufacturers-market-share
5. Status of the MEMS Industry 2020 report, *YOLE Développement*, 2020.
6. Temiz, Y., Lovchik, R.D., Kaigala, G.V., Delamarche, E. Lab-on-a-chip devices: How to close and plug the lab?. *Microelectronics Engineering*, 2015.
7. Bakshiani, M. A Self-Sustained Miniaturized Microfluidic-CMOS Platform for Broadband Dielectric Spectroscopy. *PhD Thesis*, 2015.
8. Liu, J.T., Settu, K., Tsai, J.-Z., Chen, C.-J. Impedance sensor for rapid enumeration of *E. coli* in milk samples. *Electrochimia Acta* 182, 2015.
9. Durante, G., Becari, W., Lima, F.A.S. and Peres, H.E.M. Electrical Impedance Sensor for Real-Time Detection of Bovine Milk Adulteration. *IEEE Sensors Journal*, 2016.
10. Sitkov, Zimina, N., T.M. and Soloviev, A.V. Development of Impedimetric Sensor for E. coli M-17 Antibiotic Susceptibility Testing. *IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (ElConRus)*, Moscow, Rusia, 2018.
11. Conesa, C., Civera, J.I., Seguí, L., Fito, P. and Laguarda-Miró, N. An Electrochemical Impedance Spectroscopy System for Monitoring Pineapple Waste Saccharification. *Sensors*, 2016.
12. Mansoorifar, A., Koklu, A., Ma, S., Raj, G.V. and Beskok, A. Electrical Impedance Measurements of Biological Cells in Response to External Stimuli. *Analytical Chemistry*, 2018.
13. Ramirez, N., Regueiro, A., Arias, O. and Contreras, R. Electrochemical impedance spectroscopy: An effective tool for a fast microbiological diagnosis. *Biotecnologia Aplicada*, 2008.
14. Grossi, M., Di Lecce, G., Gallina Toschi, T. and Riccò, B. Fast and Accurate Determination of Olive Oil Acidity by Electrochemical Impedance Spectroscopy. *IEEE Sensors Journal*, 2014.
15. Clemente, F., Arpaia, P. and Manna, C. Characterization of human skin impedance after electrical treatment for transdermal drug delivery. *Measurement*, 2013.
16. Gadermaier, B., Hogrefe, K., Heitjans, P. and Wilkening, M. Broadband impedance spectroscopy of Li4Ti5O12: from nearly constant loss effects to long-range ion dynamics. *Journal of Inorganic and General Chemistry*, 2021.
17. Barsoukov, E. and Macdonald, J.R. Impedance spectroscopy: theory, experiment, and applications. *John Wiley & Sons*, 2018.
18. Lvovich, V.F. Impedance Spectroscopy: Applications to Electrochemical and Dielectric Phenomena, *1st ed. Wiley*, 2012.
19. Chang, B.-Y. and Park, S.-M. Electrochemical impedance spectroscopy. *Annual Review of Analytical Chemistry*, 2010.
20. Grimnes, S. and Martinsen, O.G. Bioimpedance and bioelectricity basics. 3rd ed. Academic Press, *Elsevier Ltd*, 2015.
21. Kanoun, O. Impedance Spectroscopy: Advanced Applications: Battery Research, Bioimpedance, System Design. *Walter de Gruyter GmbH & Co KG,* 2018.
22. Brus, V. On impedance spectroscopy analysis of nonideal heterojunctions. *Semiconductor Science and Technology*, 2012.
23. Trautner, R. Grard, R. and Hamelin, M. Detection of subsurface ice and water deposits on Mars with a mutual impedance probe. *Journal of Geophysical Research: Planets*, 2003.

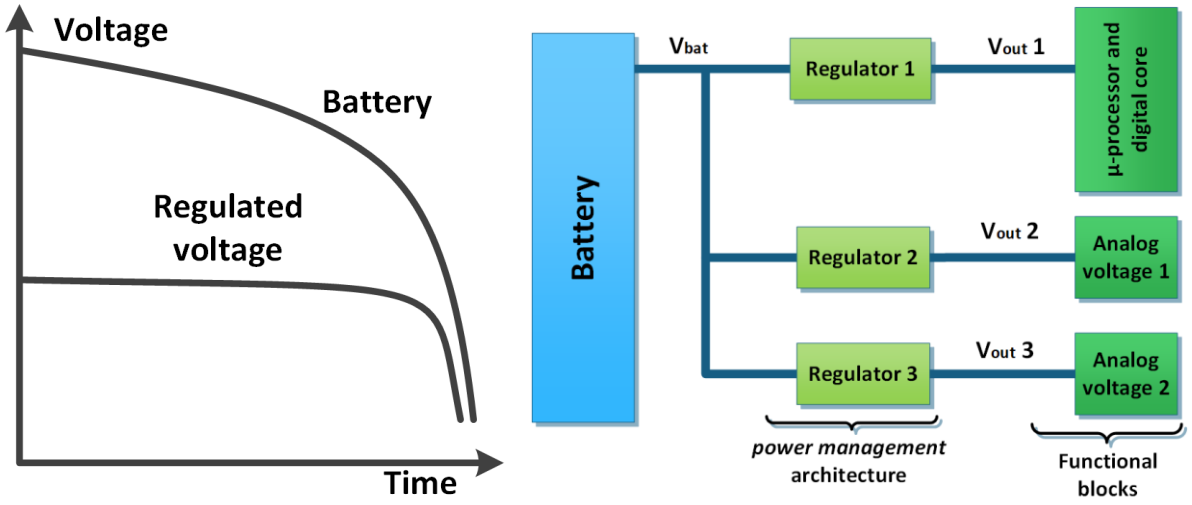
24. Van Eijnatten, M.A., Van Rijssel, M.J., Peters, R.J., Verdaasdonk, R.M. and Meijer, J.H. Comparison of cardiac time intervals between echocardiography and impedance cardiography at various heart rates. *Journal of electrical bioimpedance*, 2019.
25. Nidzworski, D., Pranszke, P., Grudniewska, M., Krol, E. and Gromadzka, B. Universal biosensor for detection of influenza virus. *Biosensors and Bioelectronics*, 2014.
26. Campbell, C.E., Laane, M.M., Haugarvoll, E. and Giaever, I. Monitoring viral-induced cell death using electric cell substrate impedance sensing. *Biosensors and Bioelectronics*, 2007.
27. Cho, S., Becker, S., von Briesen, H. and Thielecke, H. Impedance monitoring of herpes simplex virus-induced cytopathic effect in Vero cells. *Sensors and Actuators B: Chemical*, 2007.
28. Teng, Z., Kuang, X., Wang, J. and Zhang, X. Real-time cell analysis-a new method for dynamic, quantitative measurement of infectious viruses and antiserum neutralizing activity. *Journal of virological methods*, 2013.
29. Irvine, J., Sinclair, D. and West, A. Electroceramics: Characterization by Impedance Spectroscopy. *Advanced Materials*, 1990.
30. Sinclair, D.C. Characterization of electro-materials using AC impedance spectroscopy. *Boletín de la Sociendad Española de Cerámica y Vidrio*, 1995.
31. Pandey, S., Kumar, D., Parkash, O. and Pandey, L. Impedance Spectroscopy: A Powerful Technique for Study of Electronic Ceramics. *Ceramic Materials – Synthesis, Characterization, Applications and Recycling*, 2019.
32. Maya-Hernández, P.M. Personal Communication. Group of Electronic Design (GDE-I3A), University of Zaragoza, 2019.
33. Yufera, A., Rueda, A., Muñoz, J. M., Doldan, R., Leger, G. and Rodriguez-Villegas, E.O. A tissue impedance measurement chip for myocardial ischemia detection. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2005.
34. Jafari, H.M. and Genov, R. CMOS impedance spectrum analyzer with dual-slope multiplying ADC. *IEEE Biomedical Circuits and Systems Conference (BioCAS*), San Diego, USA, 2011.
35. Jafari, H., Soleymani, L. and Genov, R. 16-Channel CMOS Impedance Spectroscopy DNA Analyzer With Dual-Slope Multiplying ADCs. *IEEE Transactions on Biomedical Circuits and Systems*, 2012.
36. De Roux, E., Terosiet, M., Kölbl, F. Boissière, M., Histace, A. and Romain, O. OFDM-based electrical impedance spectroscopy technique for pacemaker-induced fibrosis detection implemented in an ARM microprocessor. *Microprocessors and Microsystems*, 2019.
37. Manickam, A., Chevalier, A., McDermott, M., Ellington, A.D. and Hassibi, A.A CMOS Electrochemical Impedance Spectroscopy (EIS) Biosensor Array. *IEEE Transactions on Biomedical Circuits and Systems*, 2010.
38. Márquez, A., Pérez-Bailón, J., Calvo, B., Medrano, N., Martínez, P.A. A CMOS Self-Contained Quadrature Signal Generator for SoC Impedance Spectroscopy. *Sensors,* 2018.
39. Rairigh, D., Mason, A., and Yang, C. Analysis of On-Chip Impedance Spectroscopy Methodologies for Sensor Arrays. *Sensor Letters*, 2006.
40. AD5933 Datasheet. *Analog Devices*, 2017.
41. Kusche, R., Klimach, P. and Ryschka,M. A Multichannel Real-Time Bioimpedance Measurement Device for Pulse Wave Analysis. *IEEE Transactions on Biomedical Circuits and Systems*, 2018.
42. Montero-Rodríguez, J.J., Fernández-Castro, A.J., Schroeder, D. and Krautschneider, W. Development of an impedance spectroscopy device for on-line cell growth monitoring. *Electronics Letters*, 2017.
43. Chowdhury, D. and Chattopadhyay, M. Study and Classification of Cell Bio-Impedance Signature for Identification of Malignancy Using Artificial Neural Network. *IEEE Transactions on Instrumentation and Measurement*, 2021.

44. Lee, J., Gweon, S., Lee, K., Um, S., Lee, K.-R. and Yoo, H.-J. A 9.6-mW/Ch 10-MHz Wide-Bandwidth Electrical Impedance Tomography IC With Accurate Phase Compensation for Early Breast Cancer Detection. *IEEE Journal of Solid-State Circuits*, 2021.
45. Ciccarella, P., Carminati, M., Ferrari, G., Bianchi, D., Grillanda, S., Morichetti, F., Melloni, A. and Sampietro, M. Impedance-Sensing CMOS Chip for Noninvasive Light Detection in Integrated Photonics. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2016.
46. Murali, P., Ranjit, K., Bhat, N., Banerjee, G., Amrutur, B., Bhat, K.N. and Ramamurthy, P.C.A CMOS Gas Sensor Array Platform With Fourier Transform Based Impedance Spectroscopy. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012.
47. Valente, V. and Demosthenous, A. Wideband Fully-Programmable Dual-Mode CMOS Analogue Front-End for Electrical Impedance Spectroscopy. *Sensors*, 2016.
48. Burns, R.P., Dunning, J. and Fu, M.J. A Low-Cost Bioimpedance Phase Angle Monitor for Portable Electrical Surface Stimulation Burn Prevention. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2021.
49. Onet, R., Rusu, A. and Rodriguez, S. High-Purity and Wide-Range Signal Generator for Bioimpedance Spectroscopy. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2017.
50. Yúfera, A. and Rueda, A. Design of a CMOS closed-loop system with applications to bio-impedance measurements. *Microelectronics Journal*, 2010.
51. Cheon, S.-i., Kweon, S.-J., Kim, Y., Ha, S. and Je, M. A Power-Efficient, Wide-Frequency-Range Impedance Measurement IC Using Frequency-Shift Technique. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021.
52. Hu, A. and Chodavarapu, V.P. General-purpose high-speed integrated lock-in amplifier with 30dB dynamic reserve at 20MHz. *Analog Integrated Circuits and Signal Processing*, 2013.
53. Huang, H. and Palermo, S. A TDC-based front-end for rapid impedance spectroscopy. *IEEE International Midwest Symposium on Cicuits and Systems (MWSCAS)*, Columbus, USA, 2013.
54. Maya-Hernández, P.M., Sanz-Pascual, M.T. and Calvo, B. Micropower CMOS lock-in amplifier for portable applications. *Electronics Letters*, 2016.
55. Márquez, A., Medrano, N., Calvo, B. and Pérez-Bailón, J. A Dual Synchronous Demodulator for Phase Sensitive Detection Applications. *IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, Dubrovnik, Croatia, 2020.
56. Shen, B. and Johnston, M.L. DC-100 kHz Tunable Readout IC for Impedance Spectroscopy and Amperometric Measurement of Electrochemical Sensors. *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, USA, 2020.
57. Yang, L. and Bashir, R. Electrical/electrochemical impedance for rapid detection of foodborne pathogenic bacteria. *Biotechnology Advances*, 2008.
58. Pérez-Bailón, J., Sanz-Pascual, M.T., Calvo, B. and Medrano, N. Wide-band compact 1.8 V-0.18 µm CMOS Analog Front-end for Impedance Spectroscopy. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2021. (early access)
59. Grassini, S., Corbellini, S., Angelini, E., Ferraris, F. and Parvis, M. Low-Cost Impedance Spectroscopy System Based on a Logarithmic Amplifier. *IEEE Transactions on Instrumentation and Measurement*, 2015.
60. Meade, M.L. Lock-in Amplifiers: Principles and Applications, *Peter Peregrinus Ltd.*, 1983.
61. Stanford Res. Sys. Lock-in amplifiers, application notes, datasheets. 1999.
62. Blair, D.P. Phase sensitive detection as a means to recover signals buried in noise. *Journal of Physics E: Scientific Instruments*, 1975.
63. Scofield, J.H. Frequency-domain description of a lock-in amplifier. *American Journal of Physics*, 1994.

64. Aguirre, J., Garcia-Romeo, D., Medrano, N., Calvo, B. and Celma, S. Square signal based algorithm for analog lock-in amplifiers. *IEEE Transactions on Industrial Electronics*, 2014.

Chapter 2
Power Management

One of the essential subsystems to achieve a truly portable battery-operated SoC solution-sensing device is the power management unit (PMU), being LDO voltage regulators the key constituting blocks. Voltage regulators generate, from the input battery voltage V_{bat}, a stable, low-noise and accurate output voltage V_{out} under variations of load and input voltage, as shown in Figure 2.1.



(a) *(b)*

Figure 2.1. a) Discharge curve of a battery under a constant load current, and b) Block diagram for a typical power management unit.

Table 2.1. Comparison between linear and switched regulators [1].

Linear regulators	Switched regulators
Limited output range ($V_{out} < V_{in}$)	Flexible output range ($V_{out} \leq V_{in}$) or ($V_{out} \geq V_{in}$)
Simple circuit	Complex circuit
Low noise content	High noise content
Fast response	Slow response
Limited energy efficiency ($\eta < V_{out}/V_{in}$)	High energy efficiency ($\eta \approx 80 – 95\%$)
Low power applications	High power applications

In general, voltage regulators can be classified into two categories, named switched and linear regulators. Their main characteristics are summarized in Table 2.1. Although switched regulators are more efficient, linear regulators are simpler; they present a regulated output with less noise and exhibit a shorter dynamic response due to their operating principle: the output voltage is controled by continuously adjusting the voltage drop on a pass element, which is connected in series between the unregulated input and the load. This, in turn, makes the output voltage, V_{out}, always lower than the input, V_{in}, so they are only efficient for low power, that is, with low supply voltage and reduced current demand [1].

Linear regulators can be classified according to the minimum operational voltage difference between the unregulated input and the regulated output, also called the dropout voltage, V_{do}. The so-called LDO regulator, with $V_{do} < 500$ mV [2], presents better efficiency so that the set of aforementioned benefits makes this choice the preferred solution in portable SoC applications powered by batteries.

Thus, this chapter presents the design and characterization of a fully integrated LDO [3-5]. It must provide, from a battery -that is a short-lived source of energy delivering a decreasing voltage level as it discharges over time- a stable, low-noise, accurate and load-independent power supply voltage for the whole multichannel sensing system conforming our IS-micro-instrument.

The achievement of a SoC design precludes the use of conventional LDOs, which rely on a μF-range off-chip capacitor at the output to both guarantee stability and minimize output voltage variations in the transient response. Besides, to prolong the battery cycle, operation with low quiescent currents is necessary. Nevertheless, low quiescent currents unavoidably slows down the LDO transient responses. Therefore, the design of on-chip capacitor-less LDO regulators requires alternative compensation schemes and transient response enhancement techniques to allow greater integration capabilities without degrading the overall performances in terms of regulation, size and power efficiency, a real challenge since tradeoffs between these parameters are interrelated.

To provide a deep insight into the theory and design of LDOs, the most important parameters that characterize a LDO regulator are firstly reviewed. Next, the basic CMOS topology of a LDO regulator is analysed, showing its basic scheme and operation principle. Then, the design and characterization of the proposed 1.8 V LDO regulator for the battery-

operated SoC solution-sensing device is presented and validated within a 10-channel microinstrument architecture to show its correct functionality. Finally, conclusions are drawn, comparing the achieved performance results with previously reported works.

A 1.2 V low voltage LDO version has been also designed [6, 7], to show the feasibility of the proposed design techniques for reduced supply voltages.

2.1. LDO CHARACTERISTIC PARAMETERS

The main parameters that define the behaviour of a low dropout regulator can be classified in static, dynamic and frequency specifications [2].

2.1.1. Static

The static specifications characterize the stationary behaviour. Basic metrics are the input voltage, output voltage, dropout voltage, load current, quiescent current, efficiency, line and load regulation and temperature dependence.

Input voltage, V_{in}. Range of input voltages, generally provided by batteries in portable applications (V_{bat}), for which the output voltage is constant.

Output voltage, V_{out}. Regulated output voltage value. It must be stable, low-noise and independent of the temperature, the input voltage and the current demanded by the load.

Dropout voltage, V_{do}. Difference between the minimum input voltage –from which the circuit is able to regulate the output voltage within the specifications– and the regulated output voltage, $V_{do} = V_{in,min} - V_{out}$.

Load current, I_{Load}. Output current provided by the LDO on demand of the circuit it supplies. Normally, the maximum value of load current preserving the output voltage in the regulation region is specified.

Quiescent current, I_q. Current consumed by the regulator when there is no system connected to the output, that is, with $I_{Load} = 0$ mA.

Efficiency, η. The value of the parameters described above determine the efficiency of the regulator, defined as the quotient between the demanded power (P_{Load}) and the supplied power (P_{Source}), that is,

$$\eta = \frac{P_{Load}}{P_{Source}} = \frac{V_{out} I_{Load}}{V_{in}\left(I_{Load} + I_q\right)} \leq \left(1 - \frac{V_{do}}{V_{in}}\right) \frac{I_{Load}}{\left(I_{Load} + I_q\right)} \tag{2.1}$$

Taking into account that $V_{out} = V_{in} - V_{do}$, the previous relationship results and to improve the efficiency, both the dropout voltage and the quiescent current must be minimized.

Load regulation, LDR. Determines the capacity of the regulator to keep the specified output voltage constant under different load conditions. It is defined as the variation in the output voltage, ΔV_{out}, for a quasi-static variation on the load current, ΔI_{Load}, and typically it is specified in mV/mA or %/mA according to

$$LDR = \frac{\Delta V_{out}}{\Delta I_{Load}}\ (mV/mA) \qquad LDR = 100\frac{\Delta V_{out}}{\Delta I_{Load}}\frac{1}{V_{out}}\ (\%/mA) \qquad (2.2)$$

Line regulation, LNR. Determines the capacity of the circuit to keep the specified output voltage constant over the input voltage range. It is defined as the variation in the output voltage, ΔV_{out}, for a quasi-static change in the input voltage, ΔV_{in}, and typically it is specified in mV/V or %/V according to

$$LNR = \frac{\Delta V_{out}}{\Delta V_{in}}\ (mV/V) \qquad LNR = 100\frac{\Delta V_{out}}{\Delta V_{in}}\frac{1}{V_{out}}\ (\%/V) \qquad (2.3)$$

Lastly, it must be noted that the output voltage, the quiescent current and the load and line regulation usually exhibit temperature dependence, so it is also important to know their variation in the operating temperature range.

2.1.2. Dynamic

The dynamic specifications characterize the transient behaviour of the LDO regulator in the face of sudden changes at the load current or at the input supply voltage. Therefore, load and line transient regulations are considered the basic dynamic metrics.

Load transient regulation. It is the response of the regulator to a step change in the load current (Figure 2.2a). It is specified through the voltage difference, $\Delta V_{tr,max}$, between the peak voltage (minimum for transitions $I_{Load,min} \rightarrow I_{Load,max}$; maximum for transitions $I_{Load,max} \rightarrow I_{Load,min}$) and the stabilized V_{out}, which are respectively called udershoot (US) and overshoot (OS) [8], and their corresponding settling times, t_s, that is, the time that elapses, from the moment the transition starts until the output voltage stabilizes whitin a certain margin of error.

Line transient regulation. It is the response of the regulator to a step change in the input voltage (Figure 2.2b). Analogous to the load transient regulation, the line transient regulation is specified by parametrizing the overshoot in the transition $V_{in,min} \rightarrow V_{in,max}$, the undershoot in the transition $V_{in,max} \rightarrow V_{in,min}$, and the related settling times, t_s.

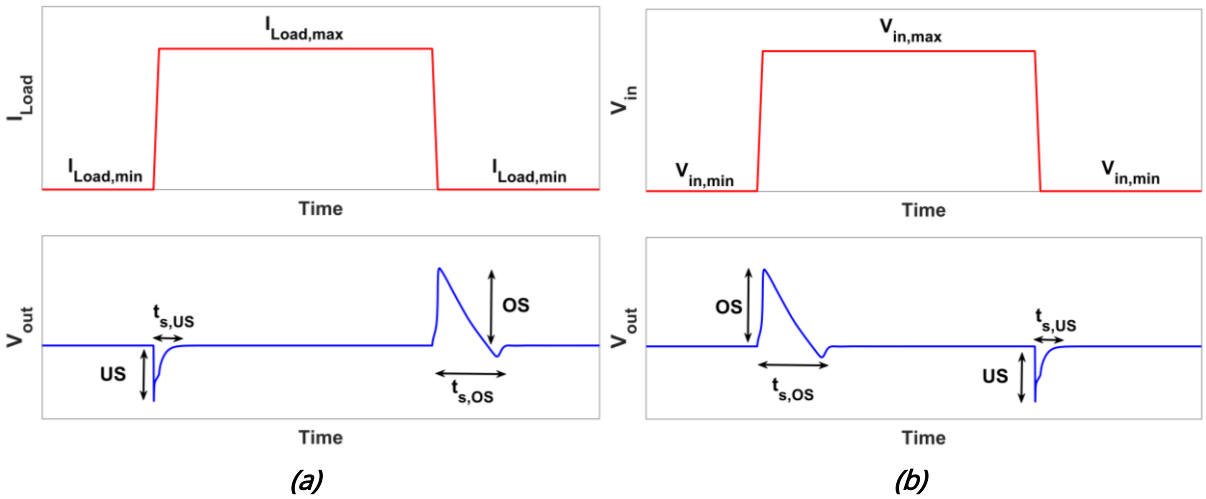


Figure 2.2. Typical transient a) load regulation; and b) line regulation.

The peaks at the output voltage and the settling time affect the precission of the regulator output, degenerating the output voltage V_{out}. Therefore, a good transient response must be ensured with small V_{out} variations and reduced settling times. Since non-linear phenomena intervene, it is difficult to obtain analytical expressions for these voltage peaks and settling times. Still, there are a series of factors that affect the transient response of a LDO [9, 10]: in addition to its frequency response, the transient performance is mainly influenced by the system ability to charge/discharge the parasitic capacitances, i.e., by the slew-rate at the critical system nodes.

2.1.3. Frequency

Included here is the power supply rejection as basic metric.

Power Supply Rejection, PSR. Measures the ability of the LDO regulator to prevent the regulated output voltage from fluctuating due to a rippled input signal. The same relationship that applies to line regulation is applied to PSR but considering the entire frequency spectrum. It is defined as

$$PSR = |20\log_{10}(V_{out}/V_{in})|(dB) \tag{2.4}$$

2.2. CMOS Low Dropout Regulator

The basic scheme of a linear regulator, which provides a regulated voltage V_{out} from an unregulated input voltage V_{in} is shown in Figure 2.3 [1]. A sampling circuit is responsible for sensing the variations of the output voltage, due to changes in the power supply or in the load current. An error amplifier (EA) compares the difference between this signal and a reference voltage, and drives the control pass element, which makes the necessary modifications to obtain the desired voltage at the output.

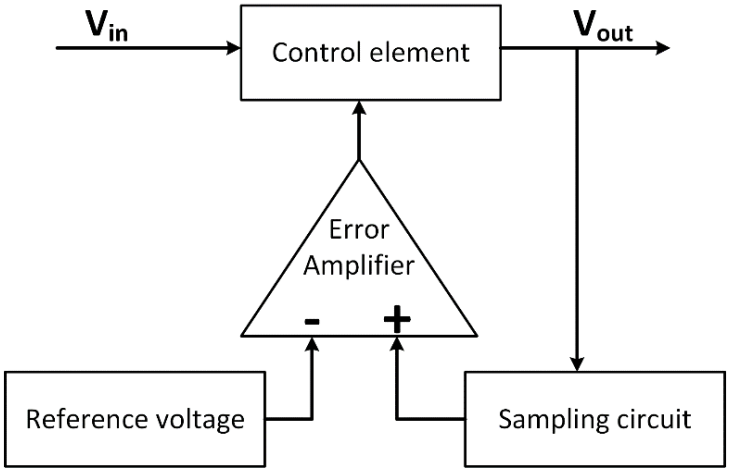


Figure 2.3. Conceptual scheme of a linear regulator.

Figure 2.4 shows the typical topology of a CMOS LDO regulator, which uses a PMOS transistor as the control pass element to minimize the dropout V_{do}, given by

$$V_{do,PMOS} = V_{sd,sat} \tag{2.5}$$

while if an NMOS transistor were to be used as the pass element, the dropout is given by

$$V_{do,NMOS} = V_{gs} + V_{ds,sat} \tag{2.6}$$

Increasing the dropout voltage and therefore decreasing the efficiency of the LDO.

A resistive network R_{fb1} – R_{fb2} is used as the sampling circuit This negative feedback resistive network samples the output voltage V_{out} through V_{fb}, which is compared with the reference voltage, V_{ref}. The difference is amplified by means of an EA and applied to the gate of the PMOS transistor, V_g, which keeps the desired output voltage constant regardless of the variations in the supply voltage, V_{in}, and the current required by the load –modelled through R_{Load} and C_{Load}–. Assuming an ideal error amplifier, the output voltage is given by

$$V_{out} = \left(1 + \frac{R_{fb1}}{R_{fb2}}\right) V_{ref} \tag{2.7}$$

Qualitatively, if the load current increases, the output voltage increases, and therefore, the V_{fb} voltage increases. Thus, the difference $(V_+ - V_-) = (V_{fb} - V_{ref})$ increases, and so does the gate voltage, V_g of the PMOS pass transistor. Therefore, its source-gate voltage, V_{sg}, decreases and, as a result, the current provided by the pass transistor decreases, decreasing the output voltage, bringing about regulation. If the load current decreases, the behaviour is analogous.

If the variation is produced in V_{bat}, the qualitative analysis is as follows. If V_{bat} increases, the source-gate voltage of the PMOS pass transistor, V_{sg}, increases and, as a result, the current provided by the pass transistor increases, increasing the output voltage, and therefore, the V_{fb} voltage increases. Thus, the difference $(V_+ - V_-) = (V_{fb} - V_{ref})$ increases, and so does the gate voltage, V_g. Therefore, V_{sg} decreases and, as a result, V_{bat} decreases, bringing stability to the system. A similar process happens if the battery supply decreases.

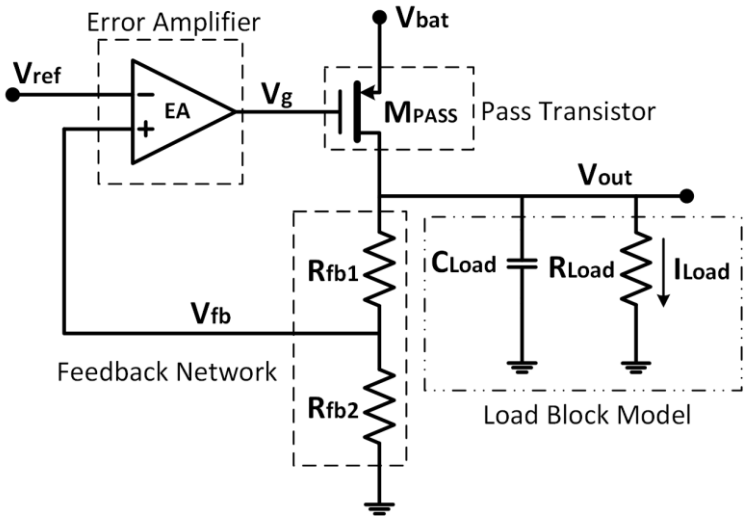


Figure 2.4. Basic topology of a LDO regulator with a PMOS transistor as the pass element.

Based on this architecture, design guidelines are to optimize the size and especially the power consumption to satisfy the critical constraints of portable on chip devices, while keeping a suitable regulating performance for our specifications: regulated output voltage V_{out} = 1.8 V for battery-compatible input voltages V_{bat} = 3.6 V–2.1 V, with a 300 mV dropout voltage, V_{do} and a maximum load current of 50 mA over a 100 pF maximum capacitive load.

This means that internal compensation is required to attain a fully integrated solution that minimizes size and cost. Besides, high precision regulation requires the use of high open loop gain error amplifiers since both line and load regulation are inversely dependent on the amplifier gain, $1/A_{EA}$, as derived from the following small signal equations obtained for load regulation and line regulation, respectively:

$$\frac{\Delta V_{out}}{\Delta I_{Load}} \approx -\frac{1}{g_{m_P} A_{EA}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \tag{2.8}$$

$$\frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{1}{A_{EA}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \tag{2.9}$$

with g_{mP} the transconductance of the pass transistor M_{PASS} and A_{EA} the open loop gain of the EA. The detailed calculus of these expressions are included in Appendix II.

To set a gain specification, the nominal value necessary to maintain the voltage V_{out} at 1.8 V with an error below 0.1 % is determined by simulation, using an ideal model for the EA –a voltage-controlled voltage source–, obtaining a minimum voltage gain of 60 dB. Furthermore, it must operate correctly over the entire range of input voltages (2.1 V - 3.6 V) with a C_{Load} of 12 pF to 20 pF corresponding to the C_{gs} capacity of M_{PASS} when operating at minimum and maximum load current capabilities.

To implement a high gain Error Amplifier with a low-level voltage supply, a multi-stage EA is typically used. However, this implies, typically a more complex architecture with higher consumption than a single-stage EA, while the necessary compensation network

of a fully integrated LDO with a multi-stage amplifier is not trivial, requiring advanced compensation techniques, such as damping factor control **[11]**, Q-reduction **[12]** or enhanced multipath nested Miller **[13]**. Therefore, to minimize size, power and simplify the LDO compensation a single-stage EA is used, based on a telescopic approach to preserve a gain high-enough to render good regulating performance.

The LDO regulator topology shown in Figure 2.4 with a single-stage telescopic Operational Transconductance Amplifier (OTA) as EA, presents two main poles as shown in Figure 2.5. The OTA high output resistance, R_{oa}, together with the parasitic $C_{gs,P}$ of the pass transistor, also high – M_{PASS} has to withstand high load currents -up to 50 mA, which requires high dimensions– make the dominant pole P_{EA} be located at the output node of the error amplifier,

$$f_{P_{EA}} = \frac{1}{R_{oa}\{C_{oa} + C_{gs} + C_{gd}(1 + A_{P_0})\}} \approx \frac{1}{2\pi} \frac{1}{R_{oa}(C_{oa} \parallel C_{gs_P})} \approx \frac{1}{2\pi} \frac{1}{R_{oa} C_{gs_P}} \tag{2.10}$$

Were $A_{P0}=A_p(s=0)=g_{mP}\{(R_{fb1}+R_{fb2})//R_{oP}//R_{Load}\}=g_{mP}R_{eq.}$

The non-dominant pole, P_{OUT}, is located at the output of the regulator,

$$f_{P_{OUT}} \approx \frac{1}{2\pi} \frac{1}{R_{Load} C_{Load}} = \frac{1}{2\pi} \frac{I_{Load}}{V_{out} C_{Load}} \tag{2.11}$$

From equation (2.11), it is clear that as the load current increases, P_{OUT} increases moving away towards higher frequencies, while for low currents, P_{OUT} approaches low frequencies, degrading the stability of the system. A more detailed analysis of the frequency response can be found in Appendix III.

Therefore, to ensure stability throughout the load current range, it must be verified that there is enough Phase Margin (PM) for the loop gain V_{fb}/V_+ (Figure 2.6a) at unity gain frequency (UGF), establishing a PM ≥ 60º as a stability criterion in our design. Figure 2.6b shows the response for a LDO characterized by poles (2.10) and (2.11) in the cases of $I_{Load,max}$ (stable system, with PM ≈ 90º@UGF) and $I_{Load,min}$ = 0 mA (PM degradation, which may make the system unstable).

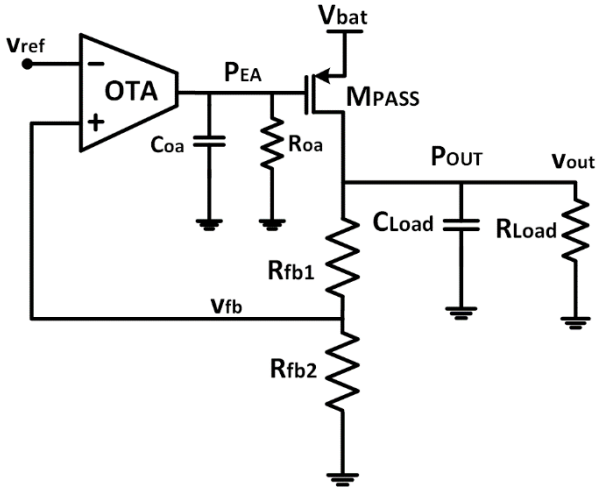


Figure 2.5. LDO regulator scheme with two poles (single stage OTA).

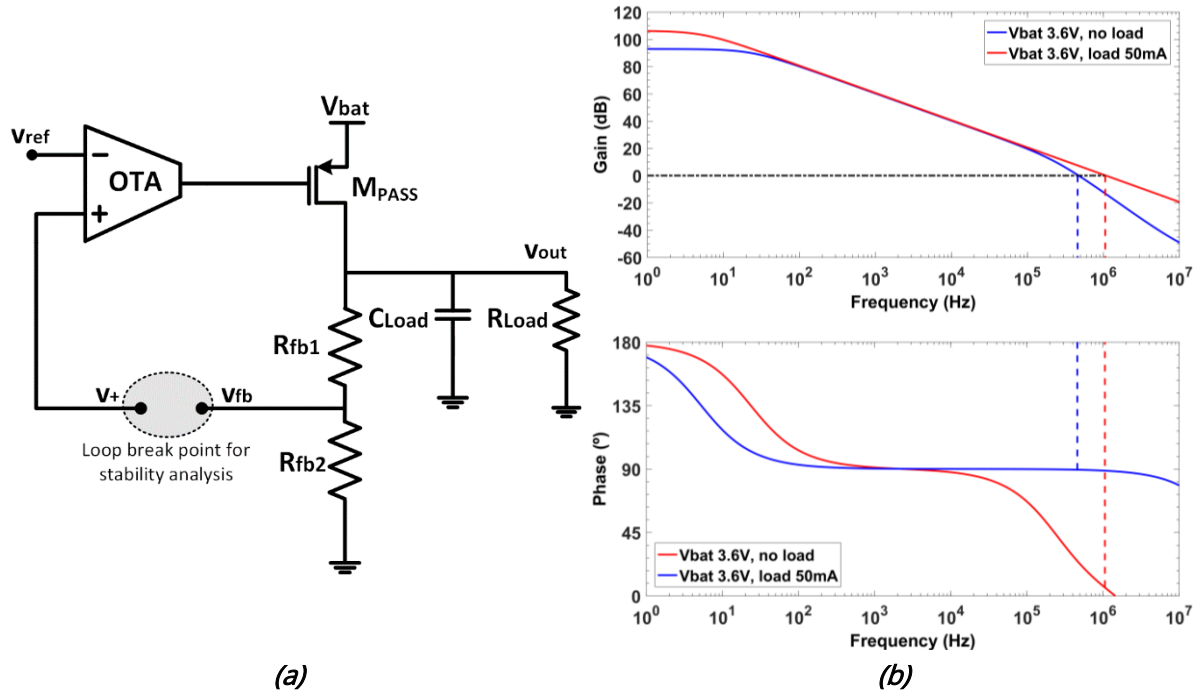


Figure 2.6. Stability analysis: a) scheme, and b) frequency response for I_{Load} = min & max.

Moreover, the PSR largely depends on the loop feedback gain [**14**], given, at low frequency, by

$$A_{fb} = \frac{A_{EA}}{\left(1 + s/\omega_{P\,EA}\right)} \frac{R_{fb2}}{R_{fb1} + R_{fb2}} \tag{2.12}$$

Since A_{EA} is high, the low frequency supply rejection should be good. However, beyond the frequency of the error amplifier pole ωp_{EA}, the feedback gain reduces and the PSR consequently degrades.

Besides reliable on-chip compensation, the mandatory operation with low quiescent current to mimimize power consumption will slow down the LDO transient response, dominated by the slew-rate characteristic at the gate of the pass transistor. To overcome this trade-off between power consumption (low quiescent current) and transient response, different techniques have been proposed, but they involve increasing the current and the circuit complexity of the resulting topology, thus degrading the power efficiency. For instance, the LDOs in **[15, 16]** use current Miller amplification, i.e., a current amplifier in series with a capacitor that creates an auxiliary fast loop both to improve the transient response and to achieve internal frequency compensation. Adaptive techniques detect load variations through a relatively small current sensing transistor in parallel with the power pass transistor. It generates a scaled copy of I_{Load}, that is next adequately injected directly at the gate of the pass transistor **[17]** or added to the bias current of the error amplifier, which is thus biased with a small fixed bias current plus an adaptive bias current proportional to I_{Load} **[18, 19]**. The associated circuit topology is simple, and thus compact. However, the transient improvement is only effective during transitions from low to high currents, but not for the opposite conversion, while the quiescent current becomes proportional to I_{Load}, increasing when the LDO is active. Alternatively, dynamic techniques rely on the employment of auxiliary current boosting paths to improve the

transient behavior, which are only active during transient periods but that remain off in steady state. Therefore, the system can operate with reduced quiescent current, and the charging/discharging current at the gate of the power transistor [10] or the biasing current of the error amplifier are increased just momentarily during transients [20-22]. As the dynamic technique exhibits better current efficiency, this approach will be adopted to achieve an internally compensated LDO regulator with enhanced time response thanks to the introduction of a novel dynamic current boosting bias circuit (CBBC).

Therefore, based on all the above, the challenge faced in the design of a fully integrated CMOS LDO regulator is to achieve stability with reasonable on-chip compensation capacitance and minimum quiescent current while exhibiting good static regulating performance, fast transient behaviour and minimum size since tradeoffs between these parameters are interrelated.

2.3. 1.8V-LDO REGULATOR

This section presents the design and experimental characterization of a low dropout regulator in a 180 nm CMOS technology providing an output voltage of 1.8 V from a 3.6 V – 2.1 V battery voltage, with a maximum load current of 50 mA over a maximum capacitive load of 100 pF. [23, 24].

We have adopted a strategy that relies on using the simplest high-gain error amplifier, a telescopic OTA structure, to achieve good regulating performance while simplifying stability to a two-pole case, with a minimum-area minimum-quiescent current solution, our two critical design requirements.

The combination of a low load capacitor in the LDO output node and the use of low quiescent currents to drive the large capacitor C_g at the gate of the power transistor overall results in voltage peaks and large settling times for the transient response. To improve this transient behaviour without jeopardizing the quiescent current, a dynamic CBBC is employed.

2.3.1. Design

Based on the fundamental topology of a CMOS LDO regulator (Figure 2.4), the proposed fully integrated internally compensated LDO voltage regulator is shown in Figure 2.7. The voltage reference V_{ref} is an external 1.2 V reference.

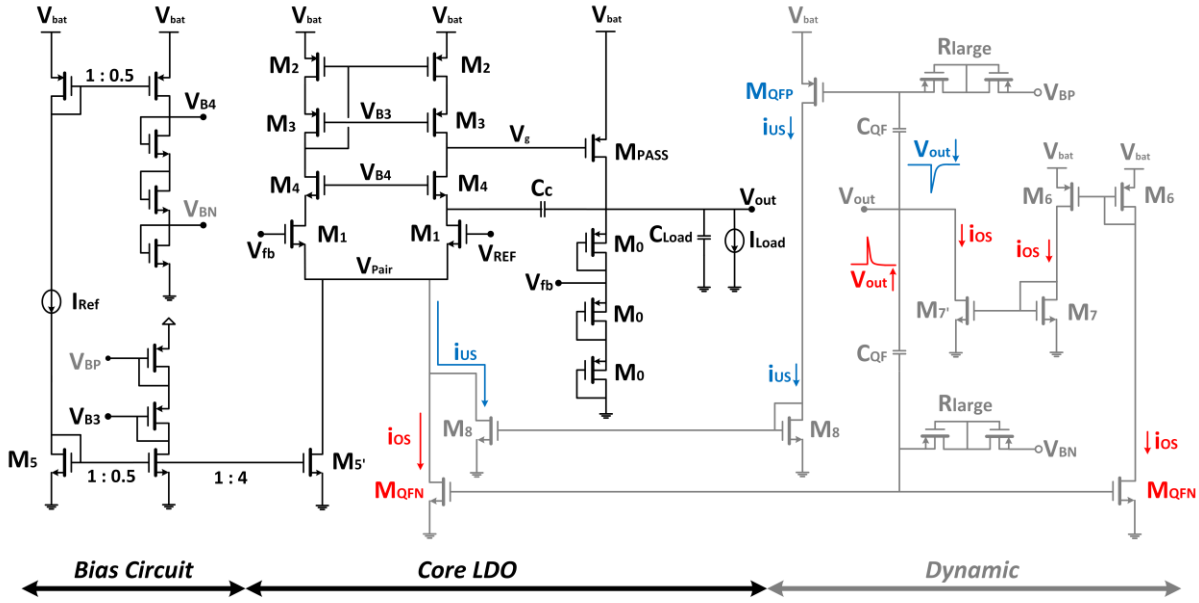


Figure 2.7. Schematic of the proposed CMOS LDO regulator.

LDO Core

Considering our design specifications V_{ref} = 1.2 V; V_{out} = 1.8 V from equation (2.7) and assuming a static current of 4 µA flowing through resistances R_{fb1}–R_{fb2} when I_{Load} = 0 mA ($I_{fb} = V_{out}/(R_{fb1} + R_{fb2})$ = 4 µA) as a tradeoff between low power consumption and moderate resistance values, it results R_{fb1} = 150 kΩ and R_{fb2} = 300 kΩ. They are implemented as active resistances using three identical PMOS transistors in diode configuration (M0 size 8 µm/1 µm, Figure 2.7) instead of as passive resistances to optimize area.

The size of the PMOS pass transistor is set to 9 mm/340 nm to guarantee operation in saturation, in the first order of approximation, for the maximum load current (50 mA) preserving a dropout voltage of $V_{do} = V_{DS,MPASS}$ = 300 mV. Minimum transistor length (L = 0.34 µm for 3.3 V MOS transistors) is used to reduce the parasitic capacitance at the pass transistor gate: C_g ~12 pF (no load) and ~20 pF (maximum load).

The EA is a telescopic NMOS input differential pair OTA, which provides high gain — comparable to that of a two-stage topology— with the simplest single-stage OTA. In this way, high precision regulation can be achieved minimizing power consumption and relaxing the system stability. It drains a total current consumption of 2.5 µA (2 µA for the differential pair plus 0.5 µA to generate the cascode bias voltages V_{B3} and V_{B4} through diode-connected transistors). Its DC gain A_{EA} is above 97 dB over the nominal battery supply operating range (2.1 V–3.6 V), and it renders a gain-bandwidth product GBW > 149 kHz with a phase margin PM = 89.6º considering a load capacitance equal to C_g. Transistor sizes in (µm/µm) of the error amplifier are M1 = 4/1, M2 = 12/1, M3 = 12/1, M4 = 4/1, M5 = 6/2, M5' = 24/2. 3.3 V nominal voltage transistors are used to properly support the input voltages.

Stability

From equation (2.11) it can be seen that for high load currents, P_{OUT} increases moving towards higher frequencies and renders a stable system, but for low load currents it gets closer to the dominant pole, reducing the phase margin below the limit that guarantees stability. Thus, a cascode compensation technique, using a single C_C = 9.5 pF Metal-Isolator-Metal (MIM) capacitor (Figure 2.7) is adopted preserving a phase margin PM above 60° (Figure 2.8). The dominant pole, P_{EA}' is now given by

$$f'_{P_{EA}} \approx \frac{1}{2\pi} \frac{1}{R_{oa}\{C_{oa} + C_{gs,P} + (C_{gd} + C_c)(1 + A_{P_0})\}} \approx \frac{1}{2\pi} \frac{1}{R_{oa}(C_{gs,P} + C_c)} \qquad (2.13)$$

This approach has been preferred over the classical Miller compensation technique, which requires a C_c = 11 pF, R_c = 17.5 kΩ network to attain the same 60° phase margin at I_{Load} = 0 mA; besides, the Miller solution exhibits an overcompensated phase margin response for high load currents (Figure 2.9).

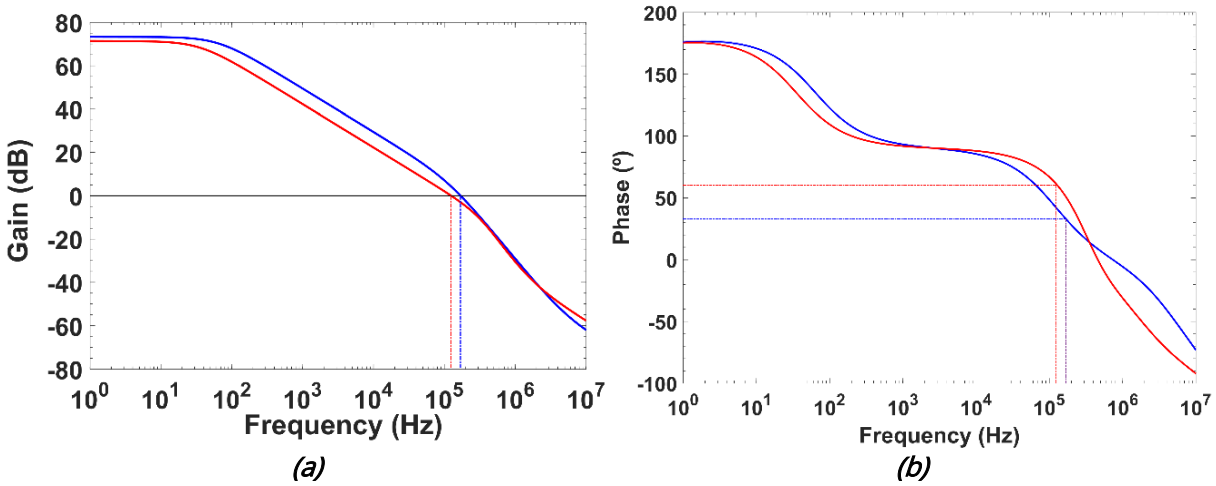


Figure 2.8. Simulated stability behaviour with (red) and without (blue) cascode compensation for I_{Load} = 0 mA, V_{bat} = 2.1 V: a) gain; and b) phase margin.

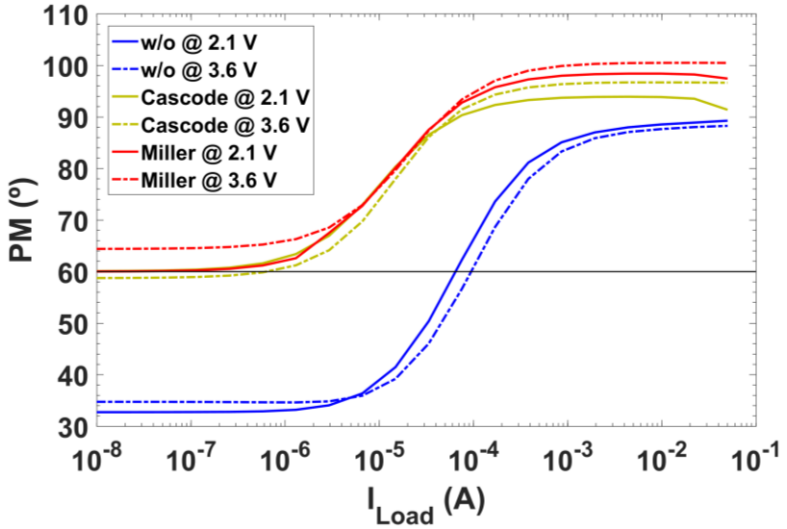


Figure 2.9. Simulated phase margin versus load current for: Cascode compensation (C_c = 9.5 pF), Miller compensation (C_c = 11 pF, R_c = 17.5 kΩ) and without compensation.

Transient Response

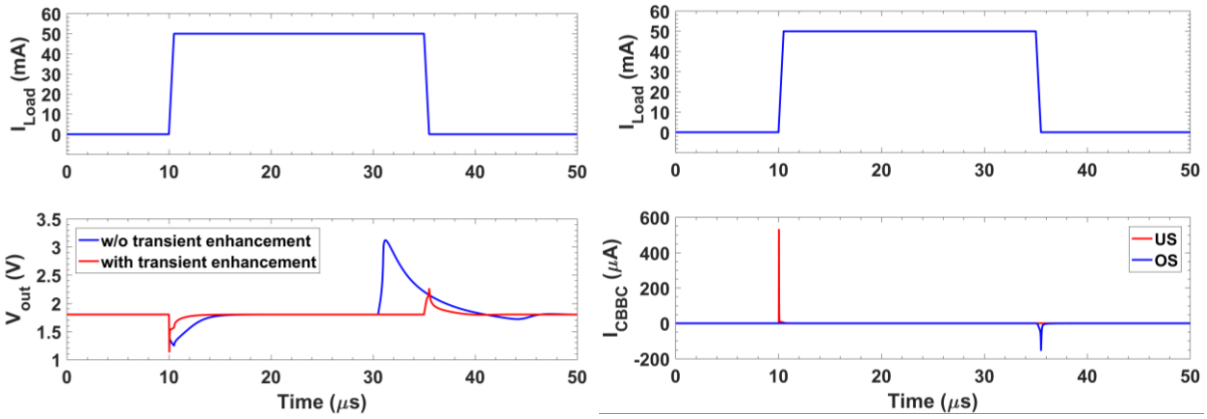
Once the LDO is stable, its load transient characterization reveals poor dynamic performance (Figure 2.10), as expected due to its low quiescent current. Therefore, a dynamic CBBC is proposed. Shown in grey in Figure 2.7, it consists of undershoot/overshoot detection circuits, with the corresponding US/OS driving circuits.

The US detection circuit is a quasi-floating gate PMOS transistor M_{QFP}. Its gate voltage is tied to a DC biasing voltage V_{BP} through large resistive elements R_{Large} –implemented using two series reverse biased PMOS diodes– and to the output node through a small valued MIM capacitor C_{QF} = 1 pF. In this way, under quiescent conditions, the M_{QFP} gate voltage takes the value V_{BP}, which is fixed to a value $V_{SG} = (V_{bat} - V_{BP})$ = 350 mV < $|V_{Th,P}|$ = 0.72 V that keeps M_{QFP} in the cut-off region. When the output voltage suddenly decreases, capacitor C_{QF} transfers the output voltage undershoot to the M_{QFP} gate, making $V_{SG} > |V_{Th,P}|$ and the transistor enters the on region. The generated current is copied through the current mirror M8, adding extra bias current to the error amplifier that speeds the discharge of capacitance C_g (Figure 2.10). When V_{out} is approximately regulated back to its nominal value, M_{QFP} returns to the off region.

Similarly, the OS detection circuit is a quasi-floating gate NMOS transistor M_{QFN}, with the gate voltage set to a DC biasing voltage $V_{GS} = V_{BN}$ = 300 mV < $V_{Th,N}$ = 0.59 V through R_{Large}, and connected to the output node through C_{QF}. In steady state, M_{QFN} is off, but when the output voltage suddenly increases, the overshoot will couple through C_{QF}, triggering on the transistor. The generated current is added to the bias current of the EA (Figure 2.10), helping to charge the gate capacitance C_g and, as a result, V_g is increased to reduce I_{Load}. Besides, M_{QFN} is replicated and the current mirror M6-M7-M7' sinks extra current at the output, helping to discharge the path formed by ($R_{fb1} + R_{fb2}$) and C_{Load}.

Both V_{BP} and V_{BN} are generated from the same bias branches used to generate the cascode bias voltages to add no extra current. Therefore, the total quiescent current in steady state is only 7 µA (0.5 µA from the reference current I_{ref} + 4 µA from the feedback network +2 µA from the EA + 0.5 µA to generate all biasing voltages). Transistor sizes in (µm/µm) of the transient enhancement circuits are M_{QFN} = 60/0.34, M_{QFP} = 180/0.34, M6 = 5/0.34, M7 = 5/0.34, M7' = 20/0.34.

Over other proposals based on the dynamic technique [20-22, 25], this scheme manages to work with no additional quiescent current and minimal additional circuitry, thus resulting in an ultralow power LDO with very competitive static and dynamic regulating performances.

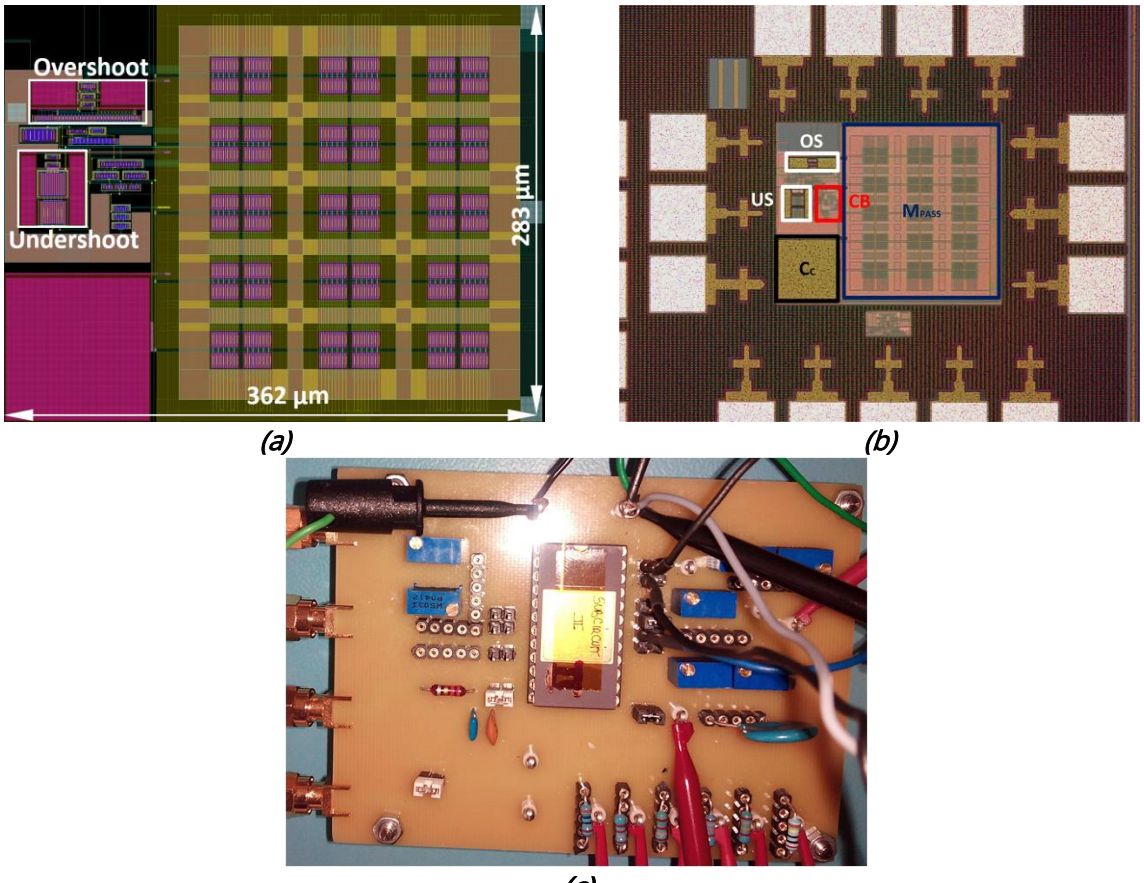


(a) *(b)*

Figure 2.10. Dynamic transient response for a load transition (@ V_{bat} = 3.6 V). a) Output voltage with and w/o CBBC; b) OS and US currents generated by the CBBC circuit to stabilice the system faster.

2.3.2. Characterization

Figure 2.11a and Figure 2.11b shows respectively the layout view and the microphotograph of the integrated LDO regulator. Its active area is 362 x 283 μm^2, mostly occupied by the power PMOS transistor. A specific Printed Circuit Board (PCB) was designed (Figure 2.11b) to complete its static, dynamic and high frequency (PSR) characterization.



(a) *(b)*

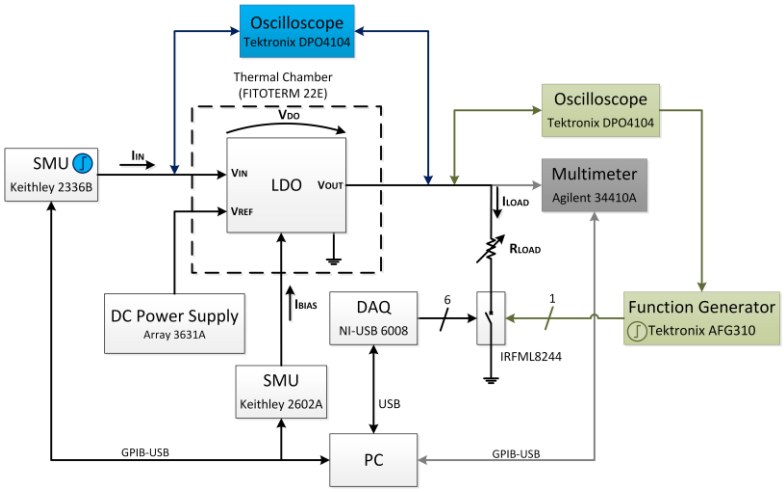
(c)

Figure 2.11. Detail of the integrated LDO regulator a) Layout view, b) microphotograph (CB: Core (without M_{PASS}) + bias) and c) PCB test.

Static Behaviour

Figure 2.12 shows the measurement setup (Figure 2.12a shows the block diagram and Figure 2.12b shows a photograph of the experimental setup) for the characterization of the main static parameters: V_{bat}–V_{out} characteristic and dropout voltage, quiescent current, line regulation LNR (circuit capacity to keep the specified output voltage in the range of input voltages) and load regulation LDR (circuit capacity to keep the specified output voltage under different load conditions). A DC Power Supply 3631A sets the 1.2 V reference voltage. To emulate different load currents (0 A, 1 µA, 10 µA, 100 µA, 1 mA, 10 mA and 50 mA), an array of six commuted resistances placed at the output of the LDO are used. Each of them is activated through a series low impedance NMOS transistor IRFML8244 ($R_{DS(on),max}$ = 41 mΩ) acting as a switch with the gate connected to the digital outputs of a Data Acquisition Card (DAQ) USB-6008.

Firstly, a DPO4104 Oscilloscope is used to corroborate the proper behaviour of the integrated LDO. Figure 2.13a shows the static V_{bat}–V_{out} performance for I_{Load} = 50 mA. Secondly, automatized measurements were accomplished to perform a complete V_{bat}–V_{out} characterization over different load currents. The input voltage V_{bat} is provided by a Source Measure Unit 2336B (SMU) that allows, for each input V_{bat}, the simultaneous measurement of the quiescent current. The output voltage is measured with a Digital



(a)

(b)

Figure 2.12. Measurement setup for the complete characterization of the LDO regulator: a) Block diagram of static (grey), transient load regulation (green) and transient line regulation (blue); and b) Experimental setup.

Multimeter of 6 1/2 digits 34410A. Tests have been performed in a range of temperatures that spans from -40 °C to 100 °C in 20 °C steps, using a thermal chamber FITOTERM 22E. Figure 2.13b presents the obtained results, with a sweep of the supply voltage from 1.6 V to 3.6 V in 0.01 V steps, at room temperature (20 °C) for different load currents (from 0 mA to 50 mA). The LDO regulator provides a constant output voltage of 1.8 V for V_{bat} > 1.94 V (V_{do} = 140 mV) with an error < 4 % for the worst case, corresponding to maximum load current. Next, in the range of –40 °C – 100 °C in 20 °C steps, this same characteristic is measured for the most critical state, i.e. at maximum current. Results are shown in Figure 2.13c. The V_{do} remains over 140 mV and, in the linear region, the output voltage experiences a maximum variation of 20 mV over the 140 °C temperature range (~143 µV/°C).

The measured quiescent current of the system over V_{bat} is shown in Figure 2.14a. Its average value is 7.45 µA, with a negligible difference (~70 nA) between the minimum and maximum battery voltage. Figure 2.14b shows the quiescent current against the battery voltage range for different temperatures. The value is kept constant at each temperature over the battery supply, increasing at a rate of ~32 nA/C.

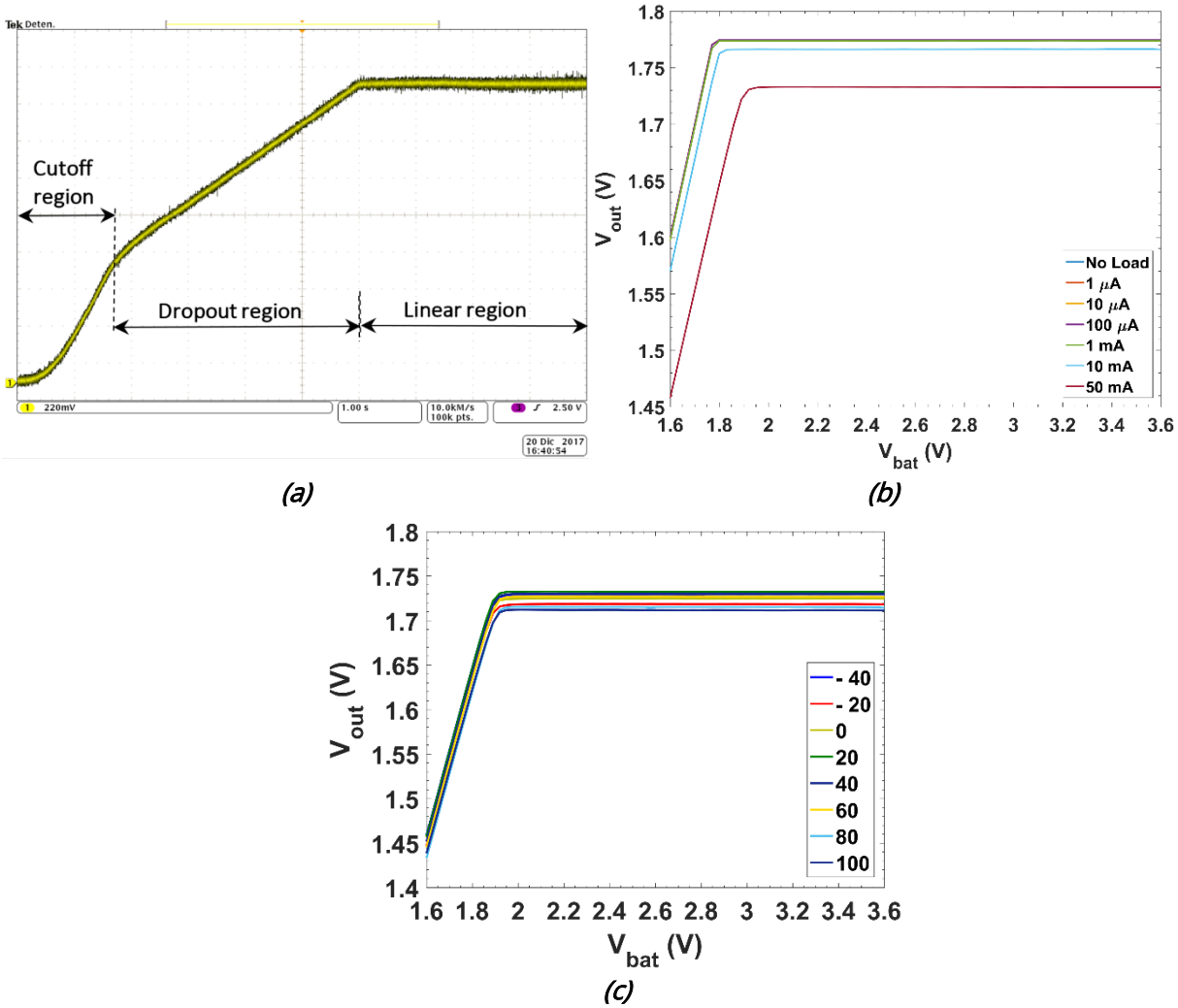
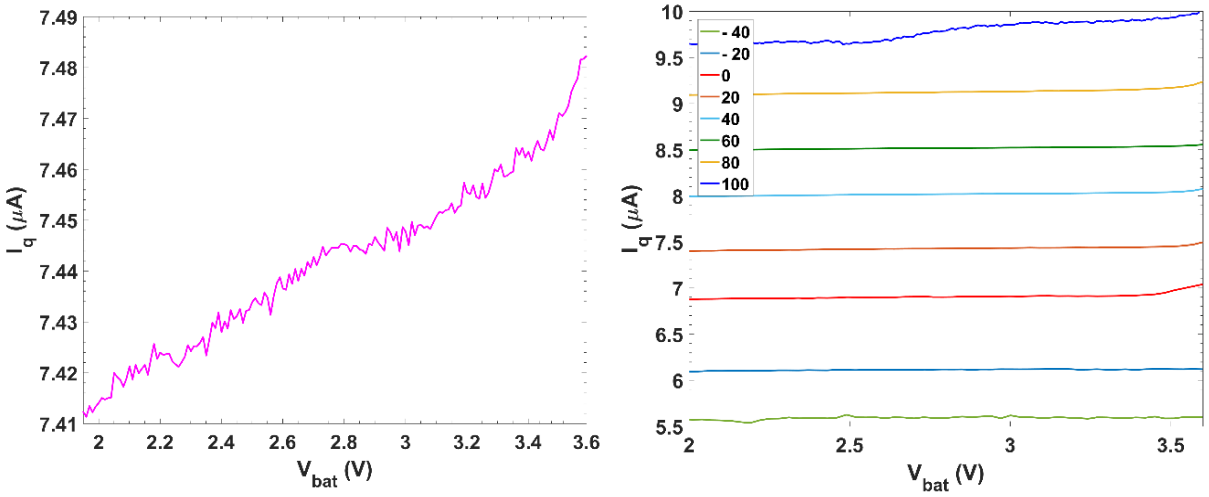
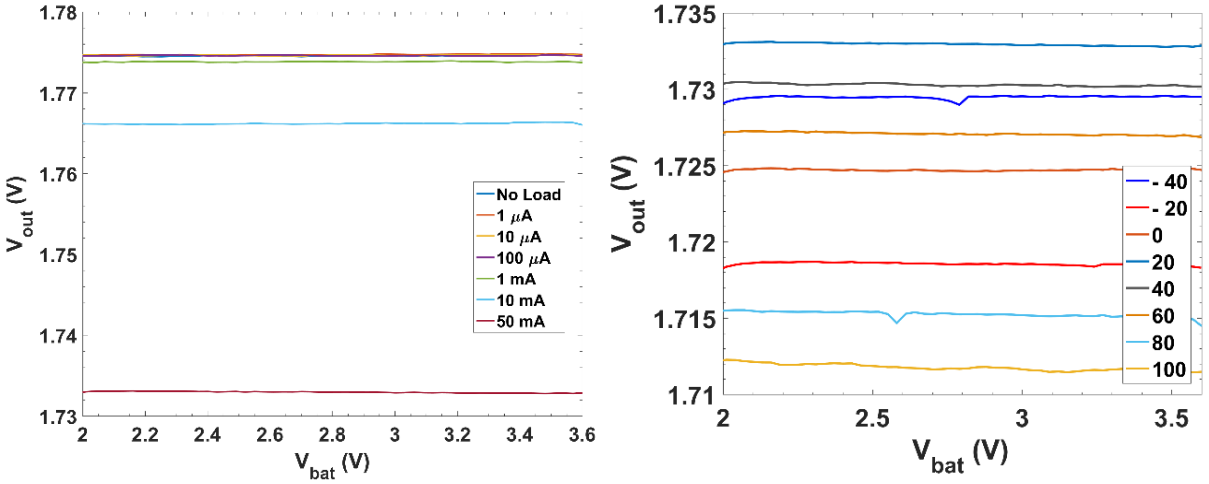


Figure 2.13. V_{in}–V_{out} characteristic: a) Oscilloscope caption at I_{Load} = 50 mA; b) different current loads; and (c) different temperatures with maximum load current (50 mA).



(a) *(b)*

Figure 2.14. Quiescent current at: a) room temperature; and b) over different temperatures.



(a) *(b)*

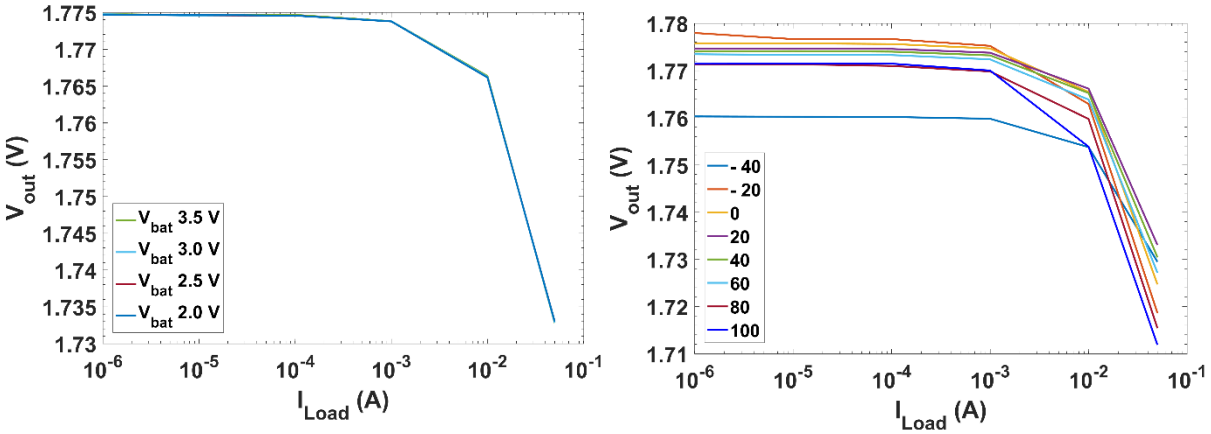
Figure 2.15. Line regulation characteristic, i.e., output voltage vs. input voltage: a) for different load currents; and b) for different temperatures under maximum load current condition.

Figure 2.15a presents the LNR performance (it is a zoomed version of Figure 2.13b in the LDO linear region). The variation of the output voltage through all the operating range for the worst case (I_{Load} = 50 mA) provides a LNR = 0.081 mV/V. Figure 2.15b presents the LNR behaviour over temperature for the worst case, I_{Load} = 50 mA. It provides a total variation of 98 μV/V°C.

Figure 2.16a presents the LDR performance for different input voltages within the operating range of the LDO regulator. The worst case (V_{bat} = 2.0 V) provides a LDR = –0.82 mV/mA. Figure 2.16b presents the LDR behaviour over temperature for the worst case, V_{bat} = 2.5 V. It provides a total variation of 970 nV/mA°C.

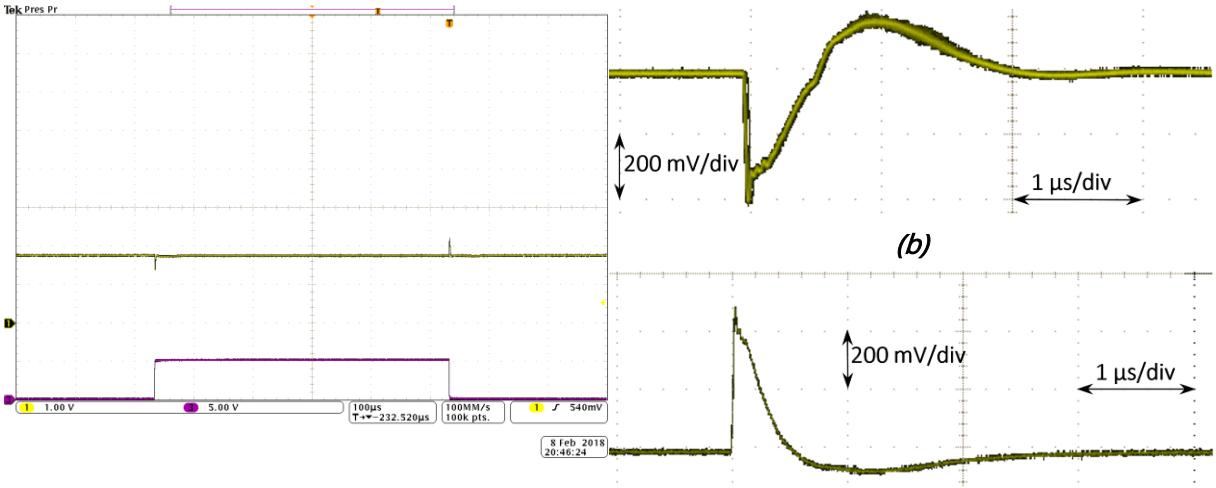
Dynamic Behaviour

The dynamic behaviour of the LDO regulator is tested at room temperature (T ~20 °C). To characterize the transient load regulation (Figure 2.12a, in green), the output voltage variation is measured for a current step from minimum to maximum load current, at a specific input voltage. That current step is generated by an AFG310 Arbitrary Function Generator used to provide a square signal that opens and closes the NMOS transistor



(a) *(b)*

Figure 2.16. Load regulation characteristic, i.e., output voltage vs. load current: a) for different input voltages; and b) for different temperatures with 2.5 V input voltage.



(a) *(b)* *(c)*

Figure 2.17. Load transient behaviour: a) with dynamic CBBC (green) output voltage and (purple) ON/OFF (50 mA/0 mA) of the switch that allows load current through; b) US zoomed image; and c) OS zoomed image.

switch connecting the output voltage with a load current of 50 mA, switching in this way from 0 mA to 50 mA.

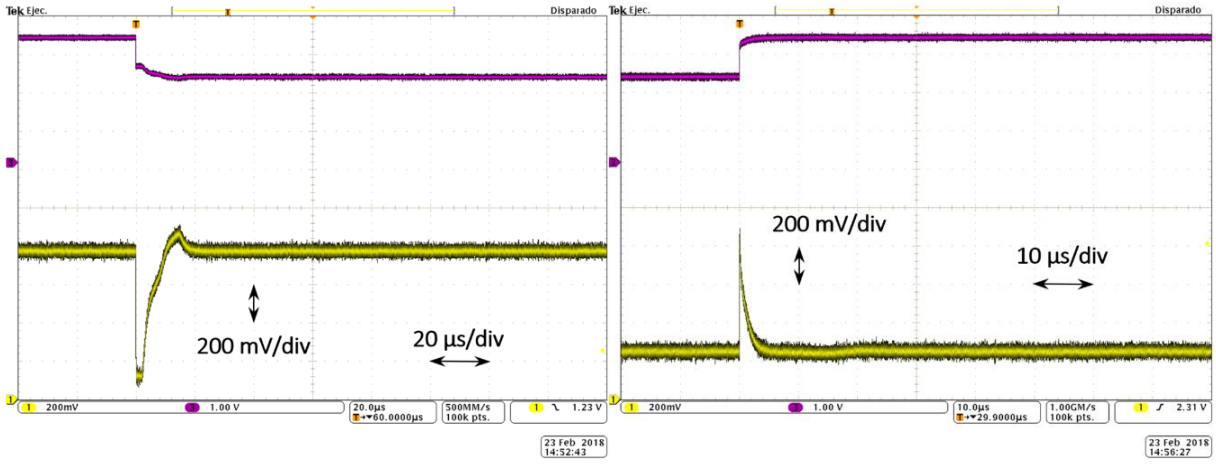
Figure 2.17a shows the oscilloscope screenshot for a current step from 0 mA to 50 mA (t_{rise} = 0.5 µs) with an input voltage of V_{bat} = 3.6 V. The regulated output voltage with the dynamic CBBC (Figure 2.17b) shows an OS/US of ~480 mV/~400 mV with settling times of 2.5 µs/2.0 µs, respectively. Compared to the transient load regulation without the dynamic enhancement circuit, it shows an improvement of two orders of magnitude in the settling times and an important reduction on the OS/US voltage variations.

Characterization of the transient line regulation (Figure 2.12a, in blue) sets an input voltage step within its linear range, at a specific load current. Figure 2.18 shows a screenshot of the transient line regulation for an input voltage step from 2.2 V to 3.2 V with a load current of 50 mA. The regulated output voltage shows an US (Figure 2.18a) of ~700 mV and a settling time of 20 µs, while the OS (Figure 2.18b) presents a voltage variation of ~600 mV and settling time of 4 µs.

Power Supply Rejection (PSR)

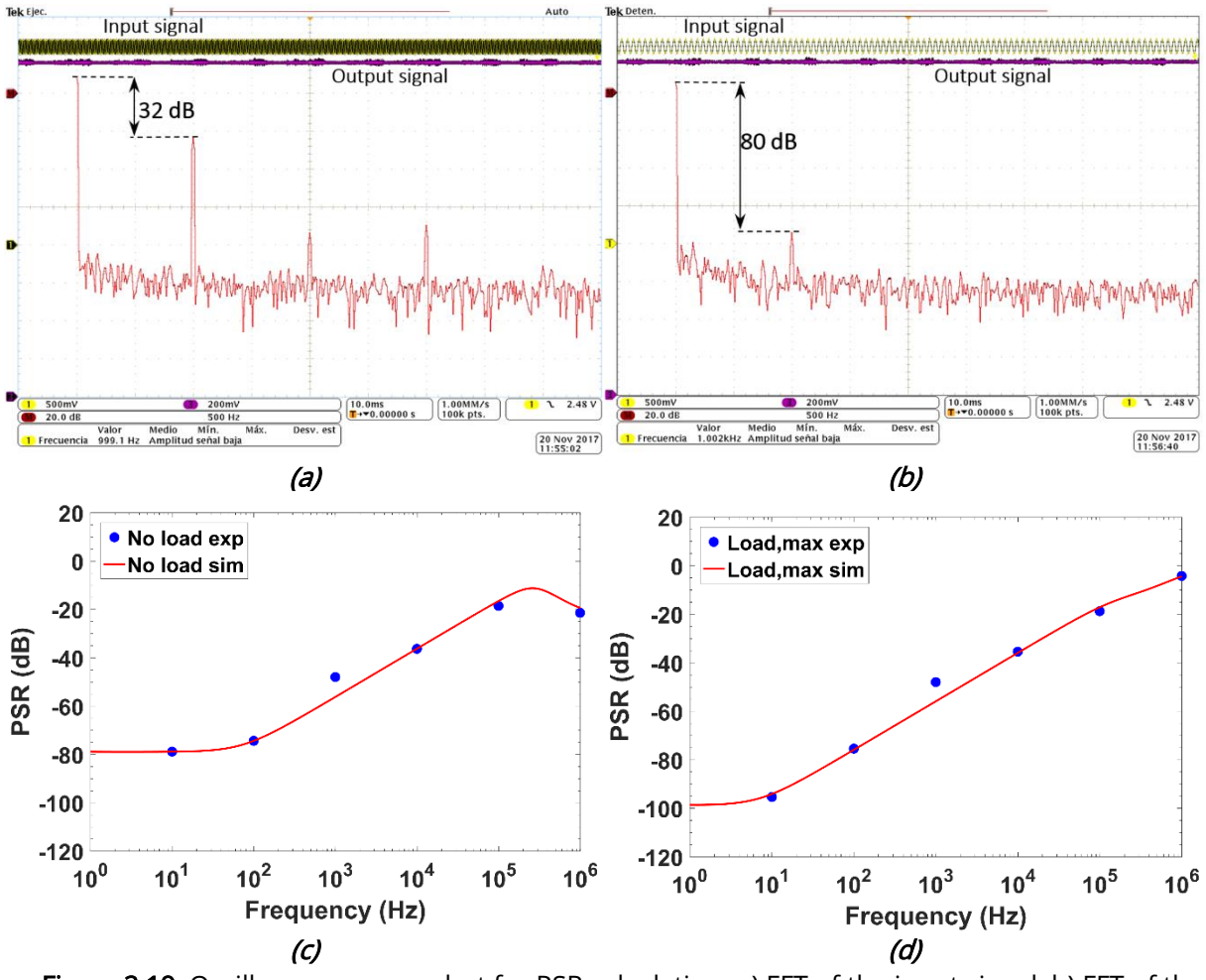
Finally, the PSR, equation (2.4), measures the capacity of the LDO regulator to reject ripple, of various frequencies, injected at its input [8].

Figure 2.19 shows the PSR value at no load condition for an input signal of 0.1 V amplitude and 1 kHz frequency over a supply voltage of 2.8 V (green) and an output



(a) *(b)*

Figure 2.18. Line transient behaviour: a) Undershoot response; and b) Overshoot response.



(a) *(b)*

(c) *(d)*

Figure 2.19. Oscilloscope screenshot for PSR calculation: a) FFT of the input signal; b) FFT of the output signal. PSR over frequency for: c) minimum load; and d) maximum load.

voltage centered at 1.8 V (purple). The FFT (red) shown in Figure 2.19a, corresponds to the input signal (green) and the one in Figure 2.19b to the output signal (purple). A drop of ~48 dB in the 1 kHz signal is measured. Figure 2.19c and Figure 2.19d shows the PSR for different frequencies for no load and maximum load current respectively. The main characteristics of the presented LDO regulator are summarized at the end of this chapter in 2.4Conclusions, where they are also compared with similar early reported works.

2.3.3. Microinstrument application

To show the functionality of the proposed 1.8 V CMOS LDO regulator, the micro-instrument shown in Figure 2.20a has been emulated. The setup (Figure 2.20a) includes 10 CMOS lock-in based signal-processing (SP) blocks, each of them encapsulated in a 24-pin dual in line (DIL-24) package, consisting of one digitally programmable analog quadrature signal generator and a dual readout system. All of them are biased to 1.8 V by using the proposed LDO regulator, encapsulated in a separate DIL-24 package (Figure 2.20b, down). Two DAQ USB-6212 emulate the impedance sensor signals and recover the corresponding DC output signals (V_x and V_y) provided by the 10 dual-channel LIAs. They also provide the clock signal required to configure the 12-bit registers that set the oscillators frequencies, sent in daisy chain.

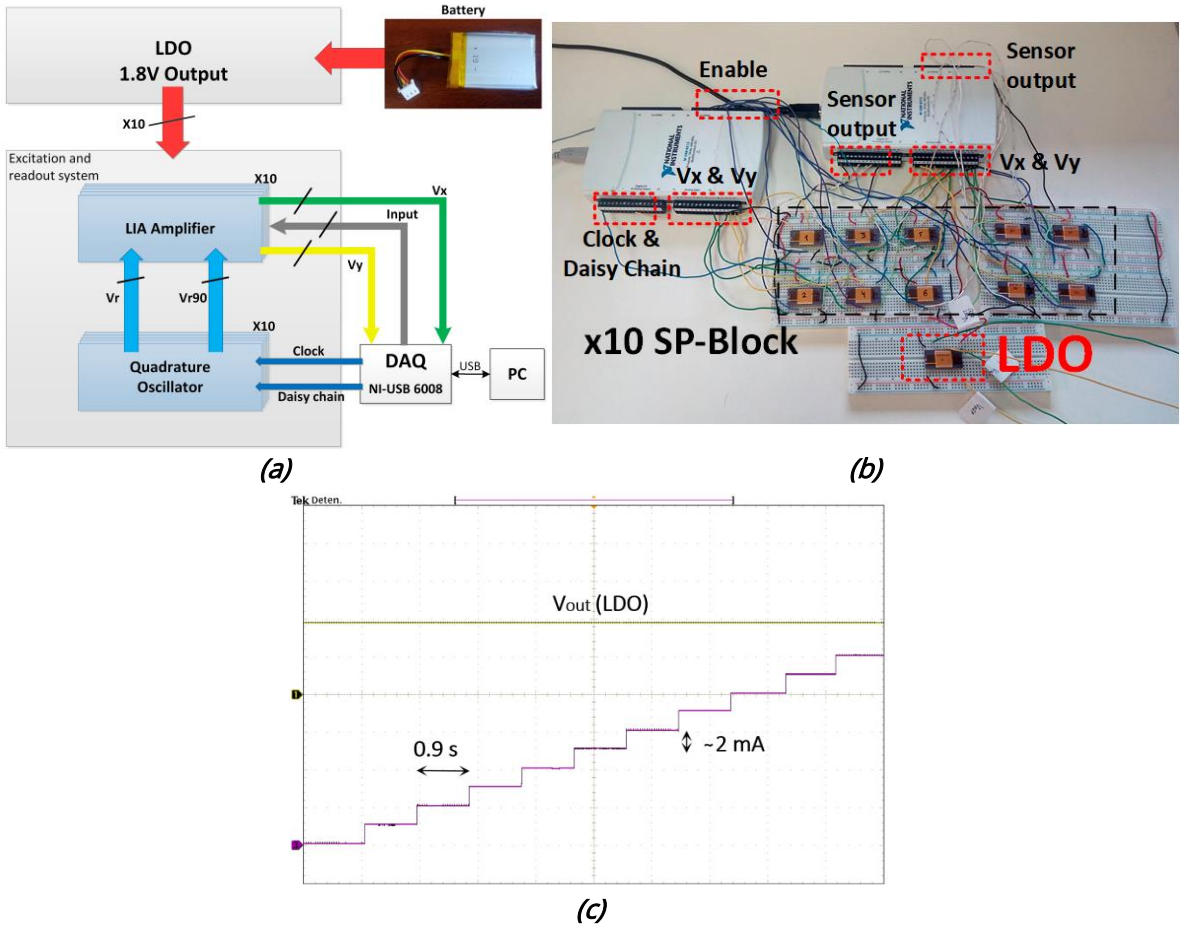


Figure 2.20. Multichannel lock-in based battery-supplied micro-instrument: a) block diagram; b) Implementation; and c) oscilloscope screenshot for the LDO output voltage (green) at activation of each signal-processing block (purple).

Each individual processing IC presents a current consumption of ~2 mA, and can be individually activated and deactivated to verify the dynamic LDO output voltage behaviour. Figure 2.20c shows the results achieved, when V_{bat} = 2.1 V, for the sequential activation (every 0.9 s) of the 10 circuits in the array, up to a total current consumption of ~20 mA. The proposed LDO regulator is perfectly capable of providing the demanded current while keeping a stable supply voltage, validating the suitability of the proposal for the target application.

2.4. CONCLUSIONS

The performance of the proposed 1.8 V CMOS LDO regulator is summarized and compared in Table 2.2 with previously reported works with similar specifications, all measured CMOS cap-less designs.

The evaluation of the performance of the different architectures is done through two figures-of-merit (FoM). The first one is defined as follows

$$FoM_1 = \frac{C_{Load} * LNR * LDR * I_q}{1000 * I_{Load,max}} \ (s) \tag{2.14}$$

FoM_1 compares the regulation performance-power efficiency trade off, where C_{Load} (pF), LNR (mV/V), LDR (mV/mA), I_q (µA) and $I_{Load,max}$ (mA) are the output capacitor, the line and load regulation, the quiescent current and the maximum load current. The factor 1000 is introduced to have FoM_1 dimensioned in (s).

The second figure-of-merit, FoM_2, is a widely adopted FoM [13, 26] to evaluate the transient performance:

$$FoM_2 = \frac{t_{settle} * I_q}{I_{Load,max}} \ (s) \tag{2.15}$$

Where t_{settle} is the time that elapses from the start of a transition ($I_{Load,min} \rightarrow I_{Load,max}$) until the output voltage stabilizes within a margin error.

For both FoMs, the smaller is the value, the better is the performance metric. Besides, an α correction factor as proposed in [21] is introduced in both FoMs ($FoM_i^{\dagger} = \alpha FoM_i$), being the α factor

$$\alpha = \frac{I_q + I_{Load,min}}{I_q} \tag{2.16}$$

to take into account the minimum load current at which the LDO must operate, thus including the $I_{Load,min}$ requirement into I_q. In this way $FoM_1^{\dagger}$ properly evaluates the regulation performance with the effective power consumption and $FoM_2^{\dagger}$ the transient response for a full load transition.

Compared with previously reported works, the proposed 1.8 V LDO regulator attains within an area of 0.10 mm^2 better overall line and load regulation with a reduction of the power consumption while it keeps similar time response parameters, operating for a range of temperatures from -40ºC to 100ºC. Based on the dynamic technique [10, 20-22], the main advantage of the proposed current bias boosting circuit (CBBC) is that it

effectively improves the transient response both with simpler circuitry (< 4 % of the total chip, including both CQF) and with no additional ground current, therefore not degrading the system power consumption and size.

According to Table 2.2, the proposed 1.8 V LDO achieves competitive FoMs, rendering the best regulating–transient performance tradeoff over a wide temperature range. More in detail, the LDO in [10] makes use of a simple differential pair as error amplifier, with triple transient improved loops; it achieves similar regulating performances, exhibiting comparable FoMs, but with a quiescent current 3.6 times greater and twice the area. Output voltage spikes detection based on RC high pass filtering is implemented in [20]; however, this requires large capacitance and resistance values: the area of the HPF is more than half of the total chip area. The LDO in [21] uses a combination of a low power simple differential pair EA and two high-speed comparators to dynamically increase the bias current of the EA. However, to achieve a settling time of 200 ns, the comparators need 20.6 µA of the total 26 µA quiescent current, severely degrading the power consumption performance. A current-reused dynamic biasing circuit in the output of a two-stage EA using an NMOS-pass transistor to improve the load transient response with no extra current is implemented in [22]. However, this quiescent current is as high as 130 µA, and this solution needs a charge-pump voltage doubler driven by an external clock to bias this output stage allowing a dropout voltage of 200 mV.

To further extent the study on LDO regulators, a 0.18 µm-CMOS 1.2 V low voltage LDO version, with embedded 0.4 V reference voltage, V_{ref} is reported in [7]. To obtain a LDO with an output of 1.2 V, compatible with battery supply voltages, for a maximum I_{Load} = 50 mA over a $C_{Load,max}$ = 50 pF, we have selected the simplest high-gain single-stage error amplifier topology suitable for low-voltage operation: a folded-cascode, which besides allows cascode compensation (C_c = 6.1 pF). For the transient enhancement, a dynamic biasing method –active only during the transient stages– is adopted, which requires minimal additional hardware. In this way, we manage to hasten the transient response without jeopardizing the power consumption and the complexity of the design.

Specifically designed to meet the constraints of battery-operated devices, it achieves minimum power (10.32 µW) and area consumption (0.109 mm^2), including the voltage-independent and temperature-independent reference voltage, achieving settling times of 1.3 µs while showing good static line and load regulation, compared with the state of the art.

Table 2.2. Comparison of the 1.8 V CMOS Capacitorless LDO regulator with previously reported works.

Parameter	This work	[27]'12	[15]'07	[18]'12	[19]'16	[10]'11	[21]'16	[22]'18	[28]'15
CMOS Tech. (µm)	0.18	0.35	0.35	0.35	0.18	0.35	0.35	0.18	0.065
V_{in} (V)	1.94 – 3.6	2.0 – 2.4	3	2.5 - 4	1.5 – 1.8	1.642 – 5	3.7	1.6 – 1.8	1.2
V_{out} (V)	1.8	1.073	2.8	2.35	1.2	1.5	3.25	1.4 – 1.6	1
V_{do} (mV) @ $I_{L,max}$ (mA)	140 @ 50	47 @ 0.5	200 @ 50	150 @ 100	300 @ 50	142 @ 100	300 @ 50	200 @ 50	150 @ 10
I_q (µA)	7.45	35.7	65	7 - 17	2.4 -242	27	26	130	50 – 90
C_{Load} (pF)	100	30	100	100	100	100	100	50	140
Line Regulation (mV/V)	0.081	39	~23	1	12.3	1.046	-	0.857	37.1
Load Regulation (mV/mA)	-0.82	13	~0.56	0.08	0.14	0.0752	~2.86	0.248	1.1
Full load ST (µs)	< 2.5	-	15	~0.15 [(a)]	~1.6	1	0.2 [(b)]	0.04 [(c)]	0.00115
PSR (dB) @ 1 kHz	-48	-38.1 @ 10 MHz	-57	-	< -33 @ 1 MHz	-60.6	~ -40	-70	< -21
Temp. range (°C)	-140	37	-	-	-	-	-	-	-
Area (mm^2)	0.10	~ 1	0.29	0.064	0.03	0.2	0.098	0.21	0.023
FOM_1 (fs)	0.989	$1.086*10^6$	1674.4	0.56 – 1.36	8.27 - 833.45	2.123	-	27.63	28567 – 51421
$FOM_1^{\dagger}$ (fs)	0.989	-	1674.4	4.56 – 11.07	8.27 - 833.45	2.123	-	27.63	28567 – 51421
FOM_2 (ns)	0.37	-	19.5	0.011 – 0.026	0.077 – 7.74	0.27	0.104	0.104	0.00575 – 0.01
$FOM_2^{\dagger}$ (ns)	0.37	-	19.5	0.086 – 0.21	0.077 – 7.74	0.27	-	0.104	0.00575 – 0.01
$FOM_1^{\dagger}xFOM_2^{\dagger}$ $(ps)^2$	0.366	-	32650.8	0.392 – 2.325	0.64 - 6451	0.573	-	2.87	164.26 - 514.21

[(a)] I_L: 50 µA – max; [(b)] I_L: 0.1 mA – max; [(c)] I_L: 9 mA – 40 mA; [(†)] $FoM_{1,2}$ with the α factor applied.

2.5. REFERENCES

1. Rincon-Mora, G. Analog IC Design with Low-Dropout Regulators (LDOs). *McGraw-Hill, Inc.,* 2009.
2. Lee, B.S. Technical Review of Low Dropout Voltage Regulator Operation and Performance. *Application Report, Texas Instrument*, 1999. Last accesed: 05th November 2021. http://www.ti.com/lit/an/slva072/slva072.pdf
3. Zhou, S., Sheng, W., Deng, F., Wu, X. and Fu, Z. A Novel PassiveWireless Sensing Method for Concrete Chloride Ion Concentration Monitoring. *Sensors,* 2017.
4. Jong-Ryul, Y., Seong-Tae, H. and Donghyun, B. Differential CMOS Sub-Treahertz Detector with Subthreshold Amplifier. *Sensors,* 2017.
5. Li, X., Zhang, H., Peng, F., Li, Y., Yang, T., Wang, B. and Fang, D. AWireless Magnetic Resonance Energy Transfer System for Micro Implantable Medical Sensors. *Sensors,* 2012.
6. Pérez-Bailón J., Márquez, A., Calvo B. and Medrano N. An all-MOS low-power fast-transient 1.2 V LDO regulator. *Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Giardini Naxos, Italy, 2017.
7. Pérez-Bailón J., Calvo B. and Medrano N. A Fully-Integrated 180 nm CMOS 1.2 V Low-Dropout Regulator for Low-Power Portable Applications. *Electronics*, 2021.
8. Lee, B.S. Understanding the Terms and Definitions of LDO Voltage Regulators. *Application Report, Texas Instrument*, 1999. Last accesed: 05th November 2021. http://www.ti.com/lit/an/slva079/slva079.pdf
9. Torres, J., El-Nozahi, M., Amer, A., Gopalraju, S., Abdullah, R., Entesari, K. and Sánchez-Sinencio, E. Low Drop-Out Voltage Regulators: Capacitor-less Architecture Comparison. *IEEE Circuits and Systems Magazine*, 2014.
10. Chen, C.M. and Hung, C.C. A fast self-reacting capacitor-less low-dropout regulator. *IEEE Solid-State Circuits Conference*, Helsinki, Finland, 2011.
11. Leung, K.N. and Mok, P.K.T. A Capacitor-Free CMOS Low-Dropout Regulator with Damping-Factor-Control Frequency Compensation. *IEEE Journal of Solid-State Circuits,* 2003.
12. Lau, S.K., Mok, P.K.T. and Leung, K.N. A Low-Dropout Regulator for SoC with Q-Reduction. *IEEE Journal of Solid-State Circuits,* 2007.
13. Bu, S., Guo, J. and Nang Leung, K. A 200-ps-Response-Time Output-Capacitorless Low-Dropout Regulator with Unity-Gain Bandwidth >100 MHz in 130-nm CMOS. *IEEE Transactions on Power Electronics,* 2018.
14. El-Nozahi, M., Amer, A., Torres, J., Entesari, K. and Sánchez-Sinencio, E. High PSR Low Drop-Out Regulator with Feed-Forward Ripple Cancellation Technique. *IEEE Journal of Solid-State Circuits,* 2010.
15. Milliken, R.J., Silva-Martínez, J. and Sánchez-Sinencio, E. Full On-Chip CMOS Low-Dropout Voltage Regulator. *IEEE Transactions on Circuits and Systems I: Regular Papers,* 2007.
16. Giustolisi, G., Palumbo, G. and Spitale, E. Robust Miller Compensation with Current Amplifiers Applied to LDO Voltage Regulators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012.
17. Rincon-Mora, G. and Allen, P. A low-voltage, low quiescent current, low drop-out regulator. *IEEE Journal of Solid-State Circuits,* 1998.
18. Ming, X., Li, Q., Zhou, Z.-K. and Zhang, B. An Ultrafast Adaptively Biased Capacitorless LDOWith Dynamic Charging Control. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2012.
19. Maity, A. and Patra, A. A Single-Stage Low-Dropout Regulator with a Wide Dynamic Range for Generic Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* 2016.

20. Ho, M. and Nang Leung, K. Dynamic Bias-Current Boosting Technique for Ultralow-Power Low-Dropout Regulator in Biomedical Applications. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2011.
21. Amayreh, M., Leicht, J. and Manoli, Y. A 200 ns Settling Time Fully Integrated Low Power LDO Regulator with Comparators as Transient Enhancement. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, Canada, 2016.
22. Desai, C., Mandal, D., Bakkaloglu, B. and Kiaei, S. A 1.66 mV FOM Output Cap-Less LDO with Current-Reused Dynamic Biasing and 20 ns Settling Time. *IEEE Solid-State Circuits Letters,* 2018.
23. Pérez-Bailón, J., Márquez, A., Calvo, B., Medrano, N. and Martínez, P.A. Fast-transient high-performance 0.18 μm CMOS LDO for battery-powered systems. *Electronics Letters,* 2017.
24. Pérez-Bailón, J., Márquez, A., Calvo, B. and Medrano, N. A 0.18 μm CMOS LDO Regulator for an On-Chip Sensor Array Impedance Measurement System. *Sensors,* 2018.
25. Chen, C.M. and Hung, C.C. A fast self-reacting capacitor-less low-dropout regulator. *IEEE Solid-State Circuits Conference (ESSCIRC)*, Helsinki, Finland, 2011.
26. Hazucha, P., Karnik, T., Bloechel, B.A., Parsons, C., Finan, D. and Borkar, S. Area-efficient linear regulator with ultra-fast load regulation. *IEEE Journal of Solid-State Circuits,* 2005.
27. Crepaldi, P.C., Pimenta, T.C., Moreno, R.L. and Rodriguez, E.C. A Low Power CMOS Voltage Regulator for a Wireless Blood Pressure Biosensor. *IEEE Transactions on Instrumentation and Measurement*, 2012.
28. Lu, Y., Wang, Y., Pan, Q., Ki, W.H. and Yue, C.P. A Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power Supply Rejection. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *2015*.

Chapter 3
Basic Cells

Dual Synchronous Demodulation-based or Lock-in based Frequency Response Analyser-Impedance Spectroscopy (FRA-IS) front-ends basically consists of an input amplifying stage, followed by two quadrature multiplying or mixer stages and output filtering stages, as was shown in Figure 1.4 (introduction).

In this chapter, the design of each of these three basic stages is done considering, for simplicity, a single-channel approach (Figure 3.1). Therefore, amplifiers are studied in the first section. Next, mixers are considered in the second section, and finally low pass filters are introduced in the last section. Different implementations are advanced taking into account our design guidelines: LVLP operation, minimum area consumption, fully differential approach, system reconfigurability for optimal adaptation from a general-purpose LVLP architecture to the characteristics of the final application. Besides, the achievement of a SoC solution to minimize the total area and optimize the cost imposes the design in the previously used 0.18-μm CMOS technology.

For each block, we separately present in each section not only the design and characterization of the different cells, but also the corresponding conclusions subsection, and therefore there is not a closing general conclusions section in this chapter.

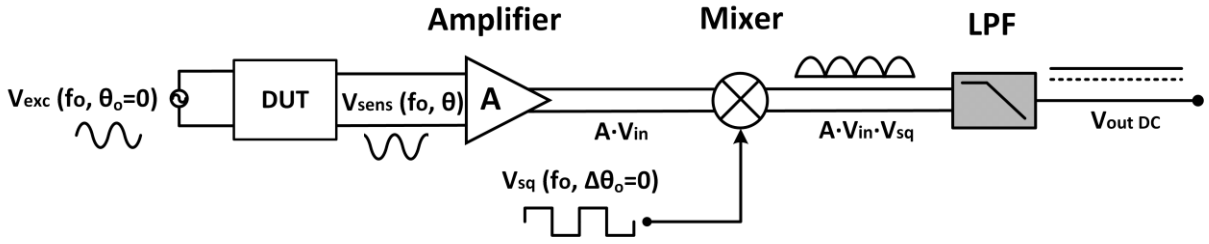


Figure 3.1. Classic structure of an analog front-end IS.

3.1. AMPLIFICATION STAGE

The amplifying stage is the input block; typically receives signals from the sensor with magnitudes varying from a few μV to mV in voltage mode, or from nA to μA in current mode. Therefore, to obtain a general purpose architecture, the proposed 1.8 V-0.18 μm CMOS fully differential amplifier must solve both AC voltage input signals (V-mode) and AC current input signals (C-mode), with a target 40 dB gain –so that the overall system noise is mainly determined by this input amplifier– and a bandwidth in the order of ~100MHz preserving LVLP characteristics.

The literature shows extensive research on front-end amplifiers [1-6]. However, among the reviewed literature, some of these papers report dual supply operation [1-3], incompatible with battery-operated portable system. They typically present single-ended structure [1-4] and have limited bandwidth below our target frequencies [1-5], limiting the operating range and the target applications or exhibit an elevated power/area consumption [6].

The works in [6-9] report open-loop structures based on a Transconductance-Transimpedance (TC-TI) topology, allowing for both voltage and current inputs, destined to cardiac electrocardiogram (ECG), photoplethysmogran (PPG) monitoring applications, presenting either low bandwidth (~100 Hz) or a high power consumption (~mW). However, this approach potentially exhibits high performance with wide frequency operation. Thus, an open-loop structure based on a TC-TI structure is chosen to implement the input stage. However, to attain the desired 40 dB gain level preserving a ~100MHz bandwidth with bounded power consumption, the amplifier is conformed as the cascade of two 20 dB stages: a preamplifier stage with a fixed 20 dB gain (80 dBΩ for current input), followed by a variable gain amplifier with an adjustable gain from 0 dB to 20 dB. To achieve the 20 dB to 40 dB gain target 100 MHz bandwidth for the overall amplifier, for each constituting cell, the bandwidth will be then designed to be slightly higher to compensate the loss of cascading several stages.

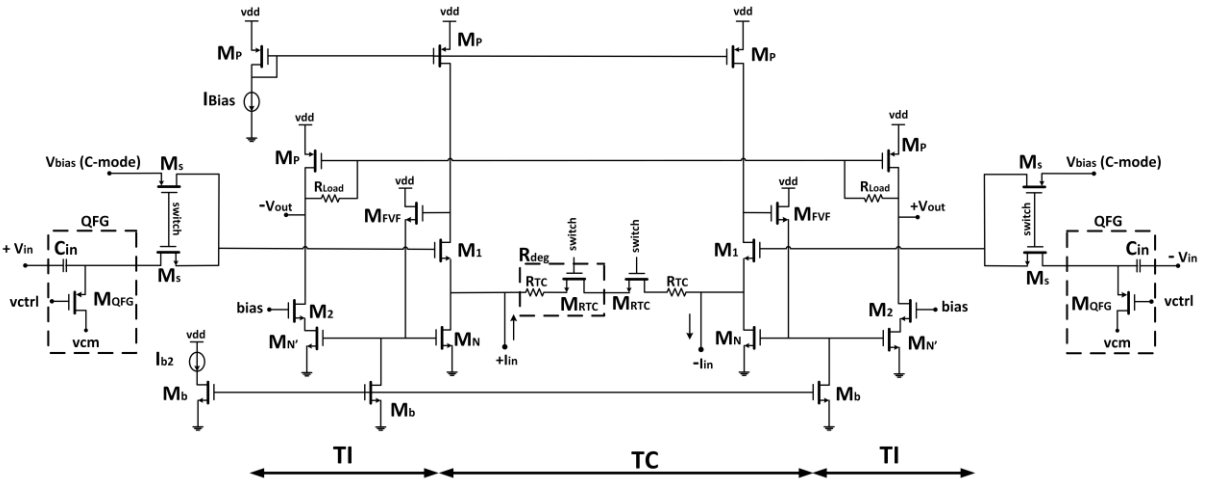


Figure 3.2. Schematic view of the proposed Low Noise Amplifier (LNA).

3.1.1. Fixed Gain Low Noise Pre-Amplifier (LNA)

Design

The complete schematic of the proposed amplifier, based on a Transconductance-Transimpedance architecture [6, 7], is shown in Figure 3.2.

The TC stage is a g_m-boosting source degenerated differential pair. Contrarily to, it uses M_1 NMOS-input transistors to reach up the desired frequencies, biased at constant current I_{Bias}. Transistors M_{FVF}, M_b (I_{b2}), M_N constitute a negative feedback g_m boosting path that reduces the equivalent M1 source resistance from $1/g_{m1}$ to $1/g_{m1}g_{mFVF}R_{out,FVF}$ [10]. In this way, M1 act as voltage followers in V-mode, copying the input voltage $\pm V_{in}$ to their corresponding sources, where it is converted to a linear current (V_{in}/R_{deg}), while in current mode M1 sources behave as suitable low-impedance input nodes.

In V-mode, the input voltage V_{in} is introduced through a Quasi-Floating Gate (QFG) connected to the gates of the degenerated M_1 NMOS differential pair. In this way, direct sensor coupling is allowed though capacitor C_{in}, while the input common mode voltage is set to $V_{cm}=V_{dd}/2$ through transistor M_{QFG} operating in the on region and thus acting as a large valued resistor (R_{Large}~GΩ). Besides, as the QFG acts as a high pass filter with cutoff frequency $f_{c,H}=1/(2\pi R_{Large}C_{in})$, by adjusting the gate voltage of M_{QFG} by V_{ctrl} its resistance value is modified and the high pass cut off frequency $f_{c,H}$ can be adjusted to fit the desired operating frequency range, eliminating low frequency noise.

In C-mode, the input current I_{in} is directly introduced to the system through the source of M1, with the gates of the differential pair in this case driven to a bias voltage $V_b = V_{cm}$.

In order to switch between input modes, a MOS switch system is implemented. It selects the suitable gate voltage to M1 while also connects (V-mode) or disconnects (C-mode) the degeneration resistance, R_{TC}. The disconnection of the degeneration resistance for the C-mode reduces the input noise [7]. This is verified in Figure 3.3, were the output integrated noise is 2.867 mV_{rms} with R_{TC} connected, while on the contrary the noise is reduced down to 1.155 mV_{rms} (60% reduction).

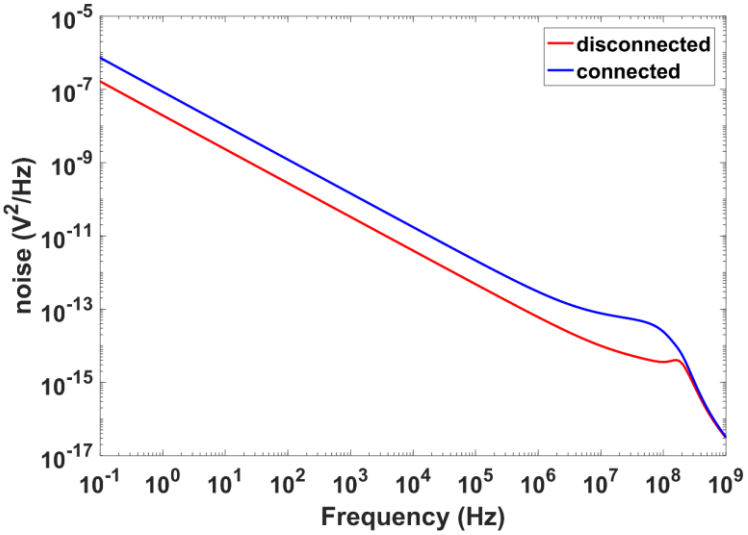


Figure 3.3. Noise analysis with and without disconnecting R_{deg} for C-mode.

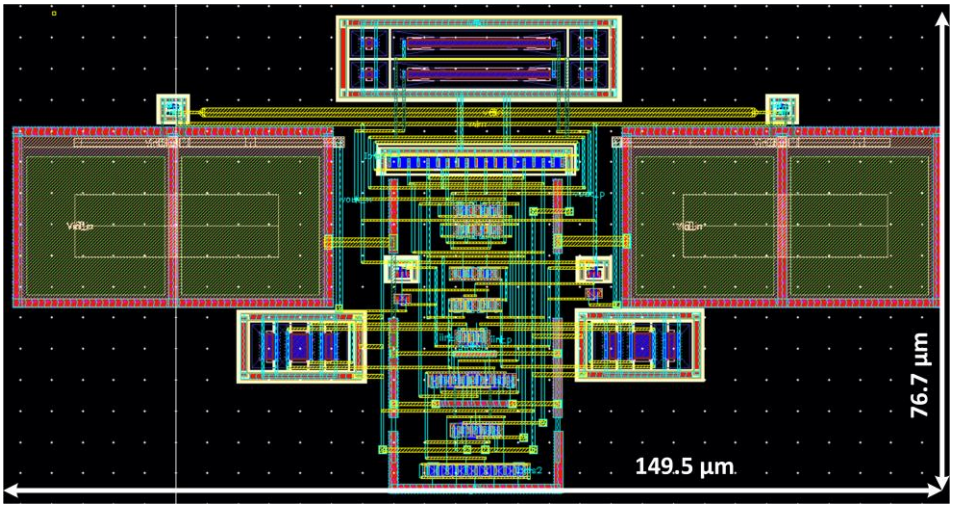
The degeneration scheme is formed by linear resistances, R_{TC}, and the mode-selection MOS switches, equally split into two (Figure 3.2) to keep the symmetry of the circuit. Thus $R_{deg}=R_{TC}+R_{MOS,switch}$, with $R_{TC} = R_{POLY}$ = 640 Ω, while $R_{MOS,switch}$= 300 Ω.

The V-mode TC output currents/C-mode input currents are sensed through transistors M_N and copied through the M_N-$M_{N'}$ NMOS current mirrors to the TI-structure, to be finally transformed to voltage through floating load resistors R_{load}, which are also used as common-mode feedback loop, sensing the output common mode to drive the gate of PMOS output transistors M_P.

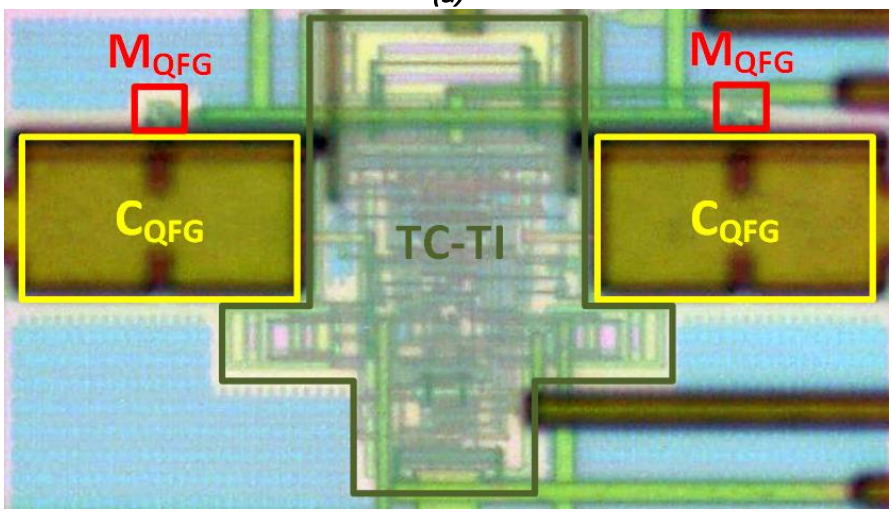
The G_V voltage gain and G_I the current gain are respectively given by:

$$G_V = \frac{\left(\frac{W}{L}\right)_{N'}}{\left(\frac{W}{L}\right)_N}\frac{R_{Load}}{R_{deg}} \qquad G_I = \frac{\left(\frac{W}{L}\right)_{N'}}{\left(\frac{W}{L}\right)_N}R_{Load} \tag{3.1}$$

where $(W/L)_N$ is the transistor size of the NMOS current mirror of the TC stage and $(W/L)_{N'}$ the transistor size of the NMOS current mirror of the TI stage. The ratio $(W/L)_{N'}/(W/L)_N$ is actually the copy factor of the TC-TI NMOS current mirror, and it is fixed to 1, the gains are dependent only on the resistors.



(a)



(b)

Figure 3.4. a) Layout view and b) microphotograph of the proposed LNA architecture.

Transistor sizes in (μm/μm) are M_1= (5/0.18), M_2= (5/0.18), M_P= (5.5/1), M_N= (5/0.18), $M_{N'}$= (5/0.18), M_b= (5/1), M_{FVF}= (5/0.18), M_{RTC}= (3/0.18), M_{Switch}= (1.5/0.18) and M_{QFG}= (0.24/0.18). C_{QFG}= 1 pF, R_{TC}= 640 Ω and R_{Load}= 24.7 kΩ. With a 1.8 V power supply, a common mode $V_{cm} = V_{dd}/2$ and a bias current –externally generated–set to I_{Bias}=25 μA and I_{b2}=0.15 μA, the total power consumption is 180.4 μW. The gain is fixed to 26dB in V-mode (89 dBΩ in C-mode) and the bandwidth reaches 110 MHz with C_{Load} = 52 fF. Figure 3.4 shows the layout view and microphotograph of the integrated proposed cell, occupying a total active area of 76.7 μm x 149.5 μm including the QFG.

Characterization

The following results are post-layout simulations as the prototypes are currently under experimental characterization.

Gain and bandwidth

Figure 3.5 shows the frequency response of the amplifier in voltage input mode (Figure 3.5a) and current input mode (Figure 3.5b). In V-mode, it shows a 26.2 dB gain for the differential output with a bandwidth higher than 110 MHz considering a C_{Load} = 52 fF. For C-mode, the gain reaches 89.0 dBΩ and a 157 MHz bandwidth.

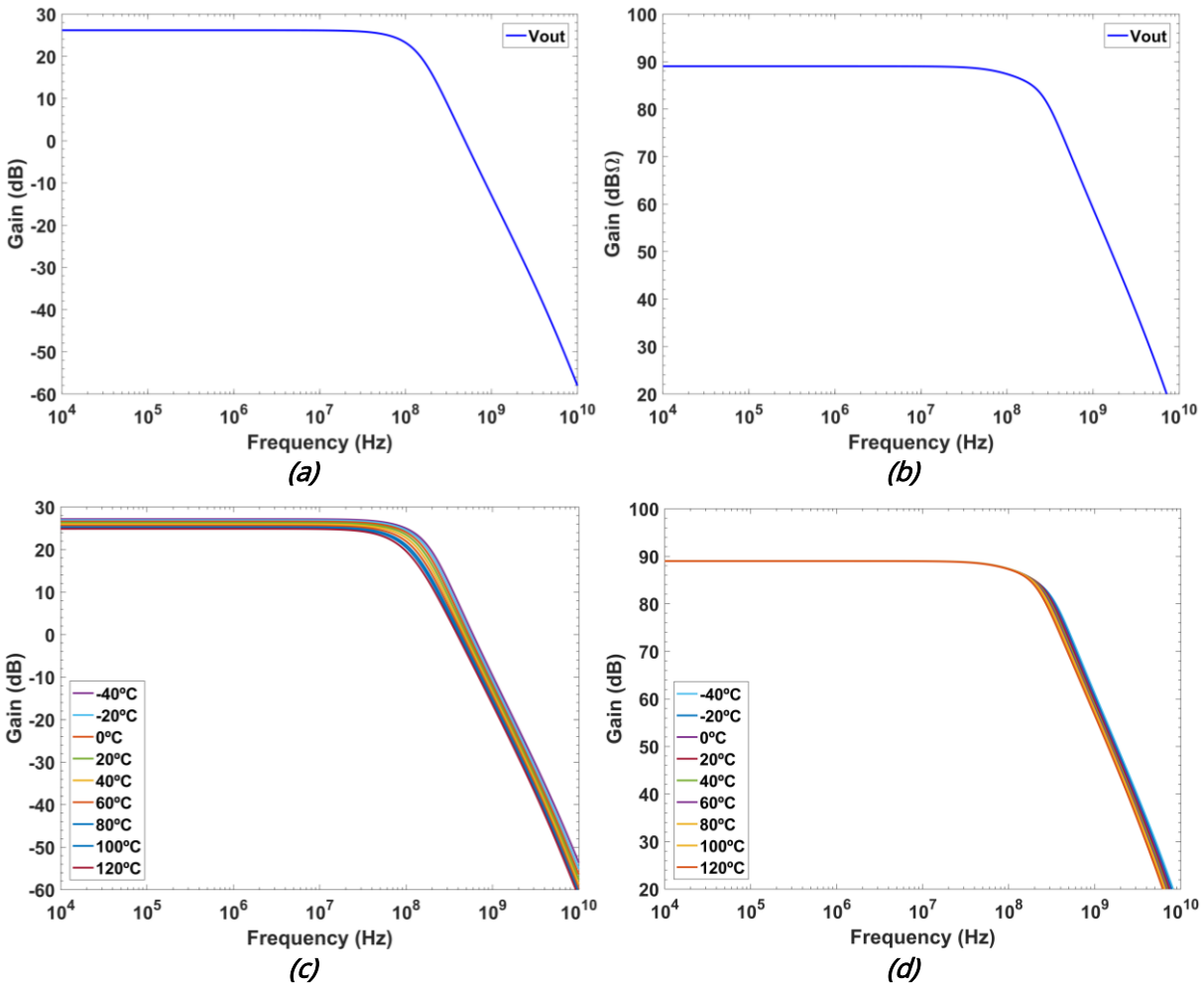


Figure 3.5. Frequency response at room temperature: a) V-mode and b) C-mode; and for different temperatures c) V-mode and d) C-mode.

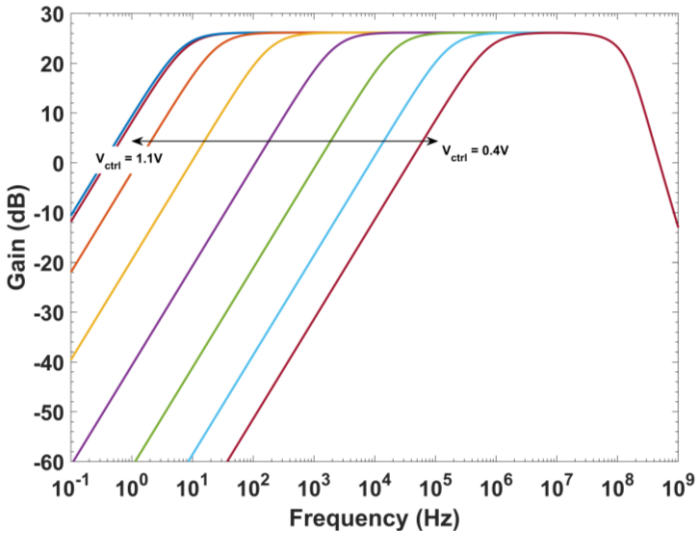


Figure 3.6. High pass frequency tuning for all V_{ctrl} range, with maximum gain.

The influence of the temperature (from -40ºC to 120ºC) over the gain and the operating range is shown in Figure 3.5c (V-mode, deviation of 0.014 dB/ºC and 293 kHz/ºC) and Figure 3.5d (C-mode, deviation of $25*10^{-5}$ dB/ºC and 34 kHz/ºC).

The high pass cut-off frequency $f_{c,H}$ control in V-mode is shown in Figure 3.6. For a 0.4 V to 1.1 V variation of V_{ctrl} in 0.1 V steps, $f_{c,H}$ varies from 736 kHz (0.4 V) to 6.9 Hz (1.1 V). For higher values of V_{ctrl}, the $f_{c,H}$ stays at 6.9 Hz while lower values keeps increasing $f_{c,H}$ until there is no bandpass, being the voltage control limit 0.4 V.

Linearity

The Total Harmonic Distortion (THD) as a function of the output amplitude is shown in Figure 3.7 for a sinusoidal signal of frequency f_{in}=20 MHz≅ $f_{c,BW}$/5, with V_{ctrl} set to 1.1 V –rendering the worst-case scenario–. In V-mode, the THD < –40 dB for output amplitudes up to 276.6 mV_{pp}, while in C-mode, the THD is below –40 dB for output amplitudes up to 390 mV_{pp}.

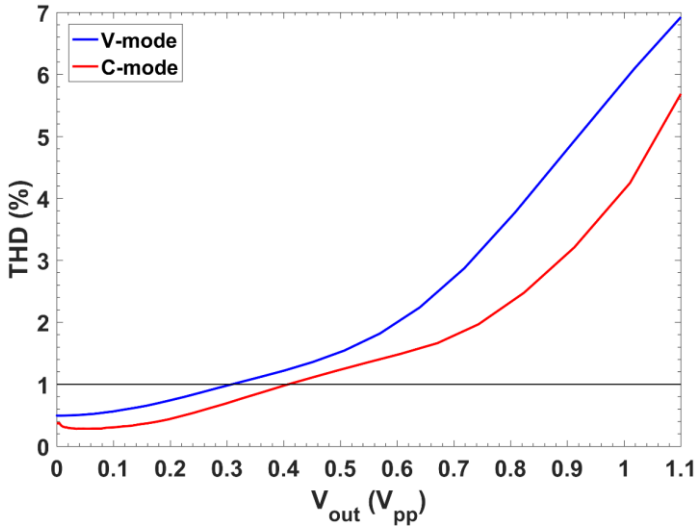


Figure 3.7. THD as a function of the output amplitude in V-mode and C-mode.

Noise

The integrated noise over the frequency range is reported in Table 3.1.

Table 3.1. Integrated noise of the Fixed-Gain Low Noise Amplifier.

Input mode	V-mode	V-mode	C-mode
V_{ctrl} (V)	1.1	0.4	Not Applicable
Gain	26 dB	26 dB	89 dBΩ
BW (Hz)	6.9-100M	736k-100M	0.16-100M
out (mV_{rms})	1.902	1.606	1.057
In (V_{rms} or A_{rms})	95.3 μV	80.5 μV	37.5 nA
In (V/√Hz or A/√Hz)	9.53 nV	8.08 nV	3.75 pA

3.1.2. Variable Gain Amplifier (VGA)

This second amplifier follows an identical structure as the one introduced above for modularity, with two main differences with respect to the previous structure. First, as this stage is designed to be connected to the previous cell outputs, input signals are limited to voltage signals and, as it is directly coupled to the previous stage, the QFG scheme is not needed. Secondly, gain variability has been added by modifying the degeneration scheme.

Design

The complete scheme is shown in Figure 3.8a. Recalling equation (3.1), and considering that the current mirror copy factor M_N-$M_{N'}$ is again 1:1, the voltage gain is given by

$$G_V = \frac{\left(\frac{W}{L}\right)_{N'}}{\left(\frac{W}{L}\right)_{N}} \frac{R_{Load}}{R_{deg}} \tag{3.2}$$

Thus, gain variation can be achieved by substituting either the constant value of R_{Load} or R_{deg} by an array of resistances. In this case, R_{Load} is kept constant to maintain the cell bandwidth constant, while the R_{deg} is implemented as an array of 4-bit digitally MOS-switchable resistances, as shown in Figure 3.8b. In this way, a programmable 6 dB to 26 dB gain range is obtained for this amplifier.

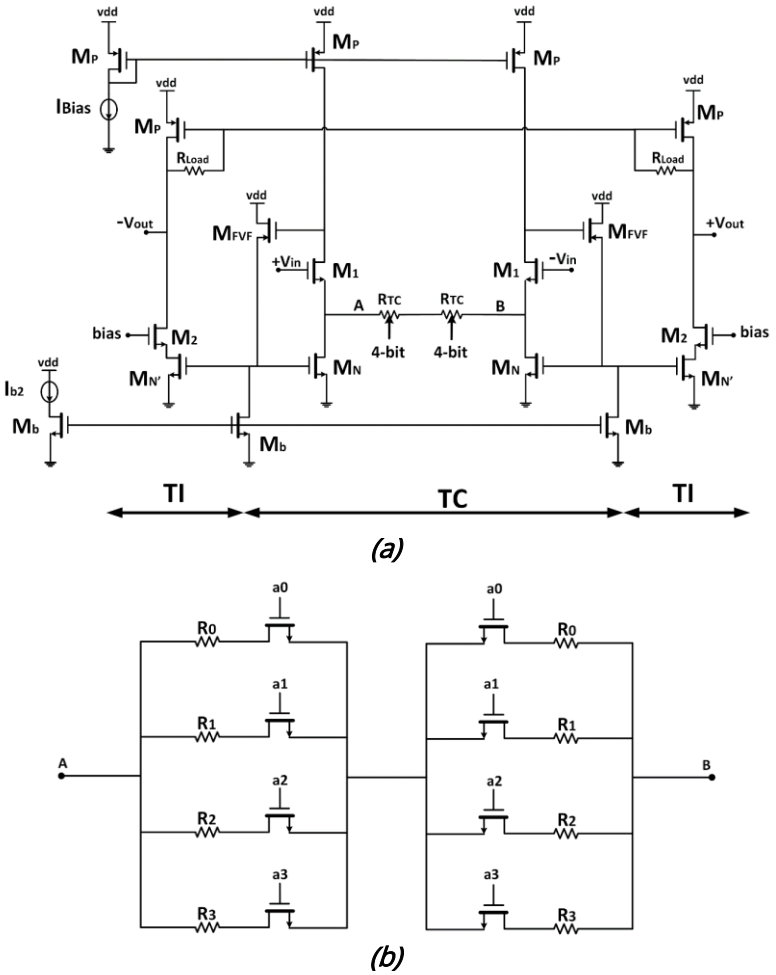
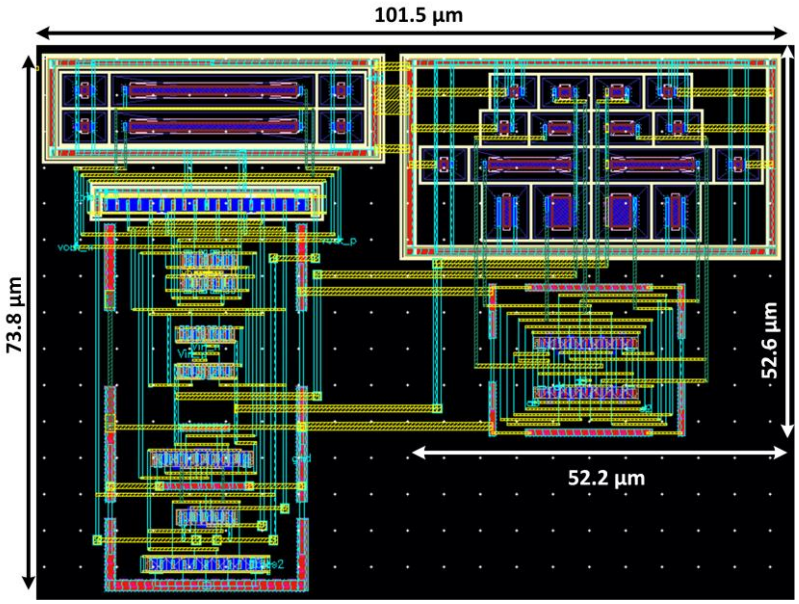


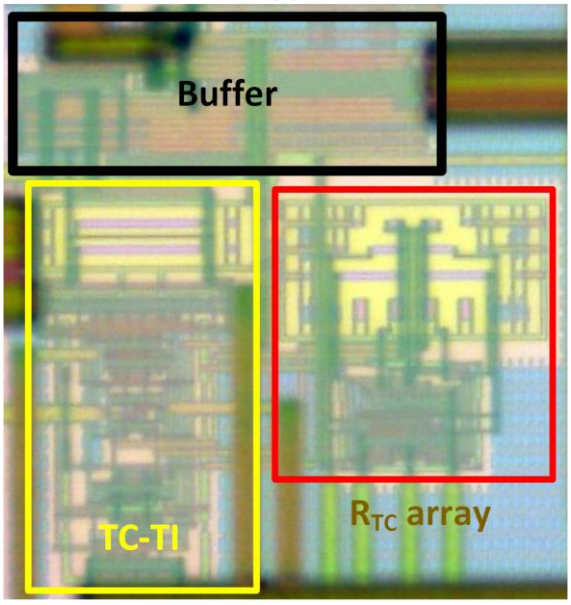
Figure 3.8. VGA a) schematic view; b) resistances array.

Transistor sizes in (μm/μm) are M_1= (5/0.18), M_P= (5.5/1) M_N=M_N'= (5/0.18), M_{Ib2}= (5/1) and M_{FVF}= (5/0.18), the load resistance is R_{Load}= 24.7 kΩ. The value of the resistances of the array are R_0= 640 Ω, R_1= 1.5 kΩ, R_2= 3 kΩ, R_3= 12 kΩ; the MOS switches size in (μm/μm) is (3/0.18), with a resistance value of ~300 Ω. To reduce the noise, low resistance values are used, however the use of small resistance values makes the parasitic resistances introduced in the layout not negligible. Therefore, we have adapted the low resistance values to account for these parasitic contributions.

The proposed VGA, as the previous LNA, operates at a 1.8 V power supply with a common mode V_{cm} voltage of 0.9 V. The bias current is set to 25 μA and I_{b2} is set to 0.15 μA, with a total power consumption of 180.4 μW. It provides a variable gain ranging from 6 dB to 26 dB with a bandwidth almost constant above 120 MHz at a C_{Load} = 52 fF. The microphotograph is shown in Figure 3.9, with an active area of 73.8 μm x 46.9 μm for the VGA core and 52.6 μm x 52.2 μm for the array of resistances, being the total active area 0.0062 mm^2. A buffer was also included to carry out the experimental high frequency characterization.



(a)



(b)

Figure 3.9. a) Layout view and b) microphotograph of the proposed VGA cell with buffer.

Characterization

The following section presents the post-layout simulation results of the main parameters for the Variable Gain Amplifier.

Gain and bandwidth

First, gain performance is validated. Figure 3.10 shows the frequency response for the different digital words. Gains are 6 dB (a3 active), 15.9 dB (a2 active), 20.8 dB (a1) and 26.1 dB (a0 active). The bandwidth is higher than 120 MHz for all gain configurations.

A sweep over the temperature (from -40ºC to 120ºC) for the maximum and minimum gain shows (Figure 3.11) a variation of 0.017 dB/ºC for maximum gain, and $55*10^{-4}$ dB/ºC for minimum gain, while the bandwidth varies 250kHz/ºC and 100 kHz/ºC respectively.

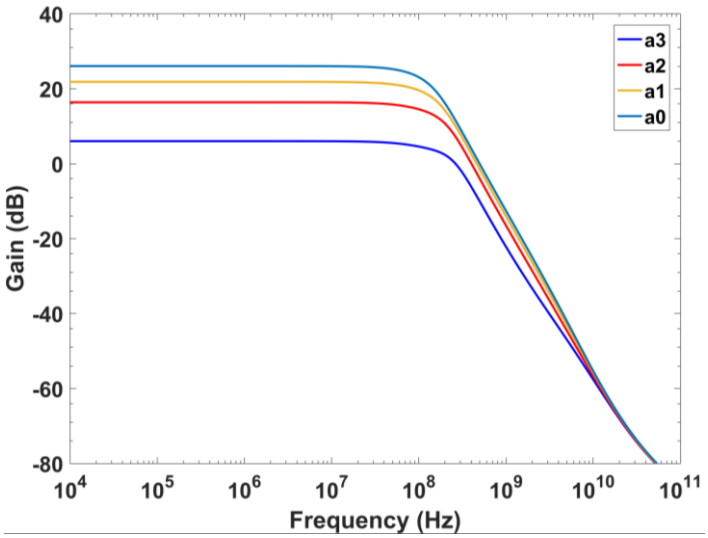


Figure 3.10. Frequency response for different gain configurations.

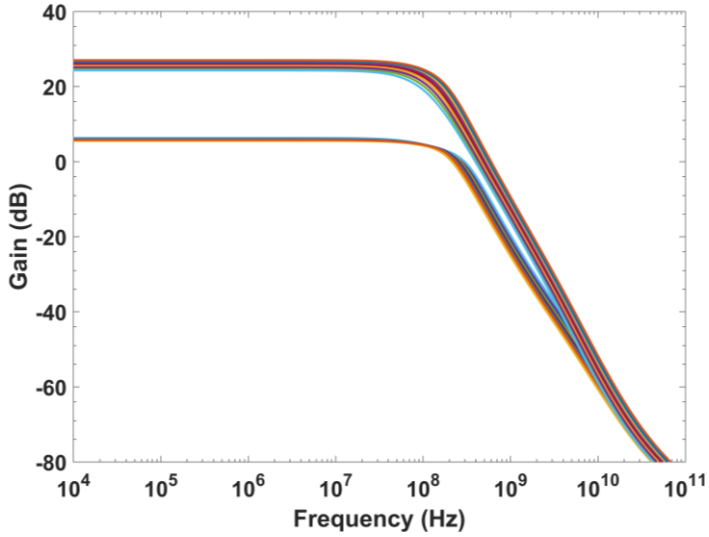


Figure 3.11. Frequency response for maximum and minimum gain, at different temperatures.

Linearity

The Total Harmonic Distortion (THD) as a function of the output amplitude is shown in Figure 3.12 at minimum and maximum gain, for a sinusoidal signal of frequency f_{in}=20 MHz ≅ f_d/5. For maximum gain, the THD is maintained below –40 dB for output signals up to 563 mV_{pp}, while for minimum gain the THD is maintained below –40 dB for output signals up to 350.5 mV_{pp}.

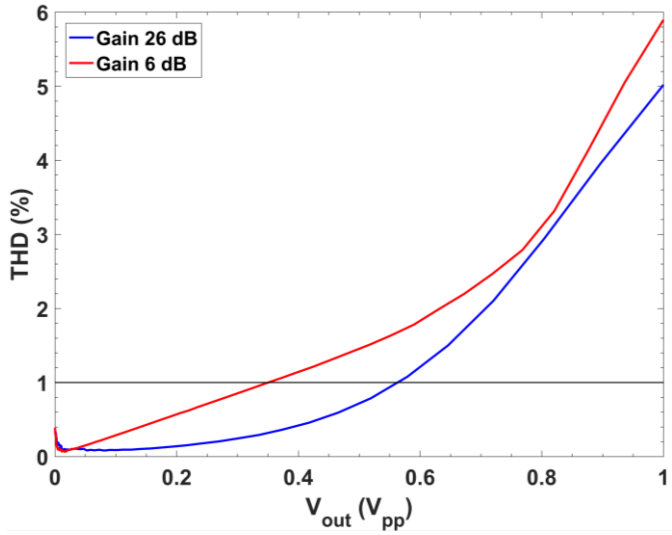


Figure 3.12. THD as a function of the output amplitude with: maximum and minimum gain.

Noise

The integrated noise over the frequency range for both maximum and minimum gain is reported in Table 3.2. The noise performance can be worse than for the LNA as the dominant noise contribution will come from the previous stage.

Table 3.2. Integrated noise of the Variable Gain Amplifier.

Gain	26.1 dB	6 dB
BW (Hz)	0.1-100M	0.1-100M
out (mV_{rms})	1.825	1.072
In (V_{rms})	80.4µ	537.3µ
In (V/√Hz)	8.04n	53.7n

3.1.3. Comparison with other works

A comparison of the presented structures with previously reported works is presented in Table 3.3. As can be noted, the proposed topologies report a high frequency range with low power and area consumption, while keeping similar input noise levels.

Two different Figures of Merit (FoM) are defined for a better comparison. The first one, FoM_1, presents a trade-off between linearity and input referred noise. It is based on the equation used for the Dynamic Range (DR):

$$DR\ (dB) = 20\log_{10}\left(\frac{linearity(V_{rms})}{noise(V_{rms})}\right) \tag{3.3}$$

FoM_1 is defined as:

$$FoM_1 = 20\log_{10}\left(\frac{linearity(V_{out,pp})/(THD(\%)/100)}{noise}\right) \tag{3.4}$$

With the noise given in V/√Hz in V-mode and A/√Hz in C-mode.

The modifications introduced are: first, as each proposal of the literature operates at a different range of frequencies, the noise referred to the input is given in V(A)/√Hz to compare the different works on equal grounds. Similarly, the linearity is reported using different combinations of amplitudes and THD values, without having a common ground to compare. Thus, we propose a linearity/THD ratio, were the bigger the value the better. Finally, the magnitude is converted to dB, where the higher the values obtained the better performance it provides.

The second figure of merit proposed, FoM_2, reflects the trade-off between power consumption and performance in terms of frequency range and gain (in V/V or V/A). Area consumption is not considered as in most of the papers used for the comparison is not provided. It is defined as:

$$FoM_2 = \frac{Gain * Freq.range(MHz)}{Power(\mu W)} \tag{3.5}$$

With Gain in V or A.

We also use the Noise Efficiency Factor (NEF) as it takes into account the trade-off between noise-BW and current. The Noise Efficiency Factor (NEF) is defined as [11]:

$$NEF = v_{in,RMS}\sqrt{\frac{2 * I_q}{V_T 4k_B T\pi BW}} \tag{3.6}$$

With V_T the thermal voltage, k_B Boltzmann's constant, T the temperature, BW the bandwidth, $v_{in,RMS}$ the input-referred noise and I_q the current consumed.

Compared with the previous proposals presented in Table 3.3, our proposals present a NEF factor of the same order of magnitude with those working at similar gain values.

From FoM_1 we can see that a better performance is achieved with our proposed structures, compared with the LNA proposed in [7]. An improvement can be seen especially in the current mode.

Note in FoM_2 how it must be differentiated between those architectures based on voltage gain (dB) and those based on transimpedance gain (dBΩ), as the value is considerable higher for the latter. Therefore, the comparison must be made between those architectures that use the same gain conversion. Except for the minimum gain configuration of [12], our proposal presents a better gain-bandwidth-power trade-off.

Table 3.3. Comparison table of the proposed amplifiers (LNA&VGA) with similar works.

Parameter	LNA @ V_{ctrl}=1.1V (V-mode)	LNA @ V_{ctrl}=0.4V (V-mode)	LNA (C-mode)	VGA	[13]'10	[6]'18 (IA)	[6]'18 (VGA)	[7]'18	[12]'19	[14]'20	[8]'21
Results	Sim	Sim	Sim	Sim	EXp	EXp	EXp	EXp	Sim	Sim	EXp
Input mode	V&C	V&C	V&C	V	C	V	V	V&C	V	V	V&C
Tech (µm)	0.18	0.18	0.18	0.18	0.35	0.18	0.18	0.18	0.18	0.18	0.18
Supply (V)	1.8	1.8	1.8	1.8	3.3	3.3	3.3	1.6	1.8	1.8	1.6
Power (µW)	180.4	180.4	180.4	180.4	726 (3)	2070	4660	72 (1)	6.2/39.6	36.1	55.8 (1)
Gain (dB)	26.2	26.2	89 dBΩ	6-26.1	N/A	9.3	0, 9.3, 21	37 dB / 117 dBΩ	39.3/39.5	0-20	55 dB /(1) 118 dBΩ
T range (°C)	-40–120	-40–120	-40–120	-40–120	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Freq. range (Hz)	6.9 – >100M	736k – >100M	0.16 – >157M	0.1–>100M	10-50M	>10M	>10M	0.1–100	250.7k–1.296M	0.1–1M	1–200/ 0.25–15
Linearity ($V_{out.pp}$) @ THD (dB)	0.277 @ -40	N/A	0.39@ -40	0.35-0.56 @-40	N/A	N/A	N/A	0.035@ -57.9 0.142@-61.7	0.092@-43.7/ 0.096@-	N/A	N/A
Noise (V(A)/√Hz)	9.53 nV	8.08 nV	3.75 pA	53.7 nV – 8.04 nV	110 pA / (2) 18.3 pA	14 nV	80n, 27n, 6.7 nV	271.4 nV / 38.4 pA(1)	25.5 nV / 11.9 nV	189.6 nV	276 nV / 44.8 pA
Area (mm^2)	0.0115	0.0115	0.0115	0.0062	0.01 (3)	N/A	N/A	N/A	N/A	N/A	N/A
CMRR (dB) @Hz	208 @100k	213 @100k	226 @100k	249/250 @100k	N/A	86 @ N/A	N/A	N/A	52.8/69.8 @ N/A	55.3 @ N/A	N/A
FoM_1 (dB)	189.3	N/A	260.3	176.3-196.9	N/A	N/A	N/A	160.1–165.3	174.8–190.5	N/A	N/A
FoM_2	11.32	11.23	24.53k	1.11-11.2	N/A	14m	2.15m, 6.26m, 24m	98.23µ / 0.98	15.55–2.49	27.8m–0.278	2m / 0.21
NEF	8.2	6.97	2.57m	46.3-6.92	59.5µ / 104.1µ	30.15	258.5-21.7	155.8 / 22m	2 / 5.33	73.01	N/A

N/A Not Available; (1) Estimated from available data; (2) Integrated noise from 1 Hz to 10 Hz/1 kHz; (3) values for 1 pixel.

3.2. MULTIPLICATION STAGE

Following with the front-end structure (Figure 3.1), the impedance sensor signal $V_{sens}(f_0, \theta)$ once has been amplified must go through a mixer driven by a f_0 square reference signal V_{sq} (Figure 3.13a).

3.2.1. Design

Focusing on a single fully differential mixer topology, the simplest mixer stage is implemented by means of passive NMOS switches controlled by complementary V_{sq}, $\overline{V_{sq}}$ signals as shown in Figure 3.13b. Note that if transistors M_2 are substituted by PMOS transistors, as shown in Figure 3.13c, it is possible to simplify the structure to operate with a single reference signal. However, this approach requires a high level of matching between both the PMOS and the NMOS transistors to achieve an accurate operation.

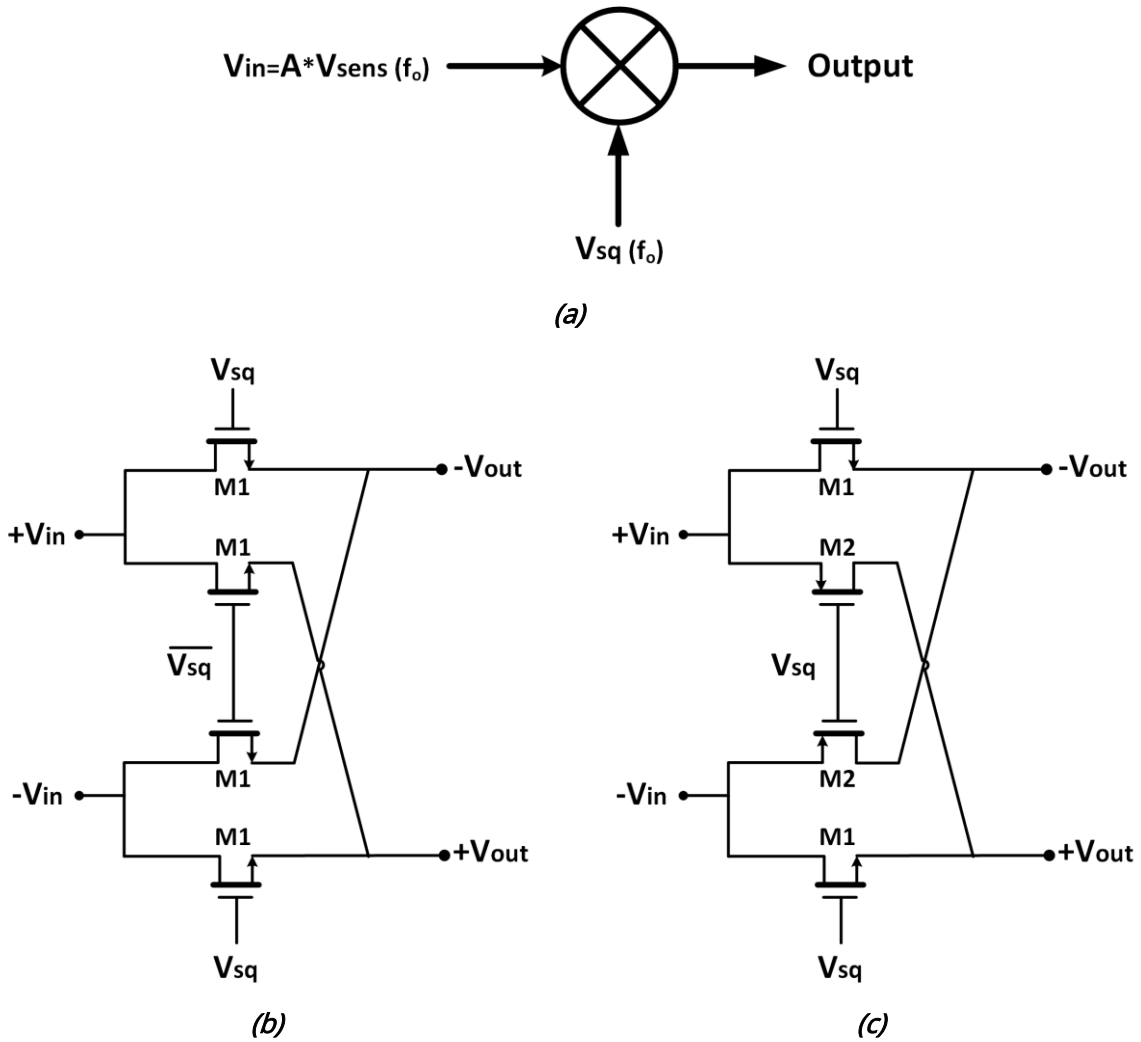


Figure 3.13. Mixer implemented with passive MOS switches: a) symbol; schematic of: b) NMOS implementation and c) NMOS-PMOS implementation.

An alternative solution consists in embed the mixer within the previous amplifying stage [15, 16]. In this way, a more compact topology is achieved. Specifically, considering the TC-TI based VGA structure early presented in Section 3.1.23.1.2 (shown again in Figure 3.14a), the proposed embedded mixer VGA architecture is the one modified as shown in Figure 3.14b.

The output TI branches are split into two, with an extra M_3 transistor –with size (2.5/0.18) in (μm/μm)– on each branch. These M_3 transistors are matched transistors driven by complementary reference V_{sq} and $\overline{V_{sq}}$ square signals, operating at the same frequency (f_0) as the amplified input sensor signals. The drains are cross-connected to each output, so when one branch is active the other is not and vice versa, achieving multiplication at the output as for the mixer in Figure 3.13b.

The power consumption is 180.4 μW, the same as with the simple VGA, while it keeps the bandwidth higher than 100 MHz and a 6-26 dB variable gain. Therefore, we achieve multiplication without increasing power consumption, with minimum area penalty, and keeping the main operating conditions.

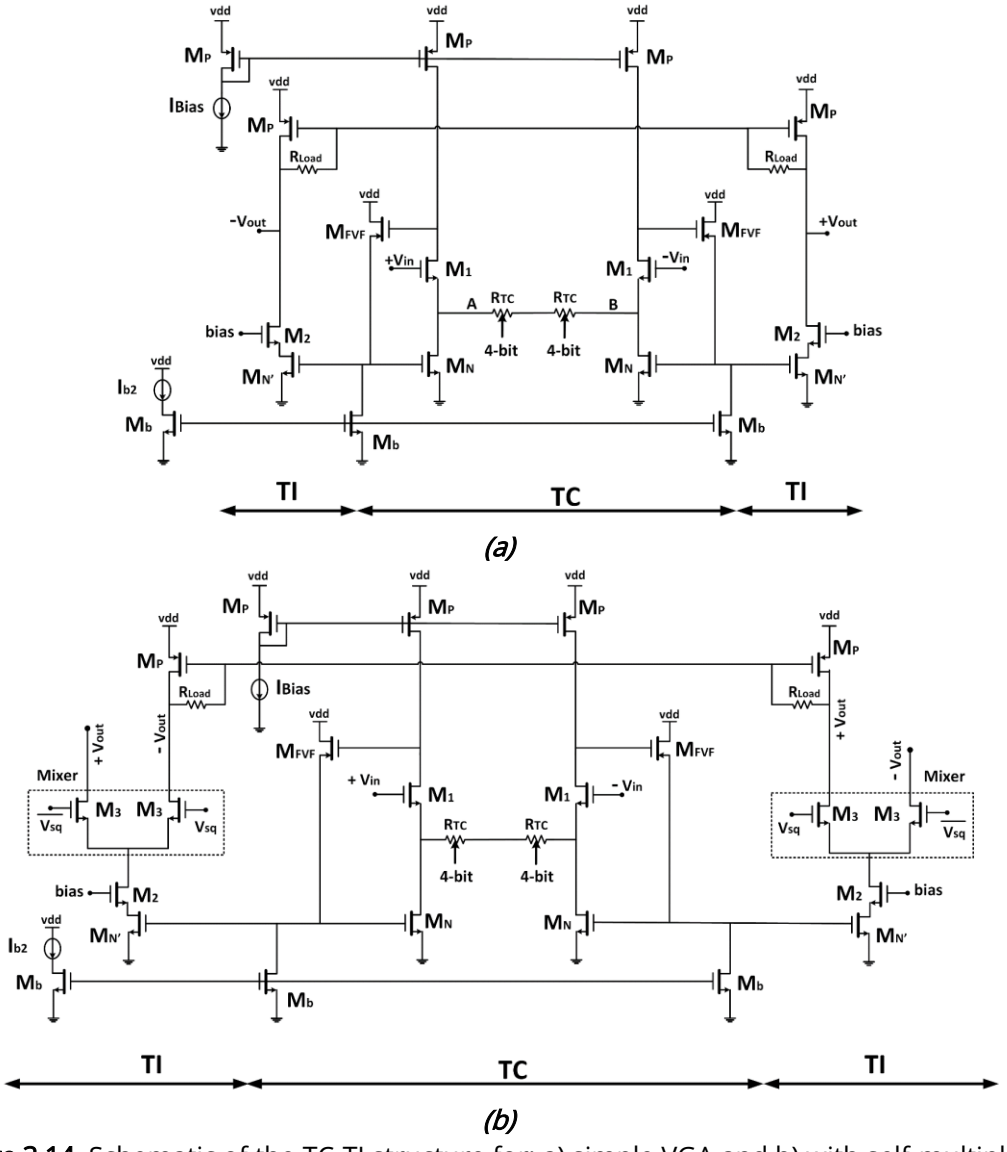


Figure 3.14. Schematic of the TC-TI structure for: a) simple VGA and b) with self-multiplication.

The layout view and microphotograph of the proposed topology is shown in Figure 3.15. The total active area is 52.9 µm x 115.4 µm (0.0061 mm^2).

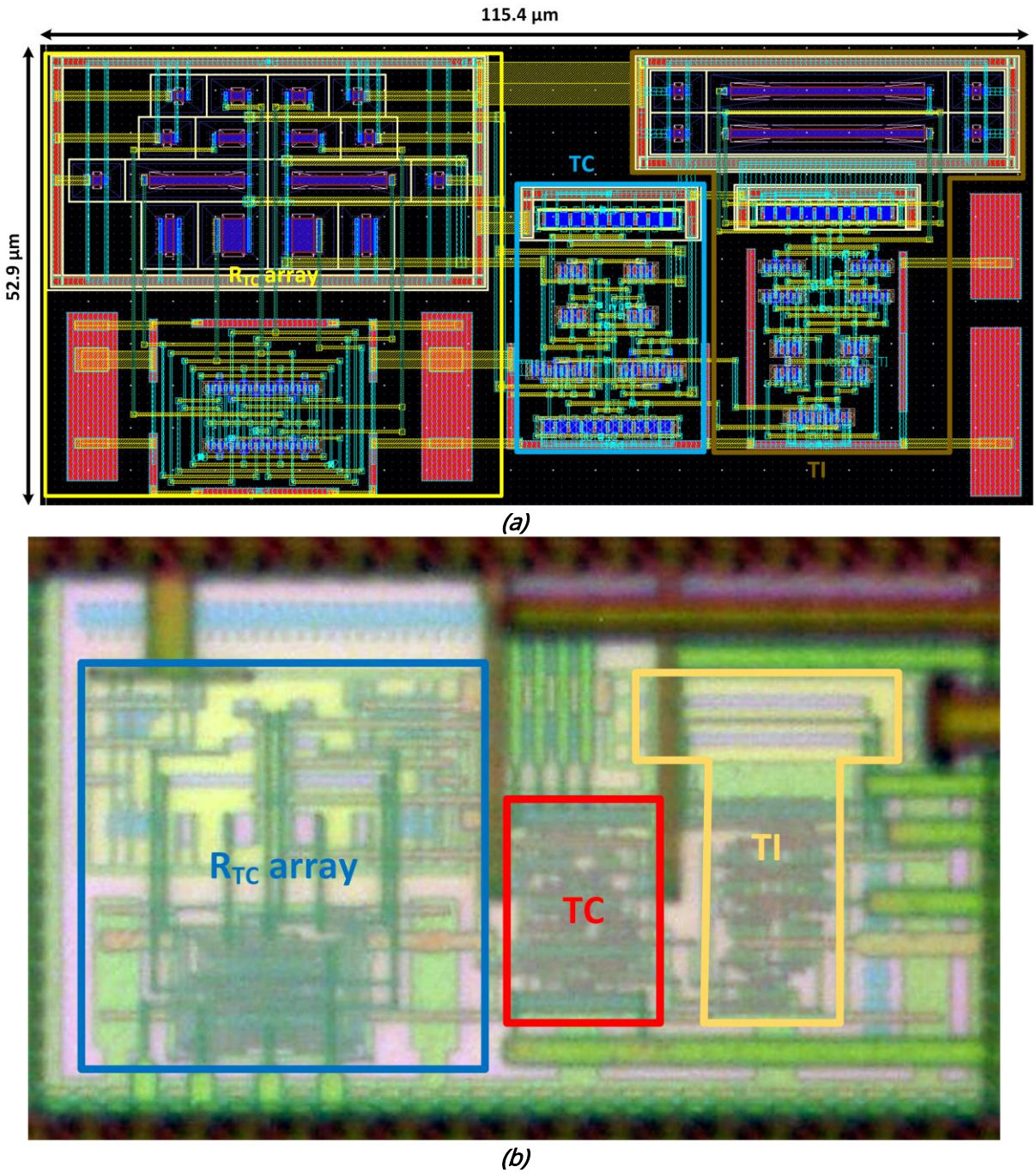


Figure 3.15. a) Layout view and b) microphotograph of the proposed VGA self-multiplied cell.

3.2.2. Characterization

The post-layout simulation results of the VGA-mixer cell are next presented. Gain-bandwidth, linearity and noise are characterized for V_{sq} = 1.8 V and $\overline{V_{sq}}$ = 0 V, to validate that performance is not modified under introduction of the embedded mixer topology, and a transient performance characterization is added to verify the mixer operation.

Gain and bandwidth

Figure 3.16a shows the differential gain frequency response at 5.9 dB (a3), 15.8 dB (a2), 20.7 dB (a1) and 26 dB (a0), exhibiting a bandwidth higher than 100 MHz for all gain configurations.

The sweep over the temperature (from -40ºC to 120ºC) for maximum and minimum gain conditions reports (Figure 3.17) a variation of 0.015 dB/ºC for maximum gain, and $62*10^{-5}$ dB/ºC for minimum gain, while the bandwidth varies 170 kHz/ºC and 410 kHz/ºC respectively.

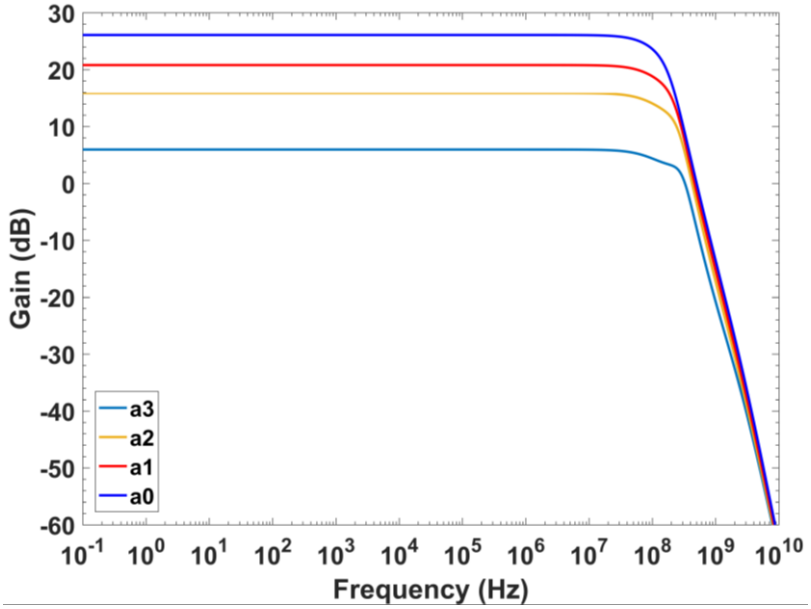


Figure 3.16. Frequency response for different gain configurations.

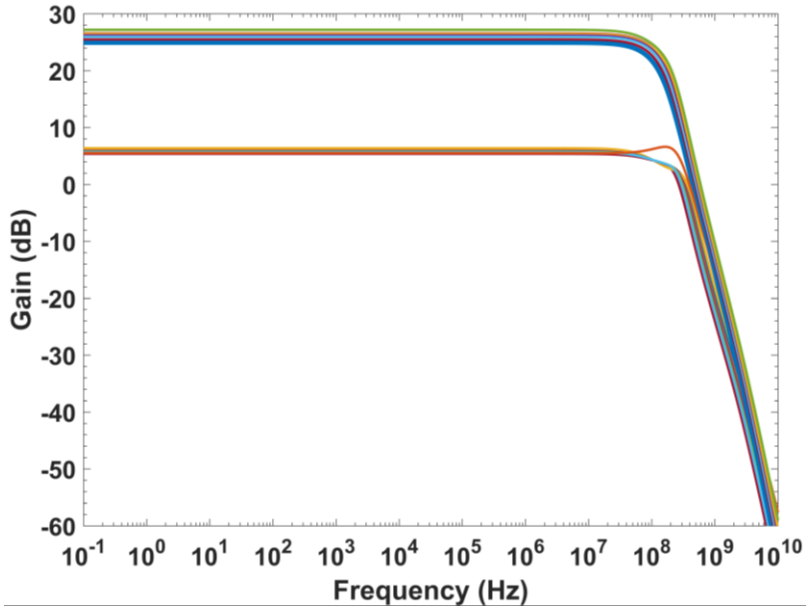


Figure 3.17. Frequency response for maximum and minimum gain, at different temperatures (from -40ºC to 120ºC).

Transient performance

Figure 3.18 presents the demodulated output signal from a 1 mV amplitude input signal operating at $f_{in} = f_0 = 10$ MHz, for maximum gain (26 dB, Figure 3.18a) and minimum gain (5.9 dB, Figure 3.18b). The spikes observed in the output signals are produced by the rise and fall transitions of the square signals V_{sq} and $\overline{V_{sq}}$.

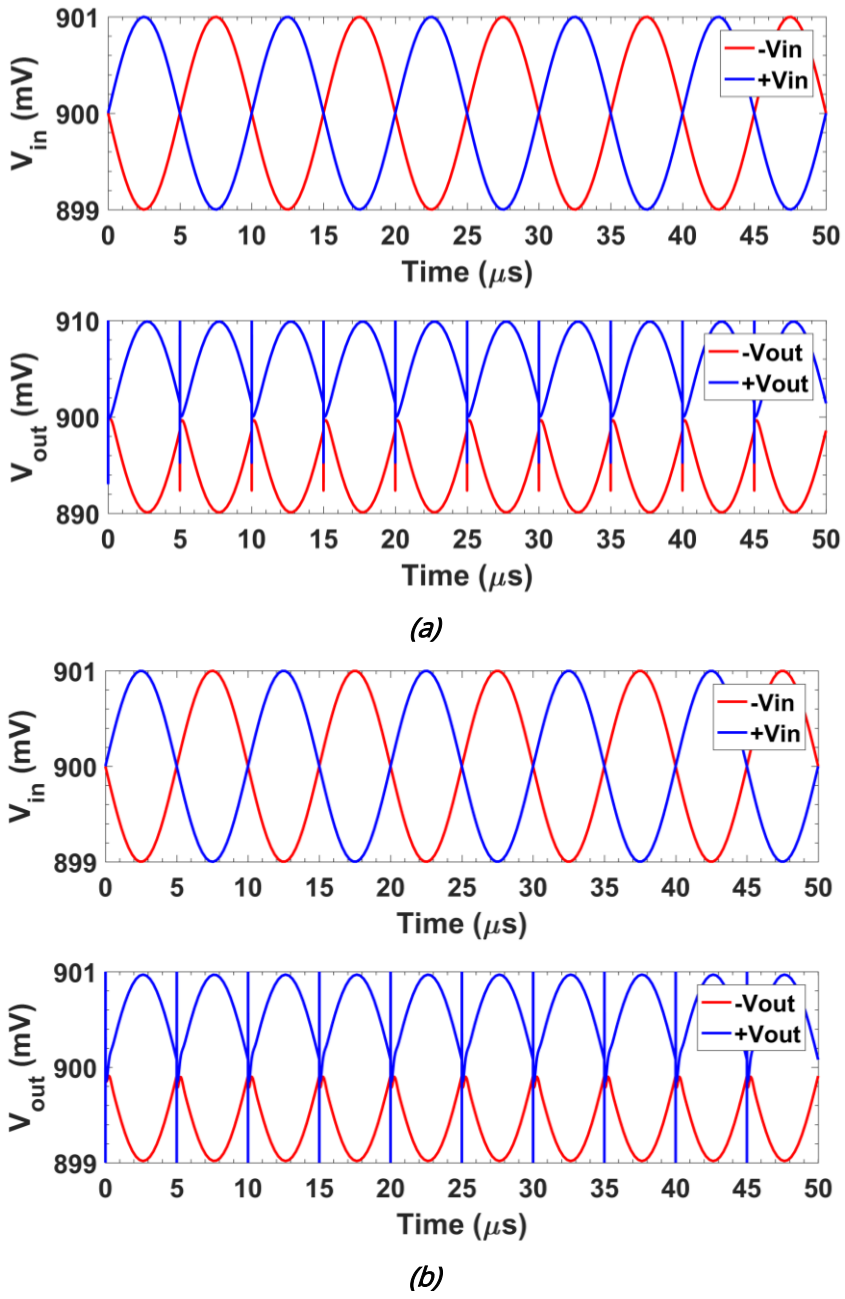


Figure 3.18. Transient behaviour at: a) maximum gain; and b) minimum gain.

Noise

The integrated noise over the frequency range for both maximum and minimum gain is reported in Table 3.4.

Table 3.4. Integrated noise of the Variable Gain Amplifier.

Gain	26 dB	5.9 dB
BW (Hz)	0.1-100M	0.1-100M
out (mV_{rms})	1.776	1.138
In (V_{rms})	89.0μ	576.9μ
In (V/√Hz)	8.9n	57.7n

3.3. FILTERING STAGE

The last front-end stage is a LPF section, which acts as a DC magnitude extractor. Assuming that all the electronics prior to the filter present low noise performance, the accuracy in the recovery largely depends on the LPF cutoff frequency $f_{c,L}$. In this sense, a LIA can be understood as a band-pass filter with central frequency f_0 and a very high quality factor $Q = (f_0/f_{c,L})$, where $f_{c,L}$ is the bandwidth of the output low-pass filter. Hence, the smaller the LPF cutoff frequency, the better the noise rejection and the better the recovery accuracy, but a compromise arises to the related acquisition times.

The design of such LPFs with very low cutoff frequencies in a fully integrated way with high performance, compact size and low-power consumption poses significant challenges. In fact, in recent years, there has been significant research efforts towards the development of such LPFs, boosted mainly because of their application in biomedical systems [17-20], where it is necessary to low pass filter the signal over the frequencies of interest –typically in the 100 mHz to 1 kHz range– to remove noise before digitizing it for further processing. Consequently, there is a vast amount of literature on integrated low pass filters with low-cutoff frequencies focused on biological signal processing. They are mainly based on G_m–C approach [21–35] due to its simplicity, resulting in better suitability for low-voltage low-power operation.

However, reviewing these proposals, besides not strictly presenting a tuneable frequency over our target sub-Hz to Hz range (5.4 kHz [21], from 2 kHz to 20 kHz [22]), some of them exhibit a power consumption rather high to be integrated within multichannel systems: ([23] consumes 75.9 μW, [24] from 59.5 μW to 90 μW, and [25] 105.3 μW including a buffer). Among those that are power-efficient, either area is jeopardized, restricting their use within portable devices (an area of 0.336 mm^2 is reported in [26], 0.2 mm^2 in [27, 28] has an external 10 nF capacitor, [29] has an area of 1 mm^2, and an area of 0.24 mm^2 is reported in [30]), or dynamic range is jeopardized (34 dB [21] and 49.9 dB [31]), whereas others achieve such low power thanks to bias currents in the order of pA or a few nA, which are difficult to be reliably generated on-chip (from 300 pA to 900 pA [32], from 90 pA to 430 pA [33], in [34] two bias currents are used

ranging from 200 pA to 4 nA and from 1 nA to 20 nA respectively, and from 250 pA to 25 nA [35]), existing on the overall power-area-dynamic range trade-off.

Thus, a novel low pass filter is needed that satisfies all the required specifications for its operation as a DC extractor in a portable multichannel IS measurement system.

3.3.1. G_m-reduction techniques

Considering the G_m-C approach, to achieve very low cut-off frequencies (<Hz) with an integrable capacitor (C ≅ 50 pF), the use of G_m-reduction techniques is mandatory. Among the reviewed literature [17, 20, 27-29, 34-37], different techniques can be found, form the simplest (operation in triode region, bulk-driven, source degeneration) to the more specific Voltage Attenuation, Current Cancellation, and Current Attenuation.

Voltage Attenuation

This technique uses a voltage attenuator at the input of the OTA (Figure 3.19) to reduce the equivalent transconductance, given by

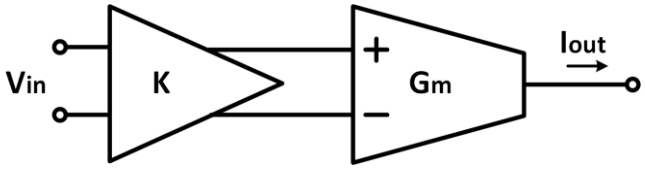


Figure 3.19. Attenuation voltage diagram. Based on [38].

$$G_{m,eq} = KG_m \tag{3.7}$$

This technique also increases the input linear range, but requires a proper DC bias voltage at the input of the transconductance cell [39]. One example of voltage attenuation found in the literature is [35]; however, it uses very low bias currents -ranging from 250 pA up to 25 nA- deteriorating the overall dynamic range. In addition, it is composed of an N-stage cascade connection of one-third linear attenuators together with an ordinary nonlinear subthreshold transconductor, increasing the area consumption.

Current Cancellation

The current cancellation (CC) technique generates a current in the opposite direction to the current of the main transconductor as shown in Figure 3.20. In this way the equivalent transconductance is reduced to

$$G_m = G_{m1} - G_{m2} \tag{3.8}$$

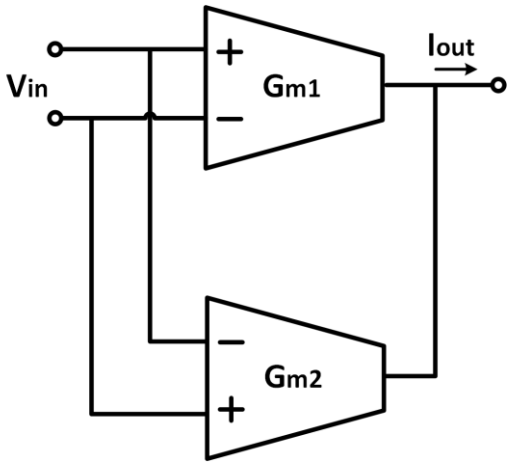


Figure 3.20. Current cancellation scheme. Based on [38].

The main drawback of this technique is the good matching required for a good operation as shown in [36], limiting the effective G_ms to the transistor mismatch while adding noise to the system [38].

Current Attenuation

The current attenuation technique uses an attenuation block to reduce the output current of the transconductor (Figure 3.21), so that the equivalent transconductance is given by

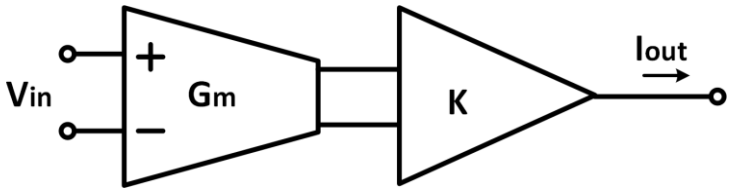


Figure 3.21. Current attenuation scheme. Based on [38].

With this technique the equivalent transconductance is given by

$$G_{m,eq} = kG_m \tag{3.9}$$

Current attenuation is applied with different methods such as series parallel (SP) division current and current division or current steering (CS).

Series Parallel

Series Parallel division current is one of the most common techniques to perform current attenuation. It reduces the current copied by the current mirrors by using a small copy factor (k<<1). The series parallel technique substitutes the simple current mirrors by sets of transistors in series and in parallel, as shown in Figure 3.22. If the size of these transistors are all the same –transistor unit M_u- then the X parallel transistors are equivalent to one transistor of size XM_u and the same happens with the Y series transistors. Therefore, the equivalent transconductance is given by

$$G_m = \frac{g_m}{XY} \tag{3.10}$$

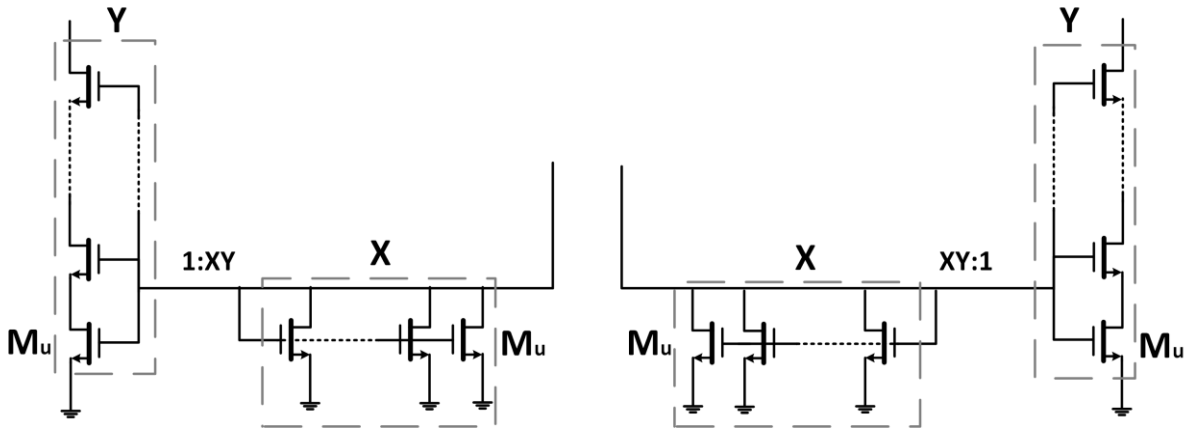


Figure 3.22. Generic Series-Parallel current mirror applied to a PMOS-input symmetrical OTA. Based on [27].

With a G_m reduced by a factor XY (k=1/XY), where g_m is the gates transconductance and X, Y the number of unit transistors M_u in parallel and in series respectively.

This method allows the implementation of a current divider as in [27], however it requires high area consumption and presents a trade-off between bias current and input linear range.

Current Steering

Finally, the Current Steering technique applied in Figure 3.23, steers current by means of two transistors operating in triode region acting as linear resistors, with their gate controlled by different voltages [17]. Both, the current division and thus, the effective transconductance can be controlled by varying these gate voltages.

This technique reports the best results in terms of G_m reduction and tunability while keeping the power and area consumption to a minimum, and thus will be the one adopted for the design of a sub-Hz Low Pass Filter, but translated to a G_m-C approach. In this way, a high impedance input node is achieved, which makes the coupling between stages straightforward.

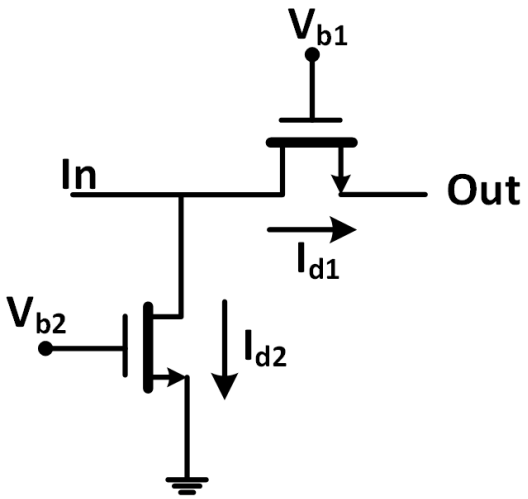


Figure 3.23. Current steering generic block.

Table 3.5. Current reduction techniques and equivalent transconductances.

Technique	Equivalent transconductance
Voltage Attenuation	$G_{m,eq} = KG_m$
Current Cancellation	$G_m = G_{m1} - G_{m2}$
Series Parallel	$G_m = g_m/XY$
Current steering	$G_m = (1-\alpha)g_{m1}$

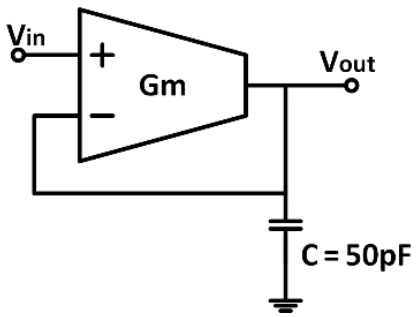
3.3.2. 1.8 V-LPF

In this section, the design and characterization of a1.8V - 0.18 µm CMOS monolithic low pass filter suitable to act as a DC magnitude extractor is presented. These results have been reported in [40].

Design

To fit within our measurement systems, the target LPF cutoff frequencies are in the sub-Hz to Hz range. Specifically, two configurable cutoff frequencies of 0.5 Hz and 5 Hz are set as specifications to bring flexibility to the system, adjusting the speed-accuracy trade-off. Besides, design guidelines are wide input range; low noise, to preserve high dynamic range; compact size (<0.1 mm^2) and minimum power consumption (<10 µW) with currents of the order of hundreds of nA to be reliably generated on-chip ($I_{Bias,nominal}$ = 500 nA).

A single-input single-output LPF is implemented, by a differential-input single-output G_m-C architecture in unity gain feedback configuration. The resulting closed-loop configuration maintains, without a specific G_m linearization technique, good linearity in the passband over all the input range while not degrading the noise [35], optimizing the dynamic range in this way. Note that for this scheme, when the input signal frequency is close to the filter cut-off frequency, there will be an important phase shift between both inputs of the transconductor, which will cause distortion. Therefore, it is not a general-purpose low-pass signal-processing filter, but a DC extractor for synchronously rectified signals operating at higher frequencies. Figure 3.24 shows the basic first order scheme and the corresponding transfer function, with a pole located at G_m/C [41]. The load capacitor value is set to 50 pF, considered the maximum practical on-chip capacitor.



$$H(s) = \frac{G_m}{sC + G_m} \tag{3.11}$$

Figure 3.24. First-order G_m-C low-pass filter and its corresponding transfer function.

Two structures have been implemented for a 1.8 V power supply: the basic integrator (Order-1 filter, O1F) in Figure 3.24 and a second-order LPF (Order-2 filter, O2F).

Transconductor Architecture

The transconductor core is the classic mirrored Operational Transconductance Amplifier (OTA) (Figure 3.25a). Its overall transconductance is given by $G_m = k*g_{m1}$, with g_{m1} the transconductance of the NMOS input differential pair M1 and k the gain factor of the current mirror. To keep an intrinsic reduced G_m value, the input pair is designed to have a small g_{m1} ~µS with a bias current I_{Bias} = 0.5 µA while unity gain (k = 1) current mirrors are used. Thus, this scheme provides the same gain $G_m = g_{m1}$ as the classical differential pair, but uncouples the input and output common-mode range at the cost of doubling the power consumption.

On the basis of this structure (Figure 3.25a), the idea is to keep constant the V–I conversion gain (g_m) so that the input NMOS differential pair is biased with a constant bias current introduced through a 1:2 current mirror, whereas a current steering technique is introduced in the output current transfer section to reduce the overall G_m.

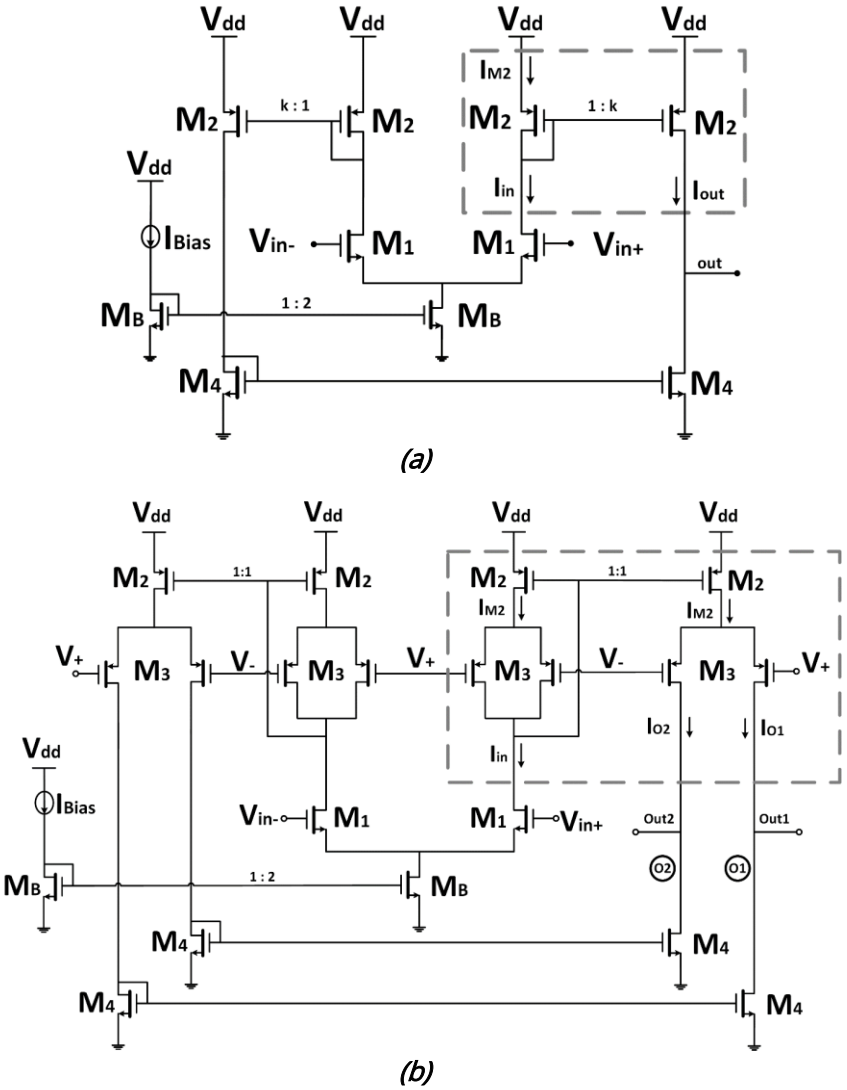


Figure 3.25. Schematic view of the OTA: a) Classic mirrored and; b) with current steering.

In this way, both G_m reduction and tuning is done in the transconductor output current transfer section, exploiting a current steering technique as the most suitable choice to effectively reduce the G_m, preserving a good overall performance tradeoff. In this way, all the requirements of a SoC high performance solution can be met simultaneously, bringing about a very competitive solution.

This is achieved by replacing the conventional M2 current mirrors by current steering M2–M3 high swing cascode current mirrors, as shown in Figure 3.25b. Transistors M2 remain equal, but cascode transistors M3 –both in the input and output branches– are split into identical transistors driven not by a constant V_C gate voltage but by complementary control voltages $V_{\pm} = V_C \pm V_{gc}$ [42], resulting in two output branches conveying complementary currents.

Note that transistors M2 present the same drain to source voltage and gate to source voltage, so that the current mirror operates properly, rendering unity gain current $I_{out} = I_{in}$. Then, the output current I_{out} is split into two complementary currents, I_{O1} and I_{O2}, whose fractional value α_i ($0 \leq \alpha_i \leq 1$) depends upon the differential control voltage V_{gc}

$$\begin{aligned} I_{out} &= I_{O1} + I_{O2,} \\ I_{O1} &= (1-\propto_i) I_{in}, \\ I_{O2} &= \propto_i I_{in}. \end{aligned} \tag{3.12}$$

Therefore, the transconductance gain for each output had complementary values:

$$\begin{aligned} G_{m_{O1}} &= (1-\propto_i) g_{m1} \\ G_{m_{O2}} &= \propto_i g_{m1} \end{aligned} \tag{3.13}$$

With $G_{mo1} + G_{mo2} = G_m = g_{m1.}$

The simulated behaviour of the DC current splitting over the control voltage variation is shown in Figure 3.26a, for $V_{gc} > 0$ (the figure is complementary for $V_{gc} < 0$). Voltage $V_C = 1.2$ V, and the tuning voltage variation V_{gc} ranges from 0 up to ~200 mV, to keep the output offset bounded below ±1 % and a DC gain error below 0.5 dB. Note that for $V_{gc} = 0$, $I_{O1} = I_{O2} = I_{Bias}/2 = 250$ nA; for $V_{gc} > 0$, $I_{O1} < I_{O2}$; for $V_{gc} < 0$, $I_{O1} > I_{O2}$ and the complementary division is obtained [42].

The simulated transconductance variation in both branches O1 and O2 is shown in Figure 3.26b. Initially, transistors $M3_{O1}$ and $M3_{O2}$ are in saturation, strong inversion, and I_{O1} and I_{O2} follow a linear relation with V_{gc} (up to ≈50 mV). Transistor $M3_{O2}$ remain in strong saturation over all V_{gc} variation, but for approximately $V_{gc} > 50$ mV, $M3_{O1}$ enters the weak inversion regime, and thus its current has an exponential relationship with V_{gc} and therefore the transconductance for O1 follows a linear dependence with V_{gc} in a logarithmic scale, as it can be seen in the figure. Figure 3.26c shows the G_m experimental characterization, validating the simulation results (Figure 3.26b).

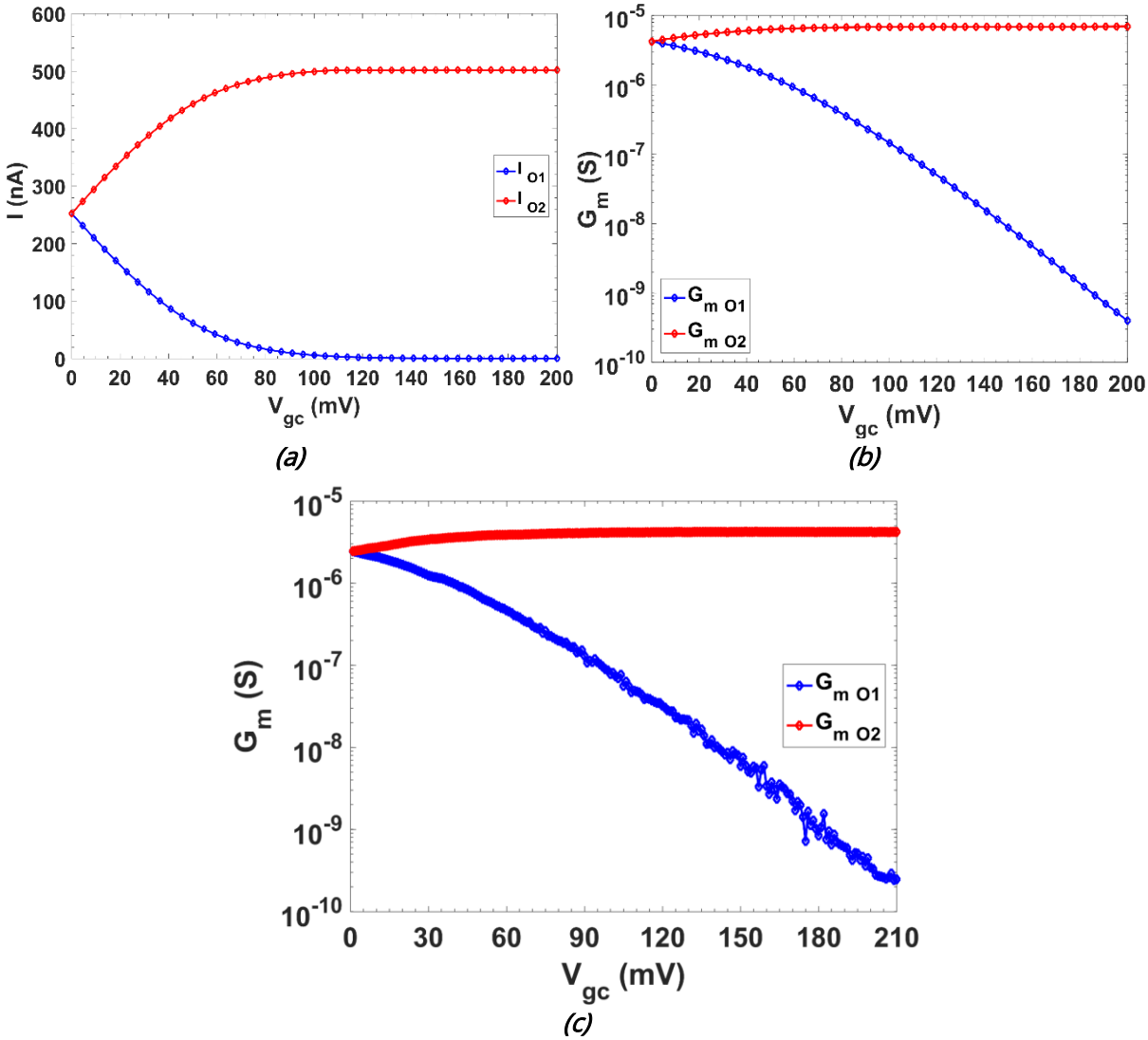


Figure 3.26. Simulated behaviour of a) current and b) G_m over V_{gc} for branches O1 and O2; c) experimental G_m over V_{gc}.

O1-Filter: O1F

The schematic of the basic unity gain integrator, named O1F, is shown in Figure 3.27a. The schematic of the basic unity gain integrator, named O1F, based on the OTA in Figure **3.25**b, is shown in Figure 3.27a. For the output stage, two conventional NMOS cascode current mirrors generate the complementary outputs O1 and O2 to better fit the required common-mode voltage of $V_{cm} = V_{dd}/2 = 0.9$V at the output nodes. Output O1 is selected as the integrator output, and output O2 is kept at $V_{dd}/2$ to preserve symmetry and assure linear current division in the output branches.

Transistor sizes (in µm/µm) are M1 = 7.5/10, M2 = 10/4, M3 = 5/4, M4 = 1/4, MB = 2/10, and MB' = 4/10. It has a 1.8 V supply voltage with a common mode $V_{cm} = V_{dd}/2 = 0.9$ V, the bias current—externally generated—is set to 0.5 µA, with a total power consumption of 5.4 µW. The reason for using such transistor lengths is, on one hand, to reduce the input-referred noise at the differential input pair, and on the other hand, to achieve a small W/L ratio reducing the input pair g_m while operating in saturation with bias currents ~µA.

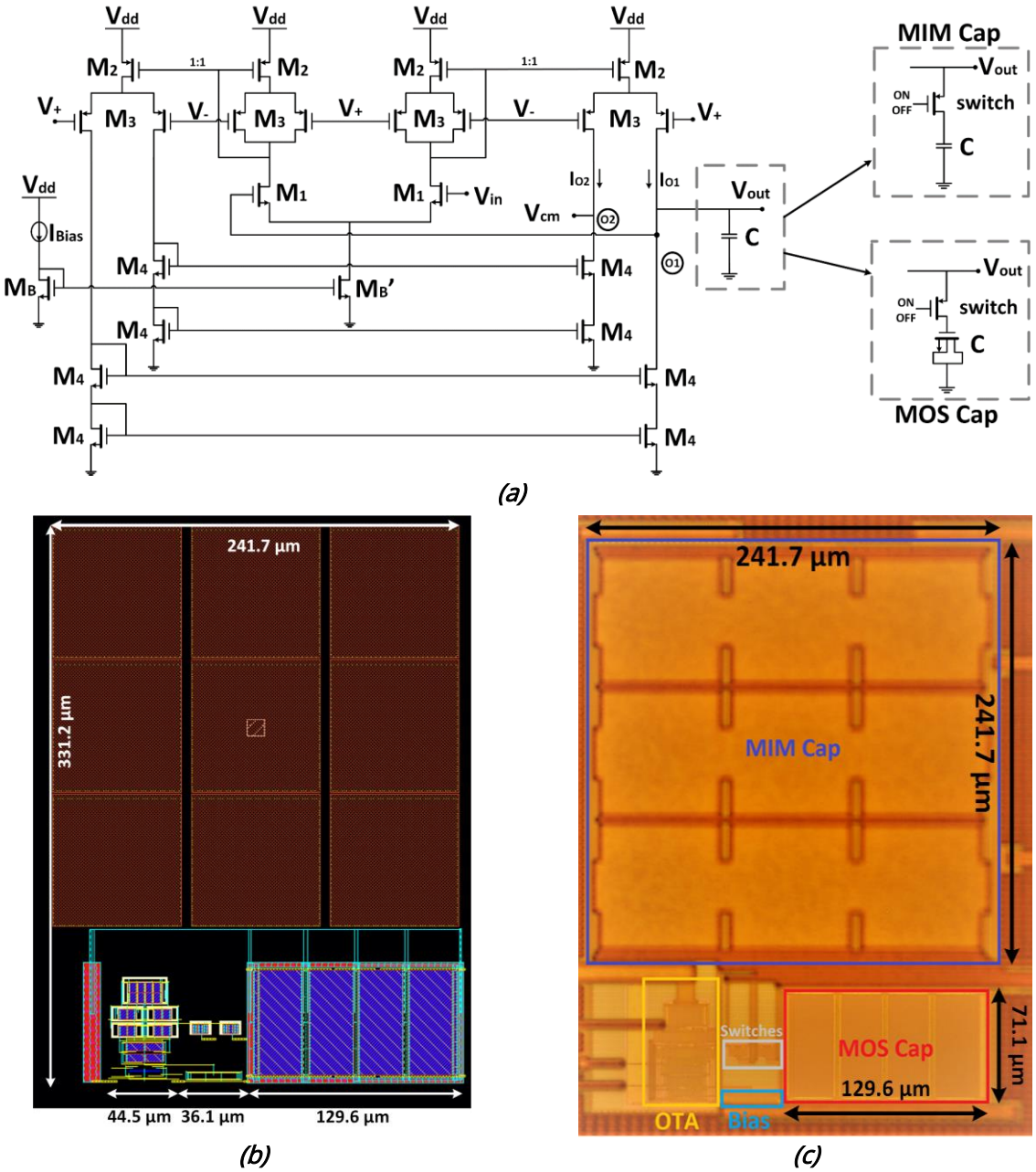


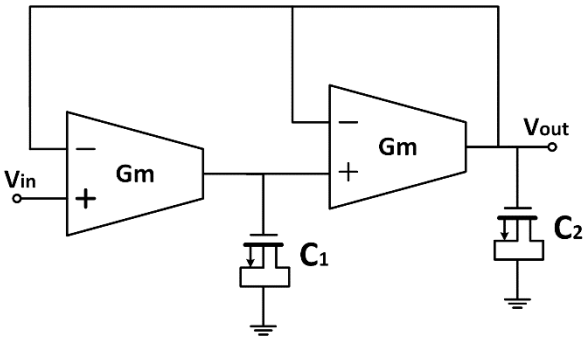
Figure 3.27. O1F a) proposed integrated circuit; b) layout view and c) microphotograph. *MIM: Metal-Insulator-Metal.

Both a MIM and a MOS capacitor are considered, so that a performance comparison can be made. For the MOS capacitor, implemented by a PMOS with size 242 µm/25 µm, the capacitance variation over the output voltage shows that from 0.4 V to V_{dd} it has a constant 50 pF capacitance.

Figure 3.27b presents the layout view and Figure 3.27c the microphotograph of the integrated O1F. A clear advantage of using a MOS capacitor instead of an MIM capacitor is the great save in area (a reduction of the 85 %, being the total active area with the MOS capacitor 0.0140 mm^2).

O2-Filter: O2F

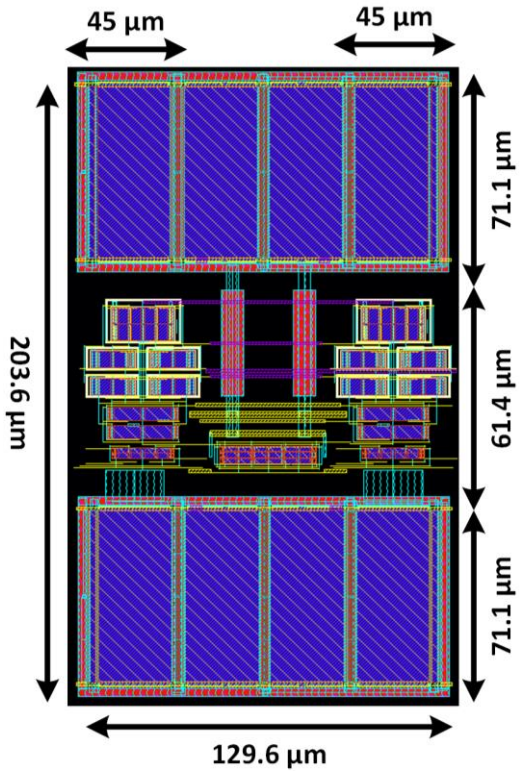
The second order filter, named O2F, is also a unity gain scheme based on [27(Sensors'19)] with a quality factor Q = 1/√2 given by $C_2 = 0.5C_1$, C_1 = 50 pF, both of them implemented as MOS capacitors. Figure 3.28a shows its structure as well as its quality factor and cutoff frequency, where each G_m structure is identical to the one reported in the previous subsection, again with a bias current of 0.5 µA, thus the total power consumption is 9.9 µW. The layout viewn and microphotograph are shown in Figure 3.28b and Figure 3.28c.



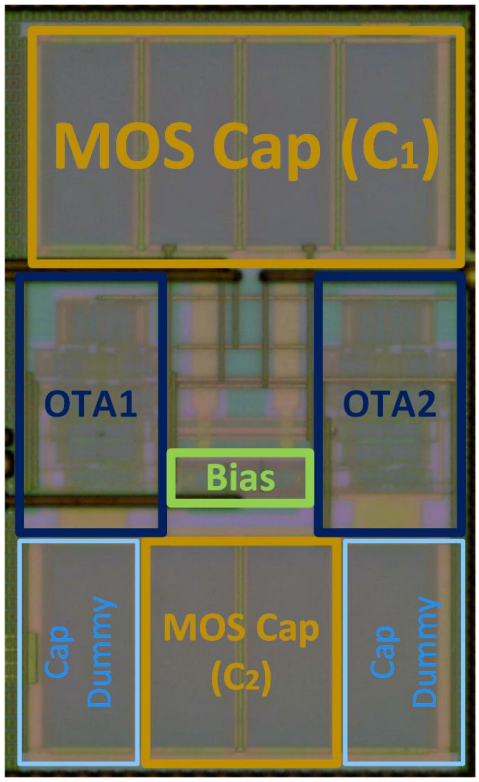
$$Q = \sqrt{\frac{C_2}{C_1}} \tag{3.14}$$

$$f_C = \frac{1}{2\pi}\sqrt{\frac{{G_m}^2}{C_1 * C_2}} \tag{3.15}$$

(a)



(b)



(c)

Figure 3.28. Proposed O2F a) schematic with Q-factor and upper-band limit; b) layout view and c) microphotograph.

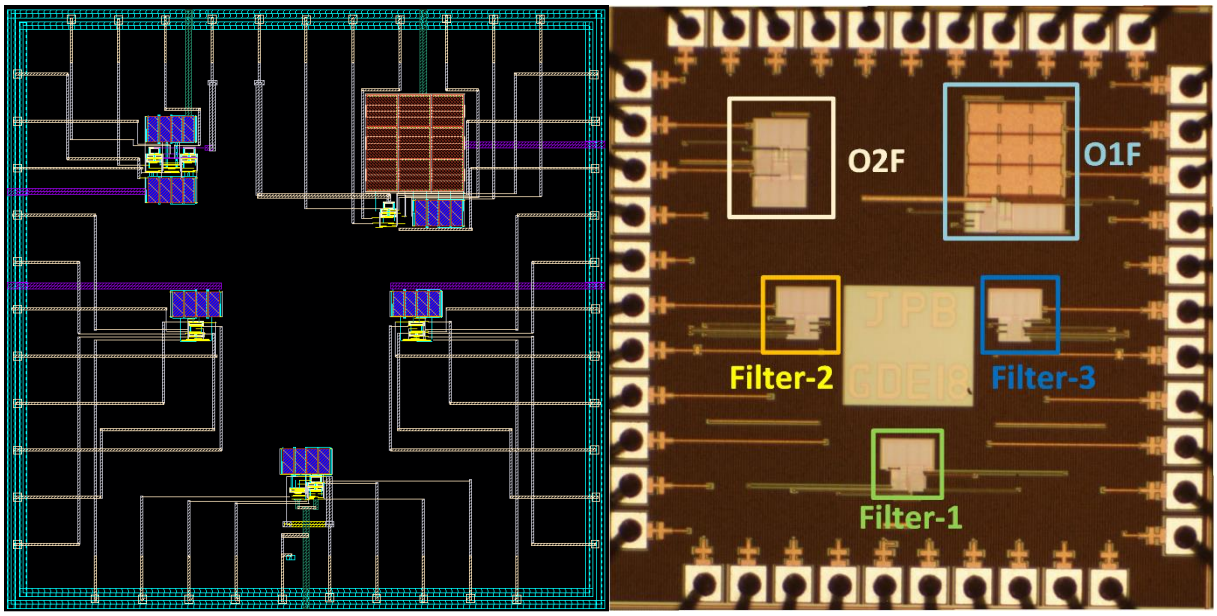
Characterization

Setup

To perform the experimental characterization of the integrated low pass filters, integrated in a single die (Figure 3.29), a printed circuit board (PCB) (Figure 3.30) have been designed. In Figure 3.31, it is shown the measurement setup –both the experimental setup (Figure 3.31a) and the block diagram (Figure 3.31b)– for the characterization of the main parameters of the circuits: tunability, cutoff frequency range, V_{in}–V_{out} characteristic, quiescent current, and linearity.

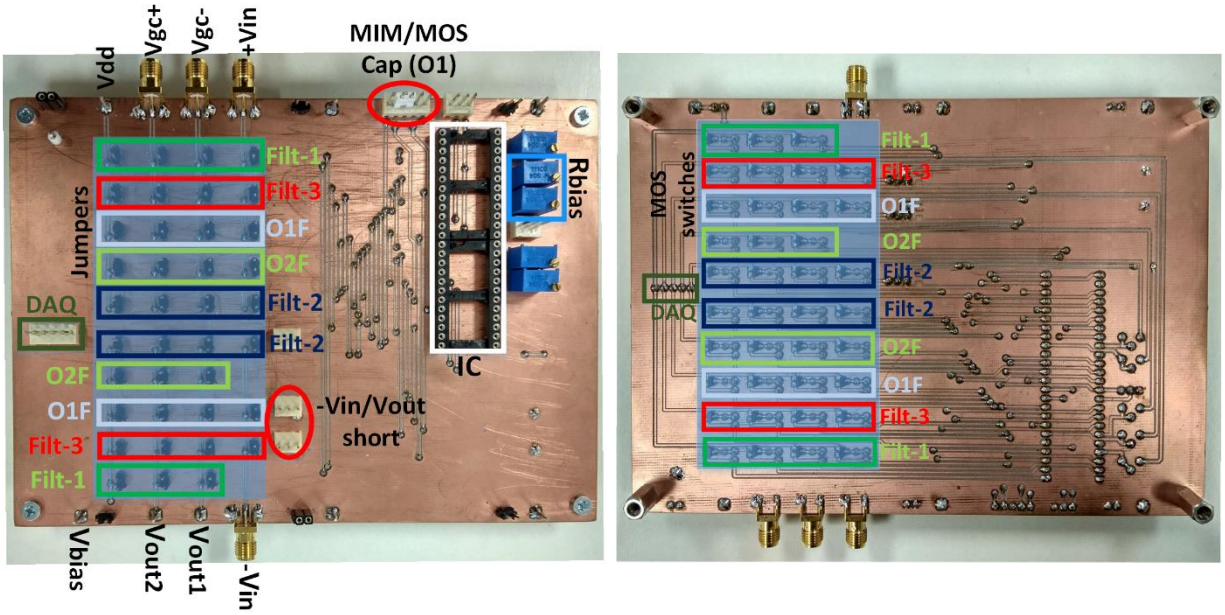
The integrated die has five separated circuits, as can be seen in Figure 3.29, corresponding to five integrated LPFs (the two presented here and three low-voltage versions reported in [**43**]) using a total of 43 pins out of the 48 existing in the packaging used (48-DIL, Dual-In-Line). All of the circuits have a common ground, but they have been biased through different input pins, as they operate at different supply voltages.

The PCB shown in Figure 3.30 has been designed with a set of jumpers (front) and switches (rear) to select, either manually or automatically with a data acquisition card (DAQ) NI-USB 6008, the circuit to be characterized without compromising the other circuits in the die. For the switches, a low impedance NMOS transistor IRFML8244 (R_{DS} = 41 mΩ, drain-to-source resistance) with their gates connected to the digital outputs of the DAQ has been used.



(a) *(b)*

Figure 3.29. a) Layout view and b) microphotography of the integrated circuit (IC), with each filter highlighted in a different colour.

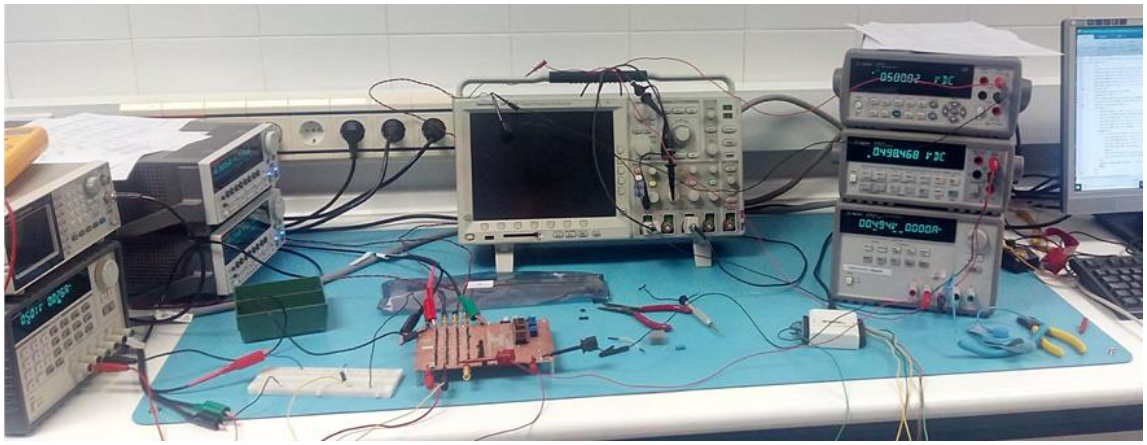


(a) *(b)*

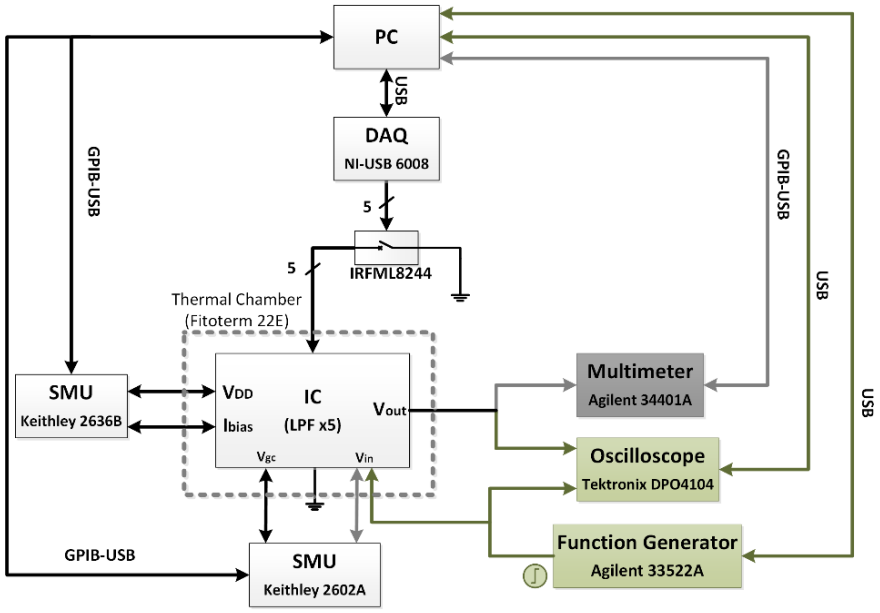
Figure 3.30. Detail of the printed circuit board test: a) front and b) rear.

In addition, there are jumpers to connect the MIM or MOS capacitor and to shortcut V_{in} with V_{out} for the O1F and Filter-3 so they can be tested as OTAs and as filters.

One channel of a dual source measurement unit (SMU) Keithley 2636B sets the voltage supply to the corresponding activated LPF, and the bias current is supplied to the circuit using the other channel. A second dual SMU is used to provide the control voltage V_{gc} and the input voltage V_{in} in the static characterization. A 34401A Agilent 6½ digital multimeter (DMM) is used to read the DC output voltage, V_{out}. For the dynamic characterization, an Agilent 3352A arbitrary waveform generator (AWG) provides the input voltage, and the transient input and output signals are read through a DPO4104 Tektronix oscilloscope. All the instrumentation is connected to a PC, having the measurement process automatized. Figure 3.31b shows in grey the instrumentation used for the static characterization and in green the instrumentation used for the dynamic characterization.



(a)



(b)

Figure 3.31. Measurement setup for the characterization of the low pass filters: a) experimental setup; and b) block diagram of static (grey) behaviour and dynamic (green) behaviour. SMU: source measurement unit, DAQ: data acquisition card.

The complementary control voltages are provided with an SMU to keep a tight control of their values and study the dependence of the filters parameters with them. However, in order to provide a portable device, this solution is not realistic, and different approaches can be employed to substitute the SMUs, either using commercial components such as a digital potentiometer [**44**], a digital-to-analog converter (DAC) [**45, 46**], or with a microcontroller (μC) if it is used to generate the excitation signal or to read the filtered signals from the LPFs; otherwise, it is also possible to use a specific integrated circuit (IC) to generate these voltages [**47, 48**].

G_m-C LPF Cutoff Tunability

Figure 3.32 shows the filters cutoff frequencies by steeping V_{gc} in 10 mV steps. The cutoff frequency of the O1F implemented with a MOS capacitor can be tuned from 66 mHz (V_{gc}= 210 mV) up to 2.5 kHz (V_{gc}= 0 mV). On the other hand, if a MIM capacitor is used, the cutoff frequency can be tuned from 66 mHz up to 1.2 kHz, achieving similar results to the ones obtained with the MOS capacitor. Thus, MOS capacitor is the most suitable choice, as it renders a comparable frequency range but with the advantage of significantly saving area. The cutoff frequency of the O2F can be tuned from 157 mHz (V_{gc} = 220 mV) up to 5.2 kHz (V_{gc} = 0 mV). Thus, the target frequencies of 0.5 Hz and 5 Hz initially established are within the ranges of both filters.

Through simulation, it has been verified that both target cutoff frequencies can be met even against PT-variations (V_{dd} is assumed to be provided by a LDO regulator [**49**]). Experimentally, to study the influence of the temperature over the cutoff frequency, the Fitoterm 22E thermal chamber has been used to sweep the temperature from −40 °C to 100 °C. Despite the dependence with the temperature, it is possible to correct the variation produced by T and achieve a constant $f_{c,L}$ over all of the temperature range thanks to the tunability of the circuit. In Figure 3.33, it is shown the V_{gc} tuning needed to keep the cutoff frequency constant at 5 Hz for both filters.

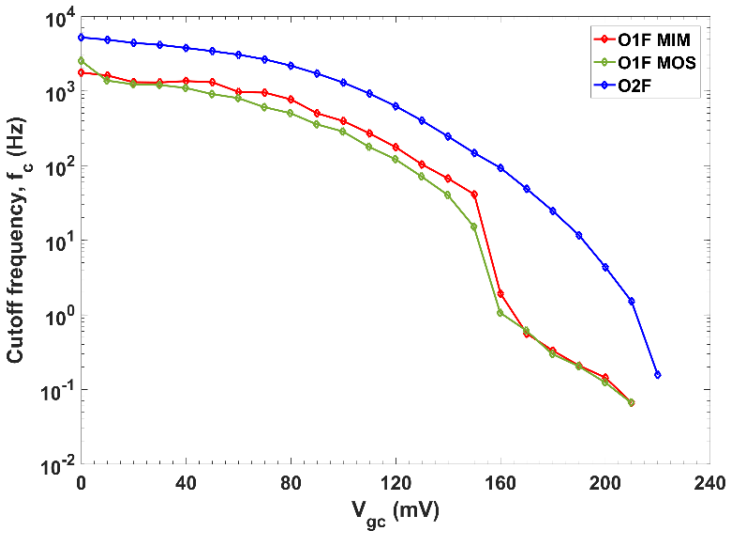


Figure 3.32. LPF cutoff frequencies for different V_{gc} values (O1F-MIM/MOS and O2F).

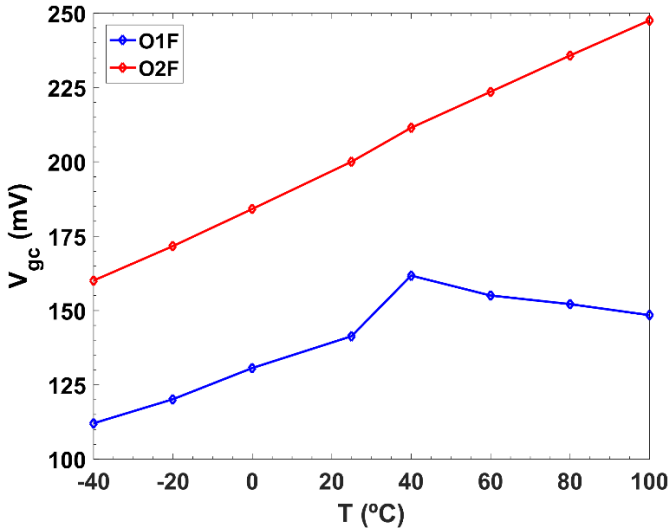


Figure 3.33. V_{gc} tuning over temperature to keep constant $f_{c,L}$ at 5 Hz (O1F-MOS/O2F).

DC Input/Output Characteristics

Focusing on our two target cutoff frequencies, 0.5 Hz and 5 Hz, Figure 3.34 shows the static V_{in}–V_{out} integrator transfer characteristic. Figure 3.34a,b presents detailed measurements of the input/output characteristics of filters O1F and O2F, respectively, for both target cutoff frequencies. Figure 3.34c shows for O2F, $f_{c,L}$ = 0.5 Hz, the oscilloscope caption of the output signal for a triangular input signal ranging from 0 to V_{dd}. These measurements have been done following the setup for static behaviour presented in Figure 3.31b, using the 34401A Agilent DMM to read the DC output voltage, and the 2602A Keithley SMU to generate and read the input voltage.

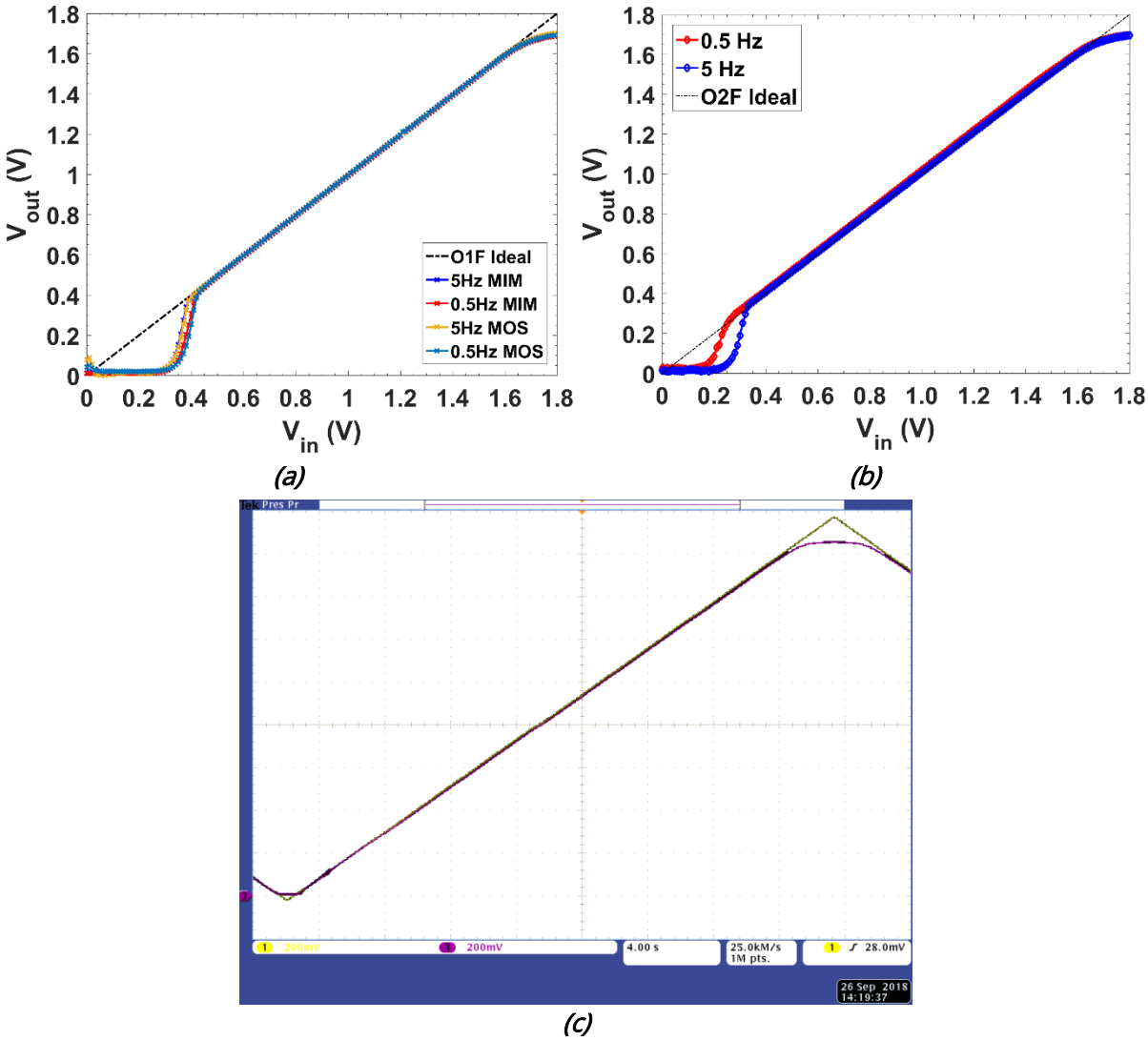


Figure 3.34. DC input/output characteristic with $f_{c,L}$ 0.5 Hz and 5 Hz for: a) O1F, b) O2F, and c) oscilloscope caption of O2F for $f_{c,L}$ = 0.5 Hz. Scale (only for Figure 3.34c): 200 mV/square and 4 s/square.

The linear input range is 0.43 V (0.45 V-MOS) to 1.65 V ($f_{c,L}$ = 0.5 Hz), and 0.39 V (0.45 V-MOS) to 1.67 V ($f_{c,L}$ = 5 Hz) for O1F (Figure 3.34a), whereas for O2F (Figure 3.34b), it ranges from 0.45 V to 1.65 V and 0.45 V to 1.67 V for $f_{c,L}$ = 0.5 Hz and 5 Hz, respectively. Note that this will not affect the achieved dynamic range, as will be shown next.

Dynamic Range

The total harmonic distortion (THD) as a function of the peak-to-peak amplitude is shown in Figure 3.35. The setup measurement follows the green setup of Figure 3.31b, which corresponds with the setup for the dynamic behaviour. A sinusoidal input signal at a frequency $f_{c,L}$/5 and with variable amplitude is generated with the 33522A Agilent AWG, whereas the DPO4104 Tektronix oscilloscope measures the output signal. The FFT of the output signal has been recovered, computing the THD for each amplitude of the input signal.

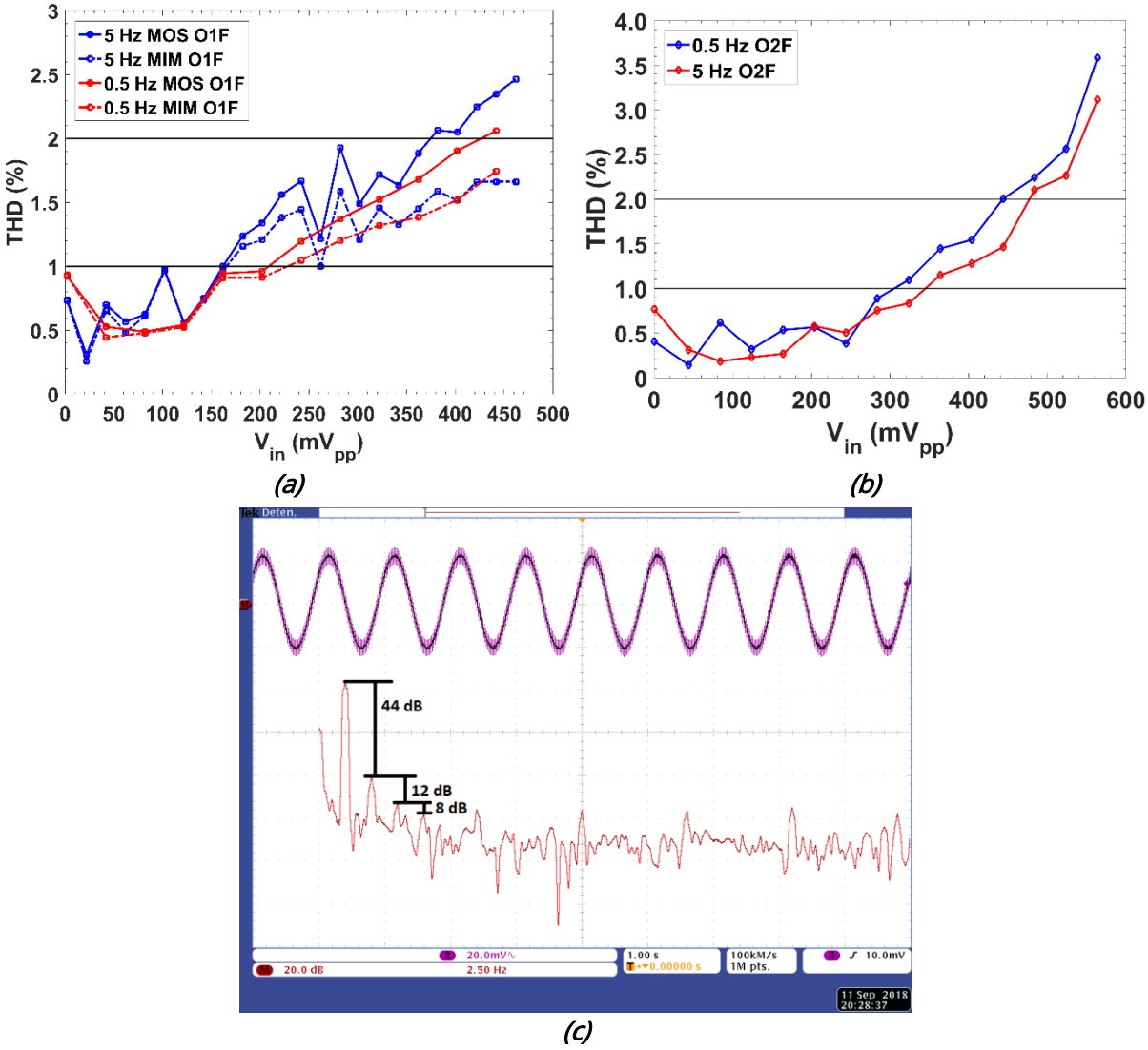


Figure 3.35. Total harmonic distortion (THD) versus input voltage peak to peak for a) O1F and b) O2F; and c) detail of the frequency spectrum for O1F MIM-Cap. ($f_{c,L}$ = 5 Hz, f_{in} = $f_{c,L}$/5, amplitude 41 mV_{pp}).

For O1F, THD is below 1 % at a frequency $f_{c,L}$/5 up to 210 mV_{pp} in the cases of $f_{c,L}$ = 0.5 Hz and up to 162 mV_{pp} in the cases of $f_{c,L}$ = 5 Hz (Figure 3.35a). For O2F, THD is below 1 % at $f_{c,L}$/5, for amplitudes up to 305 mV_{pp} and 345 mV_{pp} for $f_{c,L}$ = 0.5 Hz and 5 Hz, respectively (Figure 3.35b). The THD for the filter using a MIM capacitor presents similar values as with the MOS capacitor.

Figure 3.35c shows a detailed view of the frequency spectrum for one of the THD values shown in Figure 3.35a. It shows the input signal (in blue) with a 41 mV_{pp} amplitude and a 1 Hz frequency coupled with the 50 Hz line signal. The math function (in red) represents the FFT of the signal after being filtered by O1F with a 5 Hz cutoff frequency. From Figure 3.35c, after processing the FFT, the THD obtained is 0.65 %, which corresponds with the O1F-5 Hz MIM-Cap. value of Figure 3.35a.

The rms (root mean square) noise is obtained through simulation (Figure 3.36) of the extracted views of each circuit over an integration band of 10 kHz. Values for cutoff frequencies of 0.5 Hz and 5 Hz are, respectively: 13.3 μV_{rms} and 16.3 μV_{rms} for O1F, and 19.2 μV_{rms} and 19.9 μV_{rms} for O2F.

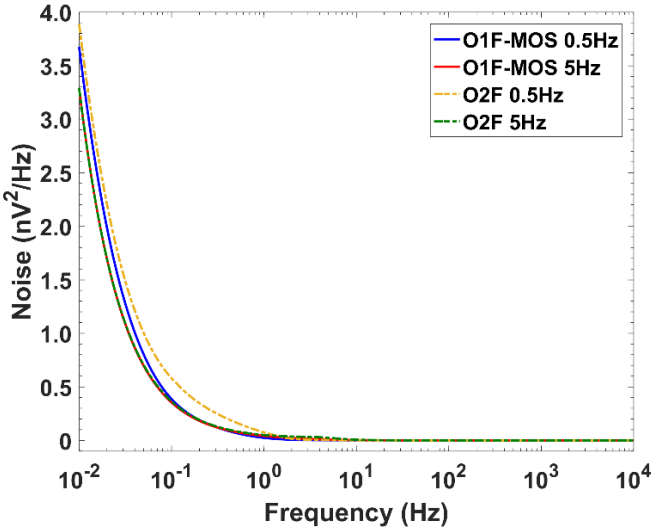


Figure 3.36. Noise over frequency for both cutoff frequencies of O1F-MOS and O2F.

The dynamic range is above 70 dB for both filters and cutoff frequencies, with the DR defined as

$$DR(dB) = 20\log_{10}\left(\frac{Linearity(V_{pp}/2)/\sqrt{2}}{noise\ (V_{rms})}\right) \tag{3.16}$$

being the linearity the input amplitude (V_{pp}/2) for a THD of -40 dB.

Comparison with other works

The proposed O1F filter presents a current consumption below 3 µA, a tuneable cutoff frequency spanning over five orders of magnitude, and an area of 0.0140 mm^2; otherwise, the O2F filter provides a better average voltage estimation but at an increase in power and area consumption. Table 3.6 shows a comparison with previously reported works covering similar tunability and frequency ranges to our proposals. Analysing the figures of merit (FoMs) in the literature [50, 30-32], we found that the main parameters involved are power, dynamic range, order of the filter (n), bandwidth (BW), and area consumption. We have included in the table two FoMs defined in [30, 31], as they not only take into account all the previous parameters, but also normalize the power (NP) and the area (NA) consumption to the technology used, according to:

$$FoM_1 = \frac{NP}{n * DR} \tag{3.17}$$

$$FoM_2 = \frac{Power * BW * NA}{n * DR} \tag{3.18}$$

with NP = Power × [0.5/($V_{dd} - V_{th}$)] × (1/V_{dd}) and NA = area(mm^2)/Tech(µm^2)^2, with V_{th} = 0.4 V for 0.18 µm CMOS technology and 0.6 V for 0.35 µm CMOS technology.

As Table 3.6 shows, both 1.8 V filters present a significant enhancement in the dynamic range, whereas the target cutoff frequencies can be maintained for a range of temperatures from -40°C to 100°C. Both FoMs show a good performance for all the frequency range compared with the other reported filters, proving it is an efficient solution in terms of power and area consumption.

Table 3.6. 1.8 V LPF performance comparison with similar G_m-C works.

Parameter	O1F	O2F	[24] '15	[51] '15	[32] '18	[31] '18	[22] '18
Results	Exp.	Exp.	Exp.	Exp.	Exp.	Exp.	Exp.
Technology (µm)	0.18	0.18	0.35	0.13	0.35	0.18	0.35
Fully-int.	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Tuneable	Yes	Yes	Yes	Yes	Yes	No	Yes
V_{supply} (V)	1.8	1.8	3.3	1.2	0.6	1	1.8
I_{Bias} (nA)	500	500	N/A*	N/A	1.5–4.5	N/A	14.9–182.3
Power (µW)	5.4	9.9	59.5–90	450	9–27(10^{-4})	0.35	0.1–1.31
Order	1	2	9	3	4	5	2
Gain offset (dB)	<0.5	<0.5	18.8/21.1@$f_{c,L}$	10	−2.77	−6/−8	0–12
Area (mm^2)	0.0140	0.0264	0.9	0.08	0.168	0.12	0.12
T range (°C)	−40 to 100	−40 to 100	N/A	N/A	N/A	N/A	N/A
$f_{c,L}$ (Hz)	0.066–2.5k	0.157–5.2k	31–8k	375k–590k	101–272	50	2k–20k
DC in/out (V)	0.39(0.45**)–1.65	0.45–1.65	N/A	N/A	N/A	N/A	N/A
Linearity (V_{pp}@THD≤1%)	0.22; 0.16[a]	0.305; 0.345[a]	0.082; 0.031[d]	0.45	N/A	N/A	0.216; 0.294
noise (µV_{rms})	13.3; 16.3[a,b]	19.2; 19.9[a,b]	93.3; 34.3[c]	342	46.6; 46.8	100	86.3; 84.3
DR (dB)	75.3; 70.9[a]	75; 75.7[a]	49.8–50.2	53.35	47	49.9	58.9; 61.8
NP (µ)	1.07	1.96	3.34–5.05	NA	NA	0.292	0.02–0.3
NA	0.432	0.815	7.347	4.734	1.371	3.704	0.980
FoM_1 (10^{-10})	1.838–3.051	1.743–1.608	12–17.34	N/A	N/A	1.868	0.114–1.219
FoM_2 (µ)	2.64*10^{-5}–1.66	1.126×10^{-4}–3.44	4.87–1.816×10^3	0.573×10^6–0.9×10^6	1.39×10^{-4}–1.12×10^{-3}	0.0415	0.11–10.4

* N/A: not available, DR: dynamic range, NP: normalization of power, FoM: figures of merit; ** minimum linear range with MOS capacitor; [a] for $f_{C,L}$=0.5 Hz&5 Hz, respectively; [b] simulated; [c] minimum noise values; [d] @THD<5 %.

3.3.3. Application as DC magnitude extractor

The previously reported circuits have been tested, operating as the last processing element in a lock-in amplifier [52], a LPF responsible for obtaining the average value of a voltage signal provided by the previous stage, a synchronous rectifier. Figure 3.37 shows an example of a signal provided by a synchronous rectifier prior to being filtered to recover its DC component, showing a 200 mV_{pp} noise-free amplitude embedded in white noise with a SNR of 20 dB. The frequency of the input test signals was set to 70 kHz, in the range of the resonance frequencies of the microcantilever-based sensors used in volatile organic compounds (VOC) detection and identification [53]. For the sake of simplicity, we considered test signals as being provided by purely resistive systems, where the DC value followed equation (3.19), being the phase shift θ = 0°. A single-phase LIA can recover the input data, whereas for signals provided by complex impedance devices (whose phase shift θ can be nonzero), a dual-phase LIA was needed to recover both amplitude and phase information, and thus two LPFs would be required to obtain the average values given in equations

$$V_x = \frac{V_{dd}}{2} - \frac{2A_s \cos(\theta)}{\pi} \tag{3.19}$$

$$V_y = \frac{V_{dd}}{2} - \frac{2A_s \sin(\theta)}{\pi} \tag{3.20}$$

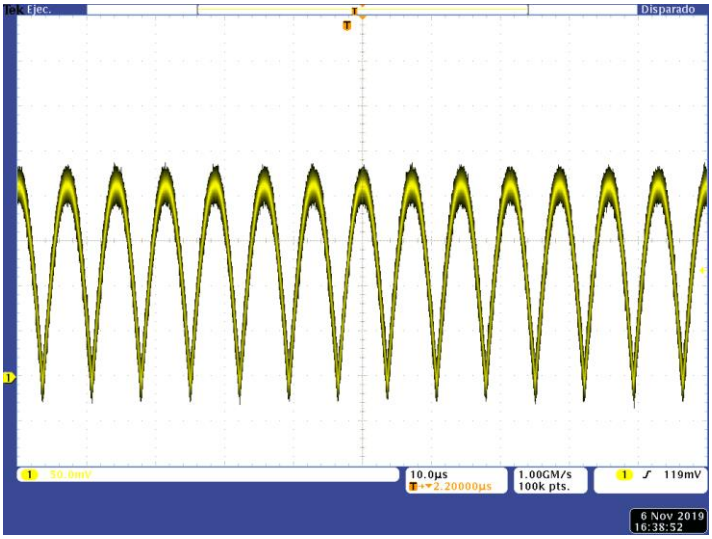


Figure 3.37. Rectified input signal for a 200 mV_{pp} amplitude with embedded white noise (SNR = 20 dB).

Figure 3.38 shows the DC voltage values recovered for input signals with amplitude values (peak-to-peak) ranging from 150 µV to 5.75 mV, and a SNR > 20 dB. The signal has been previously conditioned by a preamplifier with a gain G = 100 (40 dB). The LPF cutoff frequency has been set to $f_{c,L}$ = 5 Hz. Selecting a cutoff frequency 10 times lower ($f_{c,L}$ = 0.5 Hz), the recovered amplitude would present a higher accuracy but at a much longer output stabilization time. Similarly, a higher $f_{c,L}$ would provide a faster response but at a lower accuracy.

The recovered signals show the validity of the proposed LPFs as DC magnitude extractors in a multichannel measurement device. Higher accuracy over the recovered signal is achieved with the second order filter, although a higher consumption in power and area is required. Thus, there is an accuracy power–area trade-off that is dependent on the filters order.

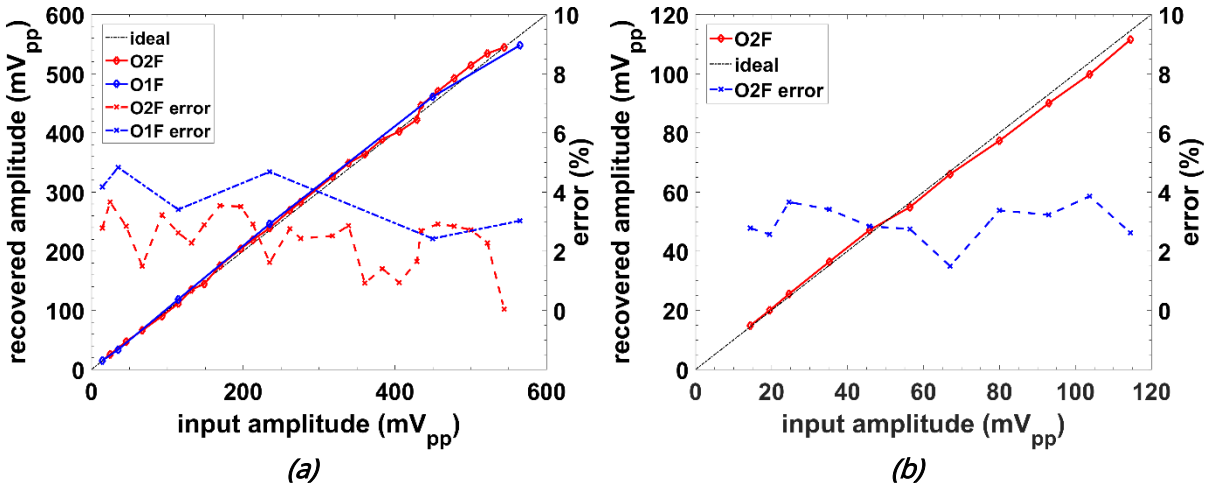


Figure 3.38. Lock-in amplifier (LIA) experimental recovered amplitude versus input signal, with $f_{c,L}$ = 5 Hz: a) amplitude values up to 560 mV_{pp} with G = 100 (40 dB); and b) zoomed area for the first 120 mV_{pp}.

3.3.4. Conclusions

A novel approach to design very low cut-off LPFs has been introduced and validated, based on a G_m-current steering technique. The first order LPF presents a five orders of magnitude $f_{C,L}$ range, with a low power consumption and a high dynamic range. Similar results are achieved with the second order structure, increasing the cutoff frequency range and slightly enhancing the dynamic range at the expense of an increase of the area and power consumption.

Compared to state-of-the-art solutions, the proposed structures exhibit very competitive performances while meeting the critical requirements of battery-portable on-chip micro-instruments in terms of power and area efficiency, critical for its implementation in multichannel measurement instruments for impedance sensor arrays, becoming a preferable choice for general-purpose reconfigurable front-end sensor interfaces.

3.4. REFERENCES

1. Garde, M.P., Lopez-Martin, A.J., Carvajal, R.G. and Ramírez-Angulo, J. Super class AB RFC OTA using non-linear current mirrors. *Electronics Letters*, 2018.
2. Garde, M.P., Lopez-Martin, A.J., Carvajal, R.G. and Ramírez-Angulo, J. Super Class-AB Recycling Folded Cascode OTA. *IEEE Journal of Solid-State Circuits*, 2018.
3. Lopez-Martin, A.J., Garde, M.P., Algueta-Miguel, J.M., Beloso-Legarra, J., Carvajal, R.G. and Ramírez-Angulo, J. Energy-Efficient Amplifiers Based on Quasi-Floating Gate Techniques. *Applied Sciences*, 2021.
4. Carrillo, J.M., Domínguez, M.A., Pérez-Aloe, R., Duque-Carrillo, J.F. and de la Cruz, C.A. CMOS Low-Voltage Indirect Current Feedback Instrumentation Amplifiers With Improved Performance. *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Genoa, Italy, 2019.
5. Yazicioglu, R.F., Merken, P., Puers, R. and Van Hoof, C. A 60μW 60nV/radicHz readout front-end for portable biopotential acquisition systems. *IEEE International Solid State Circuits Conference*, San Francisco, USA, 2006.
6. Rao, A., Teng, Y.-C., Schaef, C., Murphy, E.K., Arshad, S., Halter, R.J. and Odame, K. An Analog Front End ASIC for Cardiac Electrical Impedance Tomography. *IEEE Transactions on Biomedical Circuits and Systems*, 2018.
7. Kim, J. and Ko, H. Reconfigurable Voltage/Current Readout Instrumentation Amplifier for Cardiovascular Health Monitoring. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018.
8. Kim, J. Simultaneous Voltage and Current Measurement Instrumentation Amplifier for ECG and PPG Monitoring. *Electronics*, 2021.
9. Xu, J., Harpe, P., Pettine, J., Van Hoof, C. and Yazicioglu, R.F. A low power configurable bio-impedance spectroscopy (BIS) ASIC with simultaneous ECG and respiration recording functionality. *European Solid-State Circuits Conference (ESSCIRC)*, Graz, Austria, 2015.
10. Gupta, S., Mehra, R. and Sharma, S. Design and Analysis of Flipped Voltage Follower for Different Aspect Ratio. *International Journal of Computer Applications,* 2016.
11. Mondal, S. and Hall, D. A. An ECG chopper amplifier achieving 0.92 NEF and 0.85 PEF with AC-coupled inverter-stacking for noise efficiency enhancement. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, USA, 2017.
12. Márquez, A., Medrano, N. and Calvo, B. Low-Noise Wide-Frequency Tunable Amplifier for Bioimpedance Spectroscopy Applications. *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Genoa, Italy, 2019.
13. Manickam, A., Chevalier, A., McDermott, M., Ellington, A.D. and Hassibi, A. A CMOS Electrochemical Impedance Spectroscopy (EIS) Biosensor Array. *IEEE Transactions on Biomedical Circuits and Systems*, 2010.
14. Márquez, A., Medrano, N., Calvo, B. and Pérez-Bailón, J. A Dual Synchronous Demodulator for Phase Sensitive Detection Applications. *IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, Dubrovnik, Croatia, 2020.
15. Cinco-Izquierdo, O.J., Sanz-Pascual, M.T. de la Cruz-Blas, C.A. and Calvo-López, B. Low Power CMOS Chopper Preamplifier Based on Source-Degeneration Transconductors. *IEEE Latin American Symposium on Circuits & Systems (LASCAS)*, San Jose, Costa Rica, 2020.
16. Maya-Hernández, P.M., Sanz-Pascual, M.T. and Calvo, B. CMOS Low-Power Lock-In Amplifiers With Signal Rectification in Current Domain. *IEEE Transactions on Instrumentation and Measurement*, 2015.

17. Wong, A., Pun, K.P., Zhang, Y.T. and Hung, K. A Near-Infrared Heart Rate Measurement IC with Very Low Cutoff Frequency Using Current Steering Technique. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2005.
18. Rieger, R., Demosthenous, A. and Taylor, J. A 230-nW 10-s Time Constant CMOS Integrator for an Adaptive Nerve Signal Amplifier. *IEEE Journal of Solid-State Circuits,* 2004.
19. Yufera, A., Rueda, A., Muñoz, J.M., Doldan, R., Leger, G. and Rodriguez-Villegas, E.O. A Tissue Impedance Measurement Chip for Myocardial Ischemia Detection. *IEEE Transactions on Circuits and Systems I: Regular Papers,* 2005.
20. Li, Y., Poon, C.C.Y. and Zhang, Y.T. Analog Integrated Circuits Design for Processing Physiological Signals. *IEEE Reviews in Biomedical Engineering,* 2010.
21. Gosselin, B., Sawan, M. and Kerherve, E. Linear-Phase Delay Filters for Ultra-Low-Power Signal Processing in Neural Recording Implants. *IEEE Transactions on Biomedical Circuits and Systems,* 2010.
22. Peng, S.-Y., Lee, Y.-H., Wang, T.-Y., Huang, H.-C., Lai, M.-R., Lee, C.-H. and Liu, L.-H. A Power-Efficient Reconfigurable OTA-C Filter for Low-Frequency Biomedical Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers,* 2018.
23. Lu, J., Yang, T., Jahan, M.S. and Holleman, J. A low-power 84-dB dynamic-range tunable Gm-C filter for bio-signal acquisition. *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS*), College Station, USA, 2014.
24. Wang, S., Koickal, T.J., Hamilton, A., Cheung, R. and Smith, L.S. A Bio-Realistic Analog CMOS Cochlea Filter with High Tunability and Ultra-Steep Roll-Off. *IEEE Transactions on Biomedical Circuits and Systems,* 2015.
25. Rodriguez, S., Ollmar, S., Waqar, M. and Rusu, A. A Batteryless Sensor ASIC for Implantable Bio-Impedance Applications. *IEEE Transactions on Biomedical Circuits and Systems,* 2016.
26. Bruschi, P., Nizza, N., Pieri, F., Schipani, M. and Cardisciani, D. A Fully Integrated Single-Ended 1.5–15-Hz Low-Pass Filter with Linear Tuning Law. *IEEE Journal of Solid-State Circuits,* 2007.
27. Arnaud, A., Fiorelli, R. and Galup-Montoro, C. Nanowatt, Sub-nS OTAs, with Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors. *IEEE Journal of Solid-State Circuits,* 2006.
28. Veeravalli, A., Sanchez-Sinencio, E. and Silva-Martinez, J. Transconductance amplifier structures with very small transconductances: A comparative design approach. *IEEE Journal of Solid-State Circuits,* 2002.
29. Solis-Bustos, S., Silva-Martinez, J., Maloberti, F. and Sanchez-Sinencio, E. A 60-dB dynamic-range CMOS sixth-order 2.4-Hz low-pass filter for medical applications. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2000.
30. Lee, S., Wang, C. and Chu, Y. Low-Voltage OTA–C Filter with an Area- and Power-Efficient OTA for Biosignal Sensor Applications. *IEEE Transactions on Biomedical Circuits and Systems,* 2019.
31. Sun, C. and Lee, S. A Fifth-Order Butterworth OTA-C LPF with Multiple-Output Differential-Input OTA for ECG Applications. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2018.
32. Sawigun, C. and Thanapitak, S. A 0.9-nW, 101-Hz, and 46.3-μVrms IRN Low-Pass Filter for ECG Acquisition Using FVF Biquads. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* 2018.
33. Germanovix, W., Bonizzoni, E. and Maloberti, F. Capacitance Super Multiplier for Sub-Hertz Low-Pass Integrated Filters. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2018.
34. Rodriguez-Villegas, E., Casson, A.J. and Corbishley, P. A sub-Hertz nanopower low pass filter. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2011.

35. Sawigun, C. and Serdijn, W.A. A Modular Transconductance Reduction Technique for Very Low-Frequency Gm-C Filters. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, Korea, 2012.
36. Silva-Martinez, J. and Salcedo-Suñer, J. IC Voltage to Current Transducers with Very Small Transconductance. *Analog Integrated Circuits and Signal Processing,* 1997.
37. El Mourabit, A., Lu, G.-N. and Pittet, P. A low-frequency, sub 1.5-V micropower G/sub m/-C filter based on subthreshold MIFG MOS transistors. *European Solid-State Circuits Conference (ESSCIRC),* Grenoble, France, 2005.
38. Sawigun, C. and Serdijn, W.A. A modular transconductance reduction technique for very low-frequency Gm-C filters. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, Korea, 2012.
39. Barros de la Cruz, I. Transconductores de baja Gm para filtros de baja frecuencia. *Master thesis*, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), 2021.
40. Pérez-Bailón, J., Calvo, B. and Medrano, N. A CMOS Low Pass Filter for SoC Lock-in-Based Measurement Devices. *Sensors,* 2019.
41. Geiger, R.L. and Sanchez-Sinencio, E. Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial. *IEEE Circuits and Devices Magazine,* 1985.
42. Ramírez-Angulo, J., Sudha Gariemlla, S.R. and Lopez-Martin, A. New Gain Programmable Current Mirrors Based on Current Steering. *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, San Juan, Puerto Rico, 2006.
43. Pérez-Bailón, J., Calvo, B. and Medrano, N. 1.0 V-0.18 µm CMOS Tunable Low Pass Filters with 73 dB DR for On-Chip Sensing Acquisition Systems. *Electronics,* 2021.
44. Maxim Integrated, MAX5413/14/15, 2001. Last accesed: 25th December 2021. https://datasheets.maximintegrated.com/en/ds/MAX5413-MAX5415.pdf
45. Maxim Integrated, MAX5520, 2004. Last accesed: 25th December 2021. https://datasheets.maximintegrated.com/en/ds/MAX5520-MAX5521.pdf
46. Maxim Integrated, MAX5530, 2004. Last accesed: 25th December 2021. https://datasheets.maximintegrated.com/en/ds/MAX5530-MAX5531.pdf
47. Sharuddin, I., Lee, L. and Yusof, Z. Analysis design of area efficient segmentation digital to analog converter for ultra-low power successive approximation analog to digital converter. *Microelectronics Journal*, 2016.
48. Gosselin, B., Simard, V. and Sawan, M. Low power programmable front-end for a multichannel neural recording interface. *Canadian Conference on Electrical and Computer Engineering. Toward a Caring and Humane Technology (CCECE)*, Montreal, Canada, 2003.
49. Pérez-Bailón, J., Márquez, A., Calvo, B. and Medrano, N. A 0.18 µm CMOS LDO Regulator for an on-Chip Sensor Array Impedance Measurement System. *Sensors*, 2018.
50. Zhang, T., Pui-In, M., Mang-I, V., Peng-Un, M., Man-Kay, L., Sio-Hang, P., Fen, W. and Martins, R.P. 15-nW Biopotential LPFs in 0.35-µm CMOS Using Subthreshold-Source-Follower Biquads With and Without Gain Compensation. *IEEE Transactions on Biomedical Circuits and Systems,* 2013.
51. Sánchez-Rodríguez, T., Gomez-Galan, J.A., Carvajal, R.G., Sánchez-Raya, M., Muñoz, F. and Ramírez-Angulo, J. A 1.2-V 450-µW Gm-C Bluetooth Channel Filter Using a Novel Gain-Boosted Tunable Transconductor. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* 2015.
52. Maya-Hernández, P.M., Sanz-Pascual, M.T. and Calvo, B. Ultralow-Power Synchronous Demodulation for Low-Level Sensor Signal Detection. *IEEE Transactions on Instrumentation and Measurement,* 2018.

53. Urbiztondo, M.A., Peralta, A., Pellejero, I., Sese, J., Pina, M.P., Dufour, I. and Santamaria, J. Detection of organic vapours with Si cantilevers coated with inorganic (zeolites) for organic (polymer) layers. *Sensors and Actuators B: Chemical*, 2012.

Chapter 4
FRA-IS Front End

This chapter presents complete FRA-IS read-out schemes based on the blocks introduced and analysed in the previous chapter, satisfying the constraints required to be part of a truly portable battery-operated low-power processing system for impedance spectroscopy measurement, based on CMOS microelectronic technologies.

All designs have been implemented in the 0.18 μm CMOS technology from UMC. The first structure, a wideband front-end, consists of a LNA suitable for voltage and current input signals with a 20 dB (87 dBΩ) gain and an embedded mixer VGA with a 0-20 dB progammable gain, a bandwidth higher than 100 MHz and a low pass filter with a tuneable cutoff frequency ranging from mHz to kHz. It is powered by a 1.8 V power supply rendenring a total power consumption of 461.5 μW and an active area of 0.0769 mm^2.

The second configuration is a wideband compact front-end structure with a 0-40 dB programmable gain, an 87 MHz bandwidth and a low pass filter with a tuneable cutoff frequency ranging from mHz to kHz. The amplifying stage is reduced to only one programmable gain stage with embedded mixer reducing the area and power consumption down to 0.0569 mm^2 and 291.6 μW (with V_{dd} = 1.8 V) respectively, at the expense of reducing the total bandwidth and limiting the input signals to voltage signals.

Both architectures, besides being electrically characterized, are validated by simultaneously recoverying the DC magnitudes, V_x and V_y, used to recover the phase shift and magnitude -or the real and imaginary components- of an impedance Z implemented by one of the simplest Randles cell made of a capacitor and a resistor in parallel as shown in Figure 4.1. This model let us see both the full magnitude $|Z|$ and phase θ variation over the frequency as it shifts from a purely resistive impedance to a purely capacitive impedance. The impedance values selected are 500 nF and 100 Ω to fit the magnitude and phase shift over the frequency range of the proposed topologies. At the end of the chapter, a comparison with other architectures is done and conclusions are drawn.

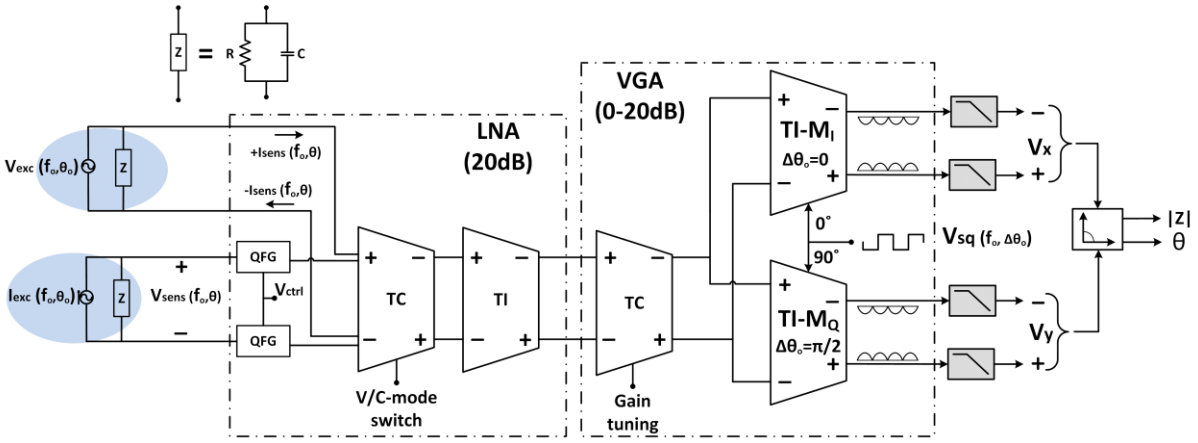


Figure 4.1. Block diagram of the proposed Dual Phase Front-End structure.

4.1. WIDEBAND FRONT-END

First, the proposed wideband FRA-IS read-out architecture recovering simultaneously both I (X) and Q (Y) responses, while meeting the required LVLP constraints demanded by portable applications is described. Then, its main performance results are summarized.

The proposed structure, shown in Figure 4.1, consists of a fully differential topology optimized to minimize noise and enhance CMRR, with an input LNA with both voltage and current input modes (as the one reported in Section 3.1.1), followed by a VGA with embedded self-multiplication as the one reported in Section 3.2 but with dual-phase output; and an output filtering stage based on the one reported in Section 3.3.2.

The result is a high performance fully reconfigurable architecture, which offers a 20-40 dB (87-107 dBΩ) gain, with a 100 MHz bandwidth and recovery errors below 1.4º (4.8º, C-mode) and 7.3% (5%, C-mode) for the amplitude and phase respectively.

4.1.1. System architecture

The detailed schematic is shown in Figure 4.2. For the input stage, to achieve a 40 dB gain, two 20 dB gain TC-TI structures are cascaded: 1) LNA with fixed 20 dB gain, V/I-input modes, tuneable input QFG to filter the outband flicker noise; and 2) VGA with programmable 0-20 dB gain, V-mode input only, embedded mixer and dual output. Note that for the VGA, the two branches I and Q share the TC stage, while two TI with embedded mixer stages are required. Thus, the dual-phase output just requires duplicating the VGA TI structure plus output LPFs, in terms of additional total area and power consumption.

At the LNA (Figure 4.2a) a switch is used to change between input modes and disconnect R_{TC} in current mode; a tuneable QFG is also used to control the $f_{c,H} = 1/2\pi R_{QFG}C_{in}$ through V_{ctrl}, in a range from 6.9 Hz to 170 kHz, setting $V_{cm,in}$ = 0.9 V.

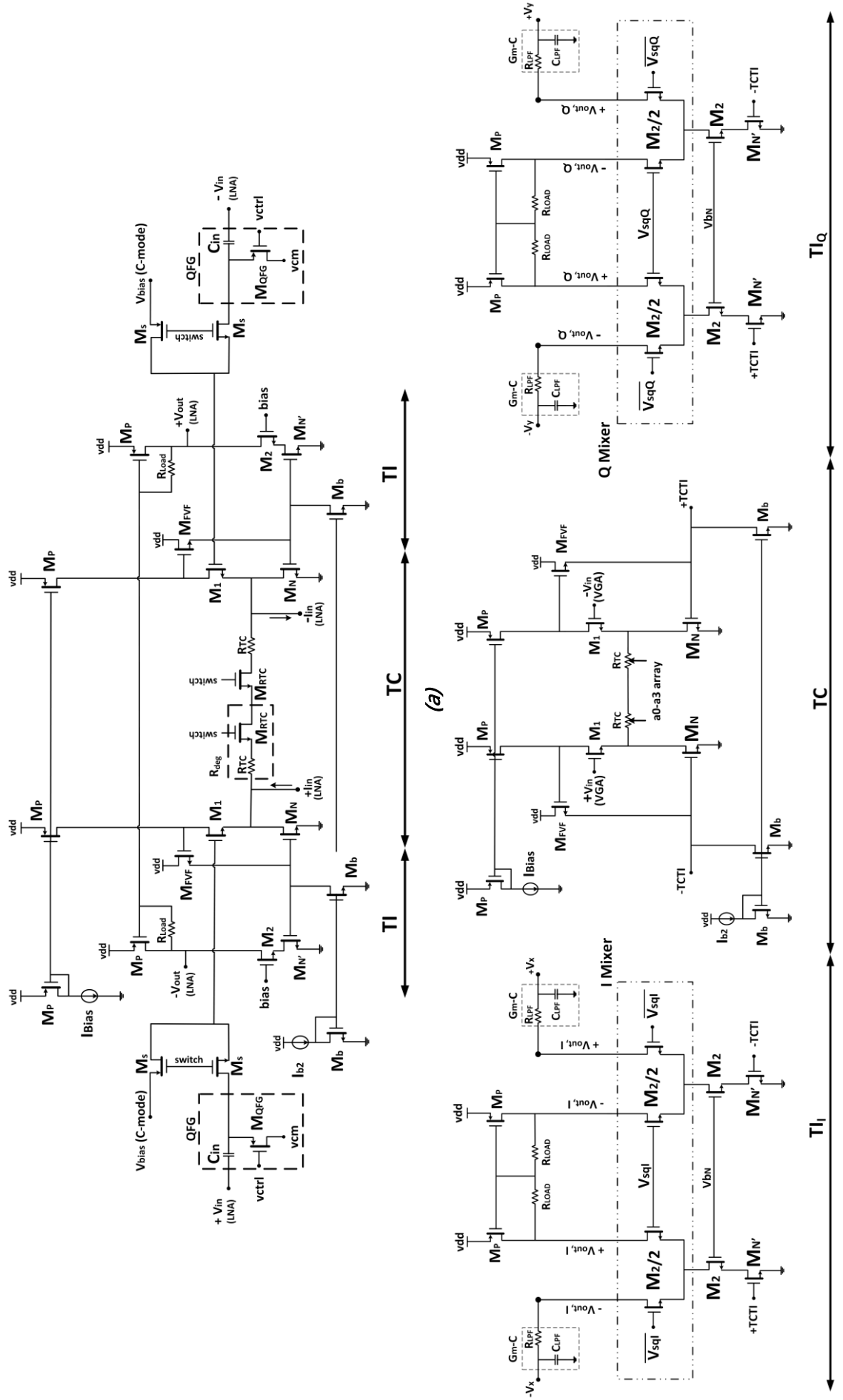


Figure 4.2. Schematic view of the proposed Dual Phase Front-End structure: a) LNA and b) VGA with embedded mixer.

The VGA Figure 4.2b) does not need the QFG stage nor does it requires switches to change between input modes, simplifying the structure.

To achieve dual-phase outputs, the TI structure of the VGA is replicated having TI_I and TI_Q, with reference signals V_{sqI} and V_{sqQ} (and their complementary signals, $\overline{V_{sqI}}$ and $\overline{V_{sqQ}}$) in quadrature between them. Gain tuning is given with a 4-bit array of resistances used for R_{TC}, implemented with symmetrical POLY-resistances and MOS-switches to activate them independently. Overall, it achieves a 20 dB to 40 dB gain (or 87 dBΩ to 107 dBΩ in current mode) with a 100 MHz bandwidth.

The embedded-multiplication, based on [1], operates, taking the TI-M_I stage, as follows: in each $M_{N'}$-M_2 TI output current branch, two $M_2/2$ split matched transistors are introduced, with their gates driven by complementary control signals (V_{sqI} and its inverse, $\overline{V_{sqI}}$, f_0, in phase with the input exciting signal, $\Delta\theta_o$=0) and connected to M_P, R_{LOAD} and the outputs $V_{out,I}^{\pm}$. In this way, $M_2/2$ act as embedded mixers, providing an output $V_{out,I} = (V_{out,I}^{+} - V_{out,I}^{-})$ according to V_{sqI} and $\overline{V_{sqI}}$ variations and the in-phase I output signal is obtained. By replicating this TI structure, with the quadrature control signals V_{sqQ} and $\overline{V_{sqQ}}$ the dual-phase architecture with both I and Q outputs is achieved.

The output signals are then filtered with a cutoff frequency tuneable Low Pass Filter obtaining the DC values V_x and V_y from which we recover the phase shift and magnitude -or the real and imaginary components- of the target impedance Z.

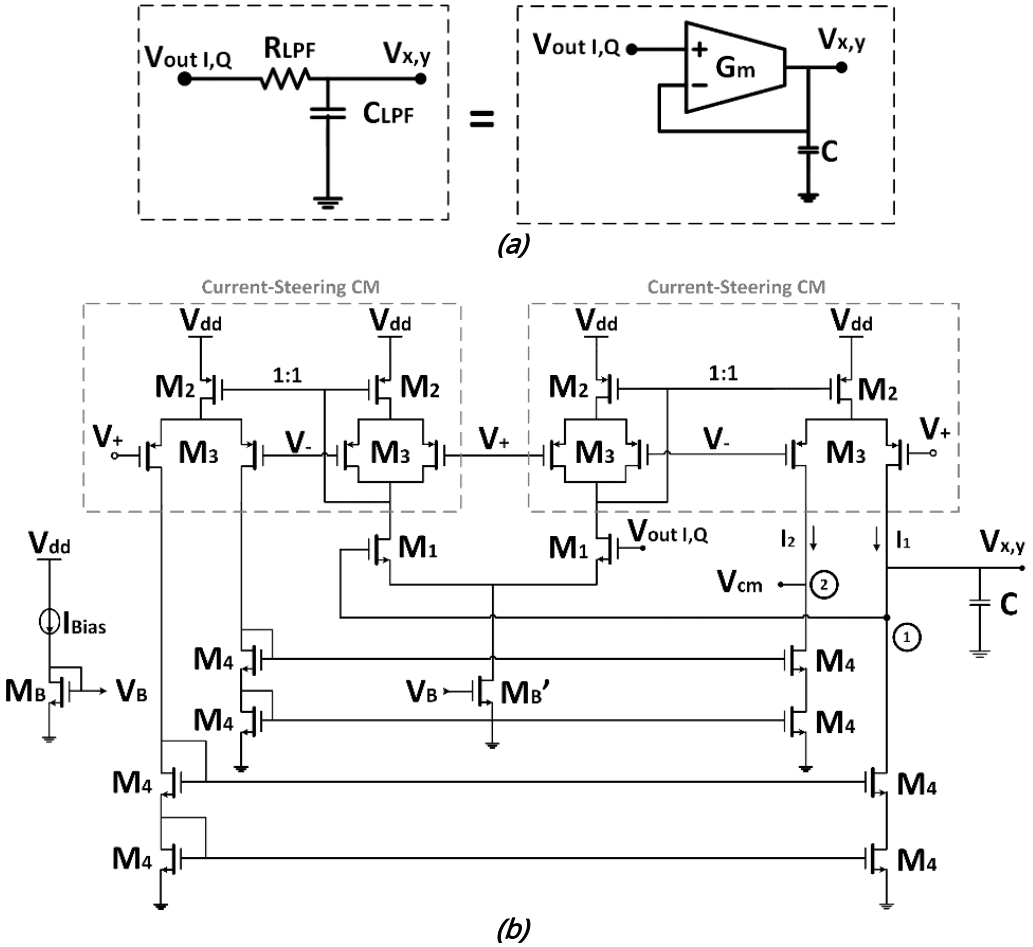
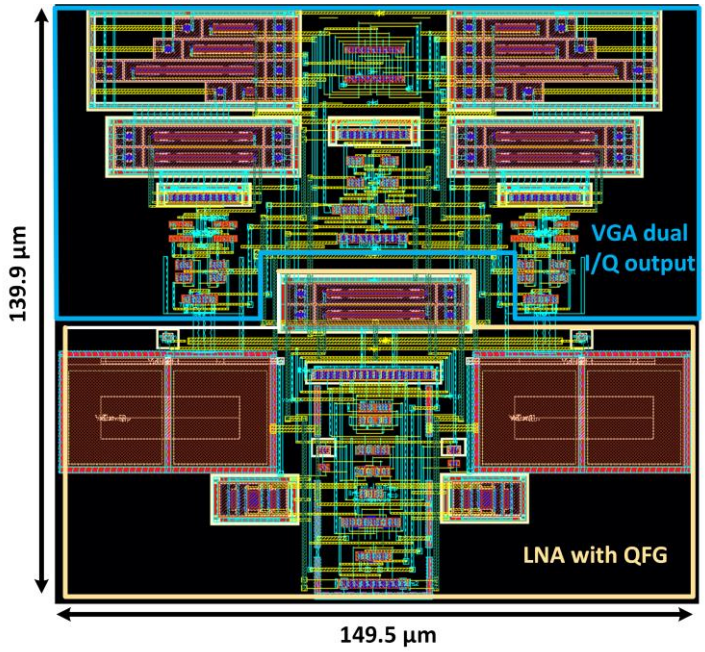
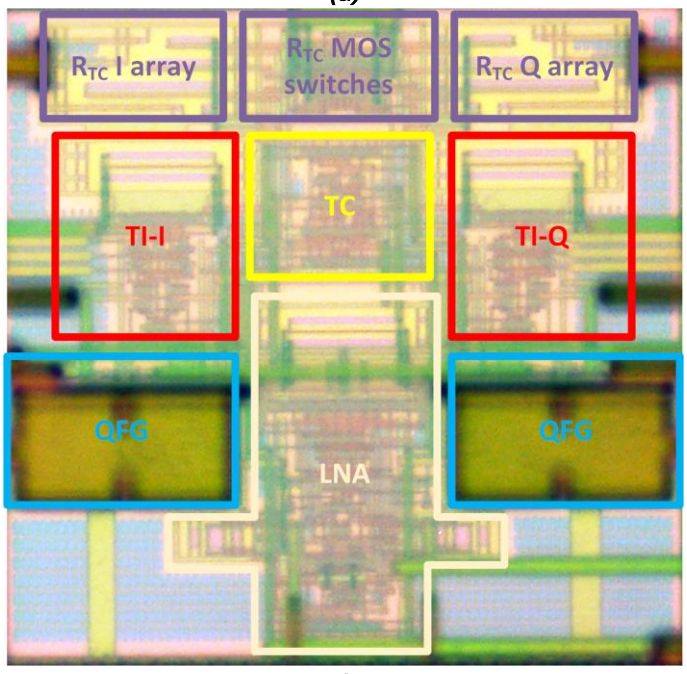


Figure 4.3. G_m-C structure to filter the output signal: a) Basic diagram; and b) Schematic view [2].

The output G_m-C integrator, shown in Figure 4.3, is the O1F-LPF previously characterized in Section 3.3.1. It is a differential-input single-output architecture in unity gain closed-loop feedback configuration. The integrating C is 50 pF; the G_m is based on a classic mirrored OTA that keeps constant the V–I conversion gain (M_1, g_{m1}), while both G_m reduction and tuning are done in the output current transfer section, exploiting a M_2-M_3 cascode current mirror steering technique as the most suitable choice to effectively reduce the G_m, while preserving a good power-area-dynamic range trade-off. It presents a tuneable cutoff frequency $f_{c,L}$ ranging from 66 mHz up to 2.5 kHz, with a power consumption of 5.4 µW, an area of 0.014 mm^2 and a DR > 70 dB.



(a)



(b)

Figure 4.4. Proposed FRA-IS structure (w/o the LPF): Dual Phase Front-End a) Layout view and b) microphotograph.

The proposed Dual-Phase Front-end has been designed in the 0.18 µm CMOS technology from UMC. With a power supply of 1.8 V, a bias current I_{Bias} *(LNA/VGA)* = 25 µA, I_{b2} *(LNA/VGA)* = 150 nA, and I_{Bias} *(LPF)* = 0.5 µA, it presents a total power consumption of 461.5 µW and an active area of 0.0769 mm^2. The microphotograph of the Front-End without the LPF is shown in Figure 4.4.

4.1.2. Performances

This section presents the main post-layout results for the Wideband Front-End electrical characterization. Finally, the proposal is validated by characterizing an impedance *Z*.

Gain and Bandwidth

Figure 4.5 shows the frequency response of the amplifier in voltage input mode (Figure **4.5**a) and current input mode (Figure 4.5b). In V-mode, it shows a tuneable gain ranging from ~20 dB to ~40 dB for the differential output with a bandwidth higher than 100 MHz. For C-mode, the gain reaches values from ~87 dBΩ to ~107 dBΩ and a bandwidth higher than 130 MHz.

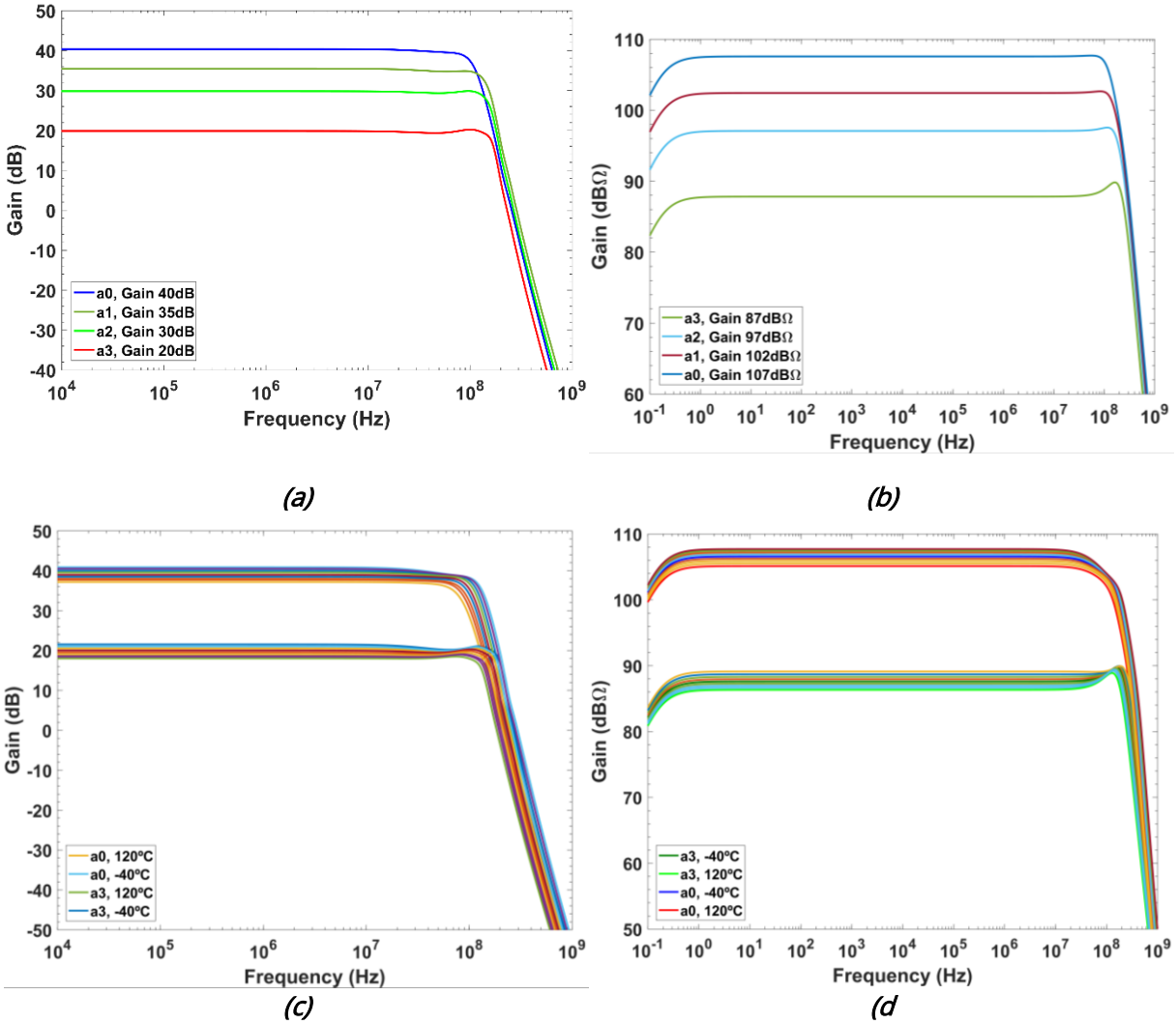


Figure 4.5. Frequency response at room temperature: a) V-mode and b) C-mode; and for different temperatures at maximum and minimum gain for c) V-mode and d) C-mode.

The influence of the temperature (from -40ºC to 120ºC) is shown in Figure 4.5c and Figure 4.5d. They present, in V-mode, a deviation of 0.0231 dB/ºC for maximum gain and 0.022 dB/ºC for minimum gain. In addition, in C-mode, the deviation is of 0.0156 dB/ºC for maximum gain and 0.0151 dB/ºC for minimum gain.

Figure 4.6, showns the high pass cutoff frequency, $f_{c,H}$ variation at maximum gain for a va riation of V_{ctrl} from 0.4 V to 1.0 V in 0.1 V steps, ranging from 6.9 Hz (1.0 V) to 170 kHz (0.4 V).

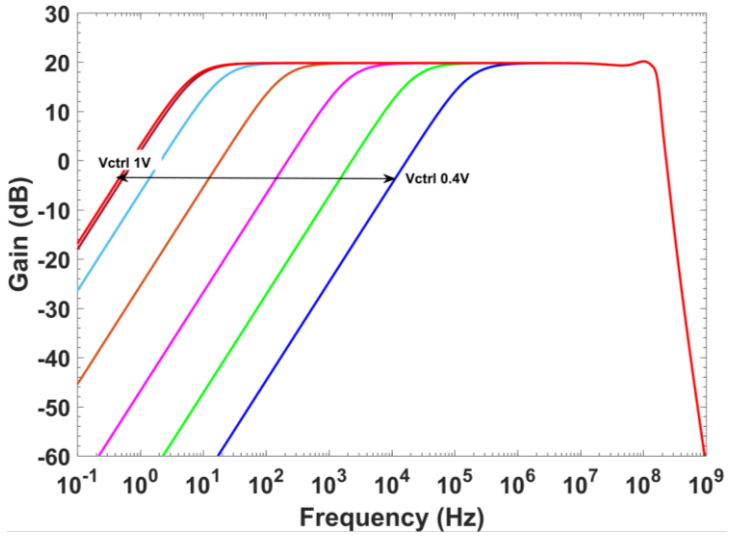


Figure 4.6. High pass frequency tuning for all V_{ctrl} range, with minimum gain.

Transient behaviour

The transient analysis is done for the input sensor signal in phase with the branch I while output Q has a π/2 phase shift, to better visualize its operation. Figure 4.7 shows the corresponding transient behaviour for both input modes with maximum and minimum gains and the output signals obtained for I and Q at f_0 = 2 MHz.

The figures above presented, show the expected synchronous rectification in I. It can be seen how for minimum gain in both V/C-modes appear spikes at the transition points. This is produced by the step of the square signal used as reference signal when it changes from gnd to V_{dd} or viceversa. Nevertheless, these spikes do not affect the value measured after filtering.

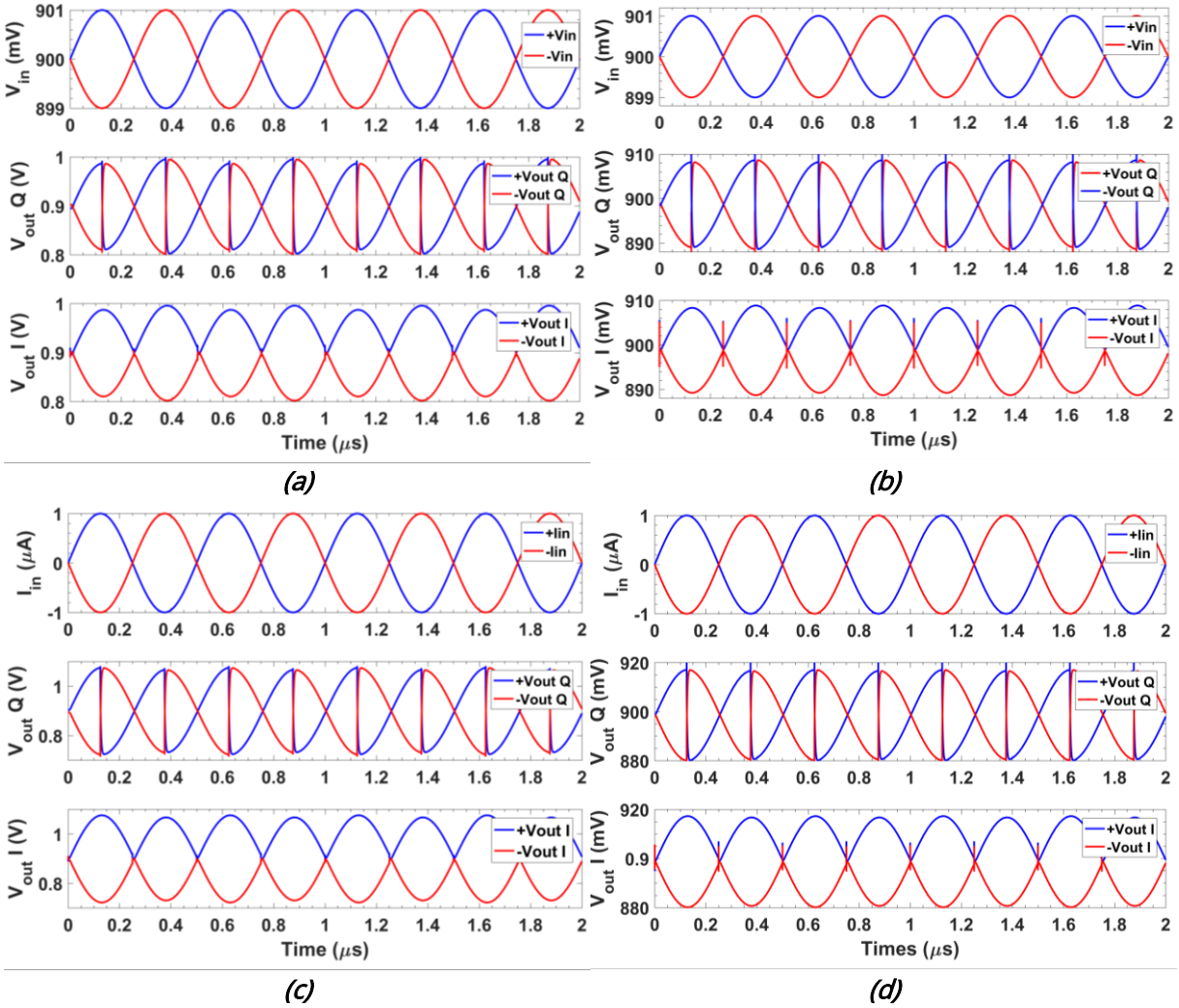


Figure 4.7. Transient behaviour at f_0 = 2 MHz with signal in-phase with I at; V-mode for a) maximum and b) minimum gain; and C-mode for c) maximum and d) minimum gain.

Noise

The rms integrated noise over the frequency range is reported Table 4.1, with V_{ctrl} = 1.0 V for V-mode (worst case).

Table 4.1. RMS Integrated noise of the wideband FE.

Input mode	V-mode	V-mode	C-mode	C-mode
Gain	19.85 dB	39.36 dB	87.0 dBΩ	106.5 dBΩ
BW (Hz)	6.9-100M	6.9-100M	0.16-100M	0.16-100M
out (mVrms)	2.487	19.55	1.526	9.853
In (rms)	253 μV	210.4 μV	68.2 nA	46.6 nA
In (V/√Hz or A/√Hz)	25.3 nV	21.0 nV	6.8 pA	4.7 pA

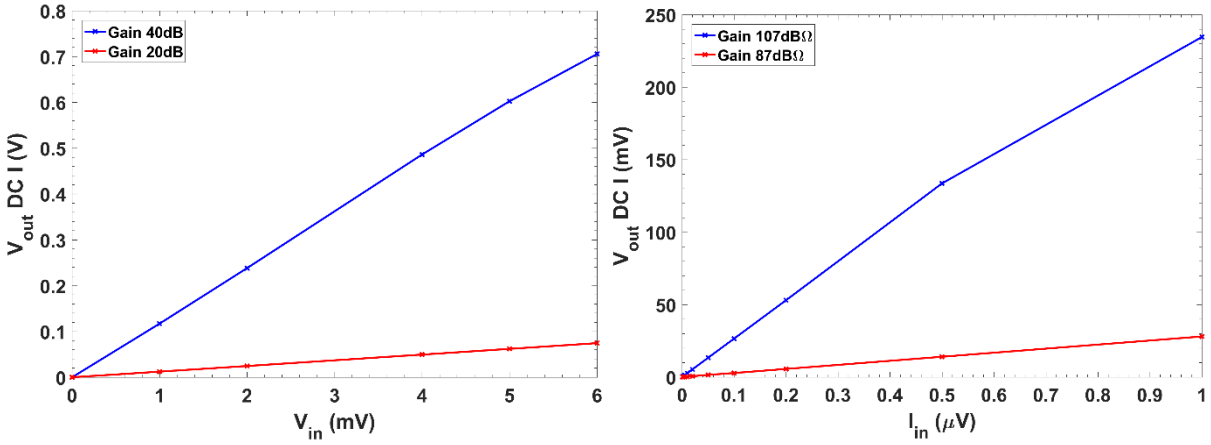
Recovery performance

The electrical characterization for both V-mode and C-mode is shown next. It is presented for each input mode the measured DC output voltage for branch I, V_x; the recovered input amplitude and its associated error for different amplitude configurations; and the recovered phase with its errors for a fixed input amplitude and different phases (Figure 4.9).

The input signal operates at f_0 = 10 kHz and the LPF cutoff frequency is set to $f_{c,L}$ = 10 Hz to reduce the acquisition times. Note that the filtering stage with a $f_{c,L}$ = 10 Hz requires stabilization times in the order of 100 ms, but the transient simulation requires to simulate the input signal at f_0, therefore at MHz operation the computational cost is too high and thus, the simulated operating frequency is limited to 10 kHz.

Figure 4.8 shows the recovered DC output I (V_x) performance for maximum and minimum gain configurations for V-mode input (Figure 4.8a) and C-mode input (Figure 4.8b), with an AC input signal ranging from 0.1 µV to 6 mV (V-mode) and from 1 nA to 1 µA (C-mode).

Figure 4.9 shows the recovered input signal amplitude and the recovered phase with their respective errors for both V-mode and C-mode. The recovered input amplitude is given for an AC input signal ranging from 0.1 µV to 6 mV for gains at 20 dB and 40 dB for V-mode (Figure 4.9a), and from 1 nA to 1 µA with gains at 87 dB and 107 dB for C-mode (Figure 4.9b). The recovered phase is given for a fixed input amplitude of 1 mV (V-mode, Figure 4.9c) and 1 µA (C-mode, Figure 4.9d) by varying the input phase from 0º to 90º in 5° steps.



(a) *(b)*

Figure 4.8. Recovered DC output I (V_x) performance for: a) V-mode with an input signal amplitude from 100 nV to 6 mV; b) C-mode with an input signal amplitude from 1 nA to 1 µA.

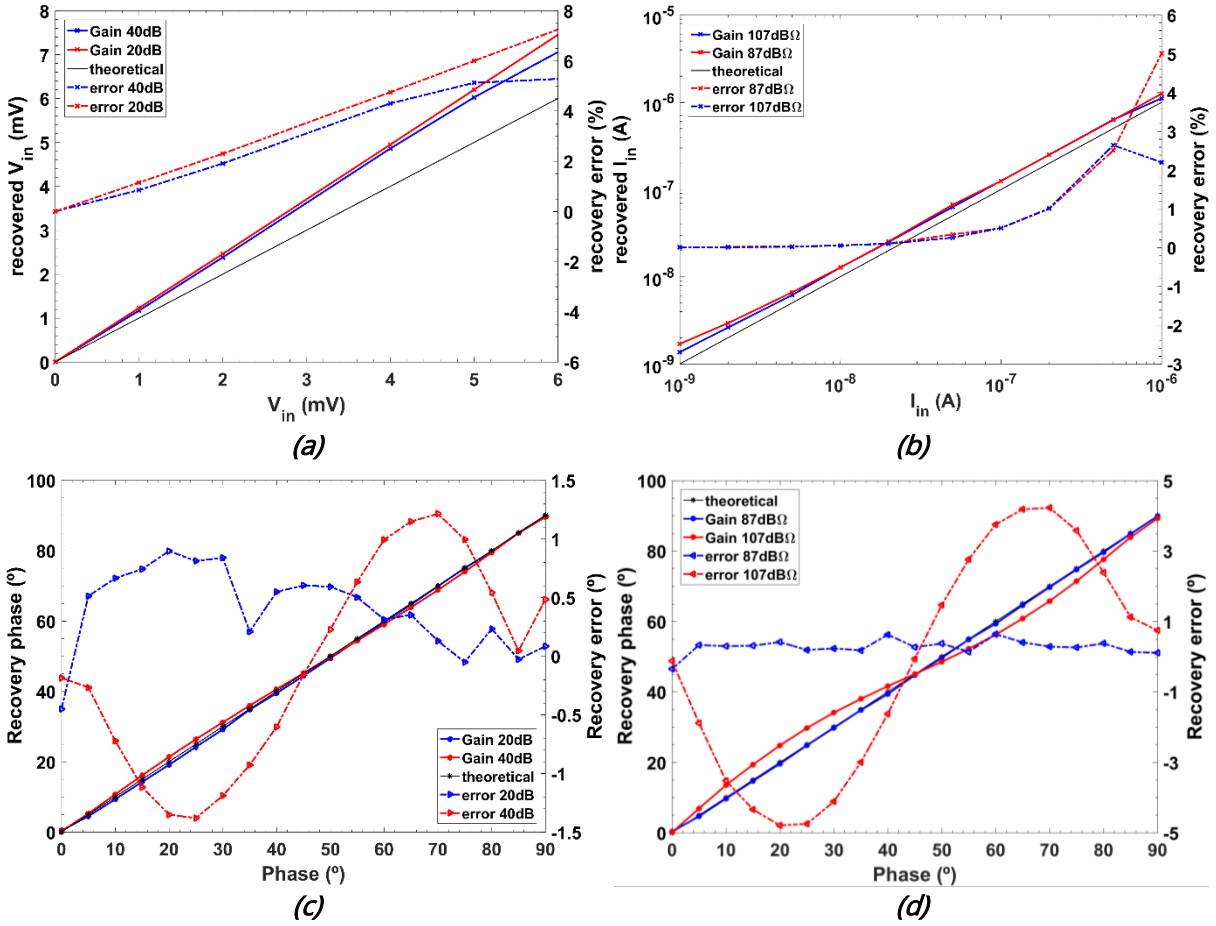


Figure 4.9. Recovered input signal amplitude and its error (%) for a) V-mode and b) C-mode; and recovered phase and its error (°) for c) V-mode and d) C-mode.

Impedance characterization

To validate this proposal, a Z impedance composed of a resistor R = 100 Ω in parallel with a capacitor C = 500 nF as shown in Figure 4.1 is used. In V-mode, it is excited with an AC current generating the input voltage, V_{in}, driven through the QFG to the input pair of the TC-stage. In C-mode, the opposite conversion is done: it is excited with an AC voltage, generating the input current, I_{in}.

The resulting DC output voltages, V_x and V_y, are used to recover the phase shift and magnitude -or the real and imaginary components- of the impedance Z according to

$$|Z| = \frac{\pi}{2}\frac{1}{G}\sqrt{V_x^2 + V_y^2} \tag{4.1}$$

$$\theta = \operatorname{atan}\left(V_y / V_x\right) \tag{4.2}$$

where G represents the gain of the amplifier stage.

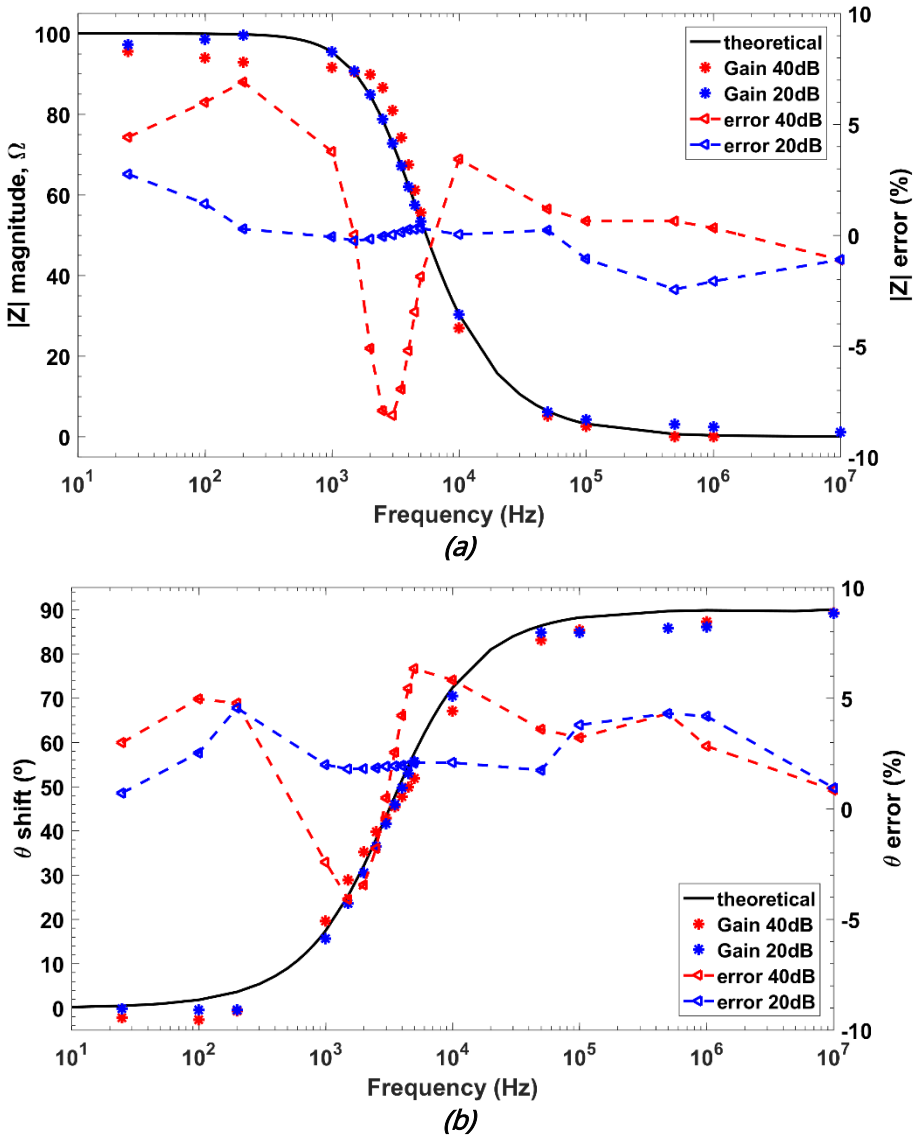


Figure 4.10. Recovered Z magnitude and phase in V-mode for 20 dB and 40 dB gain and their normalized errors (w/o calibration): a) magnitude: recovered vs theoretical; and b) phase: recovered vs theoretical.

In V-mode, Figure 4.10 shows the recovered magnitude and phase for an AC input current of 100 μA_{pp} at 18 different frequencies over the 25 Hz-10 MHz range, operating at 20 dB and 40 dB and a $f_{c,H}$ = 6.9 Hz (V_{ctrl} = 1.0 V), which renders the worst case recovery errors. Figure 4.10a shows the recovered magnitude compared to the theoretical value and Figure 4.10b shows the recovered phase compared to its theoretical value. With 40 dB gain, the full-scale magnitude and phase recovery errors are below 8 % and 6.4 % for all the frequency range. While with 20 dB gain configuration, the magnitude and phase recovery errors are below 3 % and 4.6 % respectively.

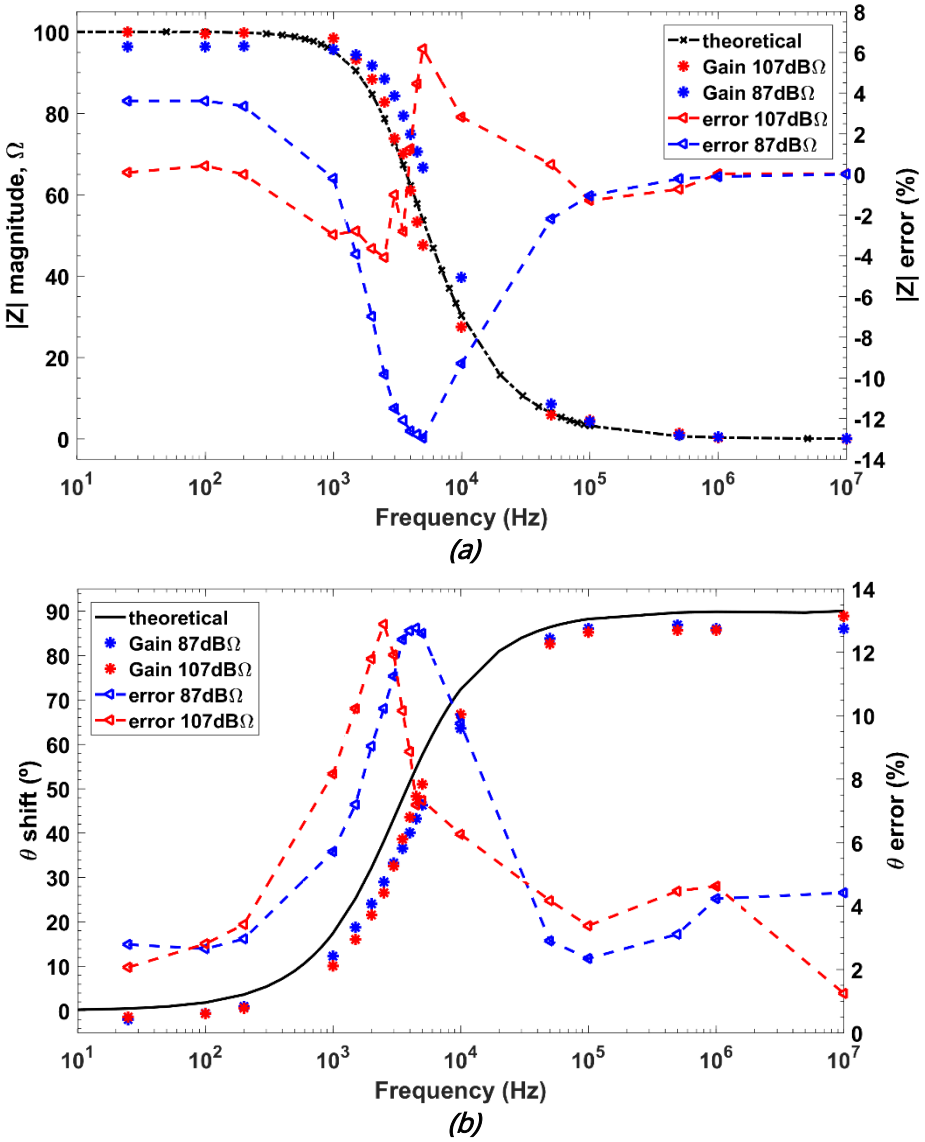


Figure 4.11. Recovered *Z* magnitude and phase in C-mode for 87 dBΩ and 107 dBΩ gain and their normalized errors (w/o calibration): a) magnitude: recovered vs theoretical; and b) phase: recovered vs theoretical.

For C-mode, Figure 4.11 shows the recovered magnitude and phase at 18 different frequencies over the 25 Hz-10 MHz range, for an AC input voltage of 1 mV_{pp} at 87 dBΩ and 350 μV_{pp} at 107 dBΩ. Figure 4.11a shows the recovered magnitude compared to the theoretical value and Figure 4.11b shows the recovered phase compared to its theoretical value. The full-scale magnitude (Figure 4.11a) and phase (Figure 4.11b) recovery errors are below 6.2 % and 12.9 % with maximum gain configuration, and below 13 % and 13 % with minimum gain configuration, for all the frequency range.

4.2. WIDEBAND COMPACT FRONT-END

A single-stage compact version of the previous dual-phase FRA-IS read-out with reduced power consumption recovering simultaneously both I and Q responses is presented in this section. While meeting the LVLP constraints, it presents an ultra-compact topology operating at frequencies up to the 100 MHz range (molecular and cell range), contributing to the creation of the next generation of lab-on-chip devices.

4.2.1. System architecture

The block diagram of the proposed IS front-end is shown in Figure 4.12. As in the previous proposal, to enhance CMRR and reduce noise, a fully differential configuration is considered. It is based on an open-loop Transconductor-Transimpedance (TC-TI) approach [**3, 4**], with shared input TC and two identical I, Q quadrature TIs with embedded mixer (TI-$M_{I,\,Q}$). These strategies result in an enhanced bandwidth with better area and power efficiency. Both DC V_x and V_y I, Q outputs are simultaneously recovered after fully integrated LPFs, implemented using the G_m-C integrator reported in [**2**], optimized to work in this application.

The schematic is shown in Figure 4.13. The input signal is driven to the TC input stage through a QFG structure to allow direct sensor/front-end coupling, setting V_{cm} = 0.9 V and a high pass frequency $f_{c,H} = 1/2\pi R_{QFG}C_{in}$. The capacitance C_{in} = 1 pF (MIM) and R_{QFG} is a NMOS transistor, whose equivalent resistance can be modified through the gate voltage V_{ctrl}, adjusting $f_{c,H}$, in a 6.7 Hz-172 kHz range to filter low-frequency noise and undesired signal contributions, regulating the operating frequency range. The shared TC-stage (Figure 4.13) is based on a NMOS-input Flipped Voltage Follower (FVF) degenerated through a 5-bit array of symmetrical resistances R_{TC}, implemented with MOS-switches in series with POLY-resistances. The input differential voltage is buffered to R_{TC} and converted to current. The TC output currents are copied to I, Q TIs through the unity gain current mirrors M_N-$M_{N'}$, then converted back to voltage using load POLY resistors R_{Load} = 35 kΩ, achieving overall programmable gains $G=R_{LOAD}/R_{TC}$ ranging from 0 dB to 40 dB in 10 dB steps and 100 MHz bandwidth, allowing to fit different target applications.

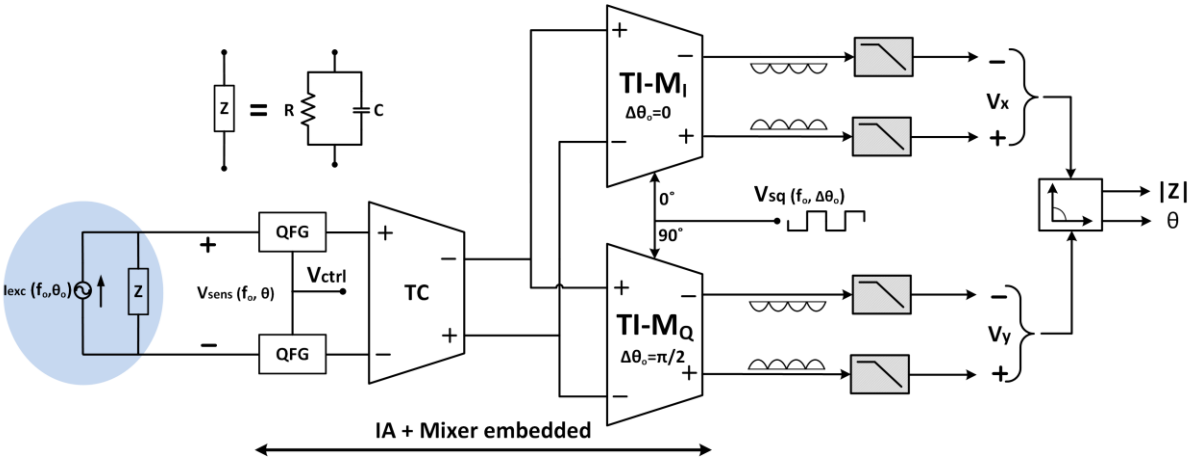


Figure 4.12. Proposed Dual-phase analog front-end structure for IS.

The embedded-multiplication technique is the same as in the previous section, using complementary control signals at the gates of matched transistors $M_2/2$- $M_2/2$ alternatively connected to outputs $\pm V_{out,Q}$. The output G_m-C integrator is the MOS-Cap O1F reported in Chapter 3, with tuneable cutoff frequency.

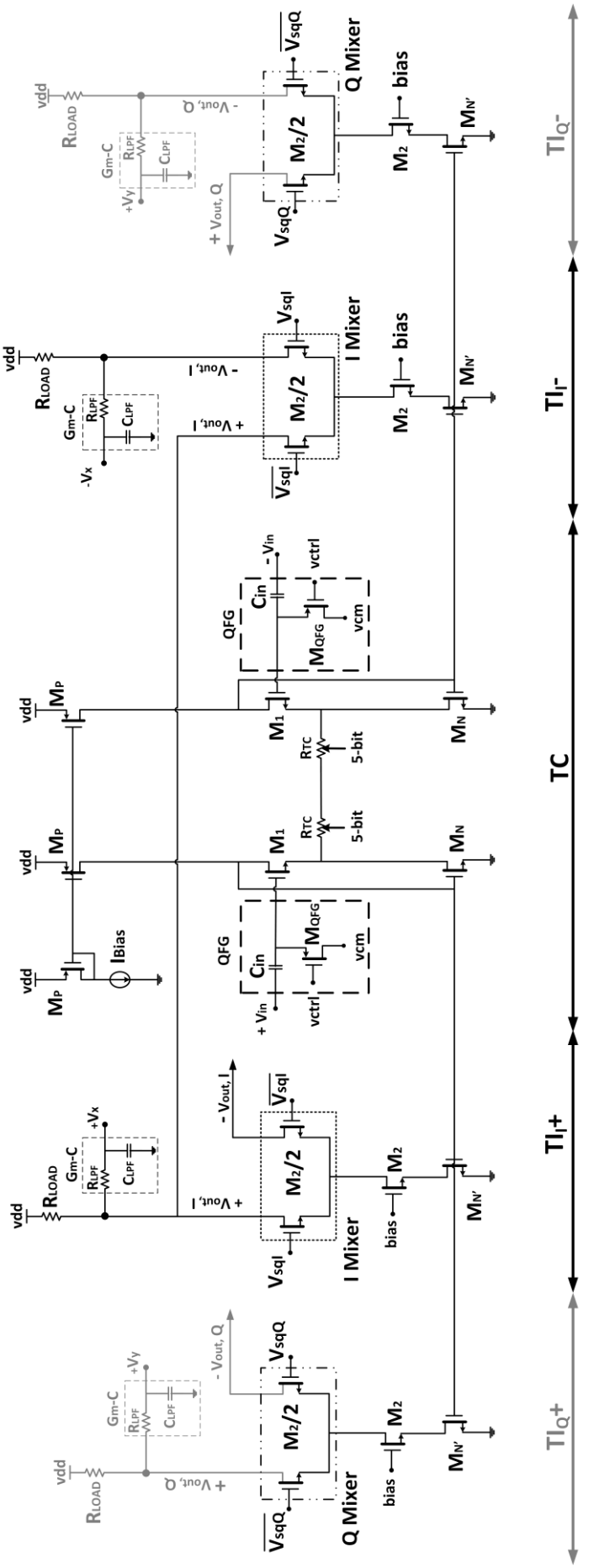


Figure 4.13. Proposed fully configurable TC-TI-M structure with dual I/Q output. Schematic view.

4.2.2. Performances

The proposed IS read-out has been designed in the 0.18 µm CMOS technology from UMC. The power supply is 1.8 V and a bias current I_{Bias} = 25 µA is set for the TC-TI-M structure (Figure 4.13) and I_{Bias} = 0.5 µA for the G_m–C integrators (Figure 4.3). It presents a total power consumption of 292 µW and an active area of 0.0569 mm^2 including the fully integrated G_m–Cs. The layout view of the proposed system is shown in Figure 4.14.

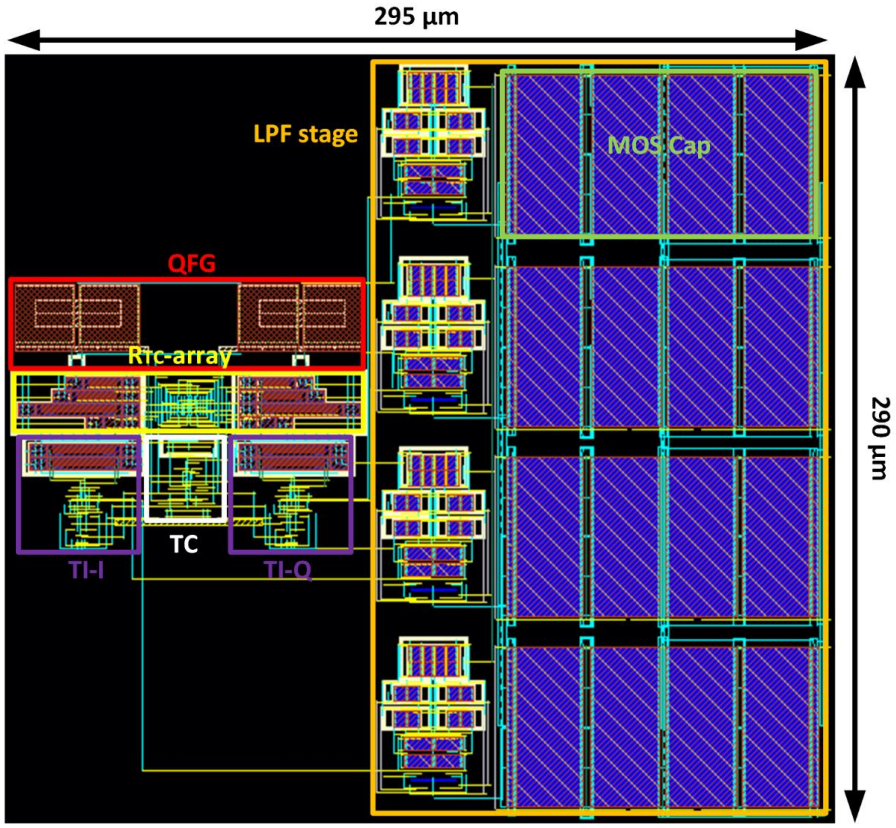


Figure 4.14. Layout view of the proposed structure.

Gain and Bandwidth

Figure 4.15 shows the 5-bit programmable gain post-layout frequency response, ranging from 0 dB to 40 dB. The bandwidth $f_{c,L}$ is kept around 100 MHz (varies from 87 MHz at maximum gain to 123 MHz at 0 dB). For the minimum gain setup, the frequency response for variable V_{ctrl} is also shown: the high pass cutoff frequency $f_{c,H}$ can be adjusted from 6.7 Hz (V_{ctrl} = 1.1 V) up to 172 kHz (V_{ctrl} = 0.5 V).

The variation over the temperature (from -40°C to 120°C) for maximum and minimum gains is shown in Figure 4.16. It shows a variation of 0.077 dB/°C for maximum gain and 0.0158 dB/°C for minimum gain respectively.

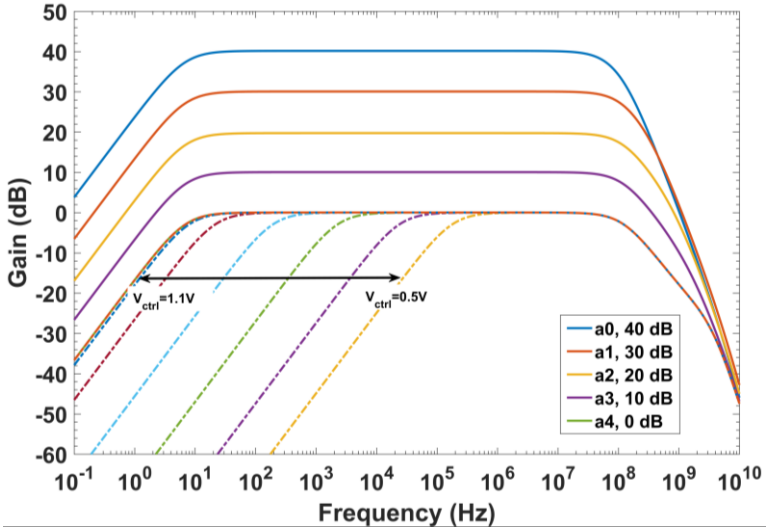


Figure 4.15. 5-bit programmable-gain, with High Pass Filtering control applied to minimum gain.

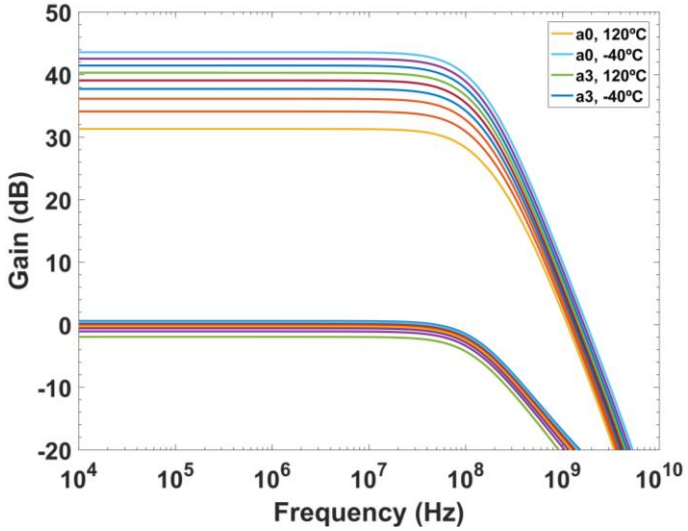
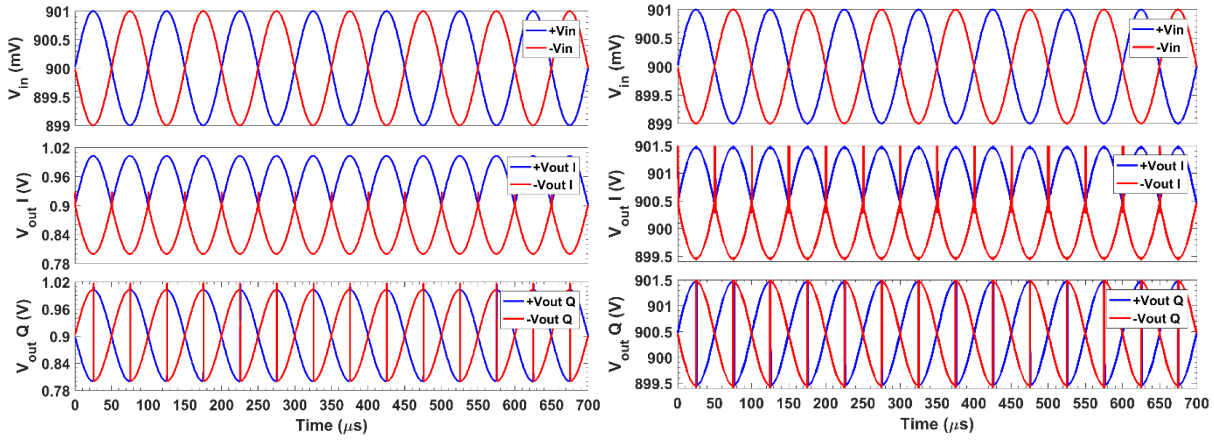


Figure 4.16. Gain variation over temperature ranging from -40°C to 120°C for maximum and minimum gain configurations.

Transient behaviour



(a) *(b)*

Figure 4.17. Synchronously rectified V_{outI} and V_{outQ} outputs. a) Gain = 40 dB; and b) Gain = 0 dB. Input signal: amplitude=1 mV, f_0 = 10 kHz in phase with V_{sqI}.

Figure 4.17 shows the behaviour of the synchronously rectified dual-phase outputs for an input signal of 1 mV at a f_0 = 10 kHz and maximum gain, with V_{sq} and V_{in} in phase. For this case, the theoretical $V_{x,theo} = (2/\pi)2V_{in}Gcos(\theta)$ = 127.3 mV, while after filtering V_{out}, the recovered V_x is $V_{x,rec}$ = 125.8 mV, showing a relative error of 1.2 %.

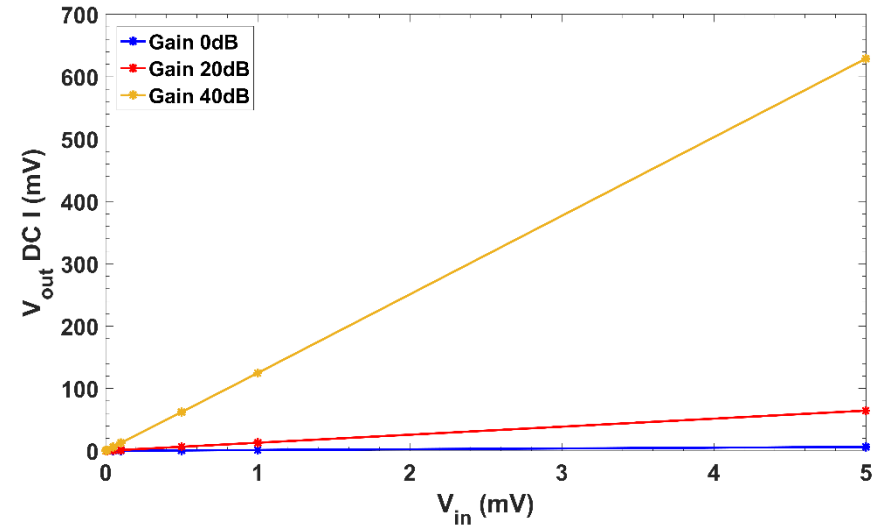
Noise

The rms integrated noise over the 6.7 Hz – 100 MHz frequency range (Table 4.2), with V_{ctrl} = 1.1 V, is 91.85 μV_{rms} for maximum gain and 1.732 mV_{rms} for minimum gain.

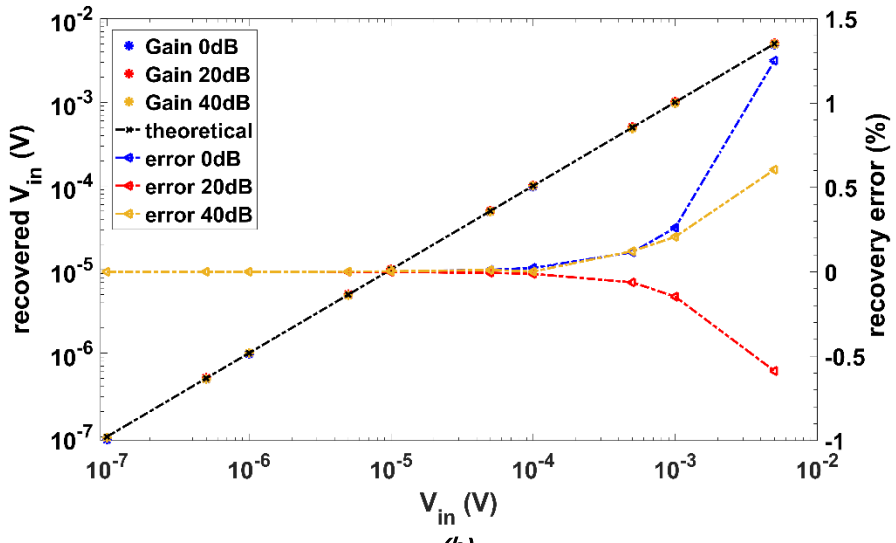
Table 4.2. RMS Integrated noise of the wideband compact FE.

Input mode	a0	a4
Gain	40.2 dB	0 dB
BW (Hz)	6.7-100M	6.7-100M
out (mVrms)	9.399	1.732
In (Vrms)	91.85 µ	1.732 m
In (nV/√Hz)	9.2	173.2

Recovery performance



(a)



(b)

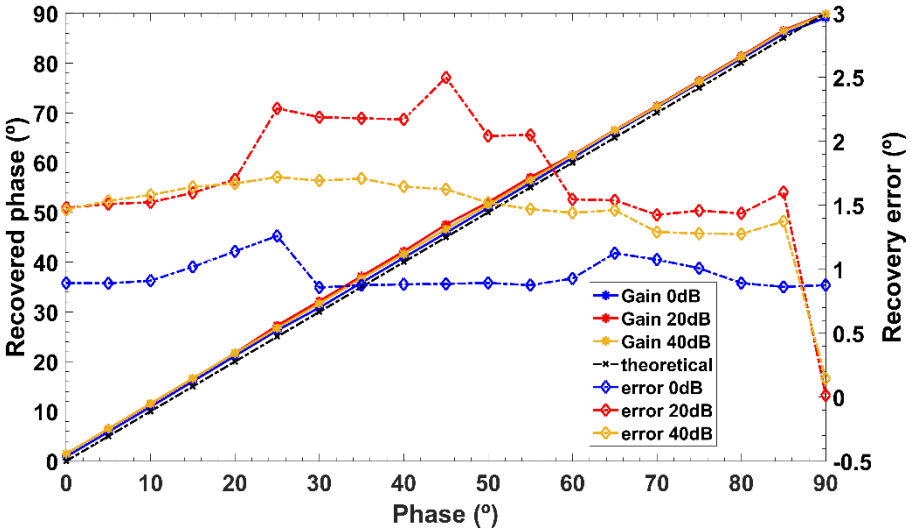


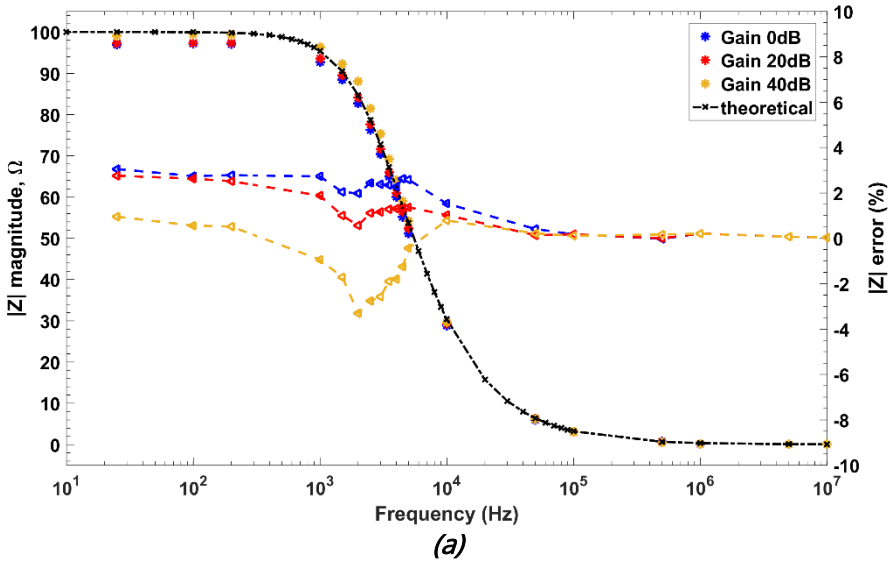
Figure 4.18. Recovered performance at 0 dB, 20 dB and 40 dB gain: a) DC output I (V_x) for an input signal amplitude from 100 nV to 5 mV; b) recovered input signal amplitude and error (%); and c) recovered phase and error (°), for a constant 1 mV input signal.

Figure 4.18a shows the simulated V_{out} DC I, V_x, and Figure 4.18b the recovered input amplitude and its error, for an AC input voltage ranging from 100 nV to 5 mV at 0 dB, 20 dB and 40 dB gain configurations, f_0 = 10 kHz in-phase with V_{sqI} and with the LPF cutoff set to $f_{c,L}$ =10 Hz. Again, due to the computational cost of simulating a single transient analysis with an f_0 in the order of MHz, and a LPF $f_{c,L}$ in the order of tens of Hz, the simulated operating frequency is limited to 10 kHz.

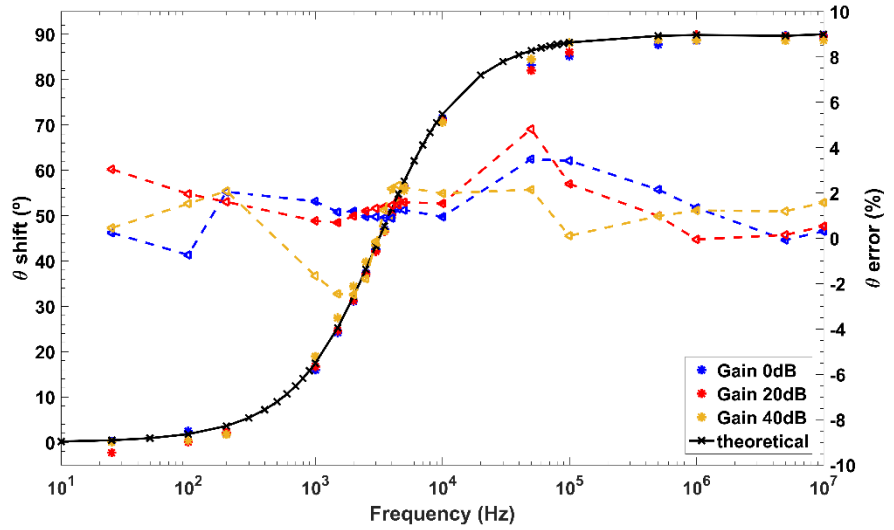
Figure 4.18c shows the recovered phase and its error at a fixed 1 mV input amplitude, f_0 = 10 kHz, $f_{c,L}$ = 10 Hz varying the input phase (θ) from 0º to 90º; note that phase offset calibration can be performed to optimize phase recovery.

Impedance characterization

To validate this proposal, the same Z impedance composed of a resistor R = 100 Ω in parallel with a capacitor C = 500 nF as shown in Figure 4.12 is used. Excited with an AC current, this generates the input voltage, V_{in}, driven through the QFG to the input pair of the TC-stage. The two resulting DC output voltages (V_x and V_y) at the branches I and Q are used to recover the phase shift and magnitude -or the real and imaginary components- of the impedance Z according to equations (4.1) and (4.2).

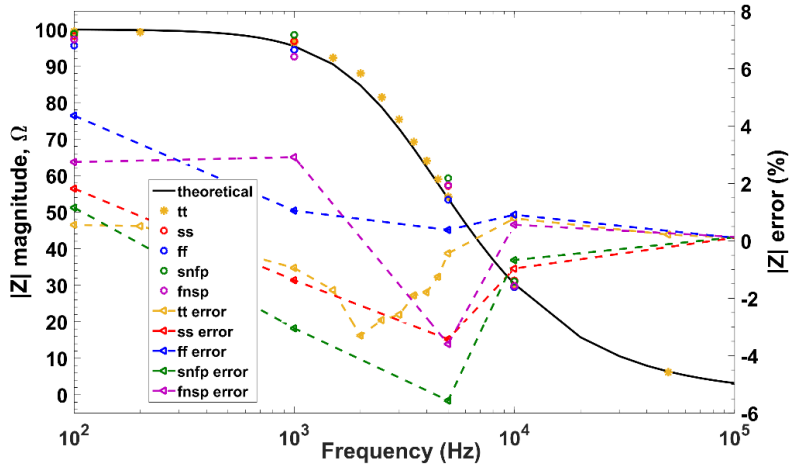


(a)



(b)

Figure 4.19. Recovered *Z* magnitude and phase for 0 dB, 20 dB and 40 dB gain and their normalized errors (w/o calibration): a) magnitude: recovered vs theoretical; and b) phase: recovered vs theoretical.



(a)

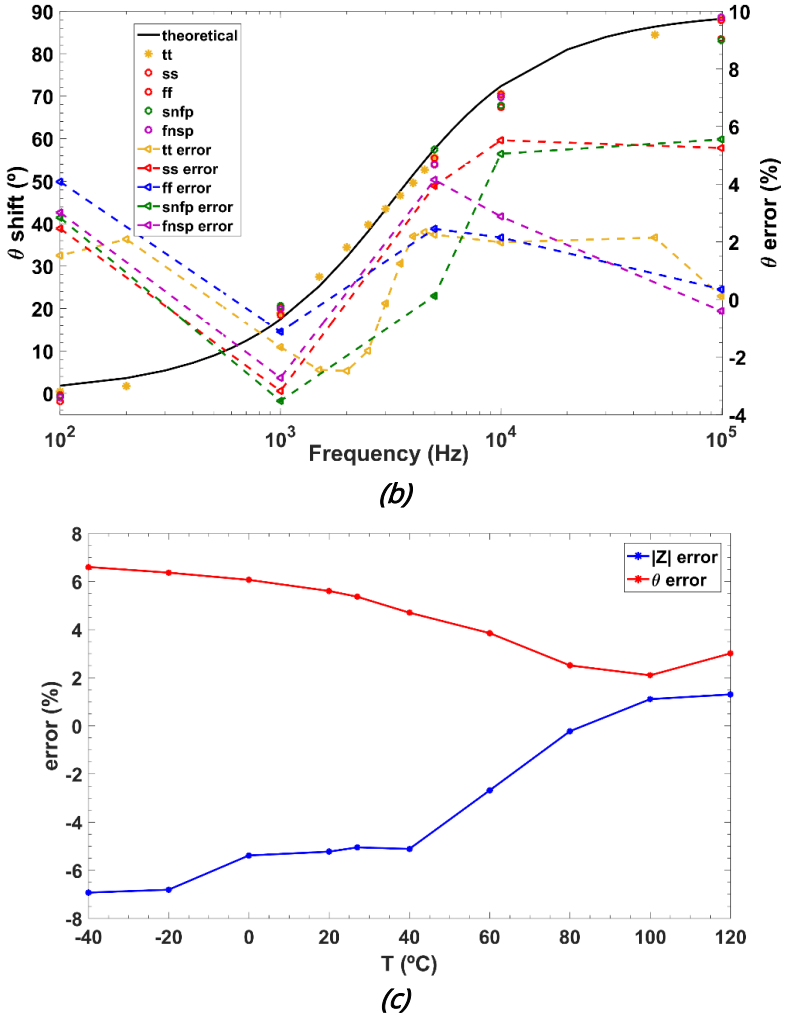


Figure 4.20. Recovered Z magnitude and phase (w/o calibration), 40 dB gain: corner analysis a) magnitude and b) phase; and c) temperature dependence at f_{in} = 5 kHz.

Figure 4.19 shows, the recovered magnitude and phase for an AC input current of 100 μA_{pp} at 19 different frequencies over the 25 Hz-10 MHz range, operating at 0 dB, 20 dB and 40 dB and a $f_{c,H}$ = 6.7 Hz (V_{ctrl} = 1.1 V), which renders the worst case recovery errors. Figure 4.19a shows the recovered magnitude compared to the theoretical value and Figure 4.19b shows the recovered phase compared to its theoretical value. The full-scale Z magnitude (Figure 4.19a) and phase (Figure 4.19b) recovery errors are below 3.3 % and 4.8 % for all the frequency range and gain configurations.

Figure 4.20 shows the corner and temperature analysis at 40 dB gain, with their full-scale errors. Figure 4.20a and Figure 4.20b display the corners for the recovered Z magnitude and phase, showing recovery errors below 5.6% (magnitude) and 5.5% (phase). Figure 4.20c presents the temperature dependence at f_{in} 5 kHz; recovery errors are below 7% for both magnitude and phase.

4.3. CONCLUSIONS

Two fully integrated reconfigurable dual-phase analog front-end for impedance spectroscopy has been presented, based on a fully differential approach. A comparison of the performance of the two proposed structures with other previously reported works operating over 100 kHz is presented in Table 4.3. Two FoMs are proposed based on [**5**] to compare the behaviour of our structure with previously reported works.

$$FoM_1 = \frac{Power\ [\mu W] * area(mm^2) * Phase\ error[°]}{Frequency\ range\ [Hz]} \tag{4.3}$$

$$FoM_2 = \frac{Power\ [\mu W] * area(mm^2) * Magnitude\ error[\%]}{Frequency\ range\ [Hz]} \tag{4.4}$$

Two fully integrated reconfigurable dual-phase analog front-end for impedance spectroscopy has been presented, based on a fully differential approach.

The dual-phase FE topology, reports the largest frequency range among the reviewed works in Table 4.3, being higher than the one achieved with compact FE topology, at the cost of a higher power and area consumption. Nonetheless, it presents competitive results in terms of power and area consumption while displaying two input signal modes, which considerably increases the complexity of the system. Its main drawback is a higher error of the recovered amplitude, but is still whithin the range of the reviewed literature.

The proposed compact mixer-embedded Front-End structure results in a compact solution (0.0569 mm^2 area) with a wide bandwidth of 87 MHz, a programmable gain from 0 dB to 40 dB and a low power consumption of 291.6 µW, while keeping both recovery errors within competitive values.

Both proposed structures present magnitude and phase recovery errors within competitive values, reporting, overall, the best performance-consumption trade-offs as shown by FoM_1 and FoM_2.

Table 4.3. Comparison with previously reported works.

Parameter	Dual-Phase FE		Dual-Phase Compact FE	[5]'13	[6]'13	[7]'15	[8]'16	[9]'20	[10]'20	[11]'21	[12]'21
Results	Post-lay		Post-lay	Exp	Sim	Exp	Sim	Sim	Exp	Sim	Exp
Mag&Phase recovery	Yes		Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
LPF integrated	Yes, tuneable		Yes, tuneable	Yes	N/A	No	Yes	Yes	Yes	Yes	N/A
Input mode	V/C		V	V	V	C	V	V	V/C	V	V
CMOS (µm)	0.18		0.18	0.18	0.18	Arduino-based	0.18	0.18	0.18	0.18	0.065
Supply (V)	1.8		1.8	1.8	±0.9	N/A	1.8	1.8	1.8	1.8	1.8, 3.3
Power (W)	461.5µ*		291.6µ*	37m	28m	N/A	482µ	36.1µ	311.4µ	544µ	9.6m
Area (mm^2)	0.0769*		0.0569*	5	0.4	N/A	0.03	N/A	0.208	1.95	16 (die, 8ch)
Gain (dB)	**(V-mode)** 20-40	**(C-mode)** 87-107dBΩ	0-40	N/A	N/A	N/A	39-59	0-20	N/A	7-48	24
Freq. range (Hz)	6.9-100M	0.16-130M	6.7–87M	15M-20M	100-580k[(c)]	0.01-100k	1.1M	0.1–1M	DC-100k	100-10M	1k-10M
Noise (V/√Hz)	21n-25.3n	4.7 pA-6.8 pA	224.4n-16.7n[(a)]	N/A	N/A	N/A	N/A	189.6n[(a)]	80fA	N/A	14.2 @10-100kHz
CMRR (dB)	137 @ 100kHz	219.9 @ 100kHz	164.4 @ 100kHz	N/A	N/A	N/A	78@100kHz	55.3	N/A	N/A	N/A
Phase recov error	<1.4°	<4.8°	<2.5° / <1°[(b)]	N/A	<2.2°	<3°	N/A	<1.7°	<10%[(d)]	<1.8°[(d)]	<4.32°
Amp recov error	<7.3%	<5%	<1.9%	N/A	<2.5%	<5%	<10%	N/A	<10%[(d)]	<1%[(d)]	N/A
FoM_1 (kHz/°/µW)	0.497µ	1.31µ	0.477µ / 0.191µ	N/A	9.42m	N/A	N/A	16.3	6.48m	190.9u	8.3m[(e)]
FoM_2 (kHz/µW)	2.59µ	1.36µ	0.362µ	N/A	8.29m	N/A	0.228	N/A	6.48m	106.1u	N/A

N/A Not Available; *Complete FRA-IS readout (FE+LPFs); [(a)]Simulated Input-referred noise; [(b)]without/with phase offset calibration; [(c)]increased to 10 MHz for minimum gain; [(d)] recovered Z error; [(e)] for an area of 2 mm^2/channel.

4.4. REFERENCES

1. Cinco-Izquierdo, O.J., Sanz-Pascual, M.T., de la Cruz-Blas, C.A. and Calvo-López, B. Low Power CMOS Chopper Preamplifier Based on Source-Degeneration Transconductors. I*EEE Latin American Symposium on Circuits & Systems (LASCAS)*, San Jose, Costa Rica, 2020.
2. Pérez-Bailón, J., Calvo, B. and Medrano, N. A CMOS Low Pass Filter for SoC Lock-in-Based Measurement Devices, *Sensors*, 2019.
3. Kim, J. and Ko, H. Reconfigurable Voltage/Current Readout Instrumentation Amplifier for Cardiovascular Health Monitoring. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018.
4. Rao, A., Teng, Y.-C., Schaef, C., Murphy, E.K., Arshad, S., Halter, R.J. and Odame, K. An Analog Front End ASIC for Cardiac Electrical Impedance Tomography. *IEEE Transactions on Biomedical Circuits and Systems*, 2018.
5. Hu, A. and Chodavarapu, V.P. General-purpose high-speed integrated lock-in amplifier with 30dB dynamic reserve at 20MHz. *Analog Integrated Circuits and Signal Processing*, 2013.
6. Huang, H. and Palermo, S. A TDC-based front-end for rapid impedance spectroscopy. *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Columbus, USA, 2013.
7. Grassini, S., Corbellini, S., Angelini, E., Ferraris, F. and Parvis, M. Low-Cost Impedance Spectroscopy System Based on a Logarithmic Amplifier. *IEEE Transactions on Instrumentation and Measurement*, 2015.
8. Maya-Hernández, P.M., Sanz-Pascual, M.T. and Calvo, B. Micropower CMOS lock-in amplifier for portable applications. *Electronics Letters*, 2016.
9. Márquez, A., Medrano, N., Calvo, B. and Pérez-Bailón, J. A Dual Synchronous Demodulator for Phase Sensitive Detection Applications. *IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, Dubrovnik, Croatia, 2020.
10. Shen, B. and Johnston, M.L. DC-100 kHz Tunable Readout IC for Impedance Spectroscopy and Amperometric Measurement of Electrochemical Sensors. *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, USA, 2020.
11. Cheon, S.-i., Kweon, S.-J., Kim, Y., Ha, S. and Je, M. A Power-Efficient, Wide-Frequency-Range Impedance Measurement IC Using Frequency-Shift Technique. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021.
12. Lee, J., Gweon, S., Lee, K., Um, S., Lee, K.-R. and Yoo, H.-J. A 9.6-mW/Ch 10-MHz Wide-Bandwidth Electrical Impedance Tomography IC With Accurate Phase Compensation for Early Breast Cancer Detection. *IEEE Journal of Solid-State Circuits*, 2021.

Chapter 5
Conclusions

In this final chapter, general conclusions are discussed and the main thesis contributions are summarized. Future research paths are finally addressed.

5.1. Contribution of this Thesis

In this thesis, we have focused on delving into the design of a truly portable, battery-operated low-power processing system for impedance spectroscopy measurement, based on CMOS microelectronic technologies, contributing to the creation of the next generation of Lab-on-Chip devices. The reported results demonstrate that wideband FRA-based IS front-ends have the potential to be integrated in low-cost CMOS processes featuring low-voltage low-power, showing very promising performances when compared with state of the art solutions.

The most relevant contributions of this work are highlighted below.

A brief introduction to the current state of the art of Impedance Spectroscopy is done in Chapter 1, deriving the motivation and objectives of this work.

In Chapter 2, the design of the power management unit based on a fully integrated Low Dropout Regulators is considered. A fully integrated 0.18 µm CMOS LDO regulator providing a regulated nominal 1.8 V supply has been presented with internal compensation and a dynamic current bias boosting circuit to enhance the transient behaviour. The experimental characterization validates the fulfilment of the target design specifications obtaining an LDO regulator compatible with portable battery operated systems, achieving better overall line (0.081 mV/V) and load regulation (-0.82 mV/mA) with a reduction of the power consumption (13.41 µW) while it keeps similar time response parameters (<2.5 µs full load ST) compared to previously reported works.

In Chapter 3, the different building blocks -amplifying stage, multiplying stage and output filtering stage- that constitute the analog front-end for impedance spectroscopy have been presented.

For the input stage, two wideband amplifiers based on a TC-TI approach are introduced: the front-end preamplifier has both voltage and current mode inputs, a fixed gain (26 dB/89 dBΩ) and minimum power and area consumption (180.4 μW, 0.0115 mm^2); the second one exhibits a 4-bit programable gain (6-26 dB), again with minimum power and area consumption (180.4 μW, 0.0062 mm^2). The mixer has been embedded within the TI output stage of this late variable gain amplifier, achieving a truly compact structure.

Finally, two fully integrated LPF based on a G_m-C structure exploiting a current steering Gm-tuning and reduction approach operating at 1.8 V power supply are designed and characterized. Both the first order and the second order LPFs presents a five orders of cutoff frequency range, from sub-Hz to kHz, with a low power consumption (5.4 μW the O1F and 9.9 μW the O2F), reduced size and a high dynamic range (>70 dB).

Finally, in Chapter 4, two wideband (~100 MHz) complete dual-phase FRA-IS read-out front-end schemes, based on the previous presented cells, are reported, capable of simultaneously recovering two DC voltage values that are proportional to the real and imaginary components of the impedance under test, Z.

The first one combines the different stages introduced in Chapter 3: a TC-TI preamplifier (26 dB/89 dBΩ) with both voltage and current input, followed by a TC-TI VGA (6-26 dB) adapted for dual-phase operation by only replicating the output TI-mixer stage, and a filtering output stage, with sub-Hz to kHz tuneable cutoff frequency, to recover the impedance magnitudes.

The second one is a compact simplified version, based on just one TC-dual TI 0-40 dB gain- tuneable amplifier, which reduces area (0.0569 mm^2) and power consumption (291.6 μW) at the expense of trading the bandwidth (87 MHz).

Both have been validated recovering an impedance Z composed of a resistor R = 500 Ω in parallel with a capacitor C = 500 nF, providing similar recovery results.

Finally, the author has also paid special attention to the automated control of instrumentation and data acquisition, developing specific characterization systems for the different integrated prototypes, designing the corresponding PCBs and the different codes necessary to carry out automation.

5.2. FUTURE RESEARCH LINES

Throughout this thesis, different proposals for each component of a portable sensor device based on a dual synchronous demodulation technique has been presented. Nonetheless, further work is still required to complete and optimize the whole system.

First, the experimental characterization of the LNA-VGA blocks must be done in order to fully validate their performance, both as individual building blocks and for the read-out chain. In this way, the implemented designs can be reviewed from the experimental data obtained so that to be optimized in any possible way. In terms of optimization, the reported LPFs have been designed following single-ended topologies, but fully differential implementations should better fit within this application, so this stage can be futher analysed and redesigned, looking for a compact tunable fully differential aprroach.

Besides, a complete System in Package (SiP) prototype with all the components to be used as an autonomous impedance characterization device, including the quadrature signal generator and an embedded microcontroller, should be designed and validated, preferably in a “real case” sensing application.

Finally, another key point to address is to parallelize the system.

Appendix I
UMC 0.18-μm CMOS Technology

UMC L180 MM/RF 1.8V/3.3V 1P6M CMOS technology based on P-substrate structure with 6 metal layers and 1 poly layer.

I.I. TECHNOLOGY CHARACTERISTICS

Shrink technology: NO
Core voltage: 1.8V
I/O voltage: 3.3V
Shallow Trench Isolation (STI)
Triple well
Substrate resistivity: 15~25 Ohm.cm on <100> P- substrate
Standard PMOS and NMOS transistors
Low V_{th} PMOS and NMOS transistors
Zero V_{th} NMOS transistors
Temperature range: -40°C to 125°C
Number of metals: 6
Interconnect material: Al
Dielectric: FSG
Top metal 8KA, 12 KA or 20KA
Inductors
MoM
MiM 1 fF/μm^2
Passivation single

I.II. DEVICE PARAMETERS

Capacitor

MIMCAS_MM	(1.28µm/1.28µm)	2.0224 fF

Resistor

RNHR1000_MM	(1µm/1µm)	902.19 Ω
RNNPO_MM	(1µm/1µm)	162.79 Ω
RNPPO_MM	(1µm/1µm)	589.10 Ω

Table I.1. Main technological parameters for transistors in UMC 180nm.

Transistor		Nominal		Low Vth		Zero Vth	
$V_{ds,max}$		1.8V	3.3V	1.8V	3.3V	1.8V	3.3V
L_{min} (µm)		0.18	0.34	0.24	0.5	0.3	0.5
L_{max} (µm)		50	50	50	50	50	50
W_{min} (µm)		0.24	0.24	0.24	0.8	0.24	0.8
W_{max} (µm)		100	100	100	100	100	100
V_{Th} (V)	NMOS	0.51	0.592	0.016	0.31	-0.19	0.062
	PMOS	-0.5	-0.72	-0.22	-0.42	N/A	N/A

Appendix II
Line & Load Regulation

This appendix collects the detailed analysis in small signal (AC) and DC of the line regulation factor, LNR, and the load regulation factor, LDR, of a LDO. As reported in Chapter 2, this LDO regulator is considered to be made up of an OTA amplifier and a pass transistor, with a resistive loop as the negative feedback. Figure II.1a shows said schematic.

III.I. AC ANALYSIS

In this section the AC analysis for the Line and Load regulation is performed.

III.I.I. Load regulation (LDR)

The equivalent scheme for small signals corresponds to that shown in Figure II.1b, where $V_{fb}=R_{fb2}/(R_{fb1}+R_{fb2})V_{out}$.

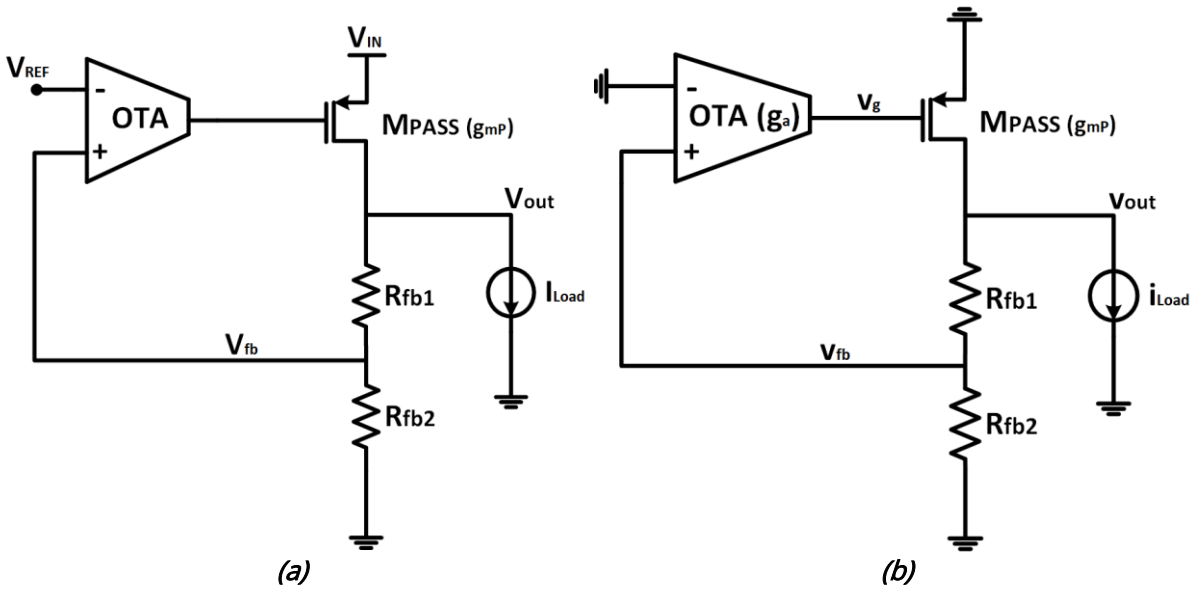


Figure II.1. LDO regulator a) basic schematic; and b) AC analysis for LDR.

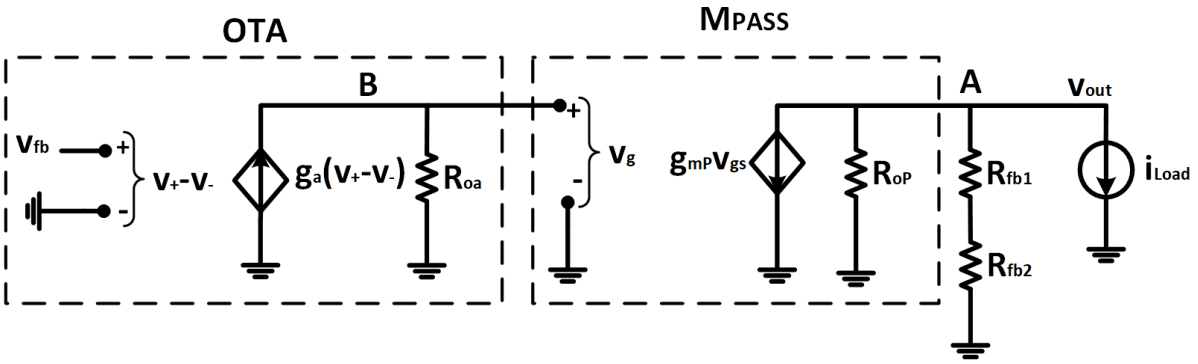


Figure II.2. Small signal model.

Substituting each component for its incremental model, the linear system of Figure II.2 is obtained. Since $V_{fb}=(v_+-v_-)=R_{fb2}/(R_{fb1}+R_{fb2})v_{out}$, and $V_{gs}=v_g$ analysing node B, we can put

$$\frac{\boldsymbol{v_g}}{\boldsymbol{R_{oa}}}=\boldsymbol{g_a}(\boldsymbol{v_+}-\boldsymbol{v_-})=\boldsymbol{g_a}\frac{\boldsymbol{R_{fb2}}}{\boldsymbol{R_{fb1}}+\boldsymbol{R_{fb2}}}\boldsymbol{v_{out}}\rightarrow\boldsymbol{v_g}=\boldsymbol{g_aR_{oa}}\frac{\boldsymbol{R_{fb2}}}{\boldsymbol{R_{fb1}}+\boldsymbol{R_{fb2}}}\boldsymbol{v_{out}} \quad \text{(II.1)}$$

On the other hand, and according to node A

$$\frac{v_{out}}{R_{oP}}+\frac{v_{out}}{R_{fb1}+R_{fb2}}+g_{m_P}v_g+i_{Load}=0 \quad \text{(II.2)}$$

(II.1) in (II.2) results in

$$\frac{v_{out}}{R_{oP}}+\frac{v_{out}}{R_{fb1}+R_{fb2}}+g_{mP}g_a\frac{R_{oa}R_{fb2}}{R_{fb1}+R_{fb2}}v_{out}+i_{load}=0 \quad \text{(II.3)}$$

Multiplying by $R_{oP}(R_{fb1}+R_{fb2})$

$$v_{out}\left(R_{fb1}+R_{fb2}+R_{oP}+g_{mp}g_aR_{oa}R_{fb2}R_{oP}\right)=-i_{load}R_{oP}\left(R_{fb1}+R_{fb2}\right) \quad \text{(II.4)}$$

Then

$$LDR=\frac{v_{out}}{i_{Load}}=-\frac{R_{oP}\left(R_{fb1}+R_{fb2}\right)}{R_{fb1}+R_{fb2}+R_{oP}+g_{m_P}g_aR_{oa}R_{oP}R_{fb2}} \quad \text{(II.5)}$$

Assuming that $g_{mP}g_aR_{oa}R_{oP}R_{fb2}$ is the dominant term on the denominator $(R_{fb1}+R_{fb2}+R_{oP}<<g_{mP}g_aR_{oa}R_{oP}R_{fb2})$, it can be approximated to

$$LDR\approx-\frac{1}{g_{m_P}g_aR_{oa}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)=-\frac{1}{g_{m_P}A_V}\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \quad \text{(II.6)}$$

Where $A_V=g_aR_{oa}$ is the OTAs open-loop voltage gain.

III.I.II. Line regulation (LNR)

Assuming now that there is a small variation in the input power supply, the resulting scheme in AC is indicated in Figure II.3a.

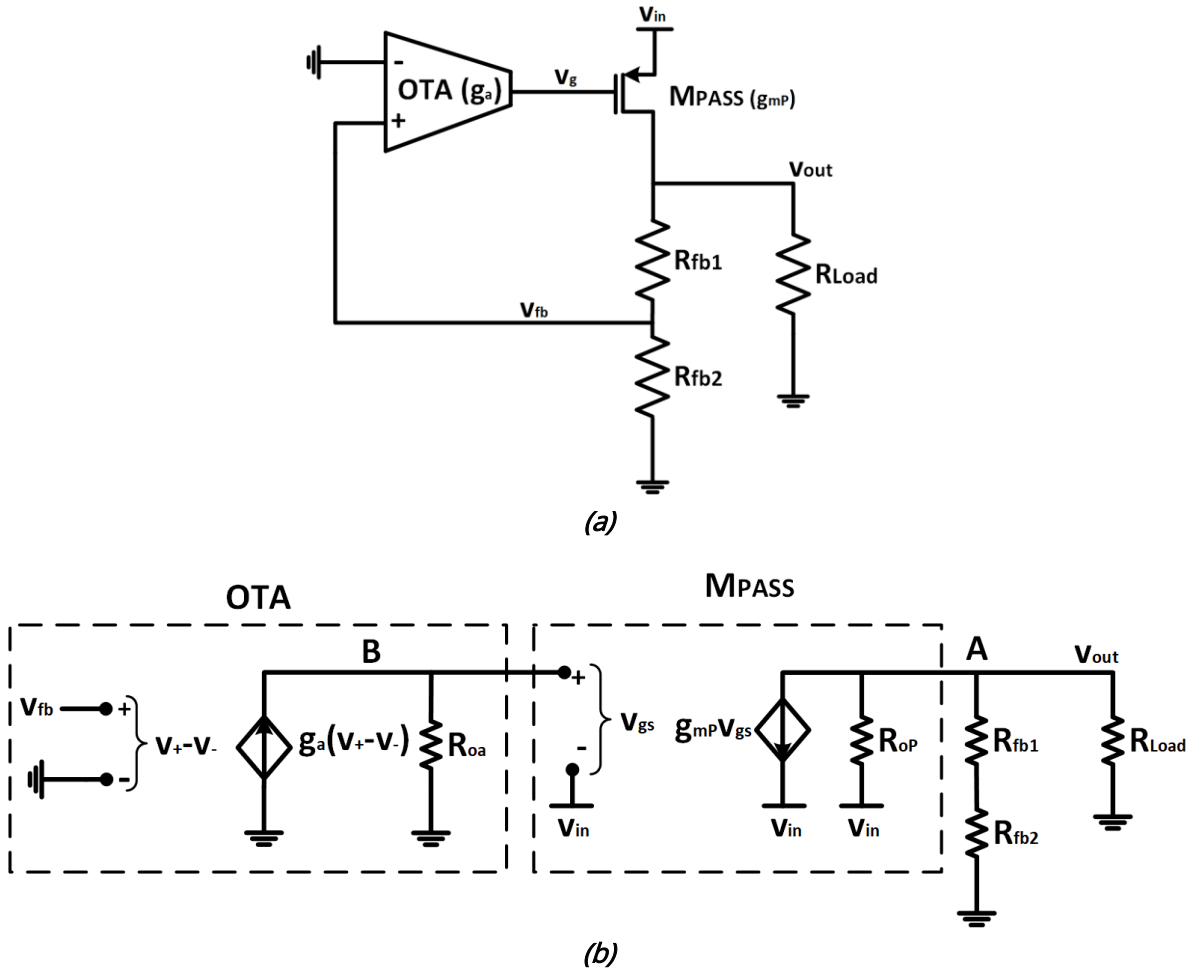


Figure II.3. LDO regulator a) scheme for LNR in AC; and b) small signal model.

Substituting each component for its respective incremental models, the equivalent circuit of Figure II.3b is obtained.

Proceeding similarly to the previous case, Kirchhoff's law applied to nodes A and B translates into

$$\frac{v_{out}}{R_{Load}} + \frac{v_{out}}{R_{fb1}+R_{fb2}} + \frac{v_{out}-v_{in}}{R_{oP}} + g_{m_P}(v_g - v_{in}) = 0 \tag{II.7}$$

$$\frac{v_g}{R_{oa}} = g_a \frac{R_{fb2}}{R_{fb1}+R_{fb2}} v_{out} \rightarrow v_g = g_a R_{oa} \frac{R_{fb2}}{R_{fb1}+R_{fb2}} v_{out} \tag{II.8}$$

Substituting v_g from (II.8) in (II.7) results in

$$\frac{v_{out}}{R_{Load}} + \frac{v_{out}}{R_{fb1}+R_{fb2}} + \frac{v_{out}-v_{in}}{R_{oP}} + g_{m_P}\left(g_a R_{oa} \frac{R_{fb2}}{R_{fb1}+R_{fb2}} v_{out} - v_{in}\right) = 0 \tag{II.9}$$

Multiplying by $R_{load}(R_{fb1}+R_{fb2})R_{oP}$

$$v_{out}\left[\left(R_{fb1}+R_{fb2}+R_{Load}\right)R_{oP}+R_{Load}\left(R_{fb1}+R_{fb2}\right)+g_{m_P}g_aR_{oa}R_{fb2}R_{Load}R_{oP}\right] = g_{m_P}R_{Load}\left(R_{fb1}+R_{fb2}\right)R_{oP}v_{in}+R_{Load}\left(R_{fb1}+R_{fb2}\right)v_{in} \quad \text{(II.10)}$$

This allows obtaining

$$LNR=\frac{v_{out}}{v_{in}}=\frac{1+g_{m_P}R_{oP}}{1+\frac{R_{oP}}{R_{Load}}+\frac{R_{oP}}{R_{fb1}+R_{fb2}}+g_{m_P}g_aR_{oa}R_{oP}\frac{R_{fb2}}{R_{fb1}+R_{fb2}}} \quad \text{(II.11)}$$

Assuming $g_{mP}R_{oP}>>1$ *and* $g_{mP}g_aR_{oa}R_{oP}R_{fb2}$ is the dominant term on the denominator ($g_{mP}g_aR_{oa}R_{oP}R_{fb2} >> (1+R_{oP}/R_{load})*(R_{fb1}+R_{fb2})$) the line regulation can be approximated by

$$LNR\approx\frac{1}{g_aR_{oa}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)=\frac{1}{A_V}\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \quad \text{(II.12)}$$

There are other contributions to LNR, since the variations of v_{in} also affect the supply voltage of the error amplifier, in this case an OTA, and the reference voltage, V_{ref}. Nonetheless, we have supposed that V_{ref} is barely influenced by v_{in}.

The effect that the variation of the power supply will have over the EA, can be translated by analogy with an operational amplifier by the $PSRR^+$ (Power Supply Rejection Ratio), which corresponds to describe it by connecting a voltage generator $v_{in}/PSRR^+$ to the non-inverting input [1].

Figure II.4a shows the excitation v_{in} corresponding to the small signal circuit, while Figure II.4b presents the equivalent model using the $PSRR^+$ of the OTA.

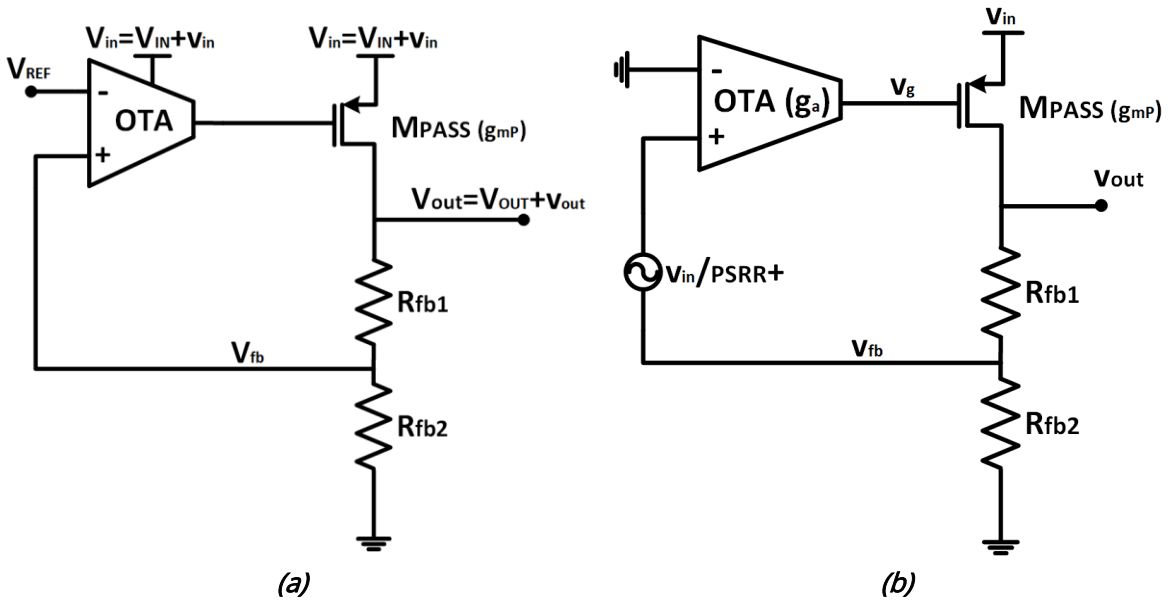


Figure II.4. LNR considering the effect of v_{in} on the OTA a) initial scheme and b) small signal model.

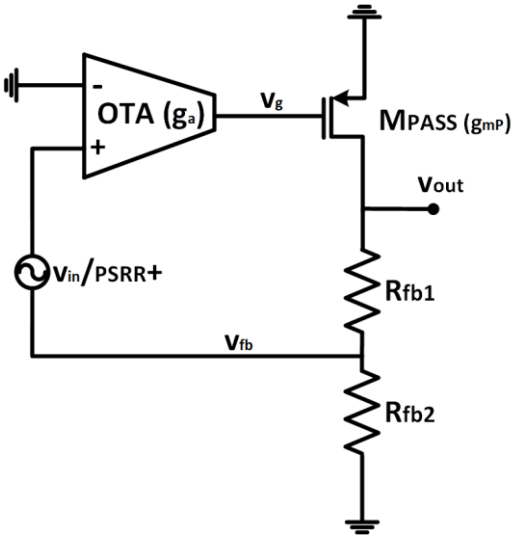


Figure II.5. V_{in} contribution on the OTA.

Since the incremental equivalent is linear, the superposition theorem can be applied to such a scheme; thus, the contribution of v_{in} coincides with the result shown in equation (II.12).

Regarding the contribution of the excitation v_{in}/PSRR$^+$ (Figure II.5), if it is considered that the OTA gain is very high, and given that $v_-\approx 0$, $v_+=0$, so that $v_{fb}=-v_{in}$/PSRR$^+$, so that

$$v_{out2} = \left(1+\frac{R_{fb1}}{R_{fb2}}\right)v_{fb} = -\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\frac{v_{in}}{PSRR^+} \tag{II.13}$$

The output voltage is

$$v_{out} = v_{out1} + v_{out2} = \left(\frac{1}{A_V}-\frac{1}{PSRR^+}\right)\left(1+\frac{R_{fb1}}{R_{fb2}}\right)v_{in} \rightarrow \tag{II.14}$$

Thus

$$LNR = \frac{v_{out}}{v_{in}} = \left(\frac{1}{A_V}-\frac{1}{PSRR^+}\right)\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \tag{II.15}$$

III.II. DC ANALYSIS

In this section the DC analysis for the line and load regulation is performed. Since the main purpose of the LDO regulator is to generate a DC voltage, it is essential to undergo the most detailed analysis possible of this system in DC.

For a first order approximation, it is considered that the error amplifier can be idealized, in the sense of considering that it has a transconductance g_a tending to infinity, as well as a very high input impedance.

Under these conditions $V_- = V_+ = V_{REF} = V_{FB}$ and $I_{R_{fb1}} = I_{R_{fb2}}$

In accordance with these conditions

$$\frac{V_{OUT}-V_{FB}}{R_{fb1}}=\frac{V_{OUT}-V_{REF}}{R_{fb1}}=\frac{V_{REF}}{R_{fb2}} \tag{II.16}$$

Thus, in first approximation

$$V_{OUT}=\left(1+\frac{R_{fb1}}{R_{fb2}}\right)V_{REF} \tag{II.17}$$

A more accurate approximation of the output voltage can be obtained by assuming that g_a is high, but finite. In this case, the input resistances of the OTA are still considered infinite so that

$$I_{Rfb1}=I_{Rfb2}=\frac{V_{OUT}-V_{FB}}{R_{fb1}}=\frac{V_{FB}}{R_{Rfb2}}\rightarrow V_{FB}=\frac{R_{fb2}}{R_{fb1}+R_{fb2}}V_{OUT} \tag{II.18}$$

Then, the I_{DS} current of the pass transistor can be expressed as

$$I_{DS}=\frac{V_{OUT}}{R_{LOAD}}+\frac{V_{OUT}-V_{FB}}{R_{fb1}}=\frac{V_{OUT}}{R_{LOAD}}+\frac{V_{OUT}}{R_{fb1}}\left(1-\frac{R_{fb2}}{R_{fb1}+R_{fb2}}\right) \tag{II.19}$$

Then

$$\rightarrow I_{DS}=\left(\frac{1}{R_{LOAD}}+\frac{1}{R_{fb1}+R_{fb2}}\right)V_{OUT} \tag{II.20}$$

Using the expression obtained for V_{OUT} in first approximation, equation (II.17), it results

$$I_{DS}=\left(\frac{1}{R_{LOAD}}+\frac{1}{R_{fb1}+R_{fb2}}\right)\left(1+\frac{R_{fb1}}{R_{fb2}}\right)V_{REF}=\frac{1}{R_{fb2}}\left(1+\frac{R_{fb1}+R_{fb2}}{R_{LOAD}}\right)V_{REF} \tag{II.21}$$

Defining $K=1+\frac{R_{fb1}+R_{fb2}}{R_{LOAD}}$, (II.21)can be rewritten as

$$I_{DS}=\frac{K}{R_{fb2}}V_{REF}=\frac{\beta}{2}(V_{IN}-V_G-|V_{TH}|)^2 \tag{II.22}$$

Which is equivalent to

$$\sqrt{\frac{2}{\beta}I_{DS}}=V_{IN}-V_G-|V_{TH}|\rightarrow V_G=V_{IN}-|V_{TH}|-\sqrt{\frac{2}{\beta}\frac{K}{R_{fb2}}V_{REF}} \tag{II.23}$$

Since V_G is the output voltage of the error amplifier, it can also be written as

$$V_G=A_V(V_+-V_-)=A_V\left[\frac{R_{fb2}}{R_{fb1}+R_{fb2}}V_{OUT}-V_{REF}\right] \tag{II.24}$$

Matching both expressions

$$V_{IN} - |V_{TH}| - \sqrt{\frac{2}{\beta}\frac{K}{R_{fb2}}V_{REF}} = A_V\left[\frac{R_{fb2}}{R_{fb1}+R_{fb2}}V_{OUT} - V_{REF}\right] \tag{II.25}$$

Therefore

$$V_{OUT} = \left(1+\frac{R_{fb1}}{R_{fb2}}\right)V_{REF} + \frac{1}{A_V}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\left\{V_{IN} - |V_{TH}| - \sqrt{\frac{2}{\beta}\frac{K}{R_{fb2}}V_{REF}}\right\} \tag{II.26}$$

Substituting K for its expression

$$V_{OUT} = \left(1+\frac{R_{fb1}}{R_{fb2}}\right)V_{REF} + \frac{1}{A_V}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\left\{V_{IN} - |V_{TH}| - \sqrt{\frac{2}{\beta}\left[\frac{1}{R_{fb2}}+\frac{1}{R_{LOAD}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\right]V_{REF}}\right\} \tag{II.27}$$

Assuming that

$$\frac{1}{R_{fb2}} + \frac{1}{R_{LOAD}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \approx \frac{1}{R_{LOAD}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \tag{II.28}$$

The output voltage V_{OUT} can be expressed as

$$V_{OUT} \approx \left(1+\frac{R_{fb1}}{R_{fb2}}\right)V_{REF} + \frac{1}{A_V}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\left\{V_{IN} - |V_{TH}| - \sqrt{\frac{2}{\beta}\left[\frac{1}{R_{LOAD}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\right]V_{REF}}\right\} \tag{II.29}$$

The expression is designated by I_{LOAD}

$$I_{LOAD} = \left[\frac{1}{R_{LOAD}}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\right]V_{REF} \tag{II.30}$$

In addition, by using said parameter, the output voltage V_{OUT} can be expressed as

$$V_{OUT} \approx \left(1+\frac{R_{fb1}}{R_{fb2}}\right)V_{REF} + \frac{1}{A_V}\left(1+\frac{R_{fb1}}{R_{fb2}}\right)\left\{V_{IN} - |V_{TH}| - \sqrt{\frac{2}{\beta}I_{LOAD}}\right\} \tag{II.31}$$

Thus, the output voltage is fundamentally controlled by V_{REF} and by R_{fb1}/R_{fb2}, as shown by equation (II.17); however, it also depends on V_{IN} and I_{LOAD}. Normally these two dependencies are usually characterized by line and load regulation, which can be determined by an incremental analysis, as has been done in the previous AC analysis, or redefined from the expression obtained for V_{OUT}, equation (II.31), such as

$$LNR = \frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{1}{A_V}\left(1+\frac{R_{fb1}}{R_{fb2}}\right) \tag{II.32}$$

$$LDR = \frac{\partial V_{OUT}}{\partial I_{LOAD}} = -\frac{1}{A_V}\frac{1}{\sqrt{2\beta I_{LOAD}}}\left(1 + \frac{R_{fb1}}{R_{fb2}}\right) \quad \text{(II.33)}$$

$$= -\frac{1}{A_V}\frac{1}{g_{m_P}}\left(1 + \frac{R_{fb1}}{R_{fb2}}\right) \quad \text{(II.34)}$$

Where g_{mP} is the incremental transconductance of the pass transistor.

These expressions for line and load regulation coincide with those obtained in the AC analysis, equations (II.6) and (II.12) respectively. It is worth noting that, likewise, LDR is also associated with the incremental output resistance that the regulator presents.

III.III. REFERENCES

1. Gray, P.R., Hurst, P.J., Lewis, S.H. and Meyer, R.G. Analysis and Design of Analog Integrated Circuits. *John Wiley & Sons, Inc.*, 2010.

Appendix III
Analysis of the LDO Frequency Response

This appendix is dedicated to the frequency analysis of a LDO without compensation as previously reported in Chapter 2, determining its characteristic equation.

For convenience, the scheme of the system is shown again in Figure III.1a. First, the characteristic equation will be determined, showing that to obtain it, it will be enough to calculate the voltage gain V_{out}/V_{ref} of the circuit in Figure III.1b, result of opening the loop.

If A_V is considered as the voltage gain of the error amplifier and A_P the corresponding gain of the pass transistor, it can be set:

$$v_g = A_V(v_{fb} - v_{ref}) \tag{III.1}$$

$$v_{out} = A_P(v_{in} - v_g) \tag{III.2}$$

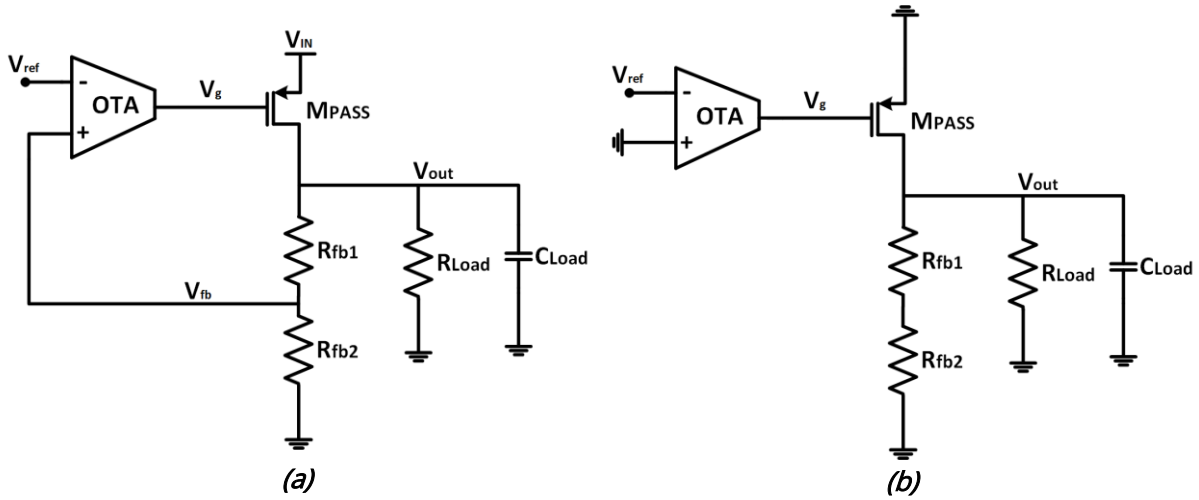


Figure III.1. Diagram of the LDO regulator with a) closed and b) open, loop configuration for frequency analysis.

$$v_{fb} = \alpha v_{out}, with\ \alpha = {R_{fb2}}/{(R_{fb1} + R_{fb2})} \quad \text{(III.3)}$$

In this way, $A_V(s=0)$ and $A_P(s=0)$ are positive magnitudes.

These equations correspond with the block diagram that is represented in Figure III.2.

Accordingly

$$v_{out} = A_P v_{in} - A_P A_V (v_{fb} - v_{ref}) = A_P v_{in} - A_P A_V (\alpha v_{out} - v_{ref}) \quad \text{(III.4)}$$

$$v_{out}(1 - A_P A_V \alpha) = A_P v_{in} + A_P A_V v_{ref} \quad \text{(III.5)}$$

Thus

$$v_{out} = \frac{A_P v_{in} + A_P A_V v_{ref}}{1 + A_P A_V \alpha} \quad \text{(III.6)}$$

Expression that shows that the characteristic equation of a low dropout is:

$$1 + A_P A_V \alpha = 0 \quad \text{(III.7)}$$

To obtain it, and since $\alpha = R_{fb2}/(R_{fb1}+R_{fb2})$, it will suffice to calculate $A_P A_V$, which corresponds to the voltage gain V_{out}/V_{ref} of the circuit in Figure III.1b.

Knowledge of this characteristic equation is essential to approach the study of the stability of the LDO, its compensation as well as its frequency response.

Once the opening of the loop has been justified, the position of the poles with this configuration is studied.

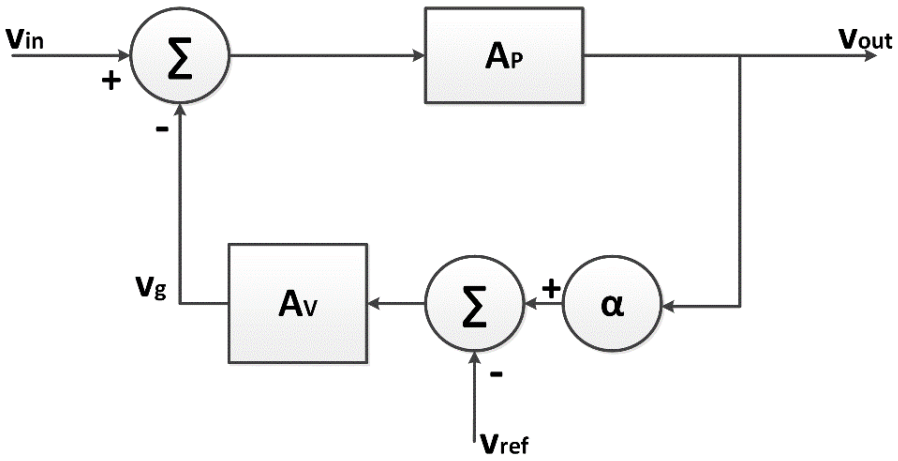


Figure III.2. Block diagram of the LDO regulator.

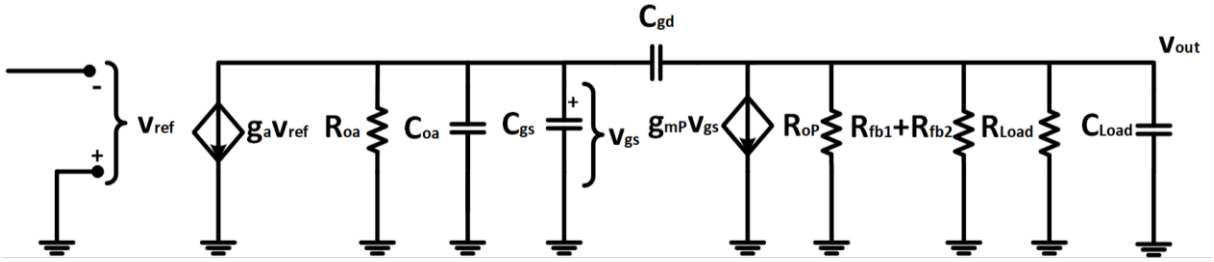


Figure III.3. Small-signal model of the open-loop configuration.

If it is assumed that the OTA is a single stage OTA, the equivalent model of the open-loop scheme, Figure III.1b, in the high-frequency range is the one shown in Figure III.3.

In this scheme, g_a is the transconductance of the error amplifier, while R_{oa} and C_{oa} characterize its output impedance. On the other hand, the set of parameters g_{mP}, R_{oP}, C_{gs} and C_{gd} characterize the incremental model of the step transistor.

If designated by $A_{P0}=A_P(s=0)=g_{mP}\{(R_{fb1}+R_{fb2})||R_{oP}||R_{Load}\}=g_{mP}R_{eq}$, and Miller's theorem is applied, the circuit above can be reduced to the one presented in Figure III.4 [1].

In this representation, $C_T=C_{gs}+C_{gd}(1+A_{P0})$.

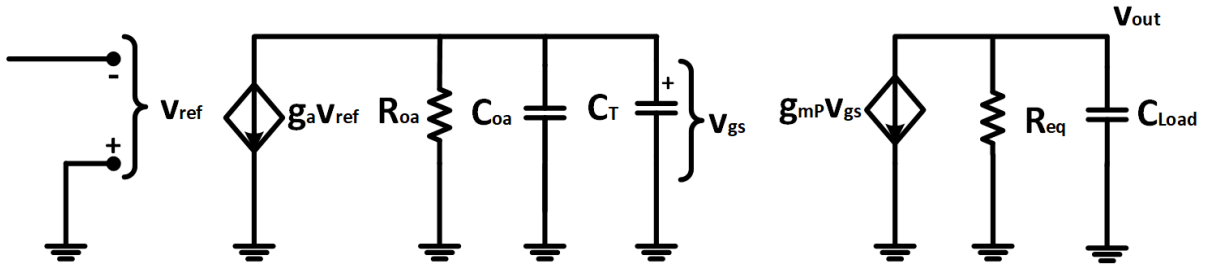


Figure III.4. Simplified circuit applying Miller's theorem.

The transfer function of the error amplifier can be easily determined, which allows to specify $A_V(s)$ as:

$$A_V(s) = \frac{g_a R_{oa}}{\left(1 + s/\omega_{p_{EA}}\right)} = -\frac{v_{gs}}{v_{ref}} \tag{III.8}$$

Thus, the system presents a dominant pole being its module:

$$\omega_{P_{EA}} = \frac{1}{R_{oa}(C_{oa} + C_T)} \tag{III.9}$$

Similarly, the pass transistor can be characterized by its voltage gain, whereby $A_P(s)$ is:

$$A_P(s) = \frac{g_{m_p} R_{eq}}{\left(1 + s/\omega_{P_{OUT}}\right)} = -\frac{v_{out}}{vgs} \tag{III.10}$$

where

$$\omega_{P_{OUT}} = \frac{1}{R_{eq} C_{Load}} \tag{III.11}$$

So, the open-loop transfer function will be

$$A_V(s) * A_P(s) = \frac{g_a R_{oa}}{\left(1 + s/\omega_{p_{EA}}\right)} * \frac{g_{m_p} R_{eq}}{\left(1 + s/\omega_{P_{OUT}}\right)} \quad \text{(III.12)}$$

where

$$\omega_{P_{OUT}} = \frac{1}{R_{eq} C_{Load}} \approx \frac{1}{R_{Load} C_{Load}} = \frac{I_{Load}}{V_{out} C_{Load}} \quad \text{(III.13)}$$

With $R_{eq}=(R_{fb1}+R_{fb2})//R_{oP}//R_{Load}$, and

$$\omega_{P_{EA}} = \frac{1}{R_{oa}\{C_{oa} + C_{gs} + C_{gd}(1 + A_{P_0})\}} \quad \text{(III.14)}$$

To design a fully integrated LDO, the compensation network must be made up of a capacitor C connected between the drain-gate terminals of the pass transistor. It will be in parallel with C_{gd}, converting the ω_{PEA} pole in the dominant pole [1].

$$\omega'_{P_{EA}} = \frac{1}{R_{oa}\{C_{oa} + C_{gs} + (C_{gd} + C)(1 + A_{P_0})\}} \quad \text{(III.15)}$$

IV.I. REFERENCES

1. Gray, P.R., Hurst, P.J., Lewis, S.H. and Meyer, R.G. Analysis and Design of Analog Integrated Circuits. *John Wiley & Sons, Inc.*, 2010.

Appendix IV
VGA Cherry-Hooper

In this appendix, the design and post-layout characterization of a Variable Gain Amplifier designed in a 0.18 µm CMOS process from TSMC is presented. Key design parameters are adjustable 40 dB gain with minimum power and area consumption, and a constant bandwidth above 100 kHz.

The purpose of this VGA is to achieve a structure with constant bandwidth and a high grade of programmability over the gain. To that end, two tuning techniques are introduced to provide a thick–fine gain tuning approximation.

IV.I. TSMC 0.18-µM CMOS TECHNOLOGY

TSMC 0.18 µm is a technology with 6 metal layers. Highly suited for MS/RF applications for todays IoT and smart wearable innovations.

IV.I.I. Technology characteristics

Shrink technology: NO
Core voltage: 1.8 V
I/O voltage: 3.3 V
Shallow Trench Isolation (STI)
Triple well (retrograde NW, PW and optional DNW)
Substrate resistivity: 8~12 ohm.cm on <100> P-substrate
Standard *Vt*, Medium *Vt* NMOS and medium *Vt* PMOS, native NMOS
HRI poly resistors
Temperature range: -40 ºC to 125 ºC
Number of metals: 3 to 6
Top metal 8kA, 20kA or 40kA
Inductors
MoM
MiM 1 fF/µm^2 of 2 fF/µm^2, mutual exclusive
Passivation single

IV.I.II. Device parameters

Capacitor

MIMCAP_2P0_SIN	(4µm/4µm)	35.6 fF

Resistor

RPHRIPOLY	(1µm/2µm)	15.9957 kΩ

Table IV.1. Main technological parameters for transistors in TSMC 180nm.

Transistor	PMOS_2v	NMOS_2v
L_{min} (µm)	0.18	0.18
L_{max} (µm)	19.95	19.95
W_{min} (µm)	0.22	0.22
W_{max} (µm)	900	900
V_{Th} (V)	-0.412	0.355

IV.II. DESIGN

The structure relies on a TC-TI approach, shown in Figure IV.1, based on the topology presented in [1], with two tuning techniques to give programmability to the gain.

The general structure has a transconductance input differential pair degenerated by a linear resistance generating the linear signal current, I_{in}. This current is conveyed to the transimpedance stage by two tuning techniques a current steering [2] and a current division [3]. Finally, a feedback compensation network is used to keep the system stable over all its operating conditions.

A block-diagram view of the proposed structure is shown in Figure IV.2, where two identical second-generation current conveyors (CCIIs) [4] are used in a differential arrangement together with two passive resistors R in series to degenerate the input for the TC stage. The TI stage is made of two single-ended class-AB transresistance amplifiers with a compensation feedback loop to stabilise the system. The current tuning techniques, current steering and current division, are applied in between stages.

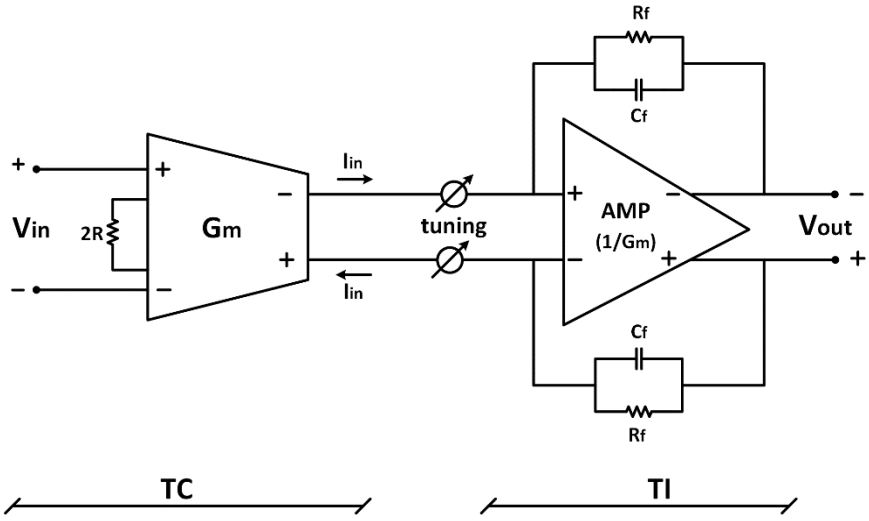


Figure IV.1. Variable Gain Amplifier proposal.

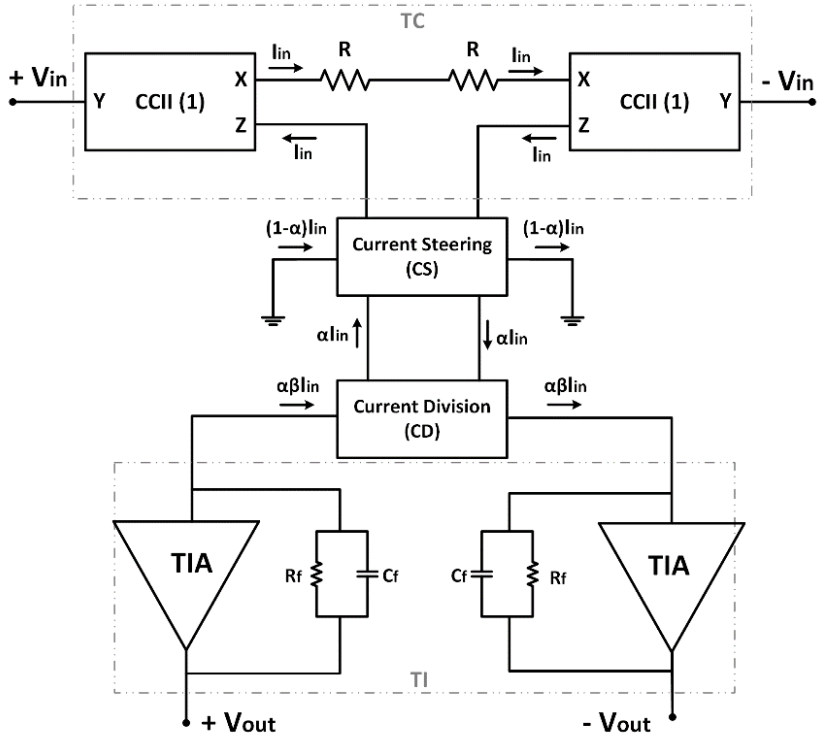


Figure IV.2. Block diagram of the VGA proposal.

Figure IV.3 shows the implementation of the CCII based on a class-AB voltage follower whose output current is conveyed to a high-impedance output node by replicating the output branch of the follower. The CCIIs of the TC-stage transfer the differential input voltage applied to the high-impedance input terminals Y at terminals X to the passive resistors R, where V-I conversion is yield. Then, the current at terminals X is conveyed to the high impedance output terminals Z.

The class-AB operation is achieved by adding a floating capacitor C_{bat} and a large resistance R_{large} as shown in Figure IV.3, transforming transistor M_P -the transistor whose gate is the common terminal between R_{large} and C_{bat}– into a QFG transistor [5]. When a positive input voltage is applied to terminal Y, the capacitor acts as a floating battery

allowing the circuit to operate in class AB having high current driving capability and, at the same time, very low quiescent power consumption.

The complete schematic of the proposed topology is shown in Figure IV.4. The degenerated differential pair uses super source follower input transistors, which act as voltage buffers. Thus, V_{in} is driven to the R terminals, generating the linear signal current $I_{in}= (V_{in+}-V_{in-})/R$ conveyed to the output stage through high-swing current mirrors that incorporate the first tuning technique, cascode current steering. This current steering is the same technique introduced in Chapter 3. The PMOS transistors M_1 are split into two identical transistors driven by complementary control voltages $V_{\pm} = V_C \pm V_{gc}$ [6], resulting in two output branches conveying complementary currents. As transistors M_P present the same drain to source voltage and gate to source voltage, the current mirror renders unity gain current. The current I_{M1} is split into two complementary currents, whose fractional value α_i $(0 \leq \alpha_i \leq 1)$ depends upon the differential control voltage V_{gc}. In this way, the overall transconductor output current can be controlled through the cascode gate voltage, so $G_m (TC) = \alpha_i/R$.

Between both TC and TI stages, a current division made of three PMOS transistors in a 1:2:1 configuration modifies the current introduced to the transimpedance stage. This transistors work as a resistive divider, controlling through the gate voltages the current flowing to the TIA. Being the current flowing thorugh expressed as $\beta(\alpha I_{in})$, where $\beta=1/(1+R_{MT1}/R_{MT2})$.

Finally, in the compensation loop of the TI-stage resistance R_f yields the output voltage, being the overall gain given by $A_V=\alpha\beta R_f/R$, with α the fractional value dependent on V_{gc} and β the fractional value dependent on tune1, while C_f is used for compensation. Both R and R_f are linear passive elements, to optimize linearity and insensibilize the gain to PVT variations.

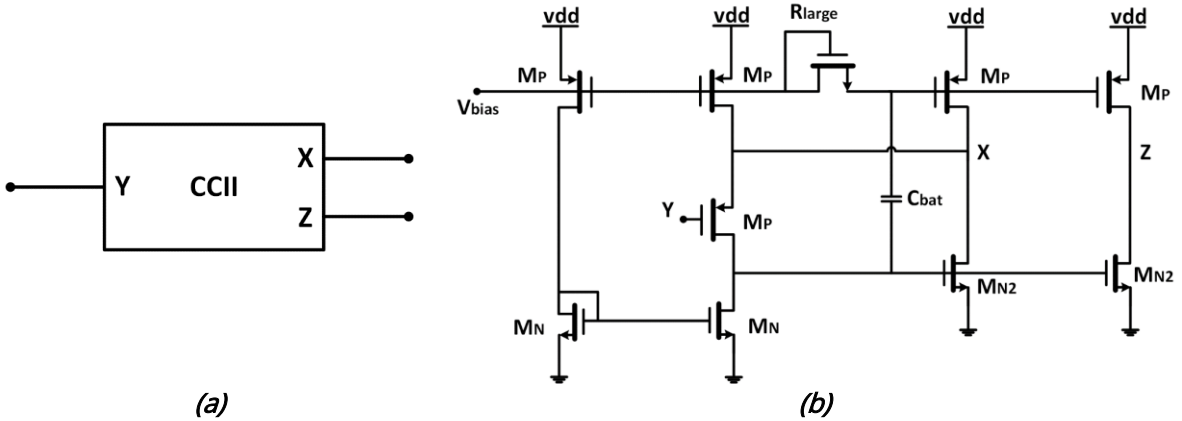


Figure IV.3. CCII a) Block diagram; and b) schematic view.

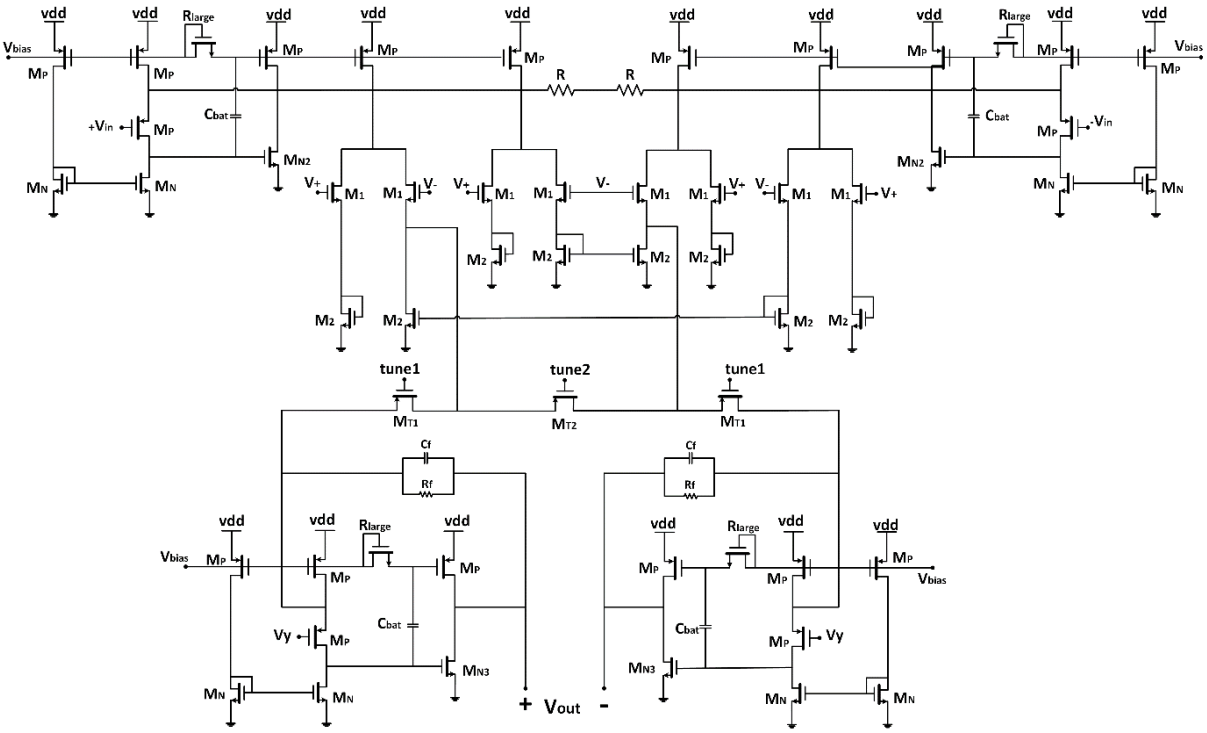


Figure IV.4. Schematic view of the proposed VGA.

The gain tuning is done in a two-step process, where firstly the Current Division (CD) is used as a thick tuning, with $tune_2$ = 330 mV and $tune_1$ ranges from 0 V to 420 mV. Then, in the second step, the Current Steering (CS) is used as a fine tuning, were V_{gc} that ranges from 0 V to 150 mV (with V_C = 1.1 V) is adjusted.

These ranges are previously determined from a calibration. The value of $tune_2$ is determined by sweeping over $tune_1$ and choosing that which keep the bandwidth as constant as possible over $tune_1$, for the maximum range possible. While the range of $tune_1$ is limited by the variation in the bandwidth. In Figure IV.5 we show this calibration, it can be seen that it is for $tune_2$ = 330 mV when the bandwidth is the most constant over all $tune_1$.

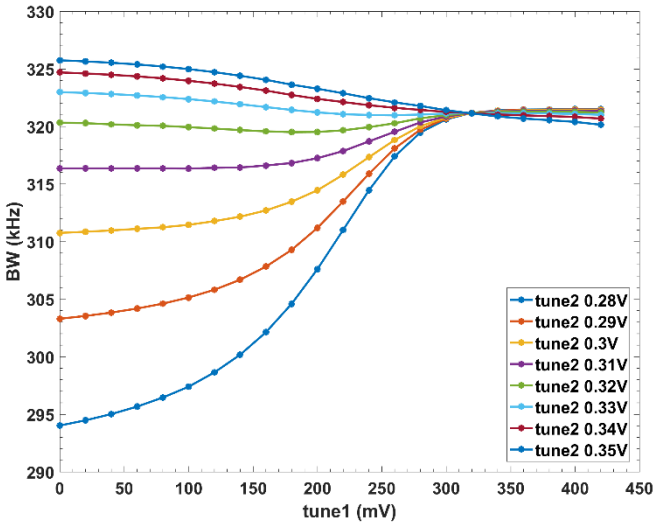


Figure IV.5. Calibration of $tune_2$ (BW vs $tune_1$ for diferent $tune_2$ curves with v_{gc}=0 V).

While the current steering calibration is done by varying V_{gc} while keeping $tune_1$ and $tune_2$ fixed to 0 V -can be to any value within the $tune_1$ range- and 0.33 V respectively. As can be appreciated in Figure IV.6, as V_{gc} is increased, the gain increases but the gain variation is smaller with as we increase V_{gc}, being the difference negligible for values bigger than 0.15 V, thus the V_{gc} ranges from 0 V up to 0.15 V.

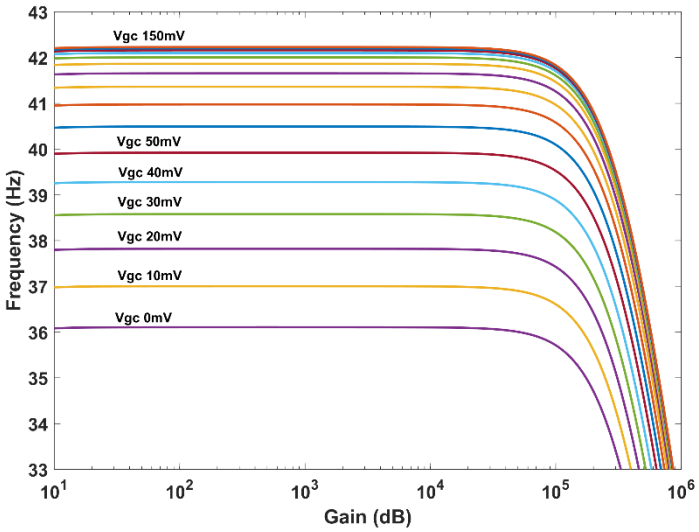


Figure IV.6. Calibration of V_{gc}. (Gain vs V_{gc} for $tune_1$ and $tune_2$ fixed to 0 V and 0.33 V respectively).

This VGA has been designed in the 0.18 µm CMOS technology from TSMC, with a 1.8 V voltage supply and a bias current of 0.5 µA using a class-AB topology (achieved through a quasi-floating C_{bat} - R_{large} gate) to optimize power. Transistor sizes in µm/µm are M_1=1/1, M_2=2.5/4, M_P=2/1, M_N=1/4, M_{N2}=2/4, M_{N3}=2.5/4, M_{T1}=200/1, M_{T2}=400/1 and M_{Rlarge}=0.22/0.18. Other components sizes are C_{bat}=2 pF, R=1 kΩ, R_{fb}=200 kΩ, C_{fb}=250 fF and C_{load}=1 pF. Total power consumption is 15.5 µW with a total active area of 149 x 207 µm^2, as shown in the layout view in Figure IV.7.

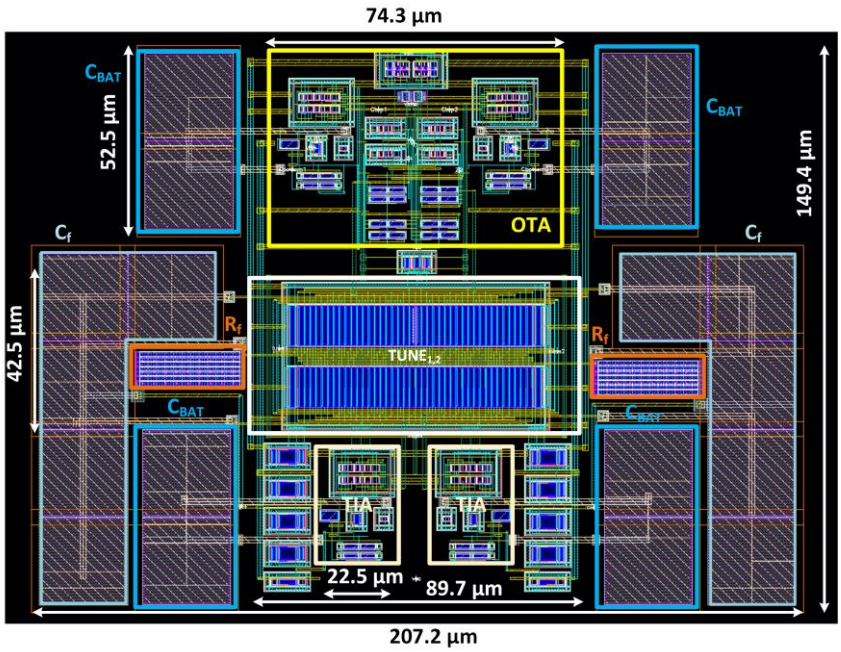


Figure IV.7. Layout view of the complete VGA structure. Size: 149x207 µm^2.

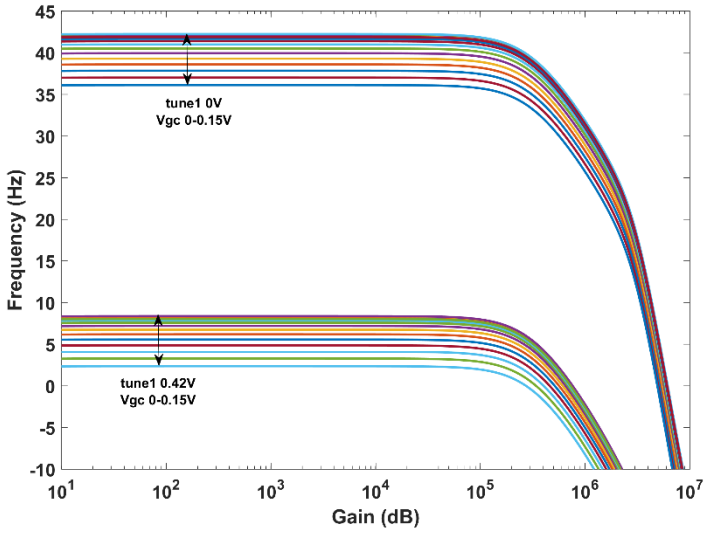
IV.III. CHARACTERIZATION

In this section, the post-layout characterization of the Variable Gain Amplifier designed above will be presented. The same structure as in the characterization of the previous reported VGA in Chapter 3 will be followed.

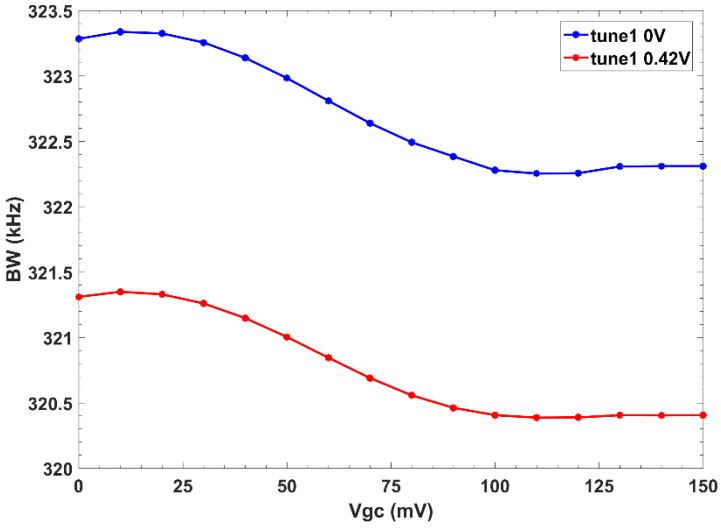
IV.III.I. Gain and bandwidth

First, the adjustable gain is validated by sweeping over V_{gc} and $tune_1$. Figure IV.8a shows the frequency response with the variation of gain from 2.35 dB (max $tune_1$, min V_{gc}) to 42.2 dB (min $tune_1$, max V_{gc}), with an almost constant bandwidth higher than 320 kHz.

Figure IV.8b shows the bandwidth variation over V_{gc} for the extreme values of $tune_1$. As can be seen there is a maximum of 1 kHz bandwidth variation over V_{gc} and a maximum 2 kHz variation over the $tune_1$ range.



(a)



(b)

Figure IV.8. a) Gain vs frequency, and b) BW deviation at room temperature for different gain values.

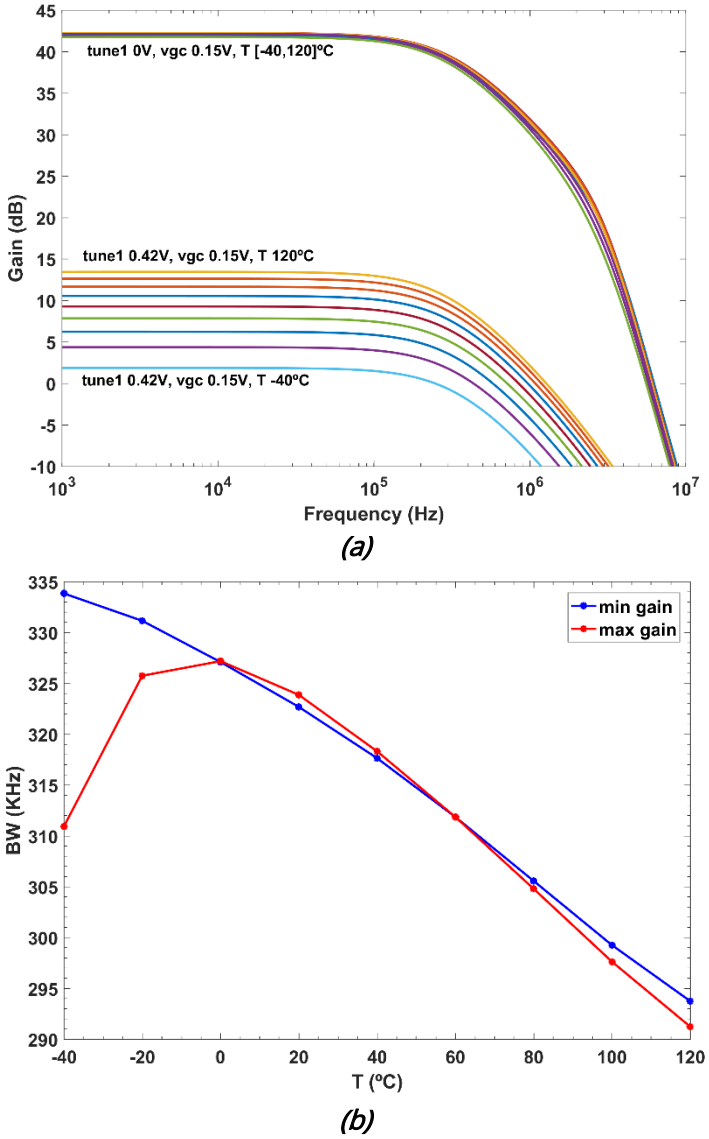


Figure IV.9. a) Gain and b) bandwidth deviation for different temperatures.

To analyse its behaviour against temperature variations, Figure IV.9 shows the gain and bandwidth deviation over temperature for maximum and minimum gain conditions. For maximum gain, the variation over temperature is almost constant, with a 1.76 mdB/ºC, and it is for minimum gain conditions where the gain variation is of 80 mdB/ºC. The bandwidth has a total variation of 225 Hz/ºC and 251 Hz/ºC for maximum and minimum gain conditions respectively.

IV.III.II. Linearity

The Total Harmonic Distortion (THD) as a function of the input amplitude is shown in Figure IV.10. A sinusoidal signal of frequency $f_{in}=f_{c,BW}/5$ with variable amplitude is used.

The THD for the VGA operating at maximum gain, 42.2 dB, is kept below -40 dB for output amplitudes up to 1.585 V_{pp} (in, 12.30 mV_{pp}). While for an output amplitude of 12.91 mV_{pp} (in, 100 μV_{pp}) reports a THD of -45.7 dB, and for an output amplitude of 129.1 mV_{pp} (in, 1 mV_{pp}) the reported THD is -46.6 dB.

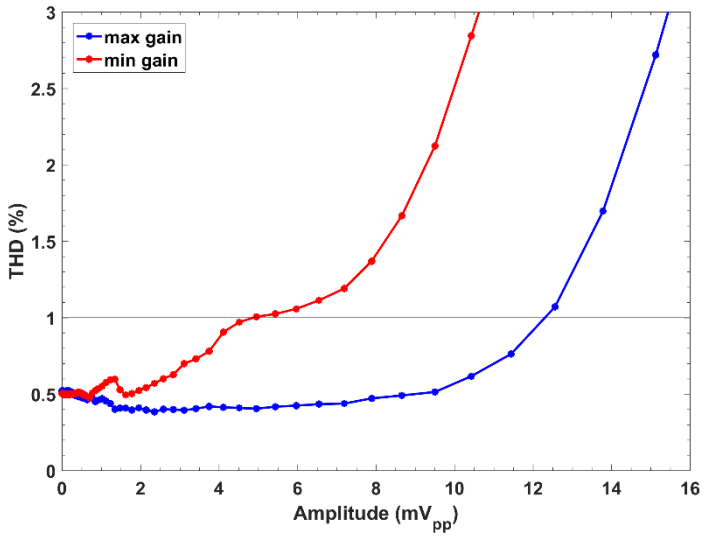


Figure IV.10. THD as a function of the input amplitude with maximum and minimum gain.

For minimum gain, 2.35 dB, THD is maintained below -40 dB for output amplitudes up to 6.39 mV_{pp} (in, 4.88 mV_{pp}). While for an output amplitude of 131.07 μV_{pp} (in, 100 μV_{pp}) reports a THD of -46.1 dB, and for an output amplitude of 1.31 mV_{pp} (in, 1 mV_{pp}) the reported THD is -45.2 dB.

IV.III.III. Noise

The equivalent rms noise (from 10 mHz to 350 kHz) referred to the output is 10.1 mV_{rms} (max gain) and 365.8 μV_{rms} (min gain). Therefore, referred to the input the noise is 78.4 μV_{rms} (max gain) and 279.1 μV_{rms} (min gain) and in V/√Hz the noise is 132.5 nV/√Hz (max gain) and 471.7 nV/√Hz (min gain).

IV.IV Comparison with Other Works

The presented Variable Gain Amplifier designed in a 0.18 µm CMOS technology from TSMC, presents a total current consumption of 8.6 µA including the 0.5 µA bias current and the current required to generate the bias voltages. A power supply of 1.8 V is employed, thus the total power consumption is 15.5 µW. It achieves a total gain variation ~40 dB with a constant BW above 320 kHz and an active area of 0.021 mm^2.

To compare the proposed structure, we will use the same FoMs proposed in Section 3.1.3 to compare the amplifiers. To ease the reading, we define them again.

FoM_1 is defined as:

$$FoM_1 = 20\log_{10}\left(\frac{linearity(V_{out,pp})/(THD(\%)/100)}{noise(V/\sqrt{Hz})}\right) \quad \text{(IV.1)}$$

FoM_2 is defined as:

$$FoM_2 = \frac{Gain(\mathrm{V/V}) * Freq.range(MHz)}{Power(\mu W)} \quad \text{(IV.2)}$$

Table IV. shows a comparison with previously reported works. Overall, this proposal presents a better tradeoff in terms of the power-area consumption and the gain and bandwidth performance as can be seen from the FoM results.

Table IV.2. Performance comparison with previously reported works.

Parameter	This work	VGA (Section 3.1.2)	[7]' 04	[8]' 09	[1]' 13	[9]' 20
Results	Post-lay	Post-lay.	Exp.	Exp.	Exp.	Post-lay
Tech. (µm) @ Supply (V)	0.18 @ 1.8	0.18 @ 1.8	0.18 @ 1.8	0.35 @ 2.5	0.5 @ 3.3	0.065 @ ±0.6
Power (µW)	15.5	180.4	1800	11250	500	0.12
T range (°C)	-40 – 120	-40 – 120	N/A	N/A	N/A	N/A
Gain (dB)	2.35 – 42.2	6 – 26.1	0 – 16	0 – 60	5 – 20	5-30
Freq. range (Hz)	320k	100M	3.84M	2.87M	1.4M	300
Linearity ($V_{in,pp}$) @ THD (dB)	4.9m – 12.3m @ - 40	0.35 – 0.56 @ - 40	N/A	N/A	N/A	N/A
noise (nV/√Hz)	472 – 133	53.7 – 8.04	4 dB	5.2 dB	0.003	N/A
Area (mm^2)	0.021	0.0062	N/A	2.55	0.25	N/A
FoM_1 (dB)	120.3 – 139.3	176.3-196.9	N/A	N/A	N/A	N/A
FoM_2 (MHz/µW)	0.027 – 2.66	1.11 – 11.2	2.13m - 0.013	255µ - 0.255	4.98m - 2.8m	4.45m - 0.08

N/A Not Available.

IV.V REFERENCES

1. Garcia-Alberdi, C., Aguado-Ruiz, J., Lopez-Martin, A.J. and Ramirez-Angulo, J. Micropower Class-AB VGA With Gain-Independent Bandwidth. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2013.
2. Pérez-Bailón, J., Márquez, A., Calvo, B. and Medrano, N. A 0.18µm CMOS Widely Tunable Low Pass Filter with sub-Hz Cutoff Frequencies. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018.
3. Acosta, L., Jimenez, M., Carvajal, R.G., Lopez-Martin, A.J. and Ramirez-Angulo, J. Highly Linear Tunable CMOS Gm-C Low-Pass Filter. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2009.
4. Sedra, A. and Smith, K. A second-generation current conveyor and its applications. *IEEE Transactions on Circuit Theory*, 1970.
5. Ramirez-Angulo, J., Lopez-Martin, A.J., Carvajal, R.G. and Muñoz-Chavero, F. Very low voltage analog signal processing based on quasi floating gate transistors. *IEEE Journal of Solid State Circuits*, 2004.
6. Ramirez-Angulo, J., Garimella, S.R.S., Lopez-Martin, A.J. and Carvajal, R.G. New Gain Programmable Current Mirrors Based on Current Steering. *IEEE International Midwest Symposium on Circuits and Systems*, San Juan, USA, 2006.
7. Gatta, F., Manstretta, D., Rossi, P. and Svelto, F. A fully integrated 0.18-µm CMOS direct conversion receiver front-end with on-chip LO for UMTS. *IEEE Journal of Solid-State Circuits*, 2004.
8. Zheng, Y., Yan, J. and Xu, Y.P. A CMOS VGA With DC Offset Cancellation for Direct-Conversion Receivers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2009.
9. Ghorbani, A.R. and Ghaznavi-Ghoushchi, M.B. An Ultra-Low Power Programmable Current Gain Amplifier with a Novel Current Gain Controller Structure for IoT Applications. *Wireless Personal Communications*, 2020.

Conclusiones

En esta tesis, nos hemos centrado en profundizar en el diseño de un sistema de procesamiento de baja potencia, operado por batería y verdaderamente portátil para la medición de espectroscopía de impedancia, basado en tecnologías microelectrónicas CMOS, contribuyendo a la creación de la próxima generación de dispositivos Lab-on-Chip. Los resultados presentados demuestran que los front-end IS basados en FRA de banda ancha tienen el potencial de integrarse en procesos CMOS con un bajo nivel tensión y de consumo en potencia, mostrando rendimientos muy prometedores en comparación con las soluciones del estado del arte.

A continuación, se destacan las contribuciones más relevantes de este trabajo.

En el Capítulo 1, se realiza una breve introducción al estado actual del arte de la espectroscopía de impedancia, de donde se deriva la motivación y objetivos de este trabajo.

En el Capítulo 2, se considera el diseño de la unidad de administración de energía basada en reguladores de baja caída de tensión totalmente integrados. Se ha presentado un regulador CMOS LDO de 0,18 µm completamente integrado que proporciona un suministro nominal regulado de 1,8 V con compensación interna y un circuito de refuerzo de polarización de corriente dinámica para mejorar el comportamiento transitorio. La caracterización experimental valida el cumplimiento de las especificaciones de diseño marcadas como objetivo, obteniendo un regulador LDO compatible con sistemas portátiles operados por baterías, logrando una mejor regulación general de línea (0,081 mV/V) y carga (-0,82 mV/mA) con una reducción del consumo de energía (13,41 µW) mientras mantienen parámetros de respuesta de tiempo similares (<2,5 µs para el tiempo de estabilización a plena carga) en comparación con otros trabajos presentes en la literatura.

En el Capítulo 3, se han presentado los diferentes componentes básicos -etapa amplificadora, etapa multiplicadora y etapa de filtrado de salida- que constituyen la etapa de front-end analógico para un sistema de medida de espectroscopía de impedancia.

Para la etapa de entrada, se presentan dos amplificadores de banda ancha basados en un enfoque TC-TI: el preamplificador frontal tiene entradas en modo de voltaje y corriente, una ganancia fija (26 dB/89 dBΩ) y un consumo mínimo de potencia y área (180,4 µW, 0,0115 mm^2); el segundo exhibe una ganancia programable de 4 bits (6-26 dB), nuevamente con un consumo mínimo de energía y área (180,4 µW, 0,0062 mm^2). El mezclador se ha integrado dentro de la etapa de salida TI de este último amplificador de ganancia variable, logrando una estructura verdaderamente compacta.

Finalmente, se han diseñado y caracterizado dos Filtros Pasa Baja (LPF) totalmente integrados basados en una estructura G_m-C que hace uso de una técnica de redirección de corrientes con un ajuste y reducción de la G_m que opera con una fuente de

alimentación de 1,8 V. Tanto el LPF de primer orden como el de segundo orden presentan un rango de frecuencia de corte de cinco órdenes de magnitud, desde sub-Hz hasta kHz, con un bajo consumo de energía (5,4 µW el O1F y 9,9 µW el O2F), tamaño reducido y un alto rango dinámico (>70 dB).

Finalmente, en el Capítulo 4, se presentan dos etapas front-end de lectura FRA-IS completos de fase dual y banda ancha (~100 MHz), basados en las celdas presentadas anteriormente, capaces de recuperar simultáneamente dos valores de voltaje de DC que son proporcionales a las componentes real e imaginaria de la impedancia bajo prueba, Z.

El primero combina las diferentes etapas presentadas en el Capítulo 3: un preamplificador TC-TI (26 dB/89 dBΩ) con entrada de voltaje y corriente, seguido de un TC-TI VGA (6-26 dB) adaptado para operación de fase dual replicando solo la etapa del mezclador TI de salida y una etapa de salida de filtrado, con frecuencia de corte sintonizable de sub-Hz a kHz, para recuperar las magnitudes de impedancia.

El segundo es una versión simplificada compacta, basada en un solo amplificador sintonizable de ganancia TC-dual TI 0-40 dB, que reduce el área (0,0569 mm^2) y el consumo de energía (291,6 µW) a costa de cambiar el ancho de banda (87 MHz).

Ambos han sido validados recuperando una impedancia Z compuesta por una resistencia R = 500 Ω en paralelo con un condensador C = 500 nF, proporcionando resultados de recuperación similares.

Finalmente, el autor también ha prestado especial atención al control automatizado de instrumentación y adquisición de datos, desarrollando sistemas de caracterización específicos para los diferentes prototipos integrados, diseñando las PCB correspondientes y los diferentes códigos necesarios para llevar a cabo la automatización.

Publication List

Publications in Scientific Journals

1. **Pérez-Bailón, J.**, Sanz-Pascual, M.T., Calvo, B. and Medrano, N. Wide-band compact 1.8 V-0.18 µm CMOS Analog Front-end for Impedance Spectroscopy. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**. **(early access)**
2. **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. 1.0 V-0.18 µm CMOS Tunable Low Pass Filters with 73 dB DR for On-Chip Sensing Acquisition Systems. *Electronics*, **2021**.
3. **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. A Fully-Integrated 180 nm CMOS 1.2 V Low-Dropout Regulator for Low-Power Portable Applications. *Electronics*, **2021**.
4. **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. A CMOS Low Pass Filter for SoC Lock-in-Based Measurement Devices. *Sensors*, **2019**.
5. **Pérez-Bailón, J.**, Márquez, A., Calvo, B. and Medrano, N. A 0.18 µm CMOS LDO Regulator for an On-Chip Sensor Array Impedance Measurement System. *Sensors*, **2018**.
6. Márquez, A., **Pérez-Bailón, J.**, Calvo, B., Medrano, N. and Martínez, P.A. A CMOS Self-Contained Quadrature Signal Generator for SoC Impedance Spectroscopy. *Sensors*, **2018**.
7. **Pérez-Bailón, J.**, Márquez, A., Calvo, B., Medrano, N. and Martínez, P.A. A fast-transient high-performance 0.18 µm CMOS LDO for battery-powered systems. *Electronics Letters*, **2017**.

Publications in International Conferences

1. **Pérez-Bailón, J.**, Calvo, B., Medrano, N. and Ramírez-Angulo, J. A 1.8 V Gm-C Highly Tunable Low Pass Filter for Sensing Applications. *International Instrumentation and Measurement Technology Conference* (*I2MTC*). Dubrovnik, Croacia. **2020**.
2. Márquez, A., Medrano, N., Calvo, B. and **Pérez-Bailón, J.** A Dual Synchronous Demodulator for Phase Sensitive Detection Applications. *International Instrumentation and Measurement Technology Conference* (*I2MTC*). Dubrovnik, Croacia. **2020**.
3. Maya-Hernández, P., Calvo, B., Sanz-Ruiz, M.T., Medrano, N. and **Pérez-Bailón, J.** A CMOS Lock-In-based Read-Out for Interdigitated Electrodes. *International Instrumentation and Measurement Technology Conference* (*I2MTC*). Dubrovnik, Croacia. **2020**.
4. Enériz, D., Medrano, N., Calvo, B. and **Pérez-Bailón, J.** A Wireless Instrumentation Control System Based on Low-Cost Single Board Computers. *International Instrumentation and Measurement Technology Conference* (*I2MTC*). Dubrovnik, Croacia. **2020**.

5. **Pérez-Bailón, J.**, Márquez, A., Calvo, B., Medrano, N. and Sanz-Pascual, M.T. A 1V-1.75µW Gm-C Low Pass Filter for Bio-sensing Applications. *9th Latin American Symposium on Circuits and Systems (LASCAS)*. Puerto Vallarta, México, **2018.**
6. **Pérez-Bailón, J.**, Márquez, A., Calvo, B. and Medrano, N. A 0.18µm CMOS Widely Tunable Low Pass Filter with Sub-Hz Cutoff Frequencies. *International Symposium on Circuits And Systems (ISCAS)*. Florencia, Italia. **2018**.
7. Márquez, A., **Pérez-Bailón, J.**, Martínez, P.A., Calvo, B. and Medrano, N. A CMOS low-power widely frequency tunable pre-conditioning stage for PSD sensor applications. *IEEE Sensors*. Glasgow, Reino Unido, **2017**.
8. **Pérez-Bailón, J.**, Márquez, A., Calvo, B. and Medrano, N. An All-MOS Low-Power Fast-Transient 1.2 V LDO Regulator. *Ph.D. Research in Microelectronics and Electronics (PRIME)*. Giardini Naxos, Italia, **2017**.
9. **Pérez-Bailón, J.**, Márquez, A., Calvo, B. and Medrano, N. Transient-enhanced Output-Capacitorless CMOS LDO Regulator for Battery-operated Systems. *International Symposium on Circuits And Systems (ISCAS)*. Baltimore, USA. **2017**.
10. Márquez, A., **Pérez-Bailón, J.**, Martínez, P.A., Calvo, B. and Medrano, N. A CMOS Low-Power 12-bit Digitally Programmable Analog Sinusoidal Actuation System. *International Instrumentation and Measurement Technology Conference* (*I2MTC*). Turín, Italia. **2017**.
11. **Pérez-Bailón, J.**, Márquez, A., Calvo, B. and Medrano, N. A Power Efficient LDO Regulator for Portable CMOS SoC Measurement Systems. *International Instrumentation and Measurement Technology Conference* (*I2MTC*). Turín, Italia. **2017**.
12. Martínez-Nieto, A., Sanz, M.T., Márquez, A., **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. A CMOS Mixed Mode Non-Linear Processing Unit for Adaptive Sensor Conditioning in Portable Smart Systems. *30th Eurosensors Conference*, Budapest, Hungría, **2016**.
13. **Pérez-Bailón, J.**, Márquez, A., Calvo, B.; Medrano, N. and Martínez, P.A. A Fully-integrated CMOS LDO regulator for battery-operated on-chip measurement system*s*. *30th Eurosensors Conference*, Budapest, Hungría, **2016**.

Publications in National Conferences

1. **Pérez-Bailón, J.**, Ramírez-Angulo, J. Calvo, B. and Medrano, N. A Fully Differential Variable Gain Amplifier for Portable Impedance Sensing Applications. *VIII Jornadas Jóvenes Investigadores I3A*, Zaragoza, España, **2019**.
2. **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. A Low Pass Filter With sub-Hz Cutoff Frequencies for a Portable On-Chip Lock-in Microinstrument. *VII Jornadas Jóvenes Investigadores I3A*, Zaragoza, España, **2018**.
3. **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. A Low-quiescent Current Full on-chip 1.2 V CMOS Low

Drop-Out Regulator. *VI Jornadas Jóvenes Investigadores I3A*, Zaragoza, España, **2017**.

4. **Pérez-Bailón, J.**, Márquez, A., Calvo, B. and Medrano, N. Low Pass Filter With sub-Hz Cutoff Frequencies for Portable Read-out Sensor Systems. *XIV Reunión Ibernam*, Tordesillas, España, **2017**.
5. Márquez, A., **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. A CMOS Low-Power Tunable Band-Pass Filter for PSD Sensor Applications. *XIV Reunión Ibernam*, Tordesillas, España, **2017**.
6. **Pérez-Bailón, J.**, Calvo, B., Medrano, N. and Martínez, P.A. A 180nm CMOS Capacitorless Low Drop-Out Regulator for Battery-operated Systems. *V Jornadas Jóvenes Investigadores I3A*, Zaragoza, España, **2016**.
7. **Pérez-Bailón, J.**, Calvo, B. and Medrano, N. Diseño de un Regulador CMOS LDO Completamente Integrado para Sistemas Alimentados por Baterías. *VII Jornadas Jóvenes Investigadores Química y Física de Aragón*, Zaragoza, España, **2016**.