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Multi-Phase Power Factor Correction for Domestic Induction Heating

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MULTI-PHASE POWER FACTOR CORRECTION FOR DOMESTIC INDUCTION HEATING

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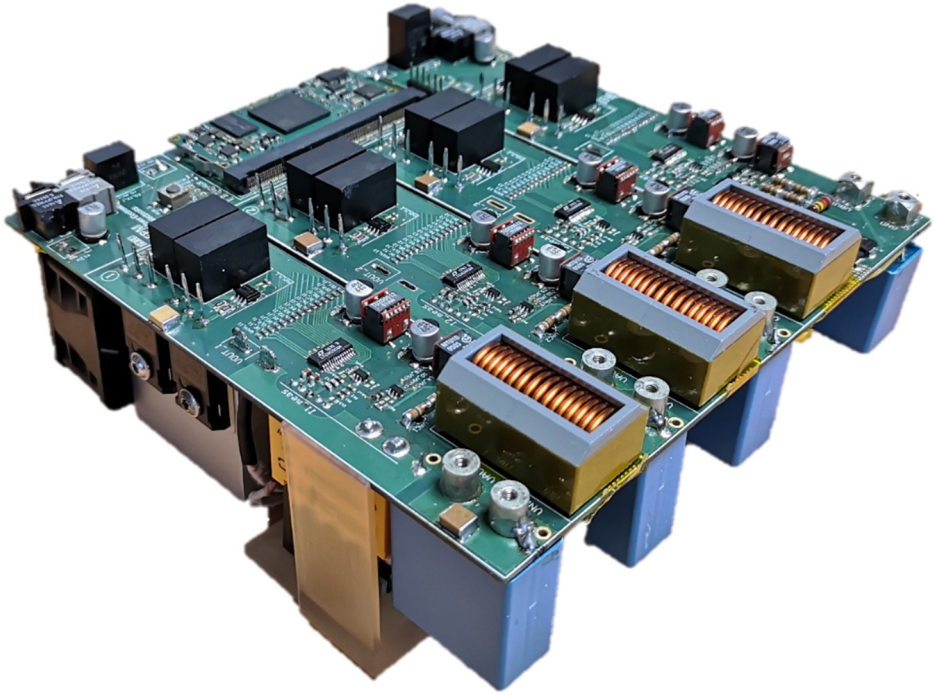
PhD Dissertation

MULTI-PHASE POWER FACTOR CORRECTION FOR DOMESTIC INDUCTION HEATING



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A mi familia

A Jeni

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Abstract

Induction heating (IH) is quickly evolving towards higher performance systems thanks to advances in enabling technologies such as power electronics, magnetic component design and digital control. In this context, domestic induction heating is progressing towards future applications with enhanced flexibility, higher output power and efficiency, and improved reliability and cost.

Considering this background, this dissertation explores the use of power factor corrector (PFC) rectifiers that provide significantly higher performance for future domestic IH systems. Nowadays, state-of-the-art of domestic IH technology relies on the use of a small dc-link capacitance with a high dc-link voltage ripple to avoid the use of PFC stages in cost-effective implementations. By contrast, this dissertation proposes the use of single/multi-phase PFC rectifiers to obtain substantial advantages such as the increased output power, lower voltage ripple and higher dc-link voltage leading to higher inverter efficiency, simplified multi-phase and multi-inductor systems, and improved EMC performance, among others.

The main contributions of this dissertation include an in-depth review of IH technology and PFC rectifier systems, the proposal of a single-phase and a multi-phase PFC rectification topologies for new domestic IH applications, and the proposal and analysis of a complete set of modulation strategies. Furthermore, in order to experimentally verify these proposals, a complete experimental test-bench has been designed and implemented including an ad-hoc three-phase high-performance power supply, a single-phase PFC rectifier topology, a multi-phase PFC rectifier topology, and an IH ZVS matrix multi-inverter. The obtained analytical and experimental results have been deeply analyzed according to the most relevant figures of merit, proving the feasibility of the proposed converter topologies and modulation strategies, and establishing the main selection and design criteria. As a conclusion of this dissertation, PFC rectifier systems are proposed as a promising technology for future high performance domestic IH systems.

This PhD dissertation has been developed within the collaboration agreement between the BSH Home Appliances Group (BSH) and the Group of Power Electronics and Microelectronics (GPEM) of the University of Zaragoza, Spain, in the framework of the BSH-UZ Innovation Chair.

Resumen

El calentamiento por inducción (IH) evoluciona rápidamente hacia sistemas de mayor rendimiento debido a los avances de la tecnología como la electrónica de potencia, el diseño de componentes magnéticos y el control digital. En este contexto, el calentamiento por inducción doméstico avanza hacia futuras aplicaciones con mayor flexibilidad, potencia, eficiencia y fiabilidad, manteniendo un coste contenido.

Teniendo en cuenta estos antecedentes, esta tesis explora el uso de rectificadores correctores del factor de potencia (PFC) ya que aportan mayores prestaciones a futuros sistemas IH domésticos. Actualmente, el estado del arte de la tecnología IH doméstica depende del uso de una pequeña capacidad de filtrado con un alto rizado de tensión para evitar el uso de etapas PFC y conseguir implementaciones rentables. Sin embargo, esta tesis propone el uso de rectificadores multifásicos o monofásicos para obtener ventajas adicionales, como una potencia de salida más elevada, mayor eficiencia debida a un bus de mayor tensión y bajo rizado, sistemas multifásicos y multi-inductores más simplificados, y una compatibilidad electromagnética (EMC) mejorada.

Las principales contribuciones de esta tesis incluyen una profunda revisión de la tecnología IH y de los sistemas rectificadores, la propuesta de una topología rectificadora PFC monofásica y una trifásica para nuevas aplicaciones IH domésticas, y la propuesta y análisis de un set completo de estrategias de modulación. Además, para verificar experimentalmente estas propuestas, se ha diseñado e implementado un banco de pruebas experimental completo, incluyendo una fuente de alimentación trifásica de alto rendimiento diseñada a medida, una topología rectificadora PFC monofásica, una topología PFC multifásica y un multi-inversor matricial ZVS para IH doméstico. Se han analizado profundamente los resultados analíticos y experimentales obtenidos según las figuras de mérito más relevantes, probando la factibilidad de las topologías conversoras propuestas y de las estrategias de modulación, y estableciendo los principales criterios de selección y diseño. Como conclusión de esta tesis, se proponen los sistemas rectificadores PFC como una tecnología prometedora para futuros sistemas IH domésticos de elevadas prestaciones.

Esta tesis ha sido desarrollada dentro del acuerdo de colaboración entre BSH Home Appliances Group (BSH) y el Group of Power Electronics and Microelectronics (GPEM) de la Universidad de Zaragoza, en el marco de la Cátedra de Innovación BSH-UZ.

List of acronyms

ADC	*Asymmetrical duty cycle*
ASD	*Adjustable-speed driver*
ASIC	*Application specific integrated circuit*
AVC	*Asymmetrical voltage cancelation*
BSH	*BSH Home Appliances Group*
CCM	*Continuous conduction mode*
CSI	*Current source inverter*
DCM	*Discontinuous conduction mode*
EMC	*Electromagnetic compatibility*
FB	*Full bridge*
FEA	*Finite element analysis*
FF	*Fixed frequency*
FPGA	*Field-programmable gate array*
GEPM	*Group of Power Electronics and Microelectronics*
GTO	*Gate turn-off thyristor*
H	*Hybrid*
HF	*Half bridge*
HMI	*Human-machine interface*
HS	*Hard switching*
IGBT	*Insulated-gate bipolar transistor*
IH	*Induction heating*
JFET	*Junction field-effect transistor*
MOSFET	*Metal-oxide-semiconductor field-effect transistor*
MTBF	*Mean time between failures*
PCB	*Printed circuit board*
PDM	*Pulse density modulation*
PF	*Power factor*
PFC	*Power factor corrector*
PWM	*Pulse-width modulation*
RL	*Equivalent series resistance-inductance*
RMS	*Root mean square*

SiC	*Silicon Carbide*
SMPS	*Switched-mode power supply*
SW	*Square wave*
THD	*Total harmonic distortion*
μC	*microcontroller*
UPS	*Uninterrupted power supply*
UZ	*Universidad de Zaragoza*
VF	*Variable frequency*
VSI	*Voltage source inverter*
WBG	*Wide band gap*
ZCS	*Zero current switching*
ZVS	*Zero voltage switching*

List of symbols

ε	*Electromotive force*
α	*Phase shift angle*
δ_{sw}	*Relative frequency sweep*
ΔT	*Temperature increase*
η	*Efficiency*
τ_x	*Relative value of x*
φ	*Displacement angle*
ω	*Angular frequency*
C	*Capacitor*
C_b	*Bus capacitor*
C_f	*Filter capacitor*
C_r	*Resonant capacitor*
C_s	*Snubber capacitor*
D	*Duty cycle*
E_{off}	*Turn-off switching energy*
E_{on}	*Turn-on switching energy*
f_0	*Resonant frequency*
f_{ac}	*Mains frequency*
f_c	*Cut-off frequency of the filter*
f_{sw}	*Switching frequency*
$f_{sw,avg}$	*Average switching frequency*
G	*Transconductance*
g_x	*Control signal of x*
i	*Number of mains phase*
i_{ac}	*Mains current*
i_{bus}	*Bus current*
i_f	*Filter current*
i_o	*Output current*
i_x	*Instantaneous current value of x*
I_x	*Average current value of x*
$I_{x,rms}$	*Rms current value of x*

j	*Number of the load in a multi-load system*
k	*number of the switching cycle*
K_i	*Integral constant of the regulator*
K_p	*Proportional constant of the regulator*
L	*Inductor*
L_0	*Balancing inductor*
L_b	*Boost inductor*
L_{eq}	*Equivalent series inductance*
L_f	*Filter inductance*
n	*Number of input mains phases*
P	*Average power*
PF	*Power factor*
P_{in}	*Input power*
P_o	*Output power*
$P_{on,x}$	*Conduction losses of x*
$P_{sw,x}$	*Switching losses of x*
Q	*Quality factor*
Q_{oss}	*Parasitic capacitance of the transistor*
R_{eq}	*Equivalent series resistance*
R_o	*Output resistive load*
$R_{x,HF}$	*High-frequency resistance of x*
$R_{x,LF}$	*Low-frequency resistance of x*
S	*Apparent power*
t_a	*Negative time*
T_{ac}	*Mains period*
t_b	*Recovery time*
THD_i	*Total Harmonic distortion of the current*
t_{on}	*Activation time*
T_{pdm}	*PDM period*
T_{sw}	*Switching period*
v_{ac}	*Mains voltage*
v_{bus}	*Bus voltage*
V_f	*Filter voltage*

v_o	*Output voltage*
v_{th}	*Threshold voltage*
v_x	*Instantaneous voltage value of x*
V_x	*Average voltage value of x*
$V_{x,rms}$	*Rms voltage value of x*
$\langle x \rangle_{T_{sw}}$	*Average value of x in a switching period*

Chapters

Chapter 1

Introduction

Industrial induction heating (IH) applications began in the early twentieth century for fast processes of metal hardening, and it was quickly extended to automotive and aircraft industries; however, domestic application was developed later, with the introduction of the insulated-gate bipolar transistor technology (IGBT). In this Chapter, an introduction to induction heating, the domestic application for cooking, and the applied technologies in this area is performed.

Contents

1. Introduction

1.1. Introduction

Induction Heating (IH) is a heating technology that uses electromagnetic fields to increase the temperature of conductive materials. The first developments were applied to industrial metal melting in the early 1900s [1], and this technology was quickly developed during world war II to reach accurate and fast processes of metal hardening, as it is shown in Fig. 1.1 [2-4]. Later, it was extended to automotive and aircraft industries. Currently, it is used in a wide variety of applications, such as manufacturing processes, medical treatments, and domestic applications, among others [5-8].

Fig. 1.1 Induction heating hardening of a gear (leflambela, HE 097 Zahnraderwärmung Applikationslabor, Spule beleuchtet, CC BY-SA 3.0).

Development of IH technology is justified by its advantages in comparison with other heating technologies using conduction, convection, or radiation thermal energy transfer mechanisms [9]. These advantages are summarized as follows. Firstly, faster heating due to fact that the induction target is heated directly, reducing wasted heat and, consequently, heating times. Because of the heat loss to the ambient and surrounding elements is minimized, higher efficiency and temperatures can be reached. Secondly, improved control is achieved since the applied power and location can be accurately defined, leading to improved treatments, such as local heating or predefined temperature profiles. A third advantage is the higher final product quality due to the repeatability of the industrial process and the contactless energy transfer, avoiding flame contact, oxidation, and warping, among other drawbacks. Finally, improved cleanness and safety are

achieved because the temperature of the surroundings of the heating area is lower, avoiding over heating other materials and as well as burn injuries. Besides, fossil fuels are not employed, removing local emissions such as combustion fumes or acoustic noise.

Fig. 1.2 Domestic IH cooker (Courtesy of the BSH Home Appliances Group).

Since the late 80's, domestic applications were able to take the advantage of this technology due to the progresses in power semiconductors, especially with the introduction of the insulated-gate bipolar transistor technology (IGBT) [10, 11]. This improved technology enabled developing compact, reliable, and cost-effective solutions. The main domestic applications of IH are the rice cookers and IH cookers (Fig. 1.2) that get not only an improved heating times and efficiency compared with classical cookers, but also improved safety and cleanness due to the lower surface temperatures [12]. This will be the main application target of this Ph.D. dissertation.

1.2. IH Physical Phenomena

Induction heating is a physical phenomenon that is produced in conductive materials, usually ferromagnetic, when they are exposed to an alternating magnetic field. In this way, the heating energy is wirelessly transferred to the part of the material to be heated, i.e. the base of the cooking pan in the case of domestic IH application. In order to get an effective energy transfer, a medium frequency magnetic field must be applied, typically in the range of tens of kHz for domestic IH, which generates the heating through two physical mechanisms.

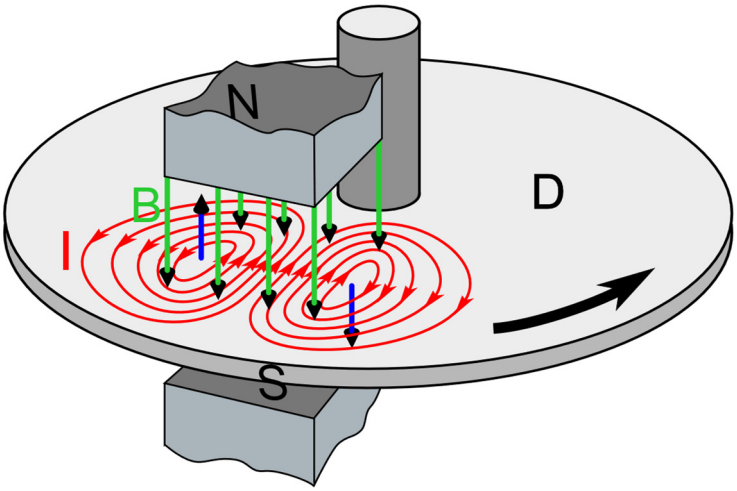


Fig. 1.3 Eddy currents (I, red) induced in a conductive material, D, as it moves under a magnetic field (B, green) generated by a magnet (N-S).

The induced currents (Fig. 1.3) that appear inside a conductive material when a variable magnetic field is applied is the main IH mechanism [13]. These currents, usually known as *Eddy currents* or *Foucault currents*, are dissipated as heat energy when the material resistance is not null. This electromagnetic phenomenon was firstly described by M. Faraday in 1831 and later completed by H. Lenz in 1834, resulting in the most popular version of Faraday´s law statement: *The electromotive force around a closed path is equal to the negative of the time rate of change of the magnetic flux enclosed by the path*. This law is mathematically represented with the following equation, where ε is the electromotive force, and ϕ is the magnetic flux.

$$\varepsilon = -\frac{d\phi}{dt}. \tag{1.1}$$

Besides the induced currents, ferromagnetic materials present another heating source related to the magnetic hysteresis [14] of the materials (Fig. 1.4), named as hysteresis losses. In this kind of materials, the magnetic dipoles, denoted as magnetic domains, are randomly distributed when no magnetic field is applied. However, in the case of applying an external magnetic field, the magnetic dipoles are aligned to the same direction of the field. As a result, when an alternate magnetic field is applied, additional losses are obtained due to the movement and friction of the magnetic domains.

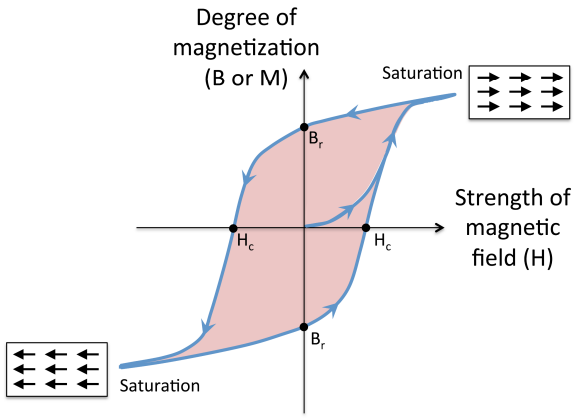


Fig. 1.4 Magnetic hysteresis cycle of a ferromagnetic material (Tem5psu, Magnetic hysteresis, CC BY-SA 4.0).

1.3. Electronic technology applied to domestic IH

IH appliances and rice cookers are the main application of domestic IH. As it has been explained before, the pot is directly heated by the effect of a varying magnetic field, leading to reduced heating times, improved efficiency, accurate control, and improved safety in the cooking process. The scheme of a classical commercial induction heating cooker is shown in Fig. 1.5. It is composed of a vitroceramic glass, which supports the pan or pot used to cook. Below this surface, there is a set of IH coils which vary according to the appliance model. These coils generate the magnetic field that heats the pot through the previously discussed mechanisms: *Eddy Currents* and magnetic hysteresis. Typically, an aluminum shielding is used to protect the remainder elements, under which the power electronic system is allocated along with the control module and the forced-convection air cooling system.

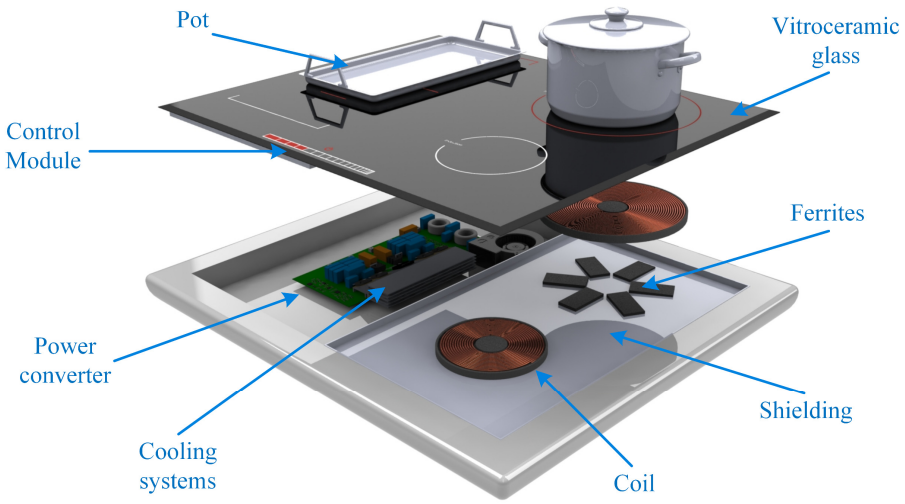


Fig. 1.5 Main elements of a typical commercial IH cooktop.

The elements of a typical domestic IH system can be classified into three main groups according to its functionality: the inductor-load system, the power electronics, and the control electronics. Each block has to be optimally and coordinately designed to get a good performance and cost-effective final product [15]. These blocks are further explained in the next sub-sections. This dissertation will focus on the design of new higher performance power electronic converters as it will be discussed later in this document.

1.3.1. Inductor-load system

The inductor-load system (Fig. 1.6 (a)) is one of the most relevant elements in the domestic induction heating system because it transforms the electrical energy into heat in the load, i.e. the pot. It consists of a planar spiral coil of conductor wires, usually copper *Litz* wires [16-19], and a vitroceramic glass, where the pot is placed. Under the windings, ferrite bars are usually allocated to concentrate the magnetic flux and improve the magnetic coupling between the vessel and the coil. An additional surface below the glass provides thermal an electrical isolation. Finally, an aluminum shielding surface avoids the electromagnetic interference in the power and control electronics.

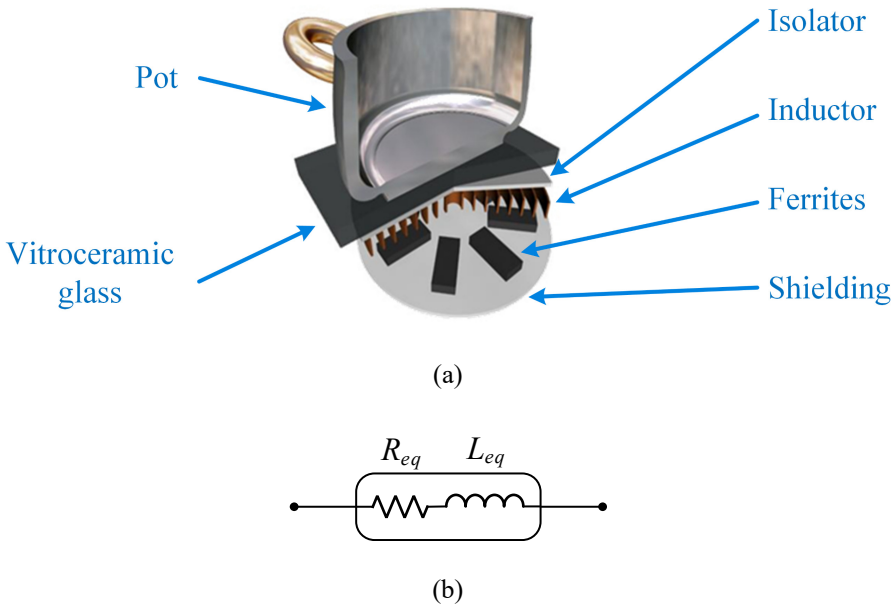


Fig. 1.6 Main elements of an inductor-load system (a) and equivalent electrical model (b).

The inductor generates a variable magnetic field using the medium-frequency current provided by the power converter. The electrical equivalent model of the inductor-load system depends on both the inductor and the pot properties, i.e. temperature [20], geometry, material, distance to the inductor, etc. The high dependence of the model with these parameters makes difficult to obtain a general model. Although, some complex

models consider the frequential dependence of the load [21-25], the most used electrical approach is based on the equivalent series resistance-inductance (RL) model [26, 27], which is only valid for a single operation point (Fig. 1.6 (b)).

Using this model, the quality factor, Q, is a useful parameter that allows characterizing the load. It is defined as follows:

$$Q = \frac{\omega L_{eq}}{R_{eq}}, \tag{1.2}$$

where ω is the angular frequency, L_{eq} is the equivalent series inductance, and R_{eq} is the equivalent series resistance. Besides, when a series resonant configuration of the load is implemented, the resonant frequency, f_0, is obtained as a function of the resonant capacitor, C_r, as

$$f_0 = \frac{1}{2\pi\sqrt{L_{eq}C_r}}. \tag{1.3}$$

As Fig. 1.7 shows, the load along with resonant capacitor behaves as an inductive load when the operating frequency, f_{sw}, is higher than the resonant frequency, and as a capacitive load when the operating frequency is lower than the resonant frequency. The maximum output power is achieved at resonant frequency since the load behaves as a purely resistive load.

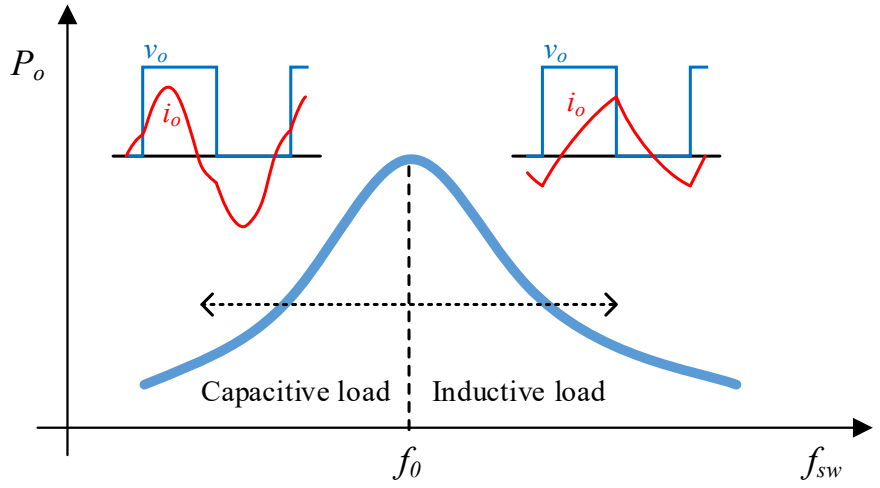
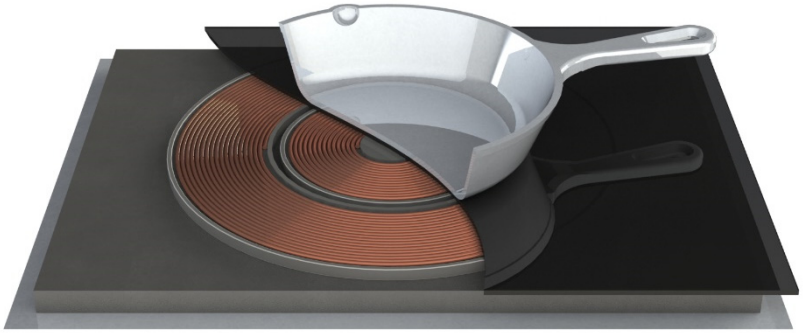


Fig. 1.7 Output power distribution, P_o, and main waveforms of a resonant load as a function of the operation frequency, f_{sw}. Voltage, v_o, and current, i_o, waveforms of the resonant load for inductive and capacitive behavior.

In recent years, domestic IH appliances have moved towards more flexible cooking surfaces, providing the user with a much more adaptable cooking area with additional degrees of freedom. In order to accomplish this, the inductor-load systems have progressed towards multi-inductor structures that enable powering any pan or pot, regardless the selected size, shape, or position. Currently, the design of these multi-inductor architectures is focused on three main trends [28]. Firstly, concentric-coils systems (Fig. 1.8 (a)) are composed of two or three concentric ring-type inductors that are activated according the area covered by the vessel [29-31]. Secondly, non-concentric-coils systems provide a reconfigurable cooking surface that allow adapting properly the heating area for a determined range of size and shape of pots. Finally, total-active surface systems (Fig. 1.8 (b)) are the most flexible solution because they consist of a set of small-size inductors that are grouped to adapt to the size and shape of the vessels to be heated [32, 33]. Therefore, these systems are not restricted by the pot shape, dimension, or quantity of the pots. The research performed in this dissertation will enable improving such systems either allowing higher power IH systems or flexible implementations with improved power control.



(a)

(b)

Fig. 1.8 Flexible cooking surfaces. (a) classical concentric coils and (b) total active surface concept.

1.3.2. Power electronics

Domestic IH appliances require an electronic power converter in order to transform the mains low-frequency ac voltage into an ac medium-frequency voltage, typically between 20 kHz and 100 kHz, to power the inductor-load system. Classical induction heating power supplies are based on a two-stage power conversion scheme as it is shown in the block diagram of Fig. 1.9. Firstly, the mains voltage is rectified to obtain a dc-link voltage, v_b. Usually, a diode full-bridge is used, and a small dc-link capacitor is placed in order to supply the high-frequency currents that are required from the inverter and, at the same time, ensure an input power factor close to one. The main drawback of this small filter capacitor is that a high-ripple dc-link voltage is obtained, decreasing the effective dc-link voltage, and therefore, increasing the inverter current levels for the same output power. Besides, an electromagnetic compatibility (EMC) filter is essential so that the appliance fulfills the EMC regulations.

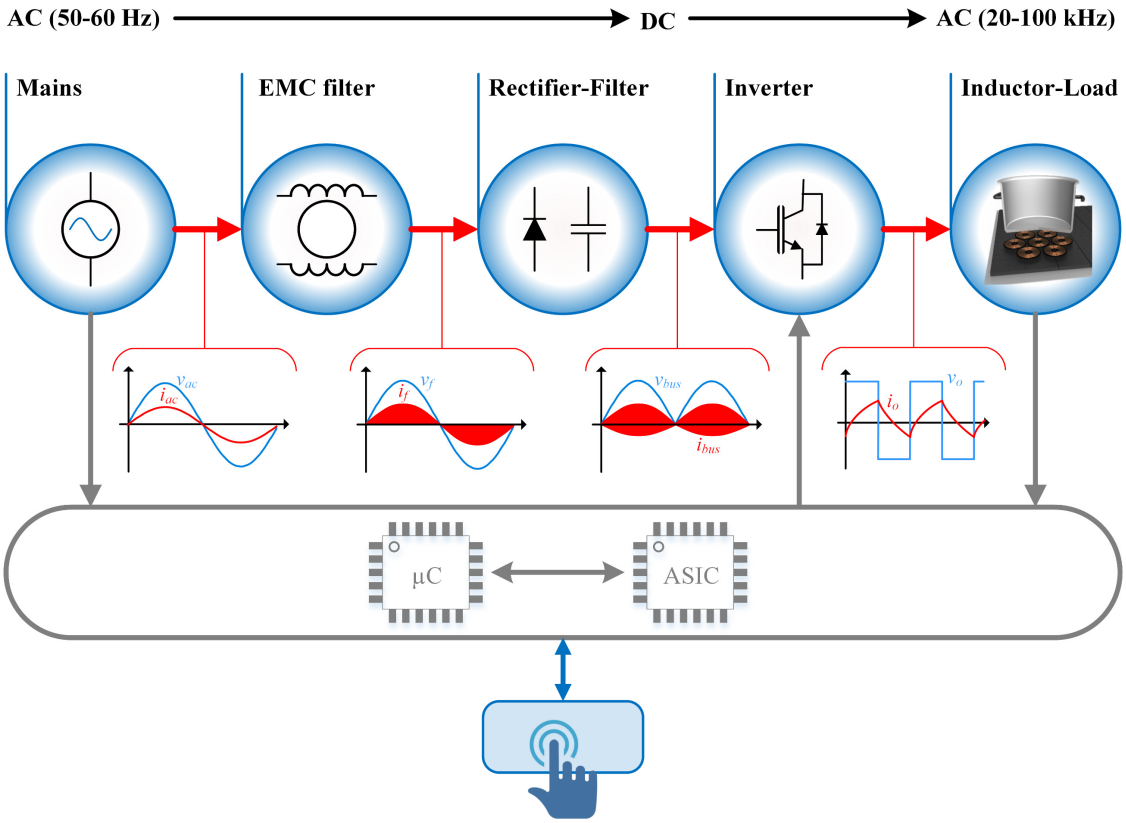
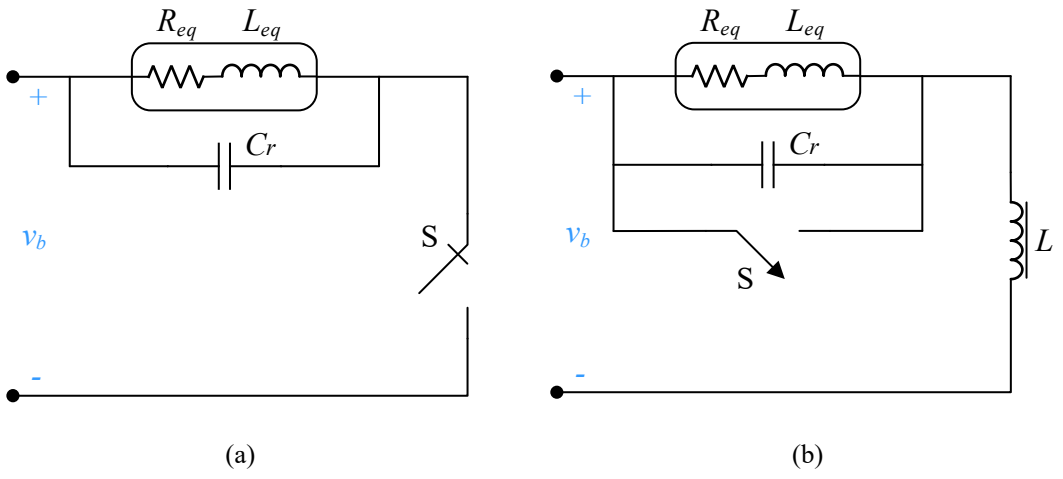


Fig. 1.9 Block diagram of a typical power electronic converter for domestic induction heating applications.

Secondly, an inverter generates the medium-frequency voltage and current delivered to the inductor. Several inverter topologies have been applied in the past to domestic IH. Nowadays, resonant and quasi-resonant topologies are the most used ones due to their

increased performance and cost-effective implementations [34]. Besides, Voltage Source Inverters (VSI) are employed instead of Current Source Inverters (CSI) because the latter requires need an additional bulky inductor. All these topologies lead to more efficient and smaller converters, getting an increased power density and enabling the development of advanced domestic IH cookers. The selection of the proper topology depends strongly on the desired final application performance. Therefore, diverse factors must be taken into account, such as number of loads, output power, cost, efficiency, etc. Moreover, there are additional factors that depend on the geographic area, i.e. mains connection and number of phases, mains voltage, EMC, or safety regulations, among others. In the following lines, the most common single-load topologies for domestic IH are presented, classified according to the number of switching devices, S.

Quasi-resonant single-switch topologies are the cheapest solutions [35-39]. Currently, they are mainly implemented in the Asian market mainly because the maximum required output power is lower than 2000 W. These topologies need high voltage switching devices, since they must typically block up to 3 - 4 times the mains voltage. Therefore, the lower mains voltage in this region (120 V) makes it easier to implement such topologies. Fig. 1.10 shows some examples of these converters in the zero-voltage-switching (ZVS) and zero-current-switching (ZCS) implementations. The main disadvantage is that the power control is limited because there is only a single control parameter, on time (ZVS) or off time (ZCS), and it depends on the load, decreasing the efficiency and the controllability. This is especially critical when several loads are powered simultaneously.



(a) (b)

Fig. 1.10 Single-switch quasi-resonant inverters for induction heating applications: ZVS (a) and ZCS (b) inverter implementations.

Half-bridge topologies use two switching devices [40-45]. The half-bridge series resonant inverter using IGBTs and antiparallel diodes (Fig. 1.11) is currently the best implementation in terms of cost-effectiveness due to the excellent trade-off among performance, cost, and complexity. This topology is usually operated in the ZVS region above the resonant frequency. The main advantage of a series resonant configuration is that an increased output power and improved efficiency is achieved for the same inductor-load system. In addition, the series configuration of the resonant capacitor avoids dc or 100-Hz ac current in the inductor and, therefore, eliminates saturation issues. Furthermore, usually a split configuration of the resonant capacitor is preferred to decrease the current harmonics present in the bus. Snubber capacitors, C_s, are also usually used to decrease turn-off switching losses of IGBTs.

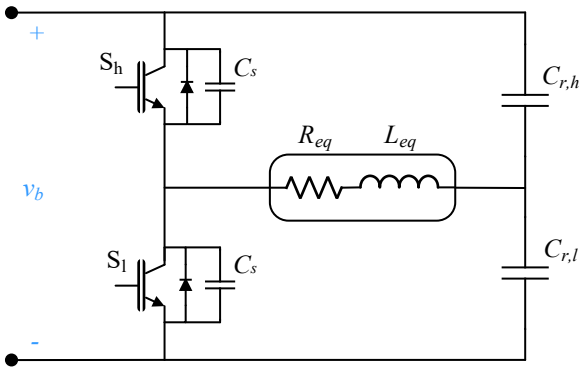


Fig. 1.11 Half-bridge series resonant inverter using split resonant capacitor and snubber capacitors. Switching devices are implemented with IGBTs and antiparallel diodes.

The full-bridge topology [46-49] is composed of four switching devices as it is shown in Fig. 1.12. Compared with the half-bridge configuration, it allows doubling the output voltage in the load and, therefore, increasing the output power. However, the higher number of switching devices increases the cost of this solution and, for this reason, it is most common in industrial applications rather than domestic ones [26]. In spite of this, some commercial implementations have been accomplished recently [50].

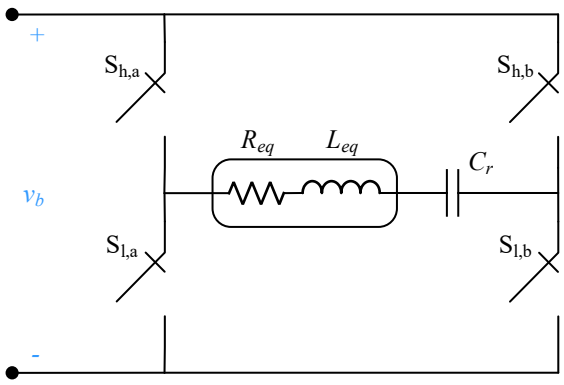


Fig. 1.12 Full-bridge series resonant inverter.

As it has been previously explained, classical domestic IH appliances are composed of several heating regions or induction coils where the pot can be placed, usually between two and four, whereas the latest trends of flexible surfaces have a higher number of coils, which can go up to 48 in the case of total-active surfaces. The aforementioned topologies are able to power a single load and, therefore, other solutions become necessary to power a higher number of loads, n, in a cost-effective and versatile way. The immediate solution for doing that is to replicate the topology as many times as number of loads [32], however, it is the least cost effective because of the increased number of switching devices.

In this context, several proposals have been presented in the past to get cost-effective solutions to power multi-load systems. The main drawbacks of the multi-output structures are that the power control becomes more complicated, and the main switches are designed considering the number of simultaneously activated loads. Therefore, the current rating of these devices significantly increases for a high number of loads, raising also the cost. As a result, multi-output topologies are preferred when a low number of loads are powered at the same time, as in the case of flexible surfaces.

Nowadays, there are two basic families of power conveter topologies applied to multi-load systems. On the one hand, configurations derived from the half-bridge or full-bridge topologies using electromechanical relays allow multiplexing several loads, as it is presented in Fig. 1.13 [51]. In this case, the relays are periodically activated to power a single load, or a combination of them, during a certain period, achieving a cost-effective solution. However, it presents some drawbacks for the user, such as acoustic noise of the relay activation or discontinuous heating of the cooking element, which can be perceptible by the user. Besides, the output power control is limited in order to fulfill the flicker limits

of the EMC regulations, and the mean time between failures (MTBF) of the converter is decreased due to the increased number of switching of the relays.

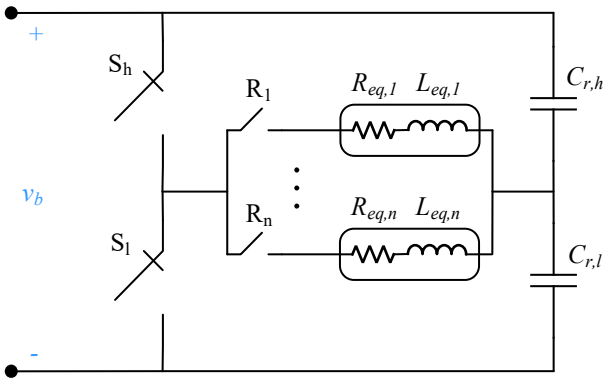


Fig. 1.13 Half-bridge series resonant inverter using electromechanical relays, R, to power *n* resonant loads.

On the other hand, multiple-output inverters using fully semiconductor implementations are the most effective solution since they allow powering several loads simultaneously and controlling the output power in each load accurately. In order to get these benefits, additional switching devices are used at the cost of a more complex control. These solutions avoid the use of electromechanical relays and their main drawbacks, improving the user experience and the shelf life of the converter.

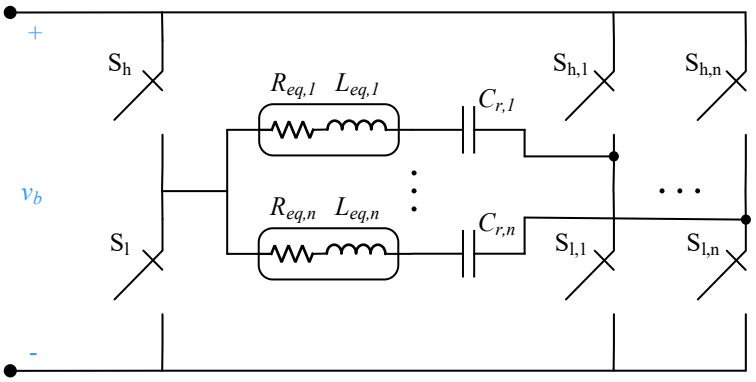


Fig. 1.14 Multi-output inverter based of the full-bridge inverter.

Some additional multi-output topologies for IH have been presented in the past and they are discussed in the following lines. The first one (Fig. 1.14) is based on the full-bridge topology, and it is able to power *N* loads using 2+2*N* switching devices. There is a common half-bridge branch and an additional half-bridge branch per load. In this case, the output powers are controlled using the switching frequency, the duty cycle, and the phase between branches [52-55]. The topology shown in Fig. 1.15 is derived from the half-bridge inverter and it can power *N* loads using 2 + *N* switching devices. It consists

of a common half-bridge inverter and an additional switch to activate or deactivate each load [52, 56-60]. Finally, solutions based on matrix structures have been proposed to power a high number of loads [61]. For instance, the topology shown in Fig. 1.16 is able to power N loads using $2\sqrt{N}$ switching devices, decreasing considerably the quantity of required power devices [62, 63].

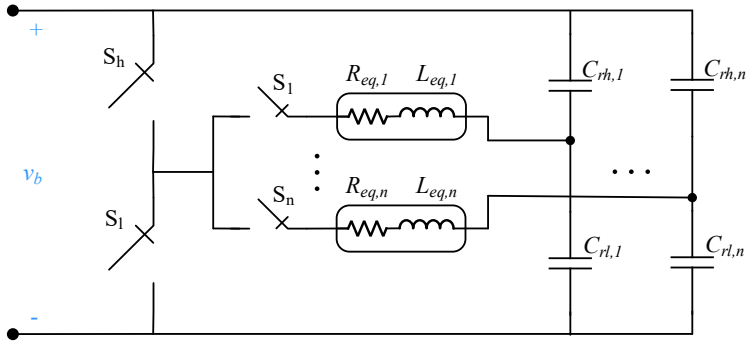


Fig. 1.15 Series resonant multi-inverter.

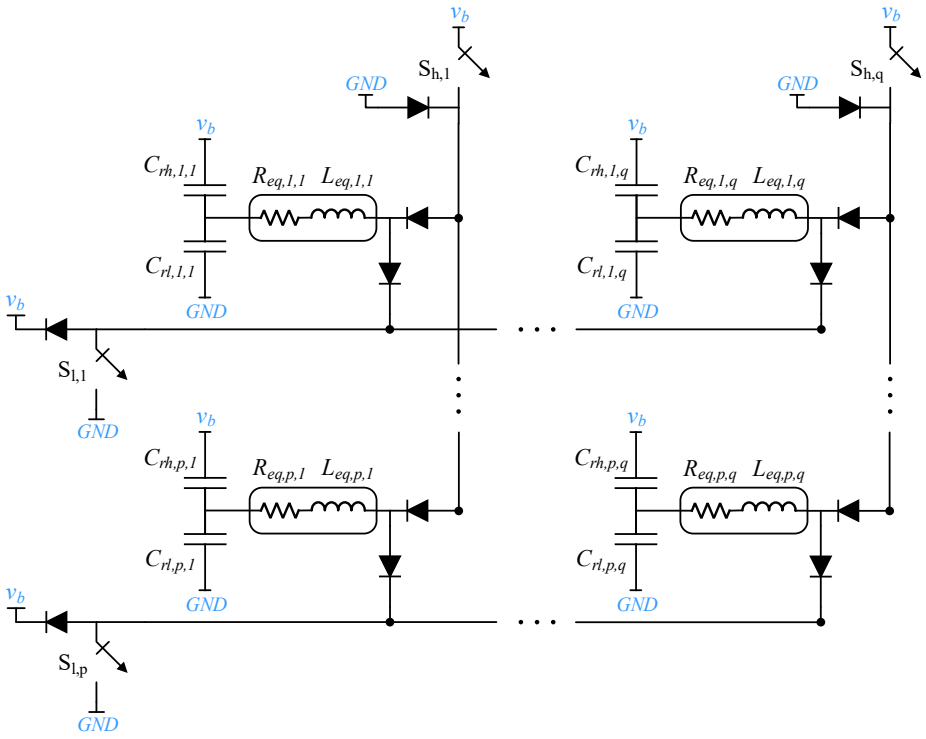


Fig. 1.16 Multi-output ZVS resonant inverter.

1.3.3. Control electronics

The control electronics must manage the power converter as well as to serve as a human-machine interface (HMI) for the domestic IH appliance. The control electronic hardware (Fig. 1.17) is typically composed of a microcontroller (μC) and an Application Specific Integrated Circuit (ASIC) or a Field-Programmable Gate Array (FPGA) [64-67]. Because of its high versatility, the microcontroller [68] manages the high-level tasks, as the communication process, the user interface, and the control algorithms, whereas the ASIC or FPGA, which allow developing specific hardware for the converter and implementing parallel processes [69, 70], manages the PWM modulations, the analog-to-digital conversion, or the power computation. One of the most relevant advantages of this separate scheme is that the ASIC is designed to manage a specific converter whereas the microcontroller can be adapted to the different implementations, getting a versatile control structure.

The gate signals of switching devices are generated by the control electronics, which is composed of two main blocks: the measurement system and the digital control. Firstly, the measurement system block manages the acquirement of several signal of the power electronics, such as the inductor current, the bus voltage, or the inductor temperature. It mainly consists of sensor circuits and analog-to-digital converters [71, 72]. Secondly, the digital control block generates the gate signals in function of the power level selected by the user and the measurement system information. This block uses different predefined control algorithms and modulation strategies in order to get the selected power safely and fulfill the pertinent regulations.

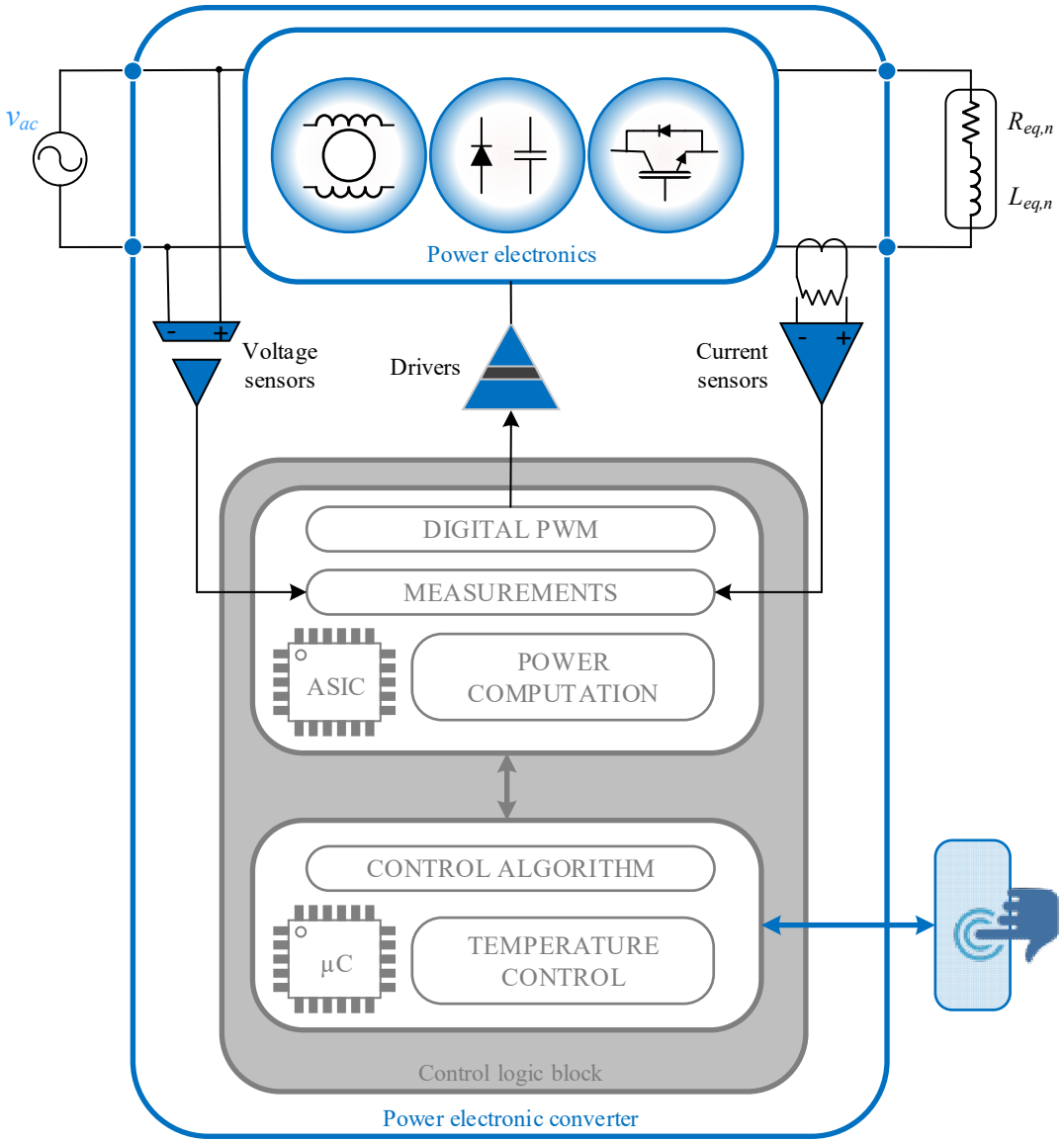


Fig. 1.17 Diagram of the control logic block of the power electronic converter. The microcontroller (µC) is used for the control algorithm whereas the ASIC is used for the higher computational tasks.

The modulation and control strategies manage the switching devices of the inverter stage to perform the power control while ensuring the correct and safe converter operation. The final efficiency and performance of the power converter are greatly defined by these modulation techniques. The most common modulation strategy applied to domestic IH appliances is the Square Wave (SW) control (Fig. 1.8 (a)) [45, 73, 74] because it allows controlling the higher power range simply and efficiently. Using this technique, the power converter usually works at frequencies higher than the resonant frequency to obtain an inductive behavior and operate in ZVS conditions. The power is decreased by increasing the operating frequency, as it is shown in Fig. 1.7. The main drawback of this technique is that a high frequency is required to get low-medium output

power, increasing the switching losses and decreasing the efficiency of the converter. Therefore, other fixed-frequency control techniques are also applied to control the lower power range, such as Asymmetrical Duty Cycle (ADC) (Fig. 1.8 (b)) [74-76], Asymmetrical Voltage Cancelation (AVC) [47, 77-79], Pulse Density Modulation (PDM) [80-83], or discontinuous modulation strategies [56, 84-86]. The PDM control (Fig. 1.8 (c)), also called burst mode, is the most common and simplest strategy because achieves a linear output power control by applying a pulsed output power to the IH-load.

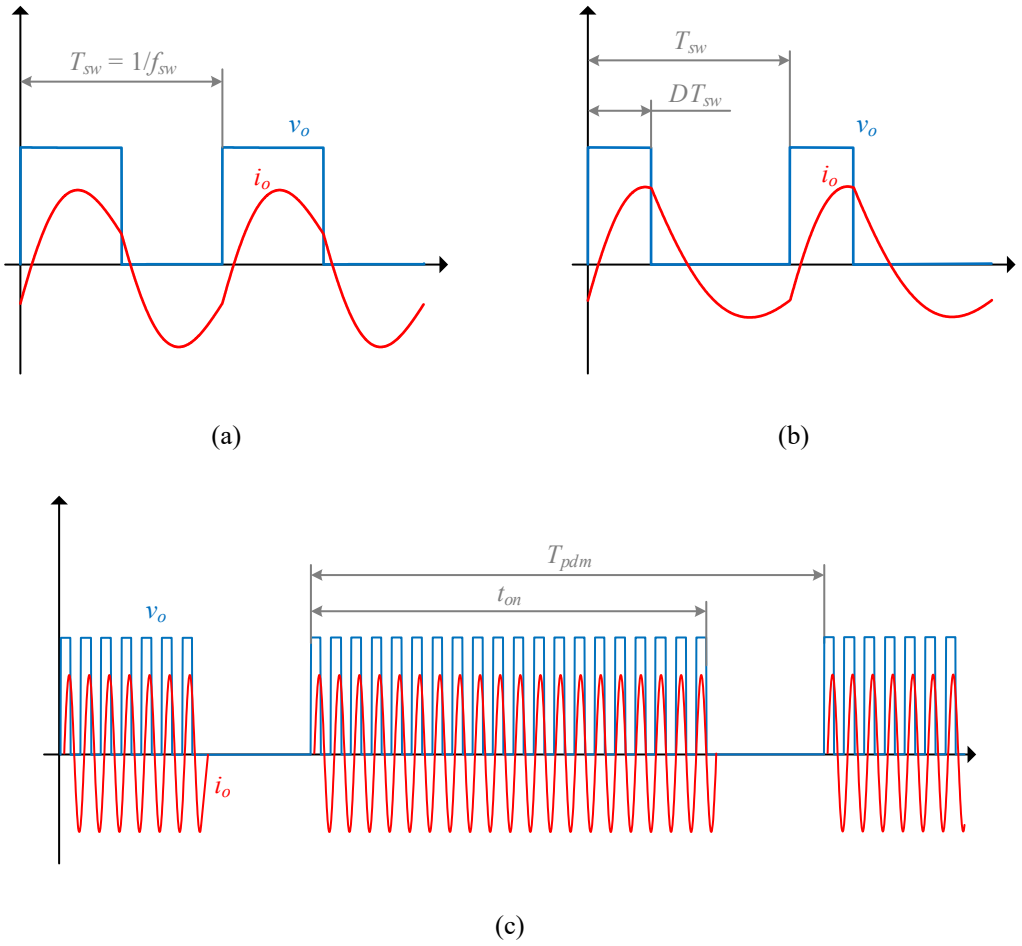


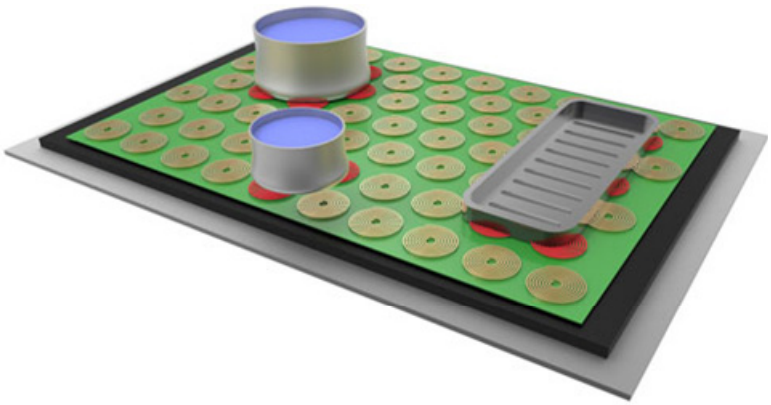
Fig. 1.18 Main waveforms and control parameters of the (a) Square Wave (SW), (b) Asymmetrical Duty Cycle (ADC), and (c) Pulse Density Modulation (PDM) modulation strategies used to control the output power of the electronic converters applied to domestic IH.

1.4. Current challenges of domestic IH

As discussed above, domestic IH cooking surfaces improve significantly the final user experience due to their fast cooking, efficiency, safety and cleanness. Besides, flexible surfaces improve further this experience because of the bigger coils with several concentric windings or fully active surfaces, enabling the use of any pan or pot, regardless the selected size, shape, or position. However, the design specifications of this technology

are more restrictive because of the control constraints: higher output power, higher efficiency, the required power density to fit the electronic system into a built-in implementation, EMC restrictions, power coupling issues between mains phases, and, last but not least, the cost, specially of inductor-load systems and power electronics of flexible surfaces.

In the past, great efforts have been made to get more cost-effective solutions. On the one hand, some proposals have been addressed to decrease the cost and increase the efficiency of inductor systems of flexible surfaces, such as inductors on extra-thin PCB (Fig. 1.19 (a)) [87], overlapped inductors (Fig. 1.19 (b)) [88, 89], or mobile inductors (Fig. 1.19 (c)) [90, 91]. On the other hand, regarding power electronics, additional efforts have been performed to reach high-efficiency converters, multi-output inverters, or low-cost measurement systems [92-95].



(a)

(b)

(c)

Fig. 1.19 Novel solutions of inductors for improved-performance and cost-effective flexible surfaces. (a) Inductors implemented on PCB as cost-saving alternative for conventional size inductors of flexible surfaces. (b) Overlapped inductors that combine the high efficiency of large inductor with the high flexibility of small adjacent coils. (c) Mobile inductor concept to decrease the cost of inductor systems and power electronics.

In this first chapter, a brief introduction about induction heating focused on the domestic application has been presented, covering the basic building blocks of an IH appliance from the power electronics point of view. The next chapter will explain in detail the rectification systems, with especial emphasis in the Power Factor Correction (PFC) rectifiers, which is the main aim of this dissertation.

Chapter 2

Overview of PFC Rectifiers for Induction Heating

Mains voltage distortion and total harmonic distortion of the current are power quality issues caused mostly because of the use of non-linear loads, such as the typical ones used in domestic IH applications. In this Chapter, a review of the state of the art of rectification systems is performed, including power factor correction systems to decrease these power quality issues. According this perspective, the objectives of this dissertation, its scope, and structure are presented.

Contents

2. Overview of PFC Rectifiers for Induction Heating

2.1. Introduction

Electric power for residential services is distributed in different ways around the world, as it is shown in Fig. 2.1. Most of the regions in Europe, Asia and Africa use 50 Hz frequency with 220 or 230 V in single phase configuration, or 400 V with 3 phase configurations whereas most of American countries use 60 Hz and 120/240 V split-phase or single-phase three-wire systems (Fig. 2.2) [96]. The domestic IH market is an international market with presence in most of the world, and in Europe specially, and therefore, different mains connections have to be taken into account when these appliances are designed.

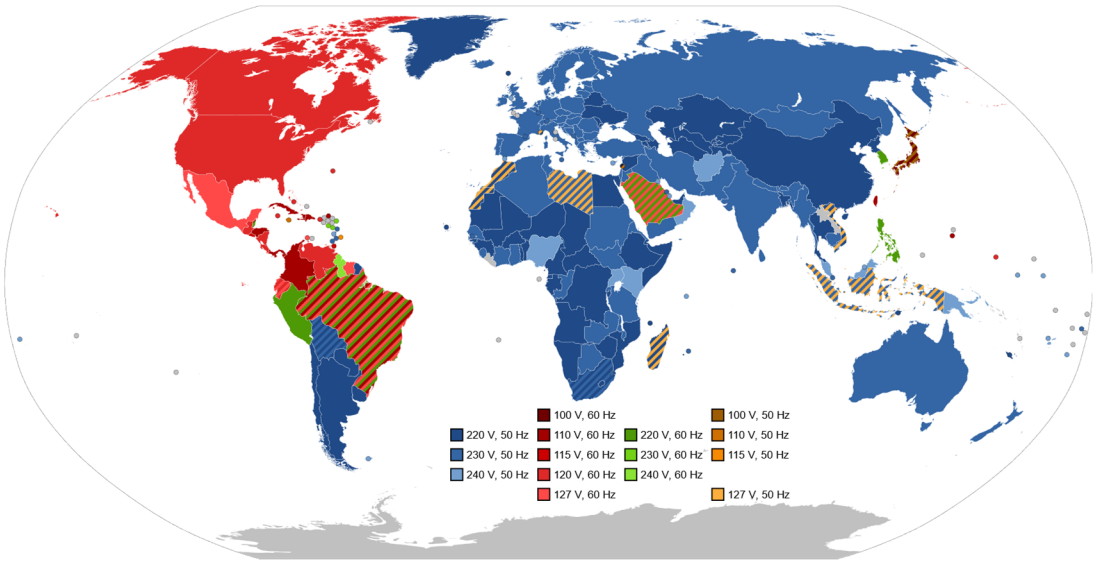
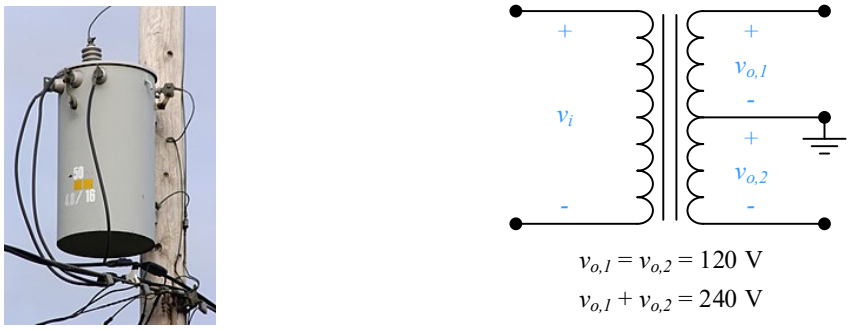


Fig. 2.1 World map of mains voltage and frequencies distribution. [SomnusDe, World Map of Mains Voltages and Frequencies, Detailed, marked as public domain, more details on Wikimedia Commons]



(a) (b)

Fig. 2.2 The 120/240 V split-phase is the most typical distribution system for residential services in American countries: (a) a pole-mounted single-phase split-phase transformer and (b) d its electric diagram.

Power electronic converters are usually implemented in electronic boards that are powered from single-phase mains and that are designed for 50-60 Hz and 220-240-V mains voltage operation, covering the greater part of the international market. However, the maximum power is constrained by the maximum admissible current that the domestic electric installation can deliver, which is defined by international standards. The CENELEC is responsible for European standardization in the area of electrical engineering.

Single-phase and three-phase residential systems are usually designed for 16-A maximum current. However, single-phase domestic systems usually have some additional power outlets for higher currents in order to power the high-demanding appliances, such as air conditioning units, ovens, or induction cooktops. Commonly, the maximum current per phase is limited to 16 A; therefore, single-phase power converters for domestic IH appliances are developed for 3.6-kW maximum power. A current state-of-the-art converter from a major manufacturer is shown in Fig. 2.3. It is important to note that this converter includes not only the power electronic board but also, the auxiliary voltage power supply and the control logic.

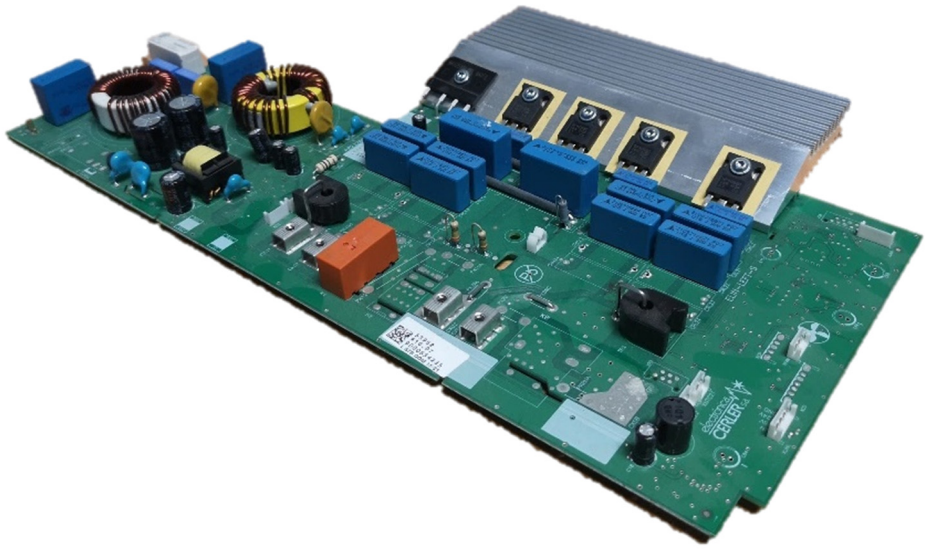


Fig. 2.3 Image showing the current power electronic converter in an isolated electronic board. It is composed of an EMC filter, a full-bridge diode rectifier, and two half-bridge inverters. Courtesy of BSH Home Appliances Group.

Most high-performance IH cooktops are designed to heat several vessels simultaneously. As a consequence, these appliances require higher power than 3.6 kW for covering the complete power demand. The solution that is usually followed is to place two separated 3.6-kW power converters in two isolated electronic boards, doubling the total power up to 7.2 kW. As a result, induction cooktops are connected to two different mains phases in case of a three-phase domestic installation, whereas in a single-phase configuration both electronic boards are paralleled and powered from the mains using the high-demand power outlet. In the next section, some key aspects regarding power quality of the mains are presented to introduce the importance of rectification systems and their effect on the mains.

2.2. Power quality

Electric power quality is determined by the quality of voltage and current waveforms, and frequency. In this way, a good power quality can be defined as a steady supply voltage that stays within the prescribed range, steady frequency close to the rated value, and sinusoidal voltage waveform. In general, it is useful to consider power quality as the compatibility among different devices connected to the mains [97-99].

Defects of power quality can be classified in different categories: harmonic distortion, voltage sags [100], voltage fluctuations and flicker, transients, etc. Each problem has a different cause: Whereas some of them are derived from the electrical infrastructures, other ones are generated by the user [101]. In this context, voltage distortion because of harmonic content is one the most important defects of power quality that is produced by power electronic equipment.

2.2.1. Mains voltage distortion

The mains can be modeled as an ideal power supply, v, and an output impedance, Z, as it is shown in Fig. 2.4 [102]. Because of the output impedance, also named mains impedance, the mains or supply voltage, v_s, is affected by the supply current, i_s, of the load, L. When resistive loads are powered, the output current is sinusoidal as the mains voltage, however, when non-linear loads are powered, the current is non-sinusoidal and the voltage is distorted due to the output impedance, decreasing the power quality because of the induced low-frequency harmonics which affect to other devices that are connected to the same network.

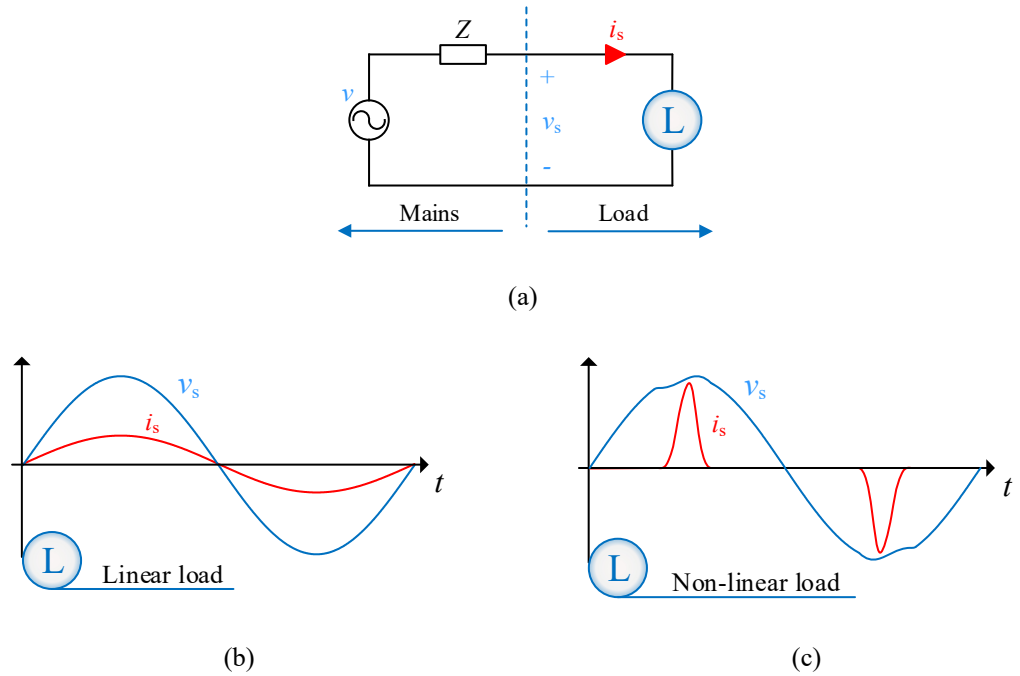


Fig. 2.4 Comparison of the mains voltage distortion due to the mains impedance and the nature of the powered load. The top figure (a) shows a load, L, powered by the mains, which is modeled as an ideal power supply, v, and a mains impedance, Z. The supply voltage, v_s, and current, i_s, are sinusoidal waveforms when a linear load is used (b) however, the voltage is distorted in the case of a non-linear current consumption (c).

In the past, this situation was not a problem because most of the connected loads were linear, such as incandescent lighting or resistive ovens. In the last decades, however, electronics devices have proliferated in industry: frequency variators, induction ovens, battery chargers, etc; in office: computers, photocopiers, etc; and in homes: television, mobile phone chargers, inverters for air conditioning or other appliances, etc. Therefore, a significant number of non-linear loads using rectification systems or ac-dc converters are connected to the mains.

For years, in order to decrease the mains voltage distortion generated by converters, electric devices commercialized in the international market have to fulfill EMC international standards. The IEEE has published numerous standards dealing with the power quality phenomena explained before. One of the most relevant for power electronic devices is the IEEE STD 519 [103]. In Europe, the IEC 61000-3-2 directive prescribes the maximum value for harmonic currents from the second harmonic up to and including the 40th harmonic current for equipment with a rated current up to 16 A, as it is the case of domestic IH.

2.2.2. Total Harmonic Distortion

Mains voltage and current are usually sinusoidal waveforms. However, when they are distorted, additional components, which are multiple of the fundamental mains frequency and are known as harmonics, appear. These components may be calculated using Fourier analysis.

In this way, a periodic non-sinusoidal waveform $f(t)$ with angular frequency, ω, is expressed as

$$f(t) = F_o + \sum_{k=1}^{\infty} f_k(t) = \frac{1}{2}a_o + \sum_{k=1}^{\infty}\{a_k \cos(k\omega t) + b_k \sin(k\omega t)\}, \tag{2.1}$$

where $\frac{1}{2}a_o$ is the average value of (2.1), k is the harmonic number and

$$a_k = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(k\omega t)d(\omega t), \quad k = [0,\infty], \quad k \in \mathbb{N}, \tag{2.2}$$

and

$$b_k = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin(k\omega t)d(\omega t), \quad k = [1,\infty], \quad k \in \mathbb{N}. \tag{2.3}$$

In Fig. 2.5, an example waveform, x, with harmonics is shown along with its Fourier analysis, and its breakdown in its main components, x_1 and x_2.

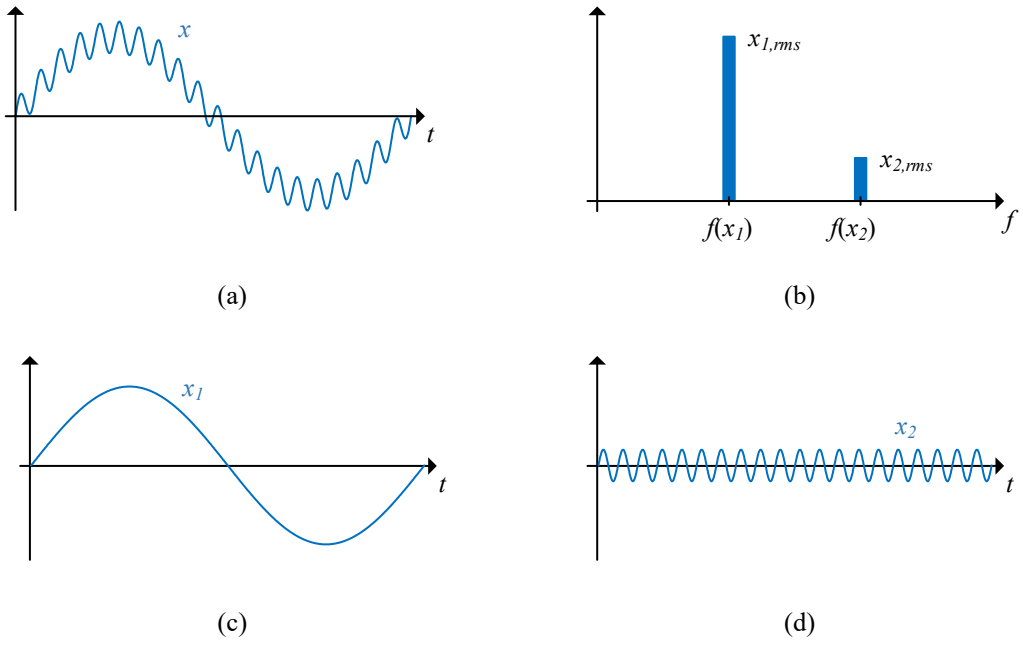


Fig. 2.5 Breakdown of a waveform, x, which is composed of two main components, using Fourier analysis. In (a) the x waveform, in (b) the Fourier analysis, and in (c) and (d) the waveforms of the two components, x_1 and x_2, respectively.

The input behavior of a power converter is characterized in general by the power factor, *PF*, the fundamental current-to-voltage displacement angle, ϕ, and the Total Harmonic Distortion of the input current, THD_i, which are related by the equation

$$PF = \frac{1}{\sqrt{1+THD_i^2}}\cos(\phi). \tag{2.4}$$

The THD_i is a measurement of the harmonic distortion present in a current waveform, *i(t)*, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. It is most commonly calculated as the ratio of the root mean square (rms) amplitude of a set of higher harmonic frequencies to the rms amplitude of the first harmonic or fundamental frequency, as is expressed in the below equation

$$THD_i = \frac{\sqrt{\sum_{k=2}^{\infty} I_{k,rms}^2}}{I_{1,rms}} = \frac{\sqrt{I_{rms}^2 - I_{1,rms}^2}}{I_{1,rms}}, \tag{2.5}$$

where $I_{n,rms}$ is the rms value of the *n*th harmonic and n=1 is the fundamental frequency. Equally, it can be calculated as a function of the rms value of the waveform, *I*.

The *PF* of an alternating electrical power system is defined as the ratio of the real power absorbed by the load to the apparent power flowing in the circuit, and it is a dimensionless number between 0 and 1. Therefore, the *PF* is expressed as

$$PF = \frac{P}{S}, \tag{2.6}$$

where *S* is the apparent power that is calculated as the product between the rms voltage, V_{rms}, and rms current, I_{rms}.

$$S = V_{rms} I_{rms} \tag{2.7}$$

A power factor of less than one indicates the voltage and current are not in phase and/or the current is distorted, reducing the average product of the two. Real power, *p(t)*, is the instantaneous product of voltage, $v(t)$, and current, $i(t)$, and represents the capacity of the electricity for performing work. The real power or active power in a period, *T*, is calculated as the average power, *P*, using the below general expression

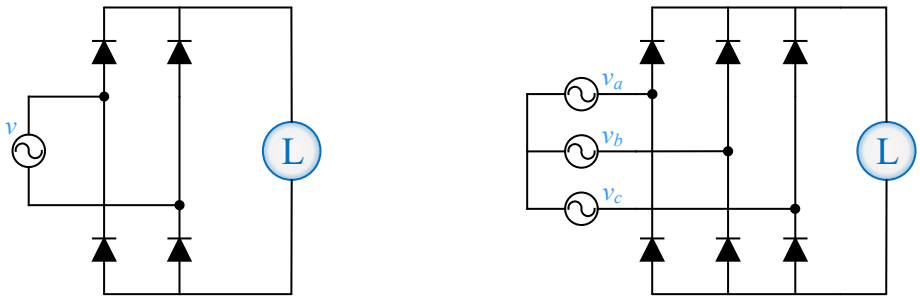
$$P = \frac{1}{T}\int_0^T p(t)dt = \frac{1}{T}\int_0^T v(t)i(t)dt. \tag{2.8}$$

In order to address the challenge of power quality in power electronic converter, special attention must be paid when designing the rectification stage of power electronic converters connected to the mains. In the next section, a review of the state-of-the-art of rectification systems is provided, regarding both conventional and power factor correction systems.

2.3. State-Of-The-Art of rectification systems

2.3.1. Conventional rectification systems

Ac–dc conversion of electric power is widely used in a wide range of applications such as adjustable-speed drives (ASDs), switched-mode power supplies (SMPSs), uninterrupted power supplies (UPSs), and battery energy storage, among others. Usually, ac–dc converters, also known as rectifiers, are developed using diodes and thyristors to provide uncontrolled and controlled, respectively, dc power with unidirectional and bidirectional power flows. The main drawbacks of conventional rectification systems include poor power quality in terms of injected current harmonics, poor power factor at the input, and mains-frequency ripple present in the output; all these elements leading to low efficiency, and costly and bulky ac and dc filters [104].



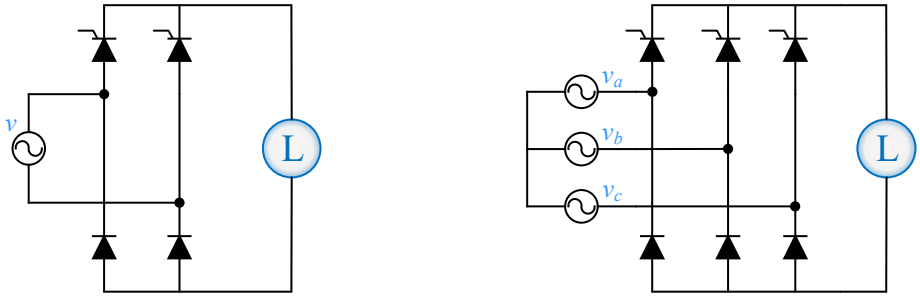
(a) (b)

Fig. 2.6 Uncontrolled rectifiers: (a) single-phase full-bridge rectifier and (b) three-phase full-bridge rectifier.

The most common uncontrolled rectifiers (Fig. 2.6) are the full-bridge rectifiers for single-phase and three-phase configurations. However, other configurations are used in power electronics, such as the half-wave rectifier, the full-wave rectifier with center-tapped transformer for single-phase applications, or the three-phase star rectifier for three-phase applications, among others [105, 106].

The controlled versions of these rectifiers are obtained by using thyristors instead of diodes. However, they are more complex because a control driver has to be included in

the circuit to activate this power device. Besides, the waveforms depend on the load type since, in an inductive load case, thyristors continue activated and carry current despite the voltage is negative, therefore, they work not only as rectifiers but as inverters depending on the load and the activation. Although the most typical controlled rectifiers are the full-controlled bridge rectifiers, Fig. 2.7 shows the half-controlled full-bridge rectifiers for single-phase and three-phase applications.



(a) (b)

Fig. 2.7 Half-controlled rectifiers using thyristors: (a) single-phase and (b) three-phase bridge rectifiers.

2.3.2. Power factor correction rectification systems

In an electric power system, a load with a low power factor draws more current than a load with a high power factor for the same amount of useful power, i.e. active power, transferred. The higher current increases the energy lost in the distribution system and require larger wires and equipment. Because of the costs of larger equipment and wasted energy, electrical utilities will usually charge a higher cost to industrial or commercial customers where there is a low power factor.

Power factor correction increases the power factor of its load, improving efficiency for the distribution system to which it is supplied. Linear loads with low power factor, such as induction motors, can be corrected with a passive network of capacitors or inductors. Non-linear loads, such as rectifiers of domestic IH appliances, distort the current drawn from the system. In such cases, active or passive power factor correction (Fig. 2.8) may be used to counteract the distortion and raise the power factor.

On the one hand, passive methods include the use of tuned LC filters and avoid the use of controlled elements, what represents a robust solution. On the other hand, active methods come as a more efficient and high-performance solution by using controlled solid-state switches in association with passive elements such as inductors and capacitors. The devices for correction of the power factor may be at a central substation, spread out

over a distribution system, or built into power-consuming equipment. In the following subsections, passive and active PFC methods applied to rectification systems are introduced.

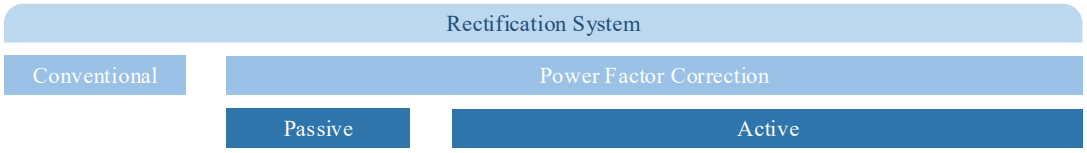


Fig. 2.8 Classification of the rectification systems.

2.3.2.1. Passive PFC rectifiers

Passive PFC rectifiers offer reliable and cost-effective solutions for those cases in which this correction is enough. In the simplest case, conventional rectification systems along with inductors, *L*, and capacitors, *C*, for filtering may be used in order to get low-complexity power factor correctors. The main advantage is the high robustness because control, sensors, or auxiliary supplies are not necessary. However, larger passive components are usually required for filtering, resulting in increased weight and volume converters. Besides, the passive filter may not respond adequately if the load power factor comes to vary. Moreover, the output voltage is not regulated and depends directly on the mains voltage level.

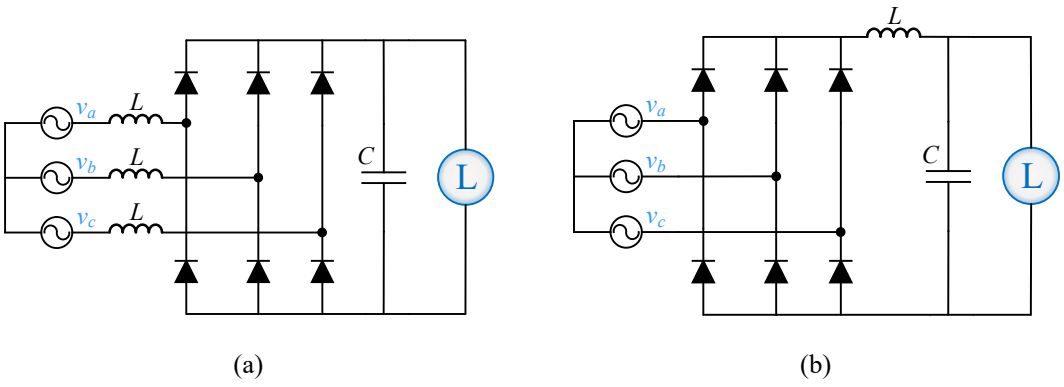


Fig. 2.9 Passive three-phase PFC rectifiers. (a) Smoothing inductor, *L*, on the ac side or (b) on the dc side.

Fig. 2.9 shows two methods of three-phase rectification using diodes with capacitive smoothing of the output voltage and inductor on the ac or dc side [107-109]. The conduction state is essentially determined by the mains line-to-line voltages, being only two diodes active carrying current at the same time. This means that each diode of the positive and negative bridge halves carries current only for one third of the mains period,

i.e. 120º. Hence, the phase currents for industrially applicable values of the smoothing inductance show 60º-wide intervals with zero current, resulting in a 30% THD_i due to the large amount of low frequency harmonic component [110, 111]. A 5% THD_i of the mains current is often required at rated power to avoid mains voltage distortion. Therefore, passive rectifier systems are usually not enough, and active power factor correctors are necessary to fulfill the mains current quality. To overcome this limitation, active PFC rectifiers offers higher performance, and they will be discussed in next subsection.

2.3.2.2. Active PFC rectifiers

Active PFC rectifies are able to reach THD_i smaller than 3% and a higher-power density, at the cost of additional semiconductor elements and a more complex control. In fact, the closed-loop operation of the static PFC power converter assures satisfactory performance with high input PF and regulated dc output voltage over a wide operating range. However, the main drawback of this rectification method is the increased complexity and a reduction in robustness in comparison with passive PFC rectification systems. Fig. 2.10 shows the classification of the active PFC rectifiers based on the topology used in the converter. These are classified as boost, buck, buck-boost, and multilevel with unidirectional and bidirectional power flows [112]. Besides, additional three-phase configurations, which are known as hybrid systems, are presented in [113-115], such as the 3rd harmonic injection systems or the combination of diode rectifier and isolated dc-dc converter systems. Moreover, ac-ac PFC converters are lately used for industrial IH applications [116-118].

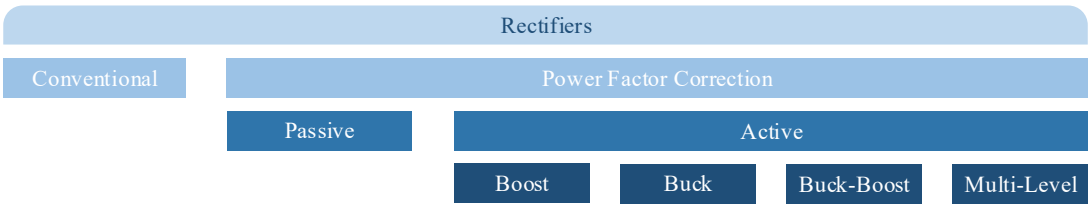


Fig. 2.10 Classification of the rectification systems, including the classification of active PFC rectifiers

- Boost rectifiers

Several issues must be taken into account to determine which type of static power converter is the most recommended for a given application, such as robustness, power density, efficiency, cost, and complexity. Within this context, numerous boost-type

topologies have been proposed in the last few years with the aim of improving the characteristics of the traditional converter used for PFC.

In Fig. 2.11 several configurations of unidirectional boost converter to improve the power quality at ac mains and dc output are shown [119-121]. These converters achieve reduced losses and higher power density by drastically reducing their weight and volume. They are composed of a diode bridge rectifier along with a step-up dc converter with filtering and energy storage elements. In the past, several alternative configurations have been proposed using the concept of interleaving and multicell implementations to improve their performance. The control of the inner current loop and dc output voltage are performed using high-frequency PWM, hysteresis current techniques, and wide-bandwidth closed-loop controllers [122-125].

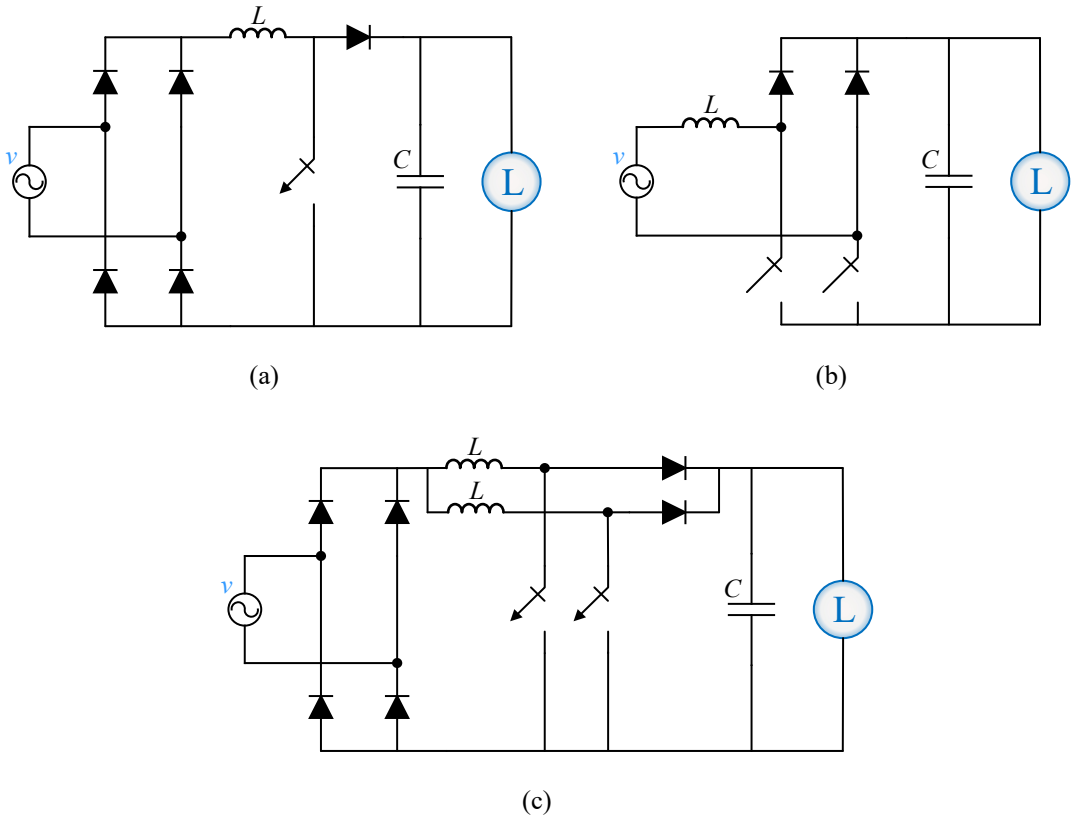


Fig. 2.11 Unidirectional PFC boost converters: (a) boost converter, (b) symmetrical two-device boost converter or totem-pole, and (c) interleaved two-cell boost converter.

The boost PFC circuit operating in continuous conduction mode is, by far, the most popular choice for medium and high power (400 W to a few kilowatts) applications. This is because the continuous nature of the boost converter input current results in low conducted electromagnetic interference compared to other active PFC topologies. These converters are extensively used in electronic ballasts, power supplies, variable-speed ac

motor drives in compressors, refrigerators, pumps, fans, etc. These converters have evolved to also enable bidirectional power flow (Fig. 2.12) in applications such as battery charging or transport.

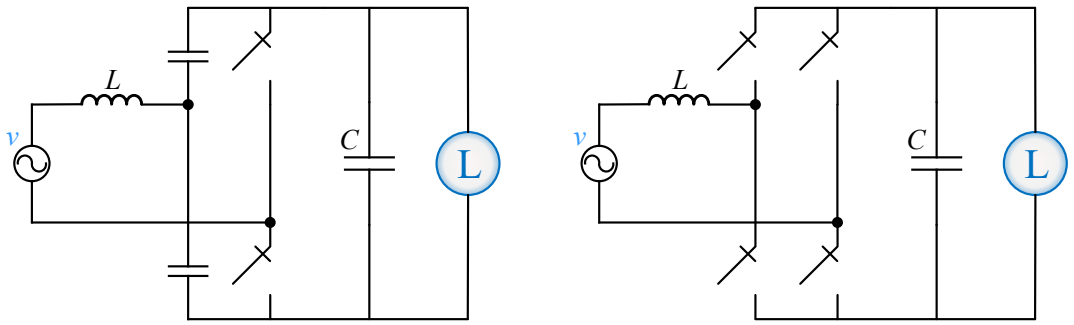


Fig. 2.12 Bidirectional PFC boost converters: (a) Half-bridge boost converter and (b) VSI full-bridge boost converter.

Three-phase systems can be derived from the single-phase boost converter by the addition of a third bridge led to the input rectifier, and moving the boost inductor to the ac side spread over the phases as is shown in Fig. 2.13. In this case, the output voltage can be controlled, but low-frequency harmonics continue to occur [126]. An improvement in the input current quality is possible by extension of the controllability using an additional power transistor as is shown in [127].

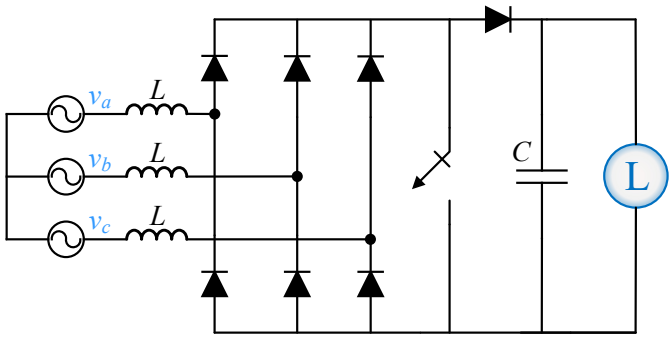


Fig. 2.13 Three-phase extension of the single-phase unidirectional PFC boost converter.

Finally, the most common topology for three-phase applications is the fully-controlled active three-phase ac-dc circuit, also known as bidirectional six-switch active PFC rectifier (Fig. 2.14). It achieves full voltage regulation and sinusoidal current, achieving a high performance despite its relatively simple structure. For this reason, the entire circuit is also available as a power module and it is widely used in industry in a wide variety of applications, such as controllable power supplies, variable speed ac machine drives, or

reactive power compensation systems. Additional boost topologies are presented in [128-131], such as Vienna rectifier or Δ-switch rectifier with significant advantages at the cost of a more complex control and implementation.

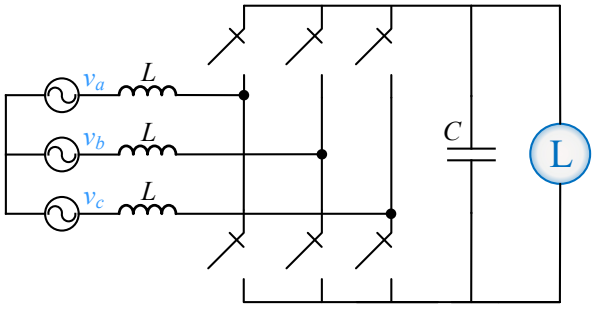
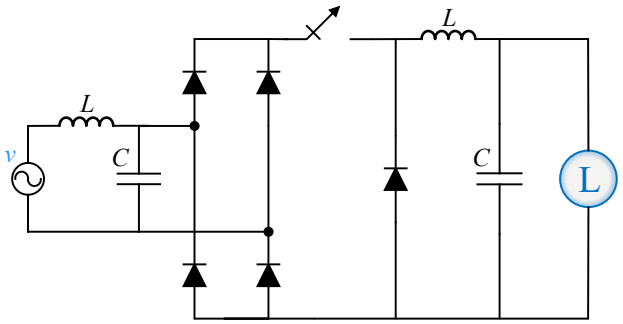


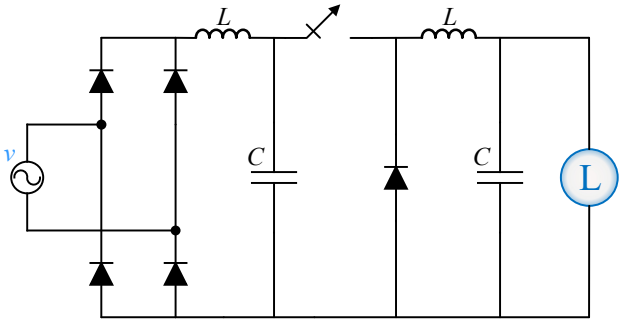
Fig. 2.14 Bidirectional six-switch active PFC rectifier.

- Buck rectifiers

The basic schematics of this topology are shown in Fig. 2.15. It consists of a diode rectifier with a step-down converter with input and output filters. Nowadays, it is also developed using a diode rectifier with filter and various combination of dc-dc converters with and without high-frequency isolation transformer. High-frequency operation reduces the size, cost, weight, and volume of transformer used for isolation. Other combinations of isolated configurations are used using forward, push-pull, half-bridge converters, etc. These topologies feature high power factor, low harmonic current in the ac mains, and meets the requirement of varying controllable output dc voltage. They are mainly used in the small-rating dc motor speed control, battery charging, isolated regulated dc supply, etc.



(a)



(b)

Fig. 2.15 Unidirectional PFC buck converter with (a) input ac filter and (b) input dc filter.

In Fig. 2.16, a typical schematic of these converters with bidirectional power flow is shown. It consists of a PWM-based current source inverter with switching devices implemented with transistors with series diodes to block the reverse voltage, or GTOs for low-frequency applications. In a large power rating application such as in traction, it is used with several series converters with transformer whereas in an isolated single-phase system with GTO to improve power quality at the input ac mains and at dc output. It may also be used in dc motor drives, battery charging, and to provide an ideal dc current source to feed current-source-inverter-based ac motor drives.

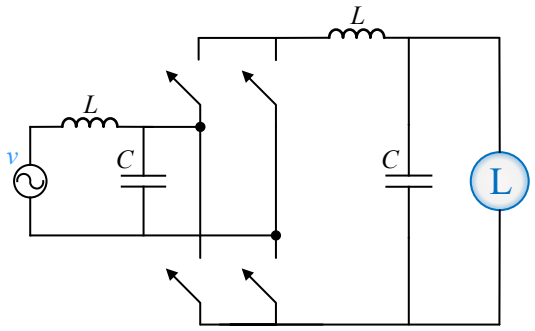


Fig. 2.16 Bidirectional PFC buck converters.

A three-phase circuit is achieved by adding a power transistor to each diode in the circuit shown in Fig. 2.9 (b). The resultant converter structure, named active six-switch buck-type PFC rectifier, is shown in Fig. 2.17 and it is very common for drive systems [132]. Other buck topologies can be found in [133], such as active three-switch buck-type PFC rectifier or Swiss rectifier.

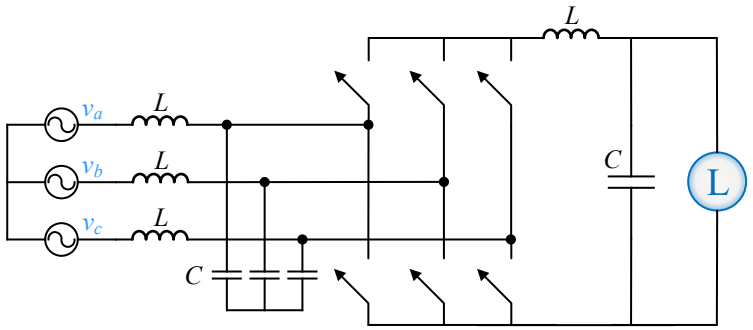


Fig. 2.17 Active six-switch buck PFC rectifier.

- Buck-boost rectifiers

Buck-boost converters are used in SMPSs, UPSs, battery chargers, small-rating brushless ac motor drives, etc. Fig. 2.18 shows two circuits with both non-isolated and isolated configurations. They are composed of a combination of diode rectifier and buck-boost dc-dc converters. Since these converters are developed in non-isolated and isolated topologies, a large number of configurations is also reported, such as the combination of buck and boost, or vice versa, buck-boost flyback, SEPIC, Zeta, Cuk, etc. These can be connected in cascade to improve power quality at the ac mains with required variable controllable output dc voltage to meet the needs of specific applications. However, high-frequency transformer isolation provides voltage adjustment for better control, safety in the load equipment, power density, reduced weight, size, loses, and better adaptability to different applications. Besides, they need only a single switch enabling regulated dc output with reduced ripple, high power factor, and low THD at the ac mains through proper control.

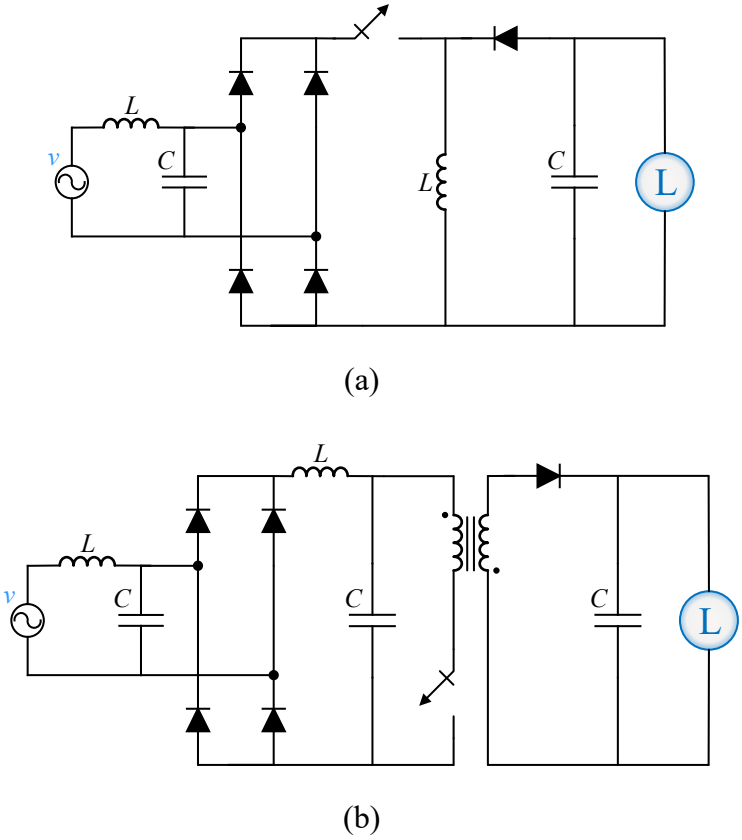


Fig. 2.18 (a) Unidirectional buck-boost converter and (b) unidirectional flyback converter.

Fig. 2.19 shows a versatile circuit that outputs variable bidirectional dc voltage and reversible current. It is quite a versatile converter with bidirectional power flow. It is a four-quadrant converter that can operate as a CSI or VSI inverter with reduced energy storage elements and has the capability of operating in buck as well as boost mode.

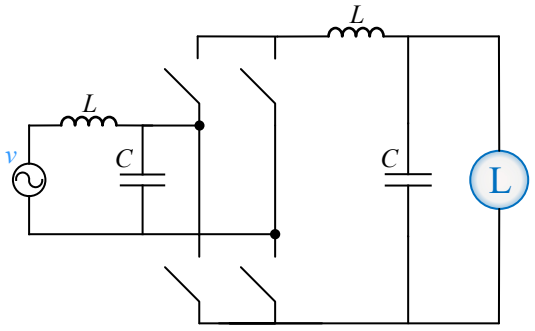


Fig. 2.19 Bidirectional buck-boost converter.

Three-phase systems with boost-type and buck-type characteristic are not common and they are implemented by the combination of buck PFC rectifier and dc-dc boost converter or vice versa. In [123], a bidirectional buck dc-dc converter comprising three

interleaved stages is presented whereas in [134] a dc-dc boost converter is implemented using the output inductor of a buck system as boost inductor.

- Multi-level rectifiers

These converters are extensively used for feeding the variable-speed drive employing brushless motors with an inverter having unidirectional power flow in applications such as air conditioning, variable speed fans, pumps, compressors, etc. Fig. 2.20 shows two examples of these type of rectifiers [135]. They are implemented using a diode rectifier with PWM control and an active bidirectional switch to reduce the harmonics. Multi-level converters provide high power factor and reduced THD of current at the ac mains input, and ripple-free regulated dc output voltage. It reduces the stress in the components and their required ratings, and provides same level of performance at reduced switching frequency, thus resulting in low switching losses and high efficiency.

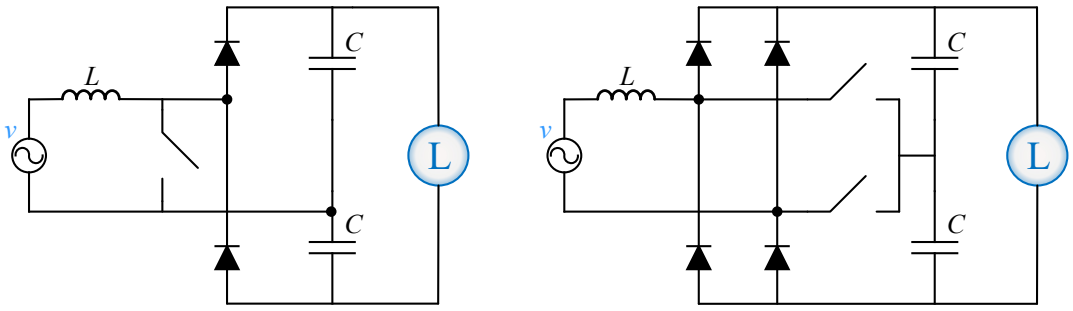


Fig. 2.20 Unidirectional multilevel converters: (a) Half-bridge multilevel converter and (b) two bidirectional-switch multilevel converter.

Additionally, a converter with bidirectional power flow is shown in Fig. 2.21. These can be classified as diode clamped, flying capacitor, and cascaded multilevel converters. These can be developed for a higher number of levels for high-voltage and high-power applications, such as battery energy storage systems, metros, traction, etc. Finally, additional three-phase structures have been proposed in different works. In [136], a three-phase multilevel hybrid switched-capacitor PFC rectifier that is suitable for high-voltage-gain applications from conventional three-phase low-voltage sources is proposed whereas in [137, 138] multi-level rectifiers using VIENNA modules are presented.

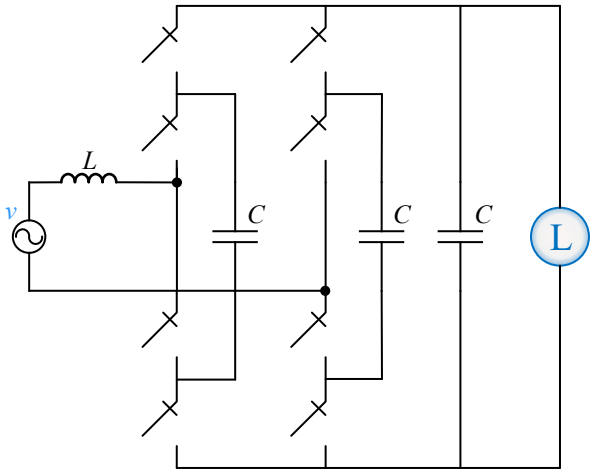


Fig. 2.21 Bidirectional flying capacitor clamped three-level converter.

2.3.3. PFC for IH applications

Using a front-end power stage that allows separating the mains from the IH inverters has been recently identified as a key research because it will allow partially overcoming the current limitations of domestic IH, obtaining a good EMC performance and avoiding the control restrictions over downstream inverters [139, 140]. Furthermore, developing a front-end stage that allows merging different mains phases in a common bus voltage will avoid the use of several isolated electronic boards as it is now, leading to a significant cost reduction among other additional advantages to domestic IH [141, 142]. Therefore, the rectification stage of the converter that is implemented using a diode bridge has to be redesign in order to fulfill all these purposes.

In the past, several works about PFC rectifiers lead to induction heating applications have been developed, focusing in the switching mode [143], the control strategy [144, 145], the topology [146, 147], or the input phases [148, 149], among other [140, 150-152]. Recently, additional efforts have been addressed in the field of industrial [116-118] and domestic IH [153, 154].

2.4. Motivation and structure of this dissertation

The research performed in this PhD dissertation has been carried out in the framework of the collaboration agreement of the Group of Power Electronics and Microelectronics (GPEM), of the “Instituto de Investigación en Ingeniería de Aragón” (I3A), and the BSH Home Appliances (BSH) Group. This collaboration was established in the early 1980s and has been continuously reinforced leading to significant industrial developments and academic results. Since the beginning of domestic IH technology, six different IH

appliance generations have been developed and put into the market. The research performed in this dissertation is aimed at improving the performance of subsequent IH appliance generations.

2.4.1. Motivation

As it has been previously discussed in these introductory chapters, the electronic design requirements of domestic IH are becoming more challenging. Higher efficiency due to environmental concerns and temperature limitations. Higher output power in order to supply bigger IH loads. Higher power density because of space limitations. Improved EMC performance and low cost to fulfill international standards and get a competitive product. Besides, the possibility of addressing different mains connections achieving a good power quality converter are essential requirements. Therefore, in order to face these challenges, the use of PFC converters is desirable.

Nowadays, PFC rectifiers have rarely been implemented in commercial IH home appliances due to complexity and cost issues. However, advances in power electronics and control, as well as the trend towards higher performance appliances motivates the proposed approach. Besides, a multi-phase PFC rectifier is also interesting, since it allows delivering higher output power compared with current state-of-the-art implementations and merging different main phases in a common bus voltage, leading to a potential cost reduction. Moreover, it introduces additional control options, what is a major advantage, especially in multi-load cases, since it improves the output power managing.

2.4.2. Goal definition

The main purpose of this research is to investigate the use of PFC rectifiers for domestic IH and to propose a suitable solution for single-phase and multi-phase applications. In order to achieve this aim, different topologies are introduced, their control strategies are analyzed, and experimental implementations are designed and built. Finally, a discussion is provided to present the main advantages and disadvantages of this approach and its implementation in the current IH technology.

2.4.3. Scope of the thesis

The following steps will be considered in this thesis to accomplish the defined goal:

- Proposal of PFC topology

Having into account the state of the art and the main advantages and disadvantages of the different type of PFC rectifiers, a single-phase topology and a multi-phase topology will be proposed. These proposals will offer a high versatility in order to perform an in-depth analysis of the operation feasibility and its application to domestic IH.

- Analysis of Modulation strategies

A complete set of modulation strategies will be proposed for the single-phase and multi-phase topologies. The control methods for its implementation will be analyzed and developed, taking into account the measurements systems, the control devices, and the fulfillment of EMC standards of power quality regarding the mains behavior of the PFC rectifier.

- Experimental implementation

Each topology will be implemented experimentally considering different features such as the switching technology, magnetic devices, or measurement systems. These prototypes will be versatile platforms to allow developing each modulation strategy, getting experimental measurements, and testing the proper operation of the converters.

- Discussion and conclusions

The experimental measurements with every modulation strategy will allow conclusions to be drawn and key figures of merit to be compared. It will provide the required information in order to analyze the advantages and disadvantages of each proposal and its application to domestic IH.

2.4.4. Report structure

This document is divided into seven Chapters. In the first Chapter, the domestic induction heating application has been presented, whereas in Chapter 2 the concept of power quality has been discussed, and a review of the state-of-the-art PFC rectifiers has also been performed.

Chapter 3 presents and describes the proposed topologies for IH with single-phase and multi-phase applications, whereas Chapter 4 proposes and analyses different modulation

strategies to control the proposed converters. In Chapter 5, the experimental implementation of the PFC rectifiers and its modulations strategies are described, and the main results are presented. Besides, the implementation of a controllable three-phase power supply that has been developed to supply the experimental prototypes is summarized.

Chapter 6 provides discussion regarding the advantages of the proposed approach for the domestic IH applications. Finally, the main conclusions of this dissertation are outlined in Chapter 7.

Chapter 3

PFC Topologies

Even though PFC rectifiers have rarely implemented in commercial IH home appliances due to complexity and cost issues, advance in power electronics and control as well as the trend towards higher performance appliances motivates the development of such systems. In this Chapter, a multi-phase and a single-phase boost active PFC rectifier topologies are proposed, and their main advantages are presented.

Contents

3. PFC Topologies

PFC rectifiers have rarely been implemented in commercial IH home appliances due to complexity and cost issues [139, 155]. However, advances in power electronics and control, as well as the trend towards higher performance appliances justifies the development of such systems. Besides, technology of wide band gap (WBG) devices have significantly improved, decreasing the cost of such devices.

3.1. Boost active PFC topologies

3.1.1. Motivation for the use of boost active PFC topologies

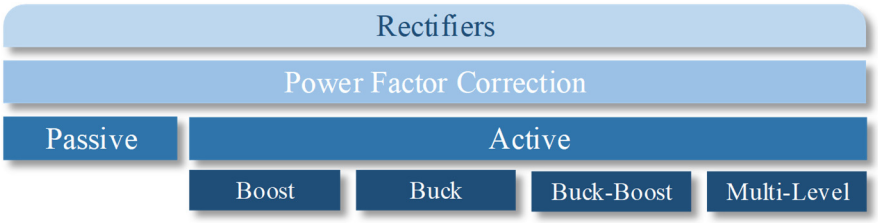
In the previous Chapter, different passive and active topologies have been presented. Passive PFC rectifiers are simpler and do not need controlled elements. However, larger magnetic components are usually required for filtering, and they are not able to reach current harmonic distortion, THD_i, smaller than 30% due to the large amount of low frequency harmonic components. Moreover, these rectifiers are not suitable because IH loads are non-linear loads since they depend of the excitation voltage. For these reasons, to fulfil the EMC standards required for IH appliances, it is proposed to use active PFC rectifiers because they can reach THD_i smaller than 3% and high power density, at the cost of a more complex control and higher devices count.

Active PFC rectifiers can be classified in boost, buck, buck-boost, and multi-level converters. As it has been previously discussed, boost-type rectifiers operating in continuous conduction mode are by far the most popular choice for medium-power applications because of the continuous nature of the boost converter input current, which results in low conducted electromagnetic interference compared to other active PFC topologies. Besides, they are especially interesting in the IH field because they allow to improve the efficiency in the back-end IH inverter.

TABLE 3.1 shows a comparative analysis of the different PFC rectifier topologies discussed. Several relevant parameters for the IH converter have been considered. These parameters give qualitative information of the behavior of the rectifier from the point of view of the energy quality, the back-end IH inverter, the bus voltage, the controllability, the components, and the cost.

TABLE 3.1

COMPARATIVE QUALITATIVE ANALYSIS OF PFC RECTIFIERS



THD$_i$	⊖	↑	↑	↑	↑
PF	⊖	↑	↑	↑	↑
IH output power	⊖	↑	↑	↑	↑
IH inverter efficiency	⊖	↑	↓	⊖	↑
Controllability	↓	↑	↑	⊖	⊖
Device voltage	⊖	↓	⊖	↓	↑
Device number	↑	⊖	⊖	⊖	↓
Bus voltage ripple	⊖	↑	↑	↑	↑
Controllable bus voltage	↓	↑	↑	↑	↑
Bus voltage range	↓	⊖	⊖	↑	⊖
Cost	↑	⊖	⊖	⊖	↓
Complexity	↑	⊖	⊖	⊖	↓

In the following lines, the main reasons for implementing a single-phase boost active PFC rectifier for domestic IH as front-end stage are listed. Firstly, EMC issues are isolated from the IH converter design, decreasing the filter size, avoiding the use of complex jitter strategies or control strategies when non-linear loads are powered [156], and avoiding

flicker restrictions. Secondly, the IH control system is improved because of the lack of flicker restrictions and the variable bus voltage, allowing an easier and more accurate power control in several IH-load scenarios, enabling also the operation closer to the resonant frequencies and, consequently, improving the IH inverter efficiency. Finally, the higher the bus voltage is, the lower the required current through the switching devices and coils is, consequently decreasing the conduction losses. The inherent higher and low-ripple bus voltage of the proposed systems enables also a better usage of the switching devices, leading to potential cost reductions and improved reliability and efficiency in the inverter stage.

As previously discussed in Chapter 2, higher performance IH cooktops are usually composed of two isolated electronic boards to be powered from two mains phases in certain regions, where the maximum phase current in domestic installations is typically limited to 16 A. However, there are different installation limitations in other regions where only a single-phase mains connection exists, but limited to 25 A, or areas where three-phase mains connections can be used. In this context, developing a front-end stage that allows merging different mains phase configurations in a common bus voltage has been identified as a key research line [142].

More specifically, a multi-phase PFC approach provides significant advantages to domestic IH [142, 157], not only the first fundamental benefit previously discussed, but also the following additional advantages. Firstly, higher power can be delivered to the pots, e.g. typically 3.6 kW systems can be easily rescaled to 11 kW, decreasing significantly the heating times in bigger pots. Secondly, the control hardware can be also simplified, i.e. a single control unit is able to control both the PFC stage and the multi-phase outputs, avoiding isolated measurement requirements and auxiliary power supplies for each phase. Finally, power coupling issues [158-160] between different mains phases when multiple inductors are activated in multi-coil IH systems are avoided because a single inductor or a set of inductors can be powered from several mains phases using a common bus.

TABLE 3.2 shows a comparative analysis of the current implementation of a domestic IH converter using a bridge rectifier along with filtering elements, and the proposed implementation for single-phase and multi-phase cases using boost active PFC rectifiers. Several relevant parameters have been discussed to provide qualitative information of the performance of the rectifier from the point of view of the energy quality, the back-end IH

inverter, the bus voltage, the controllability, the components, and the cost. All these benefits motivate and justify this research and the proposal of a front-end PFC stage. Moreover, both single-phase converters and multi-phase converters are interesting for domestic IH due to the advantages they bring. Therefore, this dissertation analyses both cases independently in terms of topologies and modulation strategies.

TABLE 3.2

COMPARATIVE QUALITATIVE ANALYSIS OF CURRENT PASSIVE RECTIFIERS, AND SINGLE-PHASE AND MULTI-PHASE BOOST ACTIVE RECTIFIERS FOR DOMESTIC IH CONVERTERS

	Domestic IH rectifiers		
	Current	Proposed	
	Passive	Boost active	
	Single-phase	Single-phase	Multi-phase
THD$_i$			
PF			
IH output power			
IH inverter efficiency			
Controllability			
Device voltage			
Device number			
Bus voltage ripple			
Controllable bus voltage			
Bus voltage range			
Cost			

Taking into account that the use of boost PFC rectifiers has been selected for performing the power factor correction, the principles of the boost topologies are explored below using the typical boost topology. Therefore, the main waveforms, the configuration sequence, and the main equations are analyzed.

3.1.2. Principles of the boost topology

Fig. 3.1 shows a typical dc-dc boost converter. It is composed of an inductor, L_b, an output capacitor, C_b, a diode, D, and a unidirectional and unipolar switching device, S. Finally, a load is considered that is modeled as a resistance, R_o.

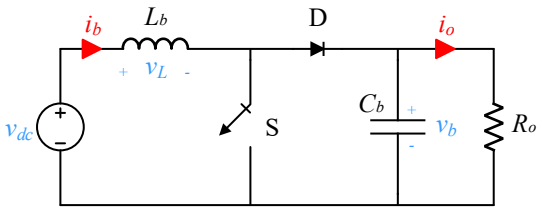


Fig. 3.1 Dc-dc boost converter.

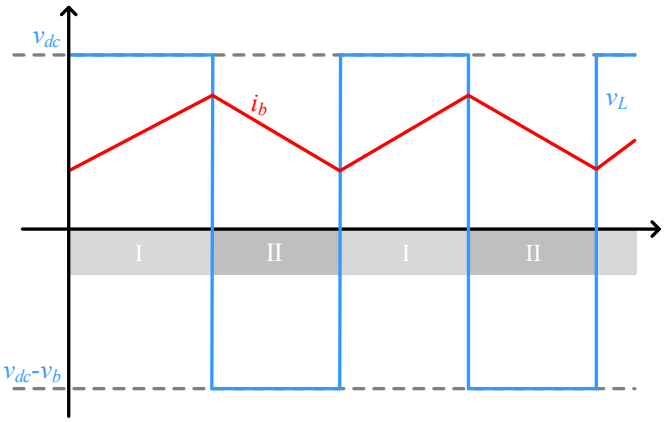


Fig. 3.2 Inductor waveforms of the dc-dc boost converter.

The main inductor current and voltage waveforms according to the activation state of the switching device are shown in Fig. 3.2, considering a continuous conduction mode operation, whereas the configuration sequence of the converter is shown in Fig. 3.3. When the switch is activated (state I), the supply voltage, v_{dc}, is applied to the inductor, increasing the current, i_b, that flows through it, accumulating magnetic energy. In this situation, the diode is deactivated and blocks the capacitor voltage, also known as bus voltage, v_b. At the state II the switch is deactivated, and the inductor current flows through the diode, supplying energy to the capacitor and the load. As a result, the magnetic energy

stored in the inductor is transferred to the capacitor as electric field energy, increasing its voltage.

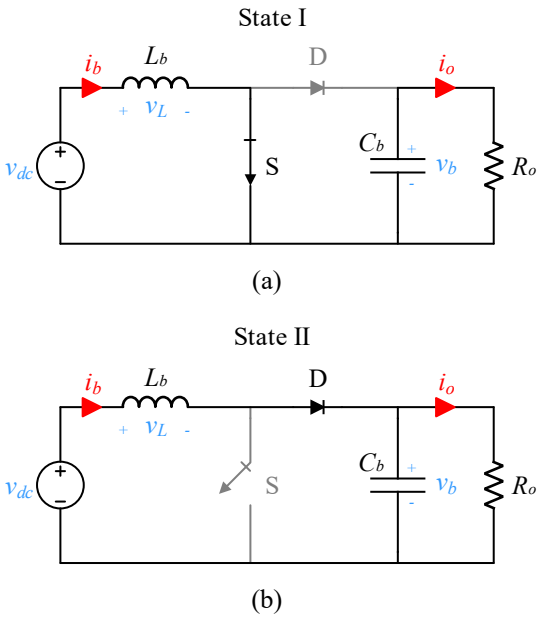


Fig. 3.3 Configuration sequence of the dc-dc boost converter with (a) the switching device, S, activated (state I) and (b) deactivated (state II).

The typical control strategy of the boost converter is based on modulating at constant switching frequency, f_{sw}, and variable duty cycle, D. The inductance, current ripple, and capacitor value are determined by the switching frequency that is commonly a design parameter. However, the duty cycle depends on the supply voltage and the desired output voltage. The inductor voltage according the activation state is defined as follows

$$v_L = \begin{cases} v_{dc}, & \text{state: I} \\ v_{dc} - v_b, & \text{state: II} \end{cases}. \tag{3.1}$$

The mean voltage of an inductor, V_L, is null in a stationary state. The duty cycle is defined as the proportional time of the period, T_{sw}, which the switching device is activated, and it is a value between 0 and 1. Taking this into account, and the boost-inductor average voltage in state I, $\langle v_L \rangle_{\text{I}}$, and the boost-inductor average voltage in state II, $\langle v_L \rangle_{\text{II}}$, the next equation can be formulated

$$D\langle v_L \rangle_{\text{I}} + (1-D)\langle v_L \rangle_{\text{II}} = 0, \tag{3.2}$$

and using (3.1)

$$Dv_{dc} + (1-D)(v_{dc} - v_b) = 0. \tag{3.3}$$

Finally, the relation between the bus voltage, v_b, and the supply voltage, v_{dc}, is defined in function of the duty cycle as

$$\frac{v_b}{v_{dc}} = \frac{1}{1-D}. \tag{3.4}$$

3.2. Single-phase PFC rectifier

The proposed single-phase PFC rectifier is shown in Fig. 3.4. It has been selected due to its versatility and its ability to implement different configurations and modulation strategies. It is based on the boost converter, and it is composed of two half-bridge legs, *a* and *b*, which allow short-circuiting the boost inductor, L_b, with the mains voltage, v_{ac} (T_{ac} period), and/or the dc bus voltage, v_b. Each half-bridge is composed of two switching devices, S_h and S_l, implemented with MOSFETs, T_h and T_l, and antiparallel diodes, D_h and D_l. A filter between the mains and the PFC stage is placed, supplying the medium frequency currents and removing the high ripple of the boost coil current, i_b. In this way, a fully filtered input current, i_{ac}, is achieved in the switching period $T_{sw} << T_{ac}$. In the proposed implementation, an inductor, L_f, and a capacitor, C_f, for filtering are used. Besides, a capacitor, C_b, filters the bus voltage and serves as a power storage, which powers the IH-inverter. In this case a multi-output inverter is represented and the set of IH inverters is composed of as many half-bridge branches, $S_{h,n}$ and $S_{l,n}$, as IH-loads. Each IH-load is composed of the equivalent series resistance, $R_{eq,n}$, and inductance, $L_{eq,n}$, and the split resonant capacitor, $C_{r,n}$.

The main advantage of the proposed bridge topology of the PFC converter is that it allows implementing several topological configurations: half bridge (HF), full bridge (FB), or a combination of both, i.e. hybrid (H), and, therefore, each of them can be analyzed.

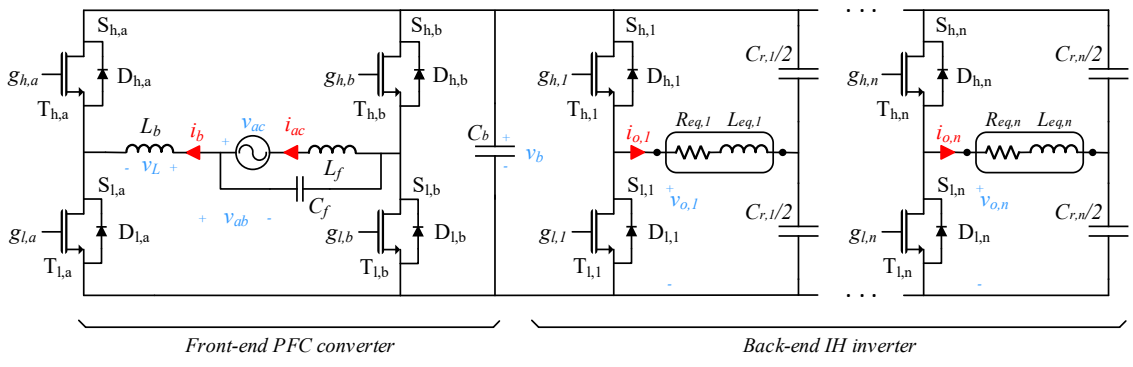


Fig. 3.4 Single-phase PFC converter powering a multi-output IH inverter with *n* loads.

3.2.1. Half-Bridge configuration

In the half-bridge configuration, the *a* branch is activated with T_{sw} period, while the *b* branch is activated with T_{ac} period to get synchronous rectification. The main advantage of this configuration is that the switching device count is reduced. However, the main disadvantage is that the i_b current control close to the mains-voltage zero-crossing becomes difficult. In this case, the mains voltage is null (v_{ac}=0) while the bus capacitor is fully charged, leading to extreme duty cycles and zero-crossing distortion when the duty cycle is limited.

Fig. 3.5 and Fig. 3.6 show the main waveforms of the boost inductor of the PFC converter and the activation states using half-bridge configuration with positive and negative mains voltage, respectively. Fig. 3.7 and Fig. 3.8 show the configuration sequence of the same situation for positive and negative mains voltage too. In this case, the *a* branch is modulating at switching frequency whereas *b* branch is modulated at mains frequency in order to get synchronous rectification.

In order to shorten the configuration sequence, the filtering elements have been disregarded. It is important to remark also that the MOSFET can and should be activated instead of the diode in order to activate the channel of the transistor and decrease conduction losses. To represent both situations, in the *b* branch the transistor is activated whereas in the *a* branch the diode is activated. Besides, the IH-inverter is simplified and modeled as a resistive load, R_o. The antiparallel diodes of the switching devices allow inverse current. For this reason, the configuration sequence has been drawn considering the situation when the inductor current becomes negative.

The half-bridge configuration can be operated in different continuous conduction mode (CCM) as it will see in later chapters. However, they are equivalent from the point of view of the main equations describing the circuit operation. The boost-inductor voltage, v_L, depends on the mains voltage polarity as follows

$$v_L = \begin{cases} v_{ac}, & \text{state: I and II,} \\ v_{ac} - v_b, & \text{state: III and IV,} \\ v_{ac} + v_b, & \text{state: V and VI,} \\ v_{ac}, & \text{state: VII and VIII,} \end{cases} \quad \begin{matrix} v_{ac} > 0 \\ \\ \\ v_{ac} < 0 \end{matrix} . \tag{3.5}$$

Following the same procedure used in (3.2), the duty cycle, D, using a CCM conduction mode is obtained according the mains voltage sign as follows

$$D = \begin{cases} \dfrac{v_b - v_{ac}}{v_b}, & v_{ac} > 0 \\ -\dfrac{v_{ac}}{v_b}, & v_{ac} < 0 \end{cases}. \tag{3.6}$$

In this case, the duty cycle is defined as the proportional time of the period, T_{sw}, where the low-side switching device, $S_{l,a}$, is activated.

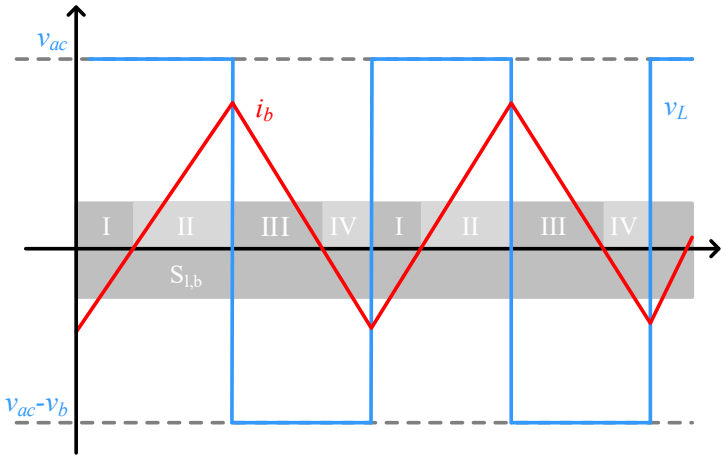


Fig. 3.5 Inductor current and voltage waveforms and activation states of the PFC converter operating in half-bridge configuration in a positive cycle of the mains voltage v_{ac}.

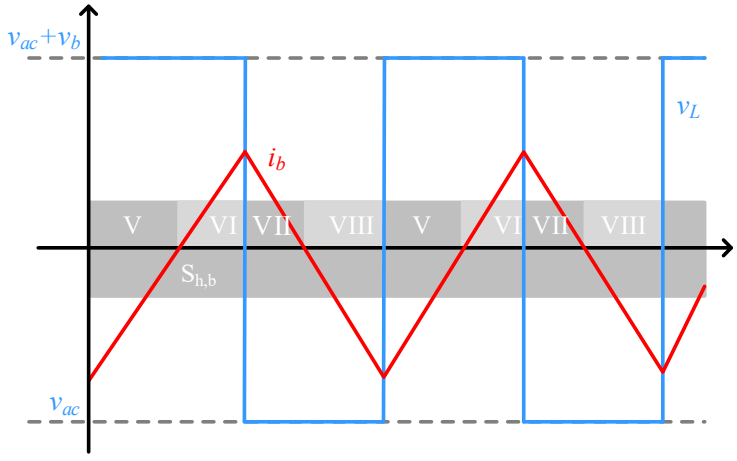


Fig. 3.6 Inductor current and voltage waveforms and activation states of the PFC converter operating in half-bridge configuration in a negative cycle of the mains voltage v_{ac}.

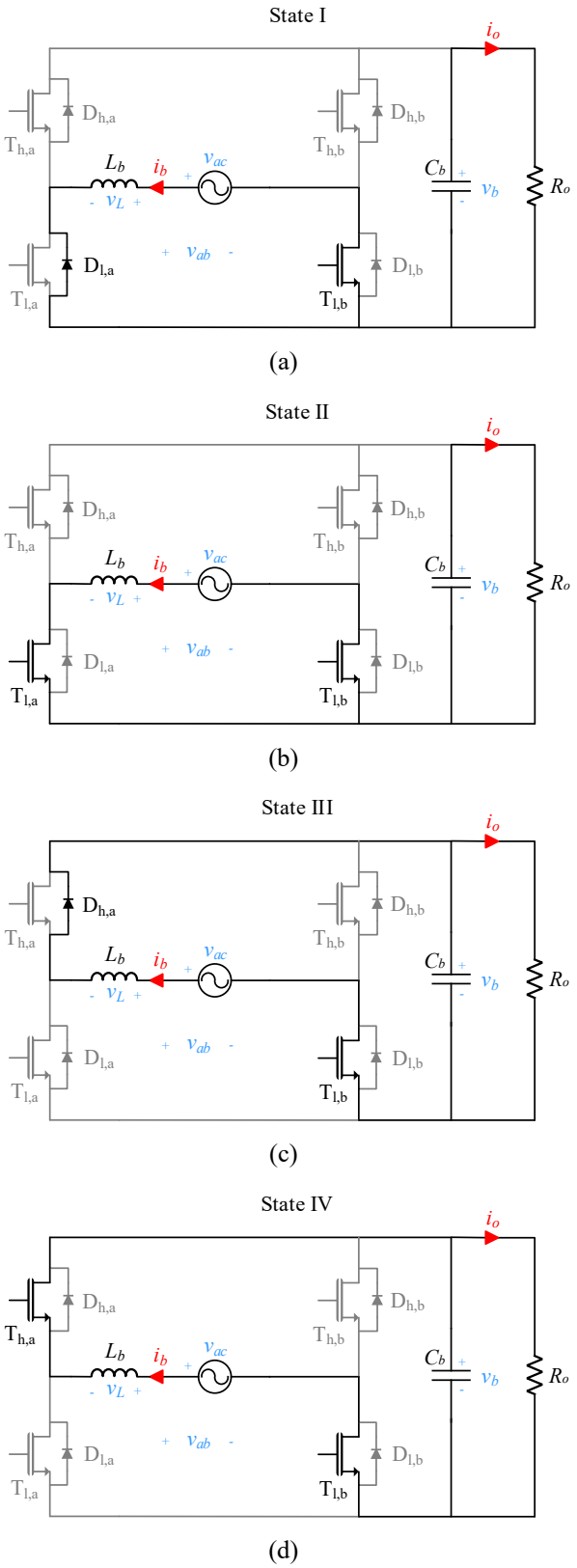


Fig. 3.7 Configuration sequence of the PFC converter operating in half-bridge configuration in a positive cycle of the mains voltage, v_{ac}, and powering a resistive load, R_o. (a) state I, (b) state II, (c) state III, and finally, (d) state IV. In this representation, the MOSFET, $T_{l,b}$, has been activated instead of the diode, $D_{l,b}$, in order to decrease the conduction losses.

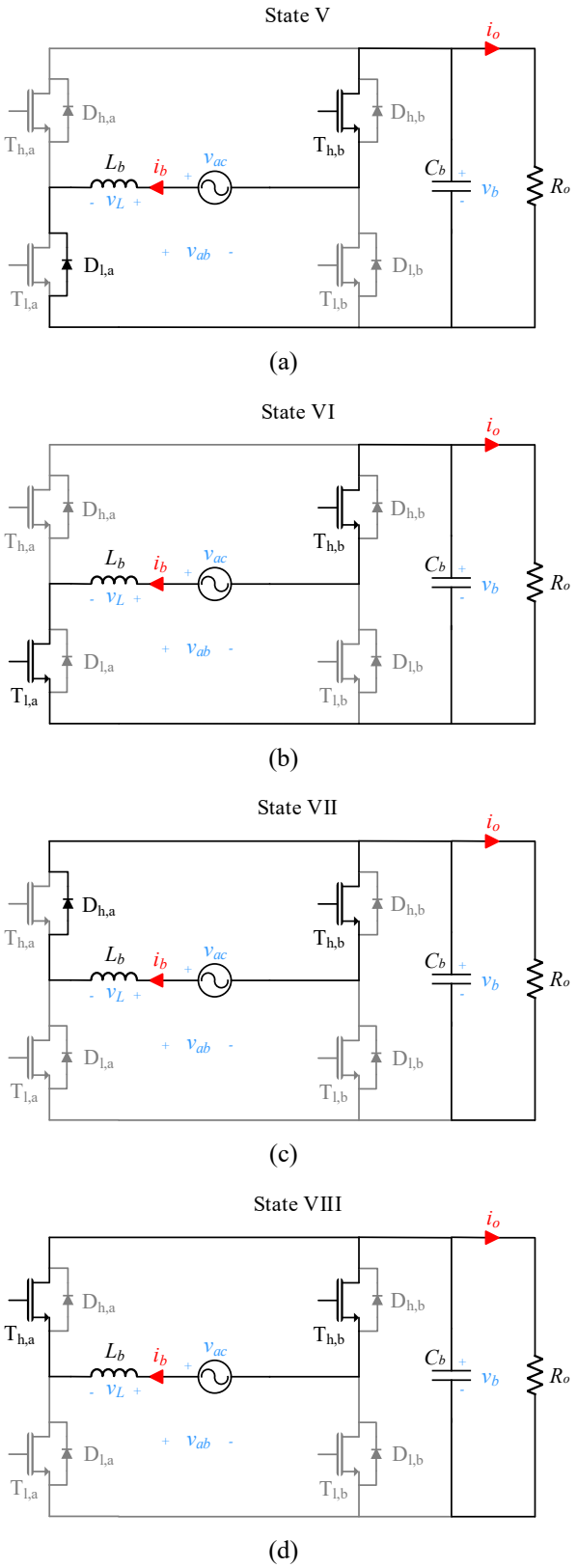


Fig. 3.8 Configuration sequence of the PFC converter operating in half-bridge configuration in a negative cycle of the mains voltage, v_{ac}, and powering a resistive load, R_o. (a) state V, (b) state VI, (c) state VII, and finally, (d) state VIII. In this representation, the MOSFET, $T_{h,b}$, has been activated instead of the diode, $D_{h,b}$, in order to decrease the conduction losses.

3.2.2. Full-Bridge configuration

The second approach is based on using the two inverter branches of the PFC converter phase-shifted 180º and complementary duty cycles. In this way, both branches are activated at T_{sw}. The main advantage of this strategy is that zero-cross distortion is avoided. However, the number of switching devices operating at high frequency is higher, increasing switching losses. Besides, the voltage applied to the boost inductor is also higher because the bus voltage is always applied to the boost inductor, increasing the current ripple and, therefore, increasing conduction losses in the boost inductor and the switching devices. As a consequence, this approach leads to lower efficiency results. Fig. 3.9 shows the boost-inductor waveforms using this implementation whereas Fig. 3.10 shows the configuration sequence.

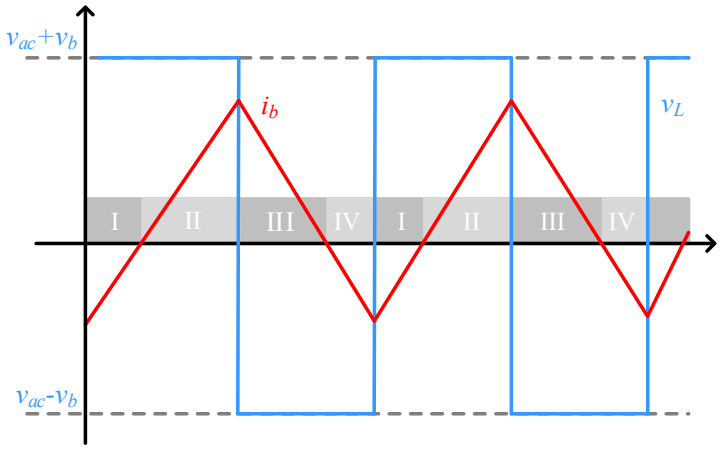


Fig. 3.9 Inductor waveforms and activation states of the PFC converter operating in full-bridge configuration.

At state I and state II, a positive voltage is applied to the boost inductor because $S_{l,a}$ and $S_{h,b}$ are activated, whereas at state III and state IV, $S_{h,a}$ and $S_{l,b}$ switches are activated, getting a negative voltage. Therefore, the boost-inductor voltage, v_b, results as a function of the activation states as

$$v_L = \begin{cases} v_{ac} + v_b, & \text{state: I and II} \\ v_{ac} - v_b, & \text{state: III and IV} \end{cases}. \tag{3.7}$$

In this case, the duty cycle does not depend on the mains voltage sign and its values are less extreme than in the half-bridge modulation, being 0.5 in the mains voltage zero crossing (v_{ac}=0) and, consequently, easing the control. For each branch, the duty cycle in a CCM conduction mode is defined as

$$\begin{aligned} D_a &= \frac{1}{2}\left(1 - \frac{v_{ac}}{v_b}\right). \\ D_b &= \frac{1}{2}\left(1 + \frac{v_{ac}}{v_b}\right). \end{aligned} \tag{3.8}$$

Being D_a and D_b the proportional time of the period, T_{sw}, which the low-side switching device is activated, $S_{l,a}$ and $S_{l,b}$ respectively.

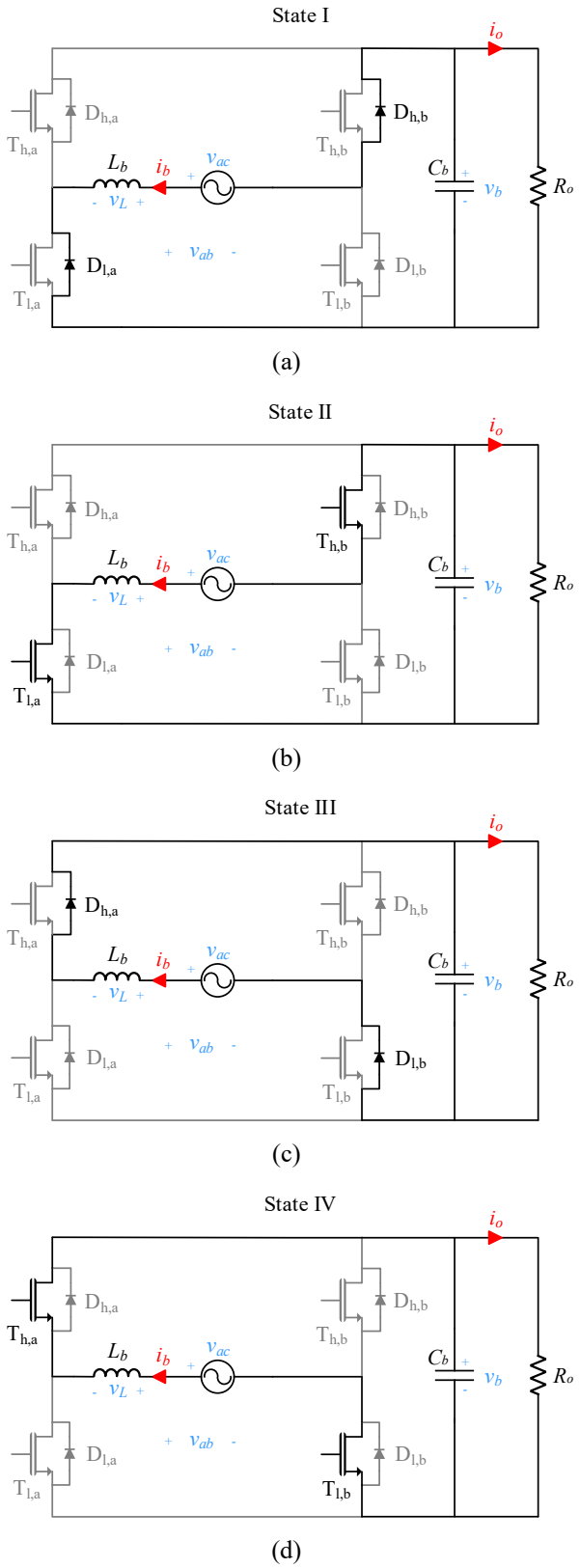


Fig. 3.10 Configuration sequence of the PFC converter operating in full-bridge configuration and powering a resistive load, R_o. (a) state I, (b) state II, (c) state III, and finally, (d) state IV.

3.2.3. Hybrid configuration

In order to improve both the efficiency and the zero-cross distortion, a combined approach is proposed. It is based on using the half-bridge configuration and changing to the full-bridge configuration close to the zero crossing. In this way, the distortion is eliminated getting an improved efficiency at the cost of additional control complexity in tradeoff with the full-bridge configuration. The combination of the two configurations slightly decreases the efficiency in comparison with the half-bridge configuration. However, it avoids the zero-cross distortion, achieving a good balance between efficiency and EMC performance. Fig. 3.11 shows the main differences in the voltage and current waveforms using each topology configuration.

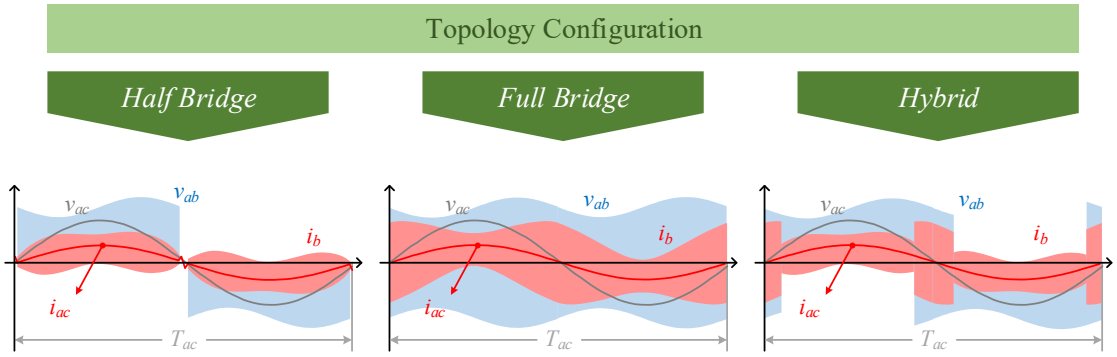


Fig. 3.11 Main current and voltage waveforms using half-bridge, full-bridge, and hybrid configuration.

3.3. Multi-phase PFC rectifier

The proposed multi-phase topology is shown in Fig. 3.12 and it is composed of (n+1) half-bridge branches, being n the maximum phase number. Each half-bridge branch is composed of two switching devices implemented with MOSFETs, $S_{h,i}$ on the high side, and $S_{l,i}$ on the low side, $i \in [0, n]$. The boost inductor, L_i, is short-circuited with the mains phase voltage, $v_{ac,i}$, $i \in [1, n]$, the voltage of middle point of the split bus capacitor, v_0, and the bus voltage, v_b, to control the mains phase current, i_i. A filter composed of a filter inductor, $L_{f,i}$, and a filter capacitor, $C_{f,i}$, supplies the medium frequency currents, removing the high frequency ripple of the boost-inductor current, $i_{L,i}$. Besides, the split capacitor, C_b, filters the bus voltage. The additional half-bridge branch assures that the split capacitor is well-balanced using the balancing inductor, L_0, and provides a return path to the mains phase current when then mains connection is not balanced, i.e. single-phase or two-phase connection.

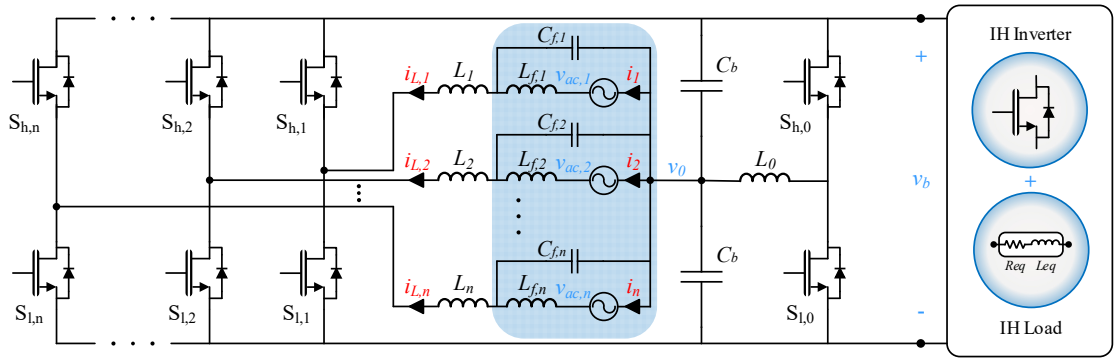


Fig. 3.12 Topology of a multi-phase PFC rectifier with *n* phases based on the boost topology. The proposed topology can work with 1, 2, or *n* activated phases. A balancing branch provides a return path to the input current when the mains currents are not balanced and adjust the voltage of the split bus capacitor. The bus voltage, v_b, is the output of the converter used to power back-end converters, e.g. IH inverters.

The phase peak voltage, $V_{ac,i,p}$, must fulfill the below equations to avoid uncontrolled current flowing through the antiparallel diodes of the switches, assuring the converter controllability.

$$V_{ac,i,p} < v_0, \tag{3.9}$$

$$V_{ac,i,p} < v_b - v_0. \tag{3.10}$$

The balancing branch is operated at frequency, $f_{sw,0}$, and duty cycle, D_0, to get a proper voltage in the middle point of the split bus capacitor.

In order to assure a smooth phase current, i_i, the operating frequency of the switching devices, $f_{sw,i}$, is higher than the filter cut-off frequency, $f_{c,i}$, and it is higher than the mains frequency, $f_{ac,i}$,

$$f_{sw,i} >> f_{c,i} \simeq f_{ac,i}. \tag{3.11}$$

Besides, this assumption allows disregarding the filtering components, $L_{f,i}$ and $C_{f,i}$, simplifying the circuital analysis.

Fig. 3.13 shows the main waveforms of the boost inductor of the *i*-branch of the multi-phase PFC converter and Fig. 3.14 shows the configuration sequence. In order to simplify the analysis, a unique branch powering the bus has been considered, and it is assumed that the bus capacitors, C_b, are higher enough to avoid the voltage change in a term and disregard the balancing branch. As in the previous cases, the IH-inverter is modeled as a resistive load, R_o.

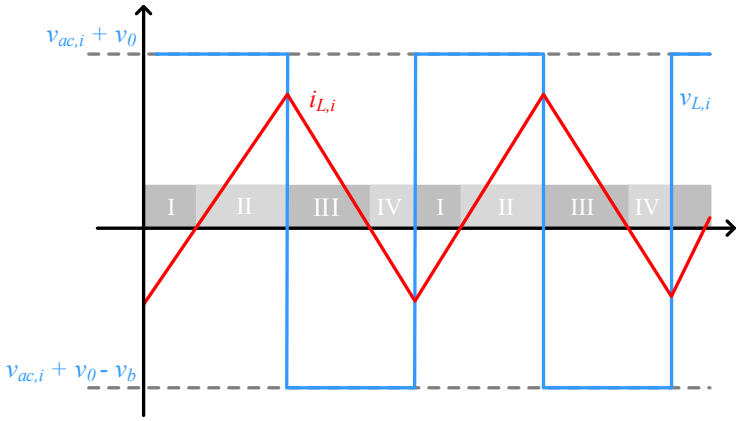


Fig. 3.13 Inductor waveforms and activation states of the *i*-branch of the multi-phase PFC converter.

The boost-inductor voltage, $v_{L,i}$, can be defined according the state of the switching devices as

$$v_{L,i} = \begin{cases} v_{ac,i} + v_0, & \text{state: I and II} \\ v_{ac,i} + v_0 - v_b, & \text{state: III and IV} \end{cases}, \tag{3.12}$$

when (3.9), (3.10), and (3.11) are fulfilled. Being the low-side switching device, $S_{l,i}$, the first one to be activated. Thereby, the duty cycle of the *i*-branch, D_i, is calculated as

$$D_i = \frac{v_b - v_0 - v_{ac,i}}{v_b}. \tag{3.13}$$

In this way, the current through the boost inductor, $i_{L,i}$, and therefore the mains phase current, i_i, can be controlled.

A solution to control the balancing branch of the multi-phase PFC converter is based on modulating it at constant frequency and 50% duty cycle in order to obtain half the bus voltage in the middle point of the split bus capacitor

$$v_0 = \frac{v_b}{2}. \tag{3.14}$$

As a result, in this case the voltage of the boost inductor is obtained as

$$v_{L,i} = \begin{cases} v_{ac,i} + \dfrac{v_b}{2}, & \text{state: I and II} \\ v_{ac,i} - \dfrac{v_b}{2}, & \text{state: III and IV} \end{cases}, \tag{3.15}$$

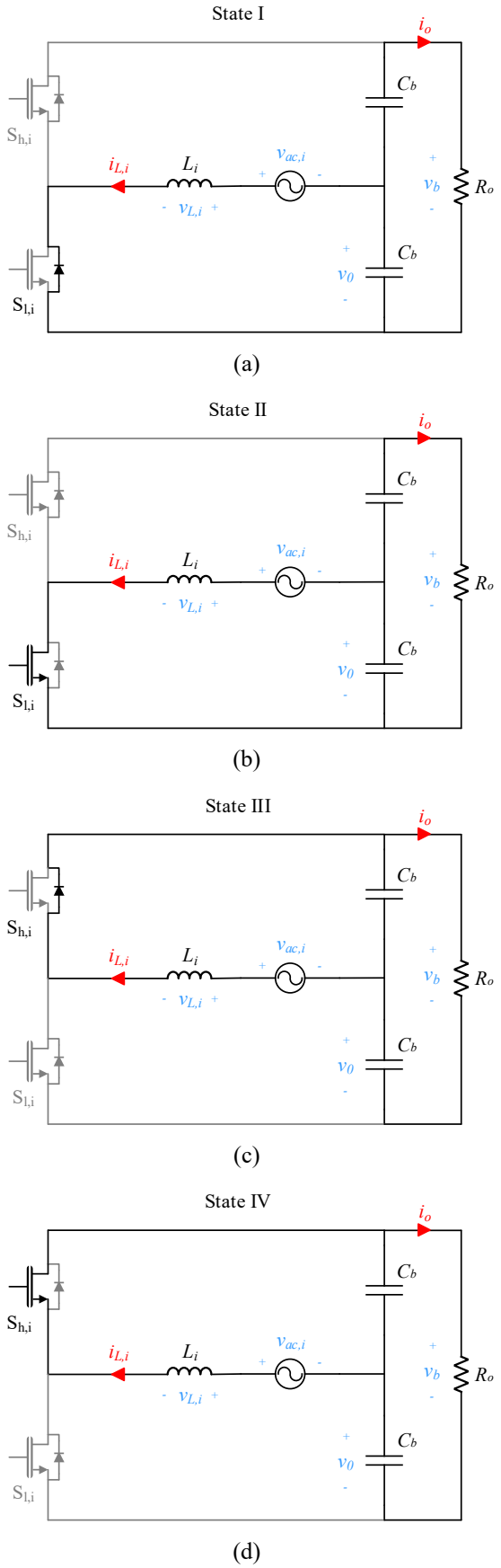


Fig. 3.14 Configuration sequence of the *i*-branch of the multi-phase PFC converter powering a resistive load, R_o: (a) state I, (b) state II, (c) state III, and finally, (d) state IV.

and the duty cycle is

$$D_i = \frac{1}{2}\left(1 - \frac{2v_{ac,i}}{v_b}\right). \tag{3.16}$$

It can be appreciated that, in comparison with (3.7) and (3.8), this topology with split bus capacitor and the proposed branch balancing modulation behaves as a full-bridge topology with half the bus voltage. As a result, it is concluded that the modulation strategies used for controlling bridge topologies of the single-phase PFC converter can be applied in this case.

Chapter 4

PFC Modulation Strategies

The PFC function can be performed using several modulation strategies. Each one of these has different advantages and disadvantages that can encourage or make more challenging its implementation. In this Chapter, the modulation strategies that allow controlling the proposed single-phase and multi-phase topologies are discussed.

Contents

4. PFC Modulation Strategies

In order to perform the PFC function, different modulation strategies can be implemented [161-170]. However, each one of these strategies has some advantages and disadvantages that can encourage or complicate its implementation according to the application area, control complexity, cost, device ratings, efficiency, EMC issues, or the operating frequency. Consequently, this Chapter performs a detailed analysis of these modulation strategies and introduces new approaches with the aim of finding a good balance between cost, efficiency and power density to obtain an effective implementation.

4.1. Single-phase PFC modulation strategies

4.1.1. Operation modes

The proposed single-phase topology enables the converter operation under different modulation strategies that can be classified according to the following elements: the conduction mode: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM); the switching frequency: Fixed Frequency (FF) or Variable Frequency (VF); and the switching mode: Zero Voltage Switching (ZVS) or Hard Switching (HS). Fig. 4.1 shows a classification of these modulation strategies according also to the topology configuration: half bridge, full bridge, and hybrid.

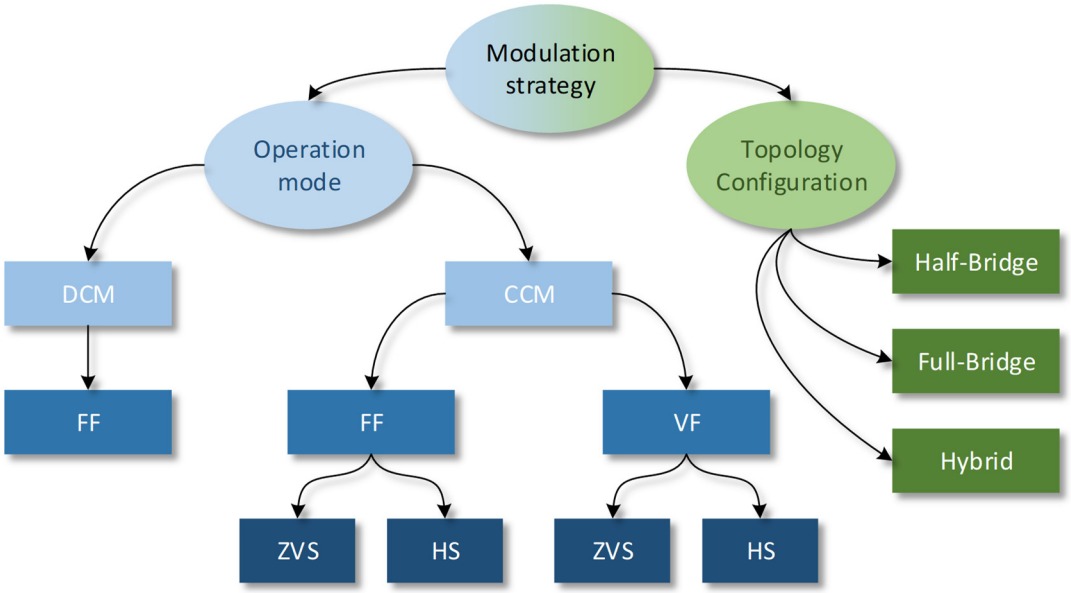


Fig. 4.1 Modulation strategies classification as a function of the topology configuration and the operation mode.

The CCM strategy can operate with fixed or variable frequency during the mains cycle. This operation mode with fixed frequency can be very interesting in applications that cannot modify the operating frequency. Besides, it can operate either with ZVS or hard switching. On the one hand, the main advantage of the ZVS operation is that the turn-on switching losses are null, decreasing switching losses. However, the boost-inductor rms current is increased due to the high ripple required to achieve the ZVS soft-switching behavior, increasing conduction losses in the boost coil and switching devices. On the other hand, a reduced ripple current can be achieved by using a high inductance value, yielding to a hard-switching behavior. As an advantage, the rms boost-inductor current is reduced, improving conduction losses. Moreover, the filtering requirements are lower than with ZVS conditions due to the low ripple. In contrast, the efficiency levels can be decreased by the additional switching losses.

Finally, the DCM operation adds an extra state in which all devices are deactivated, getting a null boost-inductor voltage, v_L, and current, i_b. This additional state allows avoiding the zero-cross distortion in the half-bridge configuration too. The antiparallel diodes are in charge of shorting the boost-inductor current, i_b, when it changes its polarity. This conduction mode has the same drawbacks as the ZVS CCM since it also operates with a high current ripple. Moreover, the turn-on switching losses are also null because of ZVS and ZCS switching. However, there are losses due to the charge of the transistor parasitic capacitance, E_{oss}.

The main advantages and disadvantages of each modulation strategy according to the aforementioned classification are explained below. As it can be seen, each modulation strategy defines a different boost-inductor current as a function of the implemented modulation strategy. However, the resultant mains currents are similar.

The ZVS FF CCM (Fig. 4.2) achieves ZVS at constant frequency. The main drawback is the high ripple of the current is necessary to perform it. This ripple leads to increased rms currents in the boost inductor, the switching devices, and the capacitors, increasing the conduction losses. In the same way, the turn-off current of the switching devices is also increased, increasing the overall switching losses. Furthermore, the bus voltage, the mains phase voltage, and the mains phase current must be measured to perform a closed-loop control, increasing cost and complexity. However, this control assures a high PF and low THD.

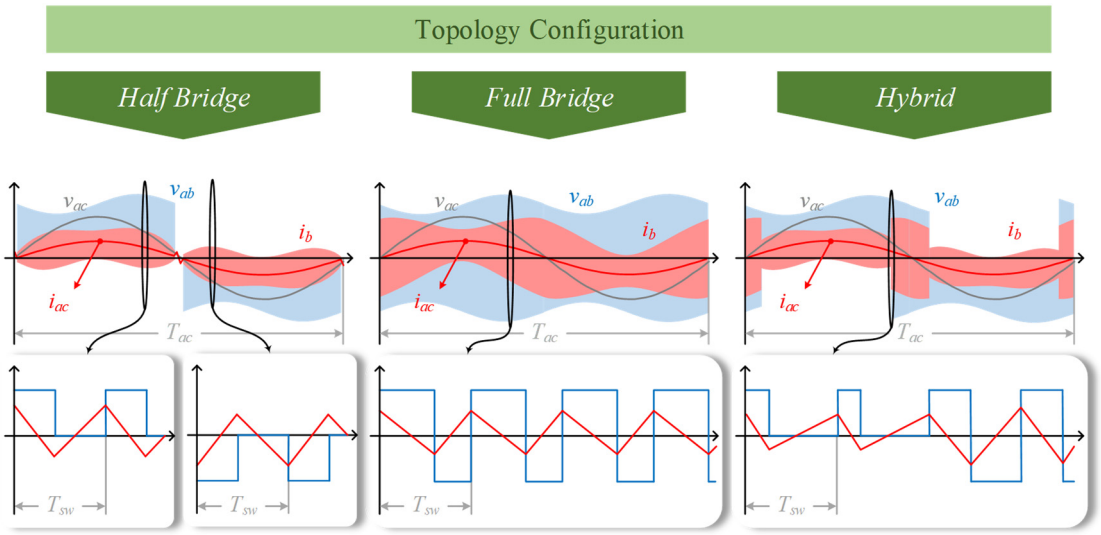


Fig. 4.2 Main waveforms of the zero voltage switching fixed frequency continuous conduction mode (ZVS FF CCM) for half-bridge, full-bridge, and hybrid configurations.

The HS FF CCM (Fig. 4.3) gets a low ripple, almost negligible when compared with the previous modulation strategy. The control is performed similarly, getting a high PF and THD. The main disadvantage is that the switching losses are penalized due to the fact that the turn-on transition is done with not null voltage.

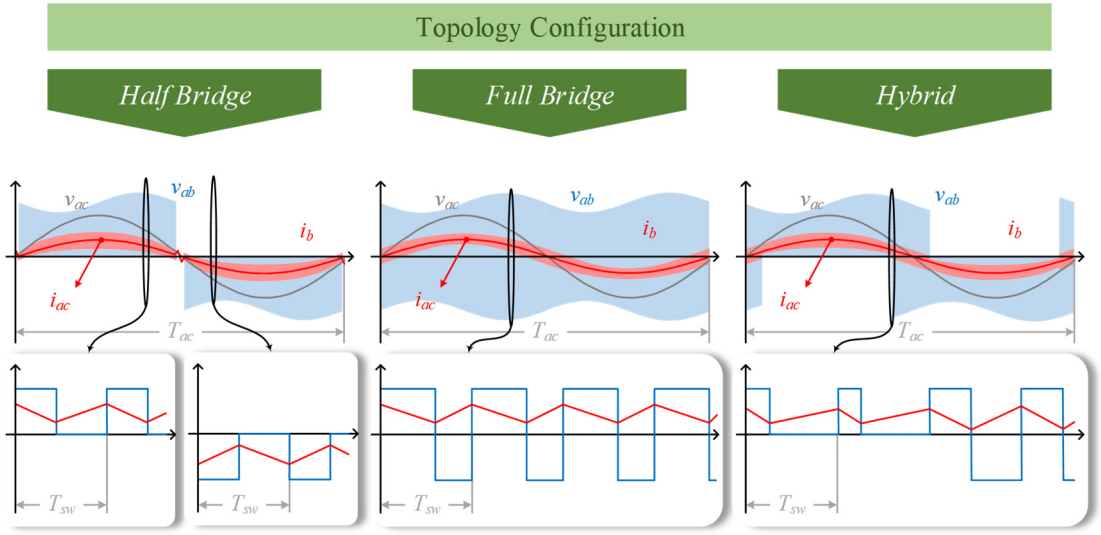


Fig. 4.3 Main waveforms of the hard switching fixed frequency continuous conduction mode (HS FF CCM) for half-bridge, full-bridge, and hybrid configurations.

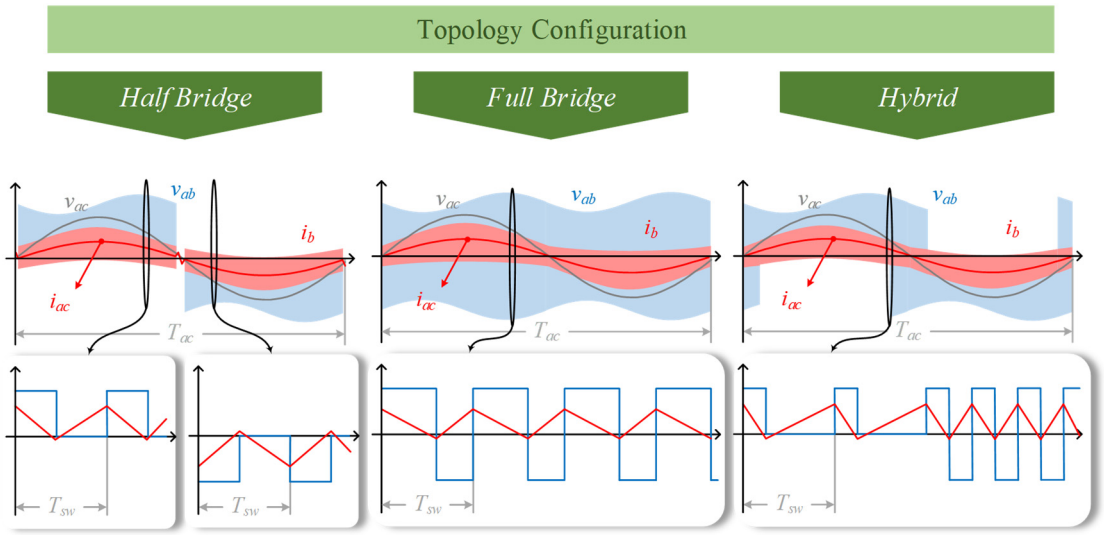


Fig. 4.4 Main waveforms of the zero voltage switching variable frequency continuous conduction mode (ZVS VF CCM) for half-bridge, full-bridge, and hybrid configurations.

The ZVS VF CCM (Fig. 4.4) performs ZVS with a lower current ripple than the first case. Moreover, the input current is not necessary to be measured to perform a closed-loop control. However, the zero cross of the boost-inductor current must be measured, in order to calculate the modulation parameters along with the measurements of the bus voltage and the mains phase voltage. The main drawback is that the switching frequency is variable, and the frequency sweep is very wide.

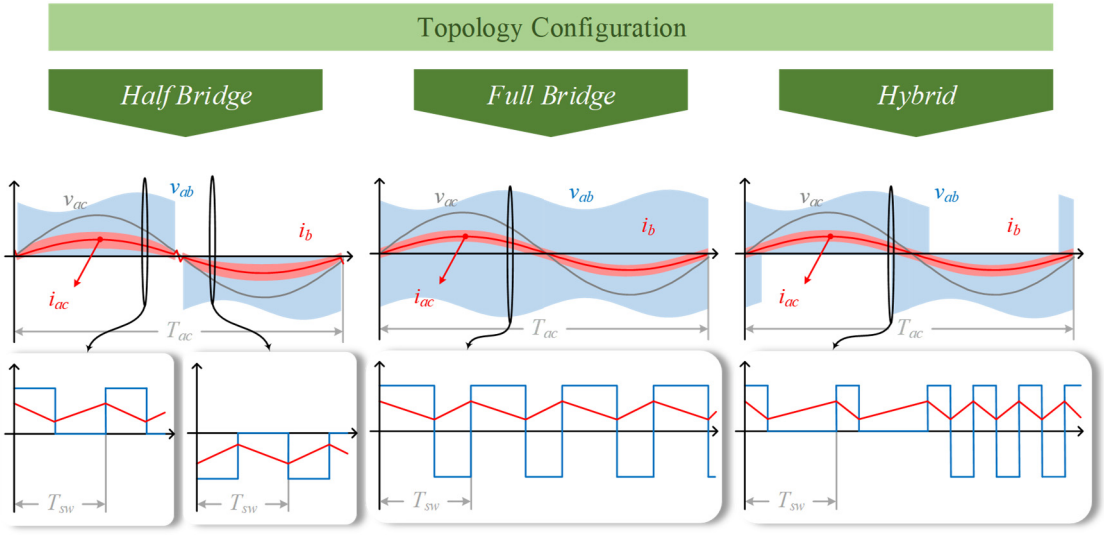


Fig. 4.5 Main waveforms of the hard switching variable frequency continuous conduction mode (HS VF CCM) for half-bridge, full-bridge, and hybrid configurations.

The HS VF CCM (Fig. 4.5) takes the advantage of the control is performed using a current-mode control. In this way, only the boost-inductor current must be measured, decreasing the control cost and achieving a good performance. On the other hand, the

frequency is also variable, although the frequency sweep is lower than in the above case. Besides, the turn-on losses are not null due to the hard switching.

Finally, the FF DCM (Fig. 4.6) performs the control using a modulation parameter obtained from the measurements of the bus voltage and the mains phase voltage. Therefore, the control cost is decreased because the current is not measured. Besides, the frequency is constant. The main disadvantage is the high current ripple, although it is lower than in the first case. Additionally, the reverse recovery losses of antiparallel diodes are not null. The main advantage of this modulation strategy is that there is not distortion of the mains current in half-bridge configuration. Fig. 4.7 sums up the modulation strategy classification along with the main waveforms.

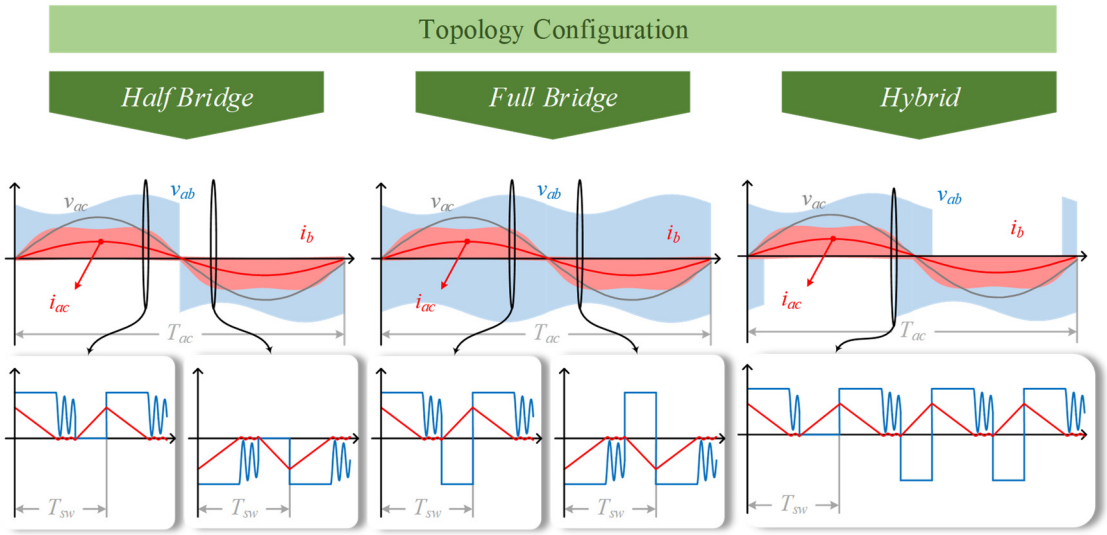


Fig. 4.6 Main waveforms of the fixed frequency discontinuous conduction mode (FF DCM) for half-bridge, full-bridge, and hybrid configurations.

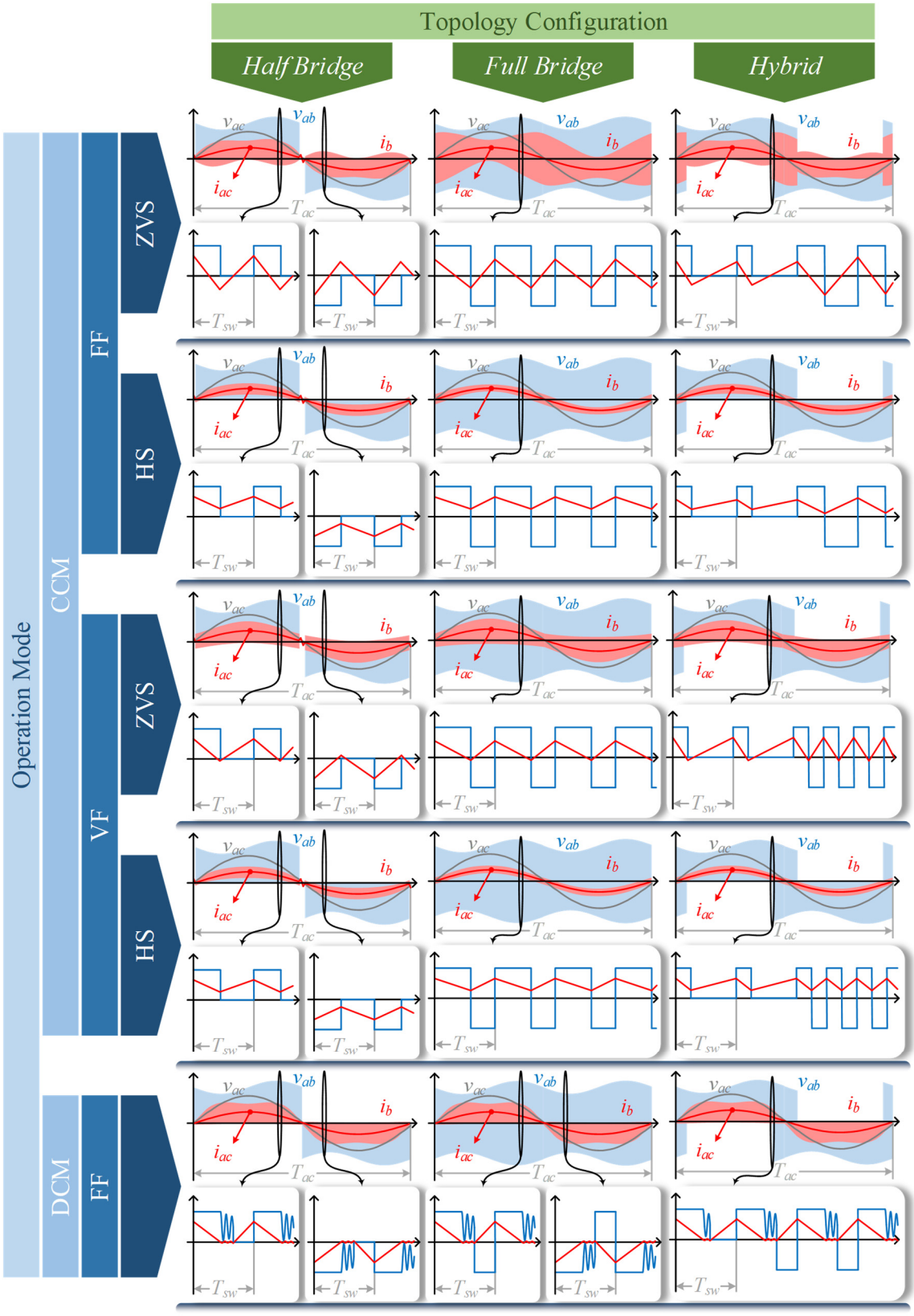


Fig. 4.7 Classification of the proposed single-phase modulation strategies depending on the topology configuration: half bridge, full bridge, or hybrid; and the operation mode: CCM or DCM with fixed or variable switching frequency, f_{sw}, and ZVS or hard switching.

4.1.2. Control design

The proposed modulation strategies achieve different performance, as it has been previously analyzed. Besides, it is important to note that from an implementation point of view, the design of the control loop is different for each one. This section details the proposed control implementation strategies, which can be classified into six groups: boost-inductor voltage control, variable-frequency activation control, current mode control, fixed-frequency activation control, hybrid control, and finally, fixed-frequency hybrid control. Fig. 4.8 summarizes the control strategies implementation classified according to the modulation strategy and the topology configuration.

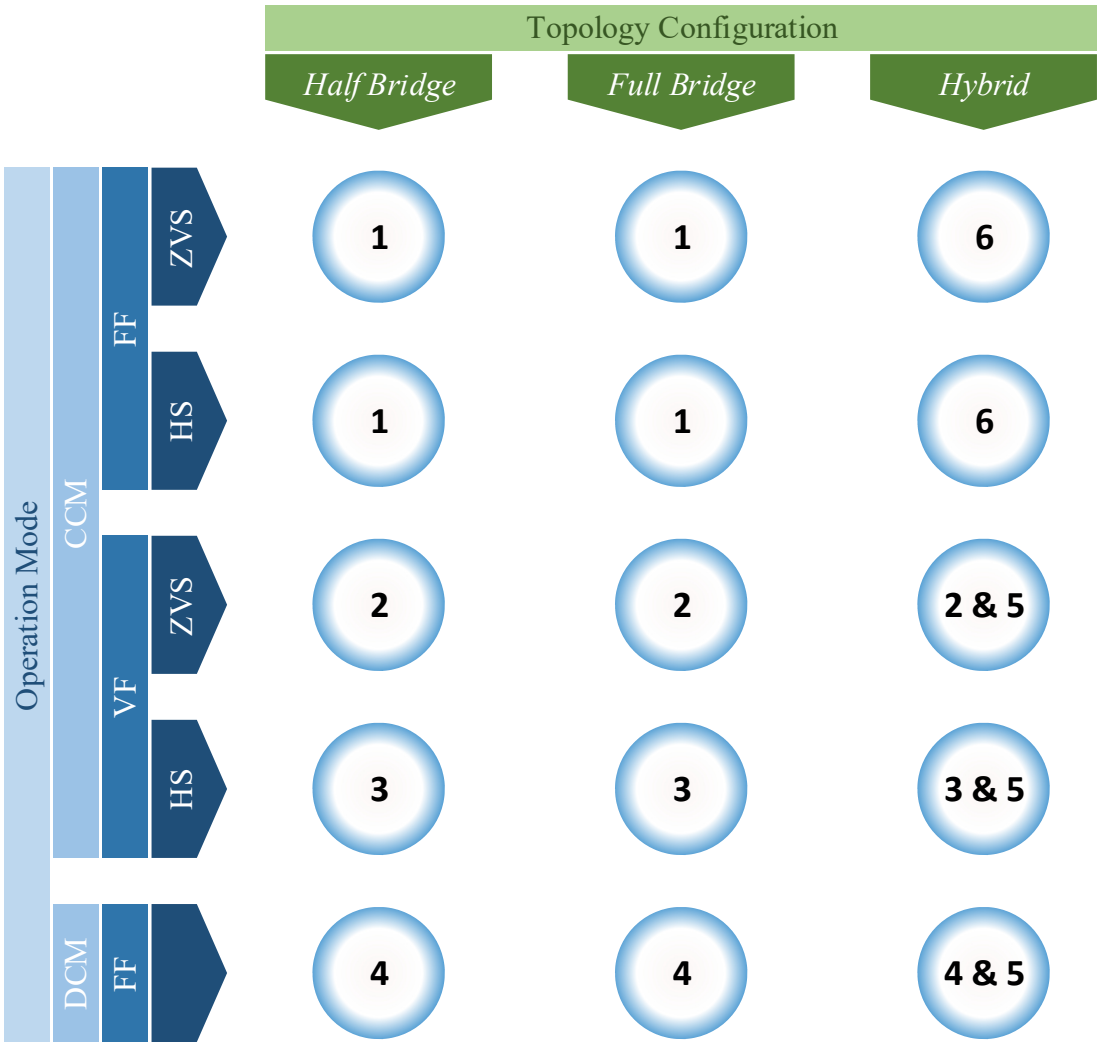


Fig. 4.8 Classification of the proposed control strategies according to the topology configuration: half bridge, full bridge, or hybrid; and the operation mode: CCM or DCM with FF or VF, and ZVS or HS. The control strategies are numerated as follows. 1: boost-inductor voltage control, 2: variable-frequency activation control, 3: current mode control, 4: fixed-frequency activation control, 5: hybrid control, and 6: fixed-frequency hybrid control.

4.1.2.1. Boost-inductor voltage control

The boost-inductor voltage control allows performing all fixed frequency CCM strategies. The converter control is based on generating a sinusoidal reference current, $i_{ac,ref}$, in phase with the mains voltage and with the desired rms current value, $I_{ac,rms}$. The regulator adjusts the mains current, i_{ac}, to follow the reference exactly.

In order to control the system and to eliminate the stationary error, a proportional, K_p, and integral, K_i, regulator is proposed. In typical control schemes, the control input calculated by the regulator is the duty cycle, D, applied to the PFC stage. However, this system is difficult to control using this scheme because its non-linearity which depends strongly on the mains voltage, the bus voltage, and the induction load.

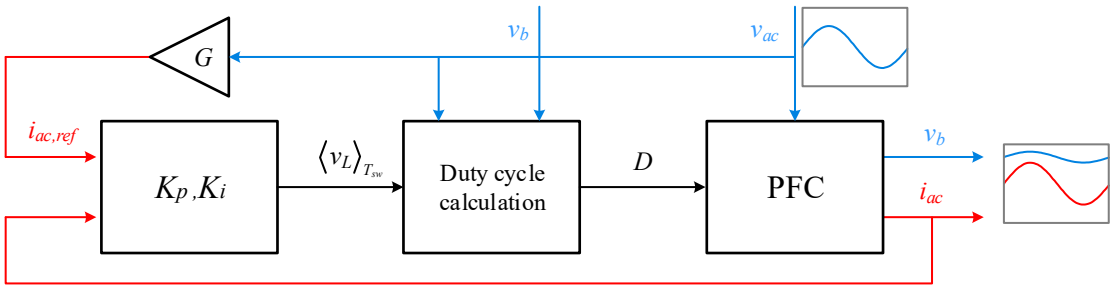


Fig. 4.9 Control scheme of the boost-inductor voltage control where the calculated action is the average boost inductor voltage in a switching period, $\langle v_L \rangle_{T_{sw}}$, which is used to calculate later the duty cycle, D, by using the converter parameters.

To overcome this issue, using the boost-inductor average voltage in a switching period, $\langle v_L \rangle_{T_{sw}}$, as controller output action is proposed, as it is shown in Fig. 2.7. According to the differential equation that models the boost coil behavior

$$i_b\big|_{t_0+T_{sw}} = i_b\big|_{t_0} + \frac{1}{L_b}\int_{t_0}^{t_0+T_{sw}} v_L dt, \tag{4.1}$$

and in an averaged form,

$$i_b\big|_{t_0+T_{sw}} = i_b\big|_{t_0} + \frac{T_{sw}}{L_b}\langle v_L \rangle_{T_{sw}}, \tag{4.2}$$

when the local average voltage in an inductor differs from zero, it means that a variation of its average current has occurred. Consequently, the v_L voltage makes possible to control the boost-inductor current, i_b, linearly and, therefore, the mains current can be properly shaped. Keeping in mind that both a half-bridge or a full-bridge configuration can be

implemented, the duty cycle can be calculated using the boost-inductor average voltage in a second step with (4.3) or (4.4), respectively.

$$D = \begin{cases} \dfrac{\langle v_L \rangle_{T_{sw}} + v_b - v_{ac}}{v_b}, & v_{ac} > 0 \\ \dfrac{\langle v_L \rangle_{T_{sw}} - v_{ac}}{v_b}, & v_{ac} < 0 \end{cases}. \tag{4.3}$$

$$\begin{aligned} D_a &= \frac{1}{2}\left(1 + \frac{\langle v_L \rangle_{T_{sw}} - v_{ac}}{v_b}\right). \\ D_b &= \frac{1}{2}\left(1 - \frac{\langle v_L \rangle_{T_{sw}} - v_{ac}}{v_b}\right). \end{aligned} \tag{4.4}$$

Where v_{ac} and v_b are the mains and the bus voltage in the switching period, respectively.

In order to perform this control, the input voltage, v_{ac}, the input current, i_{ac}, and the bus voltage, v_b, have to be measured. The reference current, $i_{ac,ref}$, is obtained by the product of the mains voltage, v_{ac}, and the transconductance, G. This parameter is defined from the rms mains voltage, $V_{ac,rms}$, and the desired input power, P_{in}, in the following expression.

$$G = \frac{P_{in}}{V_{ac,rms}^2}. \tag{4.5}$$

4.1.2.2. Variable-frequency activation control

This control makes possible to perform the ZVS and variable frequency CCM strategies or, as it is also known, the critical CCM. It is based on stablishing an activation time, t_{on}, that defines the rms input current value, $I_{ac,rms}$. To do this, the zero crossing of the boost-inductor current, i_b, has to be detected. Besides, a negative conduction or ZVS time, t_a, is defined in order to ensure the ZVS switching.

As it is shown in Fig. 4.10, firstly, a negative voltage is applied over the boost inductor. The moment in which the current becomes negative, a negative conduction time, t_a, is stablished in order to assure ZVS switching. After that, the devices are switched to apply a positive voltage to the inductor. Then, the time that the current takes to turn on positive is measured. This interval is called recovery time, t_b, and it is used to compensate

the negative conduction time. Finally, the activation time, t_{on}, is applied and, after that, the devices switch to apply a negative voltage over the boost inductor again.

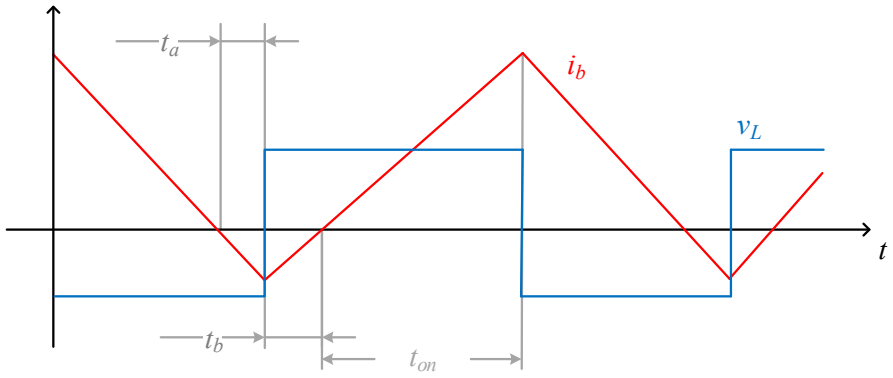


Fig. 4.10 Control scheme of the variable-frequency activation control. The activation time, t_{on}, the negative time, t_a, and the recovery time, t_b, are indicated along with the boost-inductor current, i_b, and voltage, v_L, waveforms.

The voltage applied to the boost coil depends on the topology configuration, the mains voltage, v_{ac}, the bus voltage, v_b, and the switching device activation state. The negative conduction time affects to the operating frequency range and the current ripple, and it is chosen in order to compensate the sensor current delay and load the charge of the transistor parasitic capacitance, Q_{oss}. It does not modify the desired rms input current. It is just defined by the activation time, t_{on}, as a function of the recovery time, t_b, the mains voltage, v_{ac}, the bus voltage, v_b, the transconductance, G, and the boost inductance, L_b. The activation time is calculated with equations (4.6) or (4.7) according to the topology configuration: half bridge or full bridge, respectively. As it is shown by (4.6), in the half-bridge configuration the activation time is just defined by the recovery time, the transconductance, and the boost inductor, which means that the mains and bus voltage do not need to be measured.

$$t_{on} = 2L_bG + t_b, \tag{4.6}$$

$$t_{on} = 2L_bG\left(\frac{v_{ac}}{v_b + v_{ac}}\right) + t_b. \tag{4.7}$$

4.1.2.3. Current mode control

In order to perform the hard switching and variable frequency CCM, a current mode control has been implemented. This control is based on the establishment of a superior and inferior boost-inductor current limits, $i_{b,max}$ and $i_{b,min}$ respectively. These limits depend on the reference current, $i_{ac,ref}$, and the desired current ripple, $I_{b,ripple}$, as

$$i_{b,max} = i_{ac,ref} + \frac{I_{b,ripple}}{2}, \qquad i_{b,min} = i_{ac,ref} - \frac{I_{b,ripple}}{2}. \tag{4.8}$$

As in the boost-inductor voltage control, a sinusoidal reference current, $i_{ac,ref}$, is generated in phase with the mains voltage and with the desired rms current value, $I_{ac,rms}$, which is defined by the transconductance, G, as a function of the desired input power, P_{in}. The boost-inductor current, i_b, is measured with a current sensor. As it is shown in Fig. 4.11, the moment that the boost-inductor current reaches the superior limit, $i_{b,max}$, the switching devices switch in order to apply a negative voltage to the boost inductor and vice versa. When the boost-inductor current reaches the inferior limit, $i_{b,min}$, a positive voltage is applied to the boost inductor. The switching devices that are activated or deactivated to apply a positive or negative voltage to the boost inductor depend on the topology configuration. The switching frequency depends on the boost inductance, L_b, and the current ripple, $I_{b,ripple}$.

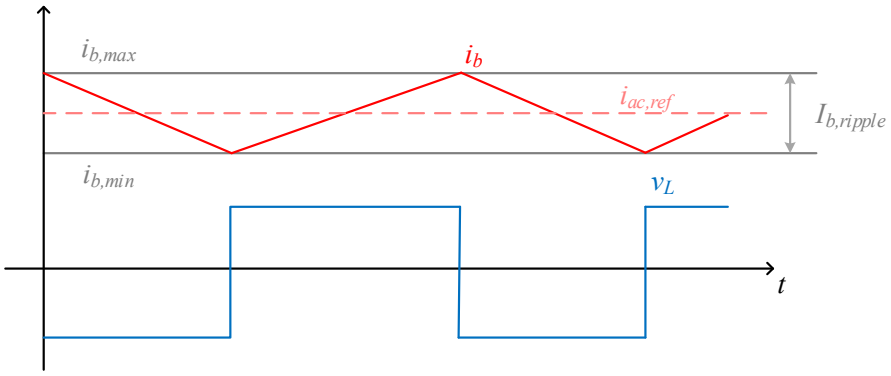


Fig. 4.11 Control scheme of the current mode control. The current ripple, $I_{b,ripple}$, and the superior, $i_{b,max}$, and inferior, $i_{b,min}$, current limits are indicated along with the boost-inductor current, i_b, and voltage, v_L, waveforms.

4.1.2.4. Fixed-frequency activation control

The fixed-frequency activation control has been implemented to perform the DCM strategy. It is similar to the variable-frequency activation control. However, in this case the current zero crossing does not need to be detected because the frequency is fixed, and the activation time, t_{on}, is calculated as a function of the converter parameters and the switching period, T_{sw}, in order to achieve the extra state of discontinuous conduction mode. The equations (4.9) and (4.10) allow calculating this parameter using the half-

bridge or full-bridge configurations, respectively. In both cases, the bus voltage, v_b, and the mains voltage, v_{ac}, have to be measured.

$$t_{on} = \sqrt{2T_{sw}L_bG\frac{v_b - |v_{ac}|}{v_b}}. \tag{4.9}$$

$$t_{on} = \sqrt{T_{sw}L_bG\frac{(v_b - v_{ac})v_{ac}}{(v_b + v_{ac})v_b}}. \tag{4.10}$$

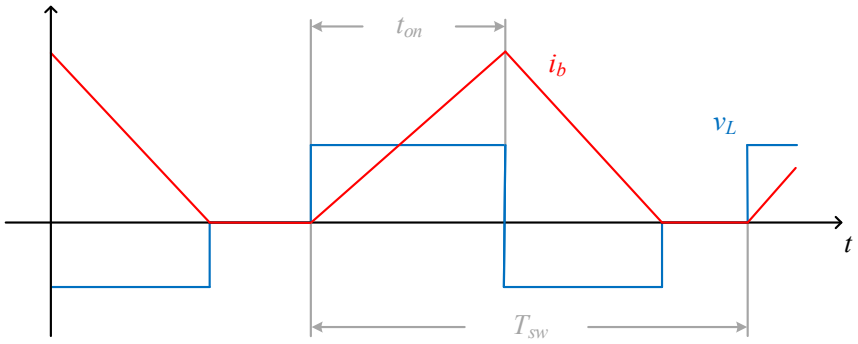


Fig. 4.12 Control scheme of the fixed-frequency activation control. The activation time, t_{on}, and the boost-inductor current, i_b, and voltage, v_L, waveforms are indicated.

Moreover, the negative conduction time, t_a, and the recovery time, t_b, are not necessary, as it is shown in Fig. 4.12. The minimum switching period, $T_{sw,min}$, that allows operating in DCM is calculated using equations (4.11) and (4.12) according to the topology configuration, half bridge or full bridge, respectively. It depends on the boost inductance, L_b, the transconductance, G, the bus voltage, v_b, and the mains voltage, v_{ac}. A conservative approach is based on considering the minimum bus voltage and the maximum mains voltage, i.e. $\sqrt{2}V_{ac,rms}$.

$$T_{sw,\min} = 2L_bG\frac{v_b}{v_b - v_{ac}}. \tag{4.11}$$

$$T_{sw,\min} = 4L_bG\frac{v_b v_{ac}}{v_b^2 - v_{ac}^2}. \tag{4.12}$$

4.1.2.5. Hybrid control

The fixed-frequency hybrid modulation is based on using the half-bridge configuration and changing to the full-bridge configuration only when the bus voltage is close to zero to avoid the zero-cross distortion. In this way, the threshold voltage, v_{th}, parameter is defined. As it is shown in Fig. 4.13, when the absolute value of the mains voltage, $|v_{ac}|$, is higher than the threshold voltage, v_{th}, the half-bridge configuration is used. Even though the control parameters depend on the topology configuration, the control strategy is independent. It allows performing hybrid modulations using the previously discussed control strategy when VF modulation strategies are implemented.

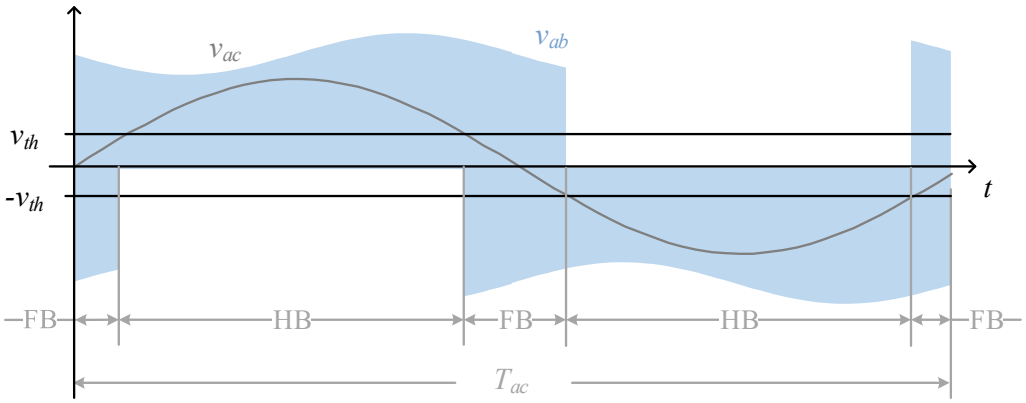


Fig. 4.13 Detail of the hybrid modulation control with the threshold voltage, v_{th}, indication, and the time of half-bridge (HB) modulation or full-bridge (FB) modulation.

4.1.2.6. Fixed-frequency hybrid control

The aforementioned change is not trivial when FF modulation strategies are used because the change between the half-bridge and the full-bridge operation creates a significant perturbation that the converter control cannot manage properly, especially in ZVS modulations (Fig. 4.14).

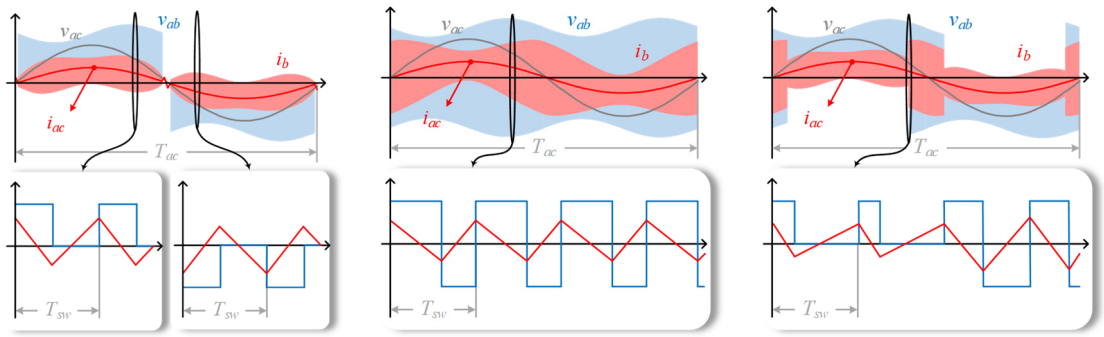


Fig. 4.14 ZVS and fixed-frequency modulation strategies using (a) half-bridge, (b) full-bridge, and (c) hybrid configuration.

Therefore, the change from the half-bridge to the full-bridge configuration in the hybrid modulation using FF modulation strategies must be carefully addressed to avoid current distortion. In order to decrease the effect of this configuration change, a soft-transient modulation strategy is proposed [142]. This strategy is based on activating the rectifier branch at the switching frequency, T_{sw}, with a phase shift, α, close to the mains voltage zero crossing. As it is shown in Fig. 4.15, the phase shift increases slightly from the threshold voltage, v_{th}, enabling the converter control to eliminate the perturbation. As it can be seen, the value of the phase shift slightly increases and decreases to avoid perturbations, and it allows the closed-loop strategy to perform the control properly.

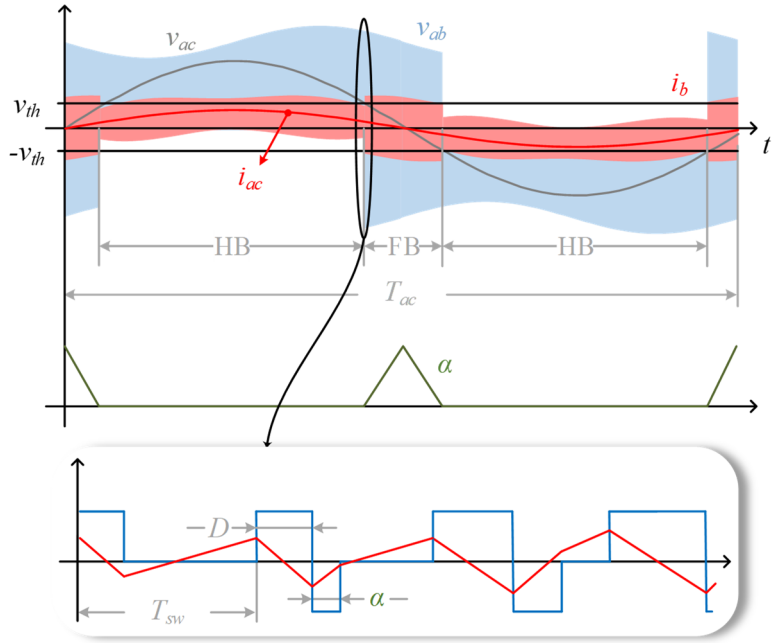


Fig. 4.15 Proposed soft-transient modulation strategy for FF hybrid modulation strategies.

The converter control (Fig. 4.16) is similar to the aforementioned boost-inductor voltage control, and it is based on generating a sinusoidal reference current, $i_{ac,ref}$, in phase with the mains voltage and with the desired rms current value, $I_{ac,rms}$. The regulator adjusts the mains current, i_{ac}, to follow the reference. The output action of the proportional, K_p, and integral, K_i, regulator is the boost-inductor average voltage.

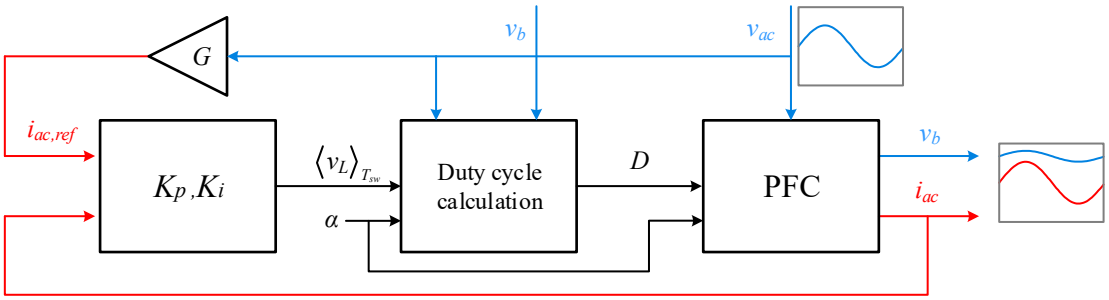


Fig. 4.16 Proposed digital control implementation where the output action of the proportional, K_p, and integral, K_i, regulator is the average inductor voltage, $\langle v_L \rangle_{T_{sw}}$. The duty cycle, D, is calculated in function of the α, v_b, v_{ac}, and $\langle v_L \rangle_{T_{sw}}$.

The boost-inductor average voltage, $\langle v_L \rangle_{T_{sw}}$, enables controlling the boost-inductor current, i_b, linearly and, therefore, the mains current, i_{ac}, can be properly shaped. Keeping in mind the phase shift, α, the duty cycle, D, can be calculated in a second step as

$$D = \begin{cases} \alpha + \dfrac{\langle v_L \rangle_{T_{sw}} + v_b - v_{ac}}{v_b}, & v_{ac} > 0 \\ \alpha + \dfrac{\langle v_L \rangle_{T_{sw}} - v_{ac}}{v_b}, & v_{ac} < 0 \end{cases} . \tag{4.13}$$

TABLE 4.1 summarizes de main implementation features of each proposed control strategy in this section to perform single-phase PFC modulation strategies. In this table, the required measurements, the control method, and the output control parameters are indicated.

The control complexity and cost have also been analyzed. Firstly, all control strategies have to measure the zero crossing of the mains voltage to obtain mains-synchronized operation. The fixed-frequency activation control (4) strategy is the least complex control strategy because it just needs an additional measurement, the bus voltage. After this, the easiest control strategy is the boost-inductor voltage control (1), since it also has to measure the mains current, or the variable-frequency activation control (2) using half-bridge configuration, because it just needs to measure the zero crossing of the boost-inductor current. Finally, the most complex strategies are the variable-frequency activation control (2) using full-bridge configuration, because it needs to measure the bus voltage as well as the zero crossing of the boost-inductor current, or the current mode control (3), since it must measure the boost-inductor current. The boost-inductor current measurement is more complex than the mains current measurement because the current

sensor has more requirements such as a higher bandwidth. Besides, the hybrid control (5) does not need additional measurements whereas the fixed-frequency hybrid control (6) has the same requirements than the boost-inductor voltage control.

TABLE 4.1

MAIN IMPLEMENTATION FEATURES OF THE CONTROL STRATEGIES

Number	*Control strategy*	*Required measurements*	*Control method*	*Control parameters*
1	Boost-inductor voltage control	Mains current, i_{ac} Mains voltage, v_{ac} Bus voltage, v_b	Closed-loop controller	Duty cycle, D
2	Variable-frequency activation control	Zero crossing of boost-inductor current, i_b. (In FB: Mains voltage, v_{ac}, and bus voltage, v_b)	Activation times	Activation time, t_{on} Negative time, t_a Recovery time, t_b
3	Current mode control	Boost-inductor current, i_b	Current limits	Activation signals of switching devices.
4	Fixed-frequency activation control	Mains voltage, v_{ac} Bus voltage, v_b	Activation times	Activation time, t_{on}
5	Hybrid control	Mains voltage, v_{ac}, and same as in 2, 3, or 4.	Complementary to 2, 3, or 4.	Same as in 2, 3, or 4.
6	Fixed-frequency hybrid control	Mains current, i_{ac} Mains voltage, v_{ac} Bus voltage, v_b	Closed-loop controller	Duty cycle, D Phase shift, α

4.2. Multi-phase PFC modulation strategies

4.2.1. Operation modes

As it has been previously discussed, the multi-phase topology with split bus capacitor configuration behaves as a full-bridge topology. As a result, the modulation strategies used for controlling the full-bridge topologies in single-phase case can be applied in this situation. Five different modulation strategies can been considered (Fig. 4.17), and they are also classified according to three main parameters: the conduction mode, the switching mode, and the switching-frequency variation [142].

As in the single-phase operation modes, in the multi-phase case the conduction mode is divided in CCM and DCM, whereas the switching modes can be classified into ZVS and HS modes. In the ZVS mode, the antiparallel diode is previously activated because

the inductor current always crosses through zero, changing the current direction before the switch activation. Consequently, the turn-on transition is performed with null voltage, avoiding the turn-on losses. This condition is not fulfilled is HS mode.

Lastly, the switching frequency classification includes FF and VF. The FF modulation strategies avoid frequency changes along the mains cycle in contrast to the VF modulation strategies. The implemented frequency mode greatly depends on the final application, and it determines the overall performance of the topology. In domestic IH applications, a fixed frequency may be mandatory in order to avoid the acoustic noise generated by the intermodulation frequencies between the IH inverter and the PFC [171].

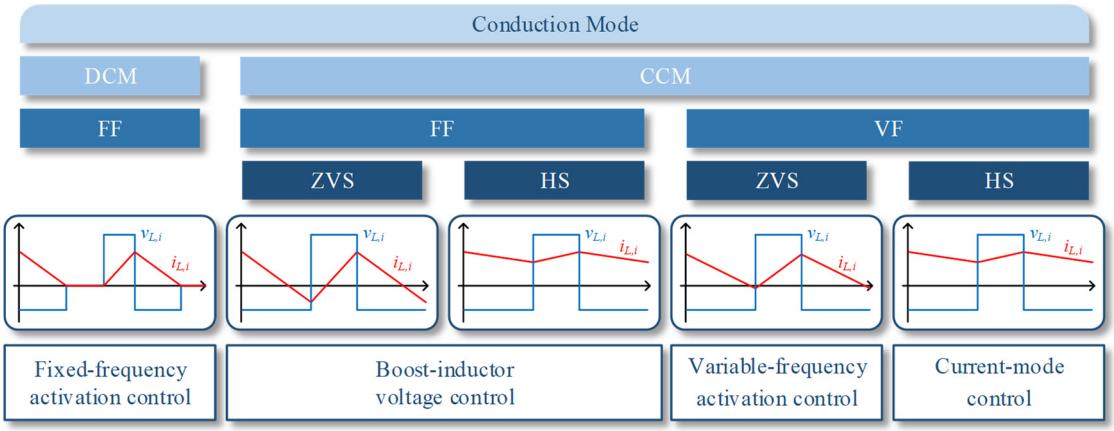


Fig. 4.17 Modulation strategy classification of the multi-phase PFC rectifier. From top to bottom: the conduction mode, Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM); the frequency mode, Fixed Frequency (FF) or Variable Frequency (VF); the switching mode, Zero Voltage Switching (ZVS) or Hard Switching (HS); the boost-inductor waveforms. Finally, the control strategy to perform each modulation strategy.

4.2.2. Control design

Due to the fact that the multi-phase topology operation is equivalent to the full-bridge configuration of the single-phase rectifier considering the half of the bus voltage, not only the same modulation strategies can be performed, but also the same control strategies. However, it is necessary take into account that the half of bus voltage appears in the equations presented in previous sections.

Specifically, in the boost-inductor voltage control for managing fixed-frequency CCM modulation strategies, the equation (4.4) is replaced for

$$D_i = \frac{1}{2}\left(1+2\frac{\langle v_{L,i}\rangle_{T_{sw}} - v_{ac,i}}{v_b}\right). \tag{4.14}$$

In the variable-frequency activation control used for managing ZVS VF CCM, the equation (4.7) results as

$$t_{on} = 4L_i G\left(\frac{v_{ac,i}}{v_b + 2v_{ac,i}}\right) + t_b. \tag{4.15}$$

In the fixed-frequency activation control implemented for controlling the FF DCM, the equations (4.10) and (4.12) are modified as

$$t_{on} = \sqrt{2T_{sw}L_i G\frac{\left(v_b - 2v_{ac,i}\right)v_{ac,i}}{\left(v_b + 2v_{ac,i}\right)v_b}}. \tag{4.16}$$

$$T_{sw,\min} = 8L_i G\frac{v_b v_{ac,i}}{v_b^2 - 4v_{ac,i}^2}. \tag{4.17}$$

Finally, in current mode control implemented for HS VF CCM modulation strategies, changes are not necessary because the control is independent of the bus voltage.

Chapter 5

Implementation and Experimental Results

In this Chapter, the proposed topologies and modulation strategies have been experimentally implemented for both single-phase and multi-phase configuration. The main waveforms of both prototypes are presented showing the viability of the proposed topologies and modulation strategies. Besides, the implementation of an ad-hoc three-phase regulable power supply that has been used to perform the experimental tests is detailed. Finally, the implementation of a matrix inverter for domestic IH applications is also shown.

Contents

5. Implementation and Experimental Results

In previous chapters, the proposed PFC boost topologies for single-phase and multi-phase cases and their modulation strategies have been discussed. The main advantages and disadvantages have been qualitatively discussed, and the waveforms and the configuration sequence of each topology have been analyzed in order to obtain the equations of the converters. Besides, several modulation strategies that are able to perform the PFC strategy have been introduced along with their main advantages and drawbacks. Finally, the control strategies that are necessary to implement these modulation strategies have been detailed, including control schemes and equations of the main control parameters.

In this Chapter, the proposed PFC topologies, modulation strategies, and controls are experimentally implemented in order to prove the feasibility of these proposals and to obtain experimental results. The obtained measurements of the PFC rectifiers using different modulation strategies, such as the main waveforms or efficiency, will allow a in depth quantitative analysis of different key figures of merit that will be discussed in the next chapter.

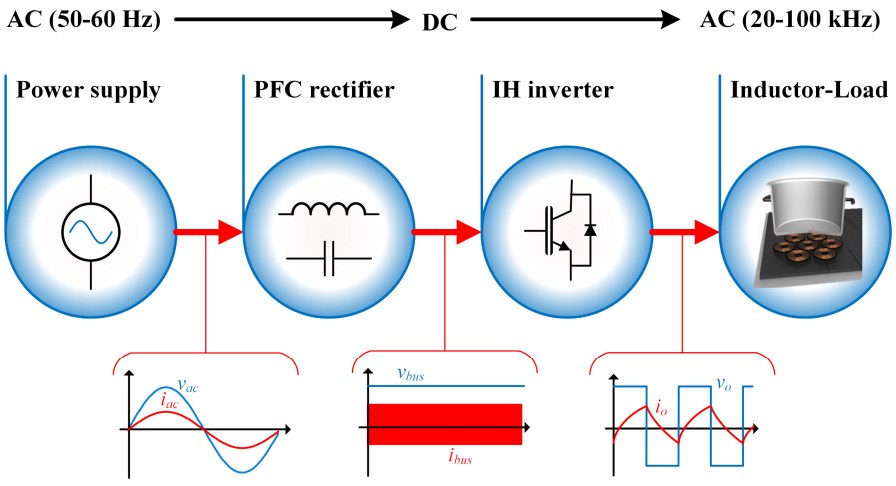


Fig. 5.1 Block diagram of the experimental implementation of the proposed PFC rectifiers.

The experimental implementations for single-phase and multi-phase cases have been developed taking into account the scheme presented in Fig. 5.1. An ad-hoc designed power supply generates the ac voltage used to emulate the single/multi-phase mains. Then, the PFC rectifier generates a dc bus voltage in order to power the IH inverter and the inductor-load system. For each particular case, single-phase or multi-phase, different

requirements are taken into account for their implementation, and therefore, they are individually developed along this chapter.

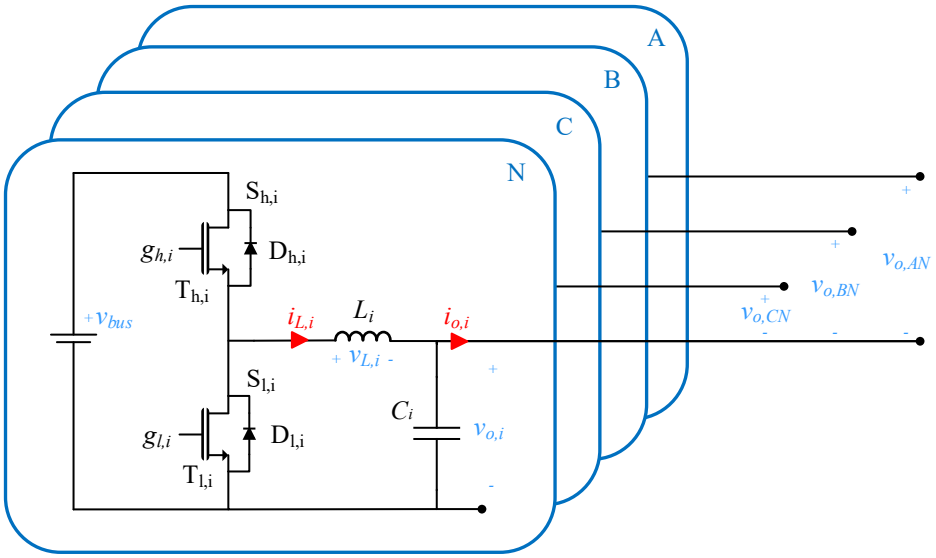
5.1. Three-phase regulable power supply

A power supply has been developed in order to power the different experimental implementations of this dissertation. The particular requirements of the power supply for this original application of the PFC rectifier to domestic IH, such as the power, control capabilities of the current and voltage, and the different number of active phases, have motivated the development of a custom-made power supply.

The proposed prototype has three independent outputs that are able to deliver ac voltage, dc voltage, or a combination of both. The output voltage is regulable up to 750 V, and the maximum current is limited to 50 A due to the saturation current of the designed magnetic components. Besides, a closed-loop control of the current has been implemented along with the voltage control. This current control limits the current according to the voltage requirements, and the required output power, increasing the safety of the power supply and decreasing the risk of breaking of back-end prototypes when improper operating is detected, e.g. a short-circuit. Moreover, the proposed converter and control are able to manage bidirectional power flow and interrupt the power supply faster than commercial power supplies. Therefore, it is safer for engineering staff.

5.1.1. Topology of the converter

The three-phase power supply has been designed using 4 independent modules. These modules are powered at bus voltage, v_{bus}, using a dc external power supply. Each module is composed of a dc-dc buck converter using a half-bridge inverter and an output filter. The inverter is composed of two switching devices, $S_{h,i}$ and $S_{l,i}$, implemented with silicon carbide (SiC) MOSFET transistors, $T_{h,i}$ and $T_{l,i}$, and parallel diodes, $D_{h,i}$ and $D_{l,i}$. The gate signals, $g_{h,i}$ and $g_{l,i}$, allow controlling the activation of the transistors. The output filter consists of an inductor, L_i, and a capacitor, C_i. The capacitor voltage is the output voltage of the module, $v_{o,i}$, whereas the inductor current is i_L, and the output current is $i_{o,i}$. The Fig. 5.2 shows the scheme of this topology for the 4 modules, which are enumerated according the *i* subscript as A, B, C, and N. The output voltages of the three-phase power supply are the output voltages of the A, B and C modules referenced to the output voltage of the N module, i.e. $v_{o,AN}$, $v_{o,BN}$, and $v_{o,CN}$, respectively.



i = A, B, C, and N.

Fig. 5.2 Topology of the converter of the three-phase power supply using 4 dc-dc buck stages.

The main waveforms of the inductor of i^{th}-module implemented using the dc-dc buck topology are represented in the Fig. 5.3, whereas Fig. 5.4 shows the configuration sequence. The proposed converter is bidirectional and, therefore, bidirectional current is considered in this analysis. In order to simplify it, a unique module is depicted using a resistance as load, R_o. As it can be seen, the low-side switching device is activated at states I and II. As a result, the inductor voltage, $v_{L,i}$, is negative and the current decrease. At the state III and IV, the applied voltage over the inductor is positive and, consequently, the current increase.

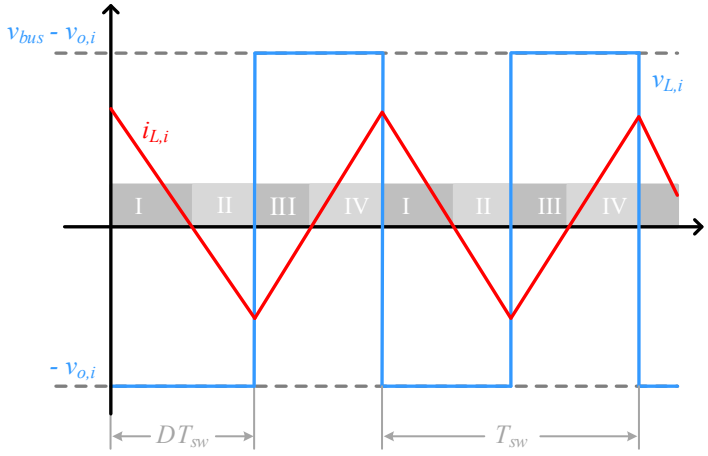
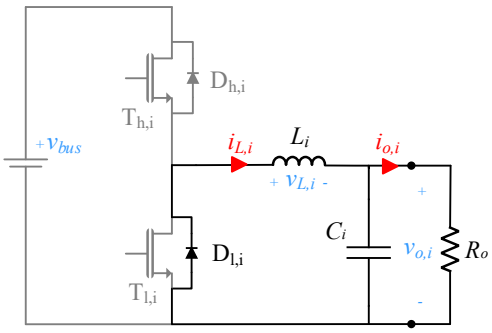


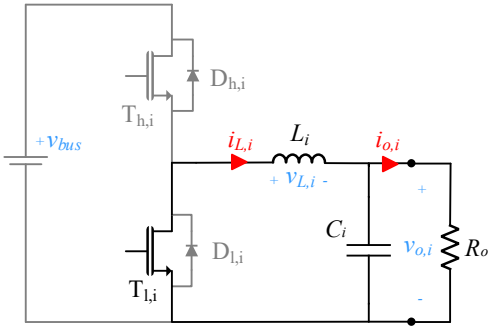
Fig. 5.3 Inductor waveforms and activation states of the i-module of the three-phase power supply.

State I



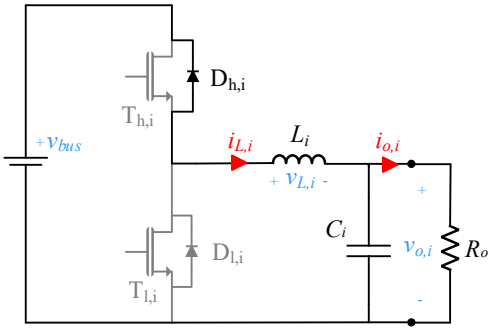
(a)

State II



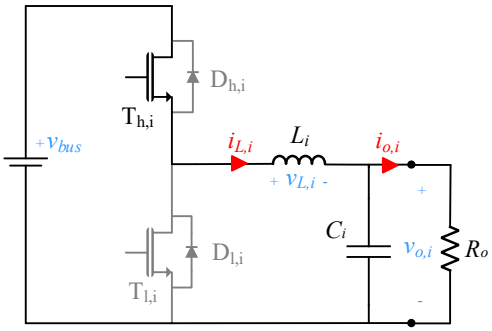
(b)

State III



(c)

State IV



(d)

Fig. 5.4 Configuration sequence of the *i*-module of the three-phase power supply powering a resistive load, R_o. (a) state I, (b) state II, (c) state III, and finally, (d) state IV.

The boost-inductor voltage, $v_{L,i}$, depends on the activation state as follows

$$v_{L,i} = \begin{cases} -v_{o,i}, & \text{state: I and II} \\ v_{bus} - v_{o,i}, & \text{state: III and IV} \end{cases}. \tag{5.1}$$

Therefore, the duty cycle, D_i, in relation to the activation time of the low-side switch and in CCM operation mode is calculated in function of the bus voltage and the output module voltage as

$$D_i = 1 - \frac{v_{o,i}}{v_{bus}}. \tag{5.2}$$

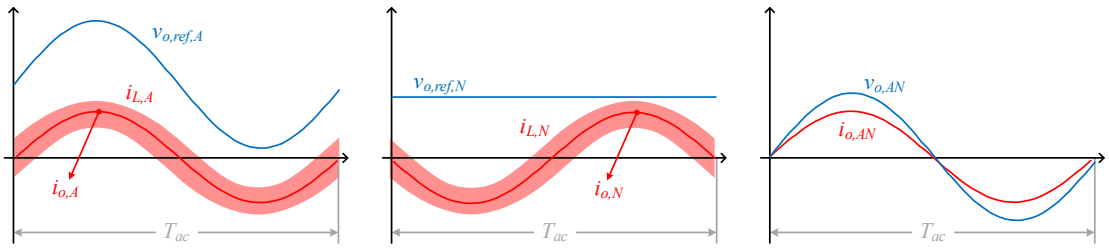
5.1.2. Modulation and control strategy

The modulation strategy is based on operating at fixed switching frequency in a CCM operation mode. Each *i*-module is controlled in order to get a reference output voltage, $v_{o,ref,i}$, and the desired *i*-phase output voltage, $v_{o,iN}$, as it is shown in Fig. 5.5. In this case, the N-module is modulated at 0.5 fixed duty cycle to obtain the half of the bus voltage at the output of the module, $v_{o,ref,N}$, as

$$v_{o,ref,N} = \frac{v_{bus}}{2}. \tag{5.3}$$

The *i*-module is controlled in order to obtain a dc-voltage value of the half of the bus voltage and the desired voltage,

$$v_{o,ref,i} = v_{o,iN} + v_{o,ref,N}. \tag{5.4}$$



(a) (b) (c)

Fig. 5.5 Modulation strategy of the three-phase power supply operating with the A and N module powering a resistive load. (a) Main waveforms of the A module, (b) the N module operating at constant 0.5 duty cycle, and (c) the resultant main waveforms at the output, i.e. the A module referenced to the N module.

The converter control is based on generating the reference voltage, $v_{o,ref,i}$ using a closed-loop control as it is shown in Fig. 5.6. In order to control also the inductor current,

the output of the regulator is the reference current of the inductor, $i_{L,ref,i}$. The duty cycle is obtained in a second step taking into account this value, the measured current, $i_{L,i}$, the bus voltage, v_{bus}, and the output voltage, $v_{o,i}$.

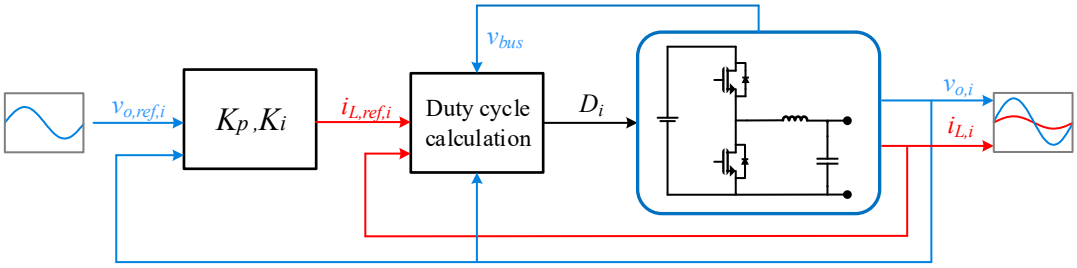


Fig. 5.6 Control scheme of the three-phase power supply using a proportional, K_p, and integral, K_i, regulator and the calculation of the duty cycle based on the reference current of the inductor, $i_{L,ref,i}$.

In particular, from the differential equation of a coil (4.1), it is possible to deduce that the average voltage of the boost inductor, $\langle v_{L,i} \rangle_{T_{sw}}$, in a switching period, T_{sw}, is proportionally related with its current variation, $i_{L,i}$, as is expressed below

$$i_{L,i}\Big|_{t_0+T_{sw}} = i_{L,i}\Big|_{t_0} + \frac{T_{sw}}{L_i}\langle v_{L,i} \rangle_{T_{sw}}. \tag{5.5}$$

Therefore, considering the current at the k switching period as the boost-inductor current, $i_{L,i}$, and the current at the k+1 switching period as the reference current, $i_{L,ref,i}$, the boost-inductor average voltage results as

$$\langle v_{L,i} \rangle_{T_{sw}} = \frac{L_i}{T_{sw}}\left(i_{L,ref,i} - i_{L,i}\right). \tag{5.6}$$

Besides, the boost-inductor average current is also obtained in function of the duty cycle, D_i, and the activation state as

$$\langle v_{L,i} \rangle_{T_{sw}} = D_i \langle v_{L,i} \rangle_{\text{I, II}} + (1 - D_i)\langle v_{L,i} \rangle_{\text{III, IV}}. \tag{5.7}$$

Taking into account equations (5.1), (5.6), and (5.7), the duty cycle can be expressed in function of the reference current as

$$D_i = \frac{\frac{L_i}{T_{sw}}\left(i_{L,i} - i_{L,ref,i}\right) + v_{bus} - v_{o,i}}{v_{bus}}. \tag{5.8}$$

5.1.3. Power supply implementation

The implementation of the 1000-V, 50-A, and three-phase power supply is presented in this section. TABLE 5.1 summarizes the main features of the power supply. The main printed circuit board (PCB), which is shown in Fig. 5.7, contains the 4 modules of buck converters. The half-bridge inverters have implemented using 4 half-bridge modules of 8-mΩ and 1700-V SiC MOSFETs CAS300M17 from CREE. The power losses are dissipated using forced-air cooling. The device control is a custom-made FPGA module with up to 200 signals, a XCF32P flash, and a XC6SLX150 SPARTAN-6 FPGA from Xilinx. The measurement system is composed of current sensors to measure the inductor current and the output current, resistive divisors to measure the bus voltage and the output voltage, and analog-to-digital converters (ADC) to send the measurement information to the device control. The selected current sensor is the 50-A CASR 6-NP from LEM whereas the selected ADCs are the 1-MSPS and 12-Bit ADCS7476 from Texas Instruments. This master PCB is completed with the AFBR-1624Z fiber optic transmitter and the AFBR-2624Z fiber optic receiver from Broadcom to communicate device control with the user interface.

TABLE 5.1

THREE-PHASE POWER SUPPLY DESIGN PARAMETERS

PARAMETER	VALUE
Output phases	1 – 3 + N
Input voltage range, v_{bus}	0 - 1000 V
output voltage range, $v_{o,i}$	0 - 1000 V
Maximum output current, $i_{o,i}$	50 A rms
Output frequency range, f_{sw}	dc - 500 Hz
Nominal output voltage, $v_{o,iN}$	230 V
Nominal output current, $i_{o,i}$	32 A
Nominal output power, $P_{o,i}$	7.5 kW
Overall output power, P_o	22 kW
Bus capacitor, C_i	80 µF
Inductance, L_i	250 µH
Switching frequency, f_{sw}	25 kHz

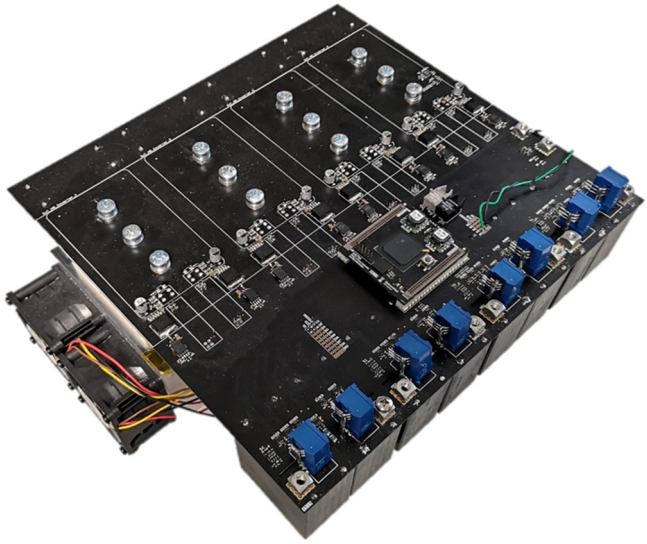


Fig. 5.7 Master PCB of the three-phase bidirectional power supply.

An additional PCB (Fig. 5.8) has been designed to perform safety functions. It is composed of 4 high current and voltage HE1AN-W-DC12V-Y7 relays from Panasonic to short the power supply in case of need. Besides, 33-Ω EY330KE resistances from Ohmite are employed to discharge the bus voltage of the outputs along with 4 IHW30N160R2 IGBTs from Infineon. This slave PCB is communicated with the master PCB to perform the control. Besides, the commercial FMBD-B92B-3612 filter from Schurter has been included at the output of the power supply.

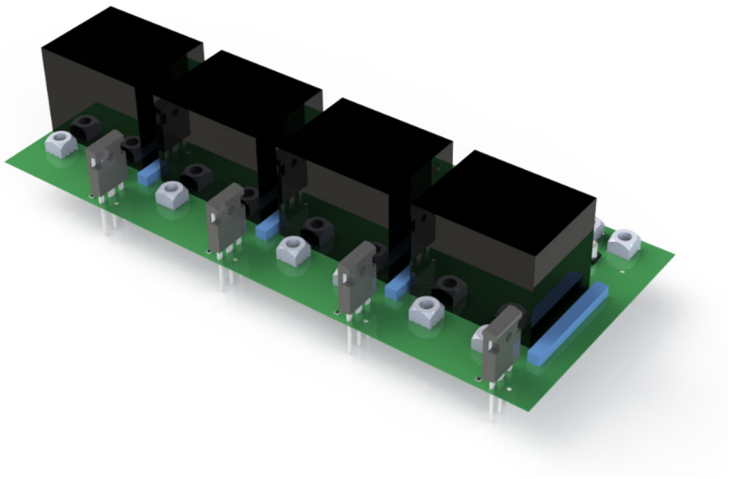


Fig. 5.8 3D render of the slave PCB of the three-phase bidirectional power supply.

Output filtering capacitors, C_i, are included in the master PCB. Each C_i capacitor consists of 2 40-µF and 1100-V film capacitors from Panasonic. The inductors, L_i, have been designed using ferrites and Litz wire. Each inductor is composed of 8 E65/32/27

ferrite cores in parallel along with 8 I65/5/50 ferrite cores to close the magnetic circuit. A 3.2-mm air gap has been implemented to increase the saturation current. TABLE 5.2 summarizes the main features of the implemented inductors, which are shown in Fig. 5.9. The estimated losses in each inductor are 25 W operating at 25 kHz of switching frequency and 32-A output current. These inductors do not need cooling because of the low losses in relation with its volume.

TABLE 5.2

DESIGN PARAMETERS OF THE POWER SUPPLY INDUCTORS, L_I.

PARAMETER	VALUE
Inductance, L_i	250 µH
Saturation current, $I_{sat,L,i}$	120 A
50-Hz resistance, $R_{L,i,LF}$	20 mΩ
25-kHz resistance, $R_{L,i,HF}$	60 mΩ
Number of turns	12
Number of strands	5000
Strand diameter	50 µm
Strand material	Copper
Core	8 x E65/32/27 8 x I65/5/50
Core material	N87 ferrite
Nominal losses	25 W
Dimensions	28 x 6.5 x 4.5 cm
Volume	819 cm^3

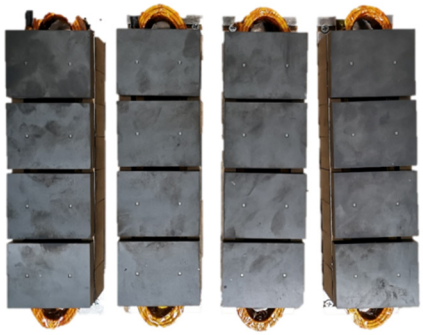


Fig. 5.9 Implemented inductors, L_i, of the three-phase bidirectional power supply.

The master PCB, the slave PCB, the 4 inductors, and the filter have been built in a custom-made 5U rack. The complete system is shown in Fig. 5.10. Besides, a Microsoft Surface Pro has been mounted as user interface. The software has been developed in Visual Basic and it allows controlling the output ac voltage, the output dc voltage, the output frequency, or the output current limit, among others. Besides, the main measurements of voltage, current, and power are represented. In Fig. 1.3 the main window of the control software is presented.

Fig. 5.10 Complete system of the three-phase bidirectional power supply in a custom-made 5U rack along with the user interface.

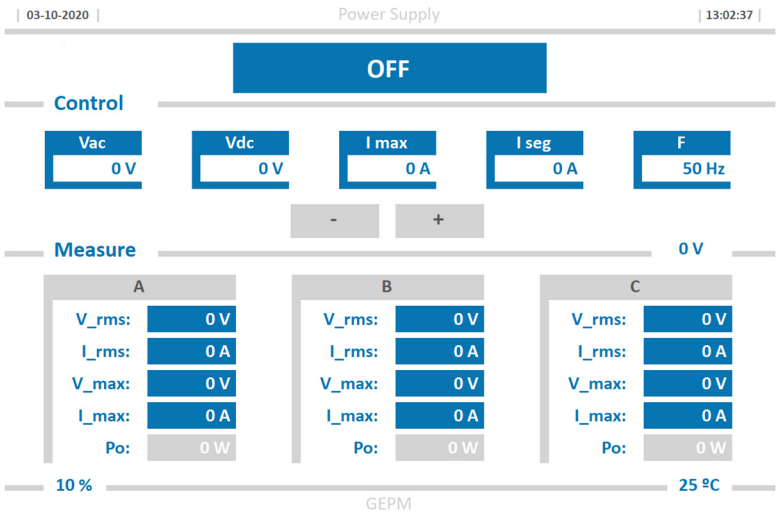


Fig. 5.11 Main control window of the control software of the user interface. From top to bottom: output activation button, control parameters, measurements, and cooling system control.

Finally, the experimental waveforms of the output voltage of the three-phase bidirectional power supply are depicted in Fig. 5.12. In particular, each phase is delivering 230-V ac voltage shifted 120 º, as in a conventional three phase connection.

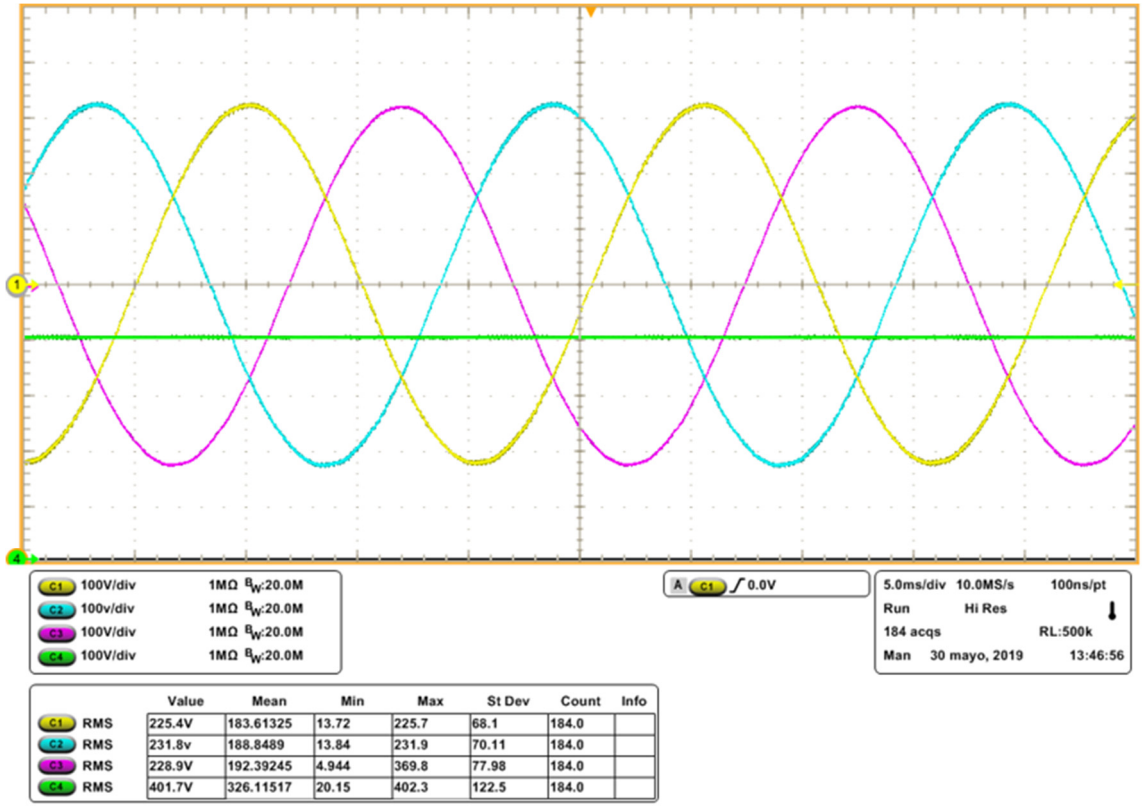


Fig. 5.12 Sinusoidal voltage waveforms of the three-phase bidirectional power supply with 800-V bus voltage and emulating a conventional three-phase system, i.e. 230-V and 50-Hz ac voltage. From top to bottom: the output voltages $v_{o,AN}$ (yellow), $v_{o,BN}$ (blue), and $v_{o,CN}$ (purple), and the output voltage of N^{th} module, $v_{o,N}$, (green). Voltage: 100 V/div. Time: 5 ms/div.

5.2. Single-phase PFC rectifier

In the previous section, the implementation of a versatile, controllable, and bidirectional three-phase power supply has been carried out to power the single-phase and multi-phase PFC rectifiers prototypes, and to enable the development and test of their modulation strategies that have been proposed in before Chapters. In this section, the implementation of the single-phase PFC rectifier and its modulation and control strategies are addressed in order to prove the proper operation of the rectifier and collect relevant information for its posterior analysis. Finally, a domestic IH example is performed using the proposed converter. The block diagram of Fig. 5.13 summarizes the scheme of this application.

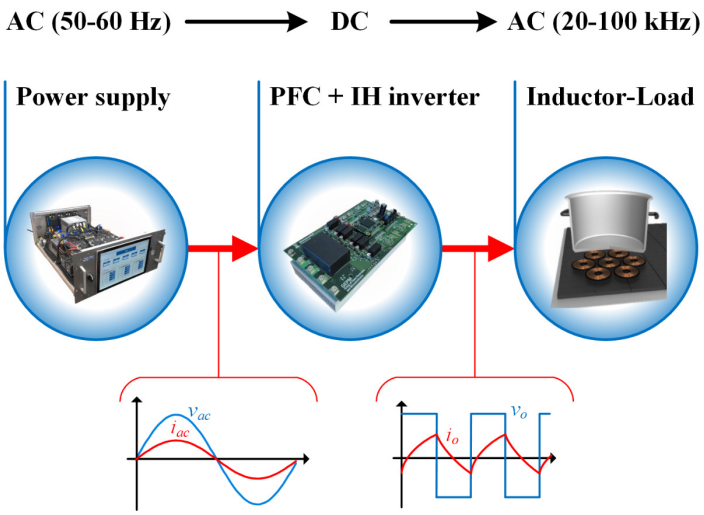


Fig. 5.13 Block diagram of the experimental implementation of the single-phase PFC rectifier for domestic IH applications.

5.2.1. PFC rectifier implementation

In order to perform and analyze each proposed strategy, a versatile platform has been designed and implemented. The prototype, shown in Fig. 5.14, is composed of a three half-bridge CCS050M12CM2 module from CREE using 1200-V and 25-mΩ SiC MOSFETs. A Spartan-6 FPGA from Xilinx is used to implement the control architecture. Besides, the whole system can be controlled from the PC through a Wi-Fi module and a PC application has been developed using Visual Basic. The platform allows measuring current, using magneto-resistive current sensors, and voltage, using voltage dividers. To perform these measurements, the CMS3050ABA current sensors from Sensitec and the 12-Bit and 10-MSPS LTC1420 parallel ADC from Linear Technology have been used. TABLE 5.3 summarizes the main converter design parameters.

TABLE 5.3

CONVERTER DESIGN PARAMETERS

PARAMETER	VALUE
Mains voltage, $V_{ac,rms}$	230 V RMS, 50 Hz
Input power range, P_{in}	500-3680 W
Bus voltage, v_b	400 V
Operating frequency, f_{sw}	40-180 kHz
Filter capacitor, C_f	5 µF
Filter inductance, L_f	50 µH (HS) 215 µH (ZVS)
Bus capacitor, C_b	1140 µF
Boost inductance, L_b	215 µH (HS) 26 µH (ZVS)

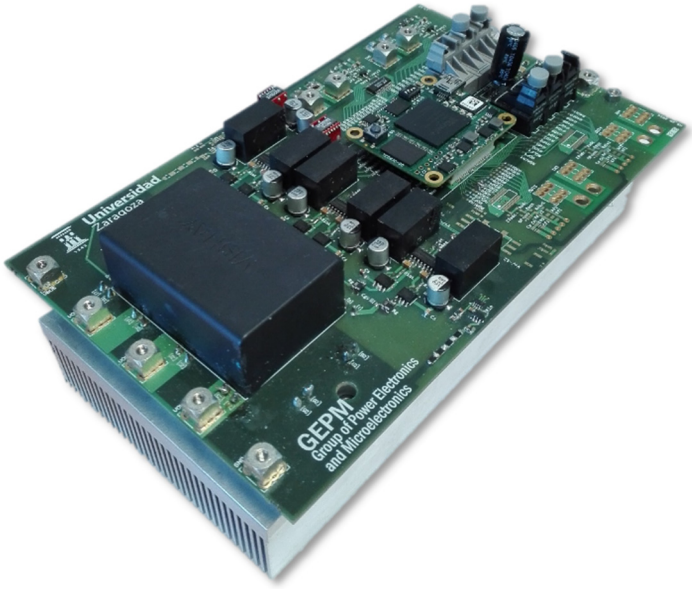


Fig. 5.14 Versatile platform prototype for the implementation of the single-phase PFC rectifier and its modulation strategies.

The boost inductors for HS and ZVS modulation strategies have been implemented in order to fulfill the requirements of inductance value, saturation current, and low losses, among others. In order to do this, different core materials and wires have been used. TABLE 5.4 summarizes the main parameters of these inductors. The ZVS boost inductor has been made using ferrite cores and Litz wire to decrease high frequency losses. A 3.2-mm gap has been implemented to increase the saturation current. The HS boost inductor, which is shown in Fig. 5.5, has been made using multi-strand wire and a kool Mµ core in

order to get high inductance value and decrease the current ripple. The ZVS inductor has also been used for DCM strategies because they have similar requirements due to the high current ripple.

TABLE 5.4

BOOST INDUCTORS DESIGN PARAMETERS

PARAMETER	ZVS BOOST INDUCTOR	HS BOOST INDUCTOR
Inductance, L_b	26 µH	215 µH
Saturation current, I_{sat,L_b}	100 A	50 A
50-Hz resistance, $R_{L_b LF}$	9 mΩ	32 mΩ
60-kHz resistance, $R_{L_b,HF}$	30 mΩ	380 mΩ
Wire	Litz	Multi strand
Wire material	Copper	Copper
Wire section	3.24 mm^2	2.5 mm^2
Number of turns	7	22
Number of strands	1650	41
Strand diameter	50 µm	278 µm
Core	2 x ELP65/10/50 2 x I65/5/50	2 x Toroid 60x32x26
Core material	N87 ferrite	Kool Mµ
Dimensions	16 x 6.5 x 1.8 cm	8 x 8 x 6.5 cm
Volume	195 cm^3	330 cm^3

Fig. 5.15 Boost inductor for HS CCM modulation strategies.

Fig. 5.16 to Fig. 5.20 show the experimental results obtained using each modulation strategy with half-bridge and full-bridge topology configurations. For each modulation strategy, the main waveforms in a mains cycle, i.e. 230-V voltage and 50-Hz frequency, are shown along with a detailed view for a selected bus voltage equal to 400 V. Moreover, the measured efficiency and the simulated power loss distribution at maximum power, i.e. 3680 W, are shown in the lower right corner. In the power loss distribution chart, the switching losses of switching devices, $P_{sw,S}$, the conduction losses of switching devices, $P_{on,S}$, the boost-inductor losses, P_{on,L_b}, the bus capacitor losses, P_{on,C_b}, and the filter losses, $P_{on,L_f} + P_{on,C_f}$, have been taken into account.

The fixed frequency strategies operate at 60 kHz, whereas the variable frequency strategies operate between 35 and 150 kHz. For all ZVS strategies, a 26-µH boost inductor and 215-µH filter inductor have been used, whereas a 215-µH boost inductor and 50-µH filter inductor has been used for all HS strategies.

As it can be seen, zero-cross distortion appears when the half-bridge configurations are used, whereas it is avoided with the full-bridge configurations. On the other hand, the boost current ripple increases which leads to additional conduction and switching losses in the switching devices since the turn-off current is higher. For these reasons, the efficiency decreases slightly. The DCM operation mode, however, avoids the zero-cross distortion with the half-bridge configuration. Consequently, the full-bridge and hybrid configuration are less interesting in this case. With this operation mode, a small oscillation of the current is appreciated due to the diode parasitic capacitance coupled with the boost coil.

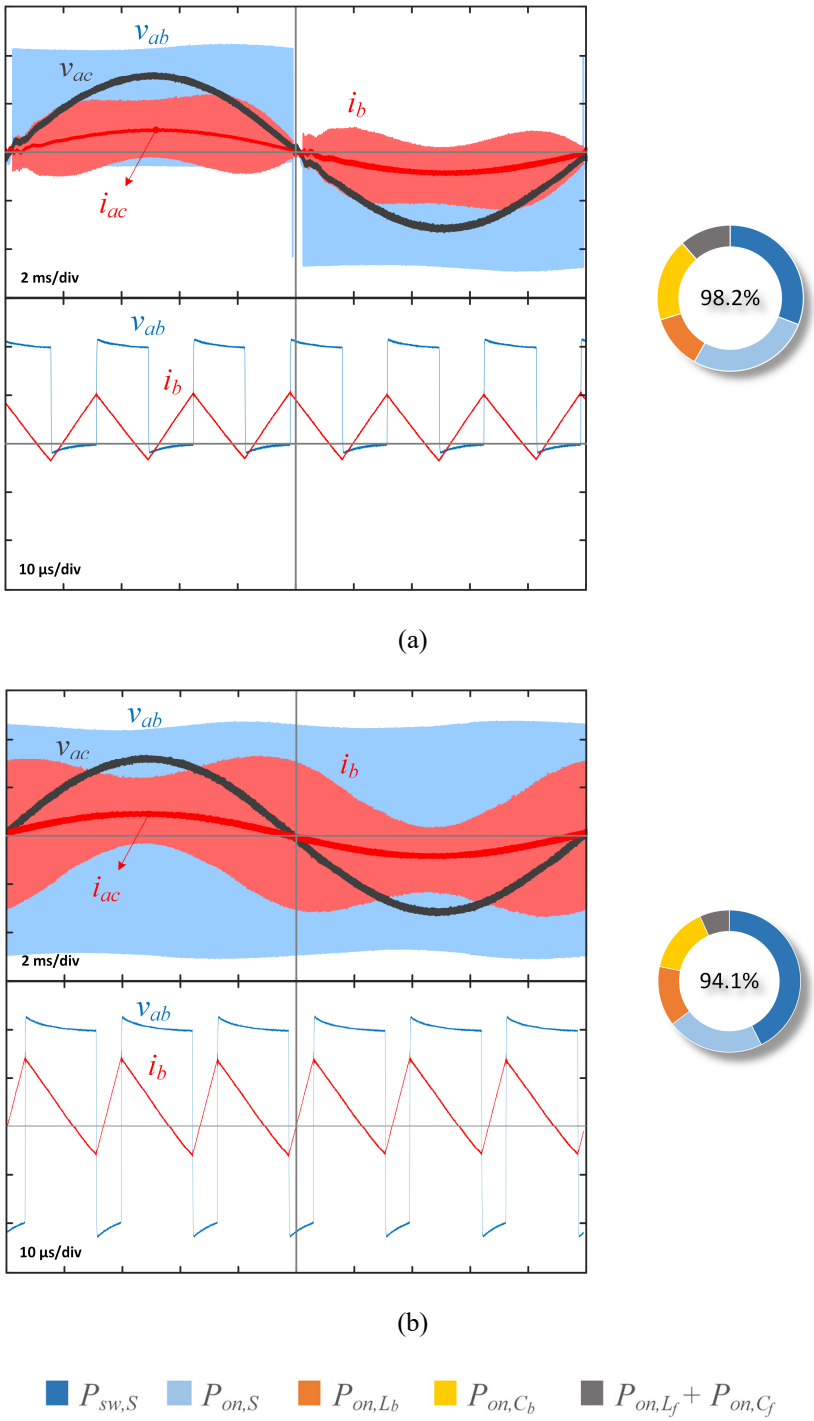


Fig. 5.16 The ZVS FF CCM using (a) half-bridge and (b) full-bridge topology configurations. On top, the main experimental waveforms (voltage: 200 V/div, current: 50 A/div, and time: 2 ms/div). On bottom, a detail view (time: 10 µs/div). On the right side, the overall efficiency and the power loss distribution at maximum power, 3680 W.

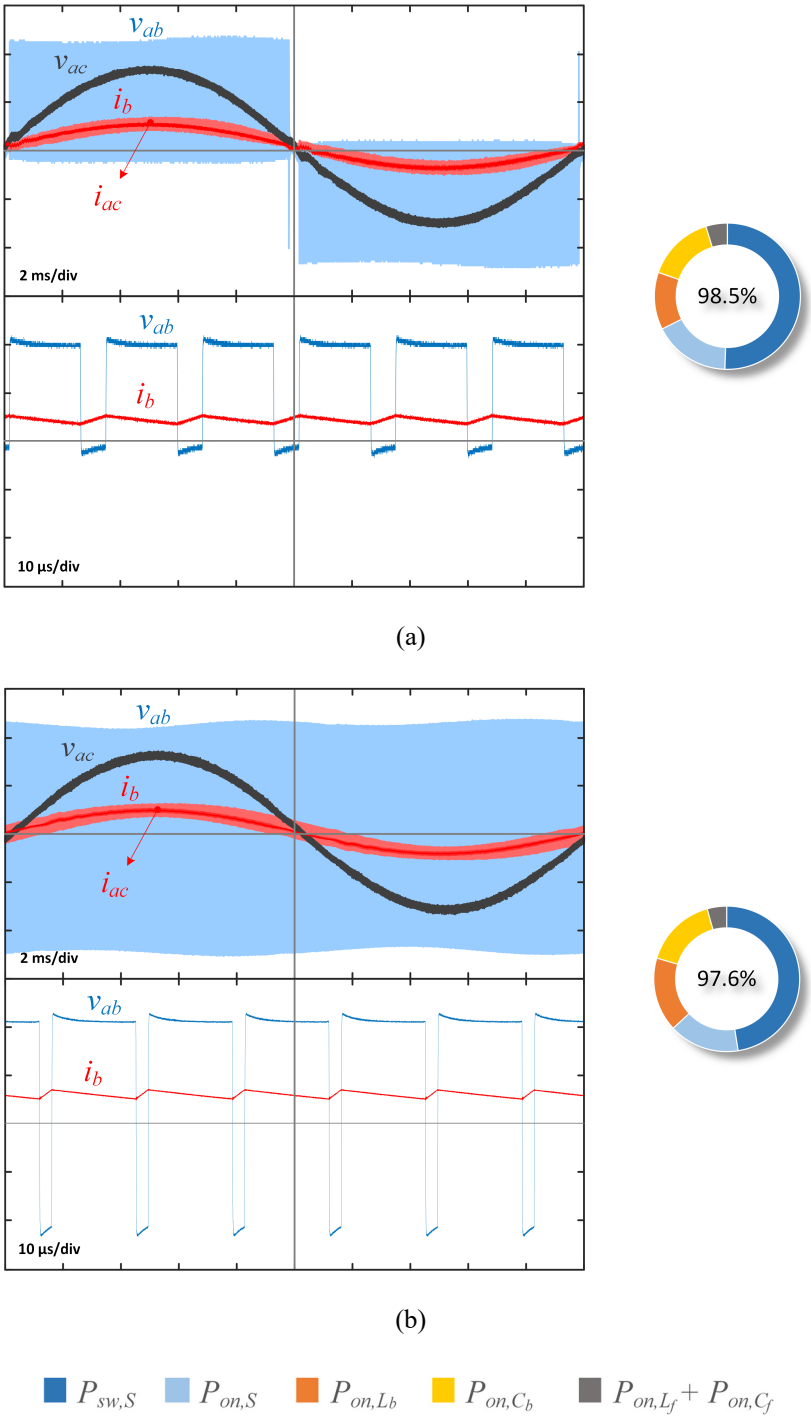


Fig. 5.17 The HS FF CCM using (a) half-bridge and (b) full-bridge topology configurations. On top, the main experimental waveforms (voltage: 200 V/div, current: 50 A/div, and time: 2 ms/div). On bottom, a detail view (time: 10 µs/div). On the right side, overall efficiency and the power loss distribution at maximum power, 3680 W.

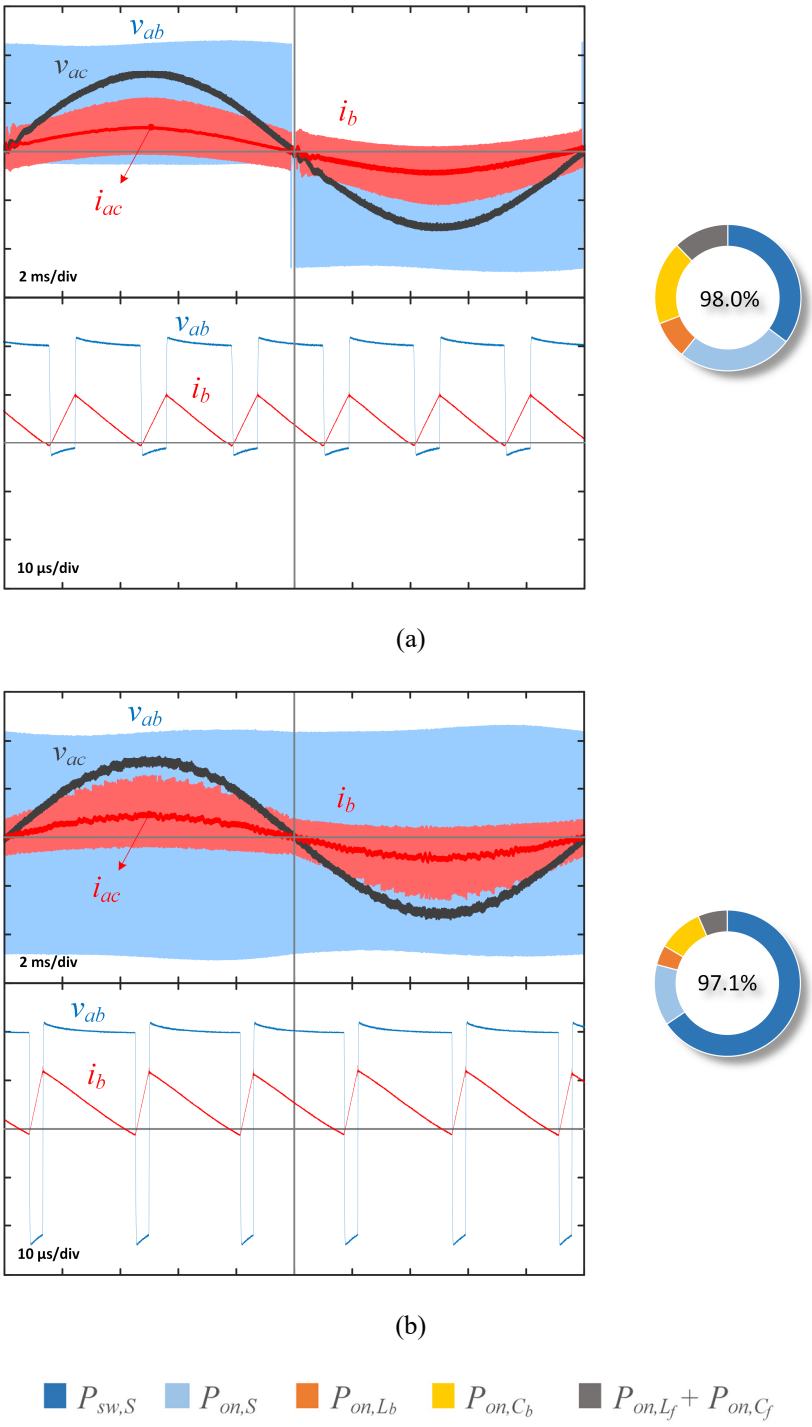


Fig. 5.18 The ZVS VF CCM using (a) half-bridge and (b) full-bridge topology configurations. On top, the main experimental waveforms (voltage: 200 V/div, current: 50 A/div, and time: 2 ms/div). On bottom, a detail view (time: 10 µs/div). On the right side, the overall efficiency and the power loss distribution at maximum power, 3680 W.

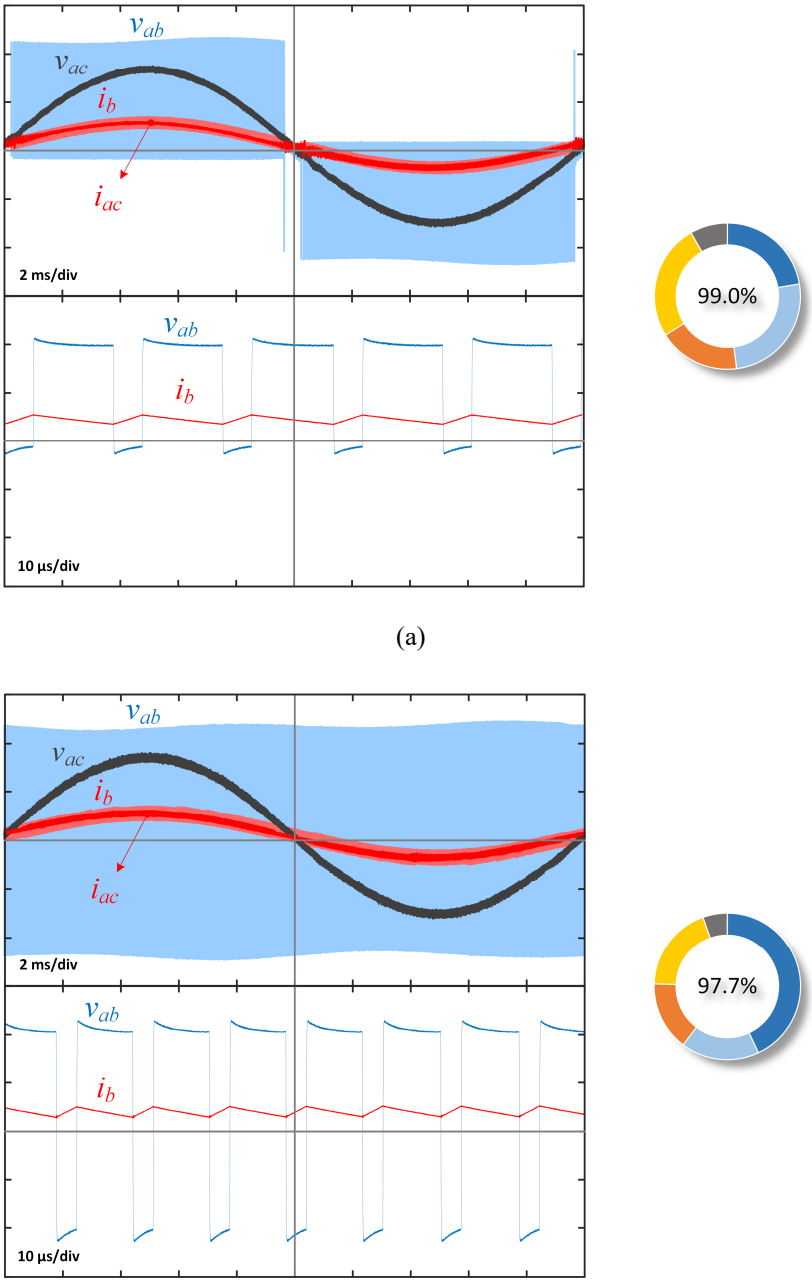
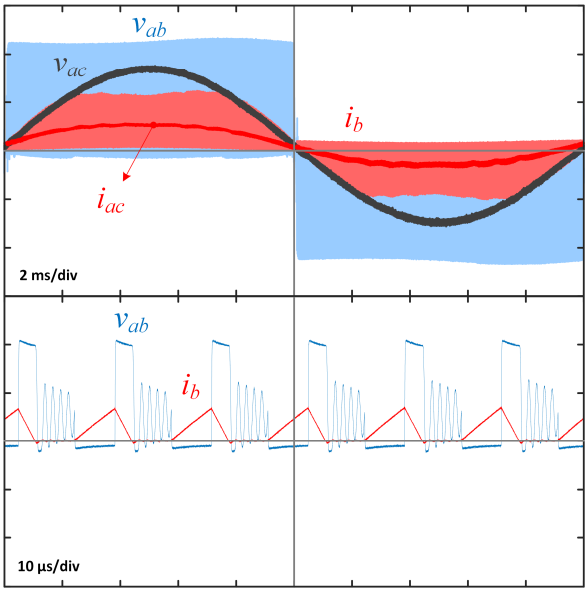
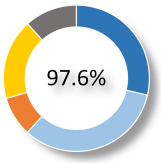
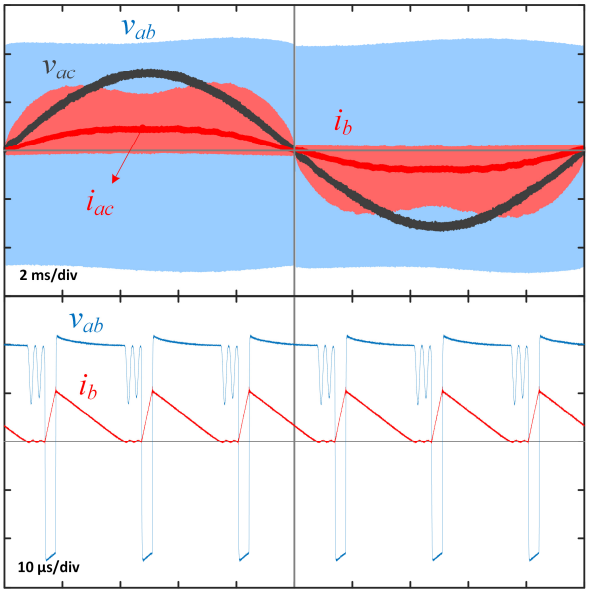


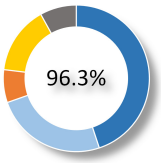
Fig. 5.19 The HS VF CCM using (a) half-bridge and (b) full-bridge topology configurations. On top, the main experimental waveforms (voltage: 200 V/div, current: 50 A/div, and time: 2 ms/div). On bottom, a detail view (time: 10 µs/div). On the right side, the overall efficiency and the power loss distribution at maximum power, 3680 W.





(a)

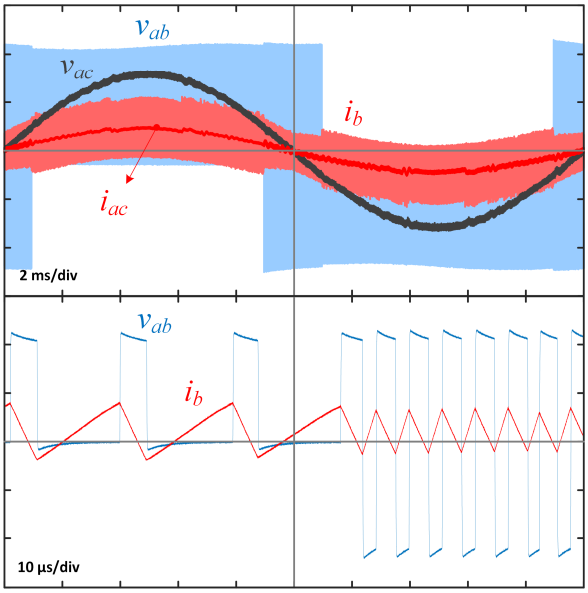


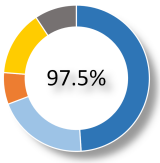


(b)

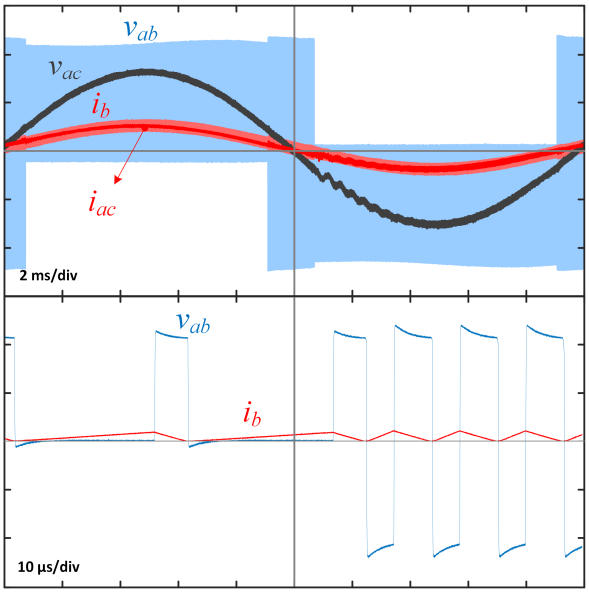
Fig. 5.20 The FF DCM using (a) half-bridge and (b) full-bridge topology configurations. On top, the main experimental waveforms (voltage: 200 V/div, current: 50 A/div, and time: 2 ms/div). On bottom, a detail view (time: 10 µs/div). On the right side, the overall efficiency and the power loss distribution at maximum power, 3680 W.

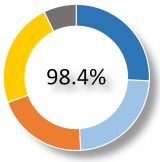
The variable frequency strategies using hybrid configuration have been also implemented (Fig. 5.21). In both cases, ZVS and hard switching strategy, the zero-cross distortion is avoided because the full-bridge configuration is used when the absolute value of the mains voltage is lower than 100 V. The detailed view shows the moment at which this change is performed.





(a)

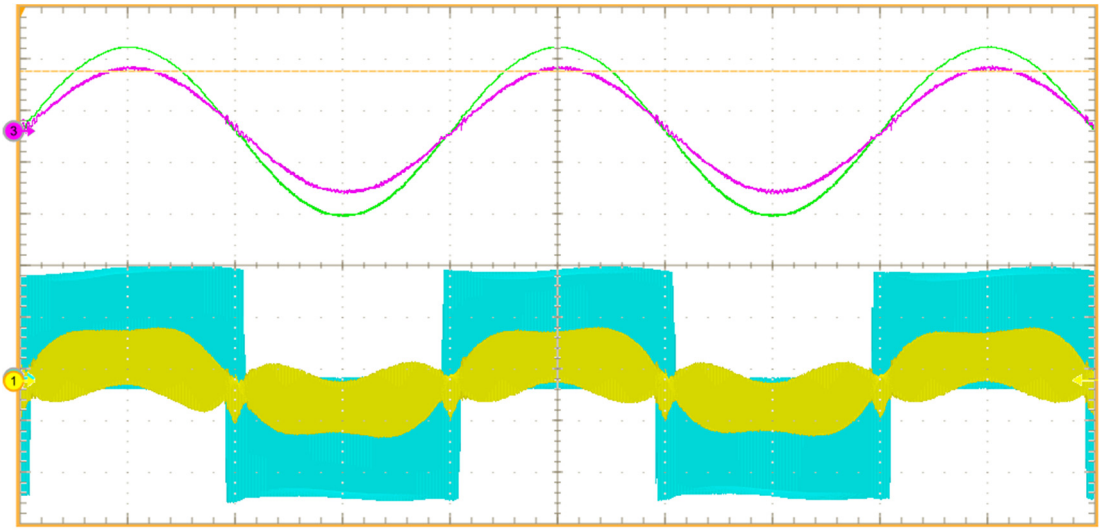




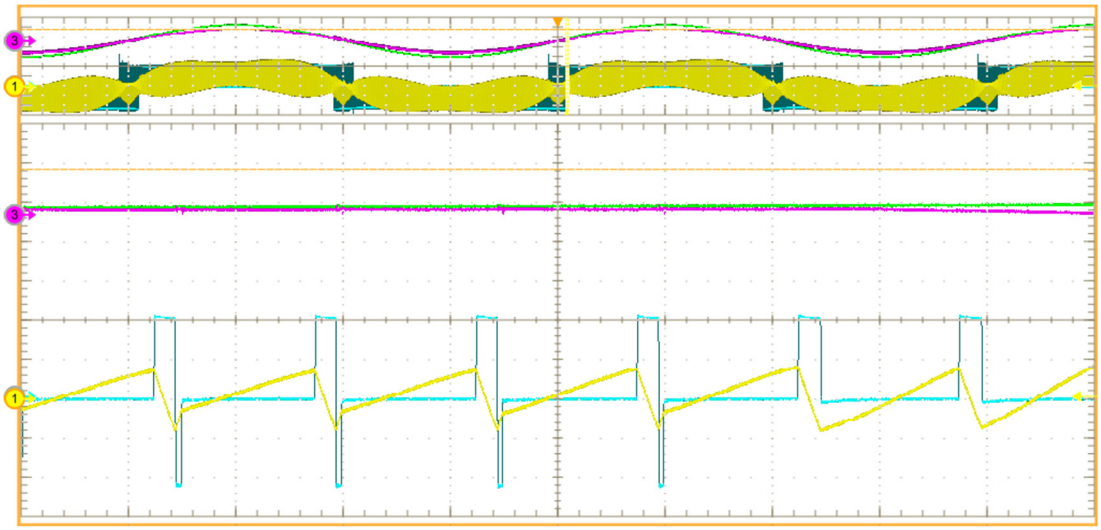
(b)

Fig. 5.21 The (a) ZVS VF CCM and (b) HS VF CCM using hybrid topology configuration. On top, the main experimental waveforms (voltage: 200 V/div, current: 50 A/div, and time: 2 ms/div). On bottom, a detail view (time: 10 µs/div). On the right side, the overall efficiency and the power loss distribution at maximum power, 3680 W.

The proposed soft-transient modulation strategy to perform the control of hybrid FF modulation strategies is shown in Fig. 5.22 and Fig. 5.23 for ZVS and HS cases, respectively. The oscilloscope screenshots include the experimental waveforms of the converter operating at 67 kHz and at maximum power, i.e. 3.7 kW, along with a detail view of the transition. It can be appreciated that the rectifier branch works at the switching frequency with a phase shift, α. In both cases, the power factor is higher than 0.99 and the zero-cross distortion is avoided because the full-bridge configuration is used, fulfilling the EMC standards with a current total harmonic distortion (THD_i) lower than 1%.

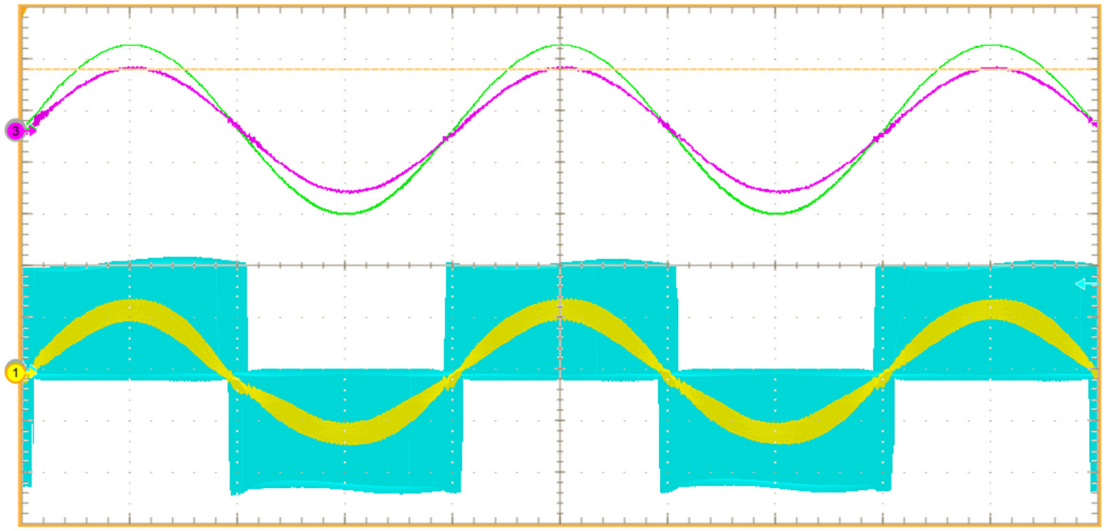


(a)

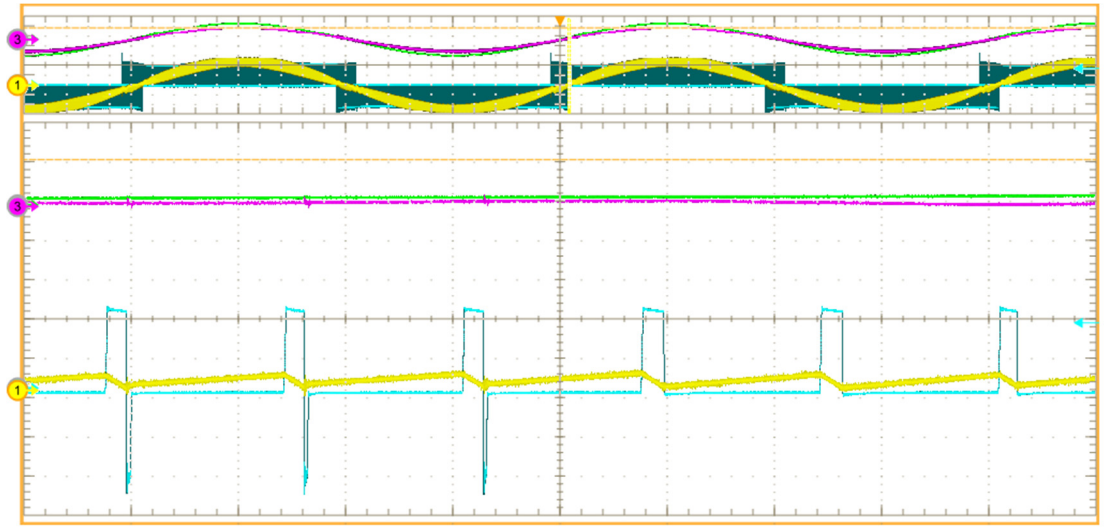


(b)

Fig. 5.22 The ZVS FF CCM and soft-transient modulation strategy using hybrid topology configuration. From top to bottom. the main experimental waveforms: v_{ac} (200 V/div, green), i_{ac} (20 A/div, purple), v_{ab} (200 V/div, blue), and i_b ((a) 50 A/div and (b) 20 A/div, yellow). Time: (a) 5 ms/div and a detail view (b) 10 µs/div.



(a)



(b)

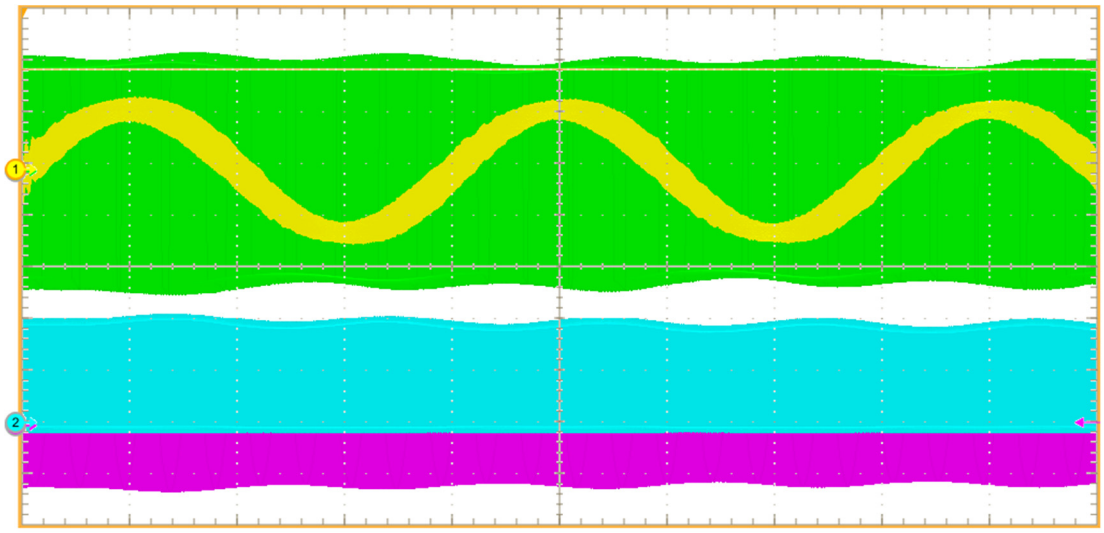
Fig. 5.23 The HS FF CCM and soft-transient modulation strategy using hybrid topology configuration. From top to bottom: the main experimental waveforms: v_{ac} (200 V/div, green), i_{ac} (20 A/div, purple), v_{ab} (200 V/div, blue), and i_b ((a) 20 A/div and (b) 10 A/div, yellow). Time: (a) 5 ms/div and a detail view (b) 10 µs/div.

5.2.2. Application to domestic IH

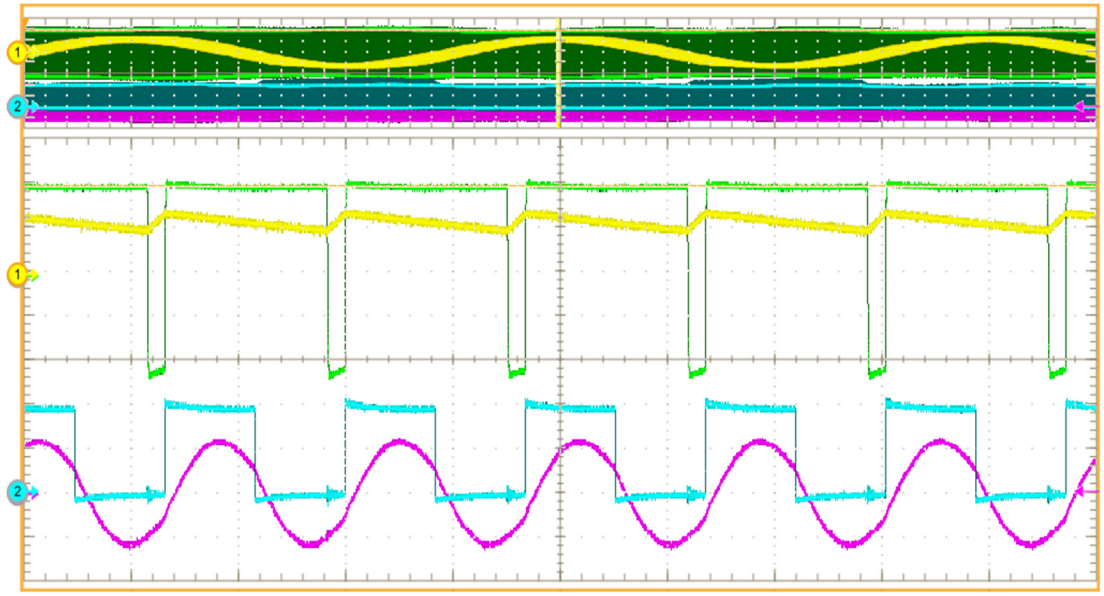
The implemented platform has been used to power an IH load using the third available inverter branch of the power module available in the PFC board. The inductor-load system consists of a 5-Ω equivalent series resistance, R_{eq}, and 80-µH equivalent series inductor, L_{eq}. A 170-nF resonant capacitor has been placed in order to obtain a 45-kHz resonant frequency.

According to the obtained measurements and, as it is discussed later in comparative analysis of Chapter 6, the HS FF CCM modulations strategy has been selected due to its performance. Besides, it avoids acoustic noise due to it works at a fixed frequency

synchronized with the IH-inverter and the zero-cross distortion using full-bridge or hybrid configurations. For this reason, it has been selected as the preferred one for this application. Fig. 5.24 depicts the experimental measurements with the converter operating at 60 kHz and maximum power, i.e. 3680 W, using full-bridge configuration.



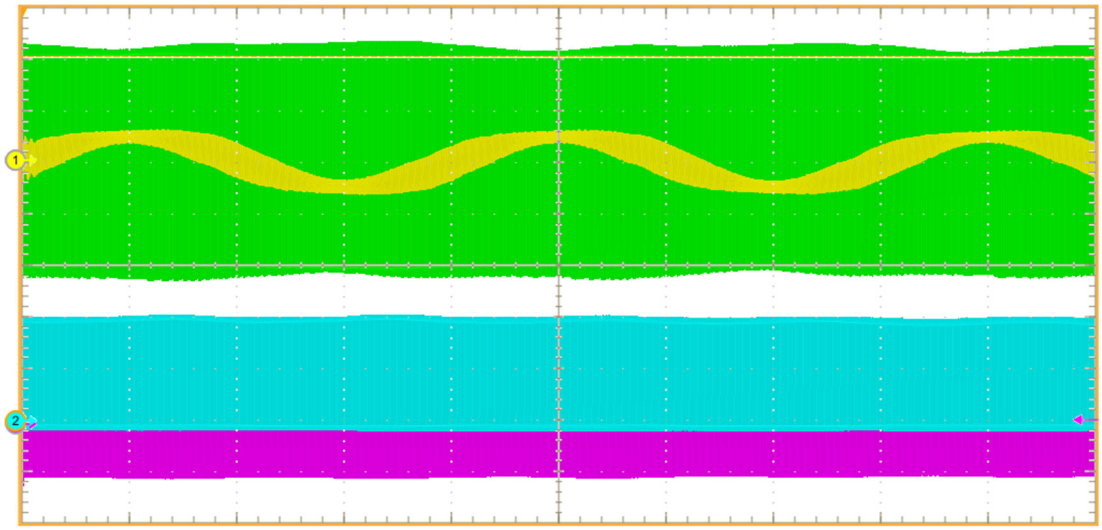
(a)



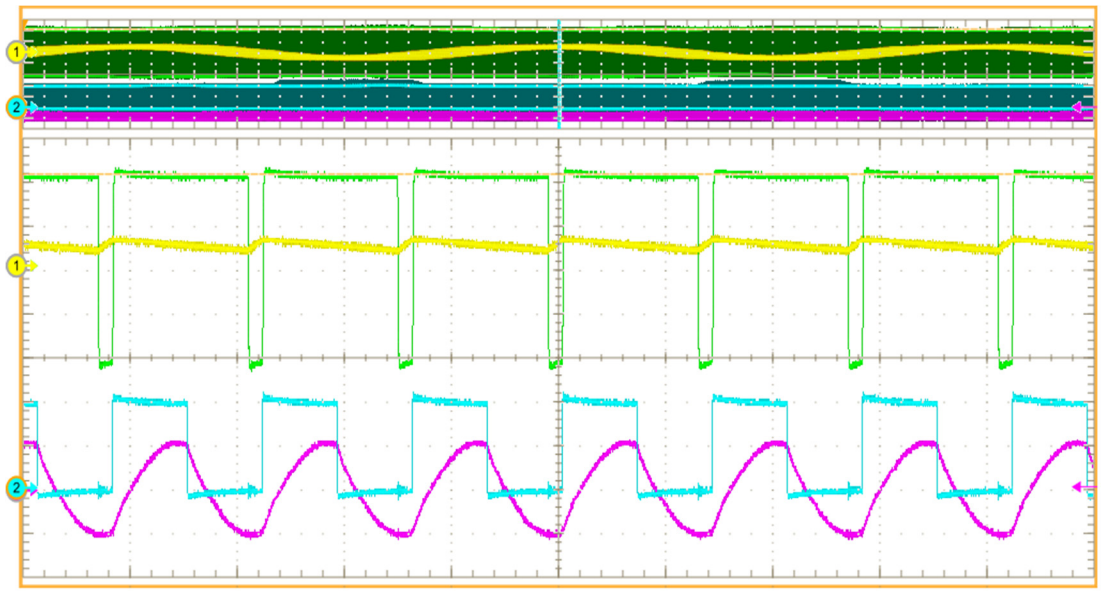
(b)

Fig. 5.24 Main waveforms of the PFC IH converter powering a domestic IH load at maximum power, 3680 W, using full-bridge HS FF CCM modulation strategy. From top to bottom: voltage between a and b branches, v_{ab}, (200 V/div, green), boost-inductor current, i_{ac}, (20 A/div, yellow), output voltage, v_o, (200 V/div, blue), and output current, i_o, (30 A/div, purple). Time: (a) 5 ms/div and (b) 10 µs/div.

In Fig. 5.25, the converter is operating at 71 kHz at medium power, i.e. 1500 W. The main waveforms of the PFC and the IH load are shown along with a detailed view.



(a)



(b)

Fig. 5.25 Main waveforms of the PFC IH converter powering a domestic IH load at medium power, 1500 W, using full-bridge HS FF CCM modulation strategy. From top to bottom: voltage between a and b branches, v_{ab}, (200 V/div, green), boost-inductor current, i_{ac}, (20 A/div, yellow), output voltage, v_o, (200 V/div, blue), and output current, i_o, (20 A/div, purple). Time: (a) 5 ms/div and (b) 10 µs/div.

5.3. Multi-phase PFC rectifier

In the previous section, the implementation of the single-phase PFC rectifier and its modulations strategies has been presented along with a domestic IH application. The experimental results prove the feasibility of the proposed converter and the control strategies.

In this section, the implementation of the multi-phase PFC rectifier and its modulation strategies is addressed in order to prove the proper operation of the rectifier and collect relevant information for its posterior analysis. In this prototype design, the maximum power density is pursued in order to fulfill the requirements of the final IH application. As a result, the power device technology and size of passive components, such as inductors and capacitors, have been selected or designed to decrease the converter overall dimensions.

Besides, an application to domestic IH is performed using a multi-output IH inverter. For doing this, the implementation of a matrix converter is carried out, focusing in the topology and the prototype implementation. Finally, the matrix converter and the multi-phase rectifier are connected to power a 11-kW IH load. The block diagram of Fig. 5.26 summarizes the scheme of this application.

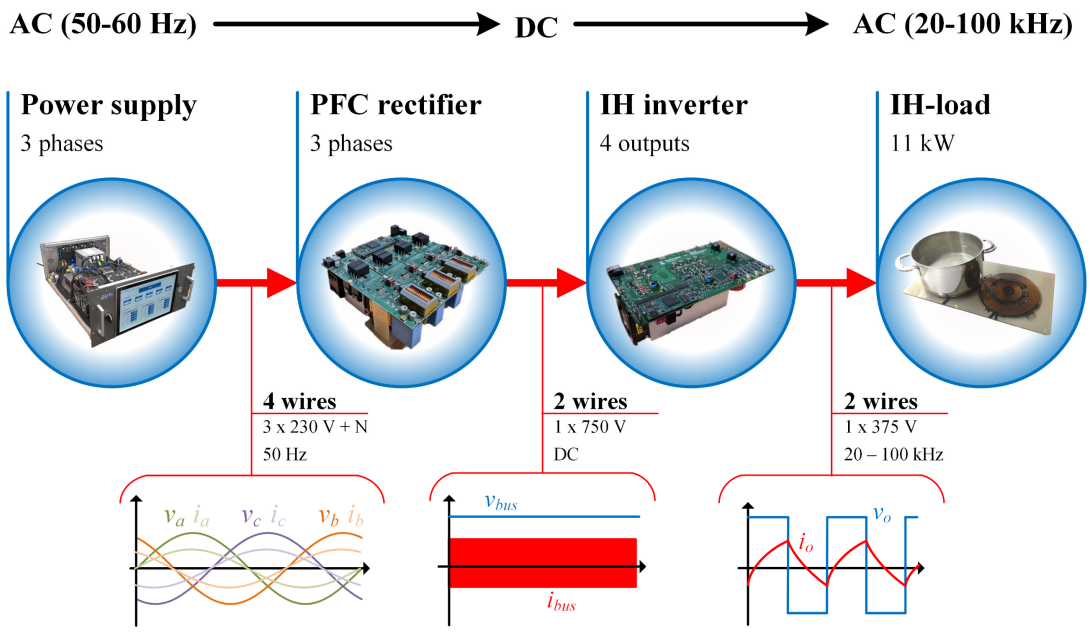


Fig. 5.26 Block diagram of the experimental implementation of the multi-phase PFC rectifier and the matrix inverter powering a 11-kW load for domestic IH applications.

5.3.1. PFC rectifier implementation

In order to experimentally verify the proposed multi-phase PFC rectifier and its modulation strategies, a versatile 11-kW and 2-dm^3 platform with up to three input mains phases, i.e. n = 3, has been designed and implemented, getting a 5.5-kW/dm^3 power density. The prototype, shown in Fig. 5.27, is composed of four half-bridge branches, implemented using 40-mΩ and 1200-V SiC MOSFETs C2M0040120D from CREE with TO-247-3 package. The power losses are dissipated using forced-air cooling. A Zynq XC7Z020 FPGA from Xilinx is used to implement the control architecture. Besides, the whole system can be managed from the PC through an optical fiber module to provide isolation and a PC application developed using Visual Basic. The platform allows measuring current using magneto-resistive current sensors and voltage using voltage dividers. 12-Bit and 10-Msps LTC1420 ADCs from Linear Technology and the CMS3050ABA current sensors from Sensitec are implemented. Besides, a 22-µH HA55L-3623220LF inductor from TT Electronics has been used as filter inductor. TABLE 5.5 summarizes the main converter design parameters.

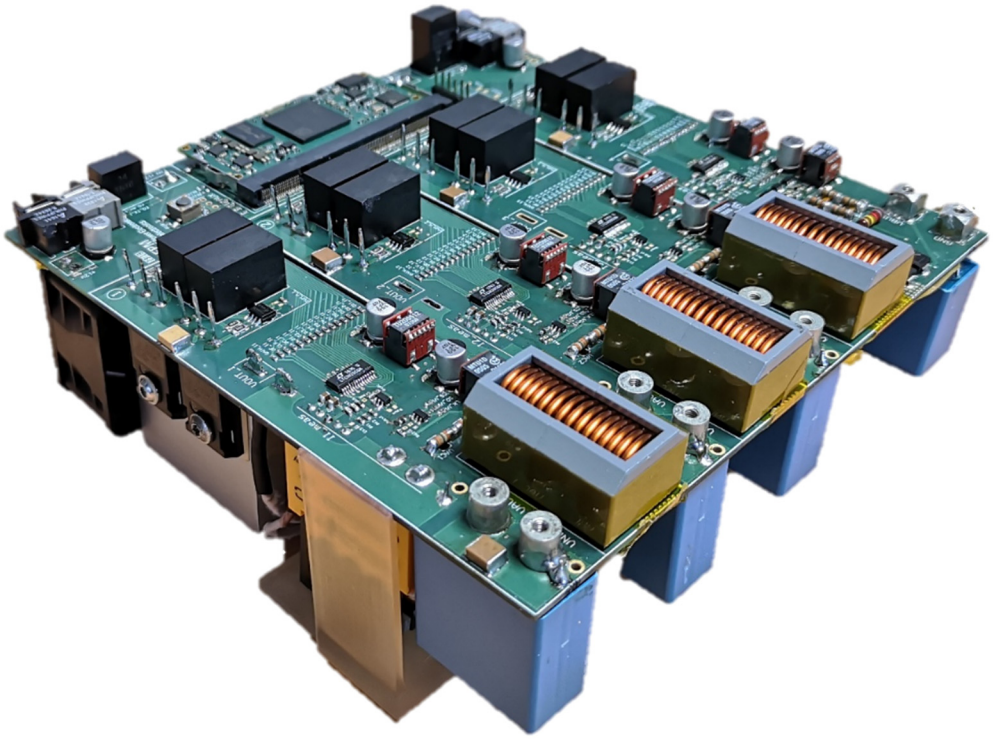


Fig. 5.27 11-kW three-phase high power-density PFC rectifier for domestic IH applications. The dimensions are 17 cm, 17 cm, and 7 cm, getting more than 5.5 kW/dm^3 including the forced-air cooling, the boost and balancing inductors, and the input filter.

TABLE 5.5

MULTI-PHASE PFC RECTIFIER DESIGN PARAMETERS

PARAMETER	VALUE
Input mains phases, n	1, 2, or 3
Mains phase voltage, v_i	230 V RMS, 50 Hz
Input phase power, $P_{in,i}$	3.6 kW
Total input power, P_{in}	11 kW
Bus voltage, v_b	750 V
Operating frequency, $f_{sw,i}$	100 kHz (FF), 30-330 kHz (VF)
Filter capacitor, $C_{f,i}$	10 µF
Filter inductance, $L_{f,i}$	22 µH
Bus capacitor, C_b	560 µF
Boost inductance, L_i	110 µH (HS), 10 µH (ZVS)
Balancing inductance, L_0	110 µH (HS), 41 µH (ZVS)

The boost and balancing inductors have been designed to fulfill the requirements of the studied modulation strategies. Two different inductor sets have been implemented depending on the selected switching mode. Each inductor is composed of two E42/21/15 ferrite cores in parallel, along with a I43/4/28 ferrite core to close the magnetic circuit. A 3.2-mm air gap has been implemented to increase the saturation current. Different copper Litz wires have been used to optimize the coil in order to get the maximum inductance value, the minimum power losses, and the minimum volume fulfilling the saturation current at maximum power. The power losses of these elements are dissipated using the same forced-air cooling.

The requirements of the boost and balancing inductors of HS modulation strategies are similar. However, the requirements of the ZVS modulation strategies are determined by the ZVS FF CCM, because this modulation strategy is the most restrictive one due to the increased current. Fig. 5.28 shows an example of the implemented inductor for HS modulation strategies and Fig. 5.29 shows a finite element analysis (FEA), which proves the proper operation of the converter thermal design. TABLE 5.6 summarizes the main parameters of these fundamental components according to the switching mode. ZVS inductors have also been used for the DCM strategy because they have similar requirements due to the high current ripple.

Fig. 5.28 Implemented boost and balancing inductors for HS modulation strategies. It features 110-µH inductance and 55-A saturation current. The dimensions are 4.3 cm, 4.7 cm, and 2.8 cm, obtaining a 57-cm^3 volume. The maximum power losses operating at 11 kW are estimated in 13 W.

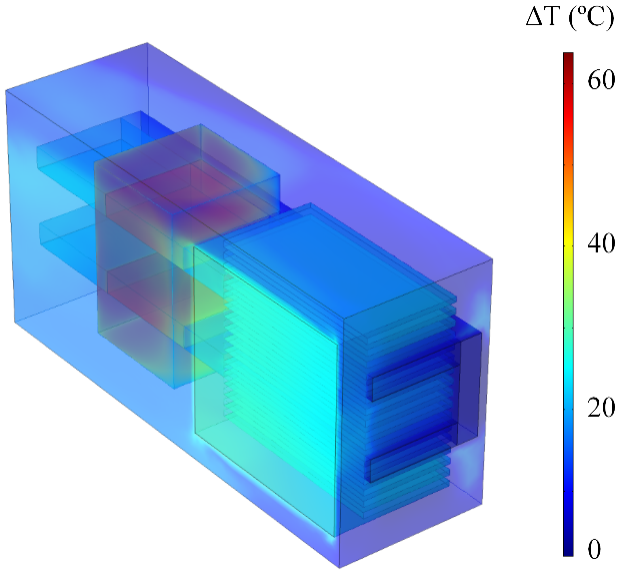


Fig. 5.29 Finite element analysis of the converter thermal design. The forced-air cooling system including the boost inductor and the heat sink has been simulated using the worst case. The color bar indicates the temperature increase (ΔT). The maximum temperature increase is 65 ºC for the inductor, and 60 ºC for the junction of the transistor taking into account the thermal resistance of the thermal pad (0.3 ºC/W) and the transistor case (0.4 ºC/W).

TABLE 5.6

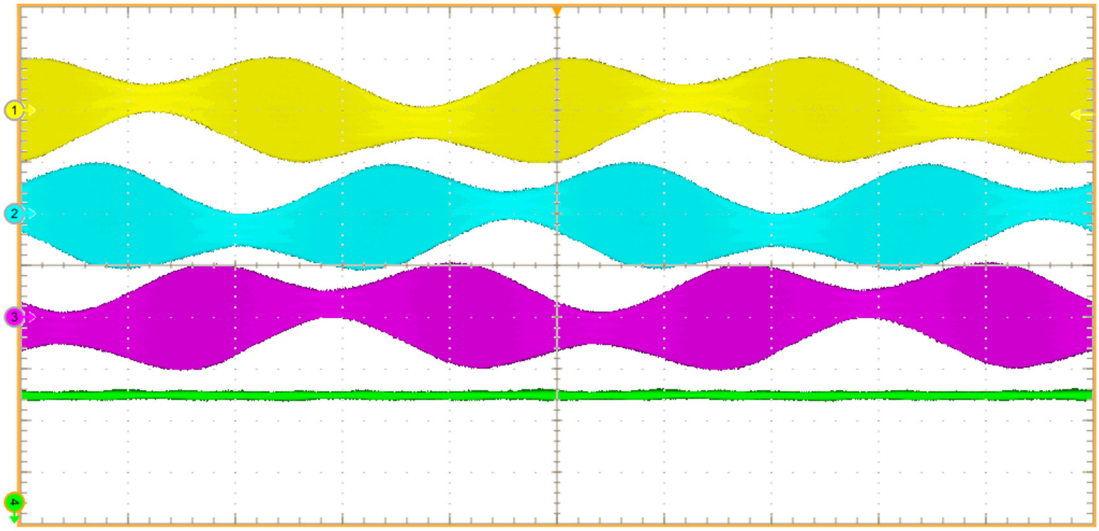
BOOST, L_1, AND BALANCING, L_0, INDUCTOR DESIGN PARAMETERS

Switching Mode	HS	ZVS	
Inductor	L_0 and L_i	L_0	L_i
Inductance (μH)	110	41	10
Saturation current (A)	55	63	120
50-Hz resistance (mΩ)	43	17	5
100-kHz resistance (mΩ)	120	41	12
Number of turns	25	16	6
Number of strands	825	1200	2400
Strand diameter (μm)	50	50	50
Volume (cm^3)	57	57	70

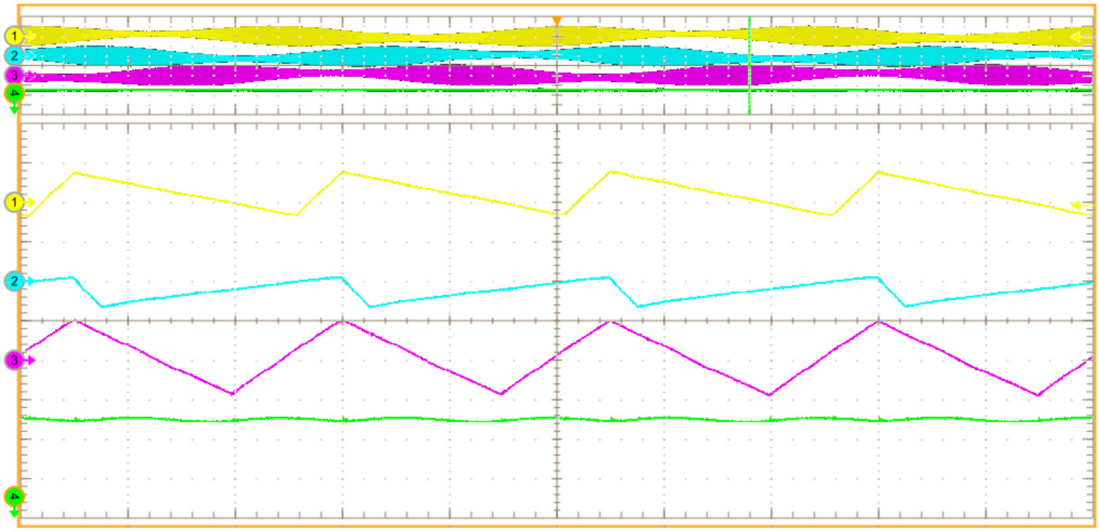
Fig. 5.30 (a) to Fig. 5.34 (a) show the experimental results obtained using the proposed modulation strategies with the converter operating at maximum power, i.e. 11 kW. Each mains phase operates at 230 V and 16 A, i.e. 3.6 kW. In each figure it is shown the boost-inductor current for each phase, $i_{L.i}$, and the bus voltage, v_b, which is established to be 750 V. The resulting bus voltage ripple is low because the three mains phases are activated. In Fig. 5.30 (b) to Fig. 5.34 (b), detailed views are shown.

It is important to note that in the ZVS modulation strategies, the boost-inductor currents always become negative, assuring therefore zero voltage switching during the turn-on transition in contrast to HS modulation strategies. These currents become null in DCM. All the proposed modulation strategies fulfill the EMC requirements with a low THD, without zero-cross distortion, and with a PF close to the unit.

In the ZVS FF CCM (Fig. 5.30), the converter is operating at 100 kHz with a 40-A rms current in the boost inductor, reaching a 100-A peak value, which is lower than the inductor saturation current, i.e. 120 A. This is the most critical case for this component.

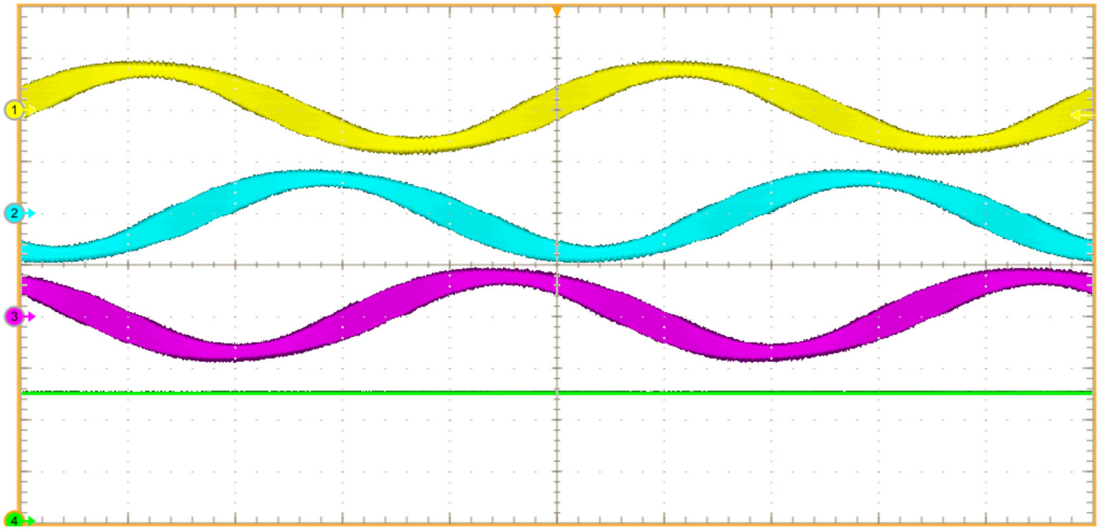


(a)

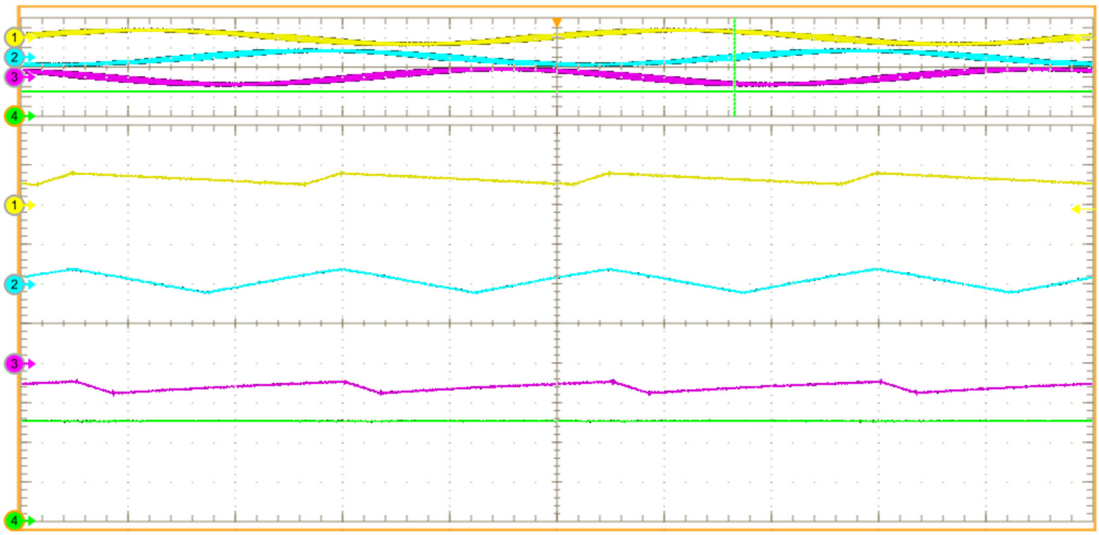


(b)

Fig. 5.30 Main experimental waveforms of the ZVS FF CCM modulation strategy (a) and detailed view (b). From top to bottom: the boost-inductor currents $i_{L,1}$, $i_{L,2}$, and $i_{L,3}$, and the bus voltage, v_b. Voltage: 300 V/div, current: 100 A/div, and time: 4 ms/div (a) and 4 µs/div (b).



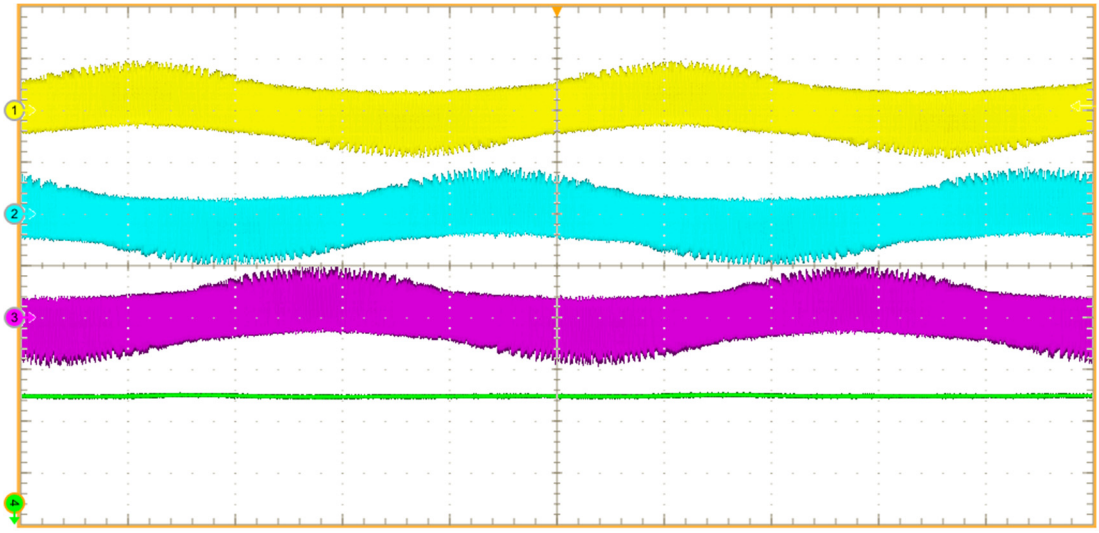
(a)



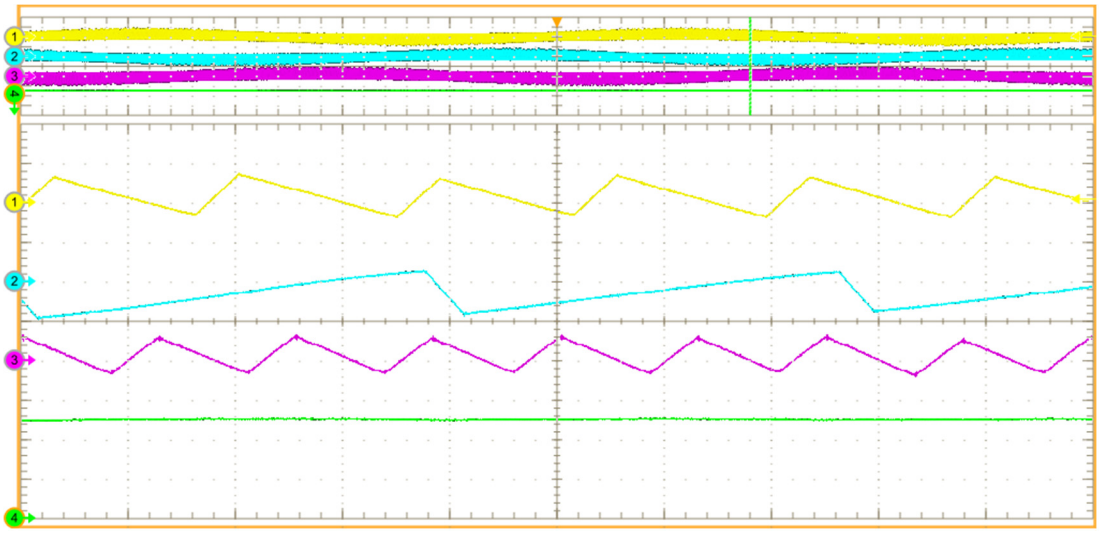
(b)

Fig. 5.31 Main experimental waveforms of the HS FF CCM modulation strategy (a) and detailed view (b). From top to bottom: the boost-inductor currents $i_{L,1}$, $i_{L,2}$, and $i_{L,3}$, and the bus voltage, v_b. Voltage: 300 V/div, current: 30 A/div, and time: 4 ms/div (a) and 4 µs/div (b).

In the HS FF CCM (Fig. 5.31), the boost-inductor current ripple is lower and, therefore, the rms current is similar to the mains phase current, i.e. 15.6 A. The maximum value is lower than 30 A, fulfilling the saturation current too. The operating frequency is 100 kHz, whereas in the ZVS VF CCM (Fig. 5.32) is ranging between 45 kHz and 330 kHz, resulting a 150-kHz average frequency. The rms current is 30 A with maximum values lower than 100 A.



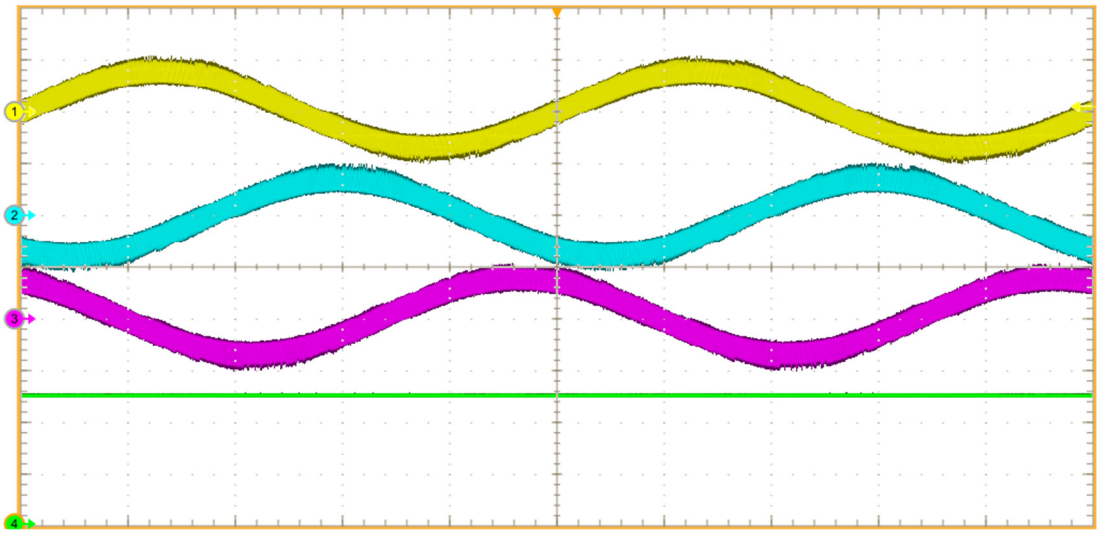
(a)



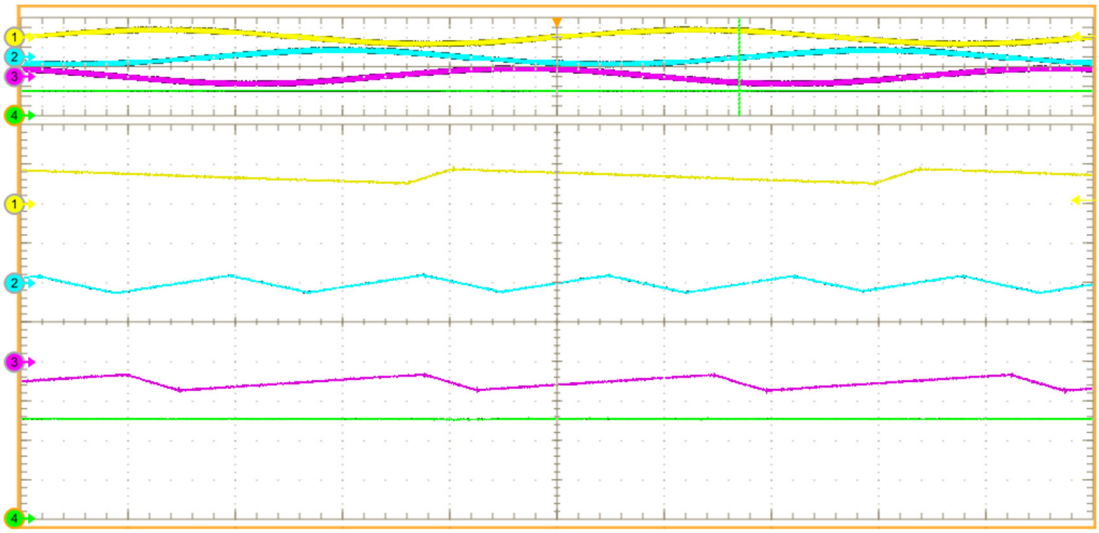
(b)

Fig. 5.32 Main experimental waveforms of the ZVS VF CCM modulation strategy (a) and detailed view (b). From top to bottom: the boost-inductor currents $i_{L,1}$, $i_{L,2}$, and $i_{L,3}$, and the bus voltage, v_b. Voltage: 300 V/div, current: 100 A/div, and time: 4 ms/div (a) and 4 µs/div (b).

The HS VF CCM (Fig. 5.33) is similar to the HS FF CCM. However, in this case, the frequency ranges between 30 kHz and 160 kHz, getting a 95-kHz average frequency. Finally, the FF DCM is shown in Fig. 5.34 with the converter operating at 100 kHz. The rms current in the boost inductor is 23 A, and its maximum value is lower than 80 A.

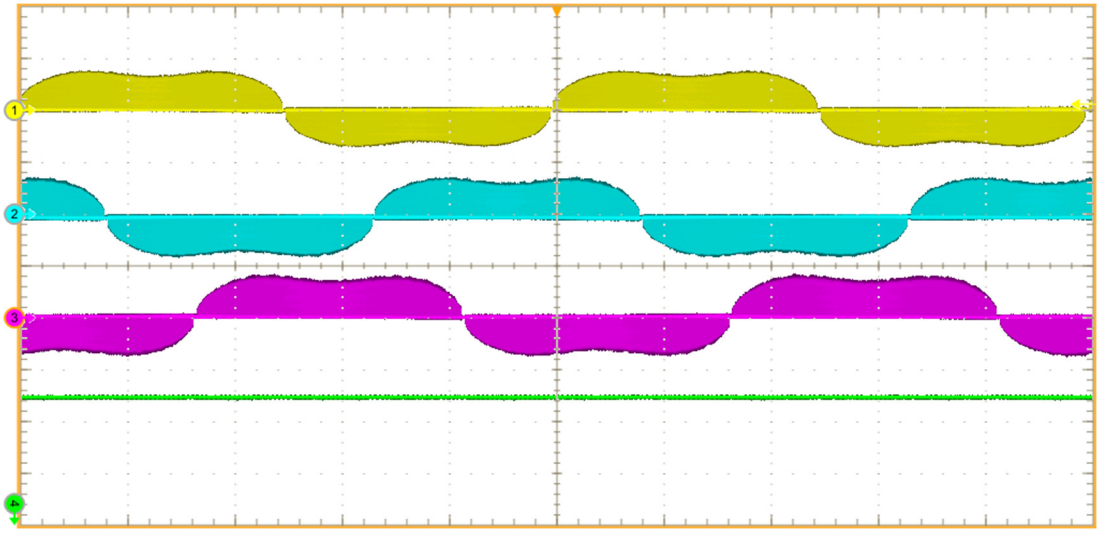


(a)

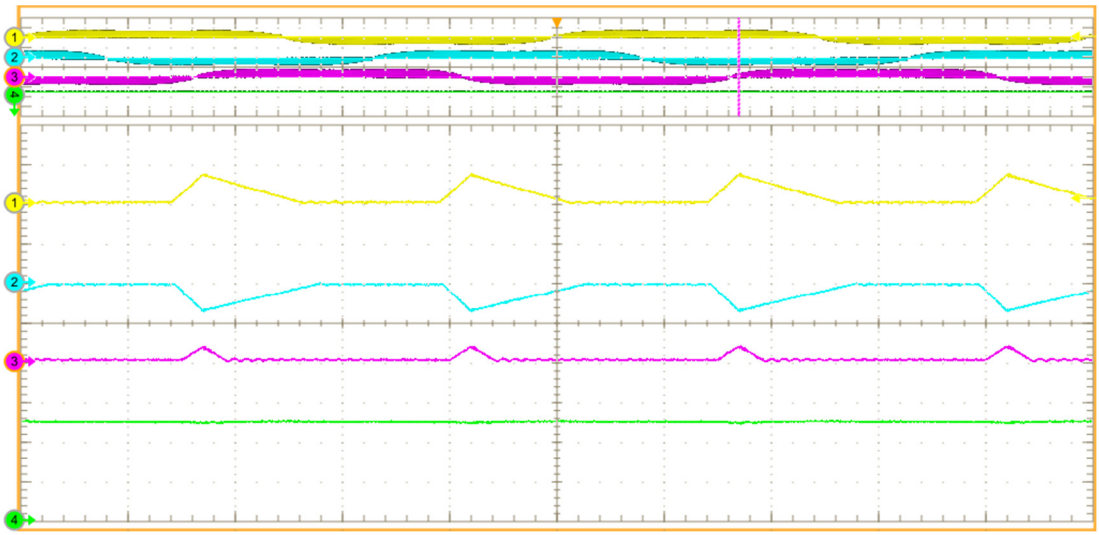


(b)

Fig. 5.33 Main experimental waveforms of the HS VF CCM modulation strategy (a) and detailed view (b). From top to bottom: the boost-inductor currents $i_{L,1}$, $i_{L,2}$, and $i_{L,3}$, and the bus voltage, v_b. Voltage: 300 V/div, current: 30 A/div, and time: 4 ms/div (a) and 4 µs/div (b).



(a)



(b)

Fig. 5.34 Main experimental waveforms of the FF DCM modulation strategy (a) and detailed view (b). From top to bottom: the boost-inductor currents $i_{L,1}$, $i_{L,2}$, and $i_{L,3}$, and the bus voltage, v_b. Voltage: 300 V/div, current: 100 A/div, and time: 4 ms/div (a) and 4 µs/div (b).

5.3.2. Application to domestic IH

In the previous section, the implementation of the three-phase PFC rectifier has been detailed. The 11-kW prototype generates a low-ripple 750-V bus voltage that is employed in this section for powering an inverter applied to a domestic IH load.

5.3.2.1. Matrix inverter topology

A matrix inverter has been proposed to perform the implementation of the IH application [61]. In Fig. 5.35, the matrix inverter topology is depicted. It is composed of a single vector with a single high-side switching device and 4 low-side switching devices, $S_{l,j}$, $j \in$ (1, 2, 3, and 4). These low-side switches are MOSFETs with parallel diodes, $T_{l,j}$ and $D_{l,j}$, respectively, whereas the high-side switch is a SiC JFET transistor, T_h. They are activated using the control signals, $g_{l,j}$ and g_h, respectively. Additional series diodes, $D_{s,j}$, and parallel diodes, $D_{h,j}$, are placed to block voltage and to allow inverse current in the high-side switch, enabling the overall output power control in each load. This matrix inverter is able to power 4 independent IH loads. Each one of them consists of its equivalent series resistance, $R_{eq,j}$, its equivalent series inductance, $L_{eq,j}$, and a series resonant capacitor, $C_{r,j}$. These loads are connected between the output of the switching devices and the medium point, n, of the split bus capacitor, C_b.

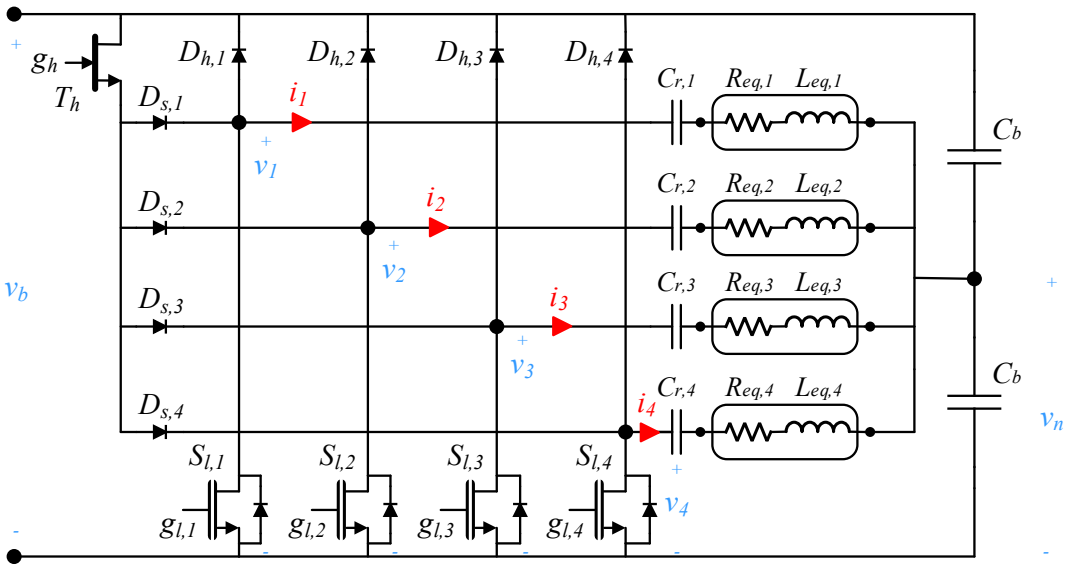


Fig. 5.35 Matrix inverter topology for domestic IH applications. This converter is able to power up to 4 IH loads and control the power accurately at each one of them.

On the one hand, the main advantage of this topology is that a reduced device count is achieved because a single high-side switch is necessary. Therefore, there are less controlled switching devices in comparison with a typical half-bridge inverter. In the last

case, 4 half-bridge branches are necessary to power 4 loads, i.e. 8 switching devices, whereas in the proposed case only 5 power devices are needed. Besides, the count of additional components, such as dc-dc converters or activation drivers, is decreased too.

On the other hand, the main drawback of this topology is that the high-side device manages the current of all the load set and, therefore, its conduction capabilities have to better than in a common implementation. As a result, the use of SiC JFET transistor has been proposed in order to decrease the conduction losses and minimize the temperature influence. Besides, among SiC devices, the JFET transistor allows a lower drain-source on resistance per area ($R_{ds(on)}$/mm^2).

The modulation strategies of the converter are the square wave control along with the pulse density modulation. The square wave control is based on operating at frequency, f_{sw}, and 0.5 fixed duty cycle. In this matrix inverter topology, all the controlled power devices are activated at the same frequency, and the four bottom switches are switched at the same time, without any kind of phase-shift. This is an additional advantage because the intermodulation noise between different half-bridge branches of a typical topology is avoided. The operating frequency is selected according to the IH load features and the required output power, ensuring ZVS conditions in switching devices. The frequency is selected to get the desired power in the most restrictive load. When a load has not to be powered, its low-side transistor remains deactivated. Usually, the most restrictive load is supplied using square wave control, whereas the output power in the remainder loads is controlled using the pulse density modulation strategy.

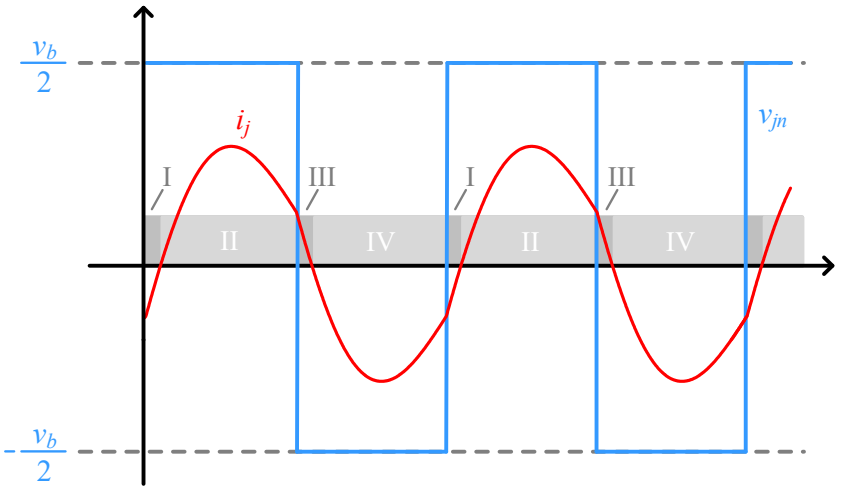


Fig. 5.36 Main waveforms of the j load and activation states of the IH matrix converter. The current waveform, i_j, and the voltage waveform, v_{jn}.

Fig. 5.36 shows the activation states and the main waveforms of the *j* load, voltage, v_{jn}, and current, i_j. The load voltage according the activation state is defined as

$$v_{jn} = \begin{cases} \frac{v_b}{2}, & \text{state: I and II} \\ -\frac{v_b}{2}, & \text{state: III and IV} \end{cases}. \tag{5.9}$$

The bus voltage is divided by the split bus capacitor and, therefore, as it is shown in (5.9), the half of the bus voltage is applied over the IH load and the resonant capacitor according to the activation state of the low-side and high-side switching devices. Close to the resonant frequency, the load behaves as a resistive load and the current is similar to a sinusoidal waveform. In this case, the power delivered to the IH load, $P_{o,j}$, is maximum, and it can be calculated using the first voltage harmonic of a square wave in function of the bus voltage as

$$P_{o,j,max} = \frac{2v_b^2}{\pi^2 R_{eq,j}}. \tag{5.10}$$

Moreover, when pulse density modulation is used, the resultant delivered power at the resonant frequency is proportionally calculated in function of the term, T_{pdm}, and the activation time, t_{on}, as

$$P_{o,j} = \frac{2v_b^2}{\pi^2 R_{eq,j}} \frac{t_{on}}{T_{pdm}}. \tag{5.11}$$

The configuration sequence of the proposed matrix inverter topology is depicted in Fig. 5.37 focusing in the *j* load. At the state I, the high-side parallel diode is activated in order to allow inverse current. When the current direction changes, the state II starts. The JFET is activated getting ZVS switching and the current flows through of this transistor and the series diode. When this device is deactivated, the low-side transistor is activated to allow the current flow, and a negative voltage is applied over the load. This is the state III. Finally, when the load current cross zero again, the direction changes, and the low-side MOSFET is activated, achieving ZVS condition in this power device.

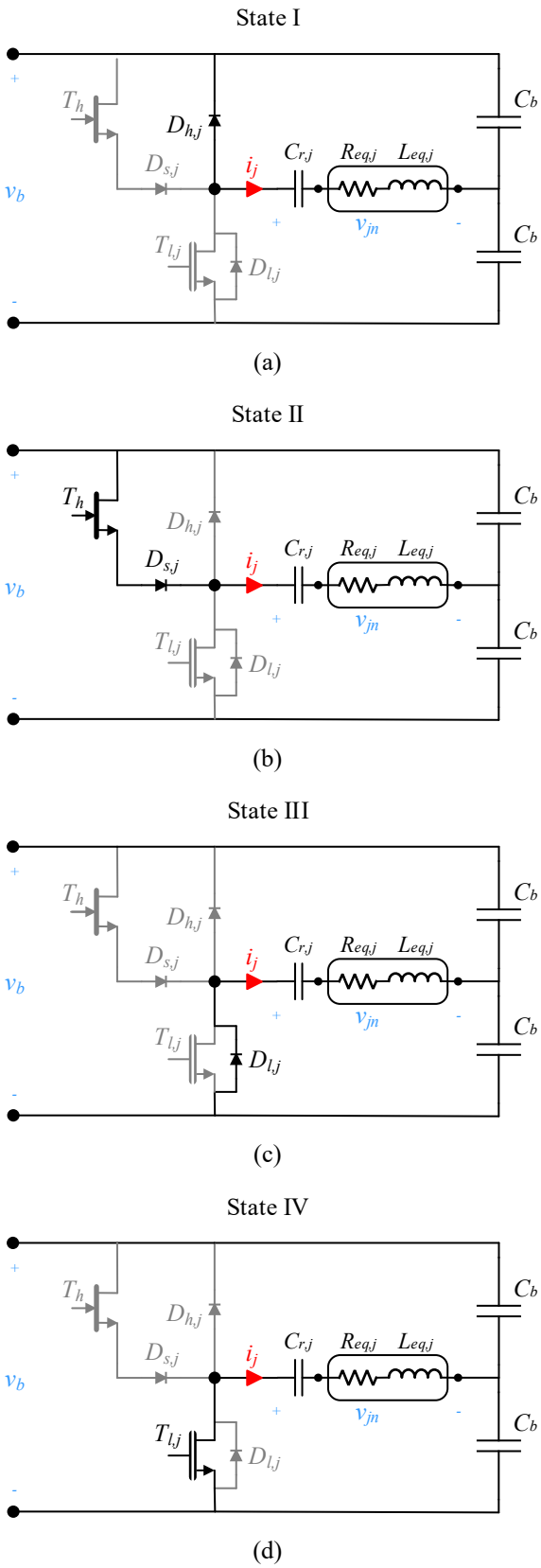


Fig. 5.37 Configuration sequence of the IH matrix converter powering the *j* load. (a) state I, (b) state II, (c) state III, and finally, (d) state IV.

5.3.2.2. Matrix converter implementation

The implementation of a 11-kW, 800-V, and 4-output matrix IH inverter is detailed in this section. TABLE 5.7 summarizes the main features of the converter, and the experimental PCB is shown in Fig. 5.38. The high-side transistor is a SiC JFET which features 1200-V, 50-A, and 20-mΩ GA50SICP12-227, from GeneSiC, and with isolated baseplate SOT-227 package. The series diodes are implemented using four fast recovery diodes in two separates SOT-227 packages. The selected devices are the 1200-V and 52-A DSEI 2x61-12B diodes from IXYS. The low-side switches and high-side diodes are implemented using two EasyPACK modules with 23-mΩ CoolSiC MOSFETs, diodes, and NTC. In particular, the 1200-V and 50-A DF11MR12W1M1_B11 module from Infineon. The power losses of power devices are dissipated using forced-air cooling. Two 450-µF aluminum electrolytic capacitors from Wurth Elektronik have been used as bus capacitor.

Voltage and current measurement systems have been included. The output voltage is measured using voltage dividers whereas the load current is measured using shunts. The selected ADCs are the 1-MSPS and 12-Bit ADCS7476 from Texas Instruments. A Zynq XC7Z020 FPGA from Xilinx is used to implement the control architecture. Besides, the whole system can be managed from the PC through a fiber optical module to provide isolation and a PC application developed using Visual Basic. The implemented drivers are the 1EDI60N12AF from Infineon whereas the dc-dc converters have been custom made because the JFET transistor requires a positive current peak during turn-on, a negative current peak during turn-off, and a continuous gate current during on-state. Small transformers using ferrite cores and the IXDN609 high-speed gate driver have been used to implement these custom-made dc-dc converters. Fig. 5.39 shows the experimental waveforms of the converter operating at maximum power to prove its proper operation.

TABLE 5.7

MATRIX IH CONVERTER DESIGN PARAMETERS

PARAMETER	VALUE
IH loads	4
Bus voltage, v_b	800 V
Maximum load power, $P_{o,j,max}$	3.6 kW
Total output power, P_o	11 kW
Operating frequency, f_{sw}	20-150 kHz

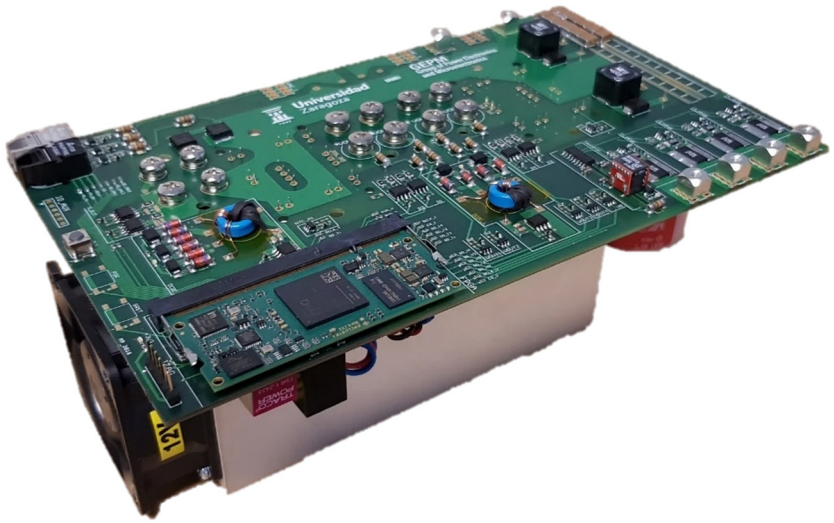


Fig. 5.38 11-kW and 4-output matrix IH converter for domestic IH applications.

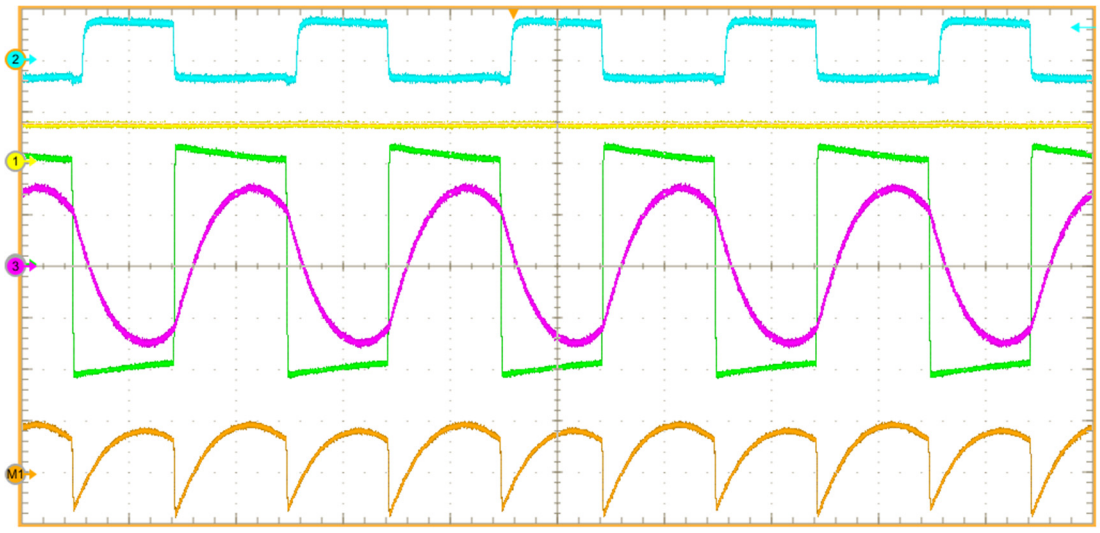


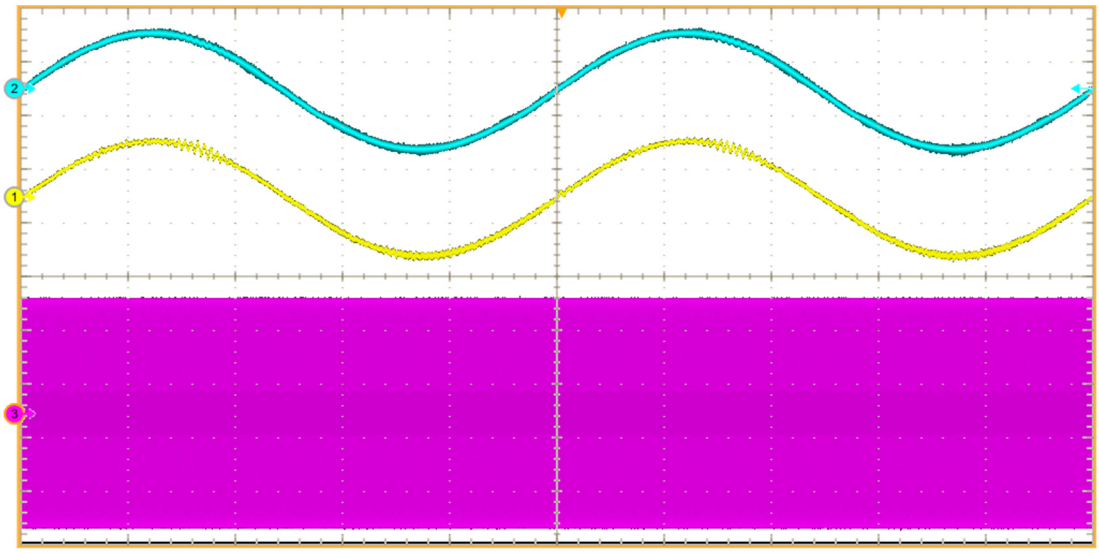
Fig. 5.39 Main waveforms of the matrix IH converter powering a domestic IH load. The converter is operating at maximum power, 11 kW, and 100-kHz frequency. The 4 outputs of the converter are powering the load, which is composed of a 10.5-Ω equivalent series resistance, 57-µH equivalent series inductance, and a 50-nF resonant capacitor. From top to bottom: low-side control signal, g_l, (20 V/div, blue), voltage of the medium point of the split capacitor, v_n, (500 V/div, yellow), load voltage, v_o, (200 V/div, green), load current, i_o, (30 A/div, purple), and output power, p_o (20 kW/div, brown). Time: 5 µs/div.

5.3.2.3. Multi-phase PFC rectifier and matrix converter results

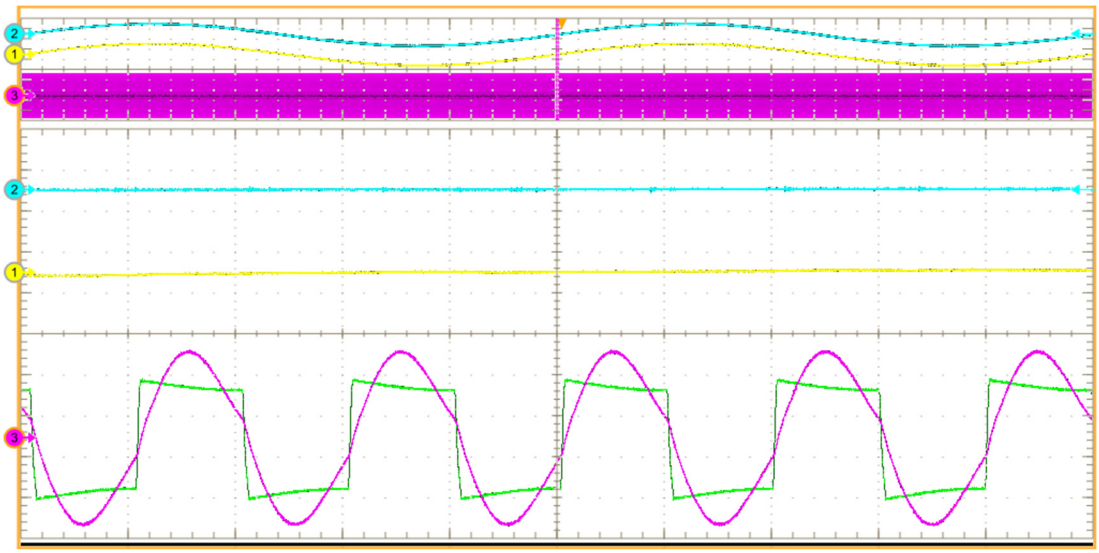
Finally, the three-phase PFC rectifier and the matrix IH converter have been tested together to power a domestic IH load. The HS FF CCM modulation strategy of the three-phase PFC rectifier has been selected due to its best efficiency with fixed frequency, as it is discussed later in the comparative analysis of Chapter 6. The PFC converter powers the matrix IH inverter using the 750-V dc bus. The operating frequencies have been established in 50 kHz for the PFC rectifier and 63 kHz for the IH inverter. The IH load is shown in Fig. 5.40, and it is composed of a 10.5-Ω equivalent series resistance and a 57-µH equivalent series inductance.

Fig. 5.41 depicts the main input and output waveforms of the set operating at maximum power, i.e.11 kW. The three mains phases are activated delivering a 15.8-A rms current each one, and the current in the IH load is 32 A rms. A 123-nF series resonant capacitor has been placed to obtain the maximum desired power at the selected operating frequency. The return path of the load is connected to the middle point of the split bus capacitor. The resonant frequency is close to the operating frequency and, for this reason, the waveform of the IH load current is sinusoidal. More in detail, the operating frequency is slightly higher to get an inductive load and achieve ZVS switching in the IH inverter. The experimental measurements prove the feasibility and proper operation of the set composed of the three-phase PFC rectifier and the matrix IH converter.

Fig. 5.40 Inductor-load system composed of two series 21-cm inductors and two zenith pots. Its equivalent series resistance is 10.5 Ω whereas its equivalent series inductance is 57 µH.

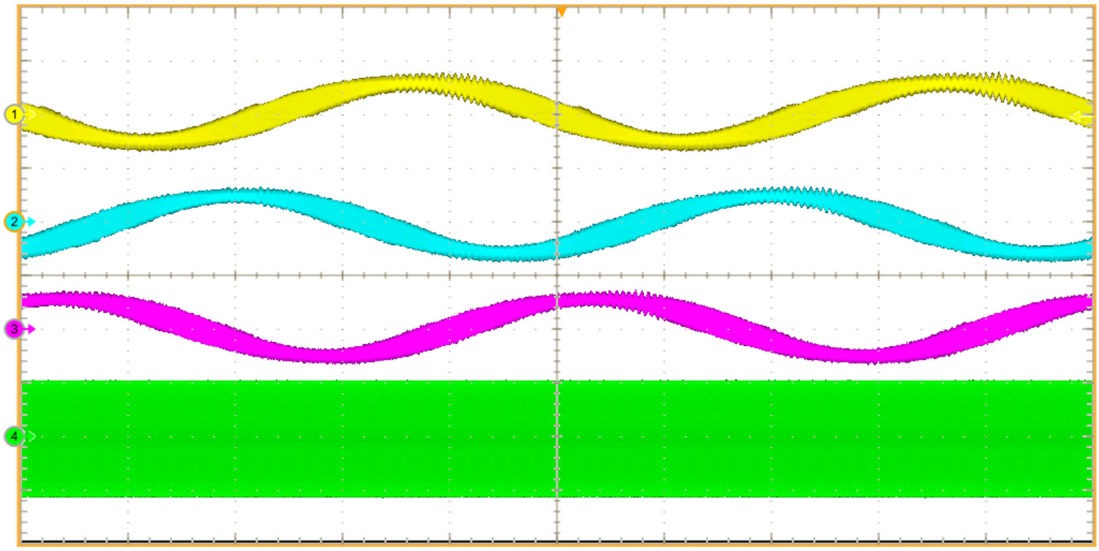


(a)

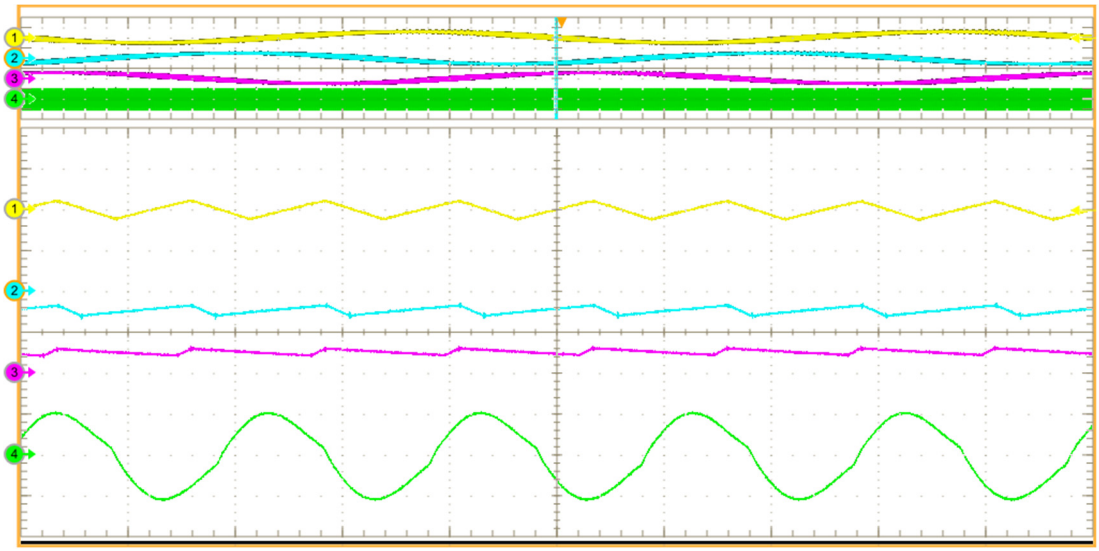


(b)

Fig. 5.41 Experimental waveforms at the input of the PFC rectifier and at the output of the IH inverter powering a 11-kW IH load. Voltage: 300 V/div. Current: 30 A/div. Time: 4 ms/div (a) and 8 μs/div (b). From top to bottom: mains phase voltage, v_I, (blue), mains phase current, i_I, (yellow), IH-load voltage, v_o, (green), and IH-load current, i_o, (purple).



(a)



(b)

Fig. 5.42 Experimental current waveforms of the boost inductors of the PFC rectifier and the output of the IH inverter powering a 11-kW IH load. Current: 40 A/div. Time: 4 ms/div (a) and 8 μs/div (b). From top to bottom: boost-inductor currents $i_{L,1}$, $i_{L,2}$, and $i_{L,3}$, and IH-load current, i_o.

Chapter 6

Result Analysis and Discussion

The measurements and results obtained using the implemented prototypes are analyzed and compared in this Chapter in order to discuss the main advantages and drawbacks of each implemented modulation strategy. Besides, comparative evaluations using normalized performance rates are provided to better highlight the strong points of each strategy.

Contents

6. Result Analysis and Discussion

In previous chapters, the use of PFC rectifiers has been proposed to improve the performance of domestic IH applications. In order to address this proposal and to analyze their implementation and main advantages and disadvantages, two PFC rectifier topologies for single-phase and multi-phase cases have been introduced. Different modulation strategies along with their control strategies have been proposed to accomplish the control of these topologies. The feasibility and proper operation of the topologies, modulation strategies, and controls have been experimentally proved in the last chapter by means of the experimental implementation of a controllable power supply to power every system, a single-phase PFC rectifier with an IH inverter, a three-phase PFC rectifier, and a matrix IH inverter. Finally, in this chapter, the obtained experimental results are going to be analyzed and compared in order to highlight the main advantages and drawbacks of each implemented modulation strategy.

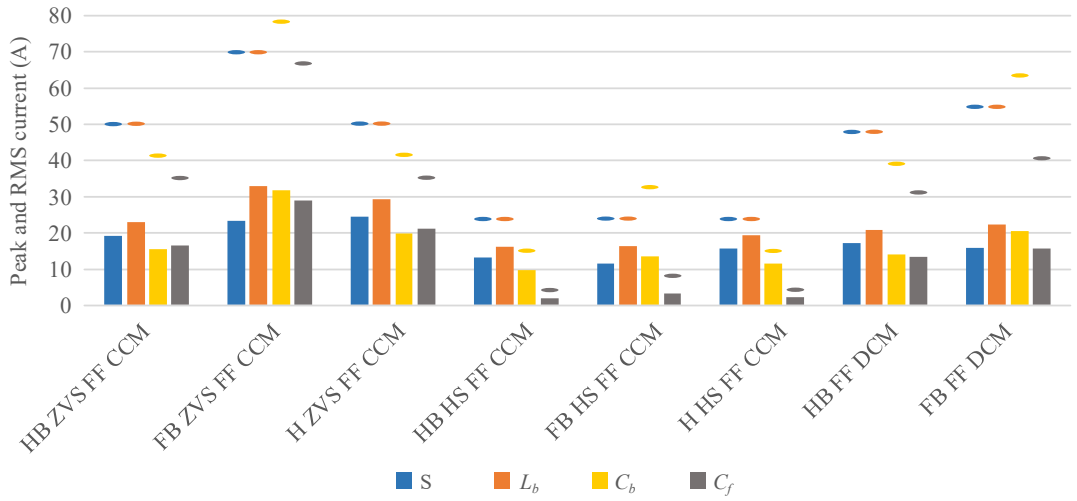
6.1. Single-phase PFC rectifier

This section provides a result analysis and a comparative discussion of the proposed single-phase modulation strategies using the implemented single-phase PFC rectifier. The advantages and disadvantages have been analyzed taking into account several parameters: device stress, efficiency, power loss distribution, operating frequency, and switching current. This discussion allows finding the modulation strategy better suited according to the implementation requirements and the application area.

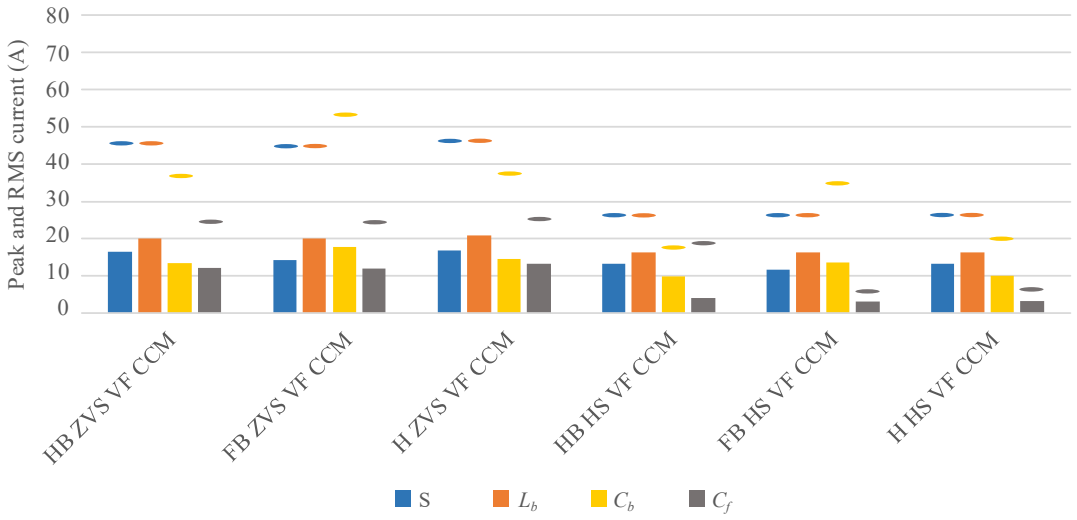
6.1.1. Result analysis

6.1.1.1. Device stress

The required current ratings of the converter components depend on the implemented modulation strategy. The bar chart of Fig. 6.1 depicts the peak current, I_p, and the rms current, I_{rms}, of the switching devices, S, the boost inductor, L_b, the bus capacitor, C_b, and the filter capacitor, C_f, at maximum power, 3680 W, for each analyzed modulation strategy.



(a)



(b)

Fig. 6.1 Current ratings: peak current, I_p, (top disks) and rms current, I_{rms}, (bars) of the switching devices, S, boost inductor, L_b, bus capacitor, C_b, and filter capacitor, C_f, of the single-phase PFC rectifier at maximum power, 3680 W, for each modulation strategy. (a) FF modulation strategies and (b) VF modulation strategies.

The maximum voltage applied to the switching devices just depends on the bus voltage, v_b, i.e. 400 V. The output average current, about 4.5 A, just depends on the output power and the bus voltage, and, therefore, it is independent of the modulation strategy. Taking into account the average current in both branches, 9 A, and the bus voltage, 400 V, an output power of 3680 W is obtained. The worst cases for the rms and peak currents are found in the ZVS CCM and DCM strategies due to the high current ripple. With 75-A peak current and 23-A rms current, the full-bridge fixed frequency strategy stands out

among them. The HS CCM strategies are the best cases. Besides, with 11.5-A rms current and 25-A peak current, the full-bridge fixed frequency strategy gets the lowest ratings. Finally, another aspect to consider is that, when using the full-bridge configuration, the rms current is evenly distributed in each switching device, whereas, when using the half bridge configuration it is not. In this configuration, the worst case has been taken into account.

The maximum voltage applied to the boost inductor depends on the selected topology. When using the half-bridge configuration this voltage is v_b, i.e. 400 V, whereas using the full-bridge configuration is $v_b + v_{ac}$, i.e. 725 V, or using the hybrid configuration is $v_b + v_{th}$, i.e. 500 V. Therefore, the insulation requirements of the boost inductor are lower using half-bridge configuration. The input current is 16 A, and it just depends on the input power, 3680 W. The peak currents are the same that in the switching devices whereas the rms currents are higher. The full-bridge ZVS fixed frequency is the worst case with 75-A peak current and 33-A rms current. The half-bridge hard switching fixed frequency is the best case with 25-A peak current and 16.1-A rms current.

The maximum voltage applied to the bus capacitor is the bus voltage, v_b, i.e. 400 V. The modulation strategies that get the worst and the best current rating are the same as before with 83-A peak current and 31.7-A rms current, and 16-A peak current and 9.7-A rms current, respectively.

Finally, the maximum voltage applied to the filter inductor and capacitor is the mains voltage, i.e. 325 V. The current ratings of the filter coil are the mains current ratings, i.e. 23-A peak current and 16-A rms current, whereas the current ratings of the filter capacitor are given by the bar chart of Fig. 6.1 for each modulation strategy.

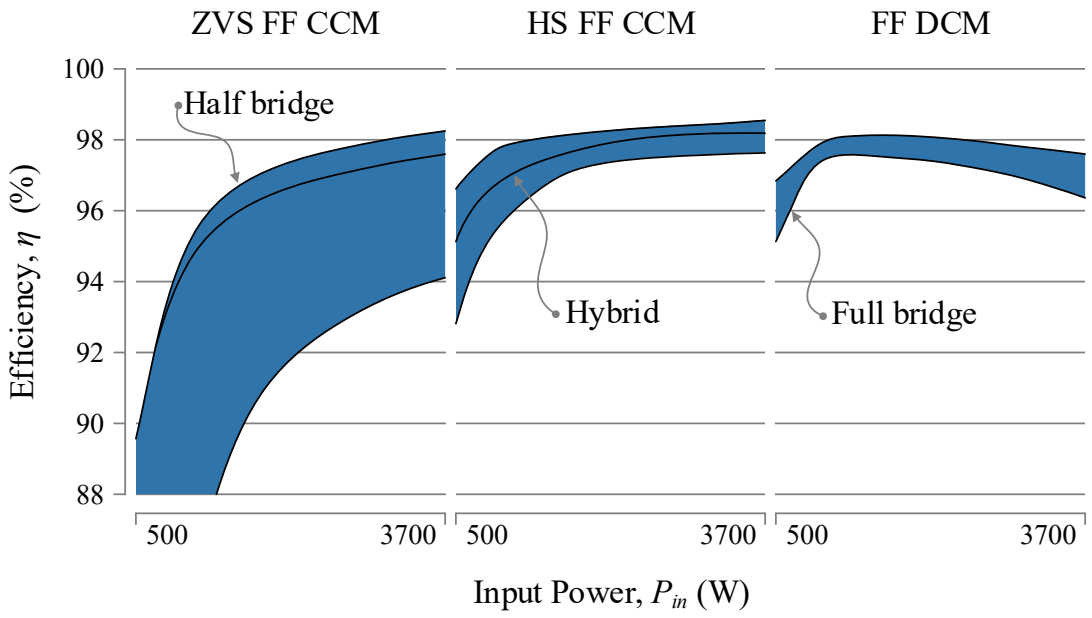
The filter and boost inductors have been designed taking into account the aforementioned current and voltage ratings. Moreover, the CCS050M12CM2 module with 1200-V and 25-mΩ SiC MOSFETs have been selected to fulfill these current and voltage requirements.

6.1.1.2. Efficiency and power loss distribution

The efficiency of the single-phase PFC rectifier, η, is calculated as

$$\eta = \frac{P_{out}}{P_{in}}, \tag{6.1}$$

being P_{out} the output power of the rectifier and P_{in} the input power. The experimental efficiency is measured by using a power analyzer, and the results as a function of the input power are shown in Fig. 6.2.



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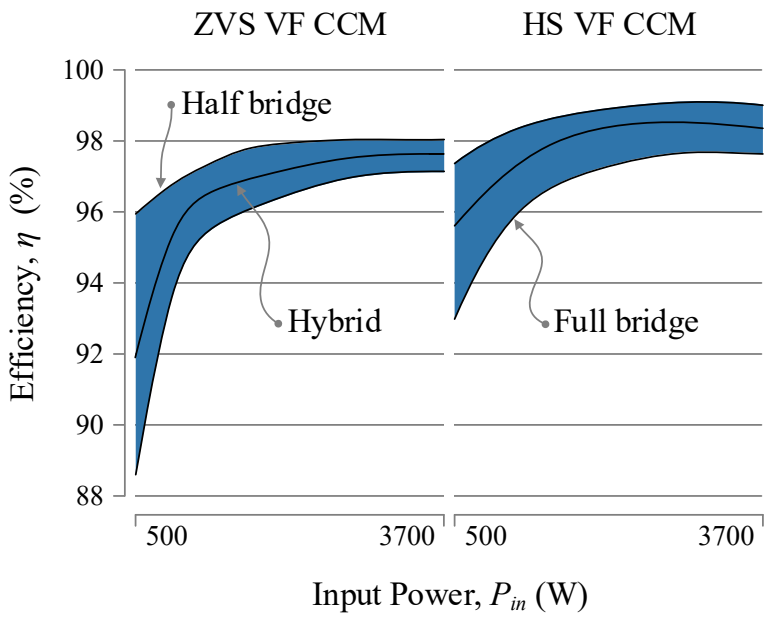


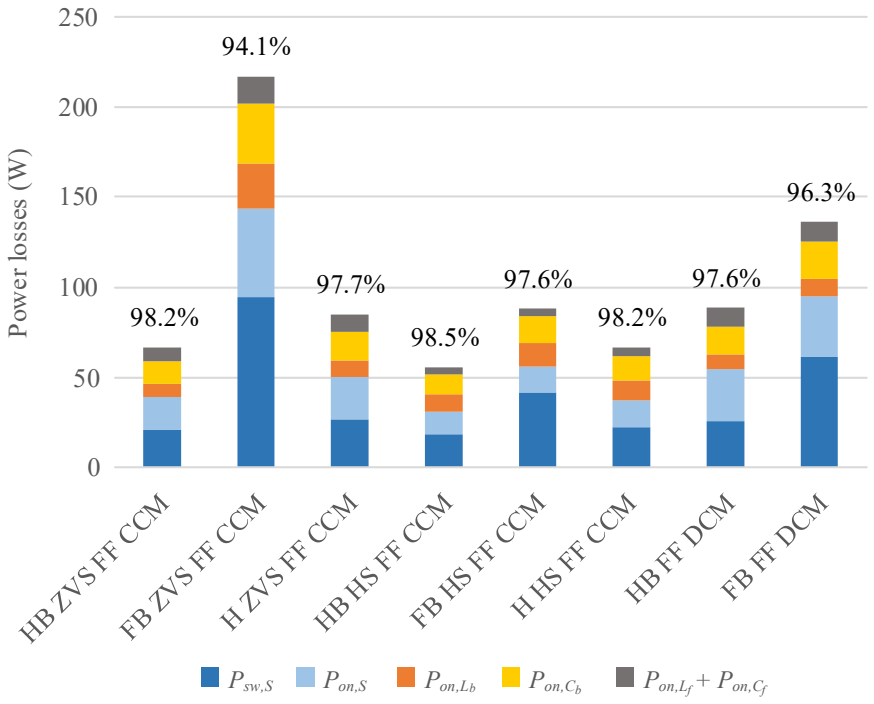
(b)

Fig. 6.2 Global efficiency, η, of the single-phase PFC rectifier as a function of the input power for each modulation strategy. The upper border reflects the case using the half-bridge configuration and the lower border is using the full-bridge configuration. Between the upper and the lower border, the hybrid configuration is included as a function of the threshold voltage. In black line, the hybrid ZVS and hard switching variable frequency CCM modulation strategy for a 100-V threshold voltage. (a) FF modulation strategies and (b) VF modulation strategies.

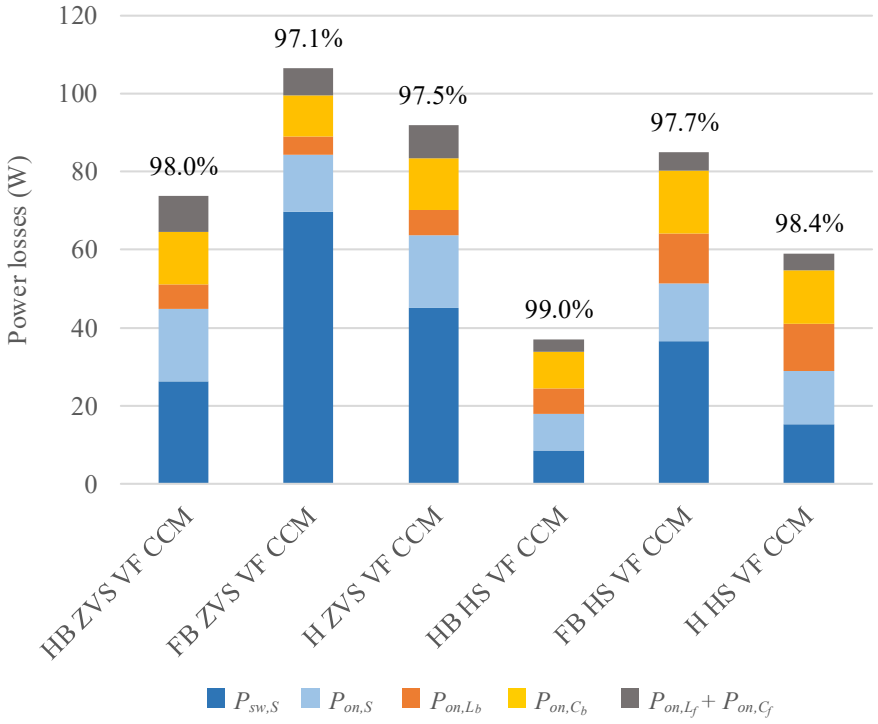
Using the half-bridge hard-switching variable-frequency CCM, the efficiency reaches up to 99% around the maximum power, i.e. 3680 W, outperforming the rest of modulation strategies in the whole operating range. However, the full-bridge ZVS fixed-frequency CCM gets the worst efficiency, reaching just up to 94% at maximum power. This is due to the high ripple of the current in the zero crossing to operate at the same frequency. Besides, a similar ripple is necessary to work at the same frequency at lower powers. Since the conduction and switching losses are similar, the efficiency is further penalized at low power. An option to improve this result consists in changing the operating frequency as a function of the power in order to get ZVS with a reduced current ripple. This approach is interesting when using an inductive IH load. In this case, the PFC stage and the IH inverter are synchronized at the same frequency. The output power is controlled by modifying the operating frequency. When the frequency is increased, the current ripple in the PFC stage is lower, decreasing switching and conduction losses.

The efficiency of the implemented hybrid strategies is shown with black lines in graphs of Fig. 6.2 using a 100-V threshold voltage, v_{th}. This parameter is similar to the efficiency of half-bridge configurations at maximum power, besides the zero-cross distortion using half-bridge configuration is avoided. In particular, the efficiency of the ZVS FF CCM improves a 3% at maximum power in comparison with the full-bridge configuration. As previously discussed, the hybrid configuration is not necessary in the FF DCM modulation strategy because there is not distortion of the mains current in half-bridge configuration.

Fig. 6.3 shows the power loss distribution and efficiency at maximum power. As previously commented, in these power loss distribution, the switching losses of switching devices, $P_{sw,S}$, the conduction losses of switching devices, $P_{on,S}$, the boost-inductor losses, P_{on,L_b}, the bus capacitor losses, P_{on,C_b}, and the filter losses, $P_{on,L_f} + P_{on,C_f}$, have been taken into account. Using the ZVS CCM and DCM modulation strategies the ripple current is higher. It can be seen that this also increases to the conduction losses of the converter components. Moreover, with the full-bridge configuration, the switching losses are higher due to the fact that both the switching current and the number of switching devices are increased, as it is later discussed.



(a)



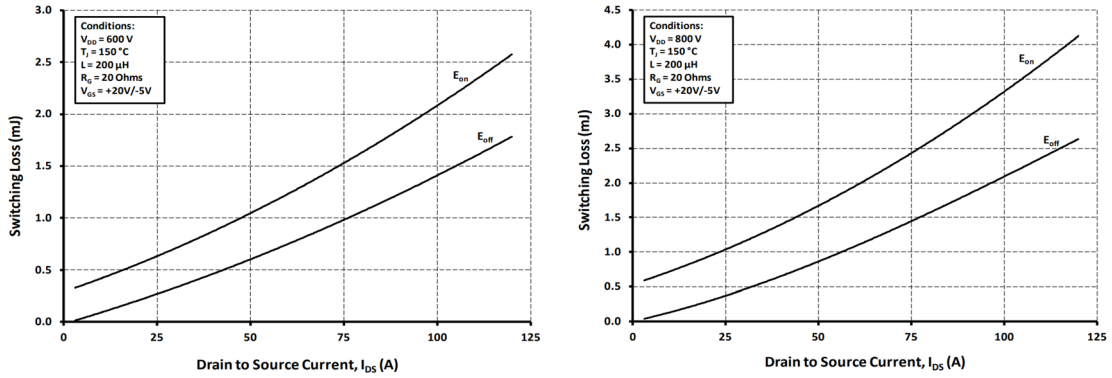
(b)

Fig. 6.3 Power loss distribution and experimental global efficiency at maximum power, 3680 W, for each modulation strategy. (a) FF modulation strategies and (b) VF modulation strategies.

In order to estimate the power losses of these main devices, the power-loss models detailed below have been used. The switching losses of a device, P_{sw}, have been calculated using the turn-off switching energy, E_{off}, and the turn-on switching energy, E_{on}. These energies depend non-linearly on the voltage and current in each switching cycle, k. Therefore, the charts provided by the datasheet (Fig. 6.4) and the equation,

$$P_{sw} = \frac{1}{T_{ac}}\left[\sum_{k=1}^{k_{max}}\left(E_{off,k}\left(v_b, i_{off}\right) + E_{on,k}\left(v_b, i_{on}\right)\right)\right], \tag{6.2}$$

have been used to calculate its. The bus voltage, v_b, is the drain-to-source voltage, V_{DS}, i_{off} and i_{on} are the drain-to-source current, I_{DS}, at the moment of the turn-off and turn-on transition, respectively, and k_{max} is the maximum number of switching cycles in a mains cycle, T_{ac}.



(a) (b)

Fig. 6.4 Turn-off switching energy, E_{off}, and turn-on switching energy, E_{on}, in function of the drain-to-source current, I_{DS}, for (a) 600 V and (b) 800 V drain-to-source voltage, V_{DS}, of the CCS050M12CM2 module. Source: manufacturer datasheet.

The conduction losses of a switching device, P_{on}, have been calculated using the MOSFET on-state resistance, R_{DS}, and the drain-to-source rms current, $I_{S,rms}$, as

$$P_{on} = R_{DS} I_{S,rms}^2. \tag{6.3}$$

The conduction losses of the boost inductor, P_{on,L_b}, have been estimated using the mains rms current, $I_{ac,rms}$, the boost-inductor rms current, $I_{b,rms}$, the low-frequency resistance, $R_{L_b,LF}$, which is associated to the mains frequency, and the high-frequency resistance, $R_{L_b,HF}$, which is associated to the operating frequency, as

$$P_{on,L_b} = R_{L_b,LF} I_{ac,rms}^2 + R_{L_b,HF}\left(I_{b,rms}^2 - I_{ac,rms}^2\right). \tag{6.4}$$

The conduction losses of the filter inductor, P_{on,L_f}, are calculated using the its low-frequency resistance, $R_{L_f,LF}$, and the mains rms current as

$$P_{on,L_f} = R_{L_f,LF} I_{ac,rms}^2. \tag{6.5}$$

Finally, the conduction losses of the filter capacitor, P_{on,C_f}, and the bus capacitor, P_{on,C_b}, are estimated using their high-frequency resistances and their rms currents.

$$P_{on,C_f} = R_{C_f,HF} I_{C_f,rms}^2. \tag{6.6}$$

$$P_{on,C_b} = R_{C_b,HF} I_{C_b,rms}^2. \tag{6.7}$$

6.1.1.3. Switching current and operating frequency

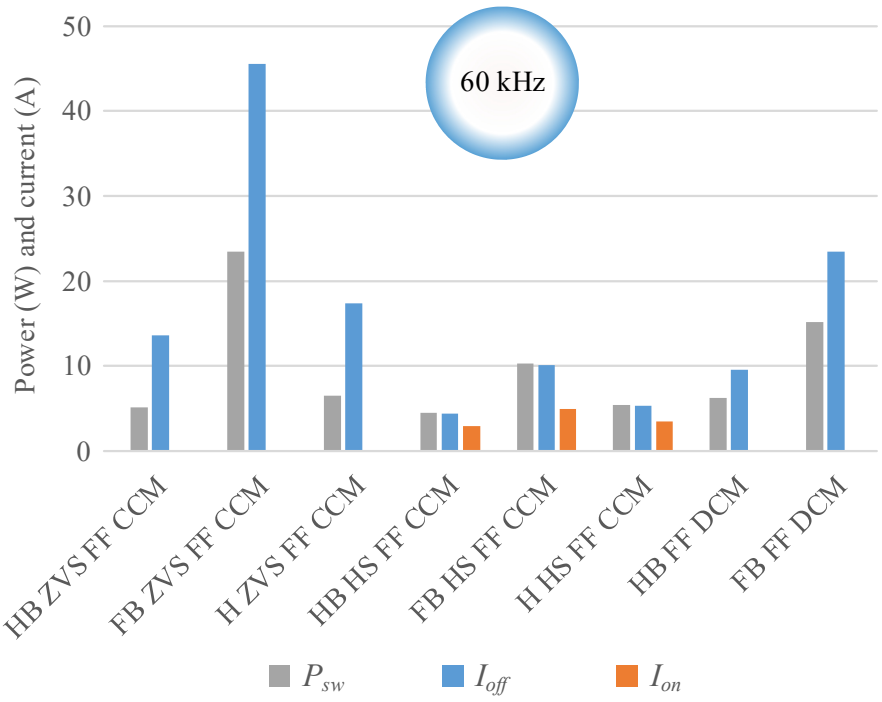
In a simplified form, the turn-on and turn-off switching losses can be also calculated using the turn-off and turn-on average current, I_{off} and I_{on}, the operating frequency, f_{sw}, and the switching energy of the MOSFETs as

$$P_{sw} = f_{sw}\left(E_{off}\left(v_b, I_{off}\right) + E_{on}\left(v_b, I_{on}\right)\right), \tag{6.8}$$

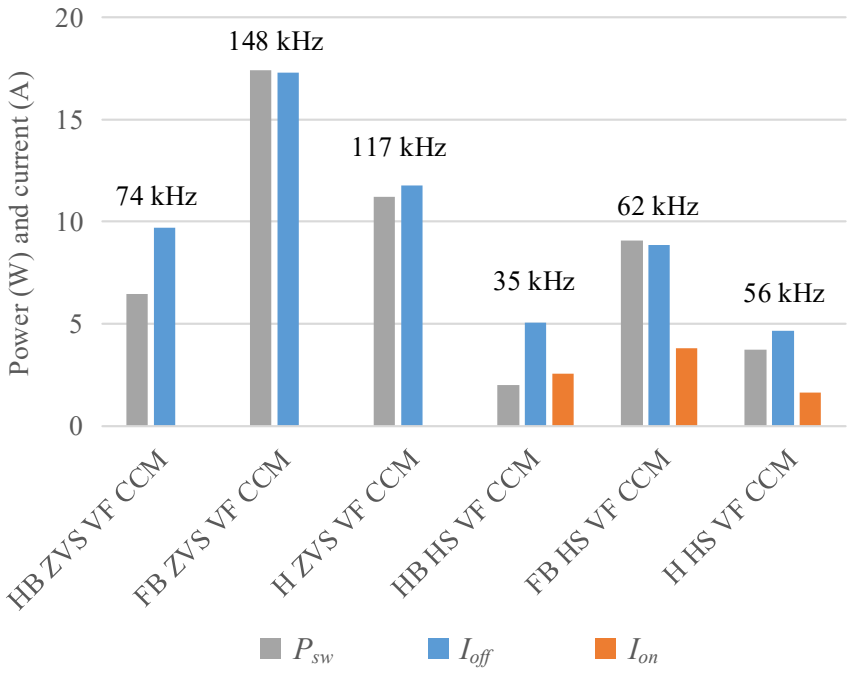
Therefore, it can be deduced from this equation that the switching losses are proportional to the average current and frequency. Fig. 6.5 shows the turn-off and turn-on average currents, and the switching losses calculated with (6.2) for each modulation strategy. As a consequence of the soft-switching behavior, there are not turn-on switching losses in ZVS CCM and DCM strategies and, therefore, the turn-on average current has not been taken into account. Usually, the turn-on switching energy of the MOSFETs is higher than the turn-off one. However, in hard-switching modulation strategies, the turn-off current is lower than in ZVS modulation strategies. Besides, the turn-on current is also lower. For these reasons, the switching losses are usually higher in ZVS CCM and DCM modulation strategies.

Regarding the operating frequency range, on the one hand, there are application areas in which getting a fixed operating frequency along the mains cycle is important. For example, in domestic IH converters, modulating with different inverters at different working frequencies can lead to acoustic noise. In these cases, working with fixed frequency modulation strategies is essential to get a proper operation. Besides, it also allows a better optimization of the filter design. On the other hand, working with variable

frequency modulations allows distributing the harmonic currents in a wide frequency range, decreasing the EMC issues.



(a)



(b)

Fig. 6.5 Switching power losses, P_{sw}, and turn-off and turn-on average current, I_{off} and I_{on}, at maximum power, 3680 W for each modulation strategy. The operating frequency is shown above each bar (average frequency considered for variable frequency strategies). (a) FF modulation strategies and (b) VF modulation strategies.

6.1.1.4. *THD and PF*

Fig. 6.6 depicts the total harmonic distortion of the input current, THD_i, whereas Fig. 6.7 shows the power factor, *PF*, of the implemented modulation strategies. The THD_i is less than 4%, getting a sinusoidal current waveform. The THD_i of DCM modulation strategies reaches up to the 6.8% because the current waveform is distorted. This distortion is generated because the boost-inductor resistance and the diode reverse current have not been taken into account in the fixed-frequency control strategy. This issue can be solved using an outer control loop. In the half-bridge configurations cases, the greater part of the mains current distortion is due to the zero-crossing distortion whereas, in VF modulation strategies, part of this THD_i is because of the high variability of the switching frequency or, as it is known, the frequency sweep.

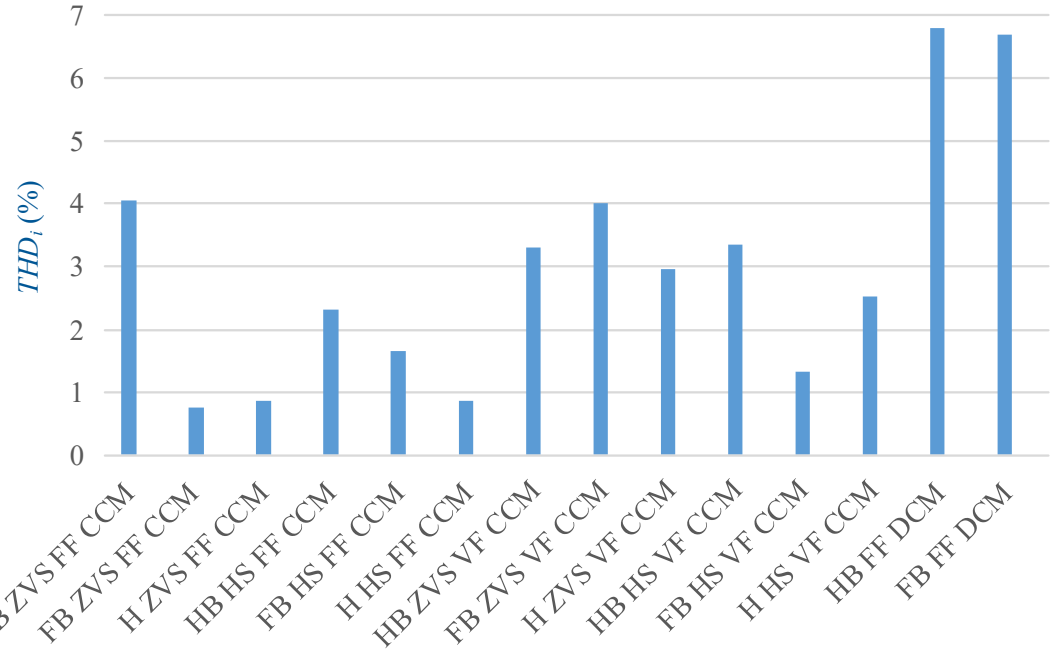


Fig. 6.6 Total harmonic distortion of the mains current, THD_i, of the single-phase PFC rectifier at maximum power, 3680 W, for each modulation strategy.

Moreover, it can be appreciated that all strategies reach a *PF* greater than 0.99. The worst case is the HS VF CCM strategy using half-bridge configuration. This is due to a small phase-shift of the mains current with respect to the mains voltage, and the zero-crossing distortion. In the ZVS VF CCM case, the main contribution to the lower power factor is the frequency sweep in addition to the zero-crossing distortion. Finally, in DCM cases, it is due to the mains current waveform is not entirely sinusoidal due to the simplifications in the control strategy, as commented above.

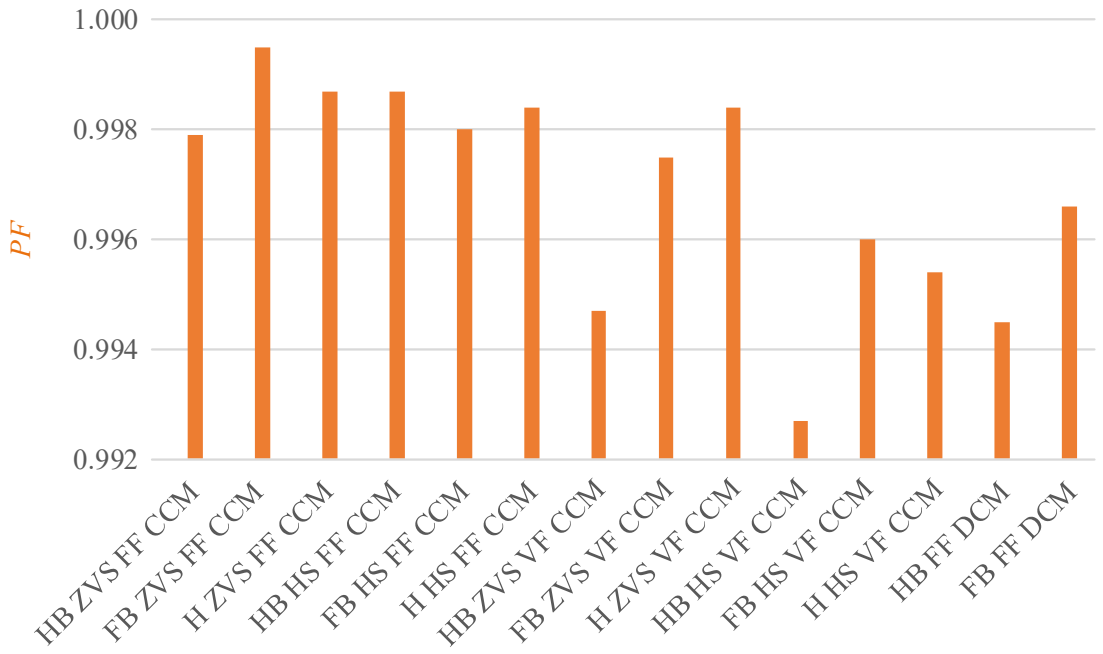


Fig. 6.7 Power factor, *PF*, of the single-phase PFC rectifier at maximum power, 3680 W, for each modulation strategy.

6.1.2. Comparative analysis of the modulation strategies

Finally, a comparative evaluation of the studied modulation strategies at maximum power with regard to several key figures of merit, such as rms current, switching current, or frequency, is provided to highlight the advantages and disadvantages of each strategy, and to facilitate the selection of an optimum modulation strategy for a specific application.

6.1.2.1. Normalized performance rates

Normalized performance rates independent of the developed system have been defined in order to provide a general quantification of the modulation strategies performance. Consequently, the rms mains current, $I_{ac,rms}$, has been used as reference value.

- Relative overall rms current

The relative overall transistor rms current is calculated as

$$\tau_{T,rms} = \frac{I_{T_{h,a},rms} + I_{T_{l,a},rms} + I_{T_{h,b},rms} + I_{T_{l,b},rms}}{I_{ac,rms}}, \tag{6.9}$$

where $I_{T_{h,a},rms}$, $I_{T_{l,a},rms}$, $I_{T_{h,b},rms}$, and $I_{T_{l,b},rms}$ correspond to the rms currents of the high-side and low-side transistors of *a* and *b* branches, respectively. This parameter allows comparing the overall transistor conduction losses, which are usually calculated using the on-state resistance and the square of the transistor rms current. It should be noted that MOSFETs are activated when the antiparallel diodes are conducting to reduce on-state losses.

The relative overall inductor rms current is calculated as

$$\tau_{L,rms} = \frac{I_{L_b,rms}}{I_{ac,rms}}, \tag{6.10}$$

where $I_{L_b,rms}$ is the boost-inductor rms current. As in the previous case, this rate is related to the conduction losses in the boost inductor.

- Relative maximum current

This parameter reflects the maximum current value in the boost inductor and the switching devices, and it is critical when the switching devices are selected and the boost inductor is designed, mainly due to the saturation current. This value is the same in both components and, therefore, it can be calculated as

$$\tau_{max} = \frac{I_{L_b,p}}{I_{ac,rms}}, \tag{6.11}$$

where $I_{L_b,p}$ is the peak current of the boost inductor.

- Relative switching current

The relative turn-off current is calculated as

$$\tau_{c,off} = \frac{I_{T_{h,a},off} + I_{T_{l,a},off} + I_{T_{h,b},off} + I_{T_{l,b},off}}{I_{ac,rms}}, \tag{6.12}$$

whereas the relative turn-on current is obtained as

$$\tau_{c,on} = \frac{I_{T_{h,a},on} + I_{T_{l,a},on} + I_{T_{h,b},on} + I_{T_{l,b},on}}{I_{ac,rms}}. \tag{6.13}$$

$I_{T_{h,a},off}$, $I_{T_{l,a},off}$, $I_{T_{h,b},off}$, and $I_{T_{l,b},off}$ are the turn-off average currents of the high-side and low-side transistors of a and b branches, respectively. $I_{T_{h,a},on}$, $I_{T_{l,a},on}$, $I_{T_{h,b},on}$, and $I_{T_{l,b},on}$ refer to the turn-on currents. These parameters allow comparing the switching loss energy of switching devices.

- Relative switching frequency

The $f_{sw,avg}$ rate refers to the mean switching frequency normalized to the nominal design frequency of the single-phase PFC rectifier, $f_{sw,PFC}$, i.e. 60 kHz. This rate, along with the relative turn-off and the turn-on currents, provide information with regard to the switching power losses of the transistors, which are calculated using the switching frequency and the switching energy.

The relative frequency sweep is calculated as

$$\delta_f = \frac{f_{sw,max} - f_{sw,min}}{f_{sw,PFC} f_{sw,avg}}, \tag{6.14}$$

where $f_{sw,max}$ and $f_{sw,min}$ refer to the maximum and the minimum switching frequencies of the power devices. This parameter indicates how much the operating frequency changes, and it is null in FF modulation strategies.

- Relative losses

Finally, the efficiency of the system is characterized by the relative losses as 1-η, being η the efficiency obtained using expression (6.1). Therefore, it can be expressed as

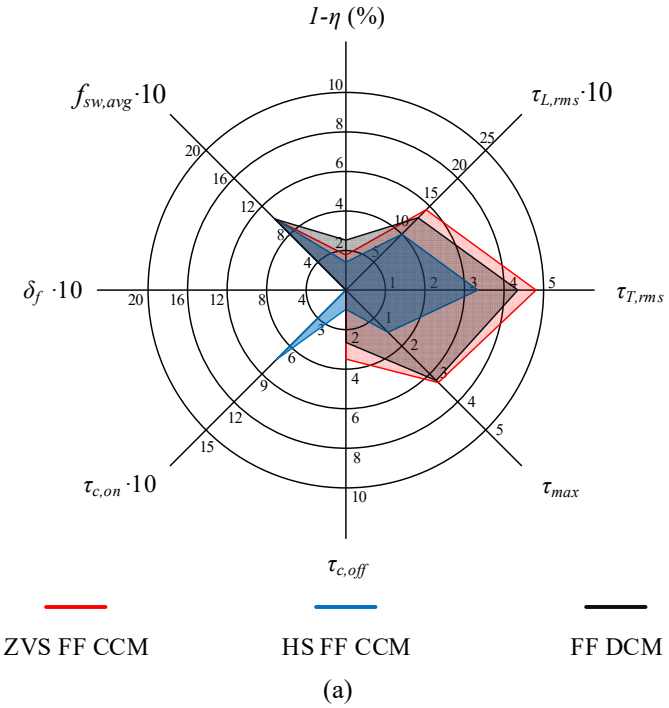
$$1-\eta = 1-\frac{P_{out}}{P_{in}}. \tag{6.15}$$

6.1.2.2. Radial graphs

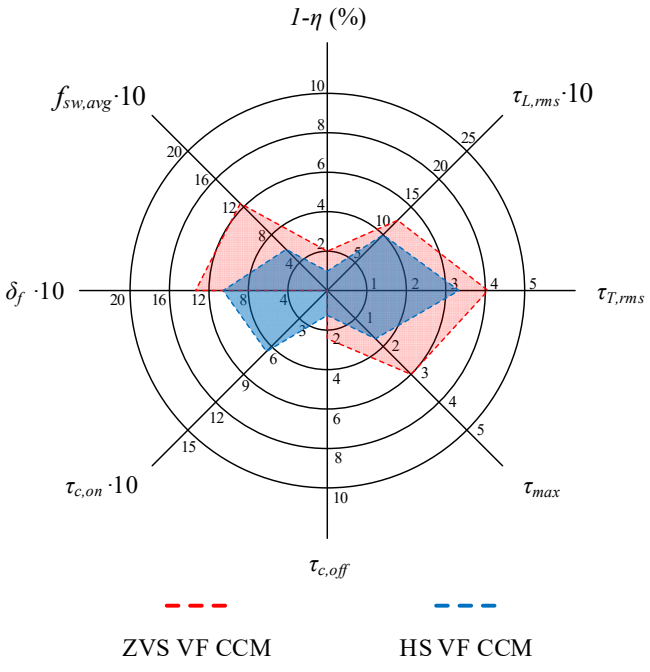
The aforementioned normalized performance rates of the different modulation strategies are compared using radial graphs. As a result, the modulation strategies that present a smaller area in the radial graph are the best performance ones with regard to the analyzed parameters: efficiency, operating frequency, switching current, maximum current, and rms current.

Fig. 6.8, Fig. 6.9, and Fig. 6.10 depict these comparative radial graphs at maximum power for the half-bridge, full-bridge, and hybrid configurations of the single-phase PFC

rectifier, respectively. Besides, they are split in FF and VF strategies. It can be appreciated that HS modulations get better performance than ZVS or DCM ones. This is due to the high current ripple, which leads to increased rms current in power devices, inductors, and capacitors; and higher turn-off currents, increasing both conduction and switching losses.



(a)



(b)

Fig. 6.8 Comparative evaluation at maximum power of (a) FF and (b) VF modulation strategies using half-bridge configuration. The employed rates are as follows: the relative losses, 1-η, the relative overall rms current of the inductance, $\tau_{L,rms}$, and the transistor, $\tau_{T,rms}$, the relative maximum current, τ_{max}, the relative turn-off current, $\tau_{c,off}$, the relative turn-on current, $\tau_{c,on}$, the relative frequency sweep, δ_{sw}, and the relative mean switching frequency, $f_{sw,avg}$.

Furthermore, the full-bridge configuration gets worse results because the voltage applied to the boost inductor is higher, increasing the current ripple and mean switching frequency in VF strategies. Hybrid configuration allows avoiding the zero crossing distortion and keeping similar performance to the half-bridge configurations.

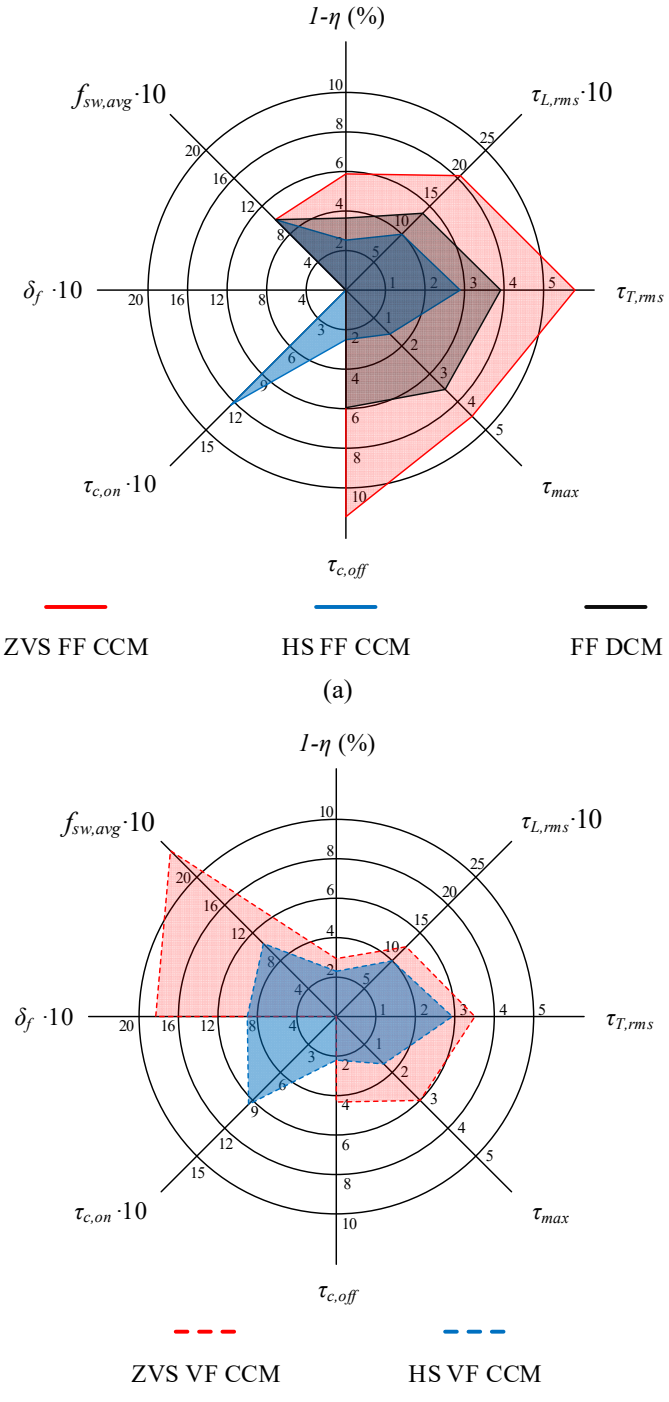
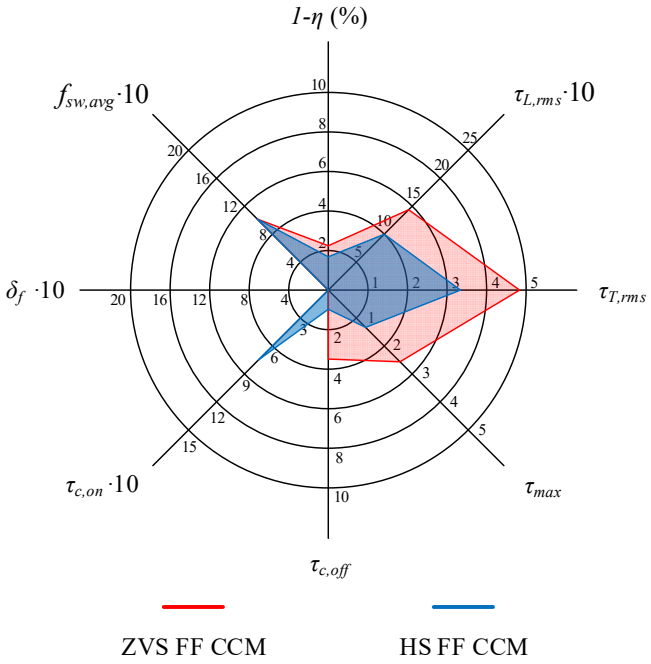
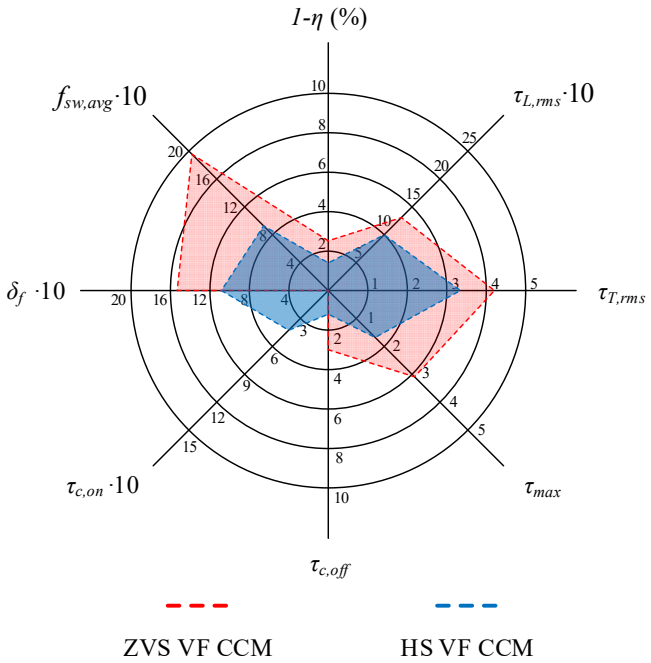


Fig. 6.9 Comparative evaluation at maximum power of (a) FF and (b) VF modulation strategies using full-bridge configuration. The employed rates are as follows: the relative losses, 1-η, the relative overall rms current of the inductance, $\tau_{L,rms}$, and the transistor, $\tau_{T,rms}$, the relative maximum current, τ_{max}, the relative turn-off current, $\tau_{c,off}$, the relative turn-on current, $\tau_{c,on}$, the relative frequency sweep, δ_{sw}, and the relative mean switching frequency, $f_{sw,avg}$.

According to this comparative analysis, the HS FF CCM modulation strategy gets a good trade-off between efficiency, device stress, implementation and control cost, and EMC. Besides, it avoids the zero-cross distortion in full-bridge or hybrid configuration, and the acoustic noise, since it works at a fixed frequency.



(a)



(b)

Fig. 6.10 Comparative evaluation at maximum power of (a) FF and (b) VF modulation strategies using hybrid configuration. The employed rates are as follows: the relative losses, 1-η, the relative overall rms current of the inductance, $\tau_{L,rms}$, and the transistor, $\tau_{T,rms}$, the relative maximum current, τ_{max}, the relative turn-off current, $\tau_{c,off}$, the relative turn-on current, $\tau_{c,on}$, the relative frequency sweep, δ_{sw}, and the relative mean switching frequency, $f_{sw,avg}$.

6.2. Multi-phase PFC rectifier

In the previous section, a comparative analysis of the proposed single-phase modulation strategies using the implemented single-phase PFC rectifier has been provided. The main advantages and disadvantages have been discussed with regards to several parameters, such as device stress, efficiency, power loss distribution, operating frequency, switching current, and EMC performance. Several normalized performance rates have been used to implement radial graphs in order to perform a comparison of the modulation strategies independent of the developed hardware. In this section, the same result analysis and comparison are provided for the multi-phase PFC rectifier. As the modulation strategies are the same, the results obtained in this case have similar justifications as the full-bridge configuration of the single-phase implementation.

6.2.1. Result analysis

6.2.1.1. Device stress

As in the single-phase case, the current ratings of the converter components depend on the implemented modulation strategy. The bar chart of Fig. 6.11 depicts the peak and the rms currents of the most critical components, such as the switching devices, inductors, bus capacitor, and filter capacitors, at maximum power, 11 kW, for each modulation strategy.

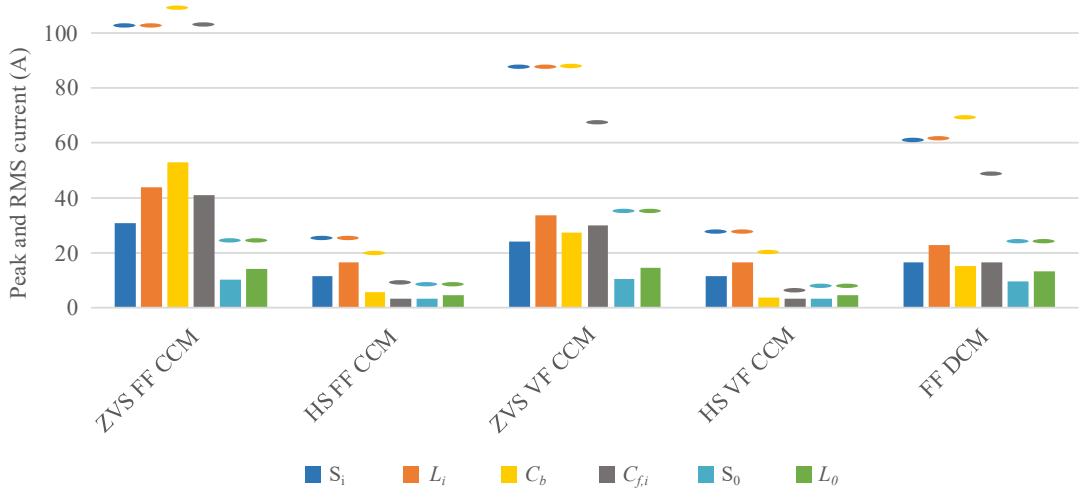


Fig. 6.11 Current ratings: peak current, I_p, (top disks) the rms current, I_{rms}, (bars) of the switching devices, S_i, boost inductors, L_i, bus capacitor, C_b, filter capacitors, $C_{f,i}$, balancing switching devices, S_0, balancing inductor, L_0, of the multi-phase PFC rectifier at maximum power, 11 kW, for each modulation strategy.

The maximum voltage applied to the switching devices is the bus voltage, i.e. 750 V. The average output current of the PFC rectifier is 14.7 A, and it is independent of the modulation strategy since it depends on the output voltage ant the bus voltage. The worst cases of rms current and peak current are found in the ZVS CCM and DCM strategies due to the high current ripple. With 104-A peak current and 30-A rms current, the ZVS FF CCM stands out among them. The HS CCM strategies, which are both very similar, get the lowest ratings of peak and rms currents, with 11.5-A rms current and 25-A peak current.

The maximum voltage applied to the boost inductors is the half of the bus voltage and the maximum of the mains voltage, i.e. 700 V. The peak currents are the same as in the switching devices whereas the rms currents are higher. The ZVS FF CCM is the worst case with 105-A peak current and 43-A rms current. The HS CCM strategies are the best cases with 25-A peak current and 16.1-A rms current.

The maximum voltage applied to the bus capacitor is the bus voltage, i.e. 750 V. The modulation strategies that get the worst and the best current rating are the same as before, the ZVS FF CCM with 110-A peak current and 53-A rms current, and the HS CCM strategies with 20-A peak current and 5-A rms current, respectively.

Finally, the maximum voltage in the filter inductor and capacitor is the mains voltage, i.e. 325 V. The current ratings of the filter coil are the mains current ratings, i.e. 23-A peak current and 16-A rms current, whereas the current rating of the filter capacitor are given by the bar chart of Fig. 6.11 for each modulation strategy. The ZVS FF CCM is the wort case with 104-A peak current and 41-A rms current.

The balancing and boost inductors have been designed considering the aforementioned current and voltage ratings. Moreover, the 40-mΩ and 1200-V SiC MOSFETs C2M0040120D from CREE have also been selected to fulfill these current and voltage requirements.

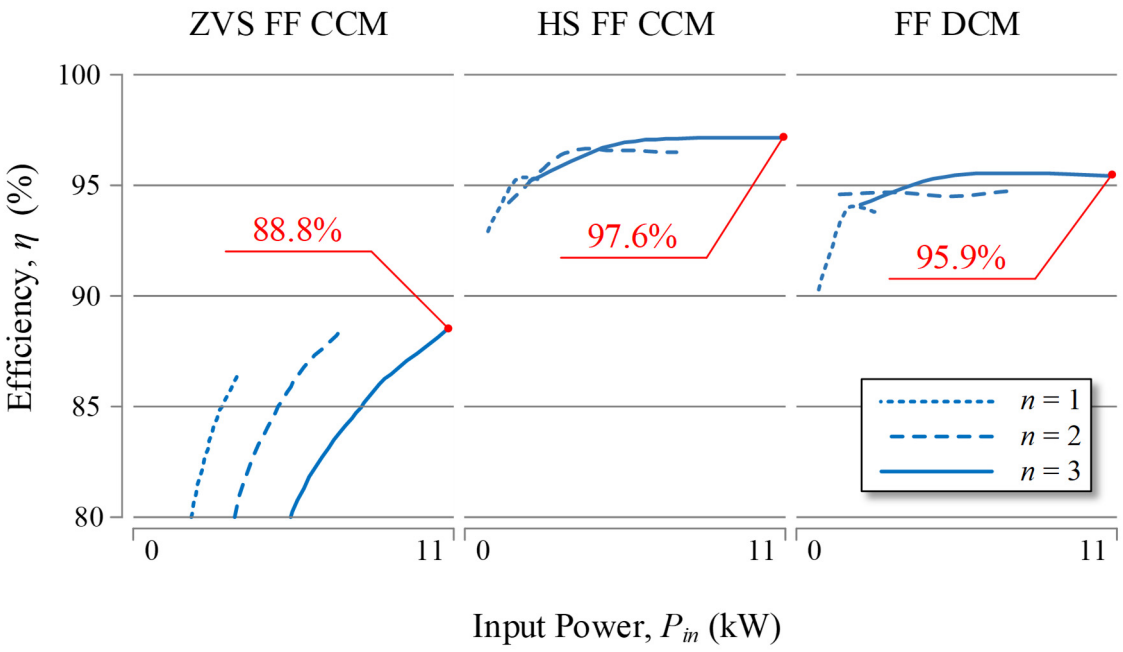
6.2.1.2. Efficiency and power loss distribution

The efficiency of the PFC rectifier, η, is calculated as

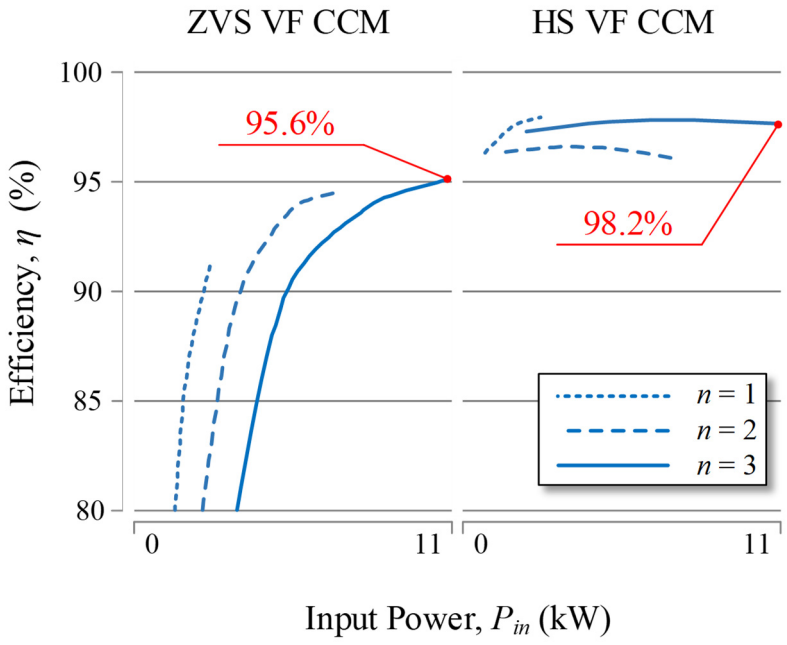
$$\eta = \frac{P_{out}}{\sum_{i=1}^{n} P_{in,i}}, \tag{6.16}$$

being P_{out} the output power, and $P_{in,i}$ the phase-i input power.

It has been experimentally measured using a 4-channel power analyzer Yokogawa PZ4000, using three channels for each input mains phase and the fourth channel for the output. The results are summarized in Fig. 6.12.



(a)



(b)

Fig. 6.12 Experimental efficiency, η, of the implemented multi-phase PFC rectifier using each modulation strategy for different numbers of activated phases, n. The efficiency has been measured in the whole operation range, from 0.7 kW to 11 kW. (a) FF and (b) VF modulation strategies

Each modulation strategy has been measured using a different number of activated phases, $n = 1$, $n = 2$, and $n = 3$. The whole power range of the converter has been analyzed, i.e. up to 11 kW., and the maximum efficiency, 98.4%, has been reached using the HS VF CCM modulation strategy.

These results show that the HS strategies get better efficiencies than the ZVS ones with the implemented switching devices. This is due to the high ripple of the boost inductance current, which increases the conduction losses in this component and in the switching devices. Even though the turn-on losses are null, the switching losses also increase because the turn-off currents are significantly high. This fact becomes more relevant in the ZVS FF CCM strategy. Additionally, the efficiency in ZVS strategies is greatly reduced in light load conditions, whereas in HS and DCM strategies this value is almost constant. This is due to the fact that the ripple increases at lower power, increasing the conduction losses. When the frequency is increased to decrease the ripple, the switching losses are higher too. Therefore, it is important to remark that in the ZVS strategies it is better to operate with less active phases, when possible, to optimize the converter efficiency. However, this consideration is not relevant in HS modulation strategies.

Fig. 6.13 shows the power loss distribution and efficiency at maximum power. The same power-loss model used in the single-phase case have been used in this case to estimate the power loss distribution. The switching energies have been obtained using charts of Fig. 6.14. It can be seen that the high ripple of ZVS and DCM strategies affects to the conduction losses of the converter components. Besides, the main contribution to power losses are the conduction and switching losses of the switching devices due to the high number of these components. Regarding the inductors, the worst case is the ZVS FF CCM strategy with 30-W loses of each boost inductor. The remaining losses of the inductors, filters, and bus capacitor are negligible.

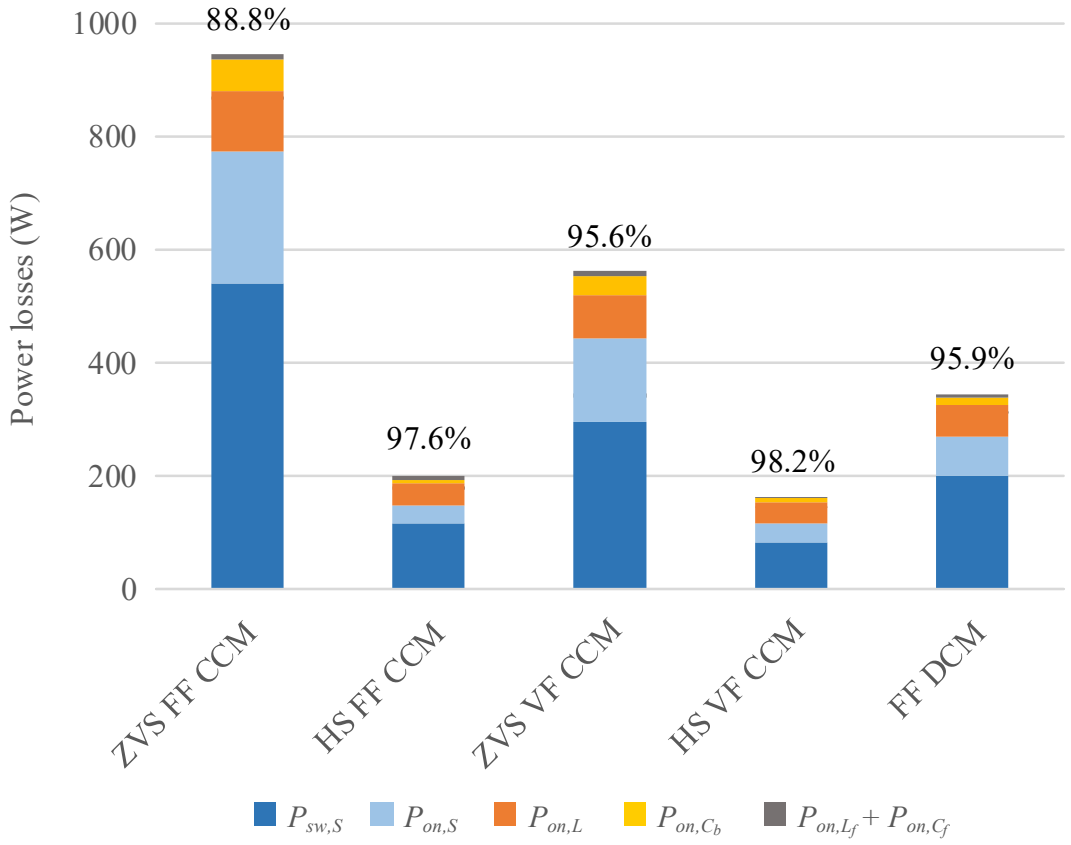
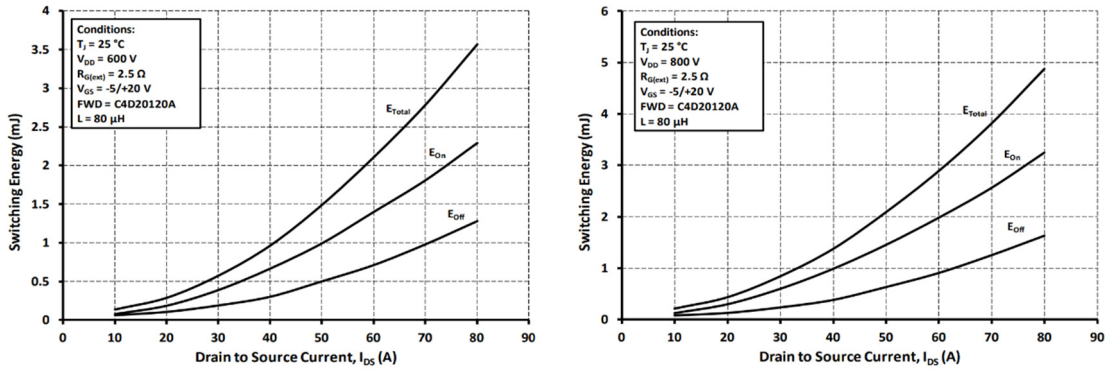


Fig. 6.13 Power loss distribution and experimental overall efficiency of the multi-phase PFC rectifier at maximum power, 11 kW, for each modulation strategy.



(a) (b)

Fig. 6.14 Turn-off switching energy, E_{off}, and turn-on switching energy, E_{on}, in function of the drain-to-source current, I_{DS}, for (a) 600 V and (b) 800 V drain-to-source voltage, V_{DS}, of the C2M0040120D MOSFET. Source: manufacturer datasheet.

6.2.1.3. Switching current and operating frequency

Fig. 6.15 shows the turn-off and turn-on average currents, and the switching losses for each modulation strategy. As in the single-phase case, it can be appreciated that the switching losses can be estimated from the average current and frequency. In ZVS CCM and DCM strategies, there are not turn-on switching losses and, therefore, the turn-on average current has not been considered. As in the single-phase case, even though the turn-on switching energy of the MOSFETs is higher than the turn-off one, the switching losses are usually higher in ZVS CCM and DCM modulation strategies because the turn-off current is lower in HS modulation strategies. Above each bar of the graph, the switching frequency is shown. For FF modulation strategies, it is constant and equal to 100 kHz, whereas the mean frequency is depicted for VF ones.

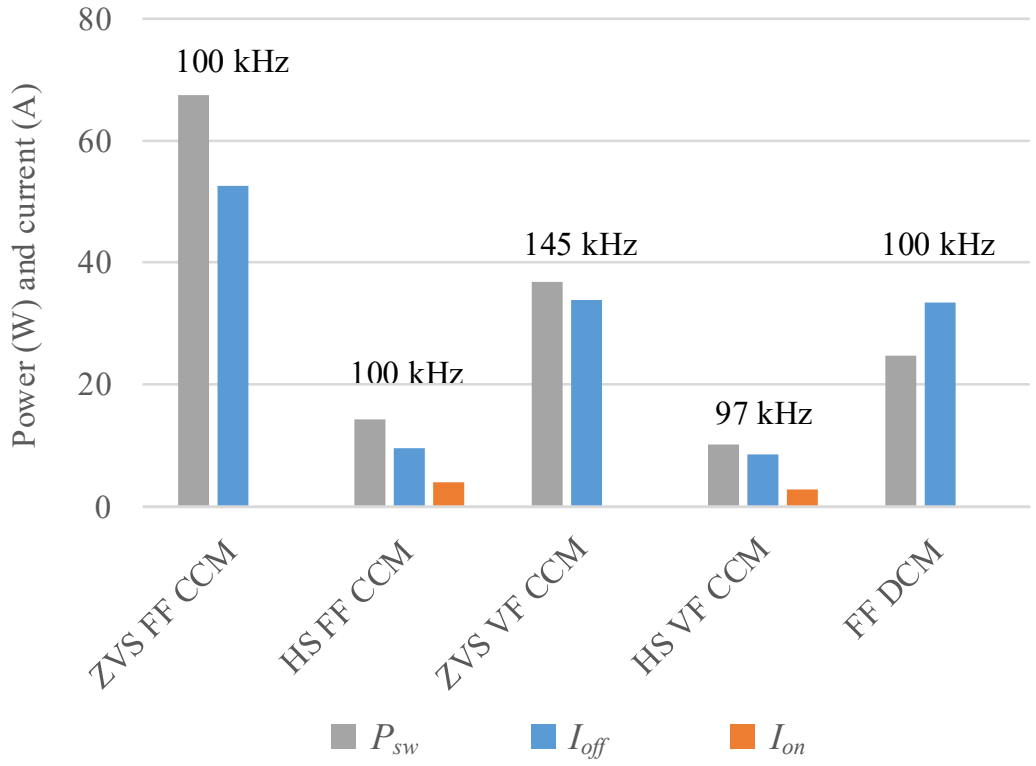


Fig. 6.15 Switching power losses, P_{sw}, and turn-off and turn-on average current, I_{off} and I_{on}, of the multi-phase PFC rectifier at maximum power, 11 kW for each modulation strategy. The operating frequency is shown above each bar (average frequency considered for variable frequency strategies).

6.2.1.4. THD and PF

Fig. 6.16 depicts the total harmonic distortion of the current, THD_i, whereas Fig. 6.17 shows the power factor, *PF*, of the implemented modulation strategies of the multi-phase PFC rectifier. On the one hand, as in the single-phase case, the THD_i worst cases are the ZVS FF CCM and the FF DCM modulation strategies. In the latter case, it is due to simplifications of the control strategy, and it can be solved using an outer control loop. In the former case, it is because the high frequency sweep, which generates small resonances among passive components and distorts the sinusoidal waveform. On the other hand, it can be appreciated that HS and DMC strategies reach a *PF* greater than 0.99, whereas in ZVS strategies the power factor is between 0,98 and 0.99. This is mainly due to the high current ripple, the frequency sweep in the VF strategy, and the phase shift between the mains voltage and the mains current in the FF modulation.

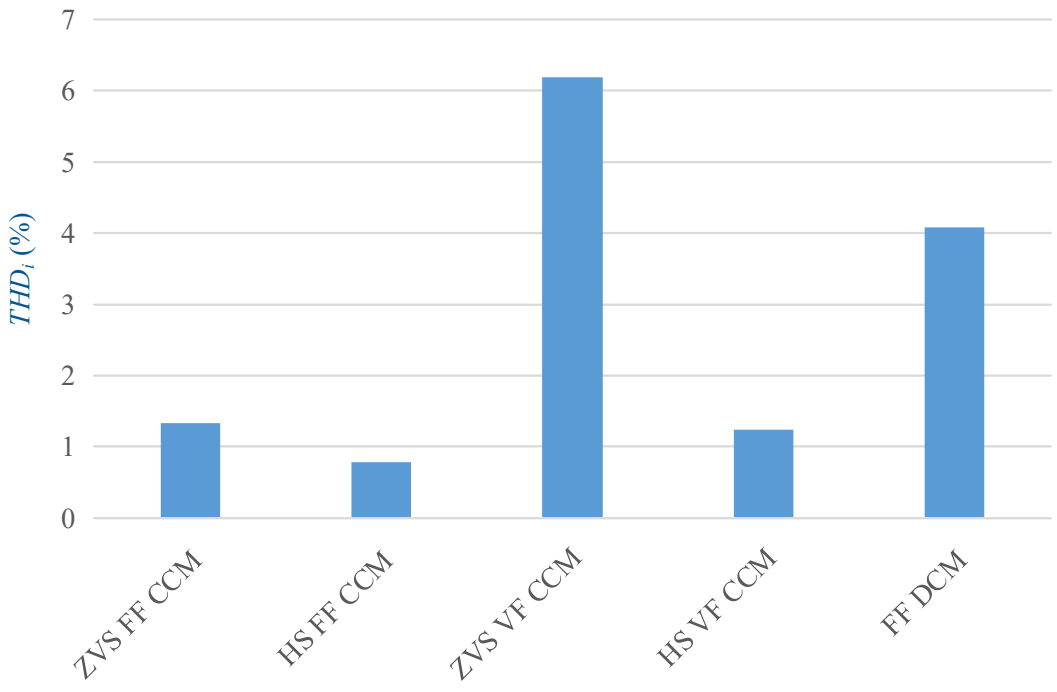


Fig. 6.16 Total harmonic distortion of the mains current, THD_i, of the multi-phase PFC rectifier at maximum power, 11 kW, for each modulation strategy.

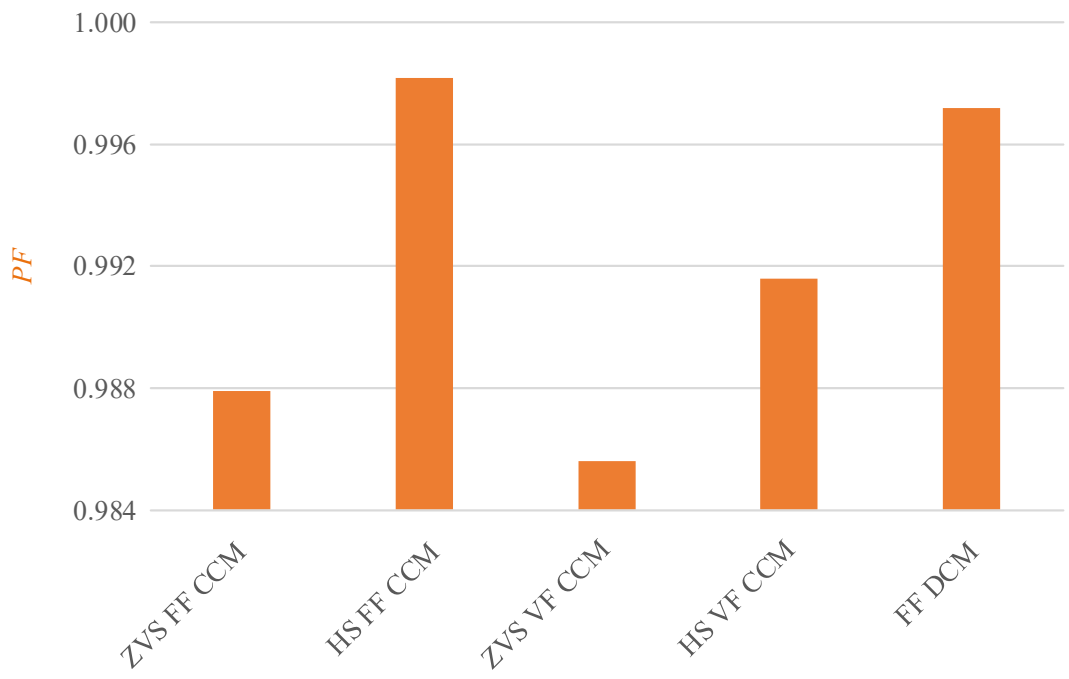


Fig. 6.17 Power factor, *PF*, of the multi-phase PFC rectifier at maximum power, 11 kW, for each modulation strategy.

6.2.2. Comparative analysis of the modulation strategies

As in the single-phase case, a comparative evaluation of the studied modulation strategies at maximum power regarding the same key figures of merit is provided to highlight the advantages and disadvantages of each strategy in this multi-phase implementation.

6.2.2.1. Normalized performance rates

The same normalized performance rates have been employed in order to provide a general quantification of each modulation strategy performance, regardless of the developed system. In this case, the mains phase rms current, $I_{rms,i}$, has been used as reference value, and the calculation of these rates is detailed below. The definition of these calculations is similar to the single-phase case, but taking into account the contribution of each phase, *i*. As a result, the summation operator is included in the equations to sum the contributions of the balancing branch, i.e. the 0 phase, and the *n* phases, being *n* the number of phases that are operating.

- Relative overall rms current

The relative overall transistor rms current is calculated as

$$\tau_{T,rms} = \frac{\sum_{i=0}^{n} I_{Th,rms,i} + \sum_{i=0}^{n} I_{Tl,rms,i}}{\sum_{i=1}^{n} I_{rms,i}}, \tag{6.17}$$

where $I_{Th,rms}$ and $I_{Tl,rms}$ correspond to the rms currents of the high and low transistors, respectively. The relative overall inductor rms current is calculated as

$$\tau_{L,rms} = \frac{\sum_{i=0}^{n} I_{L,rms,i}}{\sum_{i=1}^{n} I_{rms,i}}, \tag{6.18}$$

where $I_{L,rms}$ is the boost-inductor rms current.

- Relative maximum current

This parameter indicates the maximum current value in the boost inductors and the switching devices, and it allow performing a good selection and design of these components. This value is the same in both components, therefore it can be calculated as

$$\tau_{max} = \max_{i \in [1,n]} \left(\frac{I_{L,p,i}}{I_{rms,i}} \right), \tag{6.19}$$

where $I_{L,p}$ is the peak current of the boost inductor.

- Relative switching current

The relative turn-off current is calculated as

$$\tau_{c,off} = \frac{\sum_{i=0}^{n} I_{Th,off,i} + \sum_{i=0}^{n} I_{Tl,off,i}}{\sum_{i=1}^{n} I_{rms,i}}, \tag{6.20}$$

whereas the relative turn-on current is obtained as

$$\tau_{c,on} = \frac{\sum_{i=0}^{n} I_{Th,on,i} + \sum_{i=0}^{n} I_{Tl,on,i}}{\sum_{i=1}^{n} I_{rms,i}}. \tag{6.21}$$

$I_{Th,off}$ and $I_{Tl,off}$ show the average turn-off currents of the high-side and low-side transistors, respectively. $I_{Th,on}$ and $I_{Tl,on}$ refer to the turn-on currents.

- Relative switching frequency

In this case, the $f_{sw,avg}$ rate refers to the mean switching frequency normalized to the nominal design frequency of the multi-phase PFC rectifier, $f_{sw,PFC}$, i.e. 100 kHz. Therefore, the relative frequency sweep is calculated as

$$\delta_f = \max_{i\in[1,n]}\left(\frac{f_{sw,max,i} - f_{sw,min,i}}{f_{sw,PFC}\, f_{sw,avg}}\right), \tag{6.22}$$

where $f_{sw,max}$ and $f_{sw,min}$ refer to the maximum and the minimum switching frequencies.

- Relative losses

As in the single-phase case, the efficiency of the system is characterized by the relative losses as 1-η, being η the efficiency obtained using expression (6.16). Therefore, it can be obtained as

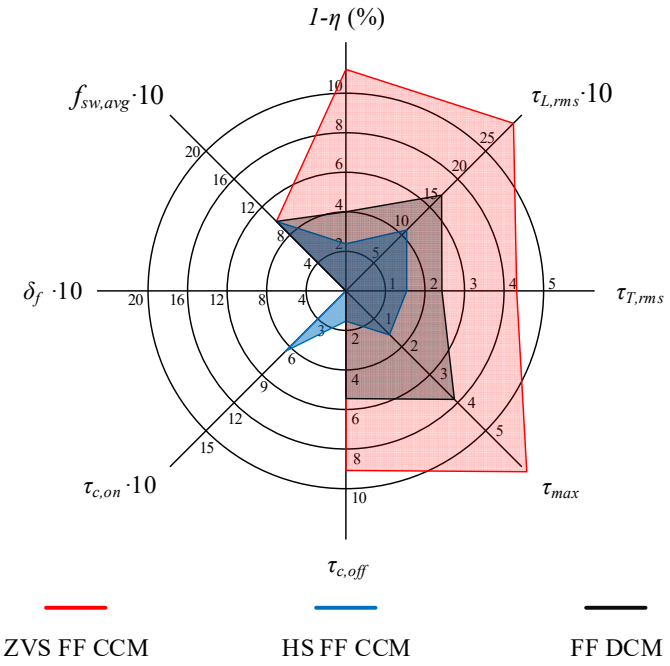
$$1-\eta = 1-\frac{P_{out}}{\sum_{i=1}^{n} P_{in,i}}. \tag{6.23}$$

6.2.2.2. Radial graphs

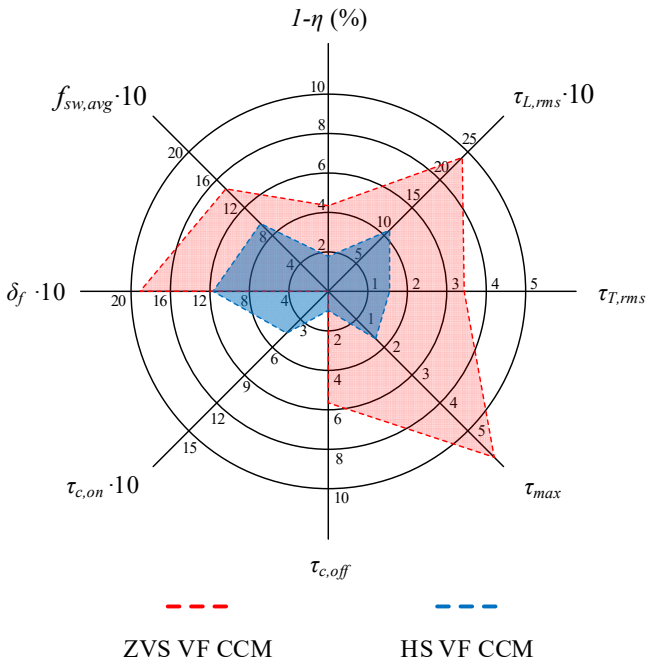
The radial graphs in Fig. 6.18 show the results of this comparative evaluation of the multi-phase PFC rectifier at maximum power. The overall efficiency of the topology highly depends on the switching mode and the ratio among the switching and conduction performance of the switching devices. In ZVS modulation strategies, the current ripple is higher, increasing rms value of the current in the switching devices, capacitors, and the boost inductance and, therefore, increasing the conduction losses. Another important consideration is that the higher the current ripple is, the higher the turn-off current becomes, leading to increased turn-off losses. Usually, the better the switching behavior is, the more recommended the HS modulation strategy is. The contrary happens when the power device conduction performance is better in comparison with the switching performance.

After this analysis, and taking into account the final domestic IH application, the HS FF CCM modulation strategy has been selected to control the proposed multi-phase rectifier. It gets a good tradeoff between efficiency, device stress, implementation, and

control complexity, fulfilling the domestic IH requirements when SiC MOSFETs are considered. In the case of an IGBT scenario, a ZVS strategy is interesting to reduce switching losses.



(a)



(b)

Fig. 6.18 Comparative evaluation at maximum power of (a) FF and (b) VF modulation strategies of the multi-phase PFC rectifier. The employed rates are as follows: the relative losses, 1-η, the relative overall rms current of the inductance, $\tau_{L,rms}$, and the transistor, $\tau_{T,rms}$, the relative maximum current, τ_{max}, the relative turn-off current, $\tau_{c,off}$, the relative turn-on current, $\tau_{c,on}$, the relative frequency sweep, δ_{sw}, and the relative mean switching frequency, $f_{sw,avg}$.

Finally, the current ratings of the current domestic IH appliance implementations using converters with full-bridge diode rectifier, and the proposed single-phase and multi-phase case using the selected modulation strategies for domestic IH applications, are compared in TABLE 6.1. Converters are delivering 3.6 kW to a domestic IH load. As it can be seen, on the one hand, the peak and rms current in the PFC stage are very similar in the full-bridge diode rectifier and single-phase case. However, it is lower for the three-phase case because the current is split among every mains phase. On the other hand, the current ratings in the inverter stage are significantly decreased using the single-phase and the multi-phase PFC rectifier in comparison with the full-bridge diode implementation because of the increased bus voltage and its low ripple.

TABLE 6.1

COMPARISON OF THE CURRENT RATINGS OF SWITCHING DEVICES IN THE RECTIFIER AND INVERTER STAGE USING DIFFERENT RECTIFIER IMPLEMENTATIONS AT 3.6 KW

Stage	Rectifier implementation	I_{rms} (A)	I_{peak} (A)
Rectifier	Full-bridge diode	8	23
	Single-phase PFC (HB)	9.75	23
	Three-phase PFC	3.9	7.7
Inverter	Full-bridge diode	24	64
	Single-phase PFC	14	27
	Three-phase PFC	7	14

Chapter 7

Conclusions

In this final Chapter, the main conclusions of this dissertation are summarized. Firstly, the most relevant conclusions and contributions obtained in each Chapter of this dissertation are summarized. After that, the main academic results are highlighted and, finally, the future research lines motivated by this dissertation are briefly explained.

Contents

7. Conclusions

In this final Chapter, the main conclusions of this dissertation and its scientific results are summarized. At the end of the conclusion section, TABLE 7.1 highlights the main novel contributions of each Chapter of this dissertation. Finally, some ideas about the future research possibilities are discussed.

7.1. Conclusions

This dissertation has been split in several Chapters focused in a common topic, the evaluation of the use of PFC rectifiers for domestic IH applications. In the first Chapter, an introduction to induction heating, the domestic applications for cooking, and the applied technology in this area have been performed.

In the second Chapter, the main power quality issues, such as mains voltage distortion or the total harmonic distortion of the current, have been presented. These effects are caused mostly because of the use of non-linear loads, such as the typical one used in domestic IH applications. Currently, these issues are solved using a small capacitor for filtering the high ripple of the current. However, it generates a high bus voltage ripple decreasing the usage ratio of switching devices and adding complexity to the control of the output power.

These converters are usually up to 3.6 kW single-phase converters, due to the current limitations of the domestic installations. Therefore, more than one converter connected to different mains phases are necessary when the total power of the appliance is higher than 3.6 kW. All these reasons motivate the research of PFC rectifiers for domestic IH, and therefore, the state of the art of rectification systems is summarized in this Chapter. These rectification systems are mainly classified in conventional, passive PFC, and active PFC rectifiers. The last ones are classified in boost, buck, buck-boost, and multi-level rectifiers. Active PFC rectifiers get a controlled low-ripple output bus voltage as well as a good consumption of the mains energy, avoiding the mains distortion issues and the high bus-voltage ripple.

7.1.1. PFC topologies

Despite the fact that PFC rectifiers have rarely implemented in commercial IH home appliances due to complexity and cost issues, advance in power electronics and control

as well as the trend towards higher performance appliances justifies the development of such systems.

In Chapter 3, the use of boost active PFC rectifiers is proposed due to its advantages for domestic IH in comparison with the other rectifier types, such as the improved efficiency in the back-end IH inverter due to the increased bus voltage, among others. In particular, the following lines summarize the main reasons for implementing a single-phase boost active PFC rectifier as front-end stage:

- EMC issues are isolated from the IH converter design, decreasing the filter size, and avoiding the use of complex control strategies.
- Improved control because of the variable and low-ripple bus voltage, enabling the operation closer to the resonant frequencies and, consequently, improving the IH inverter efficiency.
- Lower current ratings due to the higher bus voltage, decreasing conduction losses.
- Better use of switching devices because of the higher and low-ripple bus voltage.
- Due to the power storage device, i.e. the bus capacitor, increased efficiency is gotten because higher power can be pulsed. Moreover, the multiplexed control of several loads is simplified, decreasing the flicker requirements.

Moreover, as previously commented, higher performance IH cooktops are usually composed of more than one converter to be powered from several mains phases, typically two. In this context, developing a front-end stage that allows merging different mains phases in a common bus voltage is a key research line because it provides significant additional advantages to domestic IH, as discussed below:

- Higher power can be delivered to the pots, significantly decreasing the heating times.
- Hardware can be simplified due to the use of a single PCB, avoiding additional control units, isolated measurements, and auxiliary power supplies for each phase.

- Power coupling issues between different mains phases are avoided because the set of inductors is powered from a common bus.

All these benefits motivate and justify the proposal of a front-end stage. Moreover, both single-phase and multi-phase converters are interesting in this application field due to the advantages they bring. Therefore, a single-phase and a multi-phase topology are presented in this Chapter in order to investigate all these aforementioned contributions. These topologies are analyzed from the point of view of their waveforms, configuration sequences, and main equations.

On the one hand, the single-phase proposal is based on a full bridge and a boost inductor. It has a high interest because it allows different configurations: half-bridge, full-bridge, and hybrid, and therefore, different operation modes can be researched using the same topology. On the other hand, the multi-phase proposal is based on using a half-bridge branch to balance the common mains voltage of the mains phases and an additional half-bridge branch and boost inductor per mains phase. The main advantage of this topology is that it is able to operate with different number of activated mains phases because of the balancing branch, allowing different operation modes too.

7.1.2. PFC modulation strategies

The PFC function can be performed using several modulation strategies. Each one of these has different advantages and disadvantages that can encourage or make more challenging its implementation. In Chapter 4, the modulation strategies that allow controlling the proposed single-phase topology are introduced. They are classified according to the topology configuration, the conduction mode, the switching frequency, and the switching mode. Besides, the same modulations in full-bridge configuration are valid for the multi-phase topology.

On the one hand, modulation strategies using half-bridge configuration have the disadvantage of generating a zero-crossing distortion, with the exception of the discontinuous conduction mode. On the other hand, the full-bridge configuration avoids this issue at the cost of a higher rms and peak currents, increasing the current in passive components and switching devices, especially in ZVS strategies. In order to solve this drawback, the hybrid configuration and the hybrid control strategies are proposed, taking the advantages of both the half-bridge and full-bridge configurations. Fixed-frequency modulation strategies are interesting in the domestic IH field because they decrease the

risk of intermodulation noise. Besides, this frequency can be synchronized with the switching frequency of the IH inverter.

The proposed modulation strategies have different performance and requirements, and, from an implementation point of view, the design of the control loop is different for each one. Therefore, six control strategies have been proposed in this Chapter in order to implement them. They are based on the use of closed-loop controllers or the calculation of different parameters, such as duty cycle or activation times, among others. Besides, it is important to note that these equations depend of the topology type and configuration.

7.1.3. Implementation and experimental results

In Chapter 5, the proposed topologies and modulation strategies have been implemented for both single-phase and multi-phase configuration. In particular, a 3.7-kW, 400-V and single-phase versatile platform using SiC MOSFETs, and different voltage and current measurements, is implemented in order to allow testing each proposed modulation strategy. Besides, this prototype includes an additional half-bridge branch to power a domestic IH load.

In order to test the multi-phase configuration, an 11-kW, 750-V and three-phase versatile platform has also been designed and implemented. In this prototype design, maximum power density is pursued in order to fulfill the requirements of the final IH application. Besides, an application to domestic IH is performed using a multi-output IH inverter. For doing this, the implementation of a matrix converter is carried out, focusing on the topology and the prototype implementation. Finally, the matrix converter and the multi-phase rectifier are connected to power an 11-kW IH load.

The main waveforms of both protypes are presented showing the proper operation and the viability of the single-phase rectifier, the multi-phase rectifier, and their modulation and control strategies. Moreover, in this Chapter, the overall implementation, including topology, modulation strategy, control strategy, and final prototype, of an ad-hoc three-phase regulable power supply with active current control is detailed, which has been used to perform the experimental tests, powering the aforementioned single-phase and multi-phase PFC rectifiers, IH inverters, and IH loads. This power supply has the advantage of controlling and limiting the output current, increasing the safety of the power supply and decreasing the risk of breaking of back-end prototypes when improper operation is detected.

7.1.4. Result analysis and discussion

In Chapter 6, the measurements and results obtained using the implemented prototypes are analyzed and compared in order to discuss the main advantages and drawbacks of each implemented modulation strategy. In particular, several parameters have been taken into account, such as device stress, efficiency, power loss distribution, operating frequency, switching current and EMC issues. All of them allow finding the modulation strategy better suited according to the implementation requirements and the application area. Besides, comparative evaluations at maximum power using normalized performance rates independent of the developed system have been provided to better highlight the strong points of each strategy.

According to the performed analysis, in both single-phase and multi-phase cases, the HS FF CCM modulation strategy gets a good trade-off between efficiency, device stress, implementation and control cost, and EMC. Besides, it avoids the zero-cross distortion in full-bridge or hybrid configurations, and the acoustic noise, since it works at a fixed frequency. In the case of IGBT scenario, a ZVS strategy could be more interesting to reduce switching losses. TABLE 7.1 below summarizes the main novel contribution of this dissertation.

TABLE 7.1

SUMMARY OF THE MAIN NOVEL CONTRIBUTIONS

CHAPTER	CONTRIBUTIONS
1	• Study of the state of the art of IH.
2	• Study of the state of the art of rectifier systems and PFC for IH.
3	• Single-phase PFC rectifier topology for half-bridge, full-bridge, and hybrid configurations. • Multi-phase PFC rectifier topology with balancing branch. • Study of the main advantages of single-phase and multi-phase topologies for domestic IH applications. • Analysis of waveforms, configuration sequences, and main equations of the proposed rectifiers.
4	• Comparative study of modulation strategies for single-phase and multi-phase PFC rectifiers and their advantages. • Control strategies for implementing every proposed modulation strategy using closed-loop control of the inductor voltage, hybrid strategies, or hybrid strategies for fixed frequency operation, among others.
5	• 22-kW and three-phase regulable power supply with active current control. • 3.7-kW and single-phase PFC rectifier for IH. • 11-kW and three-phase PFC rectifier for domestic IH. • 11-kW and 4-output matrix inverter for domestic IH.
6	• Result analysis with regard to device stress, efficiency, power loss distribution, switching current, operating frequency, THD, and PF for single-phase and three-phase implementation. • Comparison using radial graphs of the modulation strategies for single-phase and multi-phase converters.

7.2. Scientific results

This dissertation has been developed in the framework of several research and development projects, as well as research visits to other research centers and universities. The main results of this dissertation have been published in peer reviewed international journals, international conferences, and national conferences. The most relevant results are summarized below.

7.2.1. International journals

[1] H. Sarnago, Ó. Lucía, M. Pérez-Tarragona, and J. M. Burdío, "Dual-Output Boost Resonant Full-Bridge Topology and its Modulation Strategies for High-Performance Induction Heating Applications," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 6, pp. 3554-3561, 2016.

[2] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "High performance full-bridge multi-inverter featuring 900-V SiC devices for domestic induction heating applications," *EPE Journal,* pp. 1-10, 2017.

[3] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "Design and Experimental Analysis of PFC Rectifiers for Domestic Induction Heating Applications," *IEEE Transactions on Power Electronics,* vol. 33, no. 8, pp. 6582-6594, 2018.

[4] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "A Front-End PFC Stage for Improved Performance of Flexible Induction Heating Appliances" accepted for publication in *International Journal of Applied Electromagnetics and Mechanics.*

[5] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "Multi-Phase PFC Rectifier and Modulation Strategies for Domestic Induction Heating Applications" accepted with major revisions for publication in *IEEE Transactions on Industrial Electronics.*

7.2.2. International conferences

[1] M. Pérez-Tarragona, H. Sarnago, Ó. Lucia, and J. M. Burdío, "Series resonant multi-inverter prototype for domestic induction heating," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, 2015, pp. 005444-005449.

[2] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "Full-bridge series resonant multi-inverter featuring new 900-V SiC devices for improved induction heating appliances," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1762-1766.

[3] M. Pérez-Tarragona, H. Sarnago, O. Lucía, and J. M. Burdío, "Active Power Factor Corrector for High Power Domestic Induction Heating Appliances," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 3779-3784.

[4] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "Soft-Transient Modulation Strategy for Improved Efficiency and EMC Performance of PFC Converters Applied to Flexible Induction Heating Appliances," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 3530-3534.

[5] M. Pérez-Tarragona, H. Sarnago, O. Lucía, and J. M. Burdío, "Power Factor Corrector for Flexible Domestic Induction Heating," in *International Conference on Heating by Electromagnetic Sources (HES-19)*. Padua, Italy, 2019, vol. 1, pp. 309-314.

7.2.3. National conferences

[1] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "Prototipo de multi-inversor resonante serie para calentamiento por inducción doméstico," in *XXII Seminario Anual de Automática, Electrónica industrial e Instrumentación*, Zaragoza, 2015.

[2] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "Multi-inversor puente resonante serie con dispositivos SiC de 900 V para aplicaciones de calentamiento por inducción mejoradas," in *XXIII Seminario Anual de Automática, Electrónica industrial e Instrumentación*, Elche, 2016.

[3] M. Pérez-Tarragona, H. Sarnago, O. Lucía, and J. M. Burdío, "Diseño de una etapa de potencia con PFC activo para calentamiento por inducción doméstico," in *XXIV Seminario Anual de Automática, Electrónica industrial e Instrumentación*, Valencia, 2017.

[4] M. Pérez-Tarragona, H. Sarnago, O. Lucía, and J. M. Burdío, "Estrategia de modulación de transición suave para la mejora de convertidores PFC aplicados a electrodomésticos de calentamiento por inducción flexible," in *XXV Seminario Anual de Automática, Electrónica industrial e Instrumentación*, Barcelona, 2018.

7.2.4. Awards and additional merits

The author of this dissertation has carried out some visits that have contributed to the results of this dissertation. These visits are listed and briefly described below:

- Research Engineer Internship at BSH Home Appliances Group, from June 1, 2015 to September 30, 2015. Advisor: Sergio LLorente.
- Academic Internship at the Power Electronics, Machines and Control (PEMC) Research Group, UK, from September 3, 2018 to December 2, 2018. Advisor: Prof. Pericle Zanchetta.

The most relevant additional merits are also summarized below:

- BSH Home Appliances – University of Zaragoza innovation award. October 2015.
- Extraordinary award for the best academic transcript of the master´s degree in Electronic Engineering in 2016.
- PhD scholarship of the Spanish Government (FPU grant). September 2016 - September 2020.
- BSH Home Appliances – University of Zaragoza innovation award. October 2017.
- IECON 2017. IES Student Paper Travel Assistance. November 2017.
- APEC 2018 Student Travel Support. March 2018.
- Short term mobility funding for FPU scholarships. September 2018 - December 2018.

7.3. Future research lines

This dissertation is focused on the study of PFC rectifiers for domestic IH applications. As a result of this work, a single-phase and a multi-phase rectifier and their modulation strategies have been proposed and analyzed. Future research lines are mainly oriented towards a further analysis of the cost, improved efficiency design of the back-end inverter, analysis of future fixed frequency EMC standards, new techniques for low power control, and the use of controlled rectifiers for power recovery systems for wireless power transfer systems (WPT).

7.3.1. Cost analysis

In this dissertation a technical analysis of the single-phase and multi-phase PFC rectifiers has been performed, focused on the topology, its modulation strategies and control strategies, and the performance result analysis. In order to analyze the commercial viability of this approach and perform a comparison with the current technology, an in-depth cost analysis is necessary, taking into account additional advantages and disadvantages of an industrialized solution [172].

7.3.2. Fixed-frequency EMC standards

Recently, there is a clear tendency towards increasing the number of devices, including home appliances, that use the principles of electromagnetic induction in applications not only related to induction heating but also wireless power transfer in a

broader sense. Besides, in most cases, these appliances or devices feature Bluetooth, LORA, and/or Wi-Fi connectivity. For these reasons, the implementation of different standards is being analyzed to avoid interferences among wireless devices and to allow a good compatibility. One of these standards considers fixed operating frequency for each application field. In this possible situation, domestic IH should operate at fixed frequency and the implementation of a PFC rectifier could be mandatory.

7.3.3. Low power control

Operation under light-load conditions is challenging in many applications of power electronics, and induction heating is no exception. It is specially challenging due to the use of resonant inverters. In these conditions, the control is typically performed using the pulse density modulation (PDM) strategy in order to avoid higher switching frequencies, and therefore, power losses. However, flicker standard limits the amount of pulsed power and minimum pulsation period. In practice, this leads to high power and long pulsation periods that may be notice by the user when cooking, and even affect the cooking process. For these reasons, an interesting approach is to operate the multi-phase converter in single-phase mode using a low-level bus voltage to power low demand loads, avoiding the use of PDM strategy. This approach will improve the performance of the domestic IH appliances because pulsation will not be perceived by the users, a better quality of cooking will be obtained, and an improved efficiency will decrease power loses at low power.

7.3.4. Controlled rectifiers for WPT

In the manufacturing process of the domestic IH appliances as well as in other application fields, it is needed to perform intensive tests for calibration, quality control, and to detect infantility issues, among others. Currently, these tests are performed using external IH loads and, therefore, a significant amount of power is wasted. For these reasons, the use of controlled rectification techniques is proposed to build regenerative IH loads that enables performing the test-phase in a more efficient process and emulating different possible IH loads.

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