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An anti-islanding protection based on RoCoF compliant with ENTSO-E and IEC 62116

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Abstract. In case of unintentional islanding, distributed generation units must be able to detect it and disconnect from the grid in less than 2 seconds. In this work, a Rate of Change of Frequency (RoCoF) method has been developed for islanding detection. Since these algorithms are conditioned by the requirements of grid codes, ENTSO-E network code and IEC 62116 have been taken into account.

The RoCoF anti-islanding algorithm has been developed in MATLAB-Simulink and implemented through rapid prototyping techniques in an FPGA ALTERA Cyclone V. To check the proposed protection algorithm, simulation tests have been carried out. Finally, the RoCoF anti-islanding protection has been validated using FPGA in the loop and experimentally in a real 20-kW inverter.

Key words. Anti-islanding protection methods, Rate of Change of Frequency (RoCoF), microgrids, power quality.

1. Introduction

Modern societies are establishing high renewable energies integration to get carbon neutrality in the medium term in the fight with climate change. In the case of the European Union, by way of global objectives up to 2030 it includes a 40% reduction in greenhouse gas emissions compared to 1990, and a 90% reduction in 2050. Distributed generation can help to provide the way to integrate high renewable energy penetration [1] by means of microgrids. Most microgrids can work both in grid connected mode and in islanded mode [2]. Unintentional islanding is problematic, because it is performed by an external agent and the microgrid plant controller is not aware of this issue. Thus, if local generators continue injecting power, there is a safety issue and maintenance workers can be at risk of electrocution. In consequence, a reliable anti-islanding protection scheme is one of the major concerns in distributed generation units [3].

The Rate of Change of Frequency (RoCoF) is the time derivative of the system power frequency and it is one of the most frequently used protection algorithms in distributed generation units [4]-[5].

In this paper, constraints imposed by ENTSO-E and IEC 62116 are taken into consideration in the developed RoCoF algorithm. The anti-islanding protection is developed in MATLAB-Simulink and directly implemented in a FPGA Cyclone V as part of a 20-kW PV inverter for experimental testing.

2. RoCoF protection

A. Islanding standards and Non-Detection Zones (NDZ)

The IEC 62116 establishes the procedure for evaluating the operation of anti-islanding algorithms implemented in distributed generation units, as can be seen in Fig. 1 [6].

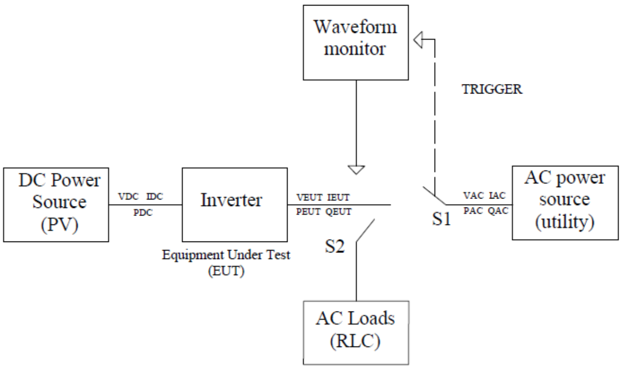

Fig. 1. Experimental arrangement for the IEC 62116 test procedure.

According to these regulations, test conditions are determined by the quality factor (Q_f), the detection time (T_{trip}) and the normal ranges of operation in voltage and frequency. The quality factor is defined in the equation (1).

$$Q_f = R \cdot \sqrt{\frac{C}{L}} \tag{1}$$

Active power balance between generation and load determine the residual voltage reached at the Point of Common Coupling (PCC) [7]. Nevertheless, frequency is determined by the reactive power balance.

During the test of the response to an islanding event, the active power (ΔP) and reactive power (ΔQ) mismatches are not enough to shift the frequency (f) out of its normal operating range, making islanding detection impossible. The NDZs can be evaluated from the following equations that determine the relationship between active power and voltage and between reactive power and frequency [8]:

$$\left(\frac{V}{V_{max}}\right)^2 - 1 \leq \frac{\Delta P}{P} \leq \left(\frac{V}{V_{min}}\right)^2 - 1 \tag{2}$$

$$Q_f \cdot \left(1 - \left(\frac{f}{f_{min}}\right)^2\right) \leq \frac{\Delta Q}{P} \leq Q_f \cdot \left(1 - \left(\frac{f}{f_{max}}\right)^2\right) \tag{3}$$

Where the parameters ($V_{max}, V_{min}, f_{max}, f_{min}$) are the limits of the allowed operating range according to grid codes.

Fig. 2 shows the calculated NDZ of IEC 62116 and ENTSO-E according to expressions (2) and (3) [9].

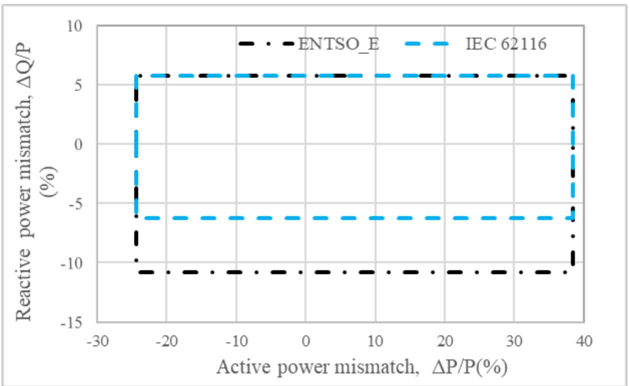

Fig. 2. NDZ of ENTSO-E and IEC 62116 comparison.

B. Reduction of Non-Detection Zone with RoCoF anti-islanding scheme

The RoCoF is one of the most common anti-islanding algorithms which is able to reduce the NDZ of the over/under voltage and frequency protection.

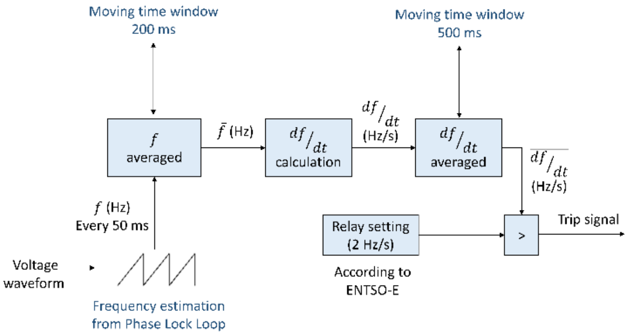

Fig. 3. RoCoF schematic diagram.

As explained before and as shown in Fig. 3, RoCoF protection is used for islanding detection. Firstly, the algorithm measures the frequency at the PCC. This frequency is estimated from the voltage signal with a Phase Lock Loop (PLL). Secondly, the derivative of frequency is calculated, and a low-pass filter is employed for eliminating high frequency harmonics [10]. Thereby the RoCoF value is obtained using a moving average filter. Finally, the RoCoF value is compared with a predefined threshold according to standards in order to detect islanding operation [9].

ENTSO-E network code establishes the ranges in voltage, frequency and derivative of frequency in which distributed generating units must remain connected. In the case of derivative of frequency, generator units must withstand ramps of 2 Hz/s (measured in a moving time window of 500 ms). This threshold and measurement window length must be taken into consideration in the RoCoF protection [11].

C. Anti-islanding protection algorithm based on RoCoF

The RoCoF anti-islanding algorithm considers an actualization time of 50 ms. In each cycle, the sum of the measured frequencies ($S = \sum f_i$) is saved, as well as the number of measurements (n) taken in this cycle. To store these values, four variables are used. Thus, each 50 ms new measurement of S and n are saved and the oldest ones are deleted. Every 200 ms, the frequency average is calculated from the values stored in the four variables, with a 50 ms latency.

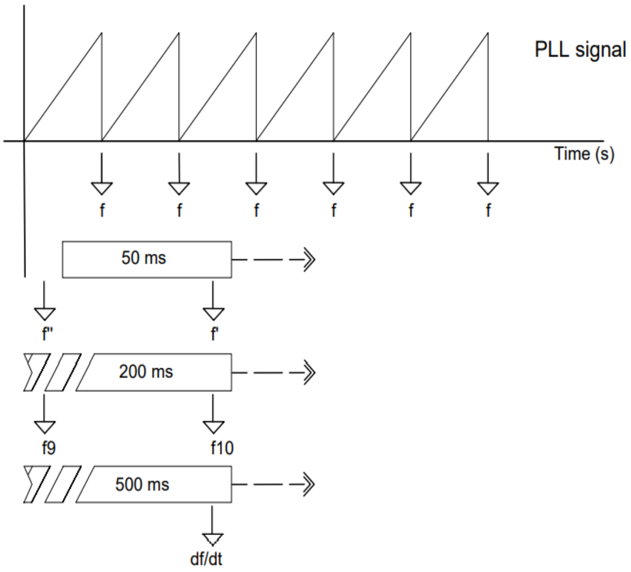

Fig. 4. RoCoF algorithm implementation in compliance with ENTSO-E thresholds.

Next, to calculate the derivative of frequency, a moving time window of 10 samples (with a length of 500 ms) is defined. The result is compared with a 2 Hz/s threshold to detect the islanding condition. In Fig. 4 the process calculation is schematized.

3. RoCoF protection simulation results

The RoCoF anti-islanding algorithm has been implemented in Simulink as well as in the inverter. The behaviour of the developed algorithm is tested in several points of the NDZ set by ENTSO-E.

The first NDZ point is shown in Fig. 5 corresponding to $\frac{\Delta P}{P}$ = 38.40% and $\frac{\Delta Q}{P}$ = 3.88%, which means a stationary frequency of 51 Hz. $\frac{\Delta P}{P}$ and $\frac{\Delta Q}{P}$ are defined for Q_f = 1 as follows

$$\frac{\Delta P}{P} = \frac{P_{load} - P}{P} \tag{4}$$

$$\frac{\Delta Q}{P} = \frac{Q_{load} - Q}{P} \tag{5}$$

where P and Q are the active and reactive power generated by the inverter, P_{load} and Q_{load} are the active and reactive power of the load.

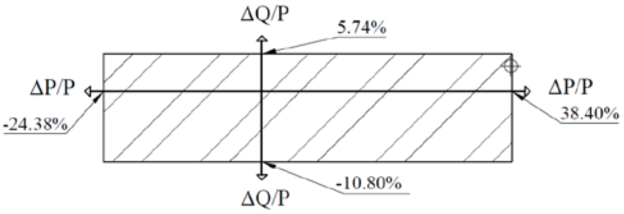

Fig. 5. NDZ point with $\frac{\Delta P}{P}$ = 38.40% and $\frac{\Delta Q}{P}$ = 3.88%.

The obtained results are shown in Fig. 6 As it can be seen, at time 1 s, a breaker opens the grid connection simulating islanding in accordance with IEC 62116 test procedure. The actuation time of the algorithm is much lower than the required 2 s. In this case, the voltage and frequency protections will not trip because the residual voltage reached is 0.85 p.u. and the frequency is 51 Hz, and both of them are within the admissible operating range according to the ENTSO-E (0.85 p.u. – 1.15 p.u. and 47.5 Hz – 51.5 Hz). Nevertheless, this disconnection of the grid causes a derivative in frequency of 2 Hz/s that is equals to the threshold admitted by ENTSO-E, and the developed algorithm is able to detect the islanding condition.

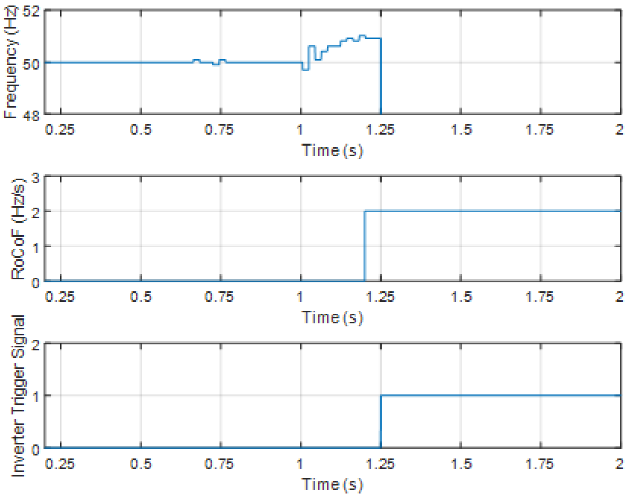

Fig. 6. Simulation results for $\frac{\Delta P}{P}$ = 38.40% and $\frac{\Delta Q}{P}$ = 3.88%.

Fig. 7 shows the NDZ point analysed in a second study case. In this scenario, $\frac{\Delta P}{P}$ = -24.38% and $\frac{\Delta Q}{P}$ = 3.88%.

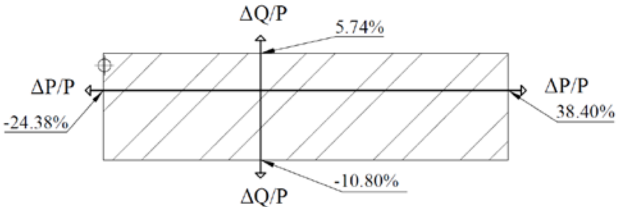

Fig. 7. NDZ point with $\frac{\Delta P}{P}$ = -24.38% and $\frac{\Delta Q}{P}$ = 3.88%.

As seen in Fig. 8, resonance frequency and residual voltage are within ENTSO-E protection limits involving not-islanding recognition from over/under frequency and voltage protections. Moreover, it can be noticed that once again the algorithm response is much faster than the 2 s required by standards and the voltage and frequency protections will not trip because the residual voltage reached is 1.15 p.u. and the frequency is 51 Hz.

Although voltage and frequency values are within the admissible operating range, this disconnection of the grid causes a derivative in frequency of 2 Hz/s and the RoCoF anti-islanding algorithm detects the islanding condition.

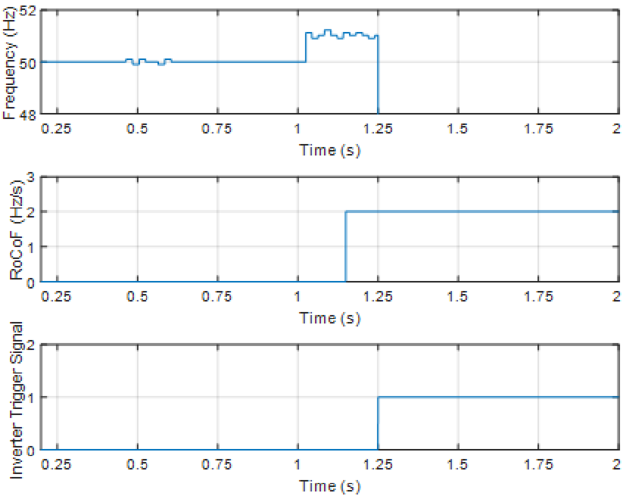

Fig. 8. Simulation results for $\frac{\Delta P}{P}$ = -24.38% and $\frac{\Delta Q}{P}$ = 3.88%.

A. FPGA in the loop co-simulation

Once the algorithm protection is fully tested in MATLAB-Simulink, HDL Coder generates VHDL code to be integrated into the FPGA ALTERA Cyclone V as part of the whole inverter control. With this rapid prototyping technique, the VHDL algorithm is evaluated through FPGA in the loop (FIL) techniques [12] and finally it is experimentally tested. Fig. 9 shows the FPGA in the loop set-up used for testing the RoCoF anti-islanding protection.

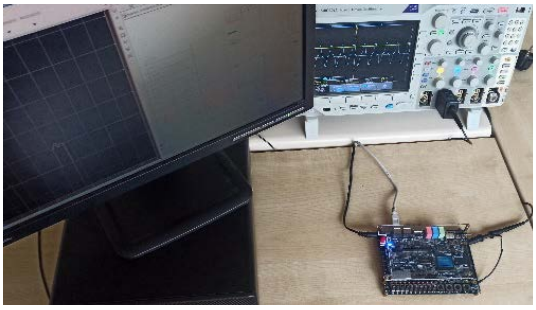

Fig. 9. FPGA in the loop testing.

FPGA in the loop provides an environment to validate HDL code for real implementation in hardware [13]. In this way, fixed-point algorithm code and VHDL synthesizability can be improved and validated as a previous step to the final implementation in the inverter [14] and, once the HDL is optimized, the anti-islanding RoCoF protection is programmed and implemented in the FPGA and co-simulated with the digital inverter twin.

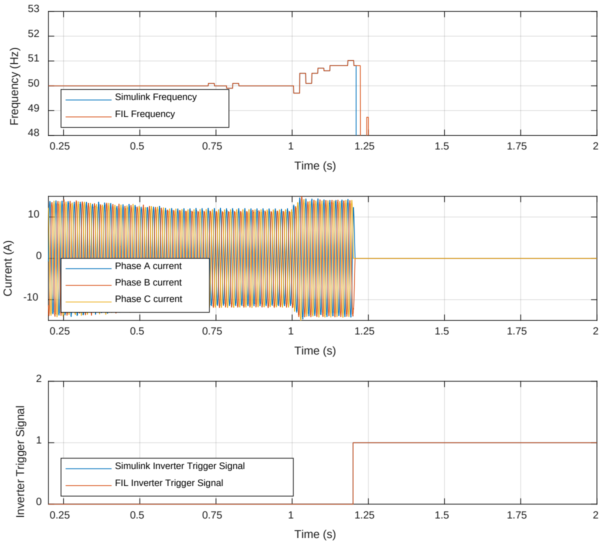

Fig. 10. Simulation results for $\frac{\Delta P}{P}$ = 38.40% and $\frac{\Delta Q}{P}$ = 3.88% of Simulink and FIL.

Fig. 10 shows the comparison between FIL and Simulink results for an NDZ point with $\frac{\Delta P}{P}$ = 38.40% and $\frac{\Delta Q}{P}$ = 3.88%. In this figure, the protection of the inverter digital twin is disconnected by the FIL inverter trigger signal.

As it can be seen, FPGA in the loop allows the validation of the detection method and the verification of the correspondence between Simulink and VHDL implementations.

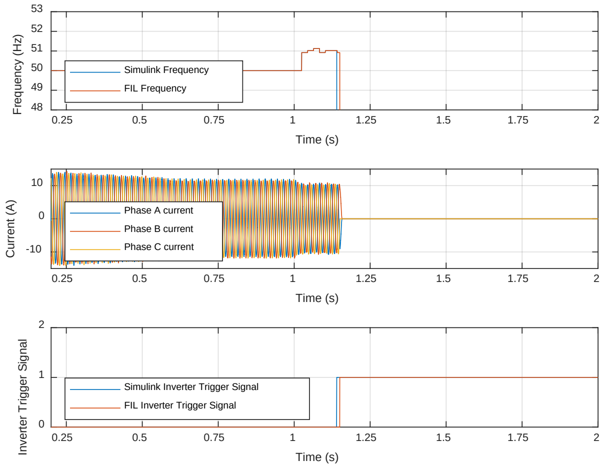

Fig. 11. Simulation results for $\frac{\Delta P}{P}$ = -24.38% and $\frac{\Delta Q}{P}$ = 3.88% of Simulink and FIL.

Fig. 11 shows a good agreement between Simulink and FIL results for an NDZ point with $\frac{\Delta P}{P}$ = -24.38% and $\frac{\Delta Q}{P}$ = 3.88%.

B. *Experimental verification of the RoCoF anti-islanding algorithm*

Finally, the RoCoF anti-islanding protection is tested in a real 20-kW inverter, as it is illustrated in Fig. 12. In this experimental set-up, the islanding condition occurs when a three-phase parallel RLC load is connected. The frequency resonance of the RLC load is 51 Hz, calculated according to [8].

Fig. 12. Experimental verification of the RoCoF anti-islanding protection in a 20-kW inverter.

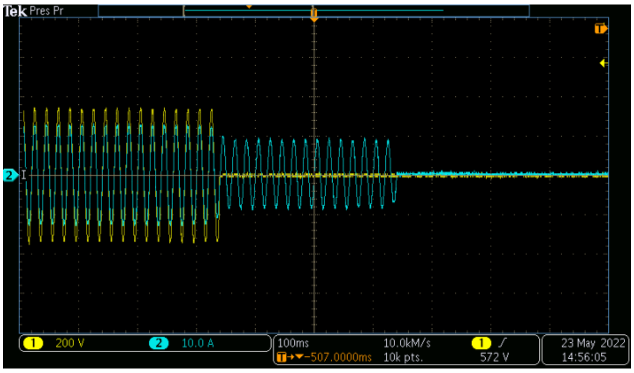

Fig. 13. The grid voltage (in yellow) and the inverter output current (in blue) at the PCC.

Fig. 13 shows the inverter output current and voltage at the PCC. As it can be seen, the RoCoF protection has the ability to cut off the inverter output current when the RoCoF protection detects islanding condition.

Conclusions

In this paper the complete development of a passive detection anti-islanding algorithm based on the Rate of Change of Frequency (RoCoF) is explained, taking into account technical restrictions that are imposed by grid connection regulations, with the main objective of reducing over/under frequency and voltage protection Non-Detection Zones (NDZ).

Simulink, FPGA in the loop and experimental tests have been used to validate the proposed RoCoF protection algorithm, which is found to be accurate and fast enough according to standards.

This paper can be a good guide for developers, since it shows the whole process, from algorithm creation to code validation.

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