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Massive Parallel Current Power Amplifier Concept for Power Hardware in the Loop Applications

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Abstract. The development of the smartgrid increases the complexity of the current electric grid. To verify and validate the operation of the systems involved in it, Power Hardware-In-the-Loop (PHIL) technique allows to test the complete system in an exhaustive way. But the reduced bandwidth of the overall test system can cause inaccuracies and instabilities, which can be harmful for the Hardware Under Test (HUT) or the people who are performing the test. To increase PHIL performance and tackle these problems, this paper proposes a new concept of high bandwidth current amplifier. It is based on a topology of massive parallel interleaved buck-boost converter, which distribute in an equal manner the total current in all the branches. This current reduction allows to use transistors with better switching behaviour, which increase the bandwidth of the converter. Furthermore, a Discontinuous Conduction Mode (DCM) is used, obtaining the nominal output current in only one switching cycle. Description of the concept and the design parameters are provided. Finally, the behaviour of the proposed Power Amplifier (PA) at high frequency setpoint currents is shown in a Matlab/Simulink simulation.

Key words. PHIL, high bandwidth current amplifier, DCM operation.

1. Introduction

The integration of renewable energies in the electric grid introduces several challenges. Among these challenges are the intermittency of their supply or the lower energy density compared with fossil fuels. To deal with these problems, the electricity network has to be able to integrate the actions of all the users connected to it in a clever way, which is called smartgrid [1].
The smartgrid development will increase the number and the diversity of the equipment installed in the electric grid. This increment will be remarkable in low grid voltages, due to the inherent lower investment per system and the proximity to the final customer. The new elements must communicate and operate between them, sometimes taking their own decisions, in order to efficiently deliver sustainable, economic and secure electricity supplies. Therefore, many authors anticipate an increase in the complexity of the electric network [2]–[4].
As a consequence of this rise in complexity, the modelling, analysis and design of future power system face new challenges. To guarantee the reliable operation of these new technologies, the test systems techniques are playing an important role. A promising test technique is Power Hardware-In-the-Loop (PHIL), which has the best trade-off between test coverage and test fidelity [5]. Fig. 1 shows a typical PHIL configuration, which is based on two main elements, the Digital Real-Time Simulator (DRTS) and the Power Amplifier (PA). The DRTS runs a mathematical model of the simulated system, which is executed in real-time. It sends the output set-point to the PA at every time-step. This PA generates the real voltage or current received from the DRTS. The Hardware Under Test (HUT) reacts with a current or voltage respectively, which is measured by the PA and by the DRTS sensors. The DRTS adds this measured value back to the mathematical model to calculate the next step.

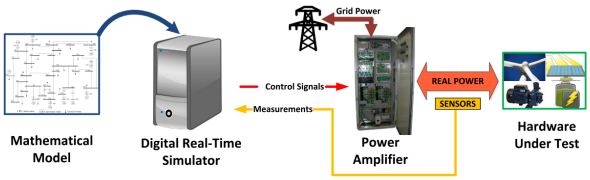

Fig. 1. PHIL basic structure, identifying most representative subsystems: Mathematical model, Digital Real-Time Simulator (DRTS), Power Amplifier (PA), and Hardware Under Test (HUT).

The main advantage of a PHIL test bench is that ideally, this can behave like any other electric system, using the same hardware for any purpose, only changing the software configuration of the real-time simulation system.

Table I. Advantages and disadvantages of different types of power amplifiers [5], [6].

	Advantages	Disadvantages
Switched amplifier	• Less expensive • Highest efficiency • Great flexibility (can operate both as current and voltage amplifier) • Smallest size • Lowest operating temperature • Low-power factor handling	• High delay and lower accuracy than linear amplifier
Linear amplifier	• Very high dynamic performance (0-5kHz bandwidth or more) • Short time delay • Easy transfer function with fewer stability issues • Highest crest-factor • Highest start-up surge current	• Very low power efficiency • Low power output (as a consequence of the first one) • Biggest size
Synchronous generator	• High power output	• Only for testing where balanced three phase power is required. • Higher level of time delay and the lowest accuracy

However, non-ideally issues, such as inaccuracy and reduced bandwidth of the overall test in closed loop, limits the range of tests due to problems of stability during the tests. To increase this range of tests in power and bandwidth, the PA plays a major role. Therefore, a PA with higher cut-off frequency and a major power capability can extend the test range.

In this paper, a new design of PA for PHIL tests is described. Section II shows a state of the art of the PA that can be found in the literature. In Section III the proposed concept is introduced and the design of the current power amplifier is presented. In Section IV the behaviour of the PA in a Matlab/Simulink simulation is analyzed. Finally, Section V shows the conclusions of the present work.

2. Power amplifiers for PHIL: State of the art

There are three types of PA used for PHIL applications: synchronous generator, lineal amplifier and switched amplifier. The main advantages and disadvantages are listed in Table **I**. The availability of synchronous generators in laboratories encouraged their use in PHIL tests when this technique was emerging [7]. However, as it can be seen in Table **I**, the use of a synchronous generator for PHIL tests has much lower performance and versatility than the linear and switched amplifier. For this reason, in recent years, synchronous generators have fallen into disuse, being the linear and switched amplifiers the most used equipment for generating real voltage and current in these tests.

Nowadays, there are several commercial PA ready to perform PHIL tests, which are listed in [5]. Also, there are some developments carried out by laboratories, which improves the performance of the present ones. In [8] a modular multiphase multilevel switched amplifier is described, with a maximum current of 100 A. This amplifier is used for testing permanent magnet synchronous machines. In [9] a Cascade H-Bridge (CHB) in parallel with a high power density 2-level converter, is used as a switched amplifier for emulating a Permanent Magnet Synchronous Machine (PMSM). This converter has a voltage bandwidth of 100kHz, but only 2kHz working as a current source. Furthermore, a converter topology based on paralleling several standard half-bridges, coupled between them by a coupled inductor connected in a cyclic cascade, is presented in [10]. This amplifier has been developed for the emulation and testing of photovoltaic inverters. In [11] it is proposed a new concept of voltage amplifier, which is a combination of a slow-switching high-voltage Neutral Point Clamped (NPC) converter with a series-connected low-voltage H-bridge to increase the bandwidth to 65 kHz.

All of them are designed to work as voltage power amplifiers, mainly because an amplifier which can emulate the electric grid, allow to test every system which is connected to it. But these voltage type amplifiers have lower bandwidth when working as a current source. However, no specific high-bandwidth current type power amplifier has been found in the literature. This kind of power amplifiers will be able to emulate all kind of different loads connected to the electric grid, allowing the generation of high frequency current harmonics. This feature will make them very useful to test voltage source as transformers, grid forming converters, batteries, and supercapacitors, among others.

3. Proposed current power amplifier

A. Concept

The buck-boost converter is widely used to manage the output current in several power electronics systems. To expand the converter bandwidth, it is needed to increase the switching frequency of the transistors. But this increment has a thermal limit in the maximum working temperature of the components. Depending on the application, this limit could be in the transistor or in a passive element, such as the filter inductor. Furthermore, it also depends directly on the total current of the converter, reducing the effective frequency as this current increases.

In order to cross this barrier, a massive parallelization of buck-boost converters is proposed, sharing the total current between all branches. In this sense, it is allowed the use of transistors with a lower nominal current, but with a better switching behaviour. Moreover, performing an interleaving operation with an equidistant phase shift between each Pulse Width Modulation (PWM), the total ripple of the output current is reduced by a factor N^2, being N the number of branches. Therefore, the inductance needed in every branch is reduced considerably, which also improves the overall dynamic behaviour of the power amplifier. The schematic of the proposed massively parallel current power amplifier is shown in Fig. 2.

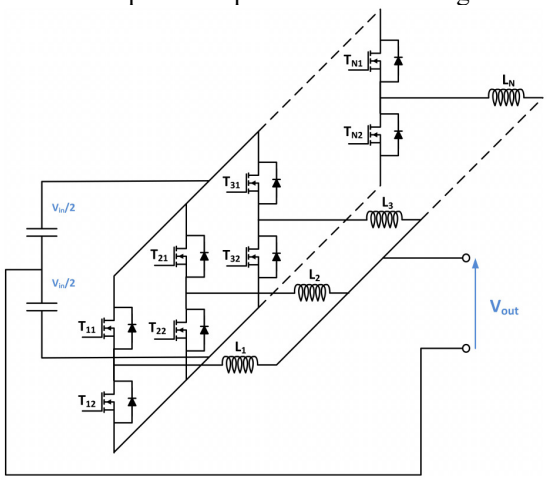

Fig. 2: Schematic of the proposed massive parallel current power amplifier.

It is proposed a Discontinuous Conduction Mode (DCM) in all the current and voltage range, instead of using a Continuous Conduction Mode (CCM). DCM method is characterized because the current starts from 0 A and finish in 0 A in every switching cycle (Fig. 3). This characteristic makes possible to achieve the nominal current in just one switching cycle, increasing the dynamic behaviour of the converter. Also, in DCM there is no right-half plane zero and the system has a transfer function of only one pole, which increase the stability of the overall converter and test. But the ripple magnitude in DCM is much higher than CCM, mainly because the ripple needs to be at least the double of the required output current [12]. However, the increment in the number of branches with interleaved operation reduces this problem.

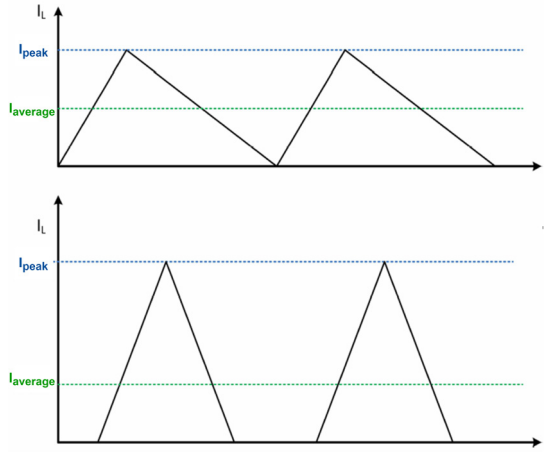

Fig. 3: Typical current waveforms in DCM operation. At least, the peak current must be the double of the average current.

B. *Design*

The electrical specification and main parameters of the proposed amplifier are shown in Table II. It has a nominal voltage of ±325 V and a nominal current of ±60 A divided in 16 branches of ±4 A, achieving a total power of 20.8 kW. A switching frequency of 144 kHz has been selected, which is just below the beginning frequency of the conducted EMI measurement at 150 kHz. The input voltage of the system is 800 Vdc powered by an active front end, which is out of scope of this paper.

Table II: Electrical specification and main parameters of the current power amplifier.

Massive parallel current power amplifier	
Nominal power	20.8 kW
Nominal voltage	±325 V
Nominal current	±64 A
Switching frequency	144 kHz
Bandwidth	> 48kHz
Number branches	16
Maximum average current per branch	±4 A
Maximum peak current per branch	15 A
Current Ripple	3% Inom
DC bus voltage	800 V
Inductance branch	50 µH

To decide the inductance value of every branch, Fig. 4 shows the maximum current ripple at every output voltage and average current. It can be seen that depending on these outputs, the peak to peak current ripple changes. Furthermore, the total effective voltage is reduced as the current increases. This is because at output voltages closed to the DC bus voltage, the control cannot achieve the desired current in a single switching cycle. A decrease in the total current or the switching frequency can increase the voltage range, but with a reduction in the maximum power and in the total bandwidth of the converter at these voltages, respectively.

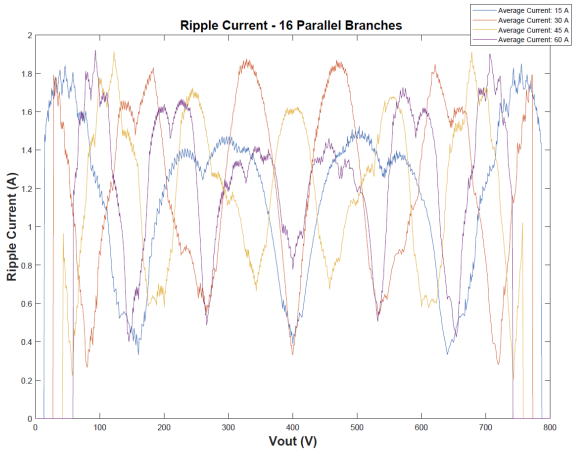

Fig. 4: Output current ripple of the converter at every output voltage and different average output current.

Fig. 5 shows the maximum peak current in every branch depending on the output voltage. This peak current is higher in the central points of the output range, because

the voltage integrated by the coil is significantly larger than the extreme points of operation. It is also mean that in these points, the conduction time of the transistors is reduced. The converter measures the input and output voltages and sets the PWM timing needs for each branch to achieve the desired peak current, which guarantees the output current setpoint sent by the DRTS.

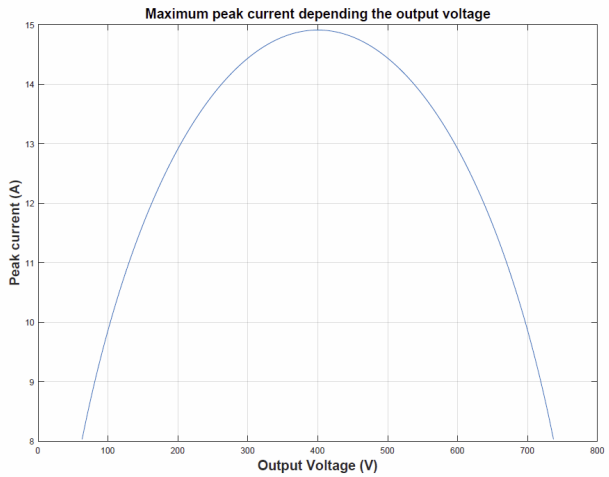

Fig. 5. Maximum peak current in every branch depending on the output voltage.

4. Simulated results

The complete proposed massive parallel current power amplifier has been simulated using Matlab/Simulink®. In order to speed up the simulation, the transistor and the input DC source have been simulated as an ideal one. The first simulation emulates the triangle switching current behaviour of a converter with a switching frequency of 5 kHz. The results can be seen in Fig. 6, where the output current of the converter follows the reference. The output current ripple changes depending on the output voltage and the setpoint current, which have been shown before in Fig. 4.

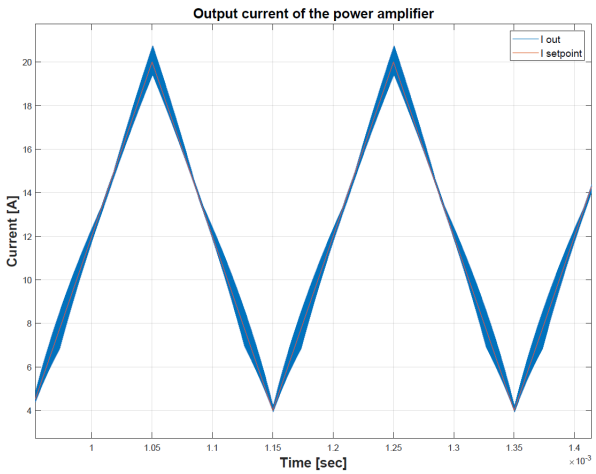

Fig. 6: Emulation of a triangular current switching behaviour of a converter which works at 5 kHz.

To test the bandwidth of the system, a sinusoidal current reference at 20 kHz has been generated. The results are shown in Fig. 7, where it can be seen that the output current of the converter starts to have a small lag between the setpoint and the output. Also, it must be noticed that the maximum output current ripple is not higher than the 3% of the nominal current defined in Table II.

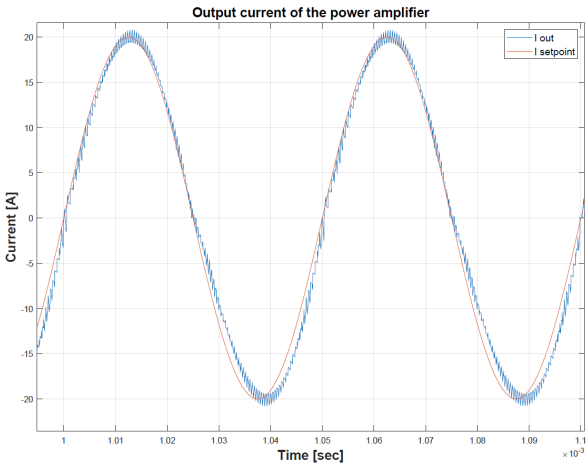

Fig. 7. Generation of a 20kHz sinusoidal current output.

5. Conclusion

PHIL is a very promising test technique for testing the new electrical assets of the smartgrid. In order to guarantee the stability of these tests, the PA bandwidth plays a major role. These amplifiers can be voltage or current type, being the first one the converters most researched. However, current type high bandwidth amplifier is needed to test voltage sources as transformers, grid forming converters or batteries.
In this paper, a new concept of current PA has been exposed. It is based on a massive parallel buck-boost converters, which are switched in an interleaved way. It has been visualized the current response of the amplifier, which makes it suitable for PHIL applications, due to the achieved bandwidth at high power operation.

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