Mains-Synchronized Pulse Density Modulation Strategy Applied to a ZVS Resonant Matrix Inverter

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***Abstract*—Multi-output inverters have become a key enabling technology to increase surface flexibility in domestic induction heating appliances. The most commonly used power converter topologies are based on electromechanical relays in order to multiplex the connected loads and to obtain a proper heat distribution. This solution, which is used in combination with other modulations such as square waveform, relies on the thermal inertia of the pot as it needs long power-averaging periods to reduce the reiteration of the switching noise. However, it presents significant limitation in terms of acoustic noise, reliability and thermal performance. To overcome these limitations, complete solid state inverters, that can be operated at higher frequencies, are proposed. This change in the design paradigm of the pulse density modulation strategies leads to improved thermal control in the pot and better user experience, but at the same time increases challenges due to design constraints imposed by EMC regulations. This paper analyzes the possibilities of a new mains-synchronized pulse density modulation applied to a flexible induction cooktop that uses a multiple-output ZVS resonant inverter topology. The feasibility of the control strategies has been tested by means of a prototype featuring 12 2-kW induction heating loads.**

***Index Terms*—Home appliances, induction heating, modulation strategies, multiple output, pulse density modulation, resonant inverters.**

I. Introduction

INDUCTION heating (IH) has become the market leading heating technology for domestic applications due to its numerous advantages such as fast heating, safe and clean operation, and high efficiency [1]. From this leading market position, further research has been pursued in order to improve the user experience, being one of the most relevant fields the increase of the cooktop surface flexibility [2].

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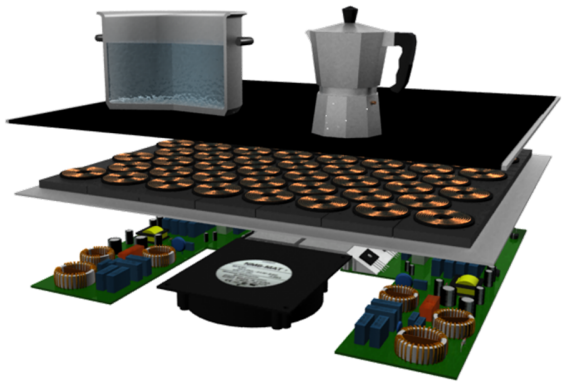


Fig. 1. Flexible surface induction heating cooktop.

Flexible surfaces allow the placement of a wide variety of pots with different sizes and shapes all over the cooktop (Fig. 1). In order to achieve that, additional challenges have to be faced: low mutual coupling inductor design, multi-output topology development, and topology control strategies selection.

The inductor design and selection presents additional constraints related to its size and shape. The size of the inductors is selected in order to power small pots while obtaining a good coupling. The shapes, which allow to tessellate the surface, include circular [3], rectangular [4], hexagonal, and oval [5] inductors. This inductor design, combined with the variability of pots, presents a wide range of different IH loads to be powered. A trade-off is to be achieved between a good power distribution and the number of independent loads to control. Thus, middle-size middle-power inductors are commonly selected [5].

In order to power a low number of different IH loads independently, several flexible and robust topologies are presented in the literature. Those approaches cover from single-inverter single-coil implementations, such as half bridge [6], full bridge [7-9], and single switch [10-12], to ad-hoc designs derived from the half-bridge [4, 13-16] or full-bridge [17-19] topologies, including some hybrid solutions as the interconnection of classic inverters with an auxiliary multiplexing mesh [20].

Most of these topologies require a high number of power devices. To achieve a cost-effective implementation, single-

switch class-e inverters present the lowest device count to obtain an independent power control over all the inductors. However, devices withstand high voltages. To solve this issue, in [21] a new topology with a similar power device count is presented. This multi-output ZVS resonant inverter is derived from the half-bridge topology parallelization, substituting the individual transistors by common ones shared by a row or a column. The independent inductor activation and deactivation is allowed due to the presence of to the series diode on each load.

In order to control the independent power transmission, several control strategies can be used. As a consequence of the characteristics of the topology, modulation strategies typically used in the half-bridge topology can be applied [22]. Additionally, pulse density modulation (PDM) strategies appear as a solution to increase the multi-output ZVS resonant inverter controllability by ensuring independent load activation. These strategies, which increase the degrees of freedom to control the [23-27] while achieving high efficiency for low power requirements [28-30], are usually analyzed with low operation periods and assuming constant voltage.

Despite the PDM strategies being widely used, they present a high dependence on the specific application and usually require high operation periods for home appliances, specifically in the presence of electromechanical relays [31]. For the case of fully solid-state inverters, the acoustic noise is greatly reduced and the period can be decreased, leading to lower heat ripple over the pot and, as a consequence, an improve on the user experience. However, the severity of the restrictions on mains power consumption regulations such as flicker [32], low frequency current harmonics [33], and conducted and radiated emissions [34] increases with a higher multiplexing rate.

This paper proposes a new mains-synchronized PDM strategy algorithm to control a ZVS multi-output matrix topology that powers a flexible surface IH cooktop. This technique allows an independent power control over the pots while operating with a constant mains power consumption by taking advantage of the multiple connected loads. Contrary to most of the literature, where PDM strategies are not analyzed from the EMC point of view, this paper sets the flicker and low frequency harmonic regulations as the basepoint to propose the control algorithm and implement the complete prototype. This diametrically opposed approach, which relies on a complete solid-state implementation and low power pulsation, aims to decrease the PDM period reducing the averaging times and improving the power control and the thermal performance of the cooktop, leading to an improved user experience, being the basis for future domestic IH technology.

The remainder of this paper is organized as follows: Section II presents the power converter topology under study and a single IH-load power control by means of square waveform (SW) modulation. Section III highlights the main constraints for designing a PDM strategy, analyzes the problem, and proposes an algorithm to implement the proposed strategy. Section IV presents the prototype implementation and the experimental setup and Section V summarizes the main experimental results. Finally, Section VI draws the main conclusions of the paper.

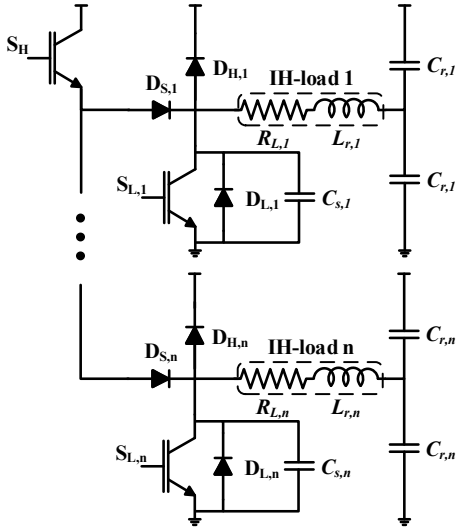


Fig. 2. Multi-output matrix ZVS resonant inverter.

II. Proposed Power Converter Topology

A. Multi-Output ZVS Inverter Topology

The proposed topology under study is a multiple-output matrix ZVS resonant inverter [21]. In order to minimize the activation restrictions of said inverter, a single column structure, with a single high side transistor and several output cells is considered. This solution presents a device count of $n+1$, being n the number of IH loads.

The proposed topology is depicted in Fig. 2. As aforementioned, it shares the high-side transistor, S_H, while each row, and thus each IH load, is presented as a different output cell. These cells are comprised of a series and an antiparallel diode, $D_{S,i}$ and $D_{H,i}$ respectively, a low-side transistor, $S_{L,i}$, with a built-in antiparallel diode, $D_{L,i}$, the IH load, and a split capacitor, $C_{r,i}$, to complete the resonant tank. Each IH load, is modelled as an equivalent series inductance, $L_{r,i}$, and resistance, $R_{L,i}$, whose value is dependent with the pot material, inductor-pot coupling, switching frequency or temperature [35], among others. Additionally, each output cell features a snubber capacitor, $C_{s,i}$, whose purpose is to reduce the turn-off losses of the inverter, in parallel with the low side transistor.

The presence of the series diode in each cell allows the independent activation of each one of the IH loads. Thus, when an IH load is deactivated, the low-side resonant capacitor is charged and the series diode is reverse biased, so no power transmission occurs. However, when the IH load is active, S_L generates a path to discharge the resonant capacitor and, therefore, the series diode is forward biased when S_H is active.

The operation of the active loads of the converter is equivalent to a half-bridge series resonant inverter. The main waveforms and states for a single active inverter are presented in Fig. 3. When the current is positive, it flows through the S_H transistor. When S_H is turned off, the current flows through $C_{s,i}$ (State II) and consecutively through $D_{L,i}$ (State III) when $C_{s,i}$ is

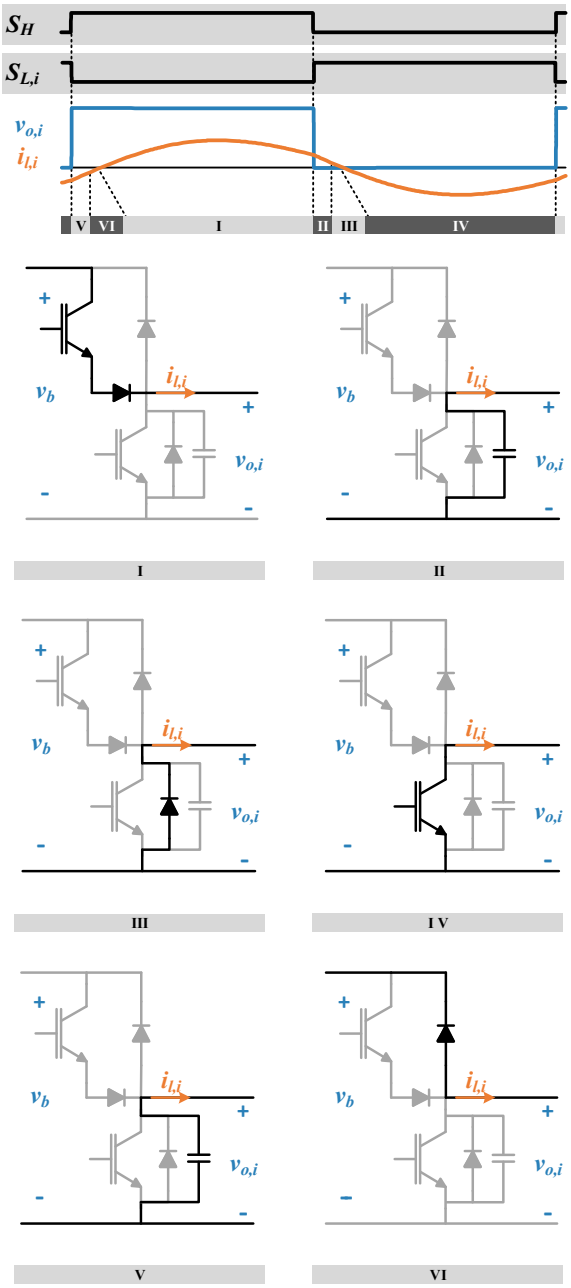


Fig. 3. Inverter main waveforms and circuit configurations for the different states.

charged. As the current becomes negative due to the resonant characteristics, current flows through $S_{L,i}$ (State IV) which presents ZVS turn-on. Once $S_{L,i}$ is deactivated, current flows through $C_{s,i}$ (State V) and $D_{H,i}$ (State VI) until the current becomes positive and S_H is activated with ZVS behavior.

B. Variable Frequency Duty Cycle Control

As a consequence of the similarities with the half-bridge inverter, the variable frequency duty cycle control (VFDC) strategy [36] appears as a suitable option to control the output power. This strategy presents the inverter switching frequency, f_{sw}, and duty cycle, D, as control parameters to choose the power transmitted to each of the IH loads.

Using the Fourier analysis, the applied voltage can be expressed as

$$\begin{aligned} v_o(t) &= \sum_{h=0}^{H}\left(A_h\cos\left(h\omega_s t\right)+B_h\sin\left(h\omega_s t\right)\right) \\ &= V_b D+\sum_{h=1}^{H}\left(A_h\cos\left(h\omega_s t\right)+B_h\sin\left(h\omega_s t\right)\right), \end{aligned} \tag{1}$$

being

$$\begin{aligned} A_h &= \frac{2V_b\sin(h\pi D)\cos(h\pi D)}{h\pi}, \\ B_h &= \frac{2V_b\sin^2(h\pi D)}{h\pi}, \end{aligned} \tag{2}$$

where h is the harmonic number, $\omega_s = 2\pi f_{sw}$ the angular frequency, and V_b the bus voltage.

Thus, the output power of the IH load i, $P_{o,i}$, can be calculated as

$$\begin{aligned} P_{o,i} &= \sum_{h=1}^{H} R_{L,i} I_{o,h,rms,i}^2 = \sum_{h=1}^{H}\frac{R_{L,i}V_{o,h,rms}^2}{R_{L,i}^2+\left(h\omega_s L_{r,i}-\left(1/h\omega_s C_{r,i}\right)\right)^2} \\ &= \sum_{h=1}^{H}\frac{2R_{L,i}V_b^2\sin^2\left(h\pi D\right)/\left(h\pi\right)^2}{R_{L,i}^2+\left(h\omega_s L_{r,i}-\left(1/h\omega_s C_{r,i}\right)\right)^2}, \end{aligned} \tag{3}$$

being $I_{o,h,rms,i}$ the RMS value of the harmonic h of the current through the load i, and $V_{o,h,rms}$ the RMS value of the harmonic h of the voltage applied to the load.

This power is limited due to the usage of the lossless snubber networks, which are designed to operate under ZVS conditions. In order to ensure it, the load current, $i_{o,i}$, has to be enough to charge and discharge the snubber capacitor. This current can be expressed as

$$i_{o,i}(t) = \sum_{h=0}^{H}\left(A_{hI}\cos\left(h\omega_s t\right)+B_{hI}\sin\left(h\omega_s t\right)\right) \tag{4}$$

being

$$\begin{aligned} A_{hI} &= A_h\frac{\left(R_{eq}-\tan(h\pi D)\left(\omega_s hL_{eq}-\frac{1}{\omega_s hC_r}\right)\right)}{R_{eq}^{\ 2}+\left(\omega_s hL_{eq}-\frac{1}{\omega_s hC_r}\right)^2}, \\ B_{hI} &= B_h\frac{\left(R_{eq}+\frac{1}{\tan(h\pi D)}\left(\omega_s hL_{eq}-\frac{1}{\omega_s hC_r}\right)\right)}{R_{eq}^{\ 2}+\left(\omega_s hL_{eq}-\frac{1}{\omega_s hC_r}\right)^2}. \end{aligned} \tag{5}$$

Given the small load times of the snubber capacitance, the current can be assumed constant and equal to the transistor turn off current, i_{off}, calculated in (6).

$$i_{off,H} = i_{o,H}(t)\Big|_{t=\frac{D}{f_{sw}}} = \sum_{i=1}^{n} i_{o,i}(t)\Big|_{t=\frac{D}{f_{sw}}} = \sum_{i=1}^{n}\sum_{h=1}^{H}\left(\frac{2V_b \sin(h\pi D)\cos(h\pi D)}{h\pi\left(R_{L,i}{}^2 + \left(\omega_s h L_{r,i} - \frac{1}{\omega_s h C_r}\right)^2\right)}\left(R_{L,i} + \tan(h\pi D)\left(\omega_s h L_{r,i} - \frac{1}{\omega_s h C_r}\right)\right)\right)$$

$$i_{off,L,i} = i_{o,i}(t)\Big|_{t=0} = \sum_{h=1}^{H}\left(\frac{2V_b \sin(h\pi D)\cos(h\pi D)}{h\pi\left(R_{L,i}{}^2 + \left(\omega_s h L_{r,i} - \frac{1}{\omega_s h C_r}\right)^2\right)}\left(R_{L,i} - \tan(h\pi D)\left(\omega_s h L_{r,i} - \frac{1}{\omega_s h C_r}\right)\right)\right) \quad (6)$$

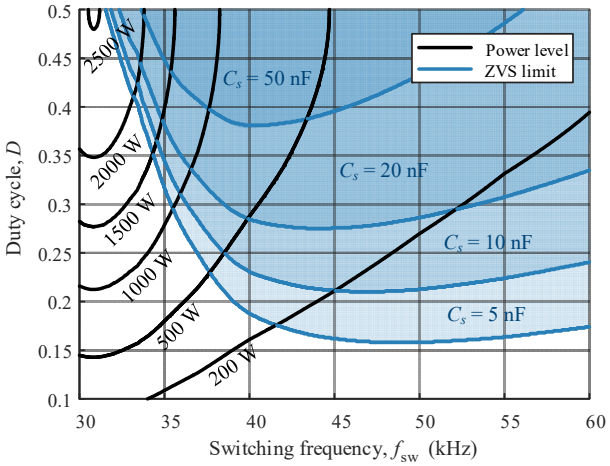


Fig. 4 Power levels and ZVS regions for different combinations of D and f_{sw} and different values of snubber capacitors.

The minimum necessary current can be derived from the IH load equivalent impedance, L_r, and the snubber capacitance, C_s, as

$$i_{off,i} \geq \sqrt{\frac{C_s V_b{}^2}{L_{r,i}}}. \quad (7)$$

In Fig. 4, a plot showing the ZVS regions for different C_s values can be seen. Switching frequency, f_{sw}, allows ZVS operation in the complete range of power. For that reason, duty cycle control will be disregarded in the remaining of this paper, and it will be focused on square waveform modulation.

III. Multi-load Control Algorithm

The proposed matrix topology together with specific IH application considerations imposes critical constraints to the multi-load control algorithm design. These can be divided in three main groups: EMC regulations, adequate inverter operation, and user experience.

A. Operation Characteristics

The most restrictive EMC regulations are the related to power variation among the different mains half cycles, including flicker regulations [32] and low frequency harmonics [33].

Flicker represents the instability of the light emitted by a bulb due to variations in the mains voltage. The fluctuation limits have been tabulated in [32] where maximum voltage drop is related with the frequency of occurrence. This fluctuation limit becomes relevant when fast inductor turn-on and turn-off can be performed so that the user is unaware of the different inductor activation. Thus, a maximum voltage drop, $V_{d,max}$, can be set as the one that does not exceed the limit for any frequency. Taking into account the equivalent mains resistance, R_{eq}, presented in [32], and considering unity power factor for the inverter, the voltage drop can be transformed in power variation, ΔP_{in}, as

$$V_{d,\max} = \frac{\Delta V_{ac,rms}}{V_{ac,rms}} = \frac{\left|\Delta I_{ac,rms} R_{eq}\right|}{V_{ac,rms}} = \frac{\left|\Delta P_{in} R_{eq}\right|}{V_{ac,rms}{}^2} \quad (8)$$

$$\Delta P_{in} = V_{d,\max} \frac{V_{ac,rms}{}^2}{R_{eq}} \quad (9)$$

being $V_{ac,rms}$ the RMS mains voltage and $\Delta I_{ac,rms}$ the RMS mains current variations between a mains half-cycle and the previous one.

Furthermore, pulsating power may affect low frequency harmonic contribution due the current consumption not being consistent for the whole mains cycle. In order to fulfill this requirement, the synchronism of the IH load activation with mains voltage zero crossing is sufficient.

Proper inverter operation increases the cooktop lifetime and is closely related to the inverter design. The most restrictive constraint is a consequence of the single high-side transistor, S_H, and leads to set a common switching frequency for all the active cells to avoid short-circuits. Another design derived constraint is the need of ZVS operation in all the active loads due to the presence of snubber networks.

From the user perspective, load activation and deactivation present additional constraints. The boiling perception is a problem that occurs with classical low-frequency inductor multiplexation, as the thermal inertia in the pot is low. The minimization of the multiplexation period, while maintaining a precise enough resolution, is key to avoid this problem. In addition, even though there is no electromechanical relays in the inverter, acoustic noise can appear as a consequence of the change in forces during the inductor activation [37] and can be reduced synchronizing the activation with the mains zero crossing.

B. Control Problem Analysis

Assuming a common f_{sw} operation for all simultaneously active loads, multi-load control relies only in the different active times. Thus, a mains-synchronized pulse density modulation (PDM) strategy is a suitable solution (Fig. 5). It is

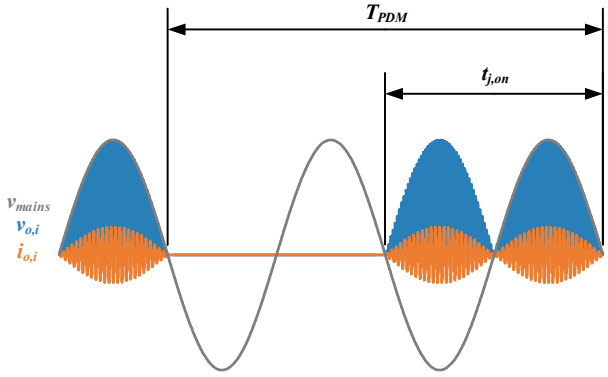


Fig. 5. Mains-synchronized PDM strategy.

important to note that the proposed topology allows, for the first time, to implement such modulation, which was not possible with past topology proposals, as the relay settling time has the same response time as the mains period.

For a set of n IH loads, the number of different combinations of inductor activations, that present at least one active inductor, is $k = 2^n - 1$, as the possible inductor states are *on* and *off*.

Based on that, and assuming a single operation point for each combination of inductor activations, the IH load power can be expressed as a function of $3k$ parameters: the activation vector, $Act_j = (Act_{1,j}, Act_{2,j}, \ldots, Act_{n,j})$, where $Act_{i,j}$ indicates if the IH load i is active, $Act_{i,j} = 1$, or not, $Act_{i,j} = 0$, in the combination j; the combination switching frequency, $f_{sw,j}$, which is selected as the VFDC control parameter while the duty cycle remains symmetrical, $D = 0.5$; and the normalized active time of each combination, $d_j = t_{j,on}/T_{PDM}$. Being the equation system to solve the power distribution

$$\begin{aligned} P_1(f_{sw,1}) \cdot Act_{1,1} \cdot d_1 + \ \ldots \ + P_1(f_{sw,k}) \cdot Act_{1,k} \cdot d_k &= P_{obj,1} \\ \ldots & \\ P_n(f_{sw,1}) \cdot Act_{n,1} \cdot d_1 + \ \ldots \ + P_n(f_{sw,k}) \cdot Act_{n,k} \cdot d_k &= P_{obj,n} \end{aligned} \quad . \quad (10)$$

Moreover, in order to keep at least one inductor active at all times, the extra equation

$$\sum_{j=1}^{k} d_j = 1 \quad (11)$$

is to be added.

These equations form a nonlinear equation system. In order to generate a linear equation system and simplify the resolution, the switching frequencies and activations can be selected in advance.

Frequency selection can be done to minimize power pulsation among the mains half cycles. For that, the sum of the n IH loads output power should be the same for all combinations of active inductors, and f_{sw} is selected to achieve that.

$$\begin{aligned} P_1(f_{sw,1}) \cdot Act_{1,1} + \ \ldots \ + P_n(f_{sw,1}) \cdot Act_{n,1} &= P_{sum} \\ \ldots & \\ P_1(f_{sw,k}) \cdot Act_{1,k} + \ \ldots \ + P_n(f_{sw,k}) \cdot Act_{n,k} &= P_{sum} \end{aligned} \quad (12)$$

where

$$P_{sum} = \sum_{i=1}^{n} P_{obj,i} \quad (13)$$

can be obtained through the sum of the n equations in (10).

Additionally, this approach sets (11) as linearly dependent of the equations in (10) and, as a consequence, the number of parameters necessary to solve the equation system is reduced in one. Thus, an analysis to discard some of the combinations might result in faster equation system solution [38].

In order to avoid power limitations and ensure ZVS operation the minimum number of active inductors in each of the selected combinations should be

$$Act_{1,1} + \ \ldots \ + Act_{n,1} = \left\lceil P_{sum} / P_{design} \right\rceil \quad (14)$$

where P_{design} is the safe-operation maximum power for any material that the inductor is designed.

This activation choice also improves the efficiency by minimizing the number of active loads and thus increasing the power in each of them, moving the switching frequency closer to resonance.

To prove that the equation system is not overdetermined, the minimum number of parameters, k_{min}, can be expressed as the possible combinations of the active loads and has to be greater or equal than the number of total loads. Therefore

$$k_{\min} = \frac{n!}{\left\lceil P_{sum}/P_{design} \right\rceil! \left(n - \left\lceil P_{sum}/P_{design} \right\rceil \right)!} \geq n \quad (15)$$

which is true for $n \geq \left\lceil P_{sum}/P_{design} \right\rceil$.

This analysis works properly for IH loads with similar equivalent resonant tank. However, in the case of resonant capacitor miss-match or, given the flexibility of these systems, loads with different equivalent parameters, IH loads may require different operating frequencies to obtain P_{design}. In that case, some of the selected combinations may present power limitations.

In order to solve this problem, without varying the power between mains half cycles, limited combinations may be replaced by a combination with an extra active inductor to increase overall achievable power. This increase in active loads might lead to higher switching frequencies and therefore lower efficiency.

Additionally, for these cases, *flicker* solutions increase the control degrees of freedom. The maximum power variation among mains half cycles is calculated using (9) so it does not restrict the pulse density modulation period. As a consequence of the difference in power, the time equation is no longer linearly dependent and therefore an extra parameter is necessary.

C. Proposed Control Algorithm

In order to solve the equation system in (10) with the selected combinations, an algorithm that ensures convergence even for underdetermined systems while maintaining $d_j > 0$, and $\sum d_j = 1$ has to be used. With this purpose Gauss-Seidel double randomized algorithm [39] is selected as its operation is not based on the power data manipulation, maintaining its physical sense and, thus, the capability of actualizing said data

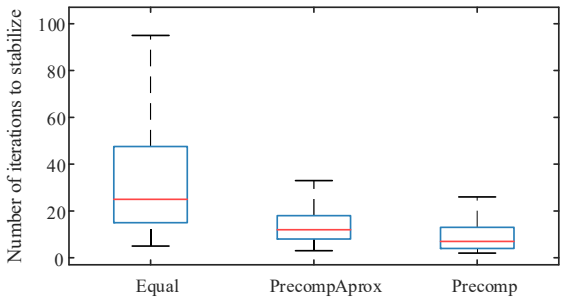


Fig. 6. Comparative chart of the number of iterations with different precomputed $d_{j,0}$ values for an unbalanced power requirement, i.e. $P_{obj,1}>P_{obj,2}$. "Equal" presents the case of $d_{j,0} = 1/\sum j$, "Precomp" present the case of $d_{j,0}$ calculated assuming equal share among the different active inductors, $P_n(f_{sw,i})=P_{sum}/\sum Act_{n,i}$ and precise objective power levels. "PrecompAprox" is calculated with approximated objective power levels.

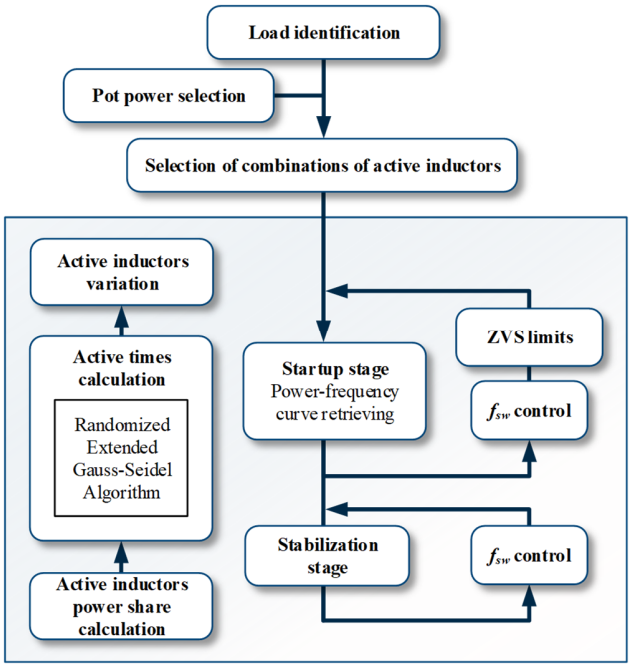


Fig. 7. Algorithm integration block diagram.

during operation due to variations in $L_{r,i}$ and $R_{L,i}$ equivalent parameters.

However, this algorithm presents a high dependence of the initial seed, $d_{j,0}$. As it can be seen in Fig. 6, precomputation of $d_{j,0}$ greatly improves the convergence. From this evaluation it should be noted that precomputations that assume general tendencies in power requirements, even if they are not completely correct, improve greatly the algorithm convergence.

Fig. 7 shows the proposed block diagram implementation for the domestic IH system under study. Load identification is performed to achieve useful control information [40], and the target output power selection is externally done by the user. The selection of the combinations of inductor activations is obtained by applying (15). The main control block is based on the Gauss-Seidel algorithm operating over the normalized transmitted power, which is actualized in each mains half-cycle.

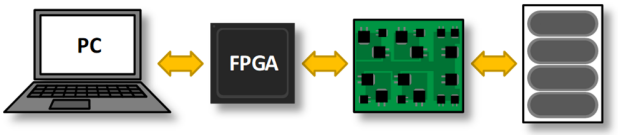
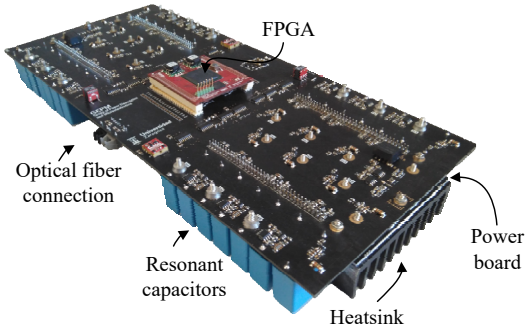
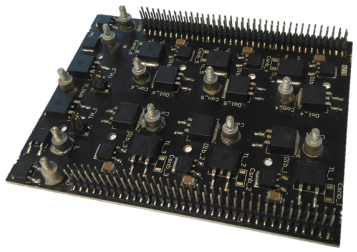


Fig. 8. Experimental test-bench block diagram: Computer, FPGA, prototype board, and inductor system.



(a)



(b)

Fig. 9. Power converter complete prototype. Complete prototype (a) and power board (b)

In order to optimize the operation, a division in the operation core is performed between startup and stabilization. During the startup, the main purpose is to store the complete frequency-power curve data for all active inductors while providing the maximum percentage of the objective power with a proper power share. During the stabilization part, the transmitted power share should present slight variations as a consequence of pot heating. Additionally, once in stabilization, variations in the output power selected by the user can be recalculated.

IV. Prototype Implementation

A complete experimental set-up has been designed and built to test the performance of the proposed power converter and control strategy composed of a PC, an power-converter-embedded FPGA, the matrix ZVS resonant power converter, and up to 12 induction coils (Fig. 8). The selected coils are oval shaped with a maximum rated power of 2000 W. The power converter prototype, shown in Fig. 9, is composed of the following PCBs: two power boards, and the control and measurement board. The first ones include the transistors, diodes, and snubber capacitors and are implemented in insulated metal substrate (IMS) PCB in order to obtain proper cooling (Fig. 9 (b)). The control PCB includes the sensors and ADCs to measure the load voltage and current, the drivers to control all the power transistors, and the connections for the integration of the FPGA.

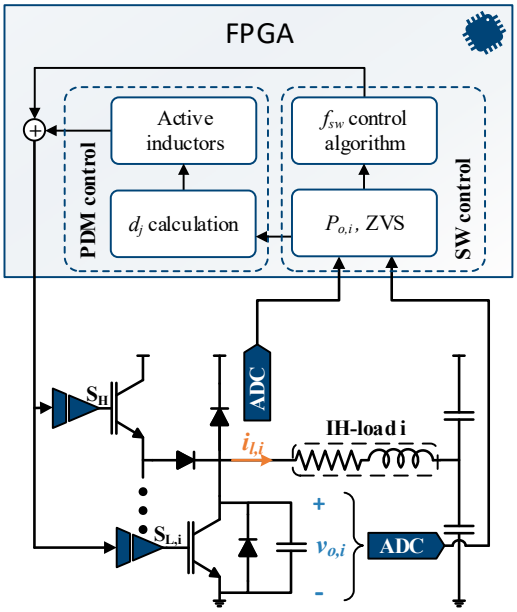


Fig. 10. Implementation block diagram.

The FPGA performs both low-level and high-level operations. The hierarchy of the operations is as follows: the low-level operations are the necessary to read the different ADCs which allow to calculate transmitted power and evaluate ZVS commutation. Based on these results, square waveform parameters are selected for each combination of inductor activations. The high-level operations include a block to save the power-frequency curves for the different inductors and to calculate the on-time, d_j, of the activation. Based on these calculations, the driver signals of the power stage are generated (Fig. 10). The PC is connected to the FPGA by means of optic fiber. It is included to incorporate the user interface that allows the user to set the objective power for the different inductors and performs complementary operations, such as the pot detection system.

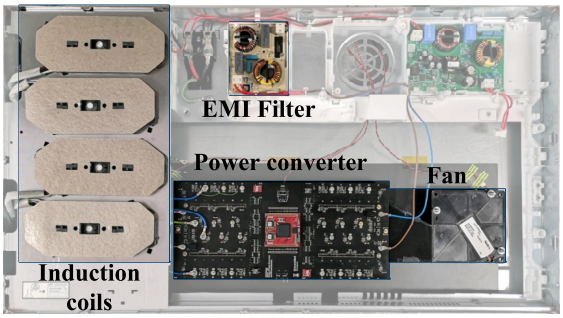
V. Experimental Results

In order to prove the proposed power converter and control strategy, the proposed test-bench has been designed and built (Fig. 11). In the experimental setup layout, two pots are placed in the cooktop covering three inductors in the following configuration: a big one that covers two, and a smaller one that covers a single one (Fig. 11 (a)). This combination has been chosen as it presents unbalanced available power for each of the recipients. However, as the proposed algorithm operates with the different inductors as independent IH loads, paired inductor activation generates a proper solution.

In Fig. 12, the waveforms of the start-up stage of the algorithm can be seen. During the algorithm initial transient, variations in the active times occur due to the differences between the power values used to precompute $d_{0,i}$ and the real power share for each activation solution. For this case, frequency-power curves are retrieved before computing the convergence so that the problems are decoupled and the image is more representative.

In Fig. 13 the waveforms of stationary activations for a balanced power choice , i.e. the power levels are similar for

(a)



(b)

Fig. 11. Experimental setup: (a) general overview and (b) main blocks detail.

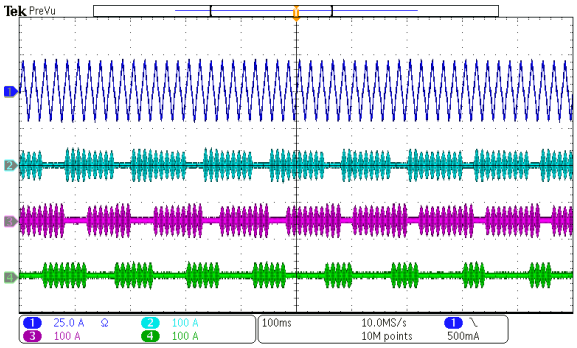


Fig. 12. Initial transient waveforms of the pulse density modulation strategy powering two pots that cover three inductors for an unbalanced objective power. From top to bottom: Input current, i_{ac}, (25 A/div, dark blue), IH load 1 inductor current, $i_{o,1}$, (100 A/div, cyan), IH load 2 inductor current, $i_{o,2}$, (100 A/div, pink), IH load 3 inductor current, $i_{o,3}$, (100 A/div, green). Time axis: 100 ms/div. Starting parameters: $Act_{i,1}$ = (1,1,0), $f_{sw,1}$ = 35.2 kHz, d_1 = 0.33, $Act_{i,2}$ = (0,1,1), $f_{sw,2}$ = 34.0 kHz, d_2 = 0.33, $Act_{i,3}$ = (1,0,1), $f_{sw,3}$ = 34.0 kHz, d_3 = 0.33, and ending parameters: $Act_{i,1}$ = (1,1,0), $f_{sw,1}$ = 35.2 kHz, d_1 = 0.5, $Act_{i,2}$ = (0,1,1), $f_{sw,2}$ = 34.0 kHz, d_2 = 0.25, $Act_{i,3}$ = (1,0,1), $f_{sw,3}$ = 34.0 kHz, d_3 = 0.25.

both pots, and an unbalanced one are presented. The balanced case, presented in Fig. 13 (a), shows similar active times for all IH loads, while the unbalanced case (Fig. 13 (b)), where the big pot power requirement is higher than the one of the smaller pot, presents higher times in the combination of inductor activations that include the inductors under the bigger pot.

Additionally, in Table I, the low frequency harmonic contribution of the usage of the PDM algorithm are shown for the case depicted in Fig. 13 (a). As it can be seen, the period of the strategy generates low frequency harmonics. However, their amplitude is two magnitude orders lower than the fundamental and even harmonics, barely contributing to the

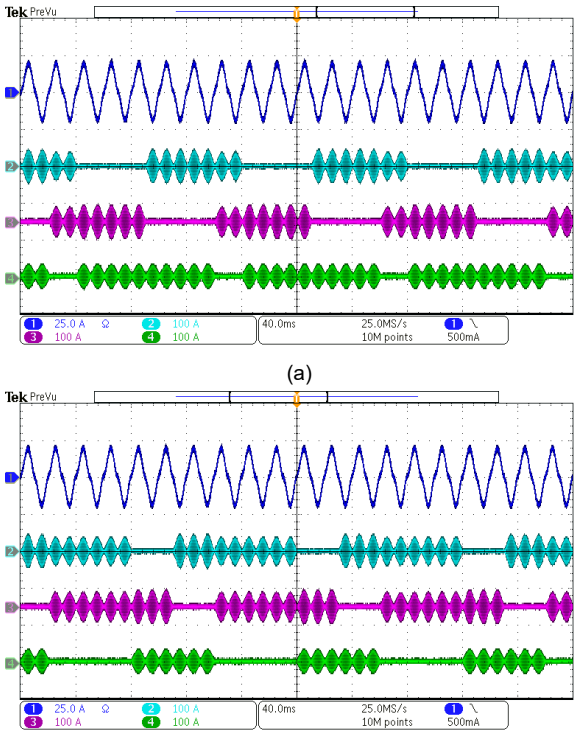


Fig. 13. Stationary stage waveforms of the pulse density modulation strategy powering two pots that cover three inductors. For a balanced objective power (a) and unbalanced objective power (b). In each image, from top to bottom: Input current, i_{ac}, (25 a/div, dark blue), IH load 1 inductor current, $i_{o,1}$, (100 A/div, cyan), IH load 2 inductor current, $i_{o,2}$, (100 A/div, pink), IH load 3 inductor current, $i_{o,3}$, (100 A/div, green). Time axis: 40 ms/div. Parameters for (a): $Act_{i,1} = (1,0,1)$, $f_{sw,1} = 34.0$ kHz, $d_1 = 0.42$, $Act_{i,2} = (1,1,0)$, $f_{sw,2} = 35.2$ kHz, $d_2 = 0.14$, $Act_{i,3} = (0,1,1)$, $f_{sw,3} = 34.0$ kHz, $d_3 = 0.42$, and for (b): $Act_{i,1} = (1,0,1)$, $f_{sw,1} = 34.0$ kHz, $d_1 = 0.25$, $Act_{i,2} = (1,1,0)$, $f_{sw,2} = 35.2$ kHz, $d_2 = 0.5$, $Act_{i,3} = (0,1,1)$, $f_{sw,3} = 34.0$ kHz, $d_3 = 0.25$.

THD of the signal. The same results are shown in Table II, for the case in Fig. 13 (b).

TABLE I
LOW FREQUENCY HARMONIC VALUES FOR THE CASE IN FIG. 13 (A)

Harmonic	Frequency (Hz)	Normalized value (%)
1/6	8.33	0.098
1/3	16.67	0.253
1/2	25	0.370
3/3	33.33	0.321
5/6	41.67	0.730
Fundamental	50	100
2	100	0.042
3	150	8.004
4	200	0.143
5	250	0.948
6	300	0.051
7	350	0.413
8	400	0.073
9	450	0.534
10	500	0.017

TABLE II
LOW FREQUENCY HARMONIC VALUES FOR THE CASE IN FIG. 13 (B)

Harmonic	Frequency (Hz)	Normalized value (%)
1/6	8.33	0.139
1/3	16.67	0.012
1/2	25	0.239
3/3	33.33	0.296
5/6	41.67	0.473
Fundamental	50	100
2	100	0.026
3	150	7.457
4	200	0.128
5	250	0.980
6	300	0.042
7	350	0.383
8	400	0.055
9	450	0.512
10	500	0.016

VI. CONCLUSIONS

In this paper, a matrix ZVS resonant power converter and a mains synchronized pulse modulation strategy has been proposed as a complementary solution to achieve independent power control in flexible surface cooktops. A stable algorithm has been proposed to combine the calculations of the active times of the different IH loads and the switching frequency of each of this activations. The algorithm preselects the active inductors combinations in order to ensure mathematical solution while operating in ZVS region and with improved efficiency.

The proposed algorithm has been implemented in a FPGA and experimentally tested in a prototype with 2000 W of maximum coil rated power, proving the feasibility of the proposed control algorithm under real operating conditions.

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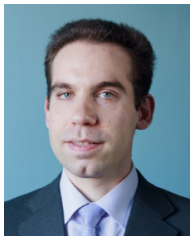

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