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Three-Stage CMOS LDO with Optimized Power and Dynamic Performance for Portable Devices

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Abstract: Low dropout (LDO) regulators are crucial components in power management systems for portable, i.e., battery-powered, devices. However, the design of LDO regulators presents a challenging trade-off between dynamic performance, power consumption, and area efficiency. This paper proposes a novel LDO regulator design that addresses these challenges by employing the reverse nested Miller compensation (RNMC) with current buffers embedded within the own class AB high gain error amplifier (EA) topology, and a time response enhancement circuit (TREC). High-gain (>120 dB) class AB EA renders good regulation performance with enhanced dynamic performance. The proposed compensation scheme improves the gain bandwidth product (GBW) and stability of the regulator, while the TREC reduces overshoot and undershoot during load transients without additional steady-state power consumption. Post-layout simulations confirm the robustness of the proposed 180 nm CMOS design across a wide range of operating conditions, achieving a regulated output voltage of 1.8 V with 100 mV dropout, good load and line regulating performance, and excellent load transient response with reduced undershoot and overshoot at minimum power (I_q = 13.8 µA) and area (314 µm × 150 µm) consumption. The proposed LDO regulator thus offers a compelling compromise between power consumption, area efficiency, and dynamic performance, making it highly suitable for portable applications.

Keywords: low-dropout regulator (LDO); fast transient; load regulation; line regulation; class AB amplifiers

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1. Introduction

Power management, i.e., the conditioning and control of electrical energy, is a critical function in many electronic systems. Generators and batteries deliver voltages and currents that exhibit variations over time and across a broad spectrum of operation conditions. A voltage regulator is employed to convert this fluctuating voltage into a stable, constant, precise, and load-independent output [1]. Traditional low-dropout regulators (LDOs) with large external output capacitors have been preferred for their superior load transient response; however, these configurations consume more area and are not suitable for system-on-chip (SoC) applications. Therefore, output-capacitor-less LDOs (OCL-LDOs) have emerged as the preferred architectures, aligning with the pursuit of efficiency and compactness [2–7].

The design of an OCL-LDO entails a careful balance of multiple performance metrics. One primary specification is the minimization of the quiescent current I_q, as it directly impacts the battery longevity in IoT devices, many of which predominantly operate in ultra-low power or standby modes [8]. From the dynamic performance perspective, it is essential to achieve a high control loop bandwidth (BW) and a high slew rate (SR), factors that directly influence the gate driving capability of the pass transistor and, consequently, transient response characteristics [9–11]. However, enhancing these parameters frequently results in increased power consumption, highlighting an intricate trade-off in LDO design.

Beyond these metrics, design considerations extend to improving the load transient response, reducing the settling/recovery time, and increasing the power supply rejection ratio (PSRR), ensuring the OCL-LDO addresses contemporary electronic demands without compromising on power efficiency.

The classic CMOS LDO regulator topology is shown in Figure 1. It consists of an error amplifier (EA), a PMOS pass transistor located between the unregulated input V_{IN} and the regulated output V_{OUT}, and a resistive negative feedback network R_{F1}–R_{F2}. The EA compares the reference voltage V_{REF} and the proportionally scaled output voltage, sensed through R_{F1}–R_{F2} and defined as $V_{FB} = \frac{R_{F2}}{R_{F1}+R_{F2}} V_{OUT}$. In response to these voltage variations, the EA modulates the gate of the PMOS pass transistor, ensuring the precise current delivery to the load (represented by I_L, C_L), across the entire operational V_{IN} domain. Regulation ensures the stability of the output voltage V_{OUT}, which is given assuming an ideal EA, by:

$$V_{OUT} = \left(1 + \frac{R_{F1}}{R_{F2}}\right) V_{REF} \quad (1)$$

One of the inherent challenges when designing an OCL-LDO is that the dominant pole is typically associated with the gate of the pass transistor, complicating the compensation process since as the output pole is load dependent, the relative position of the poles becomes load-dependent [6]. To address this issue, different compensation techniques have been introduced over the years. Noteworthy strategies include nested Miller compensation [12], reverse nested Miller compensation [13], and pole-zero cancellation, being the case where I_L = 0 (no-load), the most critical in terms of stability [14].

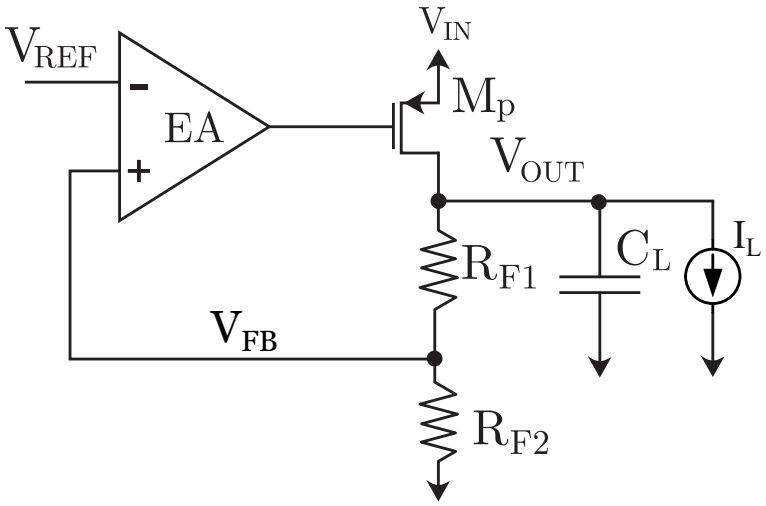

Figure 1. Classic low-dropout regulator.

On the other hand, adaptive biasing and dynamic biasing are strategies commonly used to enhance the dynamic performance of the LDO regulator. In [15], adaptive biasing is combined with two cross-summed transconductance cells to achieve a quiescent current I_q as low as 25 nA and voltage peaks ΔV_{OUT} below 275 mV. However, under maximum load conditions, I_q reaches up to 45 µA. In general, this technique enhances the dynamic response by extending the gain–bandwidth product (GBW) under maximum load conditions [16–18]. Yet, it does not offer substantial benefits in reducing undershoot [19]. Moreover, as mentioned, adaptive biasing implies an increase in the bias current when the load increases, which severely impacts its efficiency.

Conversely, in dynamic biasing, an instantaneous current spike is generated only during transient events, while the bias current is kept to a constant minimum value during steady-state operation. In [20], a dynamic biasing scheme was employed, successfully reducing the settling time to 0.28 µs with a quiescent current of 13.9 µA; however, it exhibited an undershoot of 480 mV. In [21], both dynamic and adaptive biasing techniques

were employed, resulting in a ΔV_{OUT} of 231 mV and a settling time of 0.1 µs with a low quiescent current of 0.1 µA. In spite of these advantages, the design requires a minimum load current of 100 nA, and its maximum load capability is limited to 10 mA.

In this paper, a fully integrated low-dropout (LDO) regulator with a fast transient response and low power consumption is presented. To achieve enhanced regulation performance, a two-stage op-amp operating in class AB was employed as EA. The op-amp is therefore able to deliver currents exceeding its bias current, thereby improving the dynamic response. Furthermore, a dynamic time response enhancement circuit (TREC) has been integrated, which effectively mitigates voltage overshoot and undershoot without significantly impacting consumption. The paper is organized as follows: Section 2 details the proposed LDO regulator design, compensation strategy, and the time–response improvement block. Section 3 discusses post-layout simulations, while conclusions are drawn in Section 4.

2. Proposed LDO Regulator

The complete schematic of the proposed LDO regulator is shown in Figure 2. Given an external bandgap reference $V_{\mathrm{REF}} = 1.2$ V, to achieve an output voltage $V_{\mathrm{OUT}} = 1.8$ V, according to Equation (1), R_{F2} must be twice the value of R_{F1}. The resistance values are set to $R_{F1} = 200$ kΩ and $R_{F2} = 400$ kΩ, as a trade-off between power consumption and moderate resistance values. This choice results in a static current consumption of the output M_P-R_{F1}-R_{F2} branch $I_{qFB} = 3$ µA. To reduce area, these feedback resistors are implemented, as shown in Figure 2, using three identical diode-connected PMOS transistors with dimensions $W = 1.6$ µm and L = 500 nm. PMOS transistors are used instead of their NMOS counterparts since the integrating technology is P-substrate N-well; therefore, for PMOS transistors $V_{SB} = 0$, ensuring that the three active diode resistances are identical.

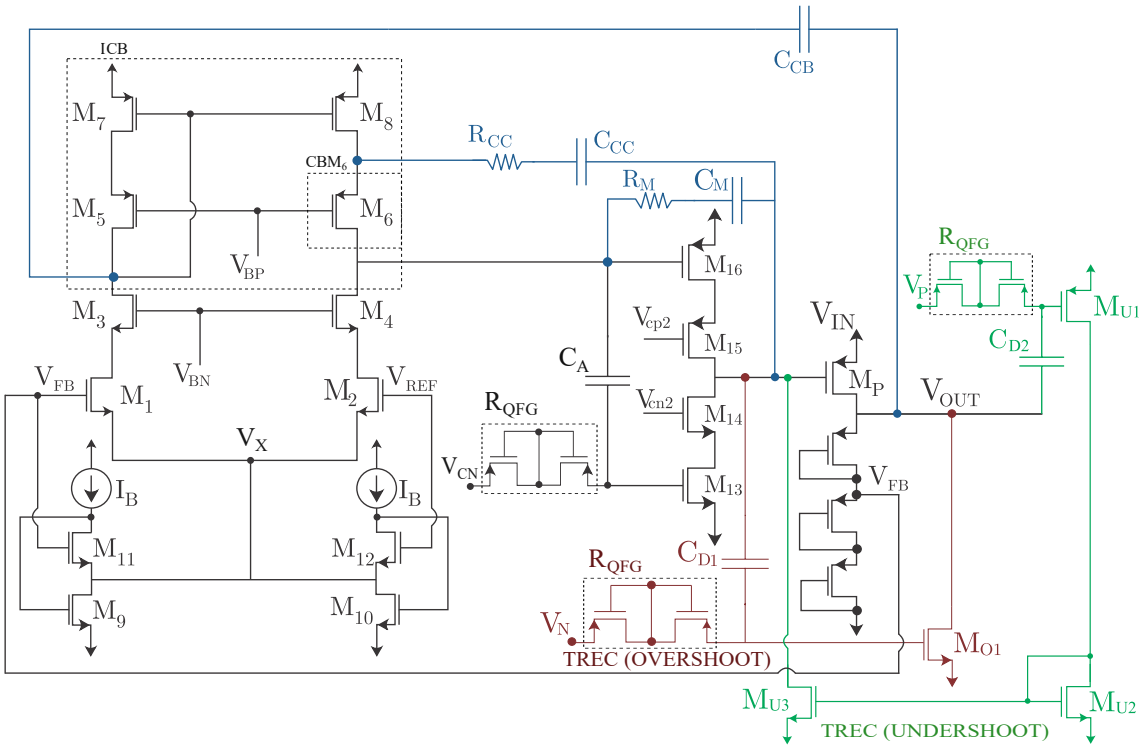

Figure 2. Schematic of the proposed low-dropout regulator.

The dimensions of the PMOS pass device M_P were set to L = 0.34 µm (minimum length for a 3.3 V MOSFET) and W = 4.5 mm to ensure it can handle load currents up to 50 mA, while preserving a dropout voltage of $V_{do} = 100$ mV. The dropout voltage is the smallest potential V_{IN}–V_{OUT} across the pass component, which must be low in order to maximize the regulation range and optimize the LDO efficiency. This is the largest transistor in the

design, resulting a parasitic gate capacitance of C_{gp} = 12 pF for a load current $I_L = 0$ and C_{gp} = 20 pF for $I_L = 50$ mA, which will be the load capacitance considered in the design of the EA.

The EA must operate properly over all the input range (V_{IN} = 1.9 V–3 V) with a load capacitance $C_{L,EA} = C_{gp}$. As already mentioned, a 2-stage class AB EA is selected to provide a good trade-off between regulation and dynamic performance while keeping the quiescent current low to reduce power consumption. As detailed in Figure 2, the first stage is a low-power telescopic class AB OTA [22]. Transistors M_9 to M_{12} and the current sources I_B establish the voltage at the source node of the input pair to $V_X = \{\max(V_{FB}, V_{\mathrm{REF}}) - V_B\}$, where V_B is the DC gate-to-source voltage of M_{11}, M_{12}. This configuration ensures that both M_1 and M_2 fully experience the input signal swing, avoiding the current limitation established by I_B in constant biasing configurations, and therefore resulting in class AB operation. The EA second stage is a cascode common-source configuration where the class AB operation is achieved by means of the quasi-floating gate (QFG) technique [23]. Under static conditions, the gate voltage of M_{13} is set to V_{CN} via the resistor R_{QFG}, which is a large value resistor in the order of GΩ implemented with two reverse-biased diode-connected PMOS transistors in series. In this way, the static current through the second stage is established. Under dynamic conditions, the voltage variations at the gate of M_{16} are conveyed to the gate of M_{13} through a capacitor C_A = 0.8 pF.

Transistor sizes of the EA are shown in Table 1. The bias current I_B of the first stage is set to 0.5 µA, and the bias current set by M_{13} through the second stage is 4 µA. The cascode bias voltages V_{BN} and V_{BP} in the first stage are generated on the chip, as shown in Figure 3. Note that to properly bias M_3 and M_4, V_{BN} must satisfy the following condition: $V_{BN} = V_{gs3,4} + V_{ov1,2} + V_X$. In the same way, to properly bias M_5 and M_6, the following condition must be satisfied: $V_{BP} = V_{DD} - |V_{ov7,8}| - |V_{gs5,6}|$. The values were set $V_{BN} = 1.2$ V and $V_{BP} = V_{DD} - 1$ V. Transistor sizes of this biasing network are also included in Table 1.

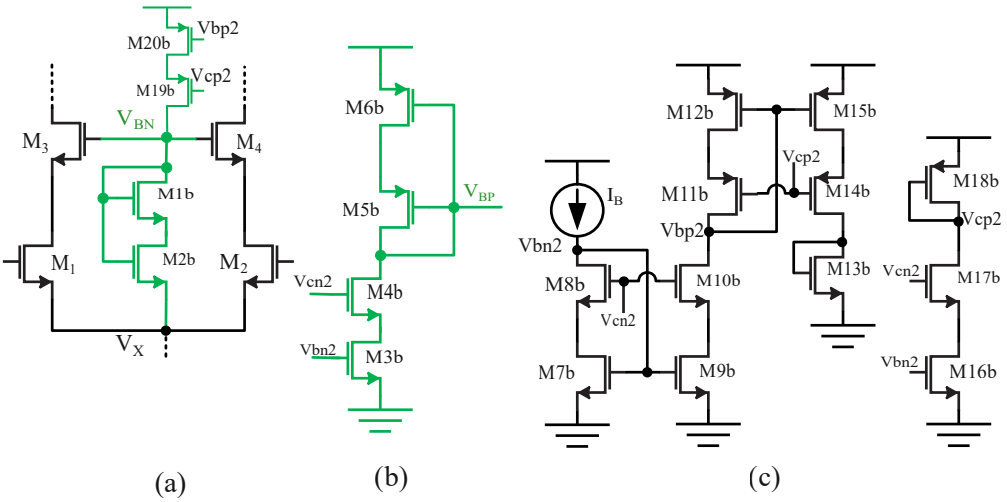

Figure 3. Biasing network to generate (**a**) V_{BN}, (**b**) V_{BP}, and (**c**) general polarization.

The EA showcases an open loop gain exceeding 120 dB, a GBW of 798 kHz, and a phase margin (PM) of 60° at $CL = 20$ pF, that is, for the maximum parasitic gate capacitance of M_P over the whole V_{IN} variation range, with 21 µW power consumption.

Table 1. Transistor sizes in the error amplifier.

	W(μm)/L(μm)
M_1, M_2	2.5/0.4
M_3, M_4	2.5/0.5
M_5, M_6, M_7, M_8	4/0.5
M_9, M_{10}, M_{11}, M_{12}	1.3/0.5
M_{13}, M_{14}	14/0.5
M_{15}, M_{16}	20/0.5
M_{1b}, M_{2b}, M_{3b}, M_{4b}	0.7/0.5
M_{5b}, M_{6b}, M_{18b}	1
M_{7b}, M_{8b}, M_{9b}, M_{10b}, M_{17b}	2.8/0.5
M_{11b}, M_{12b}, M_{14b}, M_{15b}	8.4/0.5
M_{13b}	0.35/0.5
M_{16b}, M_{19b}, M_{20b}	2.1/0.5

2.1. Compensation Strategy

Compared to the nested Miller compensation (NMC) scheme, the reverse nested Miller compensation (RNMC) utilizes an inner compensation capacitor that does not load the output and is therefore suitable for heavy capacitive loads [13,24]. Additionally, the incorporation of current buffers (CBs) results in the so-called CB-RNMC, where both the second and third stages of the LDO can be inverted by adequately choosing the polarity of the CBs [13]. This is the basis of the adopted three-stage compensation strategy, which relies on a second (cascode common-source) and a third (common-source M_P pass transistor) stage, which are both inverting and take advantage of the EA configuration by using the current buffers embedded in the first stage to accomplish the compensation scheme. In particular, M_5–M_8 are used as inverting CBs (ICBs), and M_6 as a common-gate non-inverting CB (CBM_6), both marked in Figure 2. The use of additional blocks is thus avoided and a more compact design is achieved, resulting in reduced power consumption while enhancing the dynamic response. Without compensation, the described LDO shows a PM = 10° at I_L = 50 mA, and it is unstable at IL = 0.

The small-signal model of the proposed LDO regulator is presented in Figure 4, where the blue color indicates that the ICB and CBM_6 are actually embedded in the first stage G_{m1}. From Figures 2 and 4, the CB-RNM compensation strategy utilizes two feedback loops. The outer C_{CB} – ICB loop ties the LDO output to the first stage of the EA. The second loop comprises C_{CC} in series with the common-gate transistor M_6 acting as CB. Resistance R_{CC} is introduced to better control the position of the zero $1/R_{CC}C_{CC}$. Additionally, R_M and C_M enhance the phase margin by mitigating high-frequency poles.

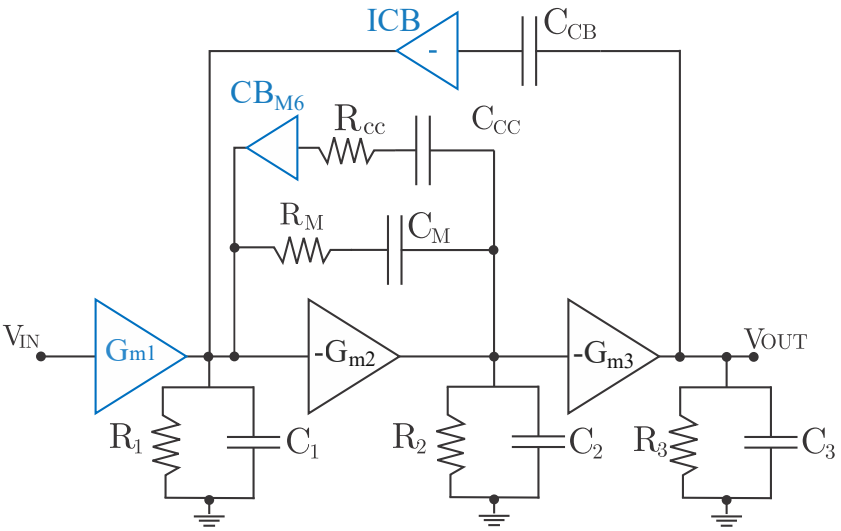

Figure 4. Small signal model of the proposed low dropout regulator.

Herein, Gm_i, C_i, and R_i represent the transconductance, parasitic capacitance, and output resistance of each stage, respectively. The DC gain and gain-bandwidth product are defined as:

$$A_{DC} = \beta G_{m1} R_1 G_{m2} R_2 G_{m3} R_3 \tag{2}$$

where β is the feedback factor and:

$$GBW = \frac{G_{m1}}{C_{CB}} \tag{3}$$

The Miller capacitor C_{CB} is used to split the dominant pole and the first non-dominant pole. Consequently, the dominant pole can be approximated by:

$$\omega_{p1} \approx \frac{-1}{R_1 C_{CB} G_{m2} R_2 G_{m3} R_3} \tag{4}$$

Whereas the first non-dominant pole is given by:

$$\omega_{p2} \approx \frac{-1}{R_{cc} C_{cc} + \frac{C_{cc}}{g_{m6}} + \frac{C_{cc} C_3}{C_{CB} G_{m3}}} \tag{5}$$

Note that Miller capacitances generate a feedforward path, introducing right-half-plane (RHP) zeros. However, the integration of current buffers (CBs) mitigates the associated stability issues by moving these zeros to the left-half-plane (LHP), thereby enhancing PM and bandwidth [13]. In the schematic depicted in Figure 2, the ICB–C_{CB}, results in a dominant first zero given by:

$$z_1 = \frac{g_{mICB}}{C_{CB}} \tag{6}$$

where $1/g_{\mathrm{mICB}}$ is the input equivalent resistance of the current buffer formed by M_5–M_8. The second zero is set by the R_{CC}–C_{CC} pair in conjunction with M_6. When R_{CC} is substantially higher than $1/g_{m6}$, the zero is defined by:

$$z_2 = \frac{1}{R_{CC} C_{CC}} \tag{7}$$

The second zero and the first non-dominant pole approximately cancel each other, so the phase margin is significantly increased and the regulator behaves like a single-pole system.

The frequency response of the LDO regulator is depicted in Figure 5. The frequency analysis for load currents spanning from $I_L = 0$ to $I_L = 50$ mA shows a DC gain ranging from 127 to 134 dB and a PM from 57° to 103° for V_{IN} = 3 V, and a gain ranging from 101 to 134 dB and a PM from 53° to 106°for V_{IN} = 1.9 V. A subsequent phase margin analysis for several load capacitances is presented in Figure 6. A consistent phase margin above 53° for all C_L values ensures the stability of the regulator.

2.2. Enhancing the Dynamic Response

To further enhance the dynamic performance without compromising power efficiency, a simple time response enhancement circuit (TREC) is incorporated. The circuit uses a dynamic path only active during transients and minimizes the need for additional components. Figure 2 depicts the TREC circuitry for both overshoot and undershoot enhancement. The TREC that activates when an undershoot occurs consists of a PMOS QFG transistor M_{U1} and an NMOS current mirror M_{U2}–M_{U3}. The gate voltage of M_{U1} is set to V_p via the resistor R_{QFG}, so that in steady state M_{U1} remains in the cut-off region because ($V_{SG,U1} = V_{DD} - V_P = 0.5$ V $< |V_{THP,U1}|$). Meanwhile, when a sudden load current increase causes V_{OUT} to decrease, this undershoot is coupled to the gate of M_{U1} by C_{D2} = 0.8 pF, thus turning M_{U1} on. The resulting current is mirrored by M_{U2}–M_{U3} (3 µm/0.34 µm, 6 µm/0.34 µm) and injected to the gate of M_P, which helps restore the

output voltage and mitigates the undershoot. Once V_{OUT} stabilizes to its nominal value, M_{U1}–M_{U3} revert to the off state.

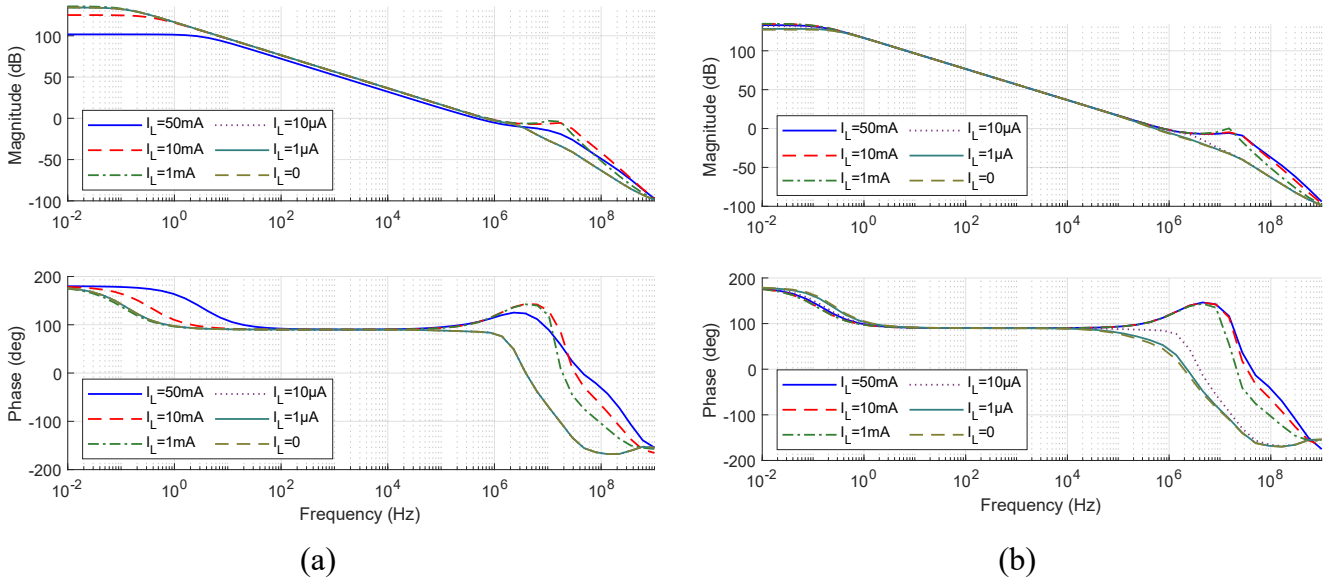

Figure 5. Open-loop frequency response for the proposed low dropout regulator under different load currents (0–50 mA), (**a**) V_{IN} = 1.9 V, (**b**) V_{IN} = 3 V.

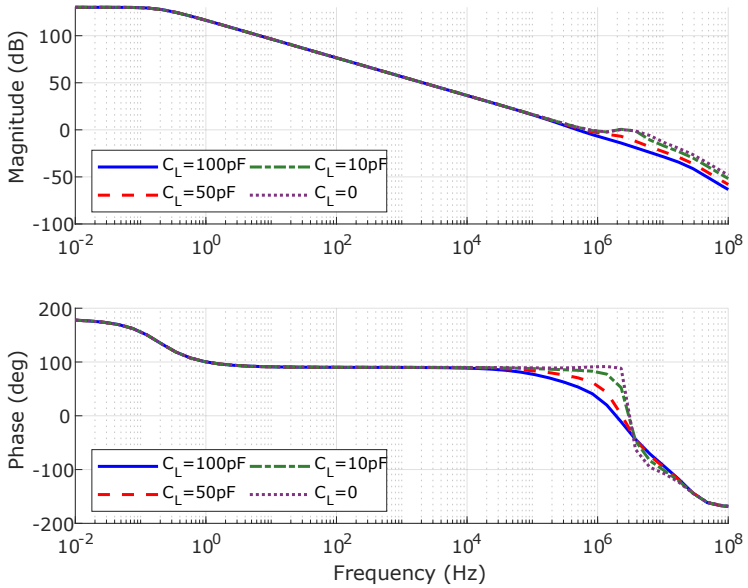

Figure 6. Open-loop frequency response for the proposed low dropout regulator under different load capacitances (0–100 pF) with I_L = 0.

As for the portion of the TREC that activates when an overshoot occurs, it consists of a single QFG NMOS transistor M_{O1}, which remains off during steady state. The DC gate voltage is set to $V_N = 0.5\ \text{V} < V_{THN}$ through the large value resistance R_{QFG}. A sudden reduction in the load current produces an increase in the gate voltage of the pass transistor, which is coupled by C_{D1} to the gate of M_{O1}, thus turning it on and establishing a discharge pathway at the output node. Once V_{OUT} reverts to its nominal value, M_{O1} deactivates. Note that, for test purposes, the bias voltages V_N and V_P are externally generated.

In Figure 7, the TREC behavior is evaluated under full load current transitions from 0–50 mA with 1 µs rise/fall time. At V_{IN} = 1.9 V, without the TREC, a load change induces an undershoot of 315 mV and an overshoot of 120 mV. The incorporation of the TREC

modulates these transients and reduces the undershoot to 182 mV and the overshoot to 106 mV. Furthermore, the overshoot settling time is reduced from 11 to 2 µs.

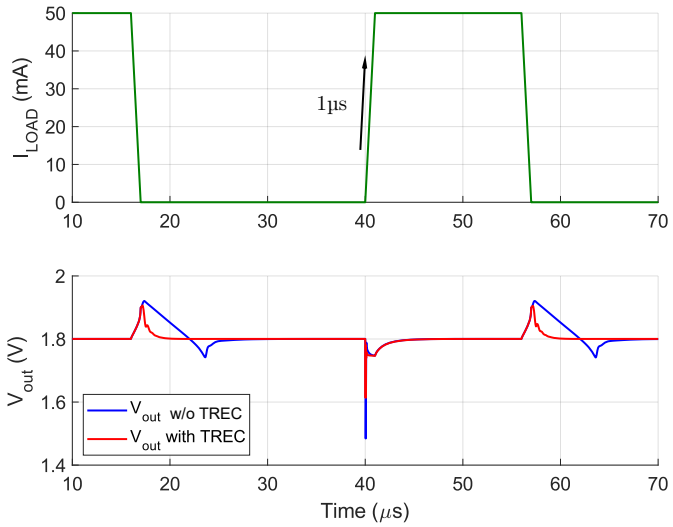

Figure 7. Post-layout load transient response for load currents from 0 to 50 mA and V_{IN} = 1.9 V (worst case).

3. Post-Layout Results

The proposed LDO regulator was designed in the UMC 0.18 µm CMOS process with 3.3 V nominal MOS transistors (V_{THP} = −0.72 V, V_{THN} = 0.59 V) to deliver an output regulated voltage V_{OUT} = 1.8 V for V_{IN} = 1.9 V–3 V and load currents 0–50 mA, with C_L up to 100 pF. The V_{REF} is externally set to 1.2 V, and the total quiescent current is 13.8 µA. The layout is shown in Figure 8, with a total area consumption of 314 µm × 150 µm. The main post-layout simulation results reported next were obtained using Spectre with a BSIM3v3 level 53 transistor model.

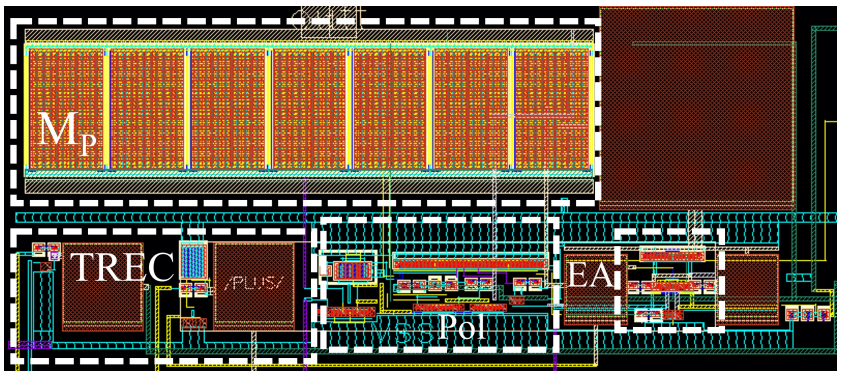

Figure 8. Layout of the proposed low dropout regulator.

3.1. Static Performance

Figure 9 shows the DC characteristic V_{IN} (V_{DD}) − V_{OUT} for different load currents and over different process corners: FF, SS, FnSp, and SnFp. The regulator presents a stable 1.8 V output voltage with a 100 mV dropout voltage. Figure 10 shows the line regulation (LNR = $\Delta V_{OUT}/\Delta V_{IN}$) over all of the input voltage range (from 1.9 V to 3.0V) at different I_L values and different process corners. Notably, the LNR is 27 µV/V (TT) and 30 µV/V (SS) at I_L = 50 mA, which corresponds to the worst case.

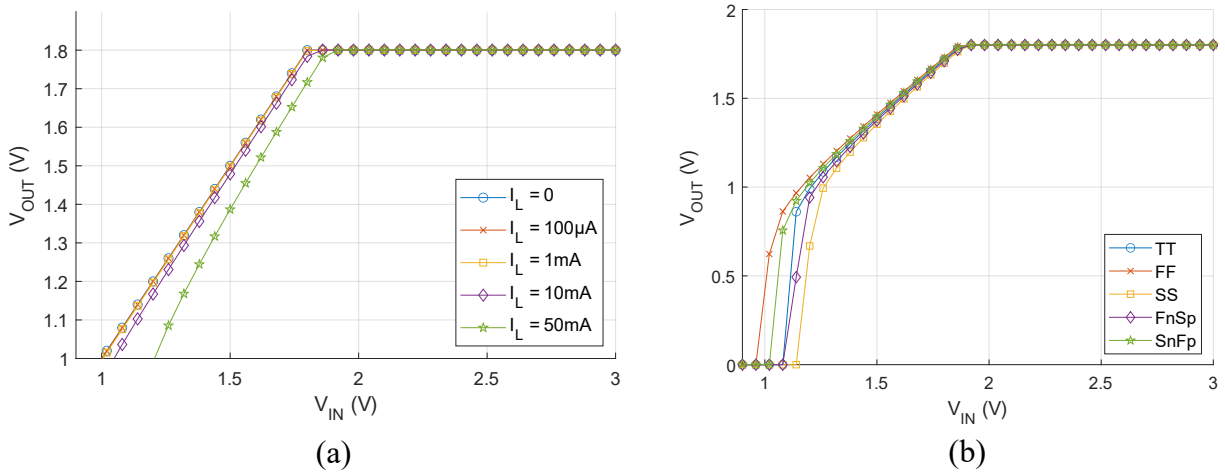

Figure 9. DC characteristic of the proposed LDO regulator (**a**) at different I_L values and (**b**) at corners with I_L = 50 mA.

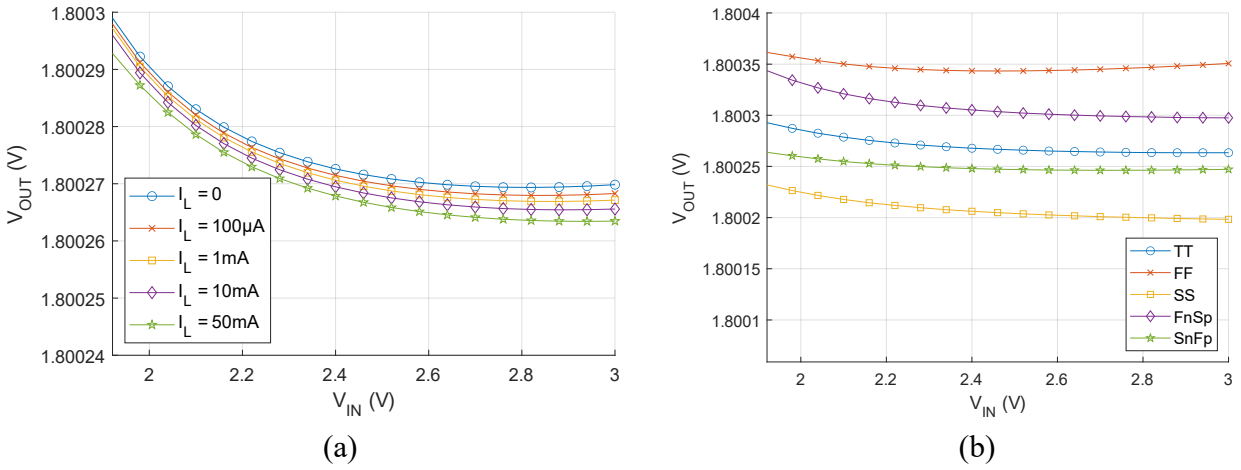

Figure 10. Line regulation (**a**) at different I_L values and (**b**) at corners with I_L = 50 mA.

Figure 11 depicts the load regulation performance (LDR = $\Delta V_{OUT}/\Delta I_L$) over the whole V_{IN} range and for different process corners with V_{IN} = 1.9 V (worst case scenario). For a load current range of 0–50 mA, the LDR is 1.4 µV/mA in the nominal case (TT) and 4 µV/mA in the worst case (SS).

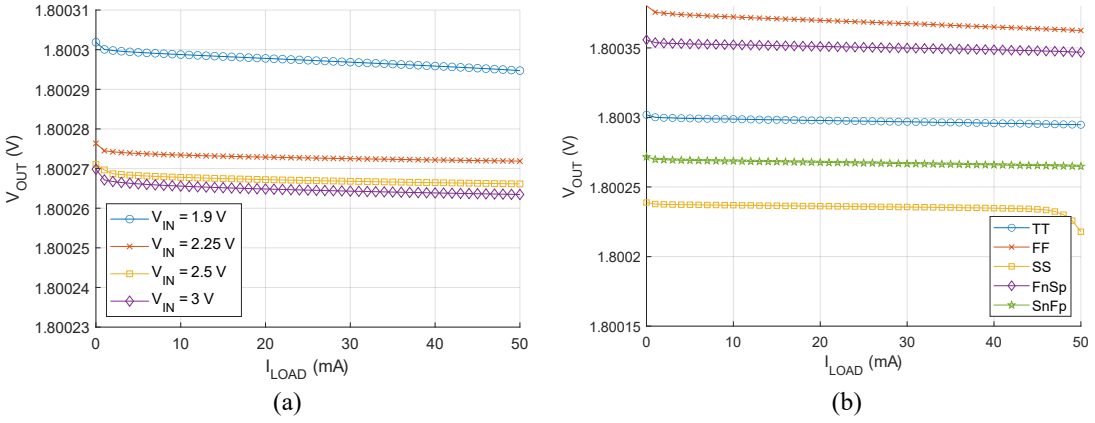

Figure 11. Load regulation (**a**) for different values of V_{IN} and (**b**) at corners with V_{IN} = 1.9 V.

3.2. Dynamic Performance

Figure 12 presents the response of the proposed LDO for a full load transient 50 mA–0–50 mA, with 1 µs edge time, at V_{IN} = 1.9 V and C_L = 100 pF. Thanks to the TREC block, with minimum current and area penalty, the overshoot and undershoot remain below 106 mV and 182 mV, respectively, with 2.03 µs recovery time measured at 99% of the final output voltage value. Figure 13 shows the response of the LDO regulator when the edge time is reduced to 100 ns. In this case, the maximum overshoot and undershoot were 97 mV and 222 mV, respectively, and the recovery time at 99% of the final output voltage is below 1.64 µs.

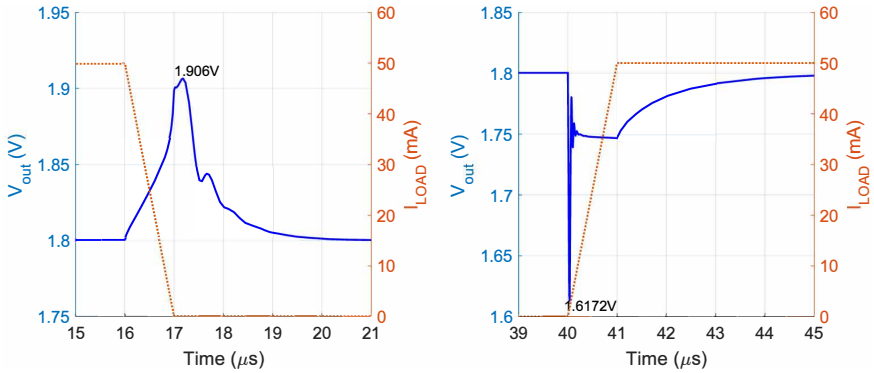

Figure 12. Load transient response (overshoot and undershoot) for load currents from 0 to 50 mA, T_{RISE} = 1 µs, and V_{IN} = 1.9 V.

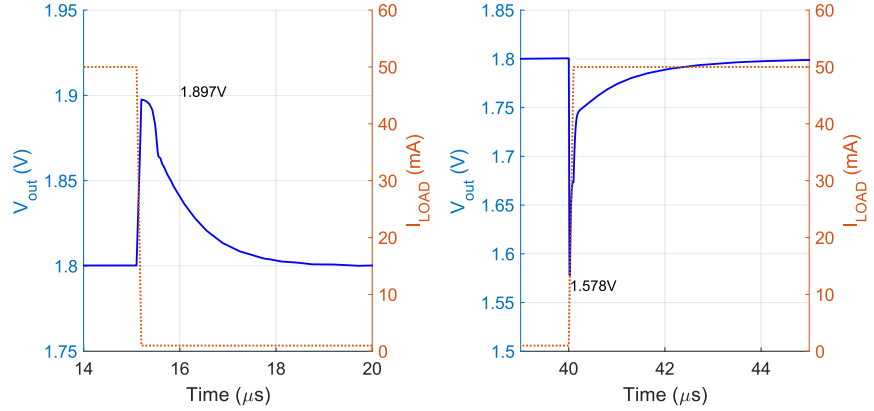

Figure 13. Load transient response (overshoot and undershoot) for load currents from 0 to 50 mA, T_{RISE} = 100 ns, and V_{IN} = 1.9 V.

3.3. Comparison

Table 2 summarizes and compares the performance of the proposed LDO regulator with other recent topologies with similar specifications. To better evaluate and compare them, several figures of merit (FOMs) were adopted. The first FOM considers the impact of the edge time, T_{edge}, a parameter that affects the regulator's response time [8]. To do so, an edge time factor, K, is used, defined by the equation:

$$K = \frac{T_{edge} \text{ used in measurement}}{\text{smallest } T_{edge} \text{ among the design comparison}} \quad (8)$$

FOM_1 is then defined as:

$$FOM_1 = K\left(\frac{\Delta V_{OUT} I_Q}{I_L}\right) \quad (9)$$

Table 2. Performance summary and comparison

	[2]'22 (Exp)	[16]'18 (Exp)	[19]'23 (Post)	[7]'18 (Sim)	This Work (Post)
Technology (nm)	180	180	180	350	180
V_{IN} (V)	1.2–1.4	1.2–1.8	1.8–2.2	3.3–3.5	1.9–3
V_{OUT} (V)	1–2.2	0.8–1.6	1.6	2.8	1.8
V_{DO} (mV)	200	200	200	500	100
I_q (µA)	14	10.2	2	50	13.8
I_L (mA)	0–100	1–100	2–100 µA	50	0–50
C_{LOAD} (pF)	0–1000	0–100	100	10	0–100
LNR (mV/V)	0.5	10	7.72	23.4	0.027
LDR (mV/mA)	0.025	0.081	0.068	0.023	0.0014
ΔV_{OUT}@T_{EDGE} (mV@µs)	252 @ 1	200 @ 0.1	466 @ 0.5	800 @ 1	182 @ 1 222 @ 0.1
Tsettle T_s (µs)	7.3	0.22	≈18	2	2.03
PSRR (dB@f(Hz))	−50 @ 1k	-	-	−45 @ 100k	−52 @ 1k
FOM_1 (mV)	0.353	0.02	0.046	0.8	0.06
FOM_2 (ns)	1.02	2.22	0.72	2	0.55
FOM_3 (fs)	1.75	8.26	1.05	5.38	0.001

The second *FOM* evaluates the dynamic performance taking into account a correction factor, γ:

$$FOM_2 = \left(\frac{T_s I_Q}{I_L}\right)\gamma \tag{10}$$

where γ is given by:

$$\gamma = \frac{I_Q + I_{L,MIN}}{I_Q} \tag{11}$$

and $I_{L,MIN}$ represents the minimum load current of the proposed regulator, which is related to its stability. Thus, γ accounts for the regulator's stability under minimum operating current conditions.

Finally, the third *FOM* [25] considers the power efficiency, as well as the regulation performance (LNR and LDR), and is defined as:

$$FOM_3 = \frac{C_{LOAD} * LNR * LDR * I_Q * 1000}{I_L} \tag{12}$$

The factor 1000 is included to adjust the units (fs). Note that, for all the considered FOMs, the lower the value, the better the performance they showcase.

From the results in Table 2, it is clear that the proposed LDO design features a broader input voltage range (V_{IN} = 1.9–3 V) and a lower dropout voltage (V_{DO} = 100 mV) making it suitable for a variety of regulation applications.

Additionally, the proposed LDO regulator excels in FOM_2 and FOM_3, which are 0.55 ns and 0.001 fs, respectively, the lowest among the compared works. These values indicate an excellent trade-off between power efficiency (I_q = 13.8 µA), regulation represented by the low values of LNR (0.027 mV/V) and LDR (0.0014 mV/mA), and dynamic performance, highlighted by a short settling time (T_s = 2.03 µs). Furthermore, in contrast to some state-of-the-art regulators, the proposed LDO is capable of operating across the entire range of load currents (I_L = 0–50 mA), indicating an overall enhanced trade-off between power efficiency, dynamic response, and stability across the entire range of loads.

4. Conclusions

In this paper, a novel fully integrated LDO regulator design with improved regulation, dynamic response, and power efficiency trade-off is proposed. The design uses a reverse nested Miller compensation (RNMC) strategy with current buffers that are embedded in the two-stage error amplifier and a time response enhancement circuit which reduces undershoot/overshoot and settling time for full load current changes. The error amplifier

consists of a telescopic OTA and a common source cascode stage, which ensures high gain over the entire input voltage range, thus providing enhanced regulation performance. Furthermore, class AB operation enhances dynamic performance without introducing additional active blocks, leading to a compact and power-efficient design. Post-layout simulation results confirm the LDO's ability to deliver a consistent output voltage of 1.8 V across a wide input voltage range (1.9–3 V) and load current range (0–50 mA) while maintaining a phase margin above 53° for all load capacitances. Additionally, the TREC reduces undershoot from 315 mV to 182 mV and overshoot from 120 mV to 106 mV during rapid load current changes, while remaining inactive during steady-state to conserve power. Overall, the proposed LDO regulator offers a compact and power-efficient solution with enhanced dynamic response, making it suitable for integration into modern low-power electronic devices.

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