Cryogenic Measurement of CMOS Devices for Quantum Technologies

Jorge Pérez-Bailón, Miguel Tarancón, Santiago Celma, and Carlos Sánchez-Azqueta

***Abstract*— In this article we present the experimental characterization of active components of a standard 65 nm CMOS technology for a temperature range from 313 to 5 K, analyzing the variation of the main parameters over temperature and voltage, recovering their main parameters (threshold voltage V_{th}, transconductance G_m and channel conductance G_{DS}). The measurement has been carried out wire-bonding the bare dies with the devices to a dedicated printed circuit board (PCB) that has been placed inside a dilution refrigerator. The I_D-V_{DS} curves for both NMOS and PMOS transistors shows an increase of I_D in the cryogenic regime that is more relevant for high values of V_{GS} because for lower values it is partially compensated by the variation of V_{th}. Also, a kink is observed in these curves for high V_{DS} values, caused by the bulk current generated by impact ionization at the drain combined with the increased resistivity of the frozen-out substrate. The transconductance G_m reaches non-zero values for higher V_{GS} as T decreases and then peaks to higher values in the cryogenic regime. In turn, G_{DS} increases for increasing T, following the behavior observed for I_D. Both results are in accordance with other thermal characterizations carried out on CMOS transistors in different technologies.**

***Index Terms*— CMOS models, cryo-CMOS, cryogenic measurement, quantum technologies.**

I. Introduction

QUANTUM technologies are a new field of research and technological development that exploits the principles of quantum mechanics, namely entanglement and superposition [1]. Among its many potential applications are quantum sensors, capable of performing low-temperature magnetization measurements with high sensitivity and wide frequency spans [2]; or quantum computers, which are expected to solve problems intractable by classical digital computers, but also to dramatically increase the efficiency and reduce computation time in many other problems [3].

Something that is often required in the applications of quantum technologies is operating at very low temperatures, typically in a cryogenic regime of the order of mK. This is particularly true for certain quantum systems that are highly sensitive to their environment and require minimized noise to preserve their quantum states. In the case of quantum sensing, there are several applications that need to operate at very low temperatures, but the most important and widely recognized one is the superconducting quantum interference device (SQUID). SQUIDs have revolutionized the field of magnetometry due to their extraordinary sensitivity in detecting extremely weak magnetic fields.

In the field of quantum computing, qubits are realized through diverse materials and methodologies. Many of these qubits require extremely low temperatures to preserve their delicate quantum coherence. Among those are superconducting qubits, which currently are the most prevalent in use [4], semiconductor qubits, which have a promising potential for their integration with classical integrated circuits (ICs) [5] and qubits based on magnetic molecules, are one of the most promising candidates to encode spin qubits, due to the vast possibilities for design offered by chemical nanoscience [6]. Operating within the range of tens or hundreds of mK, these qubits effectively mitigate decoherence and enhance the stability of their quantum states.

It is worth noting that while there are quantum systems, like trapped ions or nitrogen vacancies, that can operate at room temperature due to their weaker coupling to the environment, many quantum technologies currently rely on low-temperature environments to ensure the preservation and manipulation of their quantum properties [7].

Quantum computing, with its potential to tackle highly complex problems far beyond classical computers, holds great promise. However, to fully unleash the potential of quantum computing, quantum error correction (QEC) becomes indispensable [8]. Even at ultralow temperatures of 10 mK, qubits still present error rates of about 0.1% per computational step [9]. The current difficulty lies in scaling quantum technology to the level required for fault-tolerant operation. Current projections suggest that the implementation of a system containing approximately a million error-corrected qubits will be imperative to achieve a functional error-protected quantum computer [10].

Manuscript received 2 August 2023; revised 12 September 2023; accepted 5 October 2023. Date of publication 18 October 2023; date of current version 31 October 2023. This work was supported in part by the Spanish Ministry of Science and Innovation under Grant PID2020-114110RA-I00; and in part by the Consejo Superior de Actividades Científicas (CSIC) Program for the Spanish Recovery, Transformation and Resilience Plan funded by the Recovery and Resilience Facility of the European Union, established by the Regulation (EU) 2020/2094 under Grant 20219PT007. The Associate Editor coordinating the review process was Dr. Zhengyu Peng. *(Corresponding author: Jorge Pérez-Bailón.)*

Jorge Pérez-Bailón is with the Quantum Materials and Devices (Q-MAD) Group, Institute of Nanoscience and Materials of Aragón (INMA), and the Group of Electronic Design (GDE), University of Zaragoza, 50009 Zaragoza, Spain (e-mail: jorgepb@unizar.es).

Miguel Tarancón is with the Group of Electronic Design (GDE), University of Zaragoza, 50009 Zaragoza, Spain (e-mail: 759966@unizar.es).

Santiago Celma is with the Department of Electronic and Communications Engineering and the Group of Electronic Design (GDE), University of Zaragoza, 50009 Zaragoza, Spain (e-mail: scelma@unizar.es).

Carlos Sánchez-Azqueta is with the Department of Applied Physics and the Group of Electronic Design (GDE), University of Zaragoza, 50009 Zaragoza, Spain (e-mail: csanaz@unizar.es).

Digital Object Identifier 10.1109/TIM.2023.3325446

1557-9662 © 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: Universidad de Zaragoza. Downloaded on January 19,2024 at 12:31:49 UTC from IEEE Xplore. Restrictions apply.

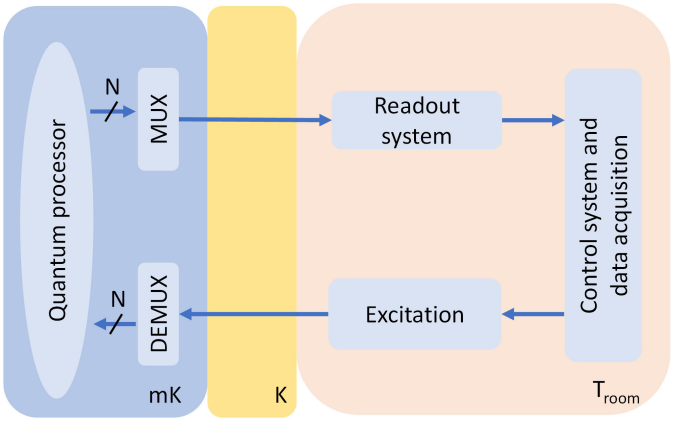


Fig. 1. Block diagram of the quantum-classical interface.

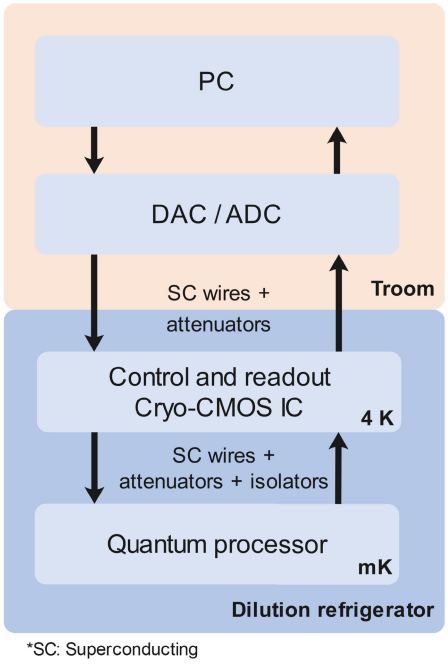


Fig. 2. Block view of the approach to interface a quantum processsor with a conventional binary computer.

In order to attain such scale, a significant enhancement is required in the control and measurement systems for quantum processors. Quantum-classical interfaces used to implement these systems using racks of room-temperature electronics connected to the quantum processor through coaxial cables with a scheme as the one shown in Fig. 1. However, to reach the million-qubit goal, a radical transformation in the method used to control these systems is needed. To that end, a different approach is currently used for the readout and control of quantum processors.

Among the many techniques that exist to interact with qubits, one of the most widely used techniques nowadays is to use tuneable couplers between qubits [11]. This system is used, for example, in Google's quantum processor, Sycamore, based on superconducting qubits called Transmons [12]. Furthermore, the qubits are coupled to a detuned resonator in such a way that measurement in the dispersive regime is possible [13].

However, these systems require one XY transmission line, three Z control lines (one for the qubit and two for adjacent couplers) per qubit, and one read line for every $\sim$6 qubits [13]. Considering that current quantum processors have tens of qubits and that it is expected to increase their number to thousands or millions of them and implement error correction systems, the number of channels and equipment needed to achieve this would be unattainable.

That is why work is being done on different proposals such as [12], [14], [15] to design CMOS ICs at cryogenic temperatures, since they present advantages such as the reduction of waveform distortion, since all the interconnections between the quantum controller and processor can be superconducting and higher stability due to strict temperature control [13], [16], [17].

This entails developing application-specific ICs (ASICs) for control and readout, strategically placed within the cryogenic environment and connected to the quantum processor through superconducting links as shown in Fig. 2 [9], [12].

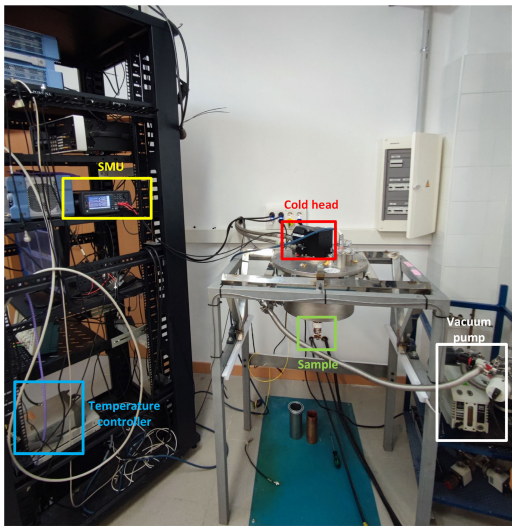
Placing the CMOS ASICs as close to the quantum processor as possible is of the utmost importance. By doing so, the need for lengthy interconnects can be minimized, improving overall system performance and efficiency. ASICs designed specifically for cryogenic operation, offer the feasibility to be integrated within the cryogenic system and connected directly to the quantum processor.

Moreover, the distinctive characteristics of these devices in cryogenic temperatures provide inherent advantages for quantum computing applications. Deep cryogenic temperatures enable the possibility of digital circuits based on Josephson junctions, and CMOS ASICs can be tailored to operate efficiently in such an environment, effectively overcoming challenges encountered by other technologies concerning heat dissipation and efficiency.

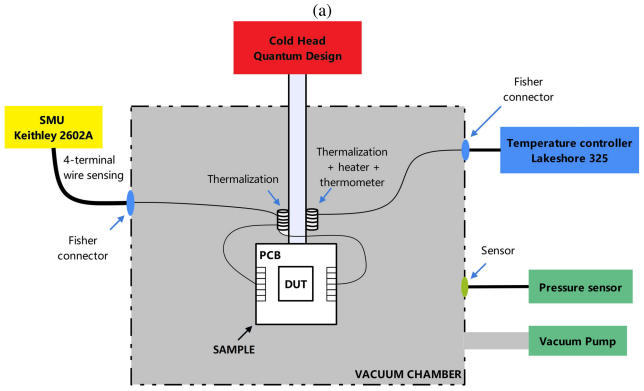
Therefore, CMOS circuits operating under cryogenic temperatures play a critical role in shaping the future of quantum computing. Their capacity to tackle power dissipation and scalability issues with quantum processors makes them indispensable. With the ability to facilitate large-scale fault-tolerant quantum computers, these cryogenic CMOS circuits pave the way for quantum computing to revolutionize diverse fields, addressing challenges beyond the capabilities of classical computing.

Another parameter that has to be considered is the finite heat dissipation capabilities of refrigerators, which force the electronics to have a very low power consumption. For instance, [18] used a mechanically driven Gifford McMahon cryo-cooler connected to a Leybold COOLPACK helium compressor unit to achieve a cooling capacity of 175 at 80 K, well above the target operation temperature of quantum computers. Because the heat dissipation capabilities of state-of-the-art dilution refrigerators are limited, and it decreases when operated in deep cryogenic regimes, the readout and control electronic systems need to have very low electrical power consumption, below $\sim$1 mW/qubit at 4 K [19] so that the refrigerators can keep the required cryogenic temperature.

Authorized licensed use limited to: Universidad de Zaragoza. Downloaded on January 19,2024 at 12:31:49 UTC from IEEE Xplore. Restrictions apply.



(a)



(b)

Fig. 3. Description of the measurement setup with the Quantum design Cryofree refrigerator. (a) Picture of the setup. (b) Schematic.

To design and fabricate the cryogenic CMOS circuits with the required high-performance capabilities in terms of low noise and low power consumption, the first stage is to develop accurate simulation models for the deep cryogenic temperature regimes that expand the current models, typically covering ranges from −40 °C (233.15 K) to +120 °C (393.15 K).

There are already proposals such as [20], which adapts the EKV model for long- and short-channel transistors at 4.2 K, or [21], which uses the 1-D Poisson equation and the drift-diffusion transport mechanism to model the depletion region and the conduction channel down to 4.2 K. On the other hand, [22] highlights some of the challenges faced for the modeling of MOSFET devices for operation at cryogenic temperatures with special focus on the threshold voltage V_{th} and the subthreshold swing, and [23] modifies the BSIM-CMG model of short-channel FinFETs to describe sub-threshold swing, threshold voltage, and effective mobility down to 10 K.

As can be seen, there are many alternatives to face the issue of modeling devices at cryogenic temperature but a great deal of research still remains to develop a general model suitable to simulate any kind of electron device. Therefore, it is necessary to characterize each technology and search for its corresponding valid model. In this context, we present the experimental characterization of active devices in a standard 65 nm CMOS process, covering the temperature range from 313 to 5 K.

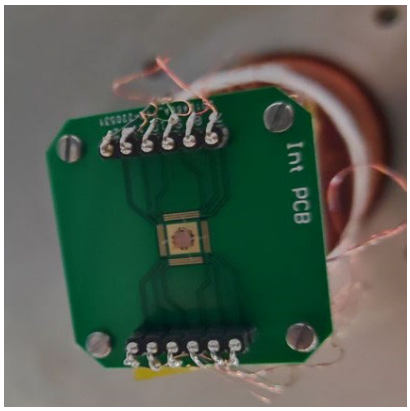


Fig. 4. Detail of the IC in the measurement setup, where it is wire-bonded to the PCB and then fit into the cryostat.

This article is organized as follows. Section II describes the IC characterized. In Section III, measurements at cryogenic temperatures are presented. Finally, the main conclusions drawn from this work are summarized in Section IV.

II. Experimental Setup

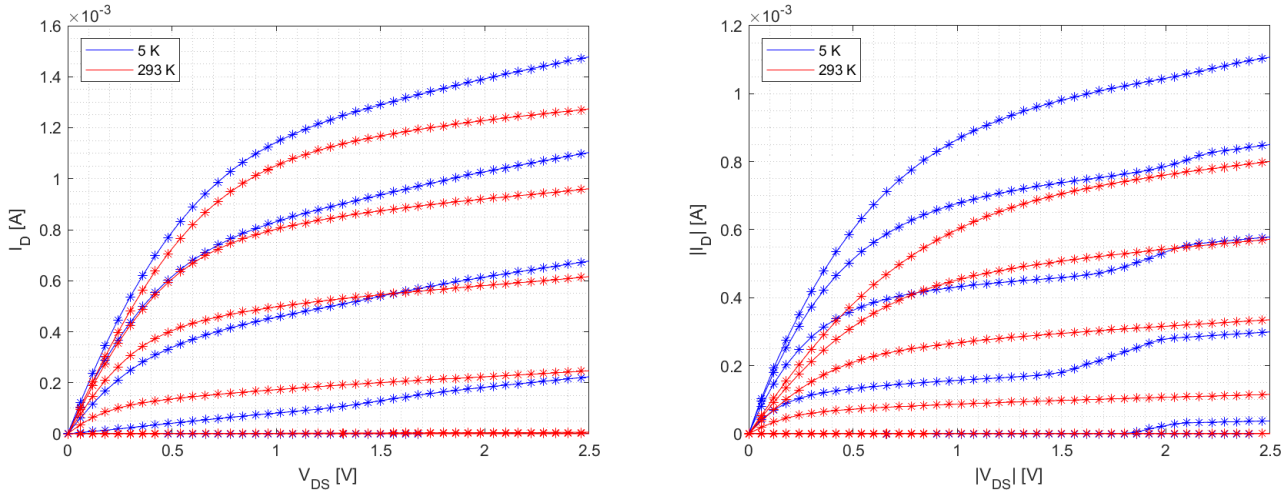
A. Measurement Setup

The experimental data have been obtained in two complementary setups. First, the transistors have been characterized in the temperature range from −40 °C (233 K) to +40 °C (313 K) using an Aralab Fitoterm 22E. Subsequently, they have been measured in a temperature range from room temperature down to 5 K using a Quantum Design Cryofree refrigerator. Fig. 3(a) shows a caption of the measurement setup and Fig. 3(b) a diagram of the setup.

The characterization process of these transistors requires a careful design of the measurement setup. To that end, the measurement process has been automated using a Keithley 2602A source/measure unit (SMU) programed via the open software Python and using the NI measurement and automation explorer (NI MAX). This is a two channel SMU that can perform four terminal measurements on each channel. Since parasite contributions need to be minimized, this four terminal method has been employed using twisted pairs wires with ground shielding to reduce any external noise. The wiring inside the refrigerator is thermalized by thermal contact with the Cold Finger made of Free Oxigen Cooper to improve thermal conductivity.

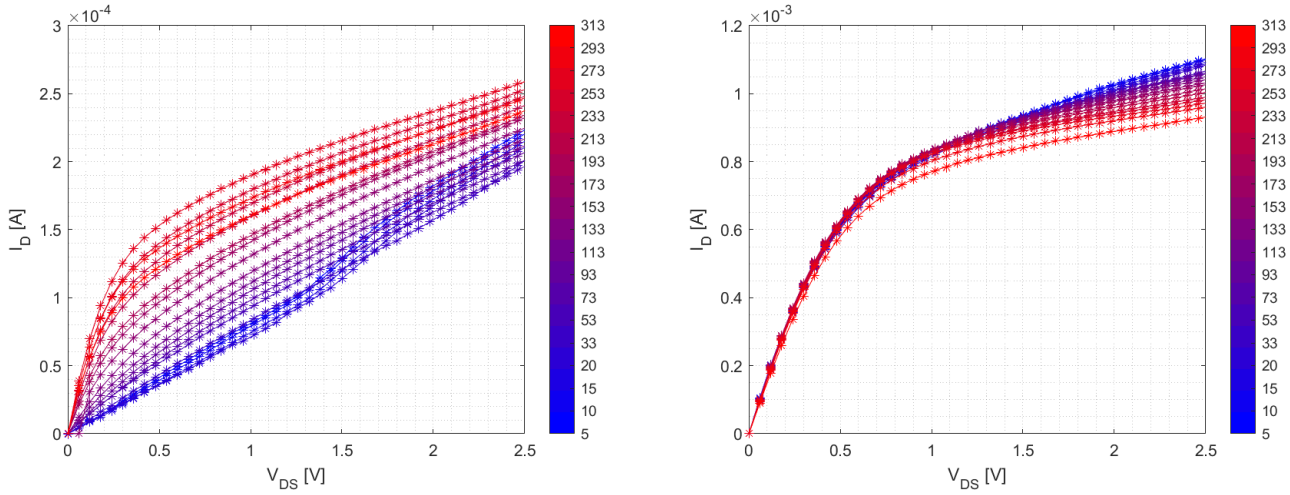
A custom printed circuit board (PCB) has also been designed and fabricated, considering also at this stage the bonding process. Since the pads of the IC have a size of only 57 × 71 μm with a separation of 90 μm between them, and therefore a slight deviation in the bonding process will produce a short circuit between them. Moreover, to maximize thermalization between the PCB and the device under test (DUT), GE-varnish with excellent thermal and electrical properties has been used to attach the dice to the PCB. While to thermalize the PCB with the Cold Finger, we finished the

Authorized licensed use limited to: Universidad de Zaragoza. Downloaded on January 19,2024 at 12:31:49 UTC from IEEE Xplore. Restrictions apply.



(a) (b)

Fig. 5. Measured I_D-V_{DS} curves for V_{GS} ranging from 0 to 2.5 V in 0.5 V steps for (a) NMOS transistor and (b) PMOS transistor, both with $W/L = 1$ μm/100 nm, for a temperature of 5 K (blue) and 293 K (red).



(a) (b)

Fig. 6. Measured I_D-V_{DS} curves for the NMOS transistor in the whole temperature range from 5 to 313 K. (a) Curve for $V_{GS} = 1$ V. (b) Curve for $V_{GS} = 2$ V.

PCB with electro-less nickel/immersion gold (ENIG) leaving the bottom layer without soldermask.

Another key aspect that has to be taken into account is the material with which the bonding is done. Nowadays, although other materials like copper, platinum, silver, and some palladium alloys are used in certain specific applications, the two most commonly used materials for bonding are aluminum and gold. While gold has a smaller resistivity than aluminum, also in the cryogenic regime, aluminum provides a low enough resistivity (about 26.5 nΩ m^{-1}) while presenting good fatigue resistance, which makes aluminum wires with small diameter the preferred choice when ultrasonic wedge bonding is employed, as it is our case. Taking the above into account, in both cases the ICs have been wire-bonded directly to a PCB with ultrasonic wedge bonding using a Kulicke and Soffa 4500 Series manual wire bonder with a 25 μm diameter aluminum wire. The temperature control is done through the Cold Head From Quantum Design that cools down the system, while the Lakeshore 335 Cryogenic Temperature Controlled reads the thermometer and controls the heater that are both located next to the PCB. This heater delivers a total of 75 W.

B. Integrated Circuit

A batch of ICs has been designed and manufactured in a 65 nm CMOS process with shallow trench isolation, twin and deep N-wells, and dual gate oxide (core and IO). The IC used in this work includes isolated NMOS and PMOS transistors (1 μm/100 nm), connected so that all of them share their gate-source and bulk terminals, while the drains can be accessed separately. The technology has a nominal supply of 1.2 V, although higher values have been tested to expand the measurement range. Fig. 4 shows the IC after being wire-bonded to the PCB and attached to the cavity of the refrigerator.

Authorized licensed use limited to: Universidad de Zaragoza. Downloaded on January 19,2024 at 12:31:49 UTC from IEEE Xplore. Restrictions apply.

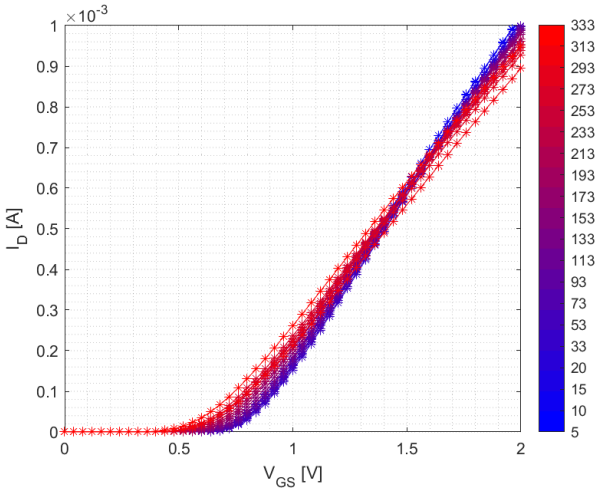


Fig. 7. Measured I_D-V_{GS} curves in the NMOS transistor in the temperature range from 5 to 313 K.

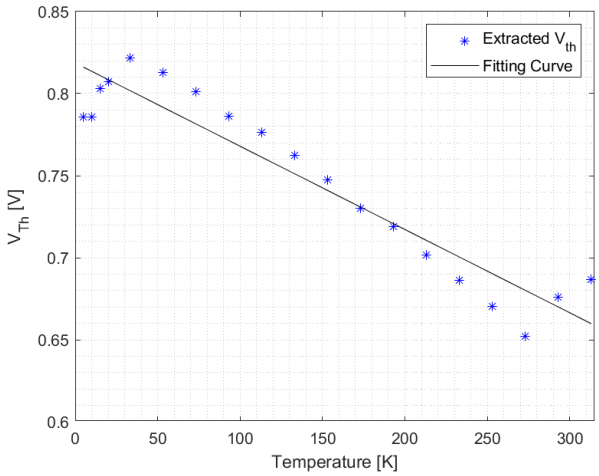


Fig. 8. Dependence of the threshold voltage V_{th} with temperature in the range from 5 to 313 K.

III. Measurements

Both the NMOS and PMOS transistors have been measured from 5 K to room temperature with 20 K steps. Whereas the I_D-V_{DS} characteristic curves of the transistors are presented for both MOS devices, the detailed analysis of their behavior will be presented focusing mainly on the NMOS transistors.

A. Transistor Characteristic Curves

Fig. 5 shows the I_D-V_{DS} curves obtained for the NMOS and PMOS transistors at 5 K and room temperature for V_{GS} ranging from 0 to 2.5 V. As it can be seen, I_D increases as the temperature decreases, which is the expected behavior due to the increase of the mobility of the carriers [24], although this only happens for high values of V_{GS}. Moreover, a kink is observed at high V_{DS} values, especially for the PMOS transistor, due to the bulk current generated by impact ionization at the drain combined with the increased resistivity of the frozen-out substrate [25].

To further analyze this effect, Fig. 6 shows the I_D-V_{DS} curves for the NMOS transistor in the whole temperature range for $V_{GS} = 1$ and 2 V, showing that the increase of current for cryogenic temperature takes place in the latter case. The reason for this, as will be shown later, is that the increase in mobility is partially compensated by the variation of the V_{th} [26].

B. Recovered Values for V_{th}

The I_D-V_{GS} curves have allowed us to conclude that V_{th} must decrease with T to compensate for the increase in carrier mobility. To check this, the $I_D - V_{GS}$ curves have been measured in the whole temperature range, as shown in Fig. 7. It can be observed that I_D at cryogenic temperatures is lower for low V_{GS} and larger for large V_{GS} than for room temperature. Fig. 7 also shows that this effect follows a continuous trend in the whole temperature range. The dependence of V_{th} with temperature in the whole range has been obtained, as shown in Fig. 8. It can be seen that, as expected, the trend is that the threshold voltage increases as temperature decreases. Also, this dependence changes in the deep cryogenic regime, for which V_{th} decreases as T decreases.

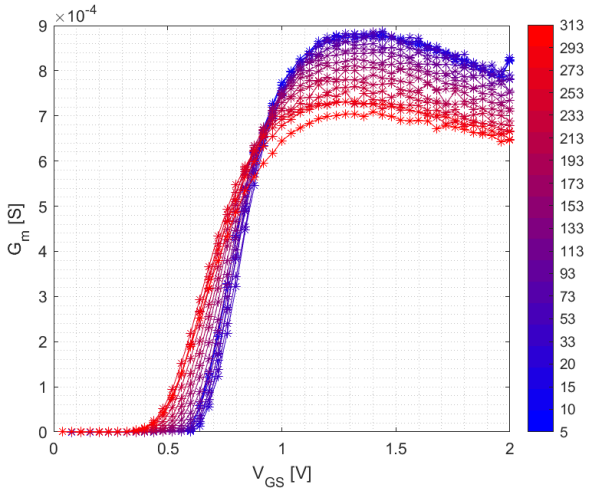


Fig. 9. Measured G_m-V_{GS} curve for the NMOS transistor for temperatures ranging from 5 to 313 K.

C. Recovered Values for G_m

One key parameter in the modeling of CMOS transistors is its transconductance G_m and channel conductance G_{DS}. In this work, its value has been extracted from the obtained $I_D - V_{GS}$ curves and the threshold voltage computed in Section III-B using

$$G_m = \frac{2I_D}{V_{GS} - V_{th}}. \quad (1)$$

Fig. 9 shows the dependence of G_m with respect to V_{GS} in the whole temperature range down to 5 K. It can be seen how the value of the transconductance G_m reaches non-zero values for higher V_{GS} as the temperature decreases, and then peaks to a higher value in the cryogenic regime than at room temperature, which is in accordance to other thermal characterization of CMOS processes [24].

Authorized licensed use limited to: Universidad de Zaragoza. Downloaded on January 19,2024 at 12:31:49 UTC from IEEE Xplore. Restrictions apply.

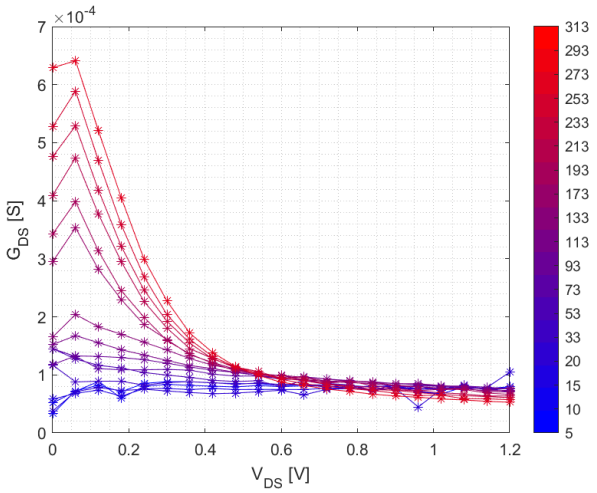


Fig. 10. Measured G_{DS}-V_{DS} curves for the NMOS transistor for temperatures ranging from 5 to 313 K.

D. Recovered Values for G_{DS}

Another fundamental parameter in the modeling of CMOS transistors is the channel conductance G_{DS}. Using that

$$G_{\mathrm{DS}} = \frac{\partial I_D}{\partial V_{\mathrm{DS}}} \tag{2}$$

its value has also been obtained from the experimental curves by computing the incremental changes in I_D with respect to the incremental changes in V_{DS}.

The results obtained are shown in Fig. 10, which represents G_{DS} against V_{DS} in the whole temperature range down to 5 K, for a V_{GS} value of 1 V. It can be seen that G_{DS} increases for increasing temperature, which is in accordance with the behavior obtained for I_D and also follows the trend shown in other cryogenic characterizations of CMOS devices such as those reported in [23].

IV. Conclusion

This article presents the experimental characterization of CMOS transistors in a 65 nm node in a temperature range from 313 K (40 °C) down to the cryogenic regime at 5 K. The experimental data have been obtained in two complementary setups, using an Aralab Fitoterm 22E chamber to cover the range from −40 °C (233 K) to +40 °C (313 K). In turn, to reach the cryogenic regime down to 5 K a dilution refrigerator model Quantum Design Cryofree has been used.

The measurement setup has been completed with a dedicated PCB, to which the bare dies, which have PADs of 57 × 71 μm and are separated 90 μm, have been bonded with ultrasonic wedge bonding using aluminum wire of 25 μm diameter and a Kulicke and Soffa 4500 Series manual wire bonder. Another specific PCB has been designed and fabricated to minimize parasitic contributions coming from the encapsulation of the IC. Finally, the process has been automated using a Keithley 2602A SMU programmed with the open software Python and using the NI MAX.

The measurement of the I_D-V_{DS} for the NMOS and PMOS transistors at room temperature and at 5 K allows to observe the expected behavior of the transistors in the cryogenic regime, which is an increased I_D due to the increase of the mobility of the carriers, a phenomenon that is more relevant for high values of V_{GS} because for lower values this is partially compensated by the variation of the V_{th}, as it has also been confirmed from the measurements. Also, a kink is observed in these curves for high V_{DS} values, especially for the PMOS transistor, which happens because of the bulk current generated by impact ionization at the drain combined with the increased resistivity of the frozen-out substrate.

Another two key parameters in the modeling of CMOS transistors are their transconductance G_m and channel conductance G_{DS}, both of which have been extracted from the $I_D - V_{\mathrm{GS}}$ curves and the obtained threshold voltage. It has been seen that G_m reaches non-zero values for high V_{GS} as T decreases, then peaking to higher values in the cryogenic regime; in turn, it has been shown that G_{DS} increases for increasing T, following the behavior observed for I_D. Both results are in accordance to other thermal characterizations carried out on CMOS transistors in different technologies.

This work presents an experimental characterization of the behavior of transistors for a standard 65 nm CMOS technology down to 5 K, allowing to observe the evolution of their main performance parameters from temperatures ranging to room temperature to the cryogenic regime, as well as some of the effects that are expected to take place at cryogenic temperature, which is the first step to develop an accurate simulation model valid in the cryogenic temperature regime.

References

[1] C.-J. Yu, S. von Kugelgen, D. W. Laorenza, and D. E. Freedman, "A molecular approach to quantum sensing," *ACS Central Sci.*, vol. 7, no. 5, pp. 712–723, May 2021.

[2] Y. Han et al., "Steep switching Si nanowire p-FETs with dopant segregated silicide source/drain at cryogenic temperature," *IEEE Electron Device Lett.*, vol. 43, no. 8, pp. 1187–1190, Aug. 2022.

[3] V. Rollano et al., "High cooperativity coupling to nuclear spins on a circuit quantum electrodynamics architecture," *Commun. Phys.*, vol. 5, no. 1, p. 246, Oct. 2022.

[4] M. H. Devoret, A. Wallraff, and J. M. Martinis, "Superconducting qubits: A short review," 2004, *arXiv:cond-mat/0411174*.

[5] A. Chatterjee, P. Stevenson, S. De Franceschi, A. Morello, N. P. de Leon, and F. Kuemmeth, "Semiconductor qubits in practice," *Nature Rev. Phys.*, vol. 3, no. 3, pp. 157–177, Feb. 2021.

[6] I. Gimeno et al., "Enhanced molecular spin-photon coupling at superconducting nanoconstrictions," *ACS Nano*, vol. 14, no. 7, pp. 8707–8715, Jul. 2020.

[7] F. Jazaeri, A. Beckers, A. Tajalli, and J.-M. Sallese, "A review on quantum computing: From qubits to front-end electronics and cryogenic MOSFET physics," in *Proc. MIXDES 26th Int. Conf. 'Mixed Design Integr. Circuits Syst.*, 2019, pp. 15–25.

[8] J. C. Bardin et al., "A 28 nm bulk-CMOS 4-to-8 GHz <2 mW cryogenic pulse modulator for scalable quantum computing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jul. 2019, pp. 456–458.

[9] J. C. Bardin et al., "Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 k," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, Nov. 2019.

[10] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, "Surface codes: Towards practical large-scale quantum computation," *Phys. Rev. A, Gen. Phys.*, vol. 86, no. 3, Sep. 2012, Art. no. 032324.

[11] O. Ezratty, "Perspective on superconducting qubit quantum computing," *Eur. Phys. J. A*, vol. 59, no. 5, p. 94, May 2023.

[12] J. Bardin, "Beyond-classical computing using superconducting quantum processors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, 2022, pp. 422–424.

Authorized licensed use limited to: Universidad de Zaragoza. Downloaded on January 19,2024 at 12:31:49 UTC from IEEE Xplore. Restrictions apply.

[13] J. Anders et al., "CMOS integrated circuits for the quantum information sciences," *IEEE Trans. Quantum Eng.*, vol. 4, 2023, Art. no. 5100230.
[14] D. J. Frank et al., "A cryo-CMOS low-power semi-autonomous qubit state controller in 14 nm FinFET technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Jul. 2022, pp. 360–362.
[15] J.-S. Park et al., "A fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22 nm FFL FinFET technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Jun. 2021, pp. 208–210.
[16] S. Joshi and S. Moazeni, "Scaling up superconducting quantum computers with cryogenic RF-photonics," 2022, *arXiv:2210.15756*.
[17] D. S. Holmes, "Cryogenic electronics and quantum information processing," in *Proc. IEEE Int. Roadmap for Devices Syst. Outbriefs*, Nov. 2021, pp. 1–93.
[18] J. Jiménez, A. Grau, and C. Padilla, "Integration of a testbench for the optical and thermal characterization of near-infrared detectors used in ground and space-based astronomy," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–7, 2020.
[19] F. Sebastiano et al., "Cryogenic CMOS interfaces for quantum devices," in *Proc. 7th IEEE Int. Workshop Adv. Sensors Interfaces (IWASI)*, 2017, pp. 59–62.
[20] A. Beckers, F. Jazaeri, A. Ruffino, C. Bruschini, A. Baschirotto, and C. Enz, "Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing," in *Proc. 47th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2017, pp. 62–65.
[21] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018.
[22] C. Enz, A. Beckers, and F. Jazaeri, "Cryo-CMOS compact modeling," in *IEDM Tech. Dig.*, Dec. 2020, pp. 3–25.
[23] S. K. Singh, S. Gupta, R. A. Vega, and A. Dixit, "Accurate modeling of cryogenic temperature effects in 10-nm bulk CMOS FinFETs using the BSIM-CMG model," *IEEE Electron Device Lett.*, vol. 43, no. 5, pp. 689–692, May 2022.
[24] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2017.
[25] E. Simoen and C. Claeys, "Impact of CMOS processing steps on the drain current kink of NMOSFETs at liquid helium temperature," *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1207–1215, Jun. 2001.
[26] C. Luo, Z. Li, T.-T. Lu, J. Xu, and G.-P. Guo, "MOSFET characterization and modeling at cryogenic temperatures," *Cryogenics*, vol. 98, pp. 12–17, Mar. 2019.

Jorge Pérez-Bailón received the B.Sc., M.Sc., and Ph.D. degrees in physics from the University of Zaragoza, Zaragoza, Spain, in 2015, 2016, and 2022, respectively.

He is currently a member of the Institute of Nanoscience and Materials of Aragón (INMA), CSIC. His research interests include analog and mixed CMOS integrated circuits, on-chip programmable circuits, smart instrumentation development, and cryo-CMOS and superconducting devices for quantum technologies.

Miguel Tarancón received the B.Sc. and M.Sc. degrees in physics from the University of Zaragoza, Zaragoza, Spain, in 2021 and 2022, respectively.

He is currently a member of the Group of Electronic Design, Aragon Institute of Engineering Research, University of Zaragoza. His research interests include cryo-CMOS for quatum computing and electronic circuit simulation.

Santiago Celma was born in Zaragoza, Spain. He received the B.Sc., M.Sc., and Ph.D. degrees in physics from the University of Zaragoza, Zaragoza, in 1987, 1989, and 1993, respectively.

He is currently a Full Professor with the Group of Electronic Design, Aragon Institute of Engineering Research, University of Zaragoza. He has coauthored more than 130 technical articles and 320 international conference contributions. He is the coauthor of four technical books and the holder of four patents. He has participated in 70 national and international research projects, 40 of which as a principal investigator. His research interests include cyber-physical systems, hardware security and cryptosystems, analog and mixed signal processing, front-ends for wireline and wireless communications, RFIC and MMIC integrated circuits, and cryo-CMOS design for quantum computing.

Carlos Sánchez-Azqueta was born in Zaragoza, Spain. He received the B.Sc., M.Sc., and Ph.D. degrees in physics from the University of Zaragoza, Zaragoza, in 2006, 2010, and 2012, the Dipl.-Ing. degree in electronic engineering from the Complutense University of Madrid, Madrid, Spain, and the Helsinki University of Technology, Helsinki, Finland, in 2009, and the Ph.D. degree in education from the University of Zaragoza, in 2022.

He is currently an Assistant Lecturer with the Department of Applied Physics, University of Zaragoza. He is also a member of the Group of Electronic Design, Aragon Institute of Engineering Research, University of Zaragoza. He has coauthored more than 45 technical articles and 150 conference contributions. He has participated in 25 national and international research projects, 12 of which as a principal investigator. His research interests include mixed signal integrated circuits, high-frequency analog communications, cryptography applications, and quantum computing.

Authorized licensed use limited to: Universidad de Zaragoza. Downloaded on January 19,2024 at 12:31:49 UTC from IEEE Xplore. Restrictions apply.