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RESEARCH ARTICLE

Software-Defined Analog Processing Based on IEC 61850 Implemented in an Edge Hardware Platform to be Used in Digital Substations

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ABSTRACT The IEC 61850 standard has brought new opportunities for developing Centralized Substation Protection and Control (CPC) platforms to be used in digital substations. The CPC operation requires a proper signal processing module that provides the necessary parameters and signals accurately and at times needed to ensure the platform's control and protection services can operate correctly. This paper proposes and implements a sampled values-analog processing module (SV-APM) for a software-based CPC in a digital substation developed in the framework of the EPICS project. The SV-APM decodes the digital messages published by merging units and extracts the information required by control and protection functions implemented in a software-based CPC platform. To check SV-APM performance, a set of tests is carried out using Real-time digital simulator (RTDS) and EPICS platform in Hardware in the Loop configuration (HiL). These tests evaluate SV-APM behavior against disturbances in communication channels, voltage and current variations, harmonic contents and frequency variations. Furthermore, latency tests are carried out to evaluate CPC response times. From tests, it is concluded that SV-APM output satisfactorily fulfills all the time response and accuracy requirements demanded during its development.

INDEX TERMS Centralized control, digital signal processing, edge computing, power system protection, IEC61850, sampled values, virtualization.

I. INTRODUCTION

The rapid evolution in which the electrical system is immersed, mainly due to the increase in the penetration of renewable energies, is posing new challenges for the protection, control and operation of traditional electrical systems. Some of these challenges have been foreseen and exposed in the literature, such as protection issues [1], [2], [3], [4], power system stability [5], [6], [7], [8] or power quality [9]. Still, others arise suddenly, forcing the adaptation of the current protection and control algorithms and the development of new techniques that allow maximizing the integration of renewables in the system.

There is a clear consensus that the solutions offered by traditional protection and control manufacturers will continue to be the basis of the electrical system. However, it must be considered that the electrical power system is constantly evolving and that renewable energy penetration levels differ from country to country [10]. The same also occurs with solutions such as STATCOM, batteries, and synchronous

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compensators used for network support. Because of this, the protection system must be able to offer parallel solutions that allow a rapid response to local challenges not covered by traditional manufacturers or whose resolution entails a substantial delay.

With the increased substation digitalization caused by the development of IEC 61850 communication standard, new opportunities have arisen for the development of platforms that can execute protection, control, monitoring and communication services in a centralized manner, commonly known as CPC (Centralized Substation Protection and Control) [11], [12], [13], [14]. Reference [15] classifies CPC technologies into three categories:

- Integrated solutions: The solution provides the complete architecture of the CPS system to be implemented in the substation, including sensors, CPC units and communication units. The communication protocol can be proprietary protocols.
- Vendor-specific solutions: The vendor provides a CPC unit with software and application algorithms in the same hardware. It must be fully IEC61850- compliance.
- Software-based solutions: This solution is based on decoupling software from their dedicated hardware to perform protection and control actions.

The present paper focuses on the last category because this solution is a hot topic that is gaining popularity due to advantages such as increased processing flexibility, scalability improvement and reduced deployment and maintenance costs [16], [17], [18].

The software-based CPC solution requires a signal processing module to operate the control and protection services implemented in the platform. This module must provide the necessary parameters and signals with accuracy and in the required times for the correct operation of the control and protection services. Only some studies have been found in the literature about this aspect. Reference [19] describes the design of a distributed signal processing unit (DSPU) applied to transmission line protection. The study extracts, from the analog signals measured in the substation bay, the information used by protection functions such as harmonics, interharmonics, $\cdots$ Once this information is obtained, it is encoded and published via the IEC 61850 GOOSE communication service. CPC subscribes to this information and performs the corresponding protection and control functions. The solution proposed in [19] does not consider how issues in communication channels, such as loss of packets and delays, can affect the operation of protection functions implemented in CPC. Furthermore, this solution involves specific hardware for its implementation.

On the other hand, from a CPC architecture point of view, there is not a single standard CPC architecture to be used in electrical substations. IEEE PES PSRC WG K15 defined five options in the working group report [11]. CPC architectures are usually based on the use of Ethernet LAN networks and intelligent merging units that digitalize the analog values measured in the substation bay. Then, this CPC architecture will be used during the study.

Considering the previous aspects, the present paper proposes and develops an Analog Processing Module (APM) based on the IEC61850 Sampled Values signal (SV) to be implemented via software in a generic hardware platform. This work is part of the EPICS project (Edge Protection and Intelligent Control in Substations) [20], where a software-based CPC platform has been designed to execute protection, control and automation algorithms in digital substations in a centralized way. EPICS separates hardware and software in protection and control systems and implements an architecture based on containerized microservices executed on generic hardware such as a conventional server. Then, EPICS platform is not built using vendor-specific software nor hardware. It is worth noting that EPICS is implemented over a server Lenovo ThinkSystem SE350 with 16 Intel Xeon D-2183IT (32 cores) at 2.2 GHz with 64GB of memory. The server has an ''Edge Computing'' design with significant smaller dimensions than traditional servers giving enough flexibility for its installation. The operating system used in that server was Rocky Linux 9.0.

As previously indicated, the signal processing unit in EPICS is performed by an Analog Processing Module (APM) based on the IEC61850 Sampled Values signal (SV). This unit is called *SV-APM*. The function of the *SV-APM* is to process IEC61850 SV signals measured in the substation bay and extract the necessary information for the correct operation of the services implemented in the CPC platform. For this task, *SV-APM* uses the following stages: signal reconstruction, frequency measurement, resampling and data window generation and, finally, a calculation of phasors, harmonics and symmetrical components. The protection and control services of the electrical power system subsequently use the outputs of the *SV-APM* module. To provide scalability to EPICS, the design of the *SV-APM* module allows to instantiate repeatedly on different cores servicing different sources each one, due to the concurrent nature of *SV-APM* instances and Shared Database, i.e., due to the capability to parallelize the tasks.

Several types of tests have been defined using a real-time simulator (RTDS) in a closed loop with the EPICS platform to validate the behavior of the *SV-APM*. These tests aim to evaluate the *SV-APM* functional behavior against disturbances in the communications network, such as loss of packets, loss of time synchronization, invalid quality and delays. Furthermore, additional tests are performed to evaluate the accuracy of phase voltage and current phasors, harmonics, network frequency and symmetrical components, verifying that the results are within a proper tolerance for use in protection and control algorithms.

It is essential to indicate that, in addition to the precision in the results, this system must be capable of meeting the requirements related to response times required by the control and protection systems. The results provided by *SV-APM* must be calculated in time to allow the other EPICS services

to react in the expected time. With this idea, latency tests have also been carried out in this study.

All in all, the contribution of the present paper can be summarized as follows:

- The proposal of a signal processing module software-based implemented in a generic conventional server. It takes as an input the signals digitalized by MU and generates the required information to feed the control and protection algorithms. From the literature review, it has not been previously explained. Then, a detailed explanation about the steps needed to implement the digital processing module is provided.
- A set of HiL tests in a lab environment. A specific methodology has been defined to compare the values generated by RTDS versus the ones calculated by the proposed processing module. The obtained result accuracy of results is within the margin tolerated by commercial IEDs.

To describe the developed work, the paper is structured as follows. Section II describes the signal processing module implemented in EPICS platform along with its modules. The laboratory test bench and the test carried out to evaluate *SV-APM* operation are described in Section III and Section IV. Finally, the principal results and conclusions are included in Sections V and Section VI.

II. SIGNAL PROCESSING MODULE DESCRIPTION

Fig. 1 shows the general scheme of the EPICS platform operation. At the left of the figure appears the Merging Unit (MU). The MU is a physical device used to convert the primary current and voltage analog signals (three-phase voltage and current signals) provided by instrument transformers (current and voltage transformers, respectively) into digital messages [21]. These digital messages are published on the process bus according to IEC 61850-9 LE [22].

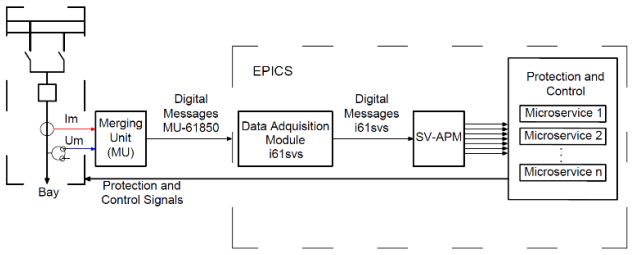

FIGURE 1. General diagram of EPICS platform.

EPICS platform, represented in the dashed line, subscribes and processes these data through the Data Acquisition Module and the Sampled Values-based Analog Processing Module (*SV-APM*). Once these data are processed, they are shared with the different microservices implemented in the Protection and Control Module. These microservices only use the variables necessary for their right operation. When microservices are processed, their protection and/or control output signals are sent to the substation bay to execute control or protection actions.

As previously indicated, EPICS uses two modules to process digital messages: *Data Adquisition Module (i61svs)*and *SV-APM*. The *Data Acquisition Module* initially processes the data sent by the MU, which arrives with a sampling period of 250 μs+Δt. Based on the specifications of [22], a value of Δt around 100 μs is expected. The *Data Acquisition Module* contains different microservices, including the so-called *i61svs*, which decodes the SV frames received from the MU at a data rate of 4000 samples per second, extracts the signals contained in such samples and delivers them to the *SV-APM* module. Once the data arrive at *SV-APM*, they are processed through different submodules. These submodules are shown in Fig. 2.

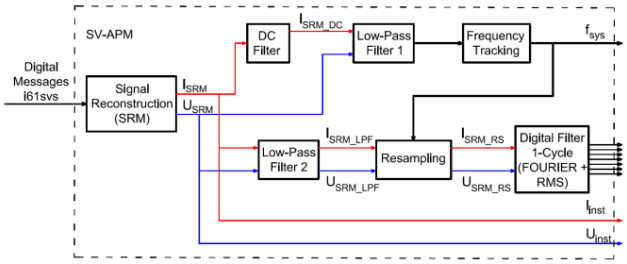

FIGURE 2. Detailed diagram of SV-APM module.

As it is shown in Fig. 2, the elements that make up the *SV-APM* are listed below:

- Signal Reconstruction Module (SRM): This submodule manages the data in case of problems associated with the communication network (packet loss, invalid data quality, loss of synchronization,...).
- DC filter. This filter removes the DC offset component from the fault current signal (I_{SRM}).
- Low-Pass filters. These filters smooth the input signals by attenuating their high-frequency variations.
- Frequency Tracking Module. This submodule is used to calculate the real frequency of the system (f_{sys}).
- Resampling Module and Generation Data Window. This submodule constructs the updated data window using the real frequency of the system.
- Digital Filter 1-Cycle (RMS calculation and Fourier transform). This submodule calculates the magnitude and angle of the signal phasors, symmetrical components and signal harmonic contents.

Table 1 summarizes the inputs and outputs used by each of the modules that make up *SV-APM*.

After the processing stage, the *SV-APM* provides the following information obtained from the three-phase voltage and current signals sent by the Merging unit to all the services available on the platform: instantaneous values (I_{inst}, U_{inst}), magnitude and phase angle of the phasors, symmetrical components, RMS values and the amplitudes of the first five harmonics. Furthermore, *SV-APM* also provides the services

TABLE 1. Input and output signals of the *sv-apm* module.

SV-APM Modules	Input signals	Output signals
Signal Reconstruction Module (SRM)	Sampled Values stored in memory by i61svs	Reconstructed signals in case of loss or delay (I_{SRM},U_{SRM})
DC filter	I_{SRM}	Reconstructed current signal without DC offset (I_{SRM_DC})
Frequency Tracking Module	I_{SRM_DC} and U_{SRM} after being processed by a low-pass filter	Real frequency of the system (f_{sys})
Resampling Module and generation data window	Reconstructed signal processed using a low-pass filter (I_{SRM_LPF}, U_{SRM_LP}) and f_{sys}	Resampled current and voltage data with a sampling rate of 80 samples per cycle (I_{SRM_RS}, U_{SRM_RS})
Digital Filter 1-Cycle (FOURIER +RMS)	I_{SRM_RS}, U_{SRM_RS}	Magnitude, Angle, Symmetrical Components, magnitude of harmonics up to order 5, and RMS

a reconstructed sample window and a global measurement of the grid frequency though the Frequency Tracking Module.

Following, the detailed operation of each of *SV-APM* sub-modules is described.

A. SIGNAL RECONSTRUCTION MODULE (SRM)

This module allows managing the data in case of problems in the communication system related to the Ethernet network:

1. Loss of packets: SRM considers a lost sample when the timestamp delay between two consecutive samples exceeds 500 μs, or they come in disorder. The objective in these cases is to reduce the impact of lost data in protection functions. SRM calculates the lost sample using a sample estimation algorithm based on Newton's interpolation polynomials of degree 2 [23]. Equation (1) describes the expression to obtain the missed samples in a function called X shown in Fig. 3. The X function represents the voltage or current waveform.

$$x(t) = x_1 + \frac{(x_2 - x_1)\cdot(t - t_1)}{t_2 - t_1} + \frac{\left(\left(\frac{x_3 - x_2}{t_3 - t_2}\right) - \left(\frac{x_2 - x_1}{t_2 - t_1}\right)\right)\cdot(t - t_1)\cdot(t - t_2)}{t_3 - t_1} \quad (1)$$

where $x(t)$ is the sample to be estimated at the timestamp t, and (x_1, t_1), (x_2, t_2) and (x_3, t_3) are the previous samples used to estimate the missed sample.
If three consecutive samples are lost, *SV-APM* and protection functions are temporally blocked. The blocking is reset by the reception of a valid SV frame with a *smpCnt* zero.

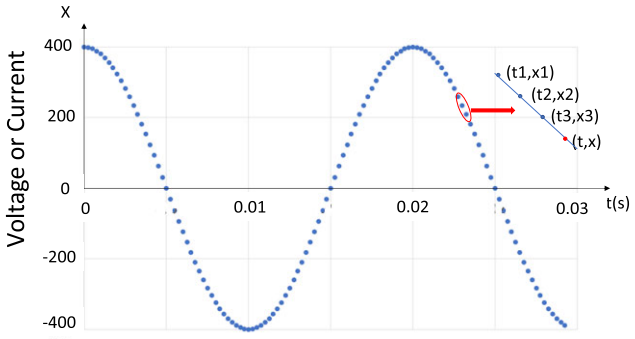

FIGURE 3. Newton's interpolation polynomial of degree 2.

2. Invalid quality data: This module temporarily disables the *SV-APM* and protection functions when specific quality bits of any received frames are invalid. The standard defines a quality byte to indicate the reliability of the samples published by the merging units. This quality byte is composed of eight quality bits. The status of these bits can impact the protection and control functions operation. Then, it is important to select, according to power system operator standards, which of them shall lock *SV-APM*. This selection is configurable in EPICS platform. Then, in case of fault, only the bits selected will be able to lock *SV-APM*, avoiding maloperation of the protection or control system. The system is unlocked after receiving a valid sampled value frame with a *smpCnt* of zero.
3. Loss of time synchronization: When time synchronization issues are detected, a synchronization error bit is generated and sent to the protection functions. The bit is reset after receiving a valid *smpCnt* of zero.

B. FREQUENCY TRACKING MODULE

The voltage and current signals in the electric grid, where the fundamental harmonic frequency is 50 or 60 Hz, contain harmonics and subharmonic components. Furthermore, during short-circuit events, DC decreasing component is usually superimposed on the alternating current.

Then, before estimating the power system frequency (f_{sys}), filters must be applied to condition the signals provided by *SRM*.

Firstly, a filter is applied to current signals provided by *SRM* to avoid DC components during a short-circuit, using reference [24].

To reduce the harmonic content and, thus, to increase the accuracy of power system frequency calculation, the input signals are also filtered using a second-order low-pass Butterworth filter with a cutoff frequency of 150 Hz (called *low-pass filter 1* in Fig. 2). This filter introduces a delay in the frequency calculation estimated below 1.6 ms, which could be considered a small tradeoff for better frequency estimation. However, it must be considered that this delay is not transmitted to the calculations carried out in the FOURIER+RMS

module. Consequently, this delay will not affect the operation of protection and control microservices.

Once input signals are filtered, a zero-crossing detection algorithm is used to estimate the power system frequency from the signals provided by the *Signal Reconstruction Module*, following the method proposed in [25]. The algorithm detects the sign changes of adjacent samples whenever they are above a specific threshold, as in Fig. 4. This study selects a threshold of 0.05 times the rated voltage value to consider the measurement errors.

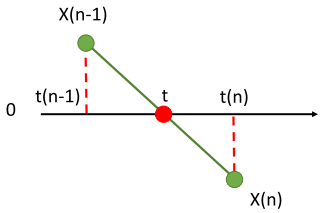

FIGURE 4. Zero-crossing detection: Linear interpolation.

Once zero-crossing is detected, the linear interpolation method described in Fig. 4 and (2) is used to find the time stamp (t) when the zero-crossing happens.

$$t = t_{n-1} - \frac{x_{n-1}}{x_n - x_{n-1}} \cdot (t_n - t_{n-1}) \tag{2}$$

The procedure used by this module to calculate the system frequency is described in [25] and details below. Three power cycles (seven zero-crosses) are considered to calculate the system frequency (f_{sys}). Every time a data set sample is received, zero-crossing is checked. When it happens, the time stamp is calculated using (2) and stored in a moving data window of size 7. Once seven zero-crossing values are available in the data window, five signal periods are calculated (T_0, T_1, ... T_4) (see Fig.5) and its average value ($T_{average}$) is used to calculate the new system frequency (f_{sys}=$1/T_{average}$).

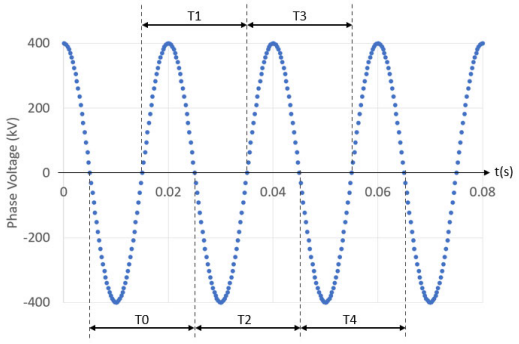

FIGURE 5. Data window for zero-crossing calculation.

Some quality criteria are considered to update the f_{sys} value. First, if the difference between a new period ($T_{average}$) and T_0 is above 90 μs, this new period is ignored. This condition avoids accounting fast phase variations in frequency calculation. Next, if the difference between the new frequency value and the current one is less than 5 mHz, f_{sys} is not updated to the new frequency value to avoid nonsignificant changes.

All the valid voltage signals are used to estimate the system frequency, making the algorithm more robust. This module considers a voltage channel valid if its RMS exceeds a validity threshold (set as 5% of the line nominal voltage). The system frequency provided by the algorithm is the average of the frequencies calculated in each of the phases.

fsys should be within the range [45 Hz-65 Hz]. In case fsys is out of this range, it is updated to the closer frequency limit, i.e., if f_{sys} is below 45 Hz, it will be set to 45 Hz. By contrast, if f_{sys} is above 65 Hz, it is updated to 65 Hz.

C. RESAMPLING MODULE AND GENERATION OF DATA-WINDOW

The first step for this module is a second-order low-pass Butterworth filter with a cutoff frequency of 700 Hz (called low pass filter 2 in Fig. 2) as anti-aliasing filter to reject higher harmonics [26]. The delay in the further calculations was estimated to be below 0.3 ms, which is considered acceptable compared with other delays in the system.

Next, the resampling period (p_{rem}) is calculated using the frequency provided by the *Frequency Tracking Module* (f_{sys}) with the following relationship:

$$p_{rem} = \frac{1}{f_{sys} \cdot N} \tag{3}$$

where N is the number of samples. In this study, 80 samples/cycle are used.

Once the resampling period is known, an array of time stamps (t') where the new samples are calculated is defined using Fig. 6 and (4). The time stamp of the first sample (t_1) is taken as a reference.

$$t' = \left[t_1, t_1 + p_{rem}, t_1 + 2 \cdot p_{rem}, \ldots, t_1 + N \cdot p_{rem}\right] \tag{4}$$

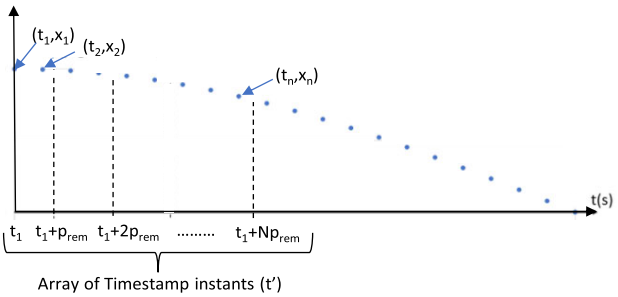

FIGURE 6. Timestamp calculation description.

The resampled data window is rebuilt from the reconstructed signals using the array of time stamps (t'). Newton's interpolation polynomial of degree 2 is used to carry out this task.

D. RMS VALUES CALCULATION AND FOURIER FILTER

The input of this module is the new data window resampled using the period of the grid frequency. The main calculations

of this module are the RMS and the Fast Fourier Transform (FFT) [27].

The RMS is used directly as the *SV-APM* output values and the FFT output is used for the last module calculations to obtain voltage and current channels: DC, magnitude, angle, magnitude to the fifth harmonic and symmetrical components.

III. LABORATORY TESTBENCH

This section describes the laboratory testbench used to check the performance of *SV-APM*. The laboratory includes an EPICS platform, a communications switch, and an RTDS [28] simulator including four giga-transceiver network communication version 2 (GTNETx2) cards and one giga-transceiver network communication (GTNET) card able to work with IEC61850 Sampled Values and GOOSE. All these elements are integrated into an infrastructure that can emulate and test any scenario in the grid.

Fig. 7 shows a diagram of the laboratory testbench. In this setup, the RTDS is used to model electrical power systems that interact with real equipment, such as testing control systems or electrical protection schemes, using Hardware in the Loop (HiL) simulations. Therefore, it is a very convenient setup to test EPICS platform services and algorithms before their implementation in the field. Examples of HiL tests can be found in [29], [30], and [31].

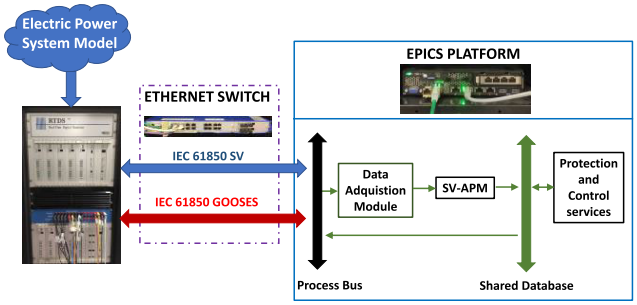

FIGURE 7. General diagram of laboratory testbench.

The RTDS allows the simulation of electrical power systems in real time. The GTNETx2 card can be programmed with the IEC61850 SV firmware (GTNETx2_SV) or with the IEC61850 GOOSE one (GTNETx2_GSE). Using GTNETx2_SV firmware, it is possible to convert signals, such as voltages and currents generated in real time, into IEC 61850 SV signals that can be subscribed by the EPICS platform. In this study, the standard IEC61850-9-2 LE [32] was used for SV publications made by the RTDS.

Using the GTNETx2_SV firmware, it is possible to subscribe to IEC 61850 SV signals published by the EPICS platform, which can send some feedback signals useful for analyzing the behavior of the service or algorithm under test.

Using the GTNETx2_GSE firmware, it is possible to publish GOOSE messages with the information needed by the service under test processed by EPICS, and with that firmware is also possible to subscribe to GOOSE messages published by the EPICS to complete the hardware in the loop (HiL) platform.

EPICS works as a generic platform where different algorithms can be developed and implemented using any programing language and deployed as containerized microservices. In this study C++ [33] has been selected. The resulting outputs of the algorithms are communicated via IEC 61850 GOOSE messages or IEC 61850 SV to the RTDS using a dedicated microservice (*SV-APM-OUT*) that executes the remedial actions over the simulated electrical power system.

To evaluate *SV-APM* performance, three microservices were needed: *i61svs*, *SV-APM* and *SV-APM-OUT*. For the operation of these tests only 3 cores were needed, one of them (*SV-APM-OUT*) not used in normal operation.

All the communications inside the laboratory testbench pass through an industrial Ethernet switch. An additional computer is used to program and configure all the elements inside the laboratory.

IV. DESCRIPTION OF THE TEST

This section summarizes the tests carried out to check the behavior of *SV-APM* modules under different scenarios. These tests can be classified as functional and performance tests. The aim of functional tests is to verify the operation of each *SV-APM* module. However, performance tests check if *SV-APM* fulfills the minimum quality criteria regarding time response to be used in a real environment.

For the execution and evaluation of all the tests, several scripts were developed in RSCAD. Table 2 makes a brief description of the tests carried out to evaluate *SV-APM* modules performance.

TABLE 2. Tests carried out to verify the behaviour of *sv-apm*.

SV-APM Module to be tested	Test description
Signal reconstruction module	Loss of packets, [34] Invalid signal quality Delays in communications Loss of time synchronization
Frequency tracking module	Slow and abrupt frequency variations Frequency ramps Voltage dips Phase jumps Voltage recovery with different frequency targets
Resampling and generation of data window module and RMS calculation and Fourier filter	Voltage and current phasors with harmonic content Voltage and current phasors without harmonic content
Performance test	Latency

The capabilities of EPICS platform in publishing IEC 61850 SV and GOOSE are used to close the loop with RTDS, analyze every variable under evaluation and check the maximum tolerable error associated.

Different criteria have been defined to consider the behavior of the module under study as suitable. To check the suitable EPICS performance, several manuals of commercial protection relays currently used in the transmission network have been consulted to establish the thresholds used in this study. These criteria are detailed below in each test type.

A. SIGNAL RECONSTRUCTION MODULE OPERATION TESTS

During these tests, it is evaluated if the data windows construction fulfills the following requirements:

- The *smpCnt* are correlatives without discontinuities.
- The voltage and current values provided by *SV-APM* correspond with the expected signals.
- The reconstruction of lost samples is correct.
- The behavior of the module blocking is correct, evaluating delays, time synchronization and quality.

To perform these evaluations, the *SV-APM* output values are compared with the provided by the RTDS (*SV-APM* input). Different thresholds bands are defined to pass tests. The next table summarizes these thresholds.

TABLE 3. Thresholds to evaluate voltages, currents, and *smpCnt*.

Signal	Threshold
V_A, V_B, V_C	$< 0.04\%$
I_A, I_B, I_C	$< 0.04\%$
smpCnt	$\pm$ 1 sample

B. FREQUENCY TRACKING MODULE OPERATION TESTS

During these tests, the frequency provided by the module is considered as suitable if the following conditions are fulfilled:

- The maximum frequency error is less than ± 10 mHz.
- The frequency value is not updated if the frequency variation is less than 5 mHz.

To perform these evaluations, the frequency of the SV-APM output signals is compared with the one provided by the RTDS (SV-APM input), verifying that it satisfies the requirements.

C. RESAMPLING AND GENERATION OF DATA WINDOW MODULE, RMS CALCULATION AND FOURIER FILTER OPERATION TESTS

During these tests, it is evaluated that:

- The maximum error in voltage magnitude at fundamental frequency is less than $\pm 0.2\%$.
- The maximum error in current magnitude at fundamental frequency is less than $\pm 0.2\%$.
- The maximum error in angles between voltages at fundamental frequency is less than $\pm 0.2°$.
- The maximum error in angles between currents at fundamental frequency is less than $\pm 0.2°$.
- The maximum error in angles between voltage and current at fundamental frequency is less than $\pm 0.2°$.
- The maximum error in the magnitude of voltage harmonics and current harmonics is less than $\pm 0.5\%$.
- The maximum error in the magnitudes of symmetrical components of voltage and currents is less than $\pm 0.2\%$.
- The maximum error in the angles of symmetrical components of voltage and currents is less than $\pm 0.2°$.

To perform these evaluations, the *SV-APM* output values are compared with the ones provided by the RTDS (*SV-APM* input), verifying that the defined tolerances are fulfilled.

D. PERFORMANCE TESTS

The aim of these tests is to calculate the time used by the SV-APM to carry out its operation. High time-delay values, i.e., high latency values, may impact on the protection systems operation producing delays in the protection trip. According to IEC61850-5 standard [35], the required time by the frames to generate (coding and sending), transmit, receive and decoding must be less than 3 ms. Then, the latency values measured during tests will be compared with this threshold to validate the *SV-APM* operation.

For this task, the RTDS system has been used to take advantage of its real-time capabilities. The procedure used to measure the latency is described in the Fig. 8 and can summarized as follows. To explain this process, we will follow the steps of a sample from its generation by the RTDS up to latency calculation. That sample is generated by RTDS using the box indicated in yellow (*SV_codification*) and sent from RTDS to the EPICS platform through a communication switch, as indicated by the red arrows. The time t_{C_A} represents the delay from the generation of the sample until it reaches the platform. Once the sample arrives, it is processed by the *i61svs* and *SV_APM* modules. The t_p variable represents the time spent in this process. After processing the sample, it is returned to the RTDS as indicated by the blue arrows and decoded taking time t_{C_B}. External software and the publication of UDP messages by RTDS are used to calculate the communication and processing total delay of every sample, as shown on the left side of the figure. These UDP messages include information about *smpCnt* and *timestamp* that allow calculating the latency of the entire process. RTDS obtains the t*imestamp* information from an external GPS synchronization signal.

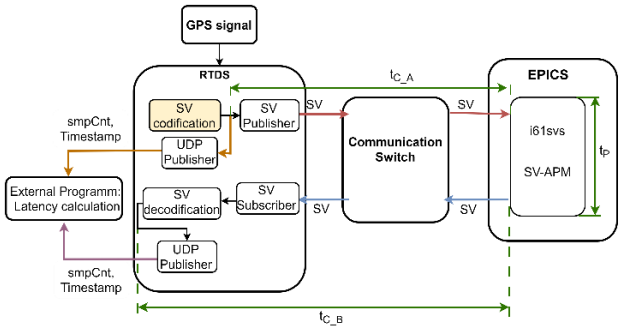

FIGURE 8. Latency test scheme.

With this information, the external program compares the *timestamp* of the samples with the same *smpCnt* and calculates an upper limit of the *SV-APM* latency. The total latency ($t_{C\_A}+t_{C\_B}+t_p$) is measured for all the values calculated over more than three days to characterize its statistical distribution.

The tests have been performed in the general purpose (non-Real Time) Linux server presented earlier. The following measures were taken to isolate the working CPUs and enhance the latency behavior: the *i61svs* service was compiled and executed directly without virtualization and all the tasks involved in the SV processing are executed in cores excluded for interrupts.

To make the test realistic, *SV-APM* was configured to handle eight sampled value streams with a single instance of the microservice on a single core.

Three of them were generated by RTDS. The five others were simulated inside the EPICS server, writing their values directly in the SV *Shared Database*. Therefore, *SV-APM* managed eight streams of three-phase data with a single core in these tests. It should be noted that *SV-APM* can be instantiated repeatedly on different cores to provide more scalability to EPICS due to the concurrent nature of *SV-APM* instances and *Shared Database*.

V. TEST RESULTS

In this section, the *SV-APM* operation is evaluated in the different scenarios described in Section II.

As it is shown in Table 4, 1915 functional tests were carried out to check *SV-APM* performance and 3 days of simulation were used to check latency. Next sections describe the most representative results of these test campaign.

TABLE 4. Functional and performance tests.

SV-APM Modules	*SV-APM* Test	Tests
Functional tests	Signal reconstruction module	15 tests
	Frequency tracking module	405 tests
	Resampling and generation of data window module	1495 tests
	RMS calculation and Fourier filter	
Performance	Latency	3 days

A. FUNCTIONAL TEST RESULTS

The oscillography presented in Fig. 9 shows the *Signal reconstruction module* operation when a time delay of 750 μs is applied to the input signal. In this scenario, the *SV-APM* module must be blocked. This behavior is shown by means of the sampled phase A current (*IA_APM_in*), which is sent by the RTDS to the *SV-APM* module, and the one provided by *SV-APM* module (*IA_APM_out*) to the process bus. Furthermore, the *smpCnt* of each sample is also represented (*SMPCNT_APM_in* and *SMPCNT_APM_out*, respectively). When the delay happens, the *SV-APM* module is blocked and

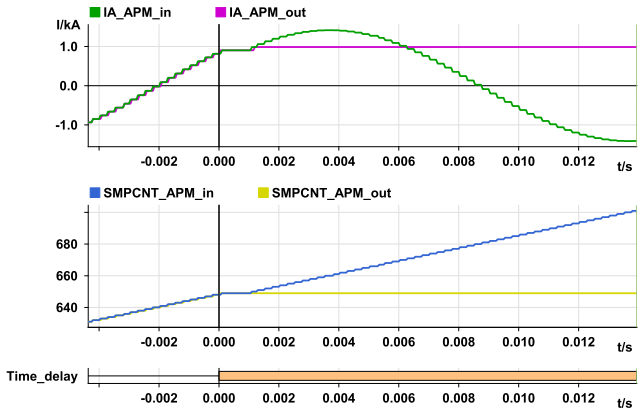

FIGURE 9. Signal reconstruction module operation, when a time delay of 750 μs is applied.

therefore, the *smpCnt* (yellow line) and the output current (pink line) values are held.

From Fig. 10 to Fig. 13, the most representative results of the performed tests to evaluate the behavior of *Frequency measurement module*are shown. The figures show the three-phase voltage analog signal (VA, VB, and VC) sent by the RTDS to the *SV-APM* module to estimate the frequency. Furthermore, the real frequency of the voltage signal (*f_expected*) and the estimated by the *SV_APM* module (*f_SV_APM*) are also shown.

In the case of Fig. 10, the performance of the *SV-APM* module is tested when a voltage signal with the harmonic content described in [36] is used. By contrast, Fig. 11 shows the *SV-APM* response when a voltage dip depth of 0.95 p.u. is applied. From these figures, it is concluded that *SV-APM* can correctly estimate the frequency of the system with a maximum deviation of 1 mHz.

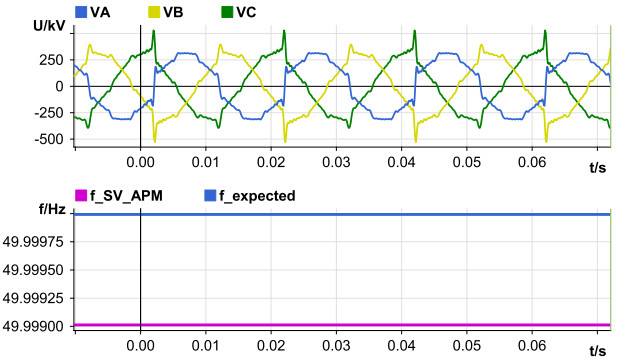

FIGURE 10. Frequency module operation under three phase voltage with harmonics content according to Table 4.

Fig. 12 and Fig. 13 show the *Frequency measurement module* response when a sudden frequency change occurs. Fig. 12 presents the *SV-APM* response when the frequency amplitude after fault conditions should reach a frequency value (50.4 Hz) different from the one before to the disturbance (50 Hz). From the figure, it can be concluded that

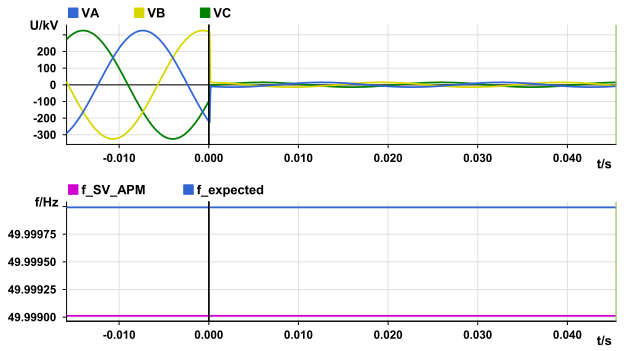

FIGURE 11. Frequency module operation under three-phase voltage sag of 0.95 p.u. for 5 seconds.

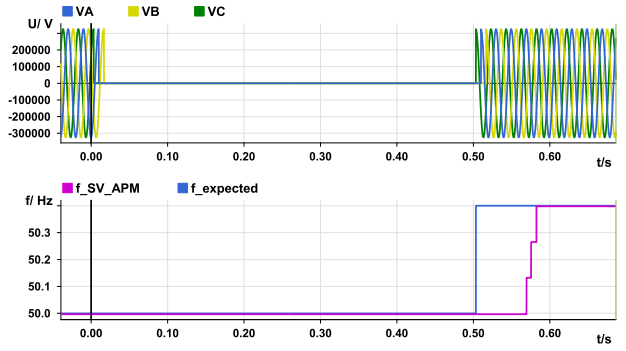

FIGURE 12. Frequency module operation under three phase voltage sag of 1 p.u. for 500 ms and recovering the voltage with different frequency (50.4 Hz).

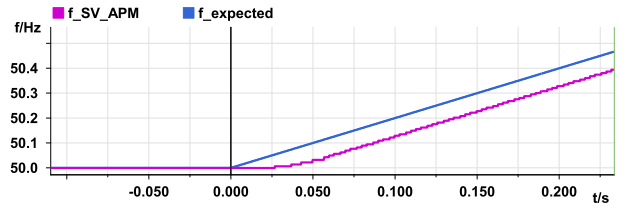

FIGURE 13. Frequency measurement during a test with rate of change of 2 Hz/s.

the *SV-APM* recovers the frequency up to 50.4 Hz, with a maximum time delay of 80 ms. Furthermore, the figure shows a constant frequency of 50 Hz during the fault. It is due to the quality criterion used by the *Frequency measuring module*that checks if the voltages exceed a specific voltage threshold (5% of rated voltage). This criterion is not satisfied in the fault shown in Fig. 12, and the frequency system value is not updated, maintaining the pre-fault frequency value.

Moreover, the frequency tracking module has been tested considering a rate of change of 2 Hz/s to check if the calculation is suitable in these scenarios. From Fig. 13 it is concluded that the *SV-APM* recovers the frequency but with a delay close to 80 ms. In both cases, the time delay obtained is in line with the results obtained by traditional protection equipment.

Finally, Fig. 14 shows as an example, a test result used to evaluate symmetrical component calculations carried out by RMS and Fourier module of *SV-APM*. The figure shows the symmetrical current magnitude in positive, negative and zero-sequence calculated by *SV-APM* (I1_SV_APM, I2_SV_APM and I0_SV_APM, respectively) and the theoretical ones (I1_expected, I2_ expected and I0_ expected). Furthermore, the control bits used to indicate that the maximum error detected exceed the threshold defined in section IV ($\pm 0.2°$) are also shown (I0_mag_Error_check, I1_mag_ Error_check and I2mag_ Error_check). As it is shown in the figure, the error threshold is not exceeded because the control bits are not activated. The same behaviour is observed for all tests performed during the evaluation stage.

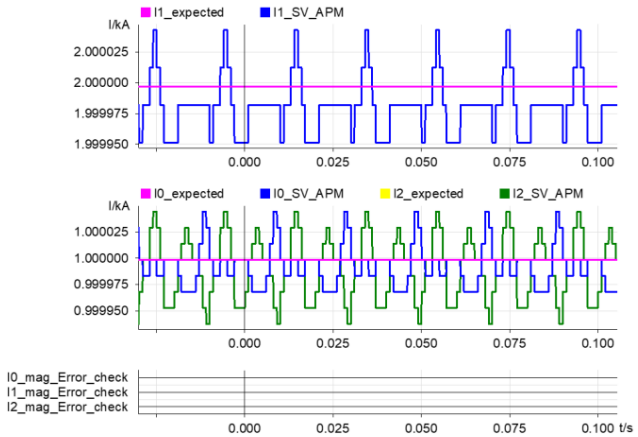

FIGURE 14. Test to evaluate RMS and Fourier module operation: symmetrical components calculation.

B. PERFORMANCE AND LATENCY INTRODUCED BY SV-APM TEST RESULTS

The distribution of the measured latency can be seen in Fig. 15. The probability of occurrence of each latency value is indicated on the vertical axis on a logarithmic scale in percentage. The minimum value that appears in the figure is 10^{-7}%. Considering the total data analyzed, values below this probability indicate that there are no samples with this latency.

As can be observed in the Fig. 15, more than 99% of the values are calculated and transmitted in less than 250μs. Additionally, the measured worst case is 1.1 ms with a very low probability ($\sim 10^{-6}$%). Then, the latency values fulfill the IEC61850-5 standard requirements described in Section IV (latency less than 3 ms).

The events with 1.1 ms of latency were studied individually and all of them followed the same pattern. An example can be seen in Fig. 16, where the dots represent the latency value measured in every sample evaluated. The high latency event occurs in time instant of 0.639 s and it is an isolated case and

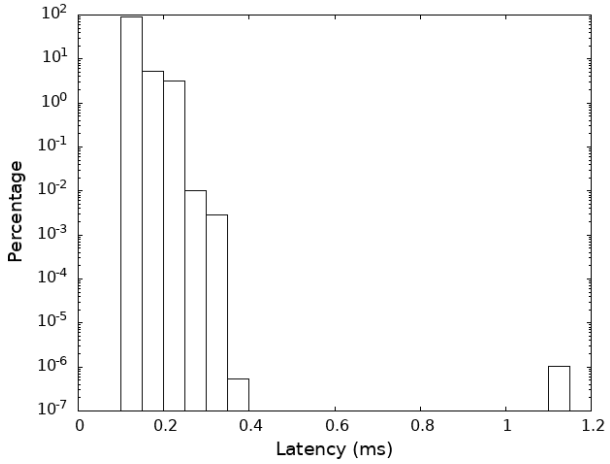

FIGURE 15. Latency measured.

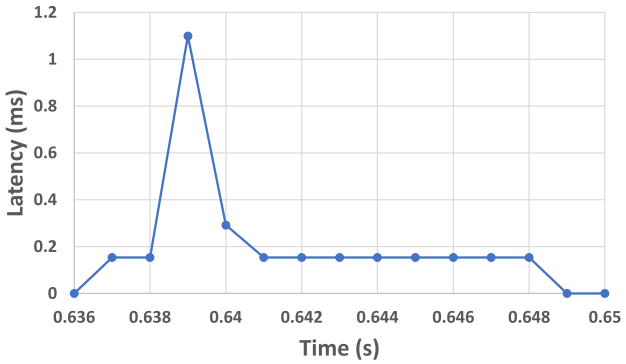

FIGURE 16. Detail of the latency measured in the worst case.

the latency measurement is recovered almost immediately, with a minor impact in the latency of the next *SV-APM* value.

Therefore, from this test it can also be concluded that *SV-APM* can manage eight streams of three-phase data with a single core, with the maximum latency of 1.1 ms measured during tests.

VI. CONCLUSION

In the present work, the feasibility of implementing an analog signal processing module based on IEC61850 SV (*SV-APM*) is demonstrated. The module is implemented in a generic EPICS hardware platform, whose purpose is to execute protection and control services in a centralized manner in digital substations. The proposed solution is flexible, scalable and does not depend on a specific hardware or software vendor solution. A detailed explanation about the steps needed to implement the digital processing module is provided.

From the functional and performance tests carried out on the *SV-APM* module, it is concluded that its outputs satisfactorily meet all the time response and accuracy requirements defined during its development. Therefore, these outputs can be used by the control and protection services of EPICS or other software-based platforms. The *SV-APM* module was subsequently tested as part of the whole EPICS platform acting as a centralized P&C system, interacting with two different protection microservices (differential and distance protection). From these tests, it was concluded that the response times are comparable to commercial non-centralized solutions [37].

As the next steps of this work, it is proposed to evaluate the scalability of the service using several SV sources by executing several instances of the *SV-APM* service and to evaluate the latencies associated in this scenario with greater computational demands for the platform.

REFERENCES

[1] V. Telukunta, J. Pradhan, A. Agrawal, M. Singh, and S. G. Srivani, "Protection challenges under bulk penetration of renewable energy resources in power systems: A review," *CSEE J. Power Energy Syst.*, vol. 3, no. 4, pp. 365–379, Dec. 2017, doi: 10.17775/CSEEJPES.2017.00030.

[2] Y. Fang, K. Jia, Z. Yang, Y. Li, and T. Bi, "Impact of inverter-interfaced renewable energy generators on distance protection and an improved scheme," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 7078–7088, Sep. 2019, doi: 10.1109/TIE.2018.2873521.

[3] R. Štefko, Z. Conka, J. Kurimský, and M. Kolcun, "Problems of protection of industrial networks with a high share of renewable energy sources," in *Proc. IEEE 3rd Int. Conf. Workshop Óbuda Electr. Power Eng. (CANDO-EPE)*, Nov. 2020, pp. 79–84, doi: 10.1109/CANDO-EPE51100.2020.9337771.

[4] J. C. Quispe and E. Orduña, "Transmission line protection challenges influenced by inverter-based resources: A review," *Protection Control Mod. Power Syst.*, vol. 7, no. 1, p. 28, Jul. 2022, doi: 10.1186/s41601-022-00249-8.

[5] J. Ma, Y. Qiu, Y. Li, W. Zhang, Z. Song, and J. S. Thorp, "Research on the impact of DFIG virtual inertia control on power system small-signal stability considering the phase-locked loop," *IEEE Trans. Power Syst.*, vol. 32, no. 3, pp. 2094–2105, May 2017, doi: 10.1109/TPWRS.2016.2594781.

[6] C. Yongning, L. Yan, W. Zhen, L. Zhen, L. Hongzhi, and Z. Zhankui, "The characteristics and challenge on large-scale renewable energy grid integration," in *Proc. IEEE Innov. Smart Grid Technol.-Asia*, May 2019, pp. 1393–1398, doi: 10.1109/ISGT-Asia.2019.8881344.

[7] H. Holttinen, J. Kiviluoma, D. Flynn, J. C. Smith, A. Orths, P. B. Eriksen, N. Cutululis, L. Söder, A. Estanqueiro, J. MacDowell, A. Tuohy, T. K. Vrana, and M. O'Malley, "System impact studies for near 100% renewable energy systems dominated by inverter based variable generation," *IEEE Trans. Power Syst.*, vol. 37, no. 4, pp. 3249–3258, Jul. 2022, doi: 10.1109/TPWRS.2020.3034924.

[8] H. Marzooghi, M. Garmroodi, G. Verbic, A. S. Ahmadyar, R. Liu, and D. J. Hill, "Scenario and sensitivity based stability analysis of the high renewable future grid," *IEEE Trans. Power Syst.*, vol. 37, no. 4, pp. 3238–3248, Jul. 2022, doi: 10.1109/TPWRS.2020.2999070.

[9] X. Liang, "Emerging power quality challenges due to integration of renewable energy sources," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 855–866, Mar. 2017, doi: 10.1109/TIA.2016.2626253.

[10] *Renewable Energy Statistics*. Accessed: Feb. 13, 2023. [Online]. Available: https://ec.europa.eu/eurostat/statistics-explained/index.php?title=Renewable_energy_statistics

[11] IEEE Power System Relaying Committee. (Dec. 2015). *Centralized Substation Protection and Control WG K15*. [Online]. Available: https://resourcecenter.ieee-pes.org/publications/technical-reports/PESTR0055.html

[12] B. de Oliveira e Sousa, J. Starck, and J. Valtari, "Viability assessment for centralised protection and control system architectures in medium voltage (MV) substations," *CIRED-Open Access Proc. J.*, vol. 2017, no. 1, pp. 1531–1534, Oct. 2017, doi: 10.1049/oap-cired.2017.0276.

[13] C. P. Teoh, R. Hunt, and G. Lloyd, "A centralized protection and control system using a well proven transmission class protection relay," in *Proc. 15th Int. Conf. Develop. Power Syst. Protection*, Mar. 2020, pp. 1–6, doi: 10.1049/cp.2020.0088.

[14] R. Wójtowicz, R. Kowalik, D. D. Rasolomampionona, and K. Kurek, "Virtualization of protection systems–tests performed on a large environment based on data center solutions," *IEEE Trans. Power Del.*, vol. 37, no. 4, pp. 3401–3411, Aug. 2022, doi: 10.1109/TPWRD.2021.3128993.

[15] J. D. Cardoza, "Market availability and testing of centralized protection and control systems," M.S. thesis, Darmstadt Univ. Appl. Sci., Darmstadt, Germany, 2021. [Online]. Available: https://doi.org/10.48444/h_docs-pub-272

[16] N. Kabbara, M. O. N. Belaid, M. Gibescu, L. R. Camargo, J. Cantenot, T. Coste, V. Audebert, and H. Morais, "Towards software-defined protection, automation, and control in power systems: Concepts, state of the art, and future challenges," *Energies*, vol. 15, no. 24, p. 9362, Dec. 2022, doi: 10.3390/en15249362.

[17] M. Nunes. *Substation Protection and Control Virtualization Revolution*. Presented at the Protection, Automation and Control World (PACWORLD). Accessed: Mar. 24, 2023. [Online]. Available: https://www.pacw.org/substation-protection-and-control-virtualization-revolution

[18] D. Samara-Rubio. *Virtual Protection Relay: A Paradigm Shift in Power System Protection*. Accessed: Mar. 24, 2023. [Online]. Available: https://www.intel.com/content/www/us/en/energy/resources/virtual-production-relay-whitepaper.html

[19] F. Hohn, J. Wang, and L. Nordström, "Design of a distributed signal processing unit for transmission line protection in a centralized substation protection architecture," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2018, pp. 138–144, doi: 10.1109/IECON.2018.8591767.

[20] ELEWIT. *Plataforma EPICS: Implementación Flexible y Escalable de Sistemas Automáticos*. Accessed: Jul. 8, 2022. [Online]. Available: https://www.elewit.ventures/index.php/es/actualidad/plataforma-epics-implementacion-flexible-y-escalable-de-sistemas-automaticos

[21] *Communication Networks and Systems for Power Utility Automation—Part 2: Glossary*, Standard IEC 61850-2:2019, International Standarization Organization, 2019.

[22] *Implementation Guideline for Digital Interface to Instrument Transformers using IEC 61850-9-2*, UCA International Users Group, Standard IEC 61850-9-2LE, 2012. [Online]. Available: http://www.ucainternational.org

[23] J. Verbeke and R. Cools, "The Newton–Raphson method," *Int. J. Math. Educ. Sci. Technol.*, vol. 26, no. 2, pp. 177–193, 1995.

[24] M. Aghasi and A. Jalilian, "Removal of decaying DC component in current signal using a novel estimation algorithm," Presented at the IPAPS, 2010.

[25] R. Cimadevilla, R. Quintanilla, and S. Ward, "Adapting protection to frequency changes," Presented at the 32nd Annu. Western Protective Relay Conf., Spokane, WA, USA, 2005.

[26] S. E. Zocholl and G. Benmouyal, "How microprocessor relays respond to harmonics, saturation, and other wave distortions," Presented at the 24th Annu. Western Protective Relay Conf., Spokane, WA, USA, Oct. 1997.

[27] P. Duhamel and M. Vetterli, "Fast Fourier transforms: A tutorial review and a state of the art," *Signal Process.*, vol. 19, no. 4, pp. 259–299, 1990.

[28] *RTDS Technologies*. Accessed: Sep. 14, 2022. [Online]. Available: https://www.rtds.com/

[29] RTDS Technologies. *Testing Centralized Automation for Digital Substations at ABB*. Accessed: Sep. 14, 2022. [Online]. Available: https://www.rtds.com/case-studies/testing-centralized-automation-digital-substations-abb/

[30] A. A. P. Hurtado, "Laboratory-scaled DEMO possibilities for testing WAMPAC solutions before field implementation," in *Proc. IEEE Madrid PowerTech*, Jun. 2021, pp. 1–6, doi: 10.1109/PowerTech46648.2021.9495064.

[31] A. A. P. Hurtado, E. M. Carrasco, M. T. V. Martínez, and J. Saldana, "Application of IIA method and virtual bus theory for backup protection of a zone using PMU data in a WAMPAC system," *Energies*, vol. 15, no. 9, p. 3470, May 2022, doi: 10.3390/en15093470.

[32] *Communication Networks and Systems in Substations—Part 9–2: Specific Communication Service Mapping (SCSM)—Sampled Values Over ISO/IEC 8802-3*, Standard IEC 61850-9-2:2011+ADM1:2020, 2020.

[33] R. Baker, *Object Oriented Programming in C++: C++ Object Oriented Programming & Features of OOP's*. Chicago, IL, USA: Independently Published, 2020.

[34] K. Sidwall and P. Forsyth, "A review of recent best practices in the development of real-time power system simulators from a simulator manufacturer's perspective," *Energies*, vol. 15, no. 3, p. 1111, Feb. 2022, doi: 10.3390/en15031111.

[35] *Communication Networks and Systems for Power Utility Automation—Part 5: Communication Requirements for Functions and Device Models*, Standard IEC 61850-5:2013, 2013.

[36] *Electromagnetic Compatibility (EMC)—Part 2–4: Environment—Compatibility Levels in Industrial Plants for Low-Frequency Conducted Disturbances*, Standard IEC 61000-2-4:2002, 2002.

[37] M. T. V. Martinez, "Description of an edge computing solution to be used in digital substations," presented at the ISGT IEEE Europe Conf., Grenoble, Grenoble, Oct. 2023.

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