Multi-Phase PFC Rectifier and Modulation Strategies for Domestic Induction Heating Applications

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***Abstract*—Domestic induction heating appliances have improved the final user experience due to the advantages that this technology offers, such as flexibility, fast heating, cleanness and safety. Currently, these appliances are implemented using several isolated electronic boards to be able to be powered from one or several mains phases, enabling its use in regions with different connections. In order to enhance this approach, a multi-phase Power Factor Correction (PFC) rectifier is proposed, improving significantly induction heating cookers. The topology is described, and a wide variety of modulation strategies are presented and analyzed, discussing their main advantages and disadvantages according to the conduction mode, operating frequency, switching mode, and control strategy. In order to validate this proposal, a 11-kW and up-to-3-phase high power-density converter for domestic IH applications is implemented and experimentally analyzed, including its main waveforms and efficiency. Finally, a comparative evaluation is performed to enable the selection of the optimum modulation strategy for each specific application.**

***Index terms*—Induction Heating, Resonant Power Conversion, Home Appliances, Power Factor Corrector, PFC rectifier, multi-phase, Zero Voltage Switching, Modulation Strategies.**

I. Introduction

Domestic induction heating (IH) featuring flexible cooking surfaces has the advantage of being able to use any pan or pot, regardless the selected size, shape, or position [1]. This technology improves significantly the final user experience due to the use of bigger coils with several concentric windings or fully active surfaces (Fig. 1) [2-4]. The design specifications of this technology are usually more restrictive because of the control constraints [5-7], higher output power, higher efficiency, the required power density to fit the electronic system into a built-in implementation, EMC restrictions, and, last but not least, the cost [8, 9]. In the past, the use of Power Factor Correction (PFC) rectifiers has been proposed in order to partially overcome these limitations and improve the user performance of modern IH appliances [10-12]. Additional efforts have been performed to reach high-efficiency converters [13-15], cost-effective measurement systems [16], or sensing applications [17].

Currently, IH cooktops are usually composed of two isolated electronic boards to be powered from two mains phases in certain regions, where the maximum phase current in domestic installations is limited to 16 A. However, there are different installation limitations in other regions where only a single-phase mains connection exists, but limited to 25 A, or areas where three-phase mains connections can be used.

Fig. 1. Flexible cooking surface using a front-end multi-phase converter to be powered from different single/multi-phase mains connections.

In this context, developing a front-end stage that allows merging different mains phases in a common bus voltage has been identified as a key research line [18]. More specifically, a multi-phase PFC rectifier provides significant advantages to domestic IH [19, 20] in comparison with classical domestic IH [1, 21]. Firstly, higher power can be delivered to the pots, e.g. typically 3.6 kW systems can be easily rescaled to 11 kW, decreasing significantly the heating times in bigger pots. EMC issues are isolated from the IH design, decreasing the filter size and avoiding the use of complex jitter strategies when non-linear loads are powered [21]. The control hardware can be also simplified, i.e. a single control unit is able to control both the PFC stage and the multi-phase outputs, removing isolated measurements and auxiliary power supplies for each phase.

Secondly, the IH system control is improved because of the variable bus voltage, allowing an easier and more accurate power control in several IH load scenarios, enabling also the operation closer to the resonant frequencies, improving the IH inverter efficiency. Furthermore, power coupling issues between different mains phases when multiple inductors are activated in multi-coil IH systems are avoided because a single inductor can be powered from several mains phases.

Finally, the higher the bus voltage is, the lower the required current through the switching devices and coils, decreasing the conduction losses. The inherent higher and low-ripple voltage of the proposed systems enables also a better usage of the switching devices, leading to potential cost reductions in the inverter stage. All these benefits motivate and justify the research and proposal of a multi-phase PFC stage.

Consequently, the main contribution of this paper is the implementation of a multi-phase PFC rectifier for a novel domestic IH application, and the proposal and analysis of different modulation strategies for its control. Besides, a discussion and a comparison are finally provided to highlight the advantages and drawbacks of each modulation strategy with regard to the switching-devices stress, boost-inductance stress, and the efficiency. The remainder of this paper is organized as follows. In Section II, a 3-phase topology with a 4-wire connection is presented. It can operate using 1, 2, or 3 mains phases, providing higher versatility and enabling its use in most regions due to its high compatibility. A full description of the topology and its analysis is provided. Section III introduces and analyzes the modulation strategies of the proposed rectifier including the control strategies, waveforms, and a brief description of their main advantages. It allows optimizing the converter according to switching device considerations, acoustic noise considerations in IH applications introducing fixed frequency strategies, optimizing the boost inductance size, or improving the converter efficiency. In Section IV a 11-kW 3-phase high power-density converter for domestic IH applications is designed and implemented, improving significantly the state-of-the-art 3.6-kW converters. The main experimental waveforms are shown, and the experimental efficiency is measured. Besides, a multi-variable comparative evaluation of the modulation strategies is provided to highlight their main advantages and disadvantages, and to ease their selection for each specific application. Finally, Section V summarizes the main conclusions of this paper.

II. Multi-Phase PFC Rectifier

A. Topology

In order to achieve the aims of this paper, controlled rectifiers are essential because of the smaller total harmonic distortion (THD) and the higher power density achievable at the cost of a more complex control [22-24]. Besides, boost topologies are specially interesting in the IH field because they allow improving the efficiency and the control strategy in the downstream IH inverter. In this paper, a multi-phase PFC rectifier is proposed to implement this front-end stage (Fig. 2). In this way, the different mains phases are joined in a common DC bus voltage, assuring a high power factor (PF) and a low THD of the phase currents [25-27].

The proposed topology is composed of (n+1) half-bridge branches, being n the maximum phase number. Each half-bridge branch is composed of two switching devices implemented with MOSFETs, $S_{h,i}$ on the high side, and $S_{l,i}$ on the low side, $i \in [0, n]$. The boost inductance, L_i, is short-circuited with the mains phase voltage, v_i, $i \in [1, n]$, the voltage of middle point of the split bus capacitor, v_0, and the bus voltage, v_b, to control the mains phase current, i_i. A filter composed of a filter inductance, $L_{f,i}$, and a filter capacitor, $C_{f,i}$, supplies the medium frequency currents, removing the high frequency ripple of the boost inductance current, $i_{L,i}$. Besides, the split capacitor, C_b, filters the bus voltage. The presented topology can work with 1, 2, or n activated phases. The additional half-bridge branch (n+1) assures that the split capacitor is well-balanced using the balancing inductance, L_0, and provides a return path to the mains phase current when then mains connection is not balanced, i.e. single-phase or 2-phase connections. The bus voltage, v_b, is the output of the converter used to power downstream converters, e.g. IH inverters.

B. Analytical description

The phase peak voltage, $v_{i,p}$, must fulfill the below equations to avoid uncontrolled current flowing through the antiparallel diodes of the switches, assuring the converter controllability.

$$v_{i,p} < v_0. \tag{1}$$

$$v_{i,p} < v_b - v_0. \tag{2}$$

The balancing branch is modulated at frequency, $f_{sw,0}$, and duty cycle, D_0, to get a proper voltage in the middle point of the split bus capacitor.

In order to assure a smooth phase current, i_i, the operating frequency of the switching devices, $f_{sw,i}$, is higher than the filter cutoff frequency, $f_{c,i}$, and this is higher than the mains

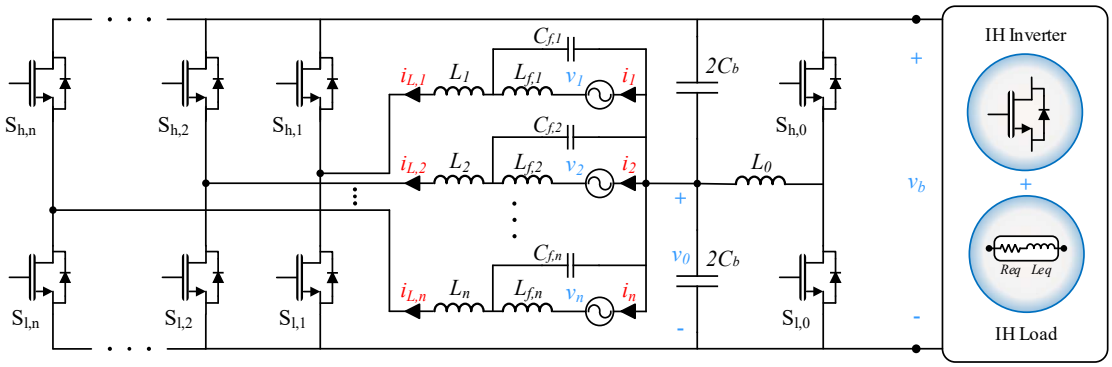


Fig. 2. Topology of a multi-phase PFC rectifier with n phases based on the boost topology.

frequency, $f_{ac,i}$,

$$f_{sw,i} >> f_{c,i} >> f_{ac,i}. \quad (3)$$

Besides, this assumption allows disregarding the filtering components, $L_{f,i}$ and $C_{f,i}$, simplifying the circuital analysis.

The boost inductance voltage, $v_{L,i}$, can be defined according the state of the switching devices as

$$v_{L,i} = \begin{cases} v_i + v_0, & 0 \le t < \dfrac{D_i}{f_{sw,i}} \\ v_i + v_0 - v_b, & \dfrac{D_i}{f_{sw,i}} \le t < \dfrac{1}{f_{sw,i}} \end{cases}, \quad (4)$$

when (1), (2), and (3) are fulfilled. The low-side switching device is the first one to be activated. Thereby, the duty cycle, D_i, is calculated as

$$D_i = 1 - \frac{v_0 + v_i}{v_b}. \quad (5)$$

In this way, the current through the boost inductance, $i_{L,i}$, and therefore the mains phase current, i_i, can be controlled. It can be appreciated in (4) that this topology with split bus capacitor configuration behaves as a bridge topology. As a result, modulation strategies used for controlling bridge topologies can be applied in this case.

III. Modulation Strategies

Five different modulation strategies have been considered (Fig. 3), and they are classified according to three main parameters: the conduction mode, the switching mode, and the switching-frequency variation [18, 20].

The conduction mode is divided in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The switching modes can be classified into Zero Voltage Switching (ZVS) and Hard Switching (HS) modes. In the ZVS mode, the antiparallel diode is previously activated because the inductance current always crosses through zero, changing the current direction before the switch activation. Consequently, the turn-on transition is performed with null voltage, avoiding the turn-on losses. This condition is not fulfilled is HS mode.

Lastly, the switching frequency classification includes Fixed Frequency (FF) and Variable Frequency (VF). The FF modulation strategies avoid frequency changes along the mains cycle in contrast to the VF modulation strategies. The implemented frequency mode greatly depends on the final application, and it determines the overall performance of the topology. On the one hand, in domestic IH applications, a fixed frequency may be mandatory in order to avoid the acoustic noise generated by the intermodulation frequencies between the IH inverter and the PFC [28]. Besides, it allows a better optimization of the filter design. On the other hand, working with variable frequency modulations allows higher efficiencies and distributing the harmonics currents in a wide frequency range, decreasing EMC issues. The main advantages and disadvantages of each modulation strategy according to the aforementioned classification are explained below.

The Zero-Voltage-Switching Fixed-Frequency Continuous-Conduction Mode (ZVS FF CCM) gets ZVS at constant frequency. The main drawback is the high ripple of the current is necessary to perform it. This ripple leads to increased rms currents in the boost inductance, the switching devices, and the capacitors, increasing the conduction losses. In the same way, the turn-off current of the switching devices is also increased, increasing the overall switching losses. Furthermore, the bus voltage, the mains phase voltage, and the mains phase current must be measured to perform a closed-loop control. However, this control assures a high PF and low THD.

The Hard-Switching Fixed-Frequency Continuous-Conduction Mode (HS FF CCM) gets a low ripple, almost negligible when compared with the previous modulation strategy. The control is performed similarly, getting a high PF and THD. The main disadvantage is that the switching losses are penalized due to the fact that the turn-on transition is done with not null voltage.

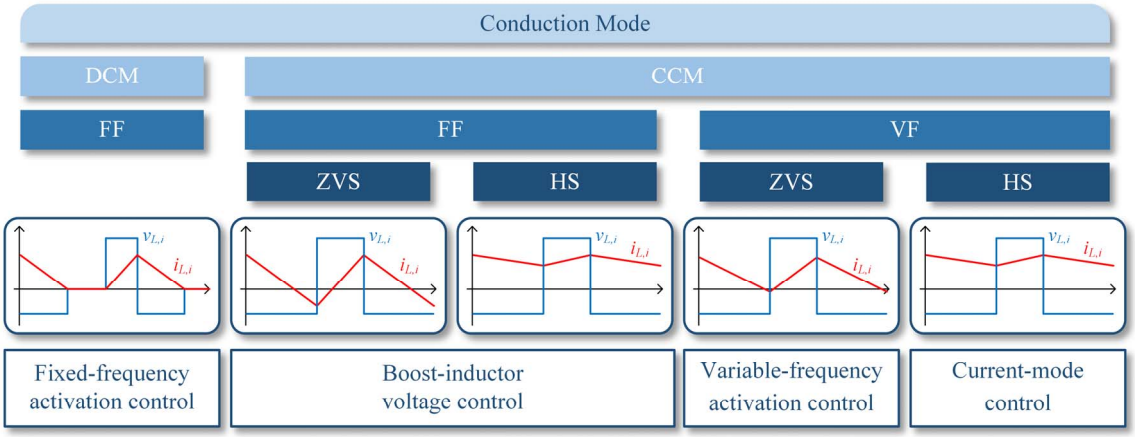


Fig. 3. Modulation strategy classification of the multi-phase PFC rectifier indicating, from top to bottom: the conduction mode, Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM); the frequency mode, Fixed Frequency (FF) or Variable Frequency (VF); the switching mode, Zero Voltage Switching (ZVS) or Hard Switching (HS); the boost inductance waveforms; and the control implemented to perform each modulation strategy.

The Zero-Voltage-Switching Variable-Frequency Continuous-Conduction Mode (ZVS VF CCM) performs ZVS with a lower current ripple than the first case. Moreover, the input current is not necessary to be measured to perform a closed-loop control. On the contrary, the zero cross of the boost inductance current must be measured, in order to calculate the modulation parameters along the measures of the bus voltage and the mains phase voltage. The main drawback is that the switching frequency is variable, and the frequency swing is very wide.

The Hard-Switching Variable-Frequency Continuous-Conduction Mode (HS VF CCM) takes the advantage of the control is performed using a current-mode control. In this way, only the boost inductance current must be measured, decreasing the control cost and achieving a good performance. On the other hand, the frequency is also variable, although the frequency swing is lower than in the above case. Besides, the turn-on losses are not null due to the hard switching.

Finally, the Fixed-Frequency Discontinuous-Conduction Mode (FF DCM) performs the control using a modulation parameter obtained from the measures of the bus voltage and the mains phase voltage. Therefore, the control cost is decreased because the current is not measured. Besides, the frequency is constant. The main disadvantage is the high current ripple, but however, it is lower than in the first case. Additionally, the reverse recovery losses of antiparallel diodes are not null.

All these modulation strategies can be applied to the proposed topology with different trade-offs between performance, cost and complexity. Their optimum selection will be later discussed together with the obtained experimental results. The main waveforms of the boost inductor of the *i*-branch of the multi-phase PFC converter and the configuration sequence using a ZVS modulation strategy are shown in Fig. 4 and Fig. 5, respectively. In order to simplify the analysis, a single branch powering the bus has been considered, and it is assumed that the bus capacitors are high enough to assume a constant voltage during a switching period, being able to disregard the effect of the balancing branch. The IH inverter is modeled as a resistive load, R_o.

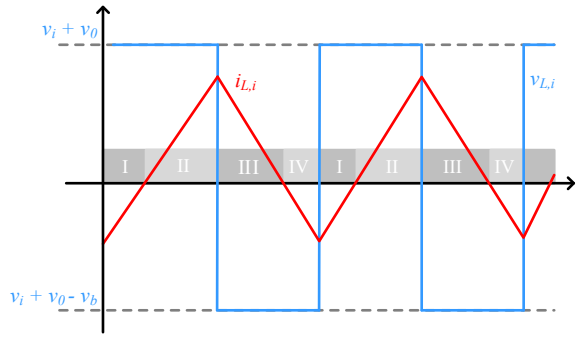


Fig. 4. Inductor waveforms and activation states of the *i*-branch of the multi-phase PFC converter.

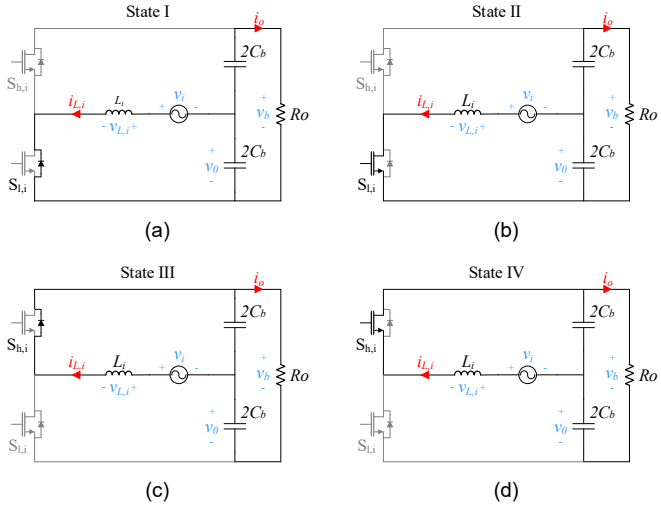


Fig. 5. Configuration sequence of the *i*-branch of the multi-phase PFC converter powering a resistive load, R_o: (a) state I, (b) state II, (c) state III, and finally, (d) state IV.

IV. Implementation and Experimental Results

A. Prototype implementation

In order to experimentally verify the proposed multi-phase PFC rectifier and its modulation strategies, a versatile 11-kW and 2-dm^3 platform with up to three mains phases, i.e. n = 3, has been designed and implemented. The prototype, shown in Fig. 6, is composed of four half-bridge branches implemented using 40-mΩ and 1200-V SiC MOSFETs C2M0040120D from CREE with TO-247-3 package. The MOSFETs are

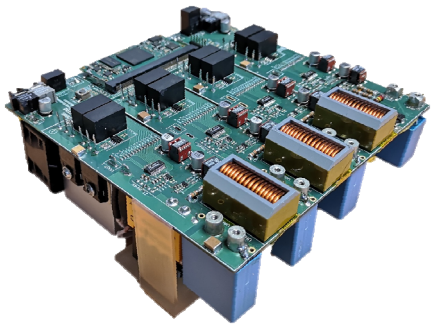
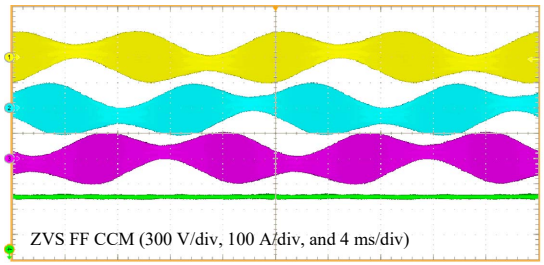


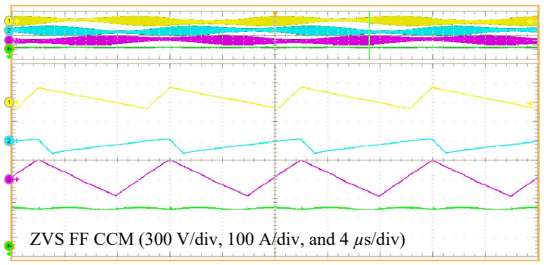
Fig. 6. A 11-kW 3-phase high power-density PFC rectifier for domestic IH applications. The dimensions are 17 cm, 17 cm, and 7 cm, getting more than 5.5 kW/dm^3 including the forced-air cooling, the boost and the balancing inductance, and the input filter.

TABLE I
MULTI-PHASE PFC RECTIFIER DESIGN PARAMETERS

Parameter	Value
Input mains phases, n	1, 2, or 3
Mains phase voltage, v_i	230 V RMS, 50 Hz
Input phase power, $P_{in,i}$	3.6 kW
Total input power, P_{in}	11 kW
Bus voltage, v_b	750 V
Operating frequency, $f_{sw,i}$	100 kHz (FF) 30-330 kHz (VF)
Filter capacitor, $C_{f,i}$	10 μF
Filter inductance, $L_{f,i}$	22 μH
Bus capacitor, C_b	280 μF
Boost inductance, L_i	110 μH (HS) 10 μH (ZVS)
Balancing inductance, L_0	110 μH (HS) 41 μH (ZVS)



(a)



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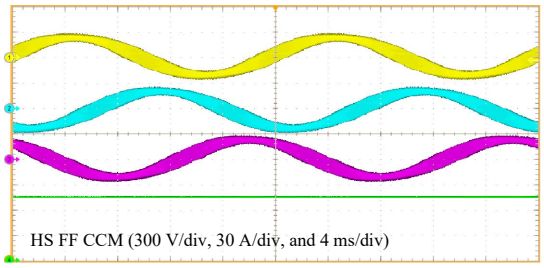

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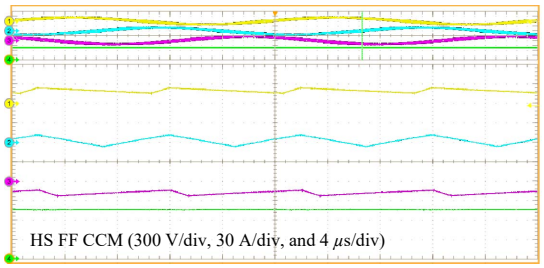

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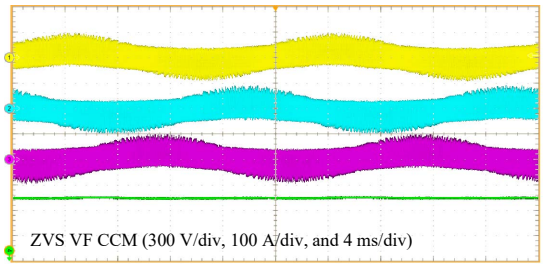
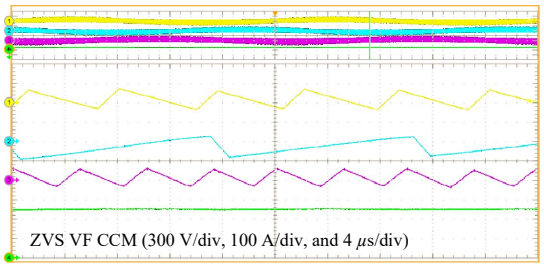


(e)



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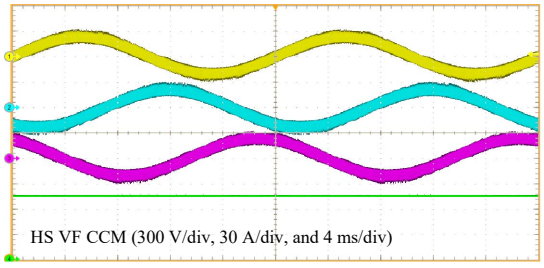

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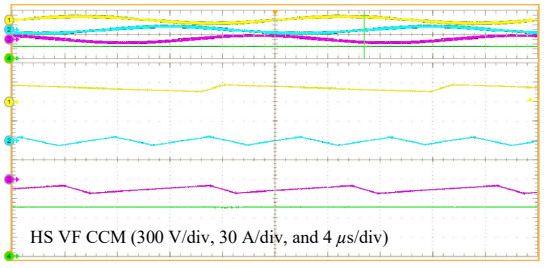

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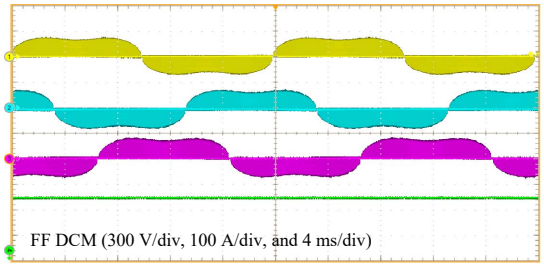
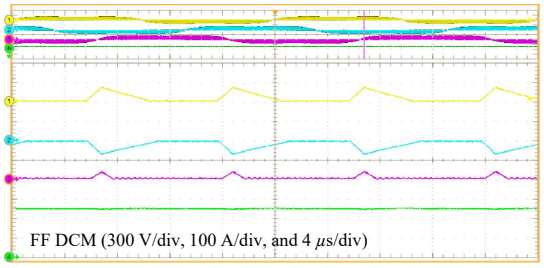


(i)



(j)

Fig. 7.Main experimental waveforms of the converter using every modulation strategy (left side) and a detailed view (right side). From top to bottom: the boost inductance currents $i_{L,1}$, $i_{L,2}$, and $i_{L,3}$; and the bus voltage, v_b. Voltage: 300 V/div and time: 4 ms/div (left side) and 4 μs/div (right side). (a) and (b) ZVS FF CCM (current: 100 A/div), (c) and (d) HS FF CCM (current: 30 A/div), (e) and (f) ZVS VF CCM (current: 100 A/div), (g) and (h) HS VF CCM (current: 30 A/div), and (i) and (j) FF DCM (current: 100 A/div).

driven by the 1EDI60N12AF gate drivers from Infineon. The power losses are dissipated using forced-air cooling. A Zynq XC7Z020 FPGA from Xilinx is used to implement the control architecture. Besides, the whole system can be managed from the PC through a fiber optical module to provide isolation and a PC application developed using Visual Basic. The platform allows measuring current using magneto-resistive current sensors and voltage using voltage dividers. 12-Bit and 10-Msps LTC1420 ADC from Linear Technology are implemented. Besides, 22-µH HA55L-3623220LF inductance from TT Electronics has been used as filter inductance. Table I summarizes the main converter design parameters.

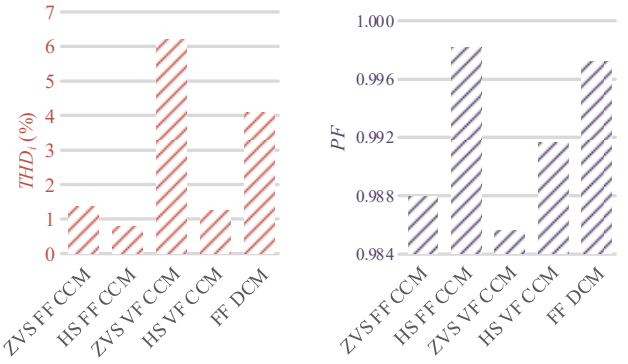
B. Experimental results and waveforms

Fig. 7 shows the experimental results obtained using the proposed modulation strategies with the converter working at maximum power, i.e. 11 kW. Each mains phase is activated delivering 230 V and 16 A to the platform, i.e. 3.6 kW. In each figure it is shown the boost inductance current for each phase, $i_{L,i}$, and the bus voltage, v_b, which is established to be 750 V. The resulting bus voltage ripple is low because the three mains phases are activated. Zoomed details are shown in the right side of Fig. 7

In the ZVS FF CCM (Fig. 7 (a) and (b)) the converter is operating at 100 kHz with a 40-A rms current in the boost inductance, reaching a 100-A peak value, which is lower than the inductance saturation current, i.e. 120 A. This is the most critical case for this component. In the HS FF CCM (Fig. 7 (c) and (d)), the ripple of this current is lower and, therefore, the rms current is similar to the mains phase current, i.e. 15.6 A. The maximum value is lower than 30 A, fulfilling the saturation current too. The operating frequency is 100 kHz, whereas in the ZVS VF CCM (Fig. 7 (e) and (f)) is ranging between 45 kHz and 330 kHz, resulting a 150-kHz average frequency. The rms current is 30 A with maximum values lower than 100 A. The HS VF CCM (Fig. 7 (g) and (h)) is similar to the HS FF CCM. However, in this case, the frequency ranges between 30 kHz and 160 kHz, getting a 95-kHz average frequency. Finally, the FF DCM is shown in Fig. 7 (i) and (j) with the converter working at 100 kHz. The rms current in the boost inductance is 23 A, and its maximum value is lower than 80 A.

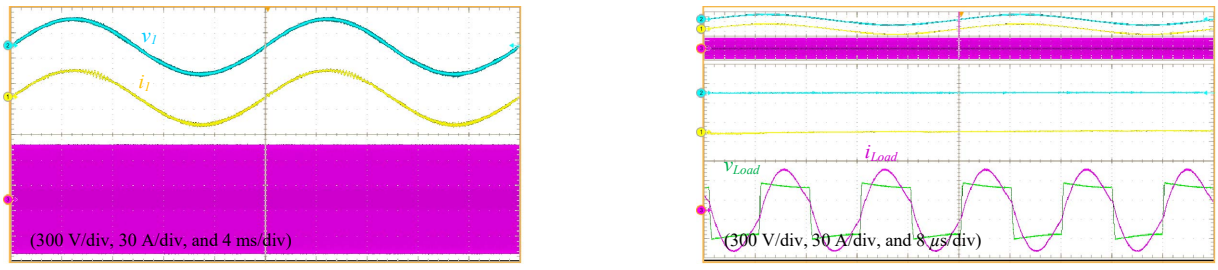
It is important to note that in the ZVS modulation strategies, the boost inductance currents always become negative, assuring therefore zero voltage switching during the turn-on transition in contrast to HS modulation strategies. These currents become null in DCM. All the proposed modulation strategies fulfill the EMC requirements with a low THD, without zero-cross distortion, and with a PF close to the unit (Fig. 8). The worst case is the ZVS VF CCM modulation strategy due to the high frequency sweep, whereas the HS CCM modulation strategies are the best cases.

The HS FF CCM modulation strategy has been selected due to its best efficiency with fixed frequency, as it is discussed later in the comparative analysis, to power an IH half-bridge inverter using the 750-V DC bus. The operating frequencies have been established in 100 kHz for the PFC rectifier and 63 kHz for the IH inverter. Fig. 9 depicts the main input and output waveforms of the converter working at maximum power delivering 11 kW. The three mains phases are working, delivering a 15.8-A rms current each one, and the current in the IH load is around 32 A rms. The IH load is composed of a 10-Ω equivalent series resistance and a 57-µH equivalent series inductance. A 123-nF series resonant capacitor has been placed to obtain the maximum desired power at the selected operating frequency. The return path of the load is connected to the middle point of the split bus capacitor, v_o. The resonant frequency is close to the operating frequency and, for this reason, the waveform of the IH load current, i_{Load}, is sinusoidal. However, the operating frequency is light higher to get an inductive load and achieve ZVS switching in the IH inverter.



(a) (a)

Fig. 8. Experimental THD (a) and PF (b).



(a) (b)

Fig. 9. Experimental waveforms at the input of the PFC rectifier and at the output of the IH inverter powering a 11-kW IH load. Voltage: 300 V/div and current: 30 A/div. Time: 4 ms/div (a) and 8 µs/div (b). From top to bottom: the mains phase voltage, v_1, the mains phase current, i_1, the IH-load voltage, v_{Load}, and the IH-load current, i_{Load}.

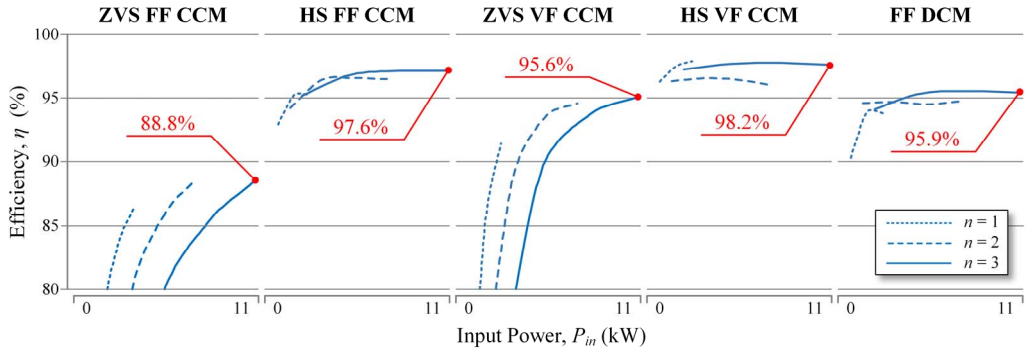


Fig. 10. Experimental efficiency, η, of the implemented 3-phase PFC rectifier using each modulation strategy for different numbers of activated phases, n. The efficiency has been measured in the whole operation range, from 0.7 kW to 11 kW.

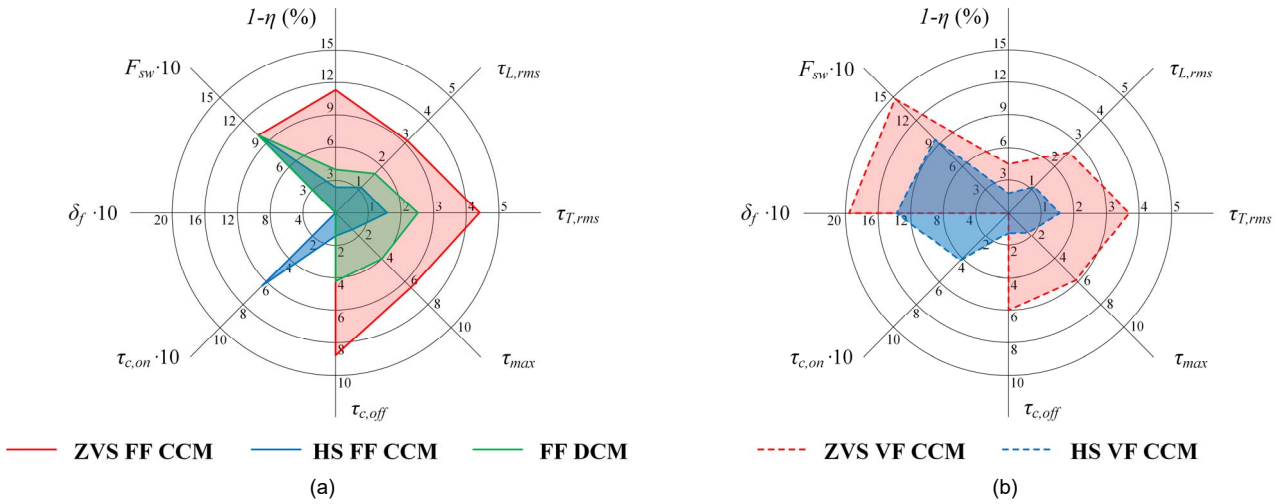


Fig. 11. Comparative evaluation of every modulation strategies. The FF ones in the left radial graph (a) and the VF ones in the right radial graph (b). The employed rates are as follows: the relative losses, 1-η, the relative overall rms current of the inductance, $\tau_{L,rms}$, and the transistor, $\tau_{T,rms}$, the relative maximum current, τ_{max}, the relative turn-off current, $\tau_{c,off}$, the relative turn-on current, $\tau_{c,on}$, the relative frequency swing, δ_{sw}, and the relative average switching frequency, F_{sw}.

C. Measured efficiency

The efficiency of the PFC rectifier, η, is calculated as

$$\eta = \frac{P_{out}}{\sum_{i=1}^{n} P_{in,i}}, \tag{6}$$

being P_{out} the output power, and $P_{in,i}$ the phase-i input power.

It has been experimentally measured using a 4-channel power analyzer Yokogawa PZ4000, using three channels for each input mains phase and the fourth channel for the output. Each modulation strategy has been measured using a different number of active phases, n = 1, n = 2, and n = 3. The whole power range of the converter has been analyzed, i.e. up to 11 kW, and the results are summarized in Fig. 10. The maximum efficiency, 98.2%, at maximum power has been reached using the HS VF CCM modulation strategy.

The results show that the HS strategies get better efficiencies than the ZVS ones with the implemented switching devices. This is due to the high ripple of the boost inductance current, which increases the conduction losses in this component and in the switching devices. Even though the turn-on losses are null, the switching losses also increase because the turn-off currents are significantly high. This fact becomes more evident in the ZVS FF CCM.

Additionally, the efficiency in ZVS strategies is greatly reduced in light load conditions, whereas in HS and DCM strategies this value is almost constant. This is due to the fact that the ripple increases at lower power, increasing the conduction losses. When the frequency is increased to decrease the ripple, the switching losses are higher too.

Finally, it is important to remark that in the ZVS strategies it is better to operate with less active phases to deliver the same power, when possible, to optimize the converter efficiency. However, this consideration is not relevant in HS modulation strategies.

D. Comparative analysis of the modulation strategies

Finally, a comparative evaluation of the studied modulation strategies at maximum power with regard to several key figures of merit, such as rms current, switching current, or frequency is provided to highlight the advantages

and disadvantages of each strategy, and to facilitate the selection of an adequate modulation strategy for a specific application.

Normalized performance rates independent of the developed system have been defined in order to provide a general quantification of the modulation strategies performance. Consequently, the rms mains phase current, $I_{rms,i}$, has been used as reference value. The radial graphs in Fig. 11 show the results of this comparative evaluation. The definition of these performance rates is shown below.

1) Relative Overall RMS Current

The relative overall transistor rms current is calculated as

$$\tau_{T,rms} = \frac{\sum_{i=0}^{n} I_{Th,rms,i} + \sum_{i=0}^{n} I_{Tl,rms,i}}{\sum_{i=1}^{n} I_{rms,i}}, \quad (7)$$

where $I_{Th,rms}$ and $I_{Tl,rms}$ correspond to the rms currents of the high and low transistors, respectively. This parameter allows comparing the overall transistor conduction losses, which are usually calculated using the on-state resistance and the square of the transistor rms current. It should be noted that MOSFETs are activated when the antiparallel diodes are conducting to reduce on-state losses.

The relative overall inductance rms current is calculated as

$$\tau_{L,rms} = \frac{\sum_{i=0}^{n} I_{L,rms,i}}{\sum_{i=1}^{n} I_{rms,i}}, \quad (8)$$

where $I_{L,rms}$ is the inductance rms current. As in the above case, this rate is related to the conduction losses in the boost inductance.

2) Relative Maximum Current

This parameter indicates the maximum current value in the boost inductors and the switching devices, and it is critical when switching devices are selected, or the inductors are designed, because it determines the inductor saturation current. This value is the same in both components, therefore it can be calculated as

$$\tau_{max} = \max_{i\in[1,n]}\left(\frac{I_{L,max,i}}{I_{rms,i}}\right), \quad (9)$$

where $I_{L,max}$ is the maximum current of the boost inductance.

3) Relative Switching Current

The relative turn-off current is calculated as

$$\tau_{c,off} = \frac{\sum_{i=0}^{n} I_{Th,off,i} + \sum_{i=0}^{n} I_{Tl,off,i}}{\sum_{i=1}^{n} I_{rms,i}}, \quad (10)$$

whereas the relative turn-on current is obtained as

$$\tau_{c,on} = \frac{\sum_{i=0}^{n} I_{Th,on,i} + \sum_{i=0}^{n} I_{Tl,on,i}}{\sum_{i=1}^{n} I_{rms,i}}. \quad (11)$$

$I_{Th,off}$ and $I_{Tl,off}$ show the average turn-off currents of the high-side and low-side transistors, respectively. $I_{Th,on}$ and $I_{Tl,on}$ refer to the turn-on currents. These parameters allow comparing the switching loss energy of switching devices.

4) Relative Switching frequency

The F_{sw} rate refers to the average switching frequency normalized to the nominal design frequency, i.e. 100 kHz. This rate along with the relative turn-off and the turn-on currents provide information with regard to switching power losses of the transistors, which are calculated using the switching frequency and the switching energy.

The relative frequency swing is calculated as

$$\delta_f = \max_{i\in[1,n]}\left(\frac{f_{sw,max,i} - f_{sw,min,i}}{100F_{sw}}\right), \quad (12)$$

where $f_{sw,max}$ and $f_{sw,min}$ refer to the maximum and the minimum switching frequencies. This parameter indicates how much the operating frequency changes. It is null in FF modulation strategies.

5) Relative losses

Finally, the efficiency of the system is characterized by the relative losses as 1-η, being η the efficiency obtained using expression (6).

The overall efficiency of the topology highly depends on the switching mode, and the ratio among the switching and conduction performance of the switching devices. In ZVS modulation strategies, the current ripple is higher, increasing rms value of the current in the switching devices, capacitors, and the boost inductance, and, therefore, increasing the conduction losses. Another important consideration is that the higher the current ripple is, the higher the turn-off current becomes, leading to increased turn-off losses. Usually, the better the switching behavior is, the more recommended the HS modulation strategy is. The contrary happens when the power device conduction performance is better in comparison with the switching performance.

After this analysis, and taking into account the final domestic IH application, the HS FF CCM modulation strategy has been selected to control the proposed rectifier. It gets a good tradeoff between efficiency, device stress, implementation, and control cost, fulfilling the domestic IH requirements when SiC MOSFETs are considered. In the case of IGBT scenario, a ZVS strategy is recommended to reduce switching losses.

V. Conclusions

This paper has proposed an implementation of a multi-phase PFC rectifier for a novel domestic IH application, including the proposal, analysis, and comparative discussion of its modulation strategies. This approach is focused on

merging the isolated electronic boards that are powered from different mains phases in order to get a compact enhanced design with additional advantages: an increased power, an improved EMC performance, a cost optimization, a more efficient and more accurate power control, and a better use of devices, improving the performance of current domestic IH systems.

A boost topology has been proposed and its modulation strategies have been presented, including its main advantages and disadvantages. A 11-kW 3-phase high power-density converter for domestic IH applications has been implemented to analyze each modulation strategy. The main experimental waveforms of the rectifier have been presented and the efficiency has been measured in the whole operation range. A comparative evaluation has been performed, defining and discussing normalized performance rates, which facilitate the selection of an adequate modulation strategy for a specific application.

The results show HS strategies are more efficient than ZVS ones in the whole operation range due to the lower ripple of the current. Concretely, the HS VF CCM is the most efficient strategy, reaching the 98.4%. Overall, the FF modulation strategies are less efficient than the VF ones. However a FF strategy can be mandatory according to the final application, as in the case of domestic IH. Finally, a 11-kW domestic IH application has been implemented using the HS FF CCM getting a proper operation of the converter and proving the feasibility of this proposal.

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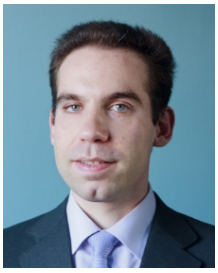

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