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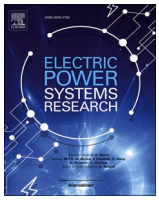

Analysis of voltage dynamics within current control time-scale in a VSC connected to a weak AC grid via series compensated AC line

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ABSTRACT

In this paper, an analytical approach is proposed to analyse the small-signal stability associated with the voltage dynamics of three paths within current control of a VSC connected to a weak AC grid via series compensated AC line: the PLL, active damping and virtual conductance loops. The basic control structure of the VSC is a cascade type based on PI controllers, where DC voltage and reactive current setpoints are used to drive the VSC terminal voltage change. Besides, active damping (AD) and virtual conductance (VC) filters are included to damp high and low frequency oscillations of terminal voltage, respectively. Different series compensation level (SCL) and AC grid stiffness values are considered while performing the analysis. The main design implications obtained through this analysis are the proposal of adequate values for PLL bandwidth according to a decreasing level of AC grid stiffness and suitable ratio values between AD and VC filter gains to ensure stability and good cross-impact, given a SCL value. The analysis is validated by means of simulations conducted in MATLAB® Simulink. The proposed analytical framework serves as a contribution to support a robust terminal voltage change mechanism within current control time-scale.

1. Introduction

With the increasing presence of power electronic devices in modern electrical grids, the interactions between converters and their adjacent transmission lines open room for emerging oscillatory problems. In weak AC grids, the inclusion of series compensated lines can assist full-range active power transfer of converters, in contrast to shunt compensated lines [1]. However, the increase in SCL may also worsen the stability of the system, as the authors in [2] observed on a system composed by a set of VSCs controlled by a virtual synchronous generator (VSG). Besides, when a power electronic-based renewable energy generator injects power to a weak AC grid, power quality and stability issues become more severe by raising the risk of unstable interaction between the converter and the AC grid [3,4]. The influence of phase-locked loop (PLL) schemes on stability has been studied by authors such as [5], pointing out the PLL as the main factor causing sub-synchronous resonance.

Authors in [6] divided the damping methods of a grid-tied inverter on the grid- and inverter-side methods. The grid-side damping measures focus on approaches to reshape the grid impedance to ensure the stability of a local grid-tied inverter, either by resistive power filter to attenuate harmonic propagation, as shown in [6,7], or by the inclusion of a solid-state transformer [8,9] . In turn, the inverter-side measures work on the modification of converter's output impedance to ensure the stability of a local grid-tied inverter. Among these, AD filters came into focus due to their capability to improve stability [10]. Authors in [11] classified the AD techniques into single loop [6,12–14] and multi-loop [3,10,15–21], being multi-loop techniques more employed due to their higher controller bandwidths and whose principle may rely on capacitor voltage [16,22–25] or current feedback control [10,15,17,21,24–26].

The problem of voltage stability in mid- and long-term time-scales has received much attraction but voltage dynamics in transient time-scale and particularly, within current control loop scale, remain still understudied [27]. The transient time-scale may vary from a few milliseconds to one second, according to [27–31]. In this sense, faster control loops within a cascade frame correspond to current control loops (less than 50 ms) in comparison with voltage control loops (from 50 ms to 1 s) [27].

With this purpose, this paper serves mainly as a continuation of the work in [27] and more partially of the work in [29–32], whose

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Nomenclature

PI	Proportional integral controller
$v_{DC,ref}$	DC voltage setpoint
v_{DC}	DC voltage input signal
$\underrightarrow{i_{cv,abc}}$	Converter output current in abc coordinates
$\underrightarrow{i_{cv,dq}}$	Converter output current in dq coordinates
$\underrightarrow{v_{cv,abc}}$	Converter output voltage in abc coordinates
$\underrightarrow{v_{cv,dq}}$	Converter output voltage in dq coordinates
θ_{grid}	Calculated grid phase angle
PLL	Phase locked loop
$k_{p,PLL}, k_{i,PLL}$	Proportional and integral parameters for PLL
$\Delta\omega$	Speed variation of PLL respect to ω_n
ω_{grid}	Actual value of grid angular frequency
ω_n	Rated value of grid angular frequency
V_d, V_q	d and q components of AC grid voltage signal
V_a, V_b, V_c	a, b and c components of AC grid voltage signal
f_s	Switching frequency
$i_{cv,d}$, $i_{cv,q}$	Converter output d-and q-axis current signals
$i_{cv,d,ref}$	Converter active current setpoint in d-axis
$i_{cv,q,ref}$	Converter reactive current setpoint in q-axis
k_{pc}, k_{ic}	Proportional and integral parameters of conventional current control loop (inner loop)
$\underrightarrow{i_{vir,dq}}$	VC current in dq coordinates
$\underrightarrow{\psi_{dq}}$	Low pass filtered signals of $\underrightarrow{v_{o,dq}}$
$\underrightarrow{v_{o,dq,AD}}$	AD voltage in dq coordinates
PCC	Point of common coupling
$C_{s,line}$	Series capacitance of series compensated AC line.
$X_{c,line}$	Series reactance of series compensated AC line
$\underrightarrow{v_{PCC,dq}}$	Voltage at PCC in dq coordinates
P_N	System capacity
V_{DC}	Rated DC voltage
R_f, L_f, C_f	Output filter resistance, inductance and capacitance
V_g	Rated AC grid voltage
R_g, L_g	AC grid resistance and inductance
SCR	Short circuit ratio
m_a, m_b, m_c	a, b and c components of modulation index
ω_b	Base angular frequency
SCL	Series compensation level
EGA	Eigenvalue trajectory analysis
AD	Active Damping
VC	Virtual Conductance
k_{Comp}	Compensation factor degree of the AC line
T_{PLL}	PLL delay
f_{PLL}	PLL bandwidth
k_{AD}	AD gain
G_{vir}	VC gain
G_{vir}/k_{AD}	Relative VC to AD gain
k	Control cycle
L_g	AC grid inductance value
PWM	Pulse width modulation technique
$\underrightarrow{v_{cv,dq,k}}$	Output dq converter voltage at instant k
$\underrightarrow{v_{cv,dq}}$	Output dq voltage at instant k-1
$G^*_{PWM,dq}$	Transfer function associated with the time delay due to the switching PWM process
T_s	Time delay due to the switching PWM process
$\underrightarrow{v_{o,dq}}$	Disturbance rejection feed-forward terms in dq coordinates
$k_{p,v_{DC}}$, $k_{i,v_{DC}}$	Proportional and integral parameters of voltage control loop (outer loop)
ϕ_{dq}	High pass filtered signals of $v_{o,dq}$
ω_{vir}	Cut-off frequency of the VC filter
ω_{AD}	Cut-off frequency of the AD filter
L_{line}	Inductance of series compensated AC line
$X_{l,line}$	Inductive reactance of series compensated AC line
$i_{o,d,q}$	AC grid current signals in dq coordinates
$\Delta v_{Cs,d}$	Voltage drop in dq coordinates due to the series capacitance of AC line
$\underrightarrow{v_{g,dq}}$	AC grid voltage signals in dq coordinates
C_{DC}	DC capacitance
f	Rated grid frequency
f_s	Switching frequency
R_{line}, L_{line}	AC line resistance and inductance
$L_{g,stiff}$	Stiff AC grid inductance
$L_{g,weak}$	Weak AC grid inductance
$L_{g,very\ weak}$	Very weak AC grid inductance
VSC	Voltage source converter

difference lies in the inclusion of a different oscillation mitigation (OM) strategy, the presence of PIs instead of proportional resonant (PR) controllers and the influence of series compensation AC line that connects the VSC with the external AC grid. Therefore, the main novelties of this paper are:

- The clarification of the cross-impact on stability of three voltage dynamic branches, PLL, AD and VC filters, within current control time-scale and the role of each voltage branch in the current-control loop.
- The influence in the previous analysis of the AC grid strength and SCL
- Impact on sub-harmonic and harmonic content due to relative tuning of AD and VC filters.

The paper is organized as follows. In Sections 2 and 3 the methodology is presented, as well as the small-signal model equations for the system. In Section 4 different eigenvalue trajectory analyses (EGAs) are conducted to study the cross- impact of the different voltage dynamic control paths on stability. In Section 5, a case study is described for the implementation of the methodology. In Sections 6 and 7, the proposed framework is validated with simulations conducted in MATLAB® Simulink and several design implications are drawn considering other AC grid strength and SCL values. In Section 8, the obtained stability limits are compared with those from other papers and in Section 9 the main conclusions are extracted.

2. Analytical framework for stability analysis of VSC voltage dynamics on current-control time-scale

In this section the analytical framework for the stability analysis is described. For this purpose, a scheme of a generic VSC connected to the AC grid by means of a series compensated AC line is presented in Fig. 1, where the blocks in yellow are the three VSC voltage dynamic paths whose cross-impact is studied.

The inverter presents a cascade PI-based system where the DC voltage setpoint, $v_{DC,ref}$, is controlled through the d-axis and the converter reactive current setpoint, $i_{cv,q,ref}$, through the q-axis. To this conventional control structure, two voltage dynamic paths are added at the inner control loop, consisting in the AD and VC filters to compensate for

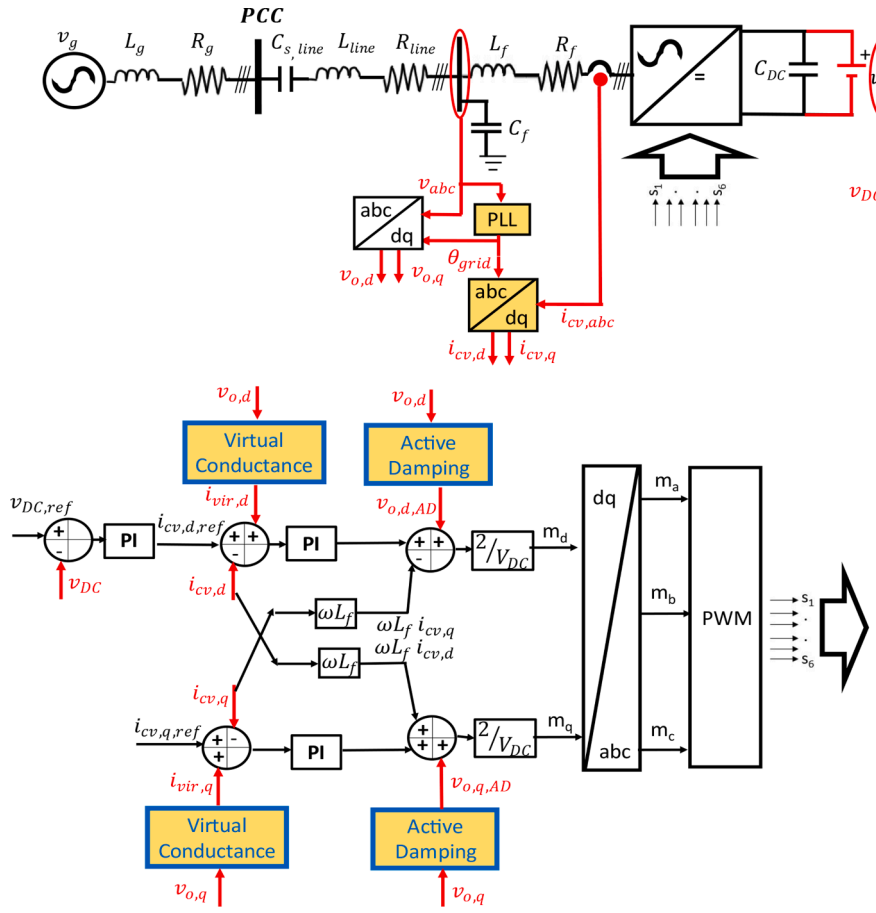

Fig. 1. Scheme of system under study.

high- and low-frequency oscillation modes. In combination with the voltage dynamic path associated with PLL, these present a cross-impact that deserves to be studied.

The inverter is connected to a simplified model of AC grid by means of a series-compensated AC line. In this paper, a simplified Thevenin model of AC grid has been considered to reproduce a comparable baseline scenario as in [27]. As for the sensed variables, the DC voltage at the input of the inverter, v_{DC}, is measured and sent as an input to the outer loop of d-axis control. The converter output current, $\underset{i_{cv,abc}}{\rightarrow}$, is sensed and transformed into dq coordinates to $\underset{i_{cv,dq}}{\rightarrow}$ and the converter output voltage is also sensed as $\underset{v_{cv,abc}}{\rightarrow}$ and transformed into dq coordinates o $\underset{v_{cv,dq}}{\rightarrow}$. To make such transformations a PLL computes the grid angle, θ_{grid}. The employed type of PLL in this paper is a synchronous-frame type to achieve an adequate decoupling between d-and q-axes [33], as presented in Fig. 2.

In Fig. 3 the analytical framework for the methodology is presented. The methodology consists in four stages, which are demonstrated by a numerical example in Sections 3 to 7:

Stage 1-model construction: the first step consists in the construction of a small-signal model of the AC grid-connected VSC by means of a series compensated AC line, and whose control scheme has been previously described and its three dynamic voltage control paths have been identified. The corresponding small-signal model equations are developed in Section 3.

Stage 2- model analysis: the small-signal model developed in Stage 1 is analysed considering three eigenvalue trajectory analyses (EGAs) to clarify the influence of each voltage dynamic path, AC grid strength (L_g) and SCL on the complete system stability. This study is concluded with the maximum SCL (k_{comp}) (1st EGA), the adequate PLL bandwidth (T_{PLL}) (2nd EGA) and with the limits of G_{vir}/k_{AD} ratio to ensure a stable behaviour given a weak AC grid strength value (3rd EGA). The detailed analyses are provided in Section 4.

Stage 3-model simulation and validation: once the different analytical stability constraints are obtained in the EGAs, these are verified by means of time-domain simulations of a specific case study application described in Section 5. The simulations are shown and commented in Section 6.

Stage 4-design implications: once the methodology has been validated through simulations, the design implications of the methodology are extended to other AC grid strength values and SCLs. For each k_{comp} level, the maximum and minimum values of G_{vir}/k_{AD} that ensure stability are obtained considering 3 different AC grid strength values.

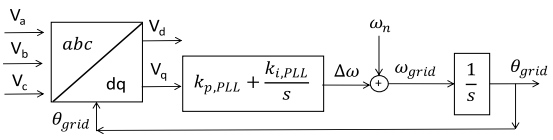

Fig. 2. Employed synchronous frame PLL scheme.

3. State-space equations and small-signal model

Small-signal modelling has been the chosen technique to assess voltage stability to detect adverse interactions due to small changes in the variables around a specific system's operating point that could compromise the detection systems. In this section, the small-signal equations that define the system under study are described, with special focus on the three voltage dynamic paths within current control

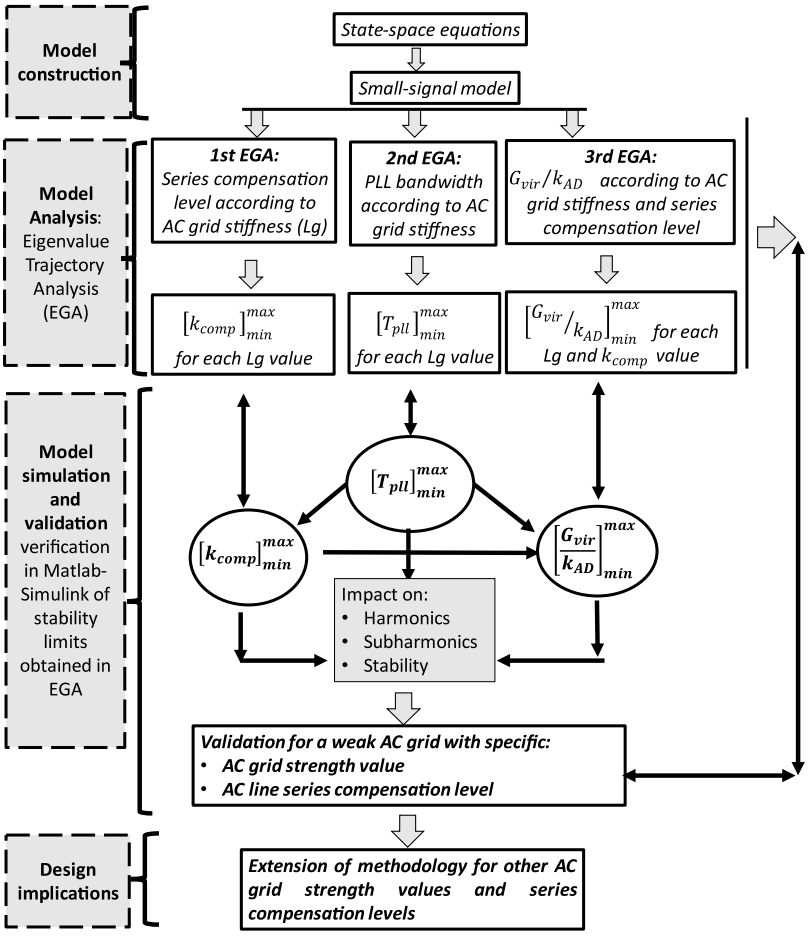

Fig. 3. Methodology flowchart.

loop. Therefore, such equations of the system shown in Fig. 1 are hereafter presented in dq coordinates.

As for the PWM delay modelling, each dq component is calculated based on θ_{grid} angle, which is computed at each control cycle, k. Due to the delay of PWM process, the output converter voltage at instant k is $\overrightarrow{v_{cv,dq,k}}$ and at the previous instant is $\overrightarrow{v_{cv,dq}}$, as seen in (1). These voltage signals are related by means of $G^*_{PWM,dq}$, which is defined in (2–4). The PLL equations are defined in (5–7).

Regarding the basic control structure of the converter, the outer and inner control loop equations are shown in (8,9) and in (10,11), respectively. The conventional inner current controllers in dq frame regulate the d and q components of the output current of the VSC, $i_{cv,d}$ and $i_{cv,q}$, so that they converge to $i_{cv,d,ref}$ and $i_{cv,q,ref}$, respectively. To improve the capability of disturbance rejection feed-forward terms, $\overrightarrow{v_{o,dq}}$ are included at the output of the current controller. The expression in (10) can be expanded if an OM structure is included. In the present paper, the OM structure is composed by two methods for damping oscillatory modes, VC and AD branches.

The mitigation of low frequency oscillations is achieved by the VC branch. It extracts the low-frequency oscillations of the dq voltage at the filter capacitor ($\overrightarrow{v_{o,dq}}$) and injects them in counterphase with the VSC. The contribution of VC branch, $\overrightarrow{i_{vir,dq}}$, is made at the input of current control, as presented in (12),(13), where G_{vir} is the emulated VC gain and ω_{vir} the cut-off frequency of the filter. Besides, ϕ_d and ϕ_q are the high pass filtered signals of v_{od} and v_{oq}, respectively. Therefore, the ($\overrightarrow{v_{o,dq}} - \overrightarrow{\phi_{dq}}$) terms are the low frequency oscillations of $\overrightarrow{v_{o,dq}}$ that are attenuated.

The mitigation of high frequency oscillations is achieved by AD branch. It extracts the high-frequency oscillations of the dq voltage at the filter capacitor ($\overrightarrow{v_{o,dq}}$) and injects them in counter-phase with the VSC. The contribution of AD voltage loop, $\overrightarrow{v_{o,dq,AD}}$, is made at the output of current control, as presented in (14),(15), where k_{AD} is the AD constant and ω_{AD} the cut-off frequency of the filter. Besides, ψ_d and ψ_q are the low pass filtered signals of v_{od} and v_{od}, respectively. Therefore, the ($\overrightarrow{v_{o,dq}} - \overrightarrow{\psi_{dq}}$) terms are the high frequency oscillations of $\overrightarrow{v_{o,dq}}$ that are attenuated.Besides, the $C_{s,line}$ value is directly linked to the compensation factor degree of the AC line, k_{Comp}(%), as indicated in (16). The equations that model the RLC filter, series compensated AC line and AC grid are shown in (17)-(21).

$$\overrightarrow{v_{cv,dq,k}} = G^*_{PWM,dq}\overrightarrow{v_{cv,dq}} \tag{1}$$

$$G^*_{PWM,dq} = \begin{bmatrix} G_{PWM,d} & -G_{PWM,q} \\ G_{PWM,q} & G_{PWM,d} \end{bmatrix} \tag{2}$$

$$G_{PWM,d} = \frac{1 + 1.5T_s s}{(1 + 1.5T_s s)^2 + (1.5T_s\omega_{grid})^2} \tag{3}$$

$$G_{PWM,q} = -j\frac{1.5T_s\omega_{grid}s}{(1 + 1.5T_s s)^2 + (1.5T_s\omega_{grid})^2} \tag{4}$$

$$\Delta\omega = k_{p,PLL}V_q + k_{i,PLL}\int_0^t V_q\delta\tau \tag{5}$$

$$\omega_{grid} = \omega_n + \Delta\omega \tag{6}$$

$$\frac{d\theta_{grid}}{dt} = \omega_{grid} \tag{7}$$

$$i_{cv,\ d,ref} = k_{p,v_{DC}}\left(v_{DC,ref} - v_{DC}\right) + k_{i,v_{DC}}\lambda_{Vdc} \tag{8}$$

$$\lambda_{Vdc} = \int_0^t \left(v_{DC,ref} - v_{DC}\right)\,\delta\tau \tag{9}$$

$$\overrightarrow{v_{i,dq,ref}} = k_{pc}\left(\overrightarrow{i_{cv,\ dq,ref}} - \overrightarrow{i_{cv,\ dq}}\right) + k_{ic}\overrightarrow{\lambda_{ic,d}} + \overrightarrow{v_{o,d,q}} \tag{10}$$

$$\overrightarrow{\lambda_{ic,d}} = \int_0^t \left(\overrightarrow{i_{\ cv,dq,ref}} - \overrightarrow{i_{dq}}\right)\delta\tau \tag{11}$$

$$\overrightarrow{i_{vir,dq}} = -G_{vir}\left(\overrightarrow{v_{o,dq}} - \overrightarrow{\phi_{dq}}\right) \tag{12}$$

$$\overrightarrow{d\phi_{dq}/dt} = \omega_{vir}\left(\overrightarrow{v_{o,dq}} - \overrightarrow{\phi_{dq}}\right) \tag{13}$$

$$\overrightarrow{v_{o,dq,AD}} = \ -k_{AD}\left(\overrightarrow{v_{o,dq}} - \overrightarrow{\psi_{dq}}\right) \tag{14}$$

$$\overrightarrow{d\psi_{dq}/dt} = \omega_{AD}\left(\overrightarrow{v_{o,dq}} - \overrightarrow{\psi_{dq}}\right) \tag{15}$$

$$k_{Comp}(\%) = \frac{X_{c,line}}{X_{L,line}} = \frac{1}{\omega_{grid}^2 C_{s,line} L_{line}} \tag{16}$$

$$\frac{d}{dt}\begin{bmatrix} i_{cv,d} \\ i_{cv,q} \end{bmatrix} = \frac{\omega_b}{L_f}\begin{bmatrix} v_{cv,d} \\ v_{cv,q} \end{bmatrix} - \frac{\omega_b}{L_f}\begin{bmatrix} v_{o,d} \\ v_{o,q} \end{bmatrix} - \begin{bmatrix} \frac{R_f\omega_b}{L_f} & -\omega_g \\ \omega_g & \frac{R_f\omega_b}{L_f} \end{bmatrix}\begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} \tag{17}$$

$$\frac{d}{dt}\begin{bmatrix} v_{o,d} \\ v_{o,q} \end{bmatrix} = \frac{\omega_b}{C_f}\begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} - \frac{\omega_b}{C_f}\begin{bmatrix} i_{cv,d} \\ i_{cv,q} \end{bmatrix} - \begin{bmatrix} 0 & -\omega_g \\ \omega_g & 0 \end{bmatrix}\begin{bmatrix} v_{o,d} \\ v_{o,q} \end{bmatrix} \tag{18}$$

$$\frac{d}{dt}\begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} = \frac{\omega_b}{L_{line}}\begin{bmatrix} v_{o,d} \\ v_{o,q} \end{bmatrix} - \frac{\omega_b}{L_{line}}\begin{bmatrix} v_{PCC,d} \\ v_{PCC,q} \end{bmatrix} - \frac{\omega_b}{L_{line}}\begin{bmatrix} \Delta v_{Cs,d} \\ \Delta v_{Cs,q} \end{bmatrix} - \begin{bmatrix} \frac{R_{line}\omega_b}{L_{line}} & -\omega_g \\ \omega_g & \frac{R_{line}\omega_b}{L_{line}} \end{bmatrix}\begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} \tag{19}$$

$$\frac{d}{dt}\begin{bmatrix} \Delta v_{Cs,d} \\ \Delta v_{Cs,q} \end{bmatrix} = \frac{\omega_b}{C_s}\begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} - \begin{bmatrix} 0 & -\omega_g \\ \omega_g & 0 \end{bmatrix}\begin{bmatrix} \Delta v_{Cs,d} \\ \Delta v_{Cs,q} \end{bmatrix} \tag{20}$$

$$\frac{d}{dt}\begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} = \frac{\omega_b}{L_g}\begin{bmatrix} v_{PCC,d} \\ v_{PCC,q} \end{bmatrix} - \frac{\omega_b}{L_g}\begin{bmatrix} v_{g,d} \\ v_{g,q} \end{bmatrix} - \begin{bmatrix} \frac{R_g\omega_b}{L_g} & -\omega_g \\ \omega_g & \frac{R_g\omega_b}{L_g} \end{bmatrix}\begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} \tag{21}$$

The parameter values for small-signal model are enclosed in Table 1, where $L_{g,stiff}$, $L_{g,weak}$ and $L_{g,very\ weak}$ correspond to SCR values of 15.15, 2.52 and 1.26, respectively. The grid stiffness is thus associated with the AC grid impedance, as in [27].

4. Eigenvalue trajectory analysis

In this section, different EGAs are carried out to clarify the impact on stability of VSC voltage dynamics in current control time-scale when connected to the AC grid via series compensated AC line. The units of vertical axes in these EGAs are radians per seconds. The main scenarios for the EGAs are summarized in Table 2

A. Impact of AC grid strength and series-compensation level

In Fig. 4 an EGA plot is shown for a variation of the AC grid inductance from $L_{g,stiff}$ to $L_{g,very\ weak}$ and considering $k_{Comp} = 50$ %. The critical eigenvalues cross the stability limit at around $L_g = 8$ mH, which means that the system parameters keep a stability margin for stiff and weak grids but not for very weak grids. As for the influence of SCL, in Fig. 5 an EGA is presented for k_{Comp} varying from 10 to 90 % within a weak AC grid. At $k_{Comp} = 60$ % the dominant sub-synchronous eigenvalues cross the imaginary axis, and the system becomes unstable.

B. Impact of PLL frequency bandwidth

In Fig. 6, the modification of PLL bandwidth is explored for an unstable system under a weak AC grid ($L_{g,weak}$) with k_{Comp}=50 %, where the PLL bandwidth is decreased from 57.7 Hz (17.33 ms) to 3 Hz (333 ms).

As seen in Fig. 6, whenever the PLL bandwidth is decreased the critical eigenvalues return to the left half-plane and the system recovers stability. However, other higher frequency eigenvalues get closer to the stability limit. Therefore, the change in PLL bandwidth may help for the recovery of the short-term stability, but it yields to new potential risks of instability.

C. Impact of AD and VC branches

To study the separate contributions on stability from VC and AD branches, an EGA corresponding to VC branch gain variation is initially studied without the presence of AD and vice-versa in a very weak AC grid case that lies within the critical stability limits.

- Impact of VC branch without the influence of AD branch

The variation of G_{vir} from 0 to 1 is presented in Fig. 7.
The low frequency modes are damped to the left half-plane, whereas

Table 1
System parameters.

(kW)	100	k_{pc}, k_{ic}	0.5, 100	f (Hz)	50	L_{line}(mH)	0.152	L_f (mH)	0.55
V_{DC}(V)	700	$k_{p,PLL}$, $k_{i,PLL}$	0.09, 4.7	f_s (kHz)	10	V_g(V)	690	C_f (μF)	32
C_{DC} (mF)	14	R_{line} (mΩ)	4.7	R_f(mΩ)	5	R_g (mΩ)	10	$k_{p,Vdc}$, $k_{i,Vdc}$	1, 40
$L_{g,stiff}$ (mH)	1	$L_{g,weak}$ (mH)	6	$L_{g,very\ weak}$ (mH)	12	L_f (mH)	0.55	C_f (μF)	32

Table 2
Scenarios for EGAs.

Figures involved	L_g	k_{comp} (%)	T_{PLL} (ms)	G_{vir}	k_{AD}	G_{vir}/k_{AD}
A-Impact of AC grid strength and SCL						
Fig. 4	$L_{g,stiff}$ to $L_{g,very\ weak}$	50	19.14	0	0	–
Fig. 5	$L_{g,weak}$	0 to 90	19.14	0	0	–
B-Impact of PLL frequency bandwidth						
Fig. 6	$L_{g,weak}$	50	17.33 to 333.33	0	0	–
C-Impact of AD and VC branches						
Fig. 7	$L_{g,weak}$	50	333.33	0 to 0.05	0	–
Fig. 8	$L_{g,weak}$	50	333.33	0	0 to 0.5	–
Fig. 9a	$L_{g,weak}$	50	333.33	$G_{vir} = k_{AD}$	0 to 0.5	1
Fig. 9b	$L_{g,weak}$	50	333.33	$G_{vir} = 7k_{AD}$	0 to 0.5	7
Fig. 10	$L_{g,weak}$	50	333.33	$G_{vir} = 3k_{AD}$	0 to 0.5	3

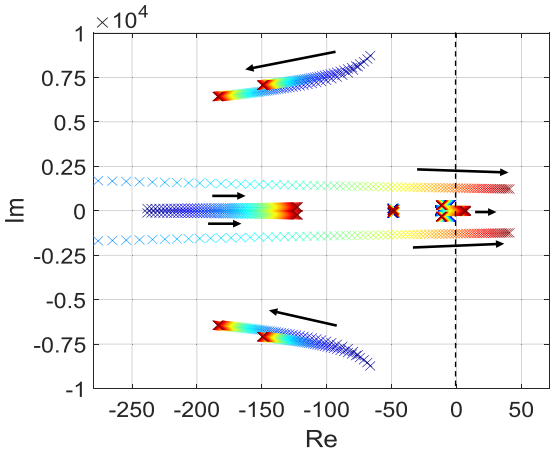

Fig. 4. EGA from $L_{g,stiff}$(blue) to $L_{g,very\ weak}$ (red).

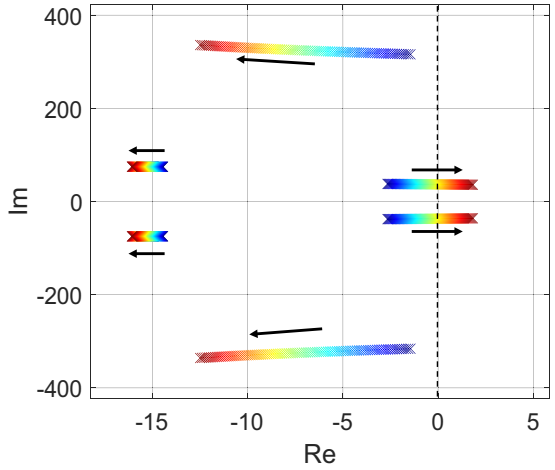

Fig. 5. EGA from k_{Comp} = 10 (blue) to 90 % (red).

the high-frequency modes move within the unstable area. The VC branch without AD filter drives the system to instability as G_{vir} is increased, though there is an initial trajectory that gets closer to the stable area. Without AD branch, the high-frequency modes are responsible for unstable operation.

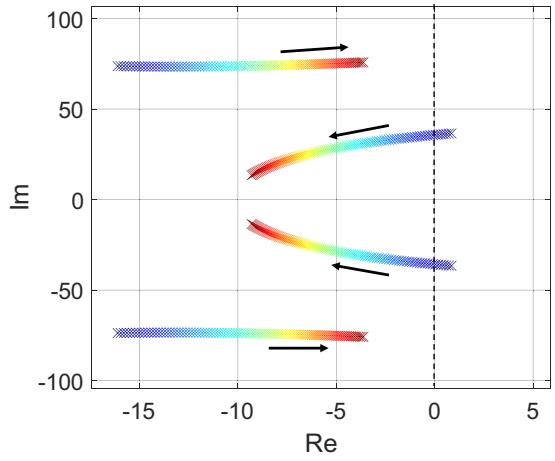

Fig. 6. EGA for the variation of PLL bandwidth between 17.33 ms (blue) to 333 ms (red).

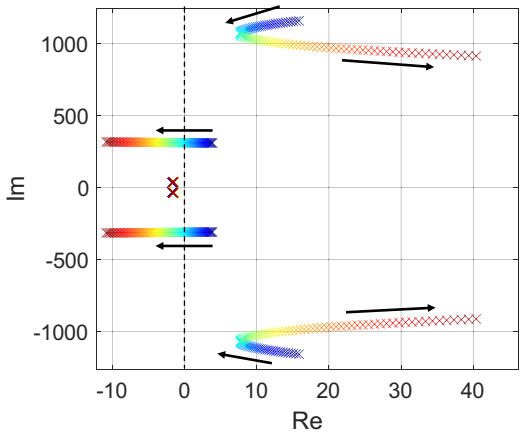

Fig. 7. EGA for G_{vir} from 0 (blue) to 1 (red).

- Impact of AD branch without the influence of VC branch

The variation of k_{AD} from 0 to 0.5 is presented in Fig. 8. While the increase of k_{AD} from 0 to 0.5 damps the high-frequency eigenvalues as it makes them move towards the left-side plane, the low-frequency oscillatory modes are driven towards to the unstable area, as seen in Fig. 8. Besides, within the last set of k_{AD} value, those damped high frequency

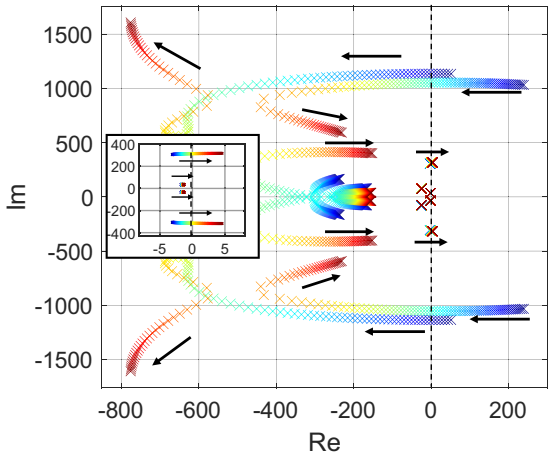

Fig. 8. EGA for k_{AD} from 0 (blue) to 0.5 (red).

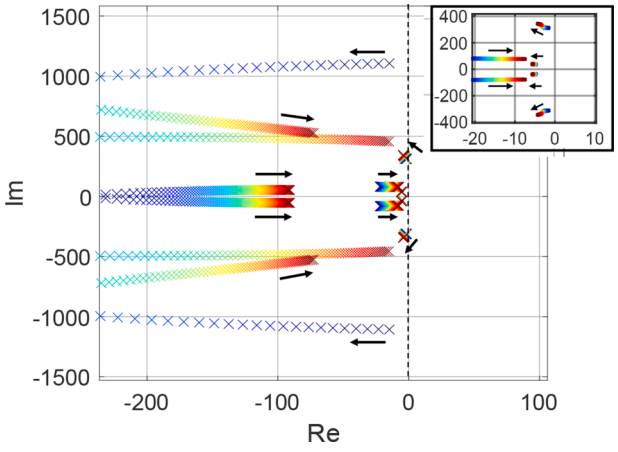

Fig. 10. EGA for k_{AD}:0 (blue)→0.5 (red) where $G_{vir} = 3k_{AD}$.

modes get closer to the half-right plane again, which contributes to a decreasing instability margin. Without the presence of VC branch, the low-frequency eigenvalues are responsible for unstable operation.

Hence, a compromise between of AD and VC gains must be achieved to damp both high- and low-frequency modes simultaneously and without negative cross-impact.

- Combined influence of AD and VC branches

EGA plots for combined influence of AD and VC branches are shown in Fig. 9(a) and(b), where G_{vir}=k_{AD} and G_{vir}=7k_{AD} have been set, respectively, for a variation of k_{AD} from 0 to 0.5.

Whereas for a $G_{vir} = k_{AD}$ the low-frequency eigenvalues are responsible for system instability, the high frequency eigenvalues are those that first drive the system to instability for $G_{vir} = 7k_{AD}$. In turn, in Fig. 10 the system lies between the two unstable situations shown previously for $G_{vir} = 3k_{AD}$, and stability is guaranteed for the same range of k_{AD} values explored as in Fig. 9. Therefore, an intermediate stable $G_{vir} = 3k_{AD}$ function between two unstable extremes, has a relatively good cross-impact on stability.

5. Case study

A case study is defined to validate the analysis in previous sections regarding the stability of the VSC connected to the AC grid via a series compensated AC line. Both the SCL of AC line and AC grid strength remain as configurable parameters to carefully reproduce the previous scenarios. Besides, an additional converter is considered while implementing the case study, i.e. a converter that tracks the maximum power of a PV plant under irradiance changes is included on the DC side of the VSC to consider influences from a PV-side converter. This converter is responsible for the system perturbation in the simulation scenarios due to a sudden 20 % decrease in photovoltaic power production change and will replace the DC voltage source in Fig. 1. The DC boost converter parameters are listed as follows: 12 mF, 4 mH and 5 kHz. The remaining parameters for VSC and AC grid side are those employed in Table 1 and the case study has been implemented in Matlab-Simulink.

6. Validation of eigenvalue analysis on a case study

In this section, the analyses obtained in Sections 3 and 4 are validated through simulations conducted in MATLAB® Simulink for the case study described in Section 5. The DC input voltage to the VSC and the RMS value of phase to ground AC voltage at PCC are shown for the different scenarios.

A. Grid strength combined with PLL bandwidth.

In Fig. 11 the DC voltage and RMS signal of AC voltage at PCC are shown for different AC grid strength and T_{PLL} values.

The VSC cases with T_{PLL} = 17.33 ms tied to stiff and weak AC grids present expected stability, being more oscillatory when tied to a weak AC grid than to a stiff grid. In contrast, T_{PLL} = 17.33 ms no longer guarantees stable behaviour for the VSC case tied to a very weak AC grid, as it leads to higher amplitude oscillations. However, when increasing the T_{PLL} to 333 ms, the VSC tied to a very weak AC grid reduces the

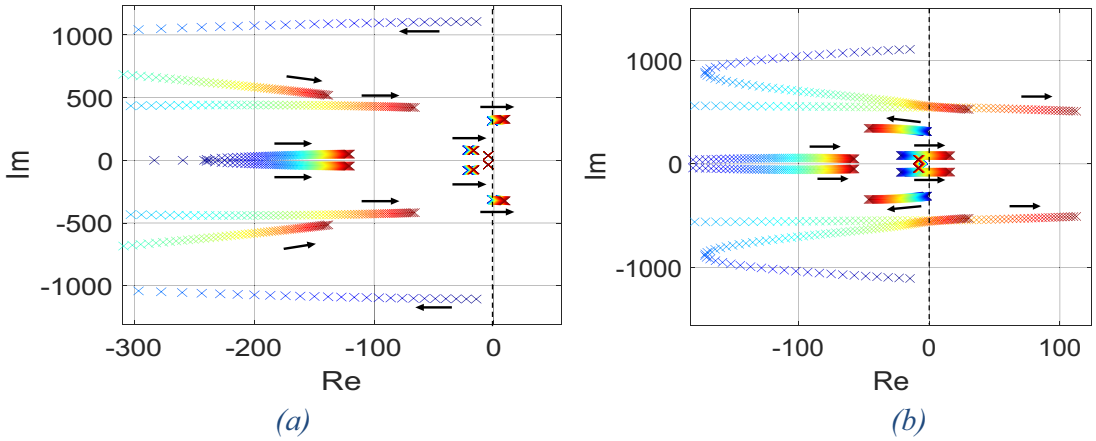

Fig. 9. EGA for k_{AD}:0 (blue)→0.5 (red):(a)$G_{vir} = k_{AD}$ and (b)$G_{vir} = 7k_{AD}$.

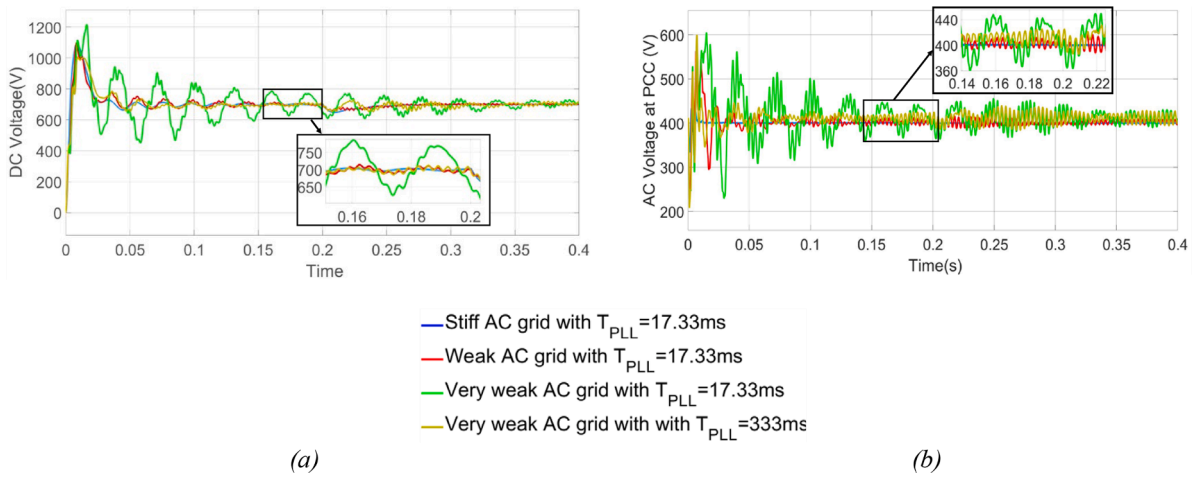

Fig. 11. DC voltage and RMS AC voltage signal at PCC for different AC grid strength and PLL bandwidth values.

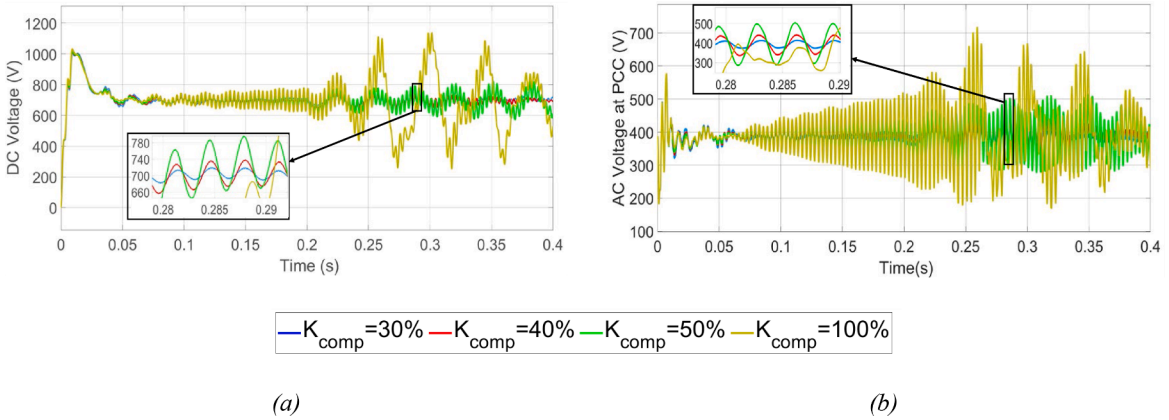

Fig. 12. DC voltage and RMS AC voltage signal at PCC for different SCLs.

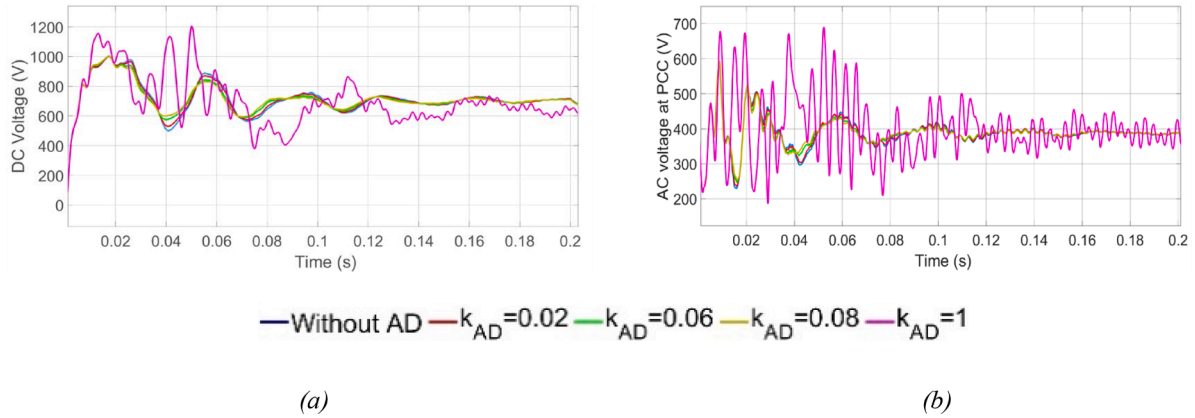

Fig. 13. DC voltage and RMS AC voltage at PCC with different k_{AD} values and constant G_{vir}.

oscillatory behaviour at PCC. From now on, T_{PLL} value is set to 333 ms, and only very weak AC grid case is considered.

B. Effect of SCL in a very weak AC grid

In Fig. 12 the DC voltage and RMS signal of AC voltage at PCC are shown for different SCLs, given a VSC tied to a very weak AC grid and with T_{PLL} = 333 ms. As demonstrated by simulations, the different signals become more and more oscillatory whenever the SCL increases. Below 50 % level, the cases are stable but from this level on, unstable. From now on, SCL of 30 % is considered. Up to this stage, the background scenario has been configured with framework AC grid strength value of 6 mH, SCL of 30 % and PLL bandwidth of 333.33 ms, so that new instability mechanisms related to VC and AD branches can be validated in next stages.

C. Impact of k_{AD} with constant G_{vir}

In Fig. 13, the DC voltage and RMS signal of AC voltage at PCC are shown for a VSC tied to a very weak AC grid for different k_{AD} values,

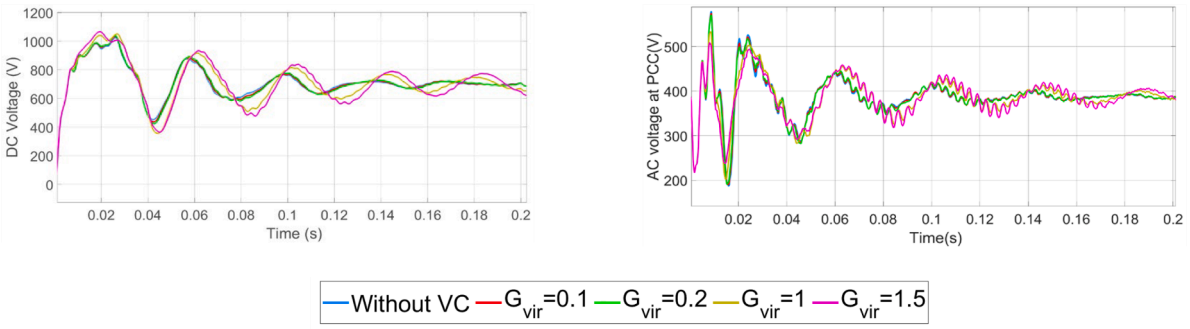

Fig. 14. DC voltage, RMS AC voltage and AC current signals at PCC with different G_{vir} values and constant k_{AD} k_{AD}.

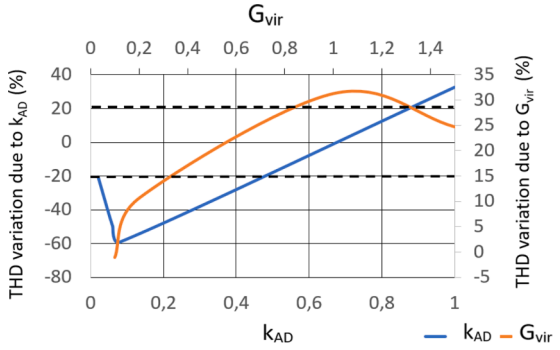

Fig. 15. Variation on THD levels on current signals at PCC due to k_{AD} and G_{vir} (%).

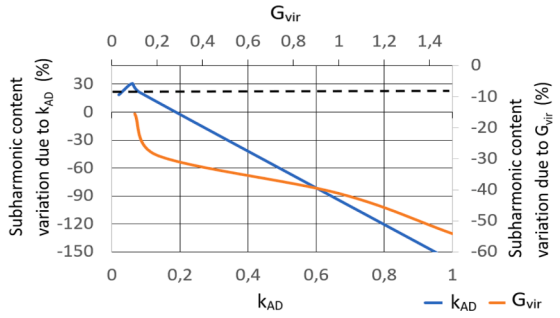

Fig. 16. Variation on Subharmonic content of current signals at PCC due to k_{AD} and G_{vir} (%).

while $G_{vir}$is kept to 0.01. As seen in Fig. 13, the different k_{AD} values reduce the oscillation amplitude of signals as far as k_{AD} is increased until 0.08. Beyond this value, the system becomes unstable.

D. Impact of G_{vir} with constant k_{AD}

In Fig. 14, the DC voltage and RMS signal of AC voltage at PCC are shown for a VSC tied to a very weak AC grid for different G_{vir} values, while k_{AD} is kept to 0.01. As in Fig. 14, the different G_{vir} values imply very similar transient behaviors of signals as far as G_{vir} is increased until 1. Beyond this value, the system becomes highly oscillatory.

E. Separate impact of G_{vir} and k_{AD}

Based on previous subsections, a discussion on the separate impact of G_{vir} and k_{AD} on THD and subharmonic content of current signals at PCC is achieved relatively to the system without VC nor AD filters, according to Figs. 15 and 16, respectively.

Regarding the THD level, as k_{AD} is increased, greater reduction in THD level is achieved until $k_{AD} = 0.08$, with respect to the system without AC nor VC filters, as seen in Fig. 15. Beyond this value, such reduction in THD level is diminished and for k_{AD} values greater than 0.65 the THD level is increased, reaching more than 20 % increase in the case of $k_{AD} = 0.1$. Thus, the AD filter complies with its function of reducing high-frequency oscillation levels whenever it is tuned below certain k_{AD} level, which also acts as a stability limit, as seen in Fig. 13. Beyond this limit, the AD filter worsens the system's stability and effectiveness. In turn, the increase of G_{vir} produces the increment in THD level with respect to the system without filters and compromises stability, as seen in Fig. 14 and Fig. 15.

As for the subharmonic content, the growth of k_{AD} until 0.08 provokes a general increase in subharmonic level whose maximum lies above 20 % increase with respect to the system without AD nor VC filters, as seen in Fig. 16. Beyond that value, the subharmonic levels are minimized, though values close to 1 drive the system to instability. Thus, it can be concluded that the increase in k_{AD} makes the subharmonic content grow with respect to the system without AD nor VC filters, whereas the k_{AD} value is kept below a boundary. In turn, as G_{vir} is increased, the subharmonic content is decreased. Hence, the VC filter complies with its function of reducing low-frequency oscillation levels whenever it is tuned below certain G_{vir} level, which acts as a stability limit. Beyond this, the VC filter worsens the system's stability, as seen in EGA plot in Fig. 14. Therefore, the impact of k_{AD} increase on subharmonic content is coherent with the EGA plots in Figs. 8 and 13, where the increase of k_{AD} provoked the movement to the unstable half-plane of low-frequency eigenvalues, despite the stabilization effect on high-frequency eigenvalues. The impact of G_{vir} on THD content is coherent with the EGA plot in Figs. 7 and 14, where the increase of G_{vir} moved the high-frequency eigenvalues towards the right side, despite the stabilising effect on low frequency eigenvalues.

F. Combined impact: the effect of G_{vir}/k_{AD}

In Section 4, an adequate G_{vir}/k_{AD} ratio within a VSC connected to a very weak AC grid was given to ensure the stability of the system, so that much lower or greater G_{vir}/k_{AD} values may endanger stability, as observed in Fig. 9. Now, similar ranges are obtained for the case study. In Fig. 17, the behaviour of DC voltage and RMS signal of AC voltage at PCC are shown for a VSC tied to a very weak AC grid, where the G_{vir}/k_{AD} ratio is varied.

As seen in Fig. 17, $G_{vir}/k_{AD} = 2.5$ improves the behaviour of signals with respect to the case without AD nor VC by reducing the oscillation amplitudes. However, $G_{vir}/k_{AD} = 0.125$ and $G_{vir}/k_{AD} = 25$ make the system more oscillatory. Therefore, G_{vir}/k_{AD} must be limited to a bounded interval to ensure the stability of the system and the

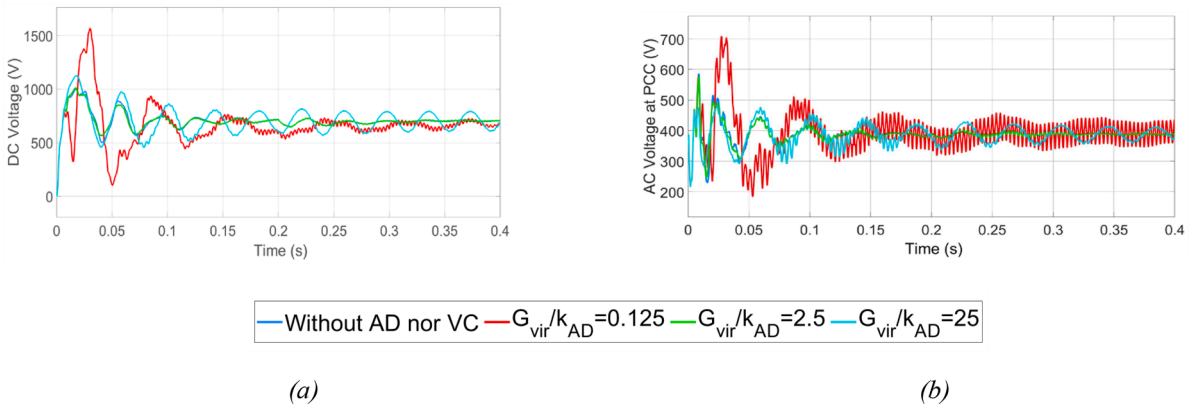

Fig. 17. DC voltage and RMS AC voltage signal at PCC with different G_{vir}/k_{AD} values.

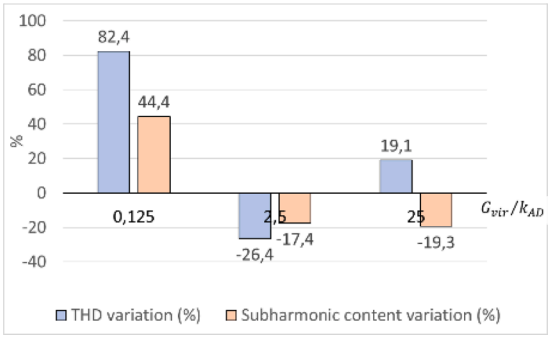

Fig. 18. THD and Subharmonic content variation (%) in AC current signal at PCC due to different G_{vir}/k_{AD} value.

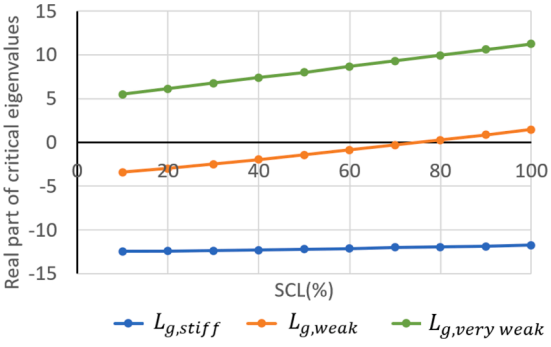

Fig. 19. Real part for different SCLs and strength of AC grid (stiff, weak and very weak).

effectiveness in reducing the high and low- frequency oscillations simultaneously without impacting negatively on each other. In Fig. 18, the impact of G_{vir}/k_{AD} ratio on the THD and subharmonic level variation of current signal at PCC is shown relatively to the system without OM filters.

By taking the case without AD nor VC as a basis, $G_{vir}/k_{AD} = 2.5$ shows improvement in THD and subharmonic level reduction, as it yields to 26.4 % and 17.4 % reductions in THD and subharmonic levels. However, $G_{vir}/k_{AD} = 0.125$ and $G_{vir}/k_{AD} = 25$ imply a worsening in current THD content and therefore, neither of them are suitable ratio values.

7. Design implications

Once the methodology has been validated through simulations, the results are extended to other values. For this purpose, the real part of the critical eigenvalues is shown for different AC grid strengths in Fig. 19, by continuing the analysis of Figs. 4 and 5.

For a stiff AC grid, the system is stable for all range of compensation levels. On the contrary, for a very weak AC grid the system is completely unstable for the entire range of k_{Comp} (%). An intermediate case corresponds to a weak AC grid, where the system remains stable for SCL below 70 % and unstable with SCL above this value.

Hence, the combination of weak AC grid strength and high SCL gives room to instabilities between VSC and AC grid that can deteriorate the voltage dynamics at the PCC, and proper relative tuning of OM filter gains is needed to mitigate oscillations and keep the system within stability. Therefore, the maximum and minimum limits of G_{vir}/k_{AD} that ensure stability are shown in Fig. 20 for different SCL and AC grid stiffness values.

As the AC grid gets weaker, the difference between the minimum and maximum value of G_{vir}/k_{AD} that ensure stability is narrowed. Besides, the minimum and maximum values of G_{vir}/k_{AD} that ensure stability increase with higher SCL.

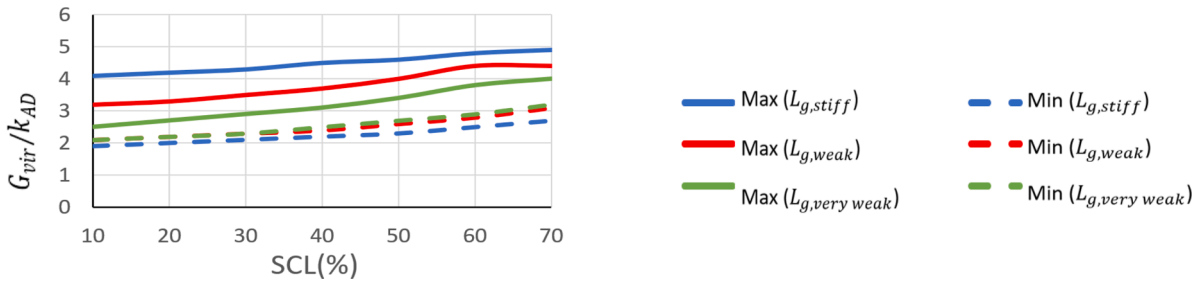

Fig. 20. Maximum and minimum values for G_{vir}/k_{AD} that ensure stability for different L_g and SCL values.

8. Comparison with other studies in the literature

In [27], it was claimed that voltage feed-forward (VFF) term poses an additional loop that introduces negative damping and thus reduces the terminal stability, especially when connected to weak AC grids. However, proper tuning of AD included in this VFF term can reverse the electrical damping characteristic. This inference in [27] supports the conclusion achieved in the present paper while exploring the effect of k_{AD} on stability and moreover, that of the combined G_{vir} /k_{AD} ratio. Similar EGAs and simulations were implemented by using a low voltage grid in [5,34], which were validated experimentally. However, no combined influence of AD with VC terms was explored in these works, and thus, such gap is filled with the present paper. Besides, authors in [2] also concluded that SCL of more than 50 % drive the system to instability if just a single VSC was considered, and the stability was ensured for larger SCL if parallel VSCs were included.

9. Conclusions

In this paper, a stability analysis of voltage dynamics that operate within current control time-scale in a VSC has been carried out. A small-signal model has been constructed based on equations and EGAs have been carried out to clarify the cross-impact of PLL bandwidth, SCL and relative G_{vir}/k_{AD} on the system's stability. Based on these EGAs, specific ranges for PLL bandwidth, SCL and the G_{vir}/k_{AD} ratio that ensure stability have been obtained. Each stability limit imposed by the PLL bandwidth, SCL and the G_{vir}/k_{AD} ratio has been verified through simulations. The design implications have been extended to other values and contrasted with other studies in the literature.

CRediT authorship contribution statement

Marta Haro-Larrode: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization, Writing – original draft, Writing – review & editing. **Pablo Eguia:** Formal analysis, Investigation, Methodology, Supervision, Writing – review & editing. **Maider Santos-Mugica:** Conceptualization, Methodology, Resources, Software, Visualization, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

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