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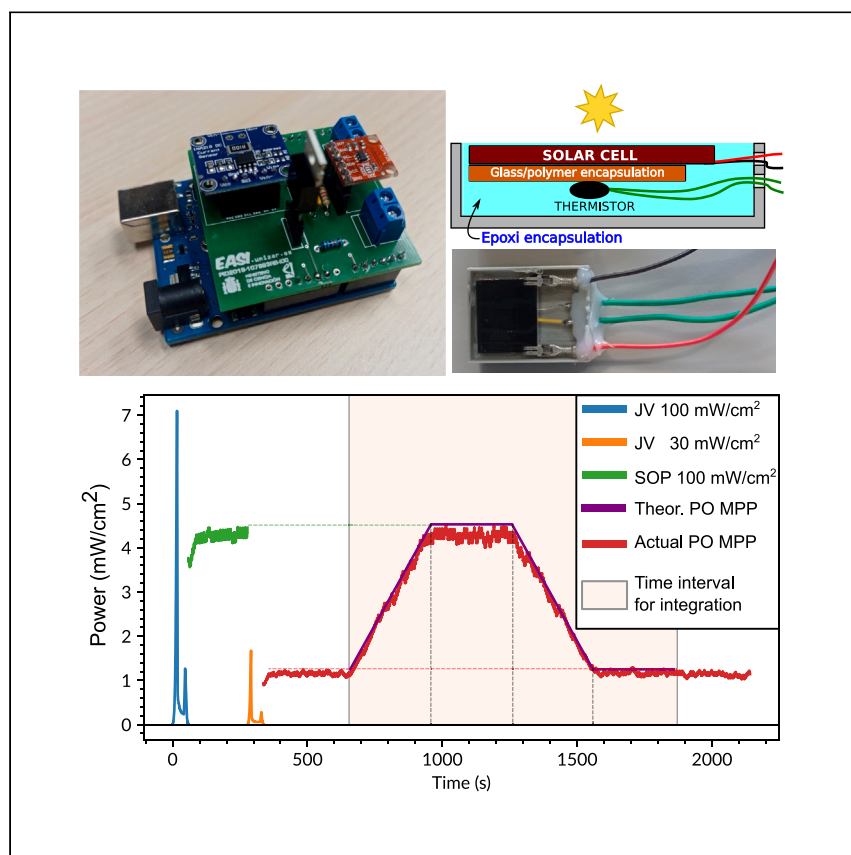
Enhanced power-point tracking for high-hysteresis perovskite solar cells with a galvanostatic approach

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Highlights

Cost-effective hardware for operational stability measurements in perovskite solar cells

Controlled current instead of voltage biasing maximizes power output

Perovskite solar cells are evaluated under EN-50530-type cycle variable illumination

While perovskite solar cells boast efficiency, stability challenges hinder commercialization. Here, Juarez-Perez et al. introduce a maximum-power-point tracking algorithm and cost-effective hardware for long-term stability testing, aiming to enhance the statistical significance of future stability advancements in perovskite solar cells.

Article

Enhanced power-point tracking for high-hysteresis perovskite solar cells with a galvanostatic approach

Emilio J. Juarez-Perez,[1,2,6,*] Cristina Momblona,[1] Roberto Casas,[3] and Marta Haro[4,5]

SUMMARY

Harnessing the untapped potential of solar energy sources is crucial for achieving a sustainable future, and accurate maximum-power-point tracking of solar cells is vital to maximizing their power generation. This article introduces a power-tracking algorithm and cost-effective hardware for long-term operational stability measurements in perovskite solar cells. Existing algorithms for photovoltaic technology lead to suboptimal performance when applied to the most stable perovskite devices (for example, triple-mesoscopic hole-transport-material-free metal halide perovskite solar cells). To address this challenge, we developed a low-cost hardware solution for research purposes that enables concurrent long-term stability measurements in parallel with a galvanostatic-type power-tracking algorithm, ensuring superior operational performance for high-hysteresis perovskite solar cells. The suggested enhancements bear significant implications for the extensive integration of perovskite solar-cell technologies, particularly those dependent on power-optimizer devices.

INTRODUCTION

Electricity generated by solar photovoltaic (PV) systems has unique advantages compared to other renewable energies (wind, hydroelectricity, biomass, among others) with a lower environmental impact and expanded integration possibilities in future society and mobility applications. As an example, silicon panels are already integrated into the urban and rural areas because of their low-cost installation and low maintenance, obtaining energy independence with long-term savings. In recent decades, novel PV technologies have emerged, with perovskite solar cells (PSCs) standing out as the most promising technology with a power conversion efficiency (PCE) record comparable to that of single-crystal silicon cells.[1] However, the potential industrial relevancy of halide perovskite technology is still compromised as the long-term operational stability has not yet been guaranteed. Analyzing and ensuring the operational stability of PSCs is a complex endeavor, contingent upon numerous factors and demanding significant economic and time investments. To promote and accelerate research and market adoption of this technology, especially given their stability challenges and hysteresis phenomena, it is crucial to have accessible and specialized equipment for widespread and high-throughput operational stability measurements in PSCs.

The factors affecting the stability of PSCs are extrinsic—temperature, humidity, O_2—or intrinsic by the choice of perovskite chemical composition, charge transport materials, metal electrodes, and device layout.[2–9] In recent years, PSCs utilizing carbon electrodes have emerged as a notably stable device architecture of choice.[10] Solar cells using metallic top electrodes—gold or silver—often suffer from stability issues

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such as oxidation of the electrode and metal migration to the perovskite layer inducing degradation in the device.[11] Furthermore, carbon-based PSCs obviate the need for hole transport materials (HTMs), thereby mitigating potential stability concerns stemming from the incorporation of dopants to enhance layer conductivity or the absence of adverse side reactions with halide perovskite materials.[12,13] Nonetheless, it is crucial to acknowledge that, while this heightened operational stability is achieved, there can be a trade-off involving a decrease in device efficiency when compared to HTM-based counterparts. HTM-free carbon-based PSCs especially present the hysteresis phenomenon and complicate the accurate evaluation of the cell performance. Hysteresis in PSCs is observed by the difference between current density-voltage (JV) curves upon a change in voltage sweep direction. The hysteresis in PSCs is not an intrinsic characteristic of the device but depends on the voltage scan parameters selected for the realization of the JV curve,[14,15] and there is no agreement on its origin.[16–22] Within the context of this work, hysteresis in the JV curve characteristics introduces notable uncertainty in the determination of the maximum power point (the cell voltage producing the maximum power output [V_{MPP}]) and, consequently, the PCE of the device. To address this challenge, researchers envisaged a stabilized output power (SOP) measurement setting the device at constant V_{MPP}, previously determined through the JV curve, for a short interval of minutes to ensure a genuinely stable power output.[23,24] In recent years of PSC research, a crucial shift has occurred in the efficiency measurement methodology, with a growing emphasis on this kind of steady-state efficiency assessments at fixed voltages to ensure the credibility of the reported results. There is a growing consensus that the traditional maximum-power-point tracking (MPPT) algorithms, commonly used to maximize power output under variable irradiation of well-established PV technologies,[25–29] should assume greater significance as the standard methodology for performance assessment in PSCs instead of the traditional fixed-voltage-rate JV curve measurements.[24,30–32] MPPT algorithms offer a realistic assessment of device efficiency in real-world scenarios and provide insights in the short-term operational stability. Early efforts in developing MPPT algorithms for PSCs were based on the perturb and observe (P&O) algorithm, revealing that devices with significant hysteresis required modeling of current data decay to accurate tracking[33] or minimizing large oscillations around optimal voltage by introducing the concept of power thresholds before changing voltage direction in the algorithm.[34] Other variations of the P&O algorithm reported include using two/three voltage point measurements or short JV sweeps[35] and stabilization times (10 s, 1 s).[36,37] Additionally, other algorithms known to be used in PSCs include the genetic algorithm[38] and the fractional open-circuit voltage tracking a circuit model of a PSC under variable illumination conditions.[39] Certainly, despite MPPT benefits in PSC research, limited number of potentiostats and solar simulators equipment in the labs, along with challenges in algorithm implementation, hinder widespread use of this technique for statistically significant batch testing in emerging photovoltaic labs.

Evolving computing—memory and operations per second—capacities of microelectronics together with its capacity to acquire and generate signal at high speed allow complex algorithms to be implemented in tiny devices at very low cost. This work presents the development of a cost-effective open-hardware-based platform[40] for long-term stability measurements on lab-scale solar cells, eliminating the need for expensive monitoring systems. Accurate tracking of the MPPT is crucial for maximizing power generation. However, existing MPPT firmware algorithms designed for classical photovoltaic technology perform suboptimally in metal halide perovskite-based single cells due to hysteresis. To address this, an MPPT algorithm is

implemented here in which controlling current (galvanostatic approach) instead of voltage bias (potentiostatic approach) applied in the device enables continuous and precise tracking of the maximum power output, resulting in superior operational performance. Furthermore, it is noteworthy that, while differentiation between potentiostatic and galvanostatic approaches may seem unnecessary in conventional non-hysteretic solar cells, as discussed in the integration of our hardware to track individual commercial silicon solar cells (see section "validation of the galvanostatic MPPT testing device"), our investigation into PSCs, which exhibit hysteresis, reveals a notable disparity between the two modes, as detailed in section "testing the low-cost galvanostatic MPPT tracker device on PSCs." This distinction is crucial for fully understanding the results and implications of our methodology within the broader context of solar-cell characterization.

This article outlines the detailed methodology employed to construct such custom hardware and implements useful algorithms for short operational stability tests on small-area lab-scale single-cell PSCs. These advancements have significant implications for widespread adoption of PSC technologies in solar-energy harvesting, driving progress toward a greener and more sustainable future.

RESULTS AND DISCUSSION

PSC assembly and encapsulation

The assembly of the PSCs was carried out using the commercial triple-mesoscopic monolithic Perovskite Solar Cell Kit provided by Solaronix. This kit offered a ready-to-use perovskite precursor solution and monolithic electrodes containing compact TiO_2, mesoporous TiO_2, mesoporous ZrO_2, and carbon layer, all optimized for their respective thicknesses. The precursor solution was carefully dropped onto the electrode stack substrate, allowing it to permeate the triple-layer mesoscopic porous structure. To ensure precise and controlled device fabrication, we applied an adhesive impregnation mask to prevent the spread of perovskite precursor solution beyond the active area. Through the annealing process (1.5 h, 50°C), the perovskite material grew within the mesoporous triple stack followed by a humidity-assisted thermal exposure (HTE) treatment.[41] The humidity treatment was performed in an oven at 40°C containing a vessel with saturated NaCl aqueous solution to reach constant 75% relative humidity.[42] The temperature and relative humidity inside the oven were continuously monitored by a sensor module (DHT22, Adafruit). Then, devices were enclosed using the standard pre-laminated glass lids with sealing gaskets from the kit as primary encapsulation stage. Copper cables were soldered to metal spring clamps attached to the electrodes to establish the electrical connections. A mask of 0.64 cm^2 was placed to delimit the active area of the solar cell. To monitor the device temperature, a 10-kΩ, 25°C negative temperature coefficient (NTC) type thermistor was fixed in contact to the back surface of the PSC ensuring that the thermistor head was not exposed to direct light illumination. Finally, the assembled device was placed in a specific jig and completely immersed in two-component transparent epoxy resin followed by a 48-h curing process working as a secondary encapsulation stage (Figures 1A and 1B).

Triple-mesoscopic PSCs underwent different durations of HTE treatment (Table S1) after conventional annealing at 50°C for 1.5 h. Initially, the PSCs exhibited JV curves with the undesired high-current shoulder near voltages close to V_{MPP} and larger than the J_{SC}. In our hands, the optimal HTE treatment duration was ~40 h, but all durations (from ~40 to ~120 h) result in cells with PCEs within ~7.5% range. The HTE step does not eliminate the hysteresis observed in all studied devices, where the
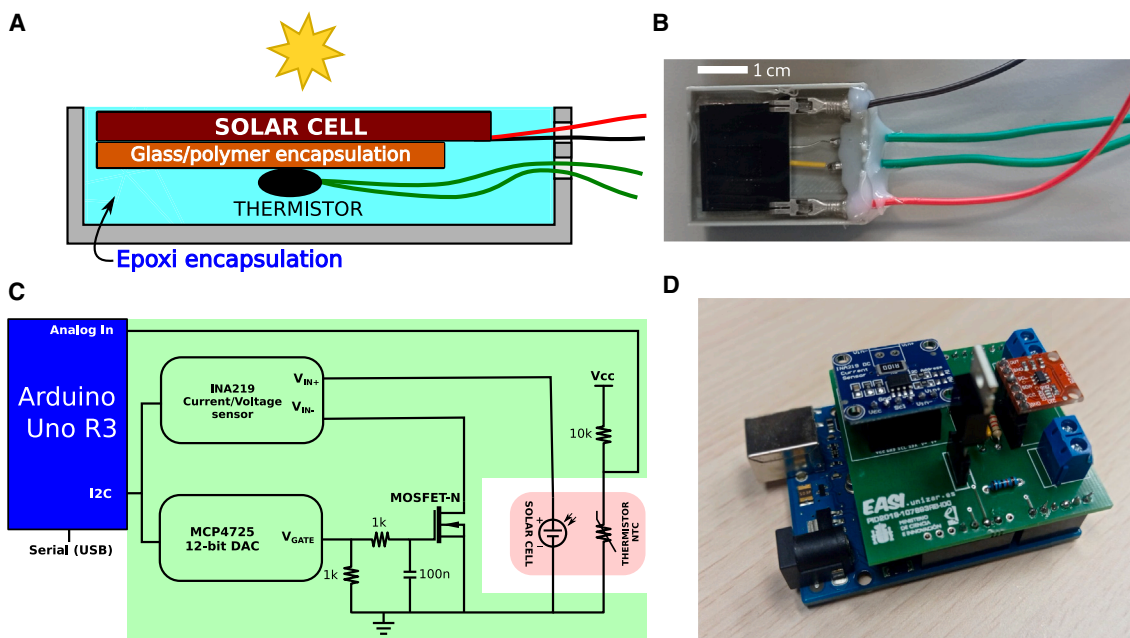
Figure 1. PSC assembly and tracker electronic scheme

(A and B) (A) Schematic cross-section of the assembled solar-cell device, and (B) top view of the physical device. Scale bar, 1 cm.

(C) Schematic representation of the Arduino board connected to INA219 and MCP4725 breakout boards, N-MOSFET, solar cell, thermistor, and USB serial connection to the PC. The pink zone highlights the encapsulated components referred in (B) and the green zone highlights components in the Arduino shield.

(D) Image of the Arduino device connected to the shield module containing the INA219 and MCP4725 breakouts, N-MOSFET, and screw terminal block connectors for solar cell and thermistor.

forward scan (from J_{SC} to V_{OC}, forward [FWD] JV) is lower in efficiency than scanning from V_{OC} to J_{SC} (backward [BWD] JV) as expected in hysteresis-normal devices.[22,43] Epoxy resin encapsulation and clamping cables decreased to ~5% the final PCE due to a deterioration in FF, specifically attributed to larger R_{SERIES} and photocurrent reduction as a result of the encapsulation process. The influence of R_{SERIES} on the FF can be described by the equation $FF = FF^0 \cdot (1 - R_{S0} \cdot I_{SC}/V_{OC})$, where R_{S0} and FF^0 denotes a series resistance and fill factor of reference. In our device measurements before and after encapsulation, the observed decrease in I_{SC} corresponds to an increase in R_{SERIES}. Consequently, this rise in R_{SERIES} contributes to the deterioration of the FF after encapsulation.

In the supplemental information, we have included JV curves and boxplots showcasing the main PV parameters extracted from the JV curve for all devices after HTE treatment and after tight epoxy encapsulation of the devices (Figures S1–S4).

While these devices might not feature exceptional efficiency within this particular typology, they demonstrate high reproducibility with commendable and consistent PCEs. The assembly process encompassing pre-laminated glass lids, sealing gaskets, soldered copper cables, attachment of NTC thermistor, and embedding in resin epoxy guarantees the robustness, reproducibility, and stability of these PSC devices, which is a crucial aspect for the MPPT tests outlined in this study.

Validation of the galvanostatic MPPT testing device

The hardware design of the power tracker system incorporates a hierarchical architecture comprising various components, each serving specific functions. The main
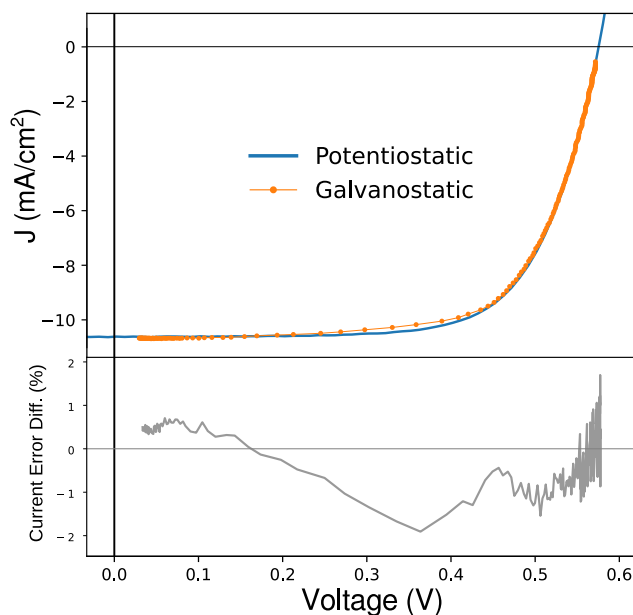
**Figure 2. Validation of galvanostatic approach via JV curve analysis**
Top: JV curve comparison for the Si solar cell recorded using two different techniques: Ossila potentiostat (blue line) and galvanostatic device (orange dotted line). Bottom: percentage error analysis between potentiostatic and galvanostatic methods, with J_{SC} normalized as 100% current reference. Illumination: LED solar simulator, 30 mW/cm^2.

components include an 8-bit microcontroller (ATmega328); a 12-bit digital-to-analog (DAC) converter (MCP4725) that generates an analog voltage that bias the gate terminal of an N-channel metal-oxide-semiconductor field-effect transistor (MOSFET) (IRLZ34N, 68 W maximum power dissipation); a 12-bit digital power monitor (INA219) that measures voltage and current of the photovoltaic device; and an NTC 10-kΩ thermistor (MF52) for monitoring the working temperature of the device. The microcontroller serves as the central processing unit driving the solar cell. Communication with this microcontroller is facilitated by a conventional computer, allowing firmware algorithm upload, data retrieval, storage, and data processing. This interaction is facilitated through a USB-based serial connection and external components, utilizing both digital and analog input/output pins, as depicted in Figure 1C.

The N-MOSFET plays a pivotal role acting as a variable electronic load driving the photovoltaic device in a galvanostatic manner because no controlled bias is applied in the photovoltaic device terminals.[44] In the typical setup, the photovoltaic device was connected in series with the drain and source terminals of the N-MOSFET, which is operated in its ohmic region by applying a continuous voltage in the gate terminal (V_{GATE}) by the DAC, which is commanded by the microcontroller enabling a variable load in the solar-cell terminals.

To verify the functionality of our galvanostatic-based MPPT testing device, we selected a commercially available single-crystalline silicon cell (1.18 cm^2) and the masked PSCs (0.64 cm^2). Figure 2 compares JV curves obtained using the Ossila potentiostat and those acquired with the galvanostatic-based MPPT hardware device developed in this work.

Galvanostatic and potentiostatic JV curves for the Si-cell device matched, well validating our hardware for JV measurements (supplemental information contains
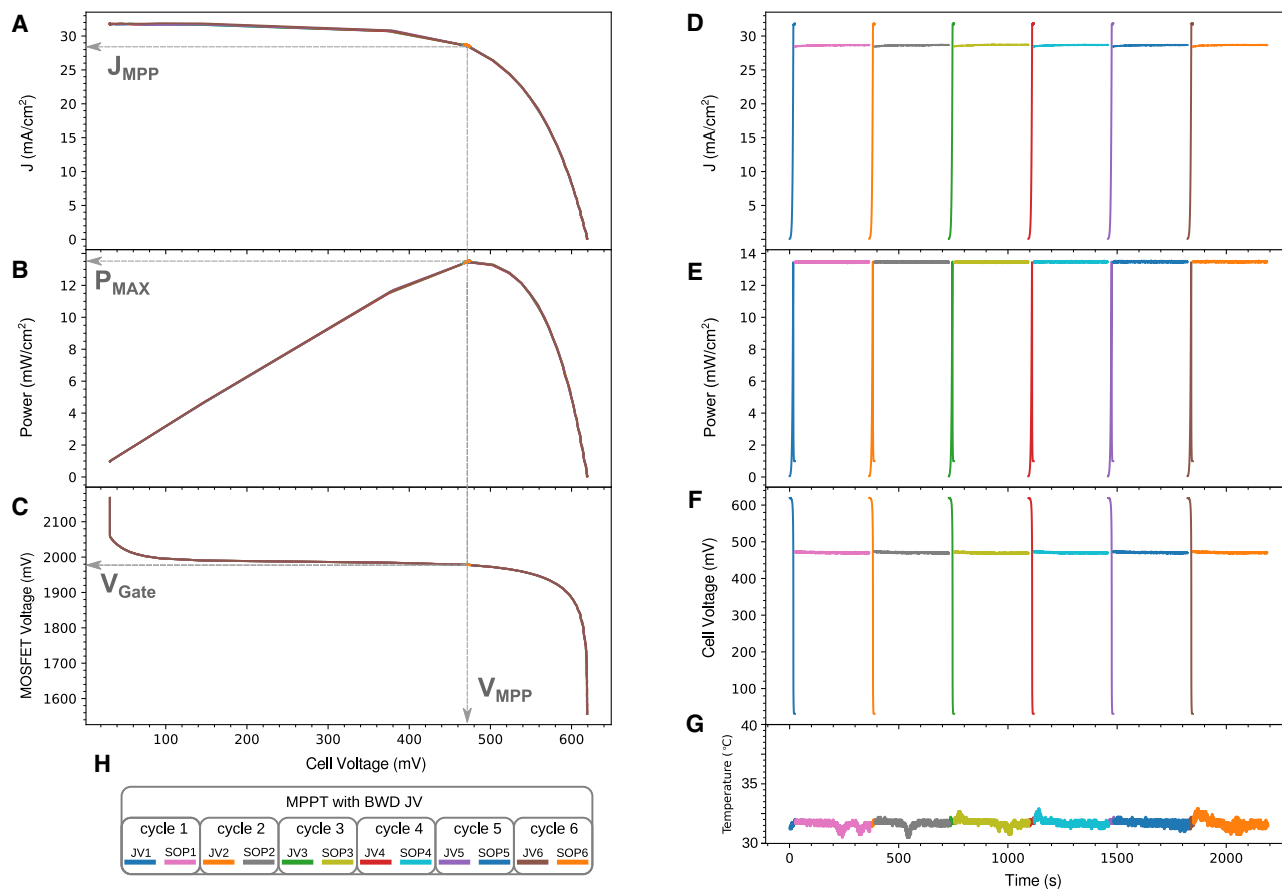
Figure 3. Validation of the galvanostatic MPPT testing device using a silicon solar cell

(A–C) (A) JV characteristics of the silicon solar cell under constant white LED illumination (~1 sun), (B) power output from the solar cell, (C) transfer function between the voltage measured in the solar cell and the voltage applied to the N-MOSFET gate (other transfer functions in Figure S6).

(D–F) Instantaneous (D) current density, (E) power, and (F) solar-cell voltage during the MPPT sequence alternating JV curves and SOP stages at V_{MPP}.

(G) Solar cell temperature during the MPPT sequence.

(H) MPPT sequence legend and color code for each stage.

JV curves and error analysis for 10, 30, 50, 70, and 100 mW/cm^2 irradiances; Figure S5).

It is relevant to emphasize that our galvanostatic JV measurement system, while highly effective for certain scenarios explained below, cannot replace the conventional potentiostatic JV measurement. For instance, the device lacks the capability to measure JV curves in dark conditions. This is because the absence of illumination means that no photocurrent is generated for the photovoltaic device, thus the N-MOSFET acting as variable resistor has no photocurrent to control. Also, V_{OC} and J_{SC} values in these galvanostatic JV curves are extrapolated values because the JV profile never can surpass the JV second-quadrant frontier values. Notwithstanding these drawbacks, this *passive* MPP tracker device will excel in measuring light-illuminated JV-SOP cycles for long-term operational stability tests.

In this context of MPPT testing, our focus shifted to the implementation of a basic P&O algorithm including determination of the JV curve of the device under illumination (Figure 3A), allowing us to find the maximum power attainable (Figure 3B) and its corresponding V_{MPP}. The V_{MPP} was then mapped univocally to a specific V_{GATE} to be applied
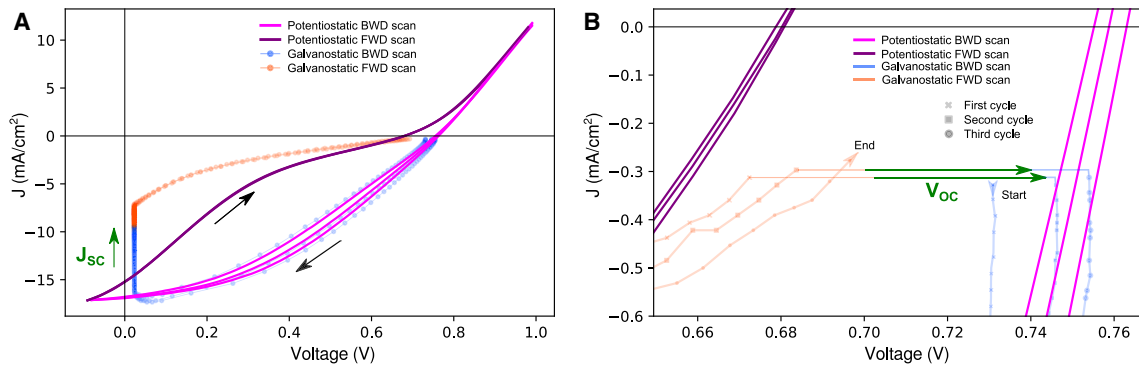
Figure 4. Comparison of galvanostatic- and potentiostatic-type JV measurements in PSC
(A) Three JV cycles from triple-mesoscopic or high-hysteresis PSCs recorded using a potentiostatic (—) or galvanostatic (-o-) technique. The green arrows highlight the transient dynamics of the recorded J_{SC} during galvanostatic measurement.
(B) Inset for the V_{OC} region in (A) illustrating the transient dynamics of the V_{OC} during galvanostatic measurement cycles (green arrows).

in the N-MOSFET (Figure 3C). Subsequently, the solar-cell device was subjected to the SOP stage setting the previously obtained V_{MPP} for 6 min. Figures 3D–3F show six cycles alternating JV scan and SOP stages in the silicon solar cell connected to our hardware. These cycles were used to record instantaneous current density (Figure 3D), instantaneous power output (Figure 3E), and instantaneous cell voltage (Figure 3F). Throughout this process, the solar cell maintained thermal equilibrium under illumination from a white light-emitting diode (LED), a state ensured by the attached thermistor (Figure 3G). This advantageous application of thermistors for temperature sensing would bear particular significance during outdoor experiments, as well as for maintaining precise thermal equilibrium during indoor measurements. Remarkably, our device indirectly sets V_{MPP} in the solar cell by leveraging the microcontroller's stored relationship between the measured voltage in the solar cell (INA219 sensor) and the V_{GATE} applied by the MCP4725 DAC in the gate of the N-MOSFET. However, there are other equivalent useful transfer functions relating V_{GATE} with current density, transimpedance, or power output from the cell (Figure S6). Overall, this validation test showcases performance and adaptability of our galvanostatic MPPT device for well-behaved solar cells (without hysteresis) offering a promising low-cost MPP tracker or power optimizer for enhancing solar energy harvesting.

Testing the low-cost galvanostatic MPPT tracker device on PSCs
After verifying the functionality of our hardware for performing JVs and the basic MPPT algorithm alternating JV-SOP sequence in a silicon solar cell, we applied it to the high-hysteresis triple-mesoscopic PSC. In comparison to the JVs conducted on the silicon solar cell (Figure 2), noticeable differences were observed between the potentiostatic and galvanostatic JVs (Figure 4A).

As observed, both types of measurements capture the hysteresis of the PSC device. The magnitude of hysteresis in PSCs is influenced by scanning speed, settling time, and recent bias history applied in the device.[22,24] The BWD (blue) JV branches of both measurements overlap well; however, the FWD (orange) curve produces a much lower current in the galvanostatic-type measurement. The explanation of this effect relies on the effective scan rate and preconditioning time experienced by the PSC during galvanostatic-type JV scan compared to potentiostatic one. Conventionally, potentiostatic JV curves can start from the first or fourth quadrant at constant voltage scan rate, inducing the so-called preconditioning stage. However, as explained above, our device is passive because it cannot obtain the JV curve of

a solar cell under dark conditions. And if illuminated, the device also cannot impose a negative bias value or a voltage higher than VOC on the solar cell terminals. The open state (low resistance, active state) of the N-MOSFET approximates the solar cell to output a quasi-J_{SC} current density, while close state (high resistance, cutoff region) induces quasi-V_{OC} voltage in the cell. The N-MOSFET acting as an electronically controlled variable load records the JV scan during the open-close transient or ohmic region. Indeed, the constant V_{GATE} scan speed implemented in the N-MOSFET does not lead to constant voltage scan rate applied at the cell terminals (Figure S6C). On other words, it is because the hysteresis index is not a valid metric for quantifying hysteresis in PSCs due to high dependence on JV scan conditions.[45] In the framework of this study and contrary to well-behaved Si solar cells, the most important aspect is that J_{SC} and V_{OC} are dynamic parameters and it holds paramount significance for the application of broadly implemented fractional J_{SC} and V_{OC} MPPT methods. Figure 4A clearly shows the decrease of J_{SC} (green arrow) when the N-MOSFET is set to low-resistance state. Photocurrent transients and their response shape during on/off light switching are related to charge generation, collection, and polarization and recently this response has been ascribed to a delayed photocurrent mode produced by a photoinduced chemical inductor.[46] Recently, a systematic review of the Perovskite Database has uncovered a consistent 4% discrepancy in J_{SC} values derived from JV and external quantum efficiency (EQE) measurements.[47] The J_{SC} dynamic behavior during EQE measurements, where the device is kept continuously short circuited, results in a lower integrated J_{SC} value. On the other hand, there is an increase of V_{OC} when the N-MOSFET is set to high-resistance or close state (Figure 4B).

Given the strong significance for the upcoming sections, it is important to note that the presence of substantial hysteresis in the JV creates a loop inside the quadrant. It means that the device can produce identical current levels at two different voltage states, depending on whether it follows the BWD or FWD JV branch. In contrast with the hysteresis observed during the potentiostatic scan, the galvanostatic hysteresis can be said to exhibit a more relaxed behavior. This aspect becomes particularly crucial when attempting to track the MPP of the solar cell using a variable resistor regulating the current output of the device.

Research articles on the PSC topic often present JV curves of PSCs, including the PCE data for both FWD and BWD JV curves as benchmark. However, a crucial challenge arises when attempting to determine the MPP of the cell: should it be based on the BWD or FWD JV curve? In this study, we investigate this ambiguity by employing the conventional potentiostatic approach for JV-SOP cycles of PSC (Figure 5), which later will help to understand the advantages of applying a galvanostatic approach for this task.

As before with the Si solar cell, the sequence commences by identifying the V_{MPP} after converting the JV curve (Figure 5A) into a power-voltage curve (Figure 5B) effectively displaying the peak power achievable. Subsequently, the V_{MPP} value is established within the potentiostat to initiate an SOP stage, which persists for a duration of 120 s. Figure 5 shows six cycles, each alternating between JV curve (three BWD + three FWD type) and SOP stages. These cycles were used to record instantaneous current density (Figure 5D), instantaneous power (Figure 5E), and voltage applied in the cell by the potentiostat (Figure 5F). Throughout the process, the device remained in thermal equilibrium (Figure 5C).

Depending on whether a BWD or FWD type JV scan is conducted, V_{MPP} is ~0.35 V or ~0.45 V, respectively. As expected, the potentiostat fixes the V_{MPP} in the solar cell
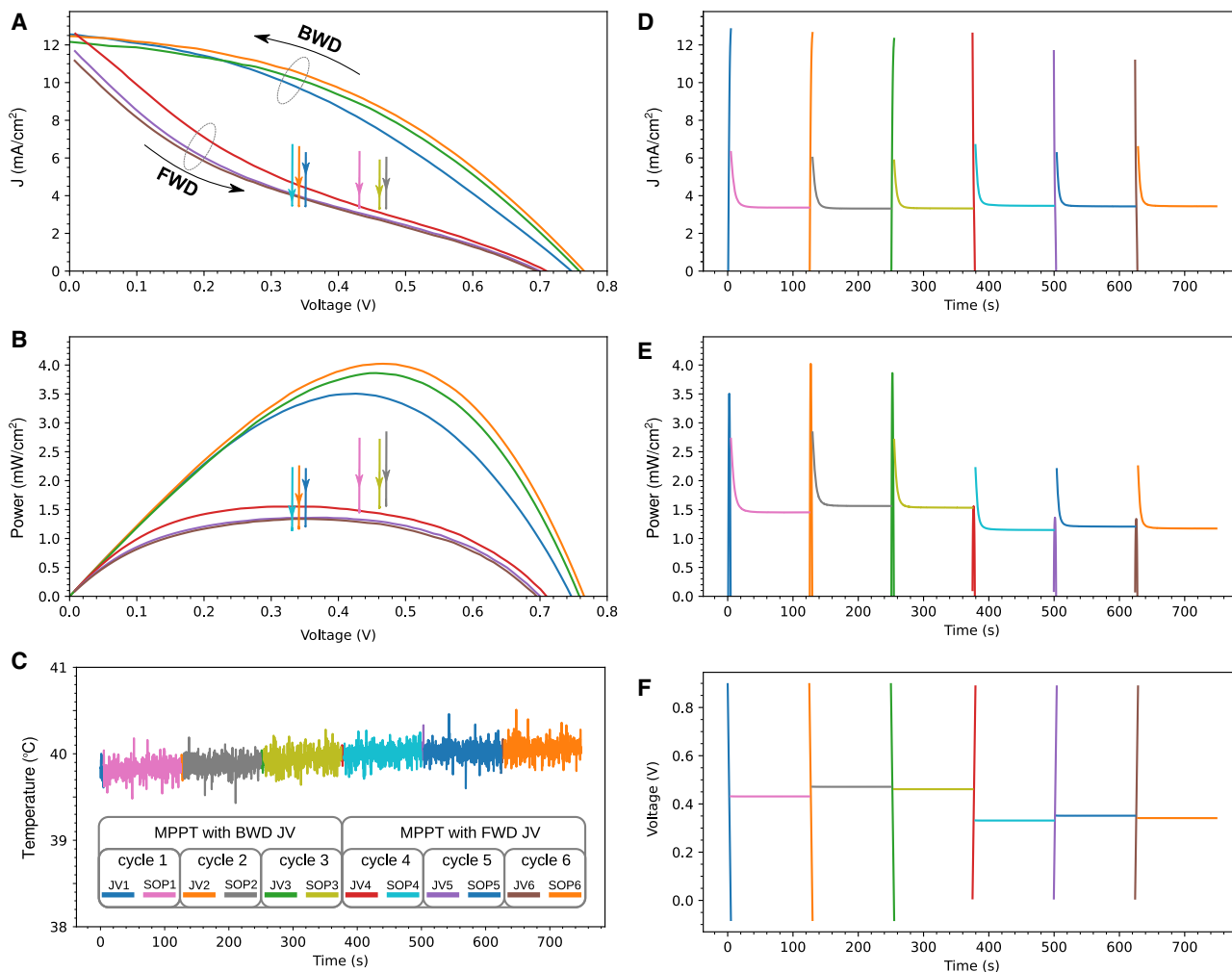
Figure 5. Six cycles of MPPT using the potentiostatic approach in PSC

First three cycles using a BWD JV for V_{MPP} determination and the last three cycles using FWD JV scans. The SOP stage has 120 s of duration.
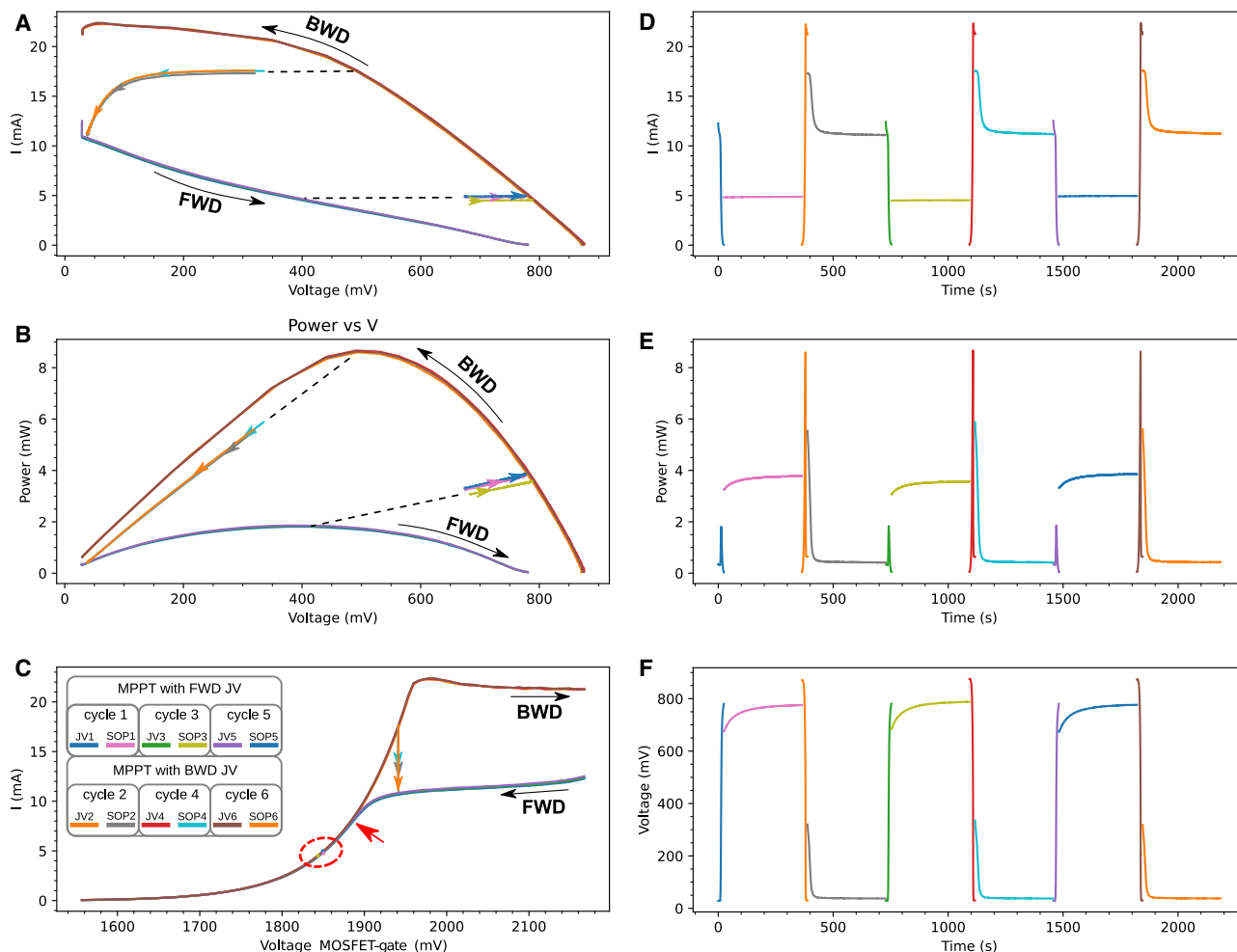
(A) JV characteristics of the triple-mesoscopic PSC under LED solar-simulator (LSH-7320, Newport, AM1.5G, 100 mW/cm^2) illumination. SOP stages in this panel appear as vertical lines with the arrowhead pointing to the current drifting in time.

(B) Power output curve from the solar cell during JV scans. SOP stages in this panel appear as vertical lines with the arrowhead pointing to the power output drifting with time.

(C–F) (C) Solar-cell temperature during the MPPT sequence. This contains the legend and color code for all figures with the sequence of cycles,

(D) instantaneous current during the MPPT sequence alternating JV curves and SOP stages at V_{MPP}, (E) instantaneous power during the MPPT sequence alternating JV curves and SOP stages at V_{MPP}, and (F) instantaneous voltage applied in the cell during the MPPT sequence alternating JV curves and SOP stages.

during the SOP stage. Noteworthy, the highest power peak achieved during the BWD JV stage is not attained during the SOP stage. It progressively declines over time (Figures 5E and 5B as indicated with arrows). The decline in power observed during the SOP stage at fixed V_{MPP} is solely attributed to the reduction of the current density output from the cell (Figure 5D). Interestingly, the current steadily decays until it reaches values comparable to those in the FWD branch during JV tracing stage (Figure 5A) and power decays until it reaches values comparable to those in the FWD branch of the power-voltage curve (Figure 5B). Therefore, FWD JV curves offer a more realistic representation of the actual PCE for devices exhibiting significant hysteresis. However, it should be noted that setting the BWD V_{MPP} still results in a power output that is marginally higher compared to V_{MPP} from the FWD branch. This raises

Figure 6. Six cycles of MPPT using the galvanostatic approach in PSC

Cycles 1, 3, and 5 (2, 4, and 6) use an FWD (BWD) JV scan for V_{MPP} determination. The SOP stage lasts 360 s.

(A) JV characteristics of the triple-mesoscopic PSC under white LED illumination. SOP stages appear as horizontal lines with the arrowhead pointing to the voltage/current drift in time. Dashed black line helps to indicate the V_{MPP} origin.

(B) Power-output curve from the solar cell during JV scans. SOP stages appear as lines with the arrowhead pointing to the power output drifting with time. Dashed black line points to the V_{MPP} origin.

(C–F) (C) Solar-cell current depending on the voltage applied in the MOSFET gate. SOP stages after BWD JV scan appear as dots (inside the red dashed circle). Red arrow indicates the optimal gate voltage to maximize power extraction of the cell. See text for details. This contains the legend and color code for all figures with the sequence of JV-SOP cycles, (D) instantaneous current, (E) power, and (F) voltage measured in the cell during the MPPT sequence alternating JV curves and SOP stages.

two important questions: is there a possibility of achieving a better PCE from the FWD branch in devices with significant hysteresis? If so, what algorithm could be employed to determine the true MPP of high-hysteresis devices?

This MPPT potentiostatic study highlights the limitations of traditional MPPT algorithms when applied to high-hysteresis PSCs. Instead of the conventional potentiostatic method above, we attach our galvanostatic-based MPPT tracker to drive the PSC utilizing the JV-SOP sequence under illumination (Figure 6). Six galvanostatic JV-SOP cycles alternated V_{MPP} extraction from FWD- or BWD-type JV curves followed by an SOP stage at V_{MPP}. As explained before for JV scan, the galvanostatic method cannot impose a voltage in the solar-cell terminals during the SOP stage but control the current flowing out from the cell through the drain/source terminals of

the N-MOSFET acting as variable resistor. This variable resistor imposes in the device the load producing the J_{MPP} recorded during the JV stage, which at the end fixes the maximum current flowing in the circuit.

It is observed that only the cycles using FWD-scan-type JV offers a stable point of electric power generation during its SOP stage (SOP1, SOP3, and SOP5; Figures 6B and 6E) while in the MPPT cycles using BWD-type JV for V_{MPP} determination, current and voltage decrease to almost no electric power generation during its SOP stage (SOP2, SOP4, and SOP6; Figures 6B and 6E). This drifting behavior is due to the determined V_{MPP} as starting point for the SOP stage. The transfer function between applied V_{GATE} vs. current output from device (Figure 6C) helps to understand this current drift from the device as follows: if the V_{MPP} determined from BWD JV requires a $V_{GATE} > 1,900$ mV during the SOP stages, the current output of the device will drift until the corresponding current is obtained from the FWD JV (cyan, purple, and orange arrows in Figure 6C). Instead, if the V_{MPP} determined from an FWD JV requires a $V_{GATE} < 1,900$ mV, the match of the BWD and FWD branch in the transfer function avoids any current drift (dots surrounded by dashed red circle in Figure 6C). Interestingly, we demonstrate that using a galvanostatic technique controlling the current output of the device simplifies the MPP tracking process. It results in a considerable increase in power extraction due to the "floating" voltage output naturally increasing from the cell using this technique compared with the conventional potentiostatic MPPT algorithm fixing V_{MPP} during the SOP stage (floating current, but it only can decrease as shown in Figures 5A and 5B). As observed in Figures 6B and 6E, the galvanostatic method produces roughly ~100% increase of the power compared to the obtainable power-voltage FWD curve but is still ~ 50% below that predicted by the power-voltage BWD curve. Note that this improvement relies on the hysteresis grade suffered by the cell. Lower or null hysteresis will imply lower or null improvement.

Due to the evolution to better output powers over time during SOP1, SOP3, and SOP5 stages, the question arose again whether it would be possible to determine an even better V_{MPP} starting point for the SOP stage. Looking at Figure 6C, we observe that there is a margin to raise the current output of the device by raising the V_{GATE} up to the frontier where BWD and FWD transfer function matches, still avoiding current drift appearing with $V_{GATE} > 1,900$ mV (red arrow, Figure 6C). First, we try to drive manually the N-MOSFET to reach this point. The Arduino controller outputs the data to the computer using the serial USB connection but also this connection allows inputs by hand to drive the V_{GATE} applied as required in the MOSFET. Then, we can control "on the fly" the variable resistor and consequently the output current from the cell. Figure 7 shows a manual control of this V_{GATE} resulting in an improvement of the power output of the cell. Using this manual control to load the cell, we can drive an SOP stage after FWD JV to increase the power output by ~200% compared to theoretical power from the FWD JV curve (Figures 7B and 7E, cycle 1). However, this power output remains below (approximately −40%) the theoretical power from the BWD JV curve. Interestingly, we can recover manually a failed SOP stage from BWD JV curve to this largest power output produced during cycle 1 (Figures 7B and 7E, cycle 2). Figure S7 shows the transfer curves for this manual operation.

The implementation of the algorithm for the automatic search of this optimal V_{GATE} driving the current needs a transfer function that relates V_{GATE} to (1) output current (Figure 6C), (2) output voltage (Figure 8A), or (3) power output from the cell
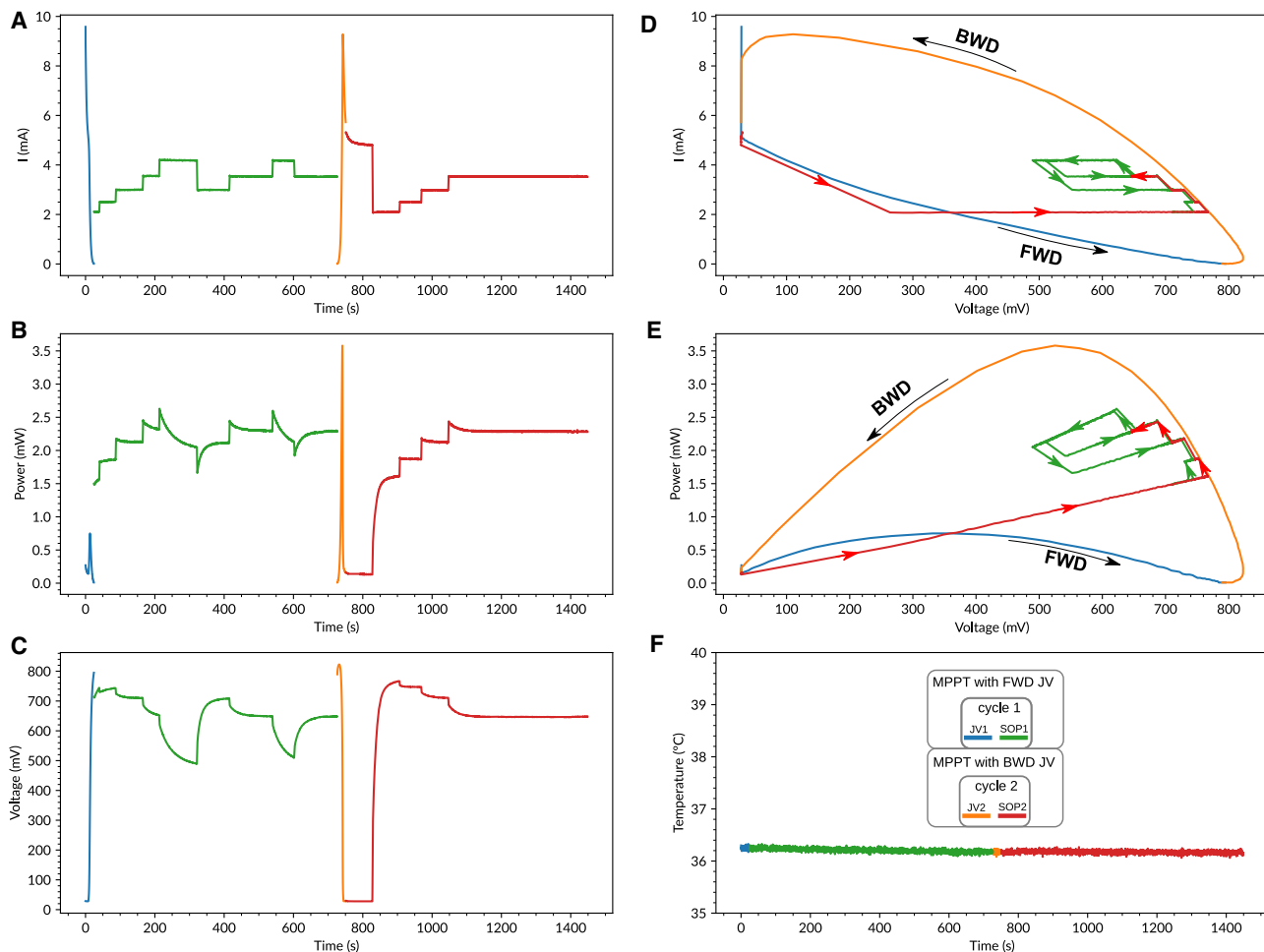
**Figure 7. Two manual MPPT cycles using the galvanostatic approach in PSC**

Cycle 1 (2) uses an FWD (BWD) JV scan for early V_{MPP} determination. After that, the SOP stages last 720 s and several V_{GATE} input commands by hand are sent to the N-MOSFET to control the output current or active load in the cell terminals.

(A–C) (A) Instantaneous current, (B) power, and (C) voltage during the MPPT sequence alternating JV curves and SOP stages under manual control.

(D and E) (D) Current-voltage (IV) curve and (E) power output curve from the solar cell during JV scan stage. SOP stages show a dynamic behavior due to the manual control of the V_{GATE} with the arrowhead pointing to the voltage/power/current drift time evolution.

(F) Solar-cell temperature during the MPPT sequence. This contains the legend and color code for all figures with the sequence of JV-SOP cycles.

(Figure 8B). The MPP search using the transfer function in Figure 6C is problematic, because it requires a threshold describing the frontier point at which to discern matched and unmatched FWD and BWD curves. The option of using the transfer function V_{GATE} vs. output voltage is more promising (Figure 8A). Here, the optimal V_{GATE} can be found by seeking the voltage at which the maximum difference between the BWD and FWD appears (Figure 8A, purple line, red arrow). Another procedure to obtain this point is using the transfer function V_{GATE} vs. cell output power to average the V_{GATE} for all FWD and BWD maximum power points (Figure 8B, red arrow). This last approach stands out as the most robust, as it remains agnostic regarding the presence or absence of hysteresis within the solar cell. For instance, a Si cell matches closely both BWD and FWD curves in all their transfer functions due to the absence of hysteresis (Figure S6). Therefore, this optimal point determination is impossible to find by looking for mismatch in the transfer curves. However, the maximum power output is univocally ascribed to the same specific V_{GATE} for both FWD and BWD power curves.
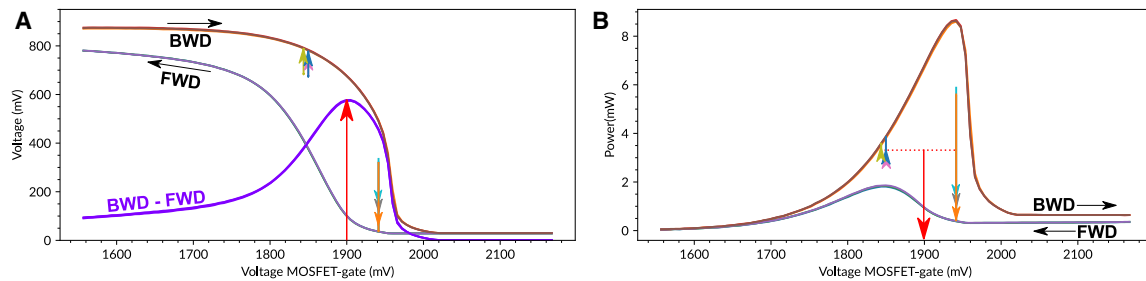
Figure 8. Determination of optimal V_{GATE} for MPP in PSC

(A) V_{GATE} vs. cell voltage and (B) V_{GATE} vs. power output transfer functions. Line color for BWD, FWD JVs, and SOP stages follows legend in Figure 6. Red arrow indicates optimal V_{GATE} to drive the output current from the cell. Purple line in (A) shows the difference between BWD and FWD traces; see details in the text.

With all this in mind, the power output vs. V_{GATE} transfer function serves as the appropriate transfer function for automating the MPP search process as Figure 8B demonstrates. It is noteworthy to mention that Pellet et al.,[34] in their work employing a potentiostatic hill-climbing algorithm, discovered that the optimal V_{MPP} slightly surpassed the V_{MPP} derived from JV curves. In contrast, the galvanostatic approach here directly ascertains this slightly above V_{MPP} without the need of iterative procedures. Figure 9 illustrates three JV-SOP cycles implementing the algorithm, each under distinct power-illumination conditions, showcasing the automatic search and optimization of V_{GATE} for achieving the MPP.

Under automatic MPP search of the triple-mesoscopic PSC under three different white LED power illumination, the SOP stages still show a lower but overall stable dynamic behavior due to the optimal V_{GATE} found. For the good performance of this automatic search of the MPP in a PSC with high hysteresis, both BWD and FWD JV scan must be determined before the SOP stage. Interestingly, we found that it is convenient to scan BWD-FWD JV loops instead of FWD-BWD loops to achieve the optimal power output more quickly because the cell keeps the high-voltage state at end of a BWD-FWD JV loop. Figure S8 shows 10 JV-SOP cycles implementing the algorithm with automatic search of the optimal V_{GATE} under the same illumination conditions, illustrating the convenience of BWD-FWD JV loops.

Implementation of the algorithm in potentiostatic mode

In principle, there is not a direct way to discover directly and without hill-climbing iteration this optimal output current by using potentiostatic JV measurements. However, we can circumvent this impediment with a workaround making use of the lesson learned using the galvanostatic approach. The proxy method would be to average $J_{MPP,BWD}$ and $J_{MPP,FWD}$ obtained potentiostatically as $J_{MPP,AVG}$ being $VJ(J_{MPP,AVG}) = V_{MPP}$ (where VJ() is the inverse function of JV()). A graphical derivation of this approach is shown in Figure S9.

Implementation of the algorithm for outdoor performance or variable irradiation

JV-SOP cycles at MPP are generally limited to research contexts for short-term stability tests using constant irradiation where JV-derivable PV parameters such as V_{OC}, J_{SC}, FF, R_{SERIES}, and R_{SHUNT} need specific monitoring over time. Practical MPPT algorithms in real-world applications do not require a full JV-curve analysis for MPP determination, as this approach is time consuming and results in suboptimal power production from the solar cell.
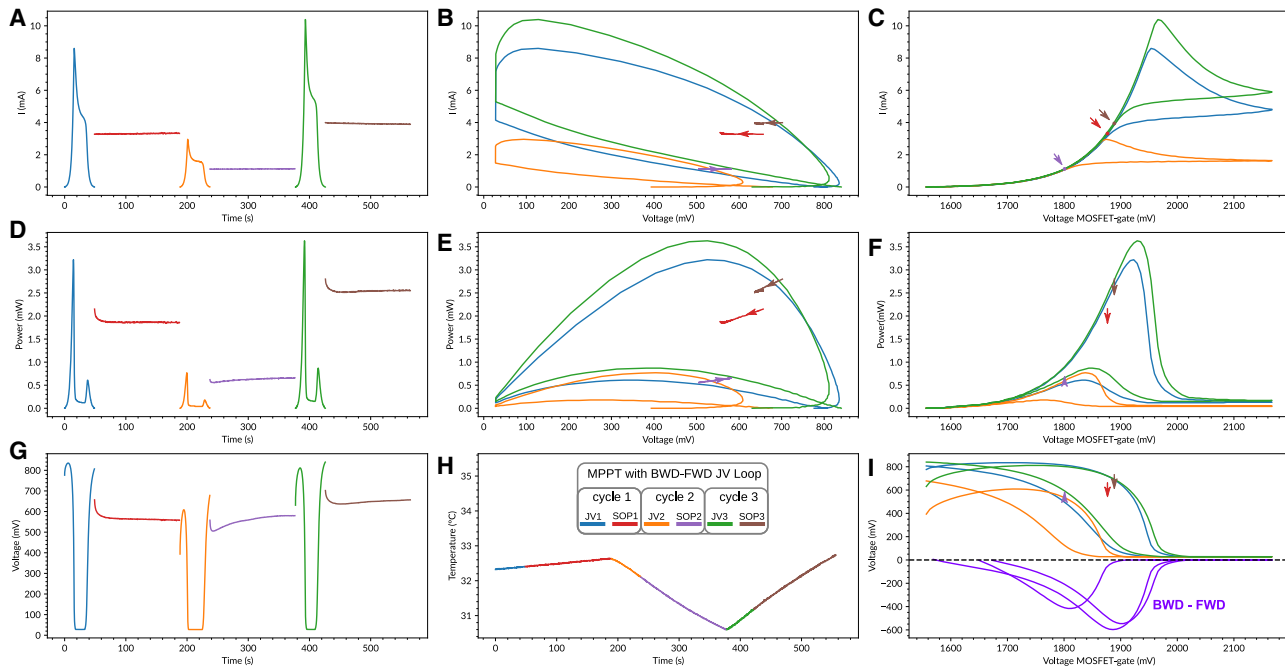
Figure 9. Three automatic MPPT search cycles using the galvanostatic approach and power vs. V_{GATE} transfer curve under three different light power irradiations

Cycles used BWD-FWD JV scan loops for optimal V_{MPP} determination. After that, the SOP stages last 120 s.

(A–C) (A) Instantaneous current, (B) voltage, and (C) power during the MPPT sequence alternating JV loop and SOP stages under automatic MPP search.

(D and E) (D) JV and (E) power-voltage curve output from the solar cell during JV scans. SOP stages show minor dynamic behavior due to the automatic control of the V_{GATE} with the arrowhead pointing to the voltage/power drift time evolution.

(F) Solar-cell temperature during the MPPT sequence. This contains the legend and color code for all figures with the sequence of JV-SOP cycles.

(G–I) V_{GATE} vs. cell (G) current, (H) power, and (I) voltage transfer functions.

In this study, we tested the capability of the microcontroller to drive a well-behaved Si solar cell under one 30- to 100-mW/cm^2 irradiation cycle (EN 50530 standard[48,49]) by implementing a fixed increment P&O MPPT algorithm.[26–29] Our MPPT hardware implementation regulated the cell current output through V_{GATE} modulation, deviating from the traditional practice of controlling the cell voltage output. Despite this difference, this device can run any direct-type MPPT algorithms uploaded within the microcontroller. Our test achieved an MPP efficiency (η^{MPP}) of 98.81%, consistent with typical outcomes of the P&O MPPT algorithm in Si cells (Figure S10).

We now focus on high-hysteresis cells such as triple-mesoscopic PSCs and use the conventional fixed-increment P&O MPPT algorithm guided by the galvanostatic approach. We applied the same 30- to 100-mW/cm^2 irradiation cycle following the EN 50530 standard as before in the Si cell. The results indicate unstable operation and power output oscillation as noted before for PSCs (Figure S11).[33–36] Subsequently, we adapted the standard algorithm to include a feedback validation process ensuring the algorithm's precision in device control. In summary, the typical P&O approach navigates through its decision tree by assessing power output increments at steps *k* and *k+1*. Our adaptation involves reevaluating again step *k* prior to the subsequent cycle to confirm the sign of the V_{GATE} yields an improved power output from the cell (Figure 10).

Based on our understanding, Figure 10 shows, for the first time, a P&O MPPT algorithm driving a real PSC (no PV model circuitry) under EN-50530-type variable illumination conditions.
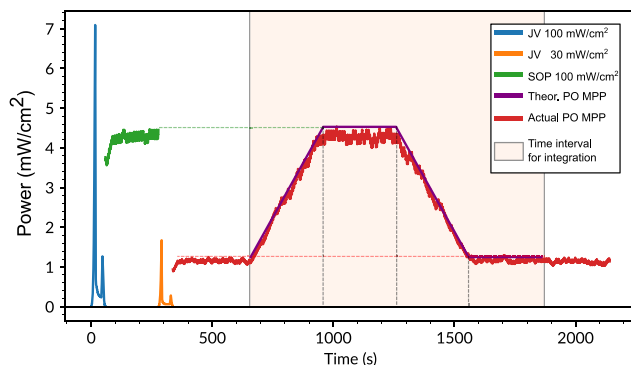
Figure 10. Fixed increment P&O MPPT with *k* feedback using the galvanostatic approach in PSC
The PSC is under one cycle of variable illumination 30/100 mW/cm^2 using 300 s of ramping and dwelling stages. In blue (orange), the 100 (30) mW/cm^2 BWD-FWD JV scan loop for optimal initial V_{MPP} determination. In red (purple), the actual (perfect) instantaneous power output. η^{MPP} = 95.02%. V_{GATE} transfer functions are shown in Figure S12.

The fast or slow response of our P&O algorithm implemented in our tracker depends on three parameters: (1) number of averaged measurements per data point (β), (2) number of averaged data points constituting a *k*-step (δ), and (3) number of discrete levels of the 12-bit DAC separating two consecutive *k*-steps (ε). One discrete level in our implementation corresponds to 5,000/4,096 ∼1.22-mV maximum resolution in the V_{GATE}. A variation of approximately ±1 mV in V_{GATE} can lead to a maximum voltage cell change of around ±40 mV in the vicinity of V_{MPP}. Conversely, outside the ±40-mV V_{GATE} window centered on V_{MPP}, the voltage cell change is limited to ±1 mV or lower. We used β = 60, δ = 10, and ε = 2 for the Si cell and PSC EN-50530 variable illumination tests above (2.33 W/m^2·s slope of variable illumination). The parameters β and δ jointly determine the time required to achieve a *k*-step (overall sampling frequency), while ε influences both the amplitude of inherent oscillations in P&O algorithms and the algorithm's rate of convergence toward the optimal output. A sampling frequency below 200 ms is typically optimal for well-behaved Si and thin-film cells under rapid changes in irradiation. In our algorithm, the decision to increase or decrease V_{GATE} (ε) to track the MPP is made approximately every 2 s (β and δ).

Enhancements to this algorithm include the ability to capture rapid changes in illumination through the fine-tuning of β and δ parameters as well as the exploration of variable ε instead of the current fixed discrete level step.[50] It is important to note that these advancements extend beyond the current scope of this study. Our ongoing research is focused on this optimization of the algorithm and deploying this tracking device to study long-term operational stability of PSCs under outdoor conditions.

In this study, we developed a galvanostatic MPPT device aimed at enhancing the PCE of high-hysteresis PSCs more rapidly compared to the potentiostatic approach. The algorithm and hardware introduced in this work have the potential to democratize and streamline both outdoor and short-term operational stability measurements in the laboratory, propelling the advancement of emerging photovoltaics characterized by substantial JV hysteresis. Moreover, the integration of galvanostatic power optimizers employing this MPP search algorithm with the solar panel prior to the inverter could potentially enable the commercial viability of extremely low-cost carbon-based PSCs afflicted by high hysteresis. This device allows cost-effective testing of solar cells, with an estimated cost of approximately 10 USD per device. The

primary cost contributors include the microcontroller, voltage-current sensor, and DAC. The resulting device is compact, portable, and easily integrable into a glove box or for unattended outdoor measurements, featuring provisions for a memory card for data storage and a battery. Device temperature, monitored via a thermistor and integrated into the circuitry of the tracker, is crucial for hybrid halide perovskites' long-term stability measurements. On the firmware side, we utilized an open-source electronics platform, specifically Arduino, to facilitate user-friendly hardware and software modifications. Additionally, leveraging in an open-source language such as Python (and associated libraries for data collection/storage/calculations and graphing) promotes extensive user engagement, encouraging continuous development and enhancement opportunities for other researchers in the PSC field.

In conclusion, our study offers a fresh perspective on the significance of MPPT tracking algorithms in the context of PSCs. By prioritizing cost-effective hardware solutions and employing a galvanostatic approach, we have demonstrated the efficacy of this method in efficiently reaching the MPP, particularly in high-hysteresis PSCs. Our findings challenge the conventional notion that MPPT algorithms are solely responsible for mitigating the hysteresis effect in PSCs. Instead, we advocate for a deeper consideration of the operating mode of these algorithms, emphasizing the importance of implementing galvanostatic approaches to achieve optimal performance. Through this paradigm shift, we aim to shift the focus from merely overcoming hysteresis to identifying the best assembly strategies for the most stable devices, paving the way for future advancements in PSC technology.

EXPERIMENTAL PROCEDURES

Resource availability

Lead contact
Requests for further information should be directed to the lead contact: Emilio J. Juarez-Perez (ejjuarezperez@unizar.es).

Materials availability
All PSCs were assembled utilizing the full Solaronix kit for the triple-mesoscopic PSC. The MPP tracker assembly involved standard electronic components detailed in subsequent sections.

Data and code availability
A frozen first-release version of all codes, diagrams, and schematics used in this study is deposited in the Zenodo repository (https://doi.org/10.5281/zenodo.10647187) and also GitHub repository (https://github.com/ej-jp/perovskino) for encouraging further development and contributions from the interested research community. Any additional queries may be addressed to the lead contact.

JV curve and operational stability measurement setup
The JV measurements were performed under simulated sunlight illumination using an LED solar simulator (LSH-7320, Newport, AM1.5G, 100 mW/cm^2). A commercial white LED was also eventually employed as a light source by matching the equivalent photocurrent in the device to 1 sun of simulated illumination power, which is explicitly stated in the JV or MPPT measurement. For the potentiostatic-type measurement, a source-meter unit (X200, Ossila) was used connected in series with the device. The JV characteristics of the PSC and a commercial monocrystal silicon single solar cell (KXOB22-12X1, IXYS, 1.18 cm^2), acting as a reference of hysteresis-free device, were acquired through voltage sweeps from −0.1 to 1.2 V and −0.1–0.65 V, respectively. The voltage step used an increment of 10 mV and a

stabilization time of 0.005 s. The galvanostatic JV measurement of the solar cells were conducted using the custom hardware developed as part of this study and detailed in the following section.

Independently of the potentiostatic or galvanostatic method used, a JV curve was recorded where J_{SC}, V_{OC}, FF, and PCE of the solar cells were calculated using the formula: PCE (%) = $(J_{SC} \cdot V_{OC} \cdot FF) \cdot 100/P_{IN}$, where J_{SC} is the short-circuit current density, V_{OC} is the open-circuit voltage, FF = $(V_{MPP} \cdot J_{MPP})/(V_{OC} \cdot J_{SC})$ is the fill factor, and P_{IN} is the incident power density. V_{MPP} and current density at the maximum power output (J_{MPP}) were determined as the voltage and current corresponding to the maximum power output ($P_{MAX} = V_{MPP} \cdot J_{MPP}$) achieved by the photovoltaic device, respectively. Series (R_{SERIES}) and shunt resistance (R_{SHUNT}) were extracted from the JV curve fit using the single-diode model in Grapa.[51]

Photovoltaic operational stability measurements of the device under potentiostatic or galvanostatic conditions were conducted using the P&O MPPT algorithm in two different modes of operation. The first mode involved alternating full JV scans to ascertain the V_{MPP} (or J_{MPP}), followed by a stage of SOP at V_{MPP} over a defined time interval. Multiple consecutive JV-SOP cycles were performed to ensure consistency and stability of the solar cell. The purpose of this first mode was using MPPT techniques for performance evaluation of PSCs under constant illumination (section "testing the low-cost galvanostatic MPPT tracker device on PSCs"). The second mode involves the conventional implementation of the P&O MPPT algorithm for outdoor performance under varying irradiation conditions (section "implementation of the algorithm for outdoor performance or variable irradiation"). It employs a fixed-step voltage increment for perturbation. In this work, the device using the second-mode P&O algorithm underwent a variable irradiation sequence test in compliance with the EN 50530 standard.[48,49] This test protocol comprised a single cycle, delineated into four distinct phases. First, there is a gradual increase in irradiance, transitioning from 30 to 100 mW/cm² over a duration of 300 s. Subsequently, the irradiance level is maintained at a constant 100 mW/cm² for the following 300 s. Next, a decline in irradiance is implemented, returning to 30 mW/cm², again spanning a 300-s interval. Finally, the irradiance level remains fixed at 30 mW/cm² for an additional 300 s.

Firmware design

For firmware development and microcontroller upload, the Arduino Integrated Development Environment (IDE) was utilized. This IDE offers a user-friendly interface for code writing, compiling, and uploading to the Arduino microcontroller. The firmware code was written in the Arduino programming language, which is based on the C/C++ programming language, enabling efficient control and operation of the system. Python scripts were developed for collecting USB serial data from the Arduino to the computer and performing postprocessing for graphical representation (matplotlib). The firmware in this work implements the first- and second-mode operation of the P&O MPPT algorithms for the microcontroller. However, using an open-hardware/software platform, users can modify the microcontroller's firmware to run custom algorithms for short-term stability assessment, such as the asymptotic P_{MAX} scan,[32] dynamical IVs,[31] or more advanced transient MPPT sequences.[30]

Codes deposited in the Github or Zenodo repository provided in-depth details about the selection process for the appropriate TTL-level N-MOSFET considering specific requirements and criteria for the Arduino platform and a calibration procedure for the INA219 sensor. One potential limitation of the proposed galvanostatic MPPT approach for PSCs is the need for careful calibration of this current/voltage

sensor to ensure accurate and reliable performance. Since this method controls the current instead of the voltage bias, precise calibration of the current control loop is essential to achieve optimal power tracking. Any inaccuracies or drift in the current control loop could lead to suboptimal tracking of the MPP, reducing the overall efficiency of the system.

From a technical standpoint, the INA219 voltage/current sensor utilized in our MPPT tracker imposes sensing constraints. Specifically, INA219 cannot measure voltages above 26 V or currents exceeding 3.2 A, limiting its capability to measure modules delivering up to 83.2 W of power. Additionally, the MOSFET, serving as the variable resistance for power dissipation, is rated to handle a maximum power of 68 W, underscoring the need for careful consideration when optimizing the tracker for PSC modules with higher power ratings.

Circuit diagrams were created using computer-aided design free software (Fritzing) and the design deposited in the Github or Zenodo repository. The circuits were then checked in a prototyping breadboard and then a custom printed circuit board shield was created for the Arduino. Gerber files are deposited in the Github or Zenodo repository.

The codename of the device (Arduino + shield) is Perovskino (Figure 1D) and the algorithms implemented are floating-voltage or passive/galvanostatic-approach methods.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.xcrp.2024.101885.

AUTHOR CONTRIBUTIONS

Conceptualization, E.J.J.-P.; software, E.J.J.-P.; electronic circuit validation, R.C.; investigation, E.J.J.-P.; data curation, E.J.J.-P.; writing – original draft, E.J.J.-P.; writing – review & editing, E.J.J.-P., M.H., C.M., and R.C.; visualization, E.J.J.-P. and C.M.; supervision, E.J.J.-P.; funding acquisition, M.H., E.J.J.-P., and R.C.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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