# Characterization of 65-nm CMOS Integrated Resistors in the Cryogenic Regime

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*Abstract*— This article presents the experimental characterization and modeling of CMOS resistors in a temperature range extending from room temperature (300 K) down to the deep cryogenic regime at 4 K. A set of poly-silicon resistors with different bulk structures and sizing have been fabricated in a 65 nm CMOS process and their *I*–*V* curves have been obtained experimentally in the 4 to 300 K range with a temperature step of only 0.5 K to obtain a large set of resistance values equally distributed along the temperature range. The plot of the resistance values against temperature has allowed us to obtain the temperature coefficient  $\alpha(T)$ of the different resistors in the whole temperature range down to 4 K. Interestingly, for all the measured resistors the  $\alpha(T)-T$  curves show a change in tendency for temperatures spanning from 66 to 98 K, this is, in the vicinity of the condensation temperature of nitrogen  $(77 K)$ , where most of the thermal contraction of materials occurs.

*Index Terms*— Cryo-CMOS, cryogenic measurement, quantum technologies.

### I. INTRODUCTION

**QUANTUM** computing is expected to overcome classical computing in situations of increased complexity. Nowadays, the most commonly used realization of qubits are superconducting qubits, UANTUM computing is expected to overcome classical computing in situations of increased complexity. Nowadays, the semiconductor qubits, or spin qubits based on magnetic molecules, and all of them need to operate in the deep cryogenic regime at a few mK to extend their coherence time. These conditions bring strong challenges in the design of the control and readout electronics of quantum computers, which usually operate at room temperature.

<span id="page-0-3"></span><span id="page-0-2"></span>Recent studies [\[1\],](#page-2-0) [\[2\]](#page-2-1) have demonstrated that CMOS devices can be used to implement full systems with power dissipation levels at deep cryogenic temperatures compatible with state-of-the-art refrigerators (500 mW at 4.2 K). This makes CMOS a potential alternative to solve one of the main problems identified before practical quantum computers are built, which is the interface between the qubits and the electronics necessary to control and read them out [\[3\],](#page-2-2) [\[4\].](#page-2-3)

The main issue with cryogenic CMOS is that the standard model BSIM3 incorporates behavioral information of devices in a temperature range from about 120 ◦C down to about −40 ◦C, leaving the cryogenic regime uncovered. This is because integrated circuits are typically used for industrial, commercial, and military applications, for which the operation in the cryogenic regime is not relevant [\[5\].](#page-2-4)

In recent years, there has been a growing interest in designing and validating CMOS circuits at increasingly lower temperatures, which in turn has made it necessary to develop device simulation models covering these temperatures [\[6\]. R](#page-2-5)esearch efforts have been devoted to the characterization of CMOS devices such as transistors

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Fig. 1. Block diagram of the experimental setup: a Gifford McMahon cryo-cooler is connected to the cold head, fabricated resistors are placed below inside the sample chamber, which is connected with the SMU Keysight B2912B that measures the *I*-*V* response.

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<span id="page-0-6"></span><span id="page-0-5"></span><span id="page-0-4"></span>Fig. 2. Examples of the temperature sweep in the entire temperature range for a Polysilicon P+ bulk with silicide  $(R2P +)$ .

<span id="page-0-9"></span><span id="page-0-8"></span><span id="page-0-7"></span>[\[7\], pa](#page-2-6)ssive components  $[8]$ , or complex memory structures  $[9]$ ,  $[10]$ in wider temperature ranges including the cryogenic regime.

This work presents the characterization down to the deep cryogenic regime at 4 K of 65 nm CMOS poly-silicon resistors with different bulk structures and sizes. The experimental measurements, carried out with a temperature step of 0.5 K, have allowed us to obtain the temperature coefficient  $\alpha(T)$  of the resistors in the whole temperature range.

# <span id="page-0-11"></span><span id="page-0-10"></span>II. EXPERIMENTAL SETUP AND CHARACTERIZATION

The device under test (DUT) is an integrated circuit composed of six CMOS resistors, each of them implemented as highly doped poly-silicon, of which two are N+ type and the other four are P+ type. To allow the measurements in a cryogenic chamber, the die with the resistors has been wire-bonded to a dedicated PCB using

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TABLE I MAIN CHARACTERISTICS OF THE RESISTORS CHARACTERIZED

<span id="page-1-0"></span>

<b>Name</b>	<b>Implementation characteristics</b>	Nominal Value at 300 K	WIL
$R1 N+$	Polysilicon N+ bulk with silicide, RF-type	$74.5\,\Omega$	$2 \mu m/10 \mu m$
$R1P+$	Polysilicon P+ bulk no silicide, RF-type	$3.50\,\mathrm{k}\Omega$	$2 \mu m/10 \mu m$
$R2N+$	Polysilicon N+ bulk no silicide, RF-type	$794\,\Omega$	$2 \mu m/10 \mu m$
$R2P+$	Polysilicon P+ bulk with silicide	$149\,\Omega$	$10 \mu m/100 \mu m$
$R3P+$	Polysilicon P+ bulk with silicide, RF-type	78 Ω	$2 \mu m/10 \mu m$
$R4P+$	Polysilicon P+ bulk no silicide, RF-type	$3.47\,\mathrm{k}\Omega$	$5 \mu m/25 \mu m$

<span id="page-1-1"></span>

<span id="page-1-3"></span>Fig. 3. Measured resistance–temperatures curves. Resistance follows the trend observed at room temperature, but when approaching the deep cryogenic regime it gets flatter and even reverses its dependency on temperature.

TABLE II MEASURED  $\alpha(T)$  PEAKING VALUE

<b>Name</b>	$T[K^{-1}]$	Peak $\alpha(T)$ [K <sup>-1</sup> ]
$R1 N+$	96.4	$3.20 \times 10^{-3}$
$R1P+$	98.6	$4.11 \times 10^{-4}$
$R2 N+$	66.4	$1.57 \times 10^{-4}$
$R2P+$	83.5	$4.5 \times 10^{-3}$
$R3P+$	88.8	$3.8 \times 10^{-3}$
$R4$ P+	91.9	$4.81 \times 10^{-4}$

 $25 \mu m$ , 1 mm aluminum wires, which add about  $1 \Omega$  to each resistor. The main properties of the resistors are presented in Table [I.](#page-1-0)

The experimental setup is shown in Fig. [1.](#page-0-0) The resistors have been measured using a Keysight B2912B source-measure unit (SMU) with a 4-wire configuration. The temperatures from 300 K to 4 K have been obtained by a Gifford McMahon cryo-cooler connected to a Leybod COOLPACK helium compressor unit and measured by a LakeShore Temperature Controller Model 335. The SMU has been programmed with Python, saving current and voltage readings using an NI measurement and automation explorer (MAX). The cryo-cooler is controlled via Labview, saving the temperature reading every 0.1 s.

The change of resistance with temperature is quantified by the temperature coefficient  $\alpha(T) = (1/R_T)(dR/dT)$ . To analyze the behavior of  $\alpha(T)$  of each resistor, their  $I-V$  curves have been obtained from room temperature (300 K) to 4 K. To ensure that temperature remains stable for every  $I-V$  curve, the measurement execution time has been reduced to 0.5 s, which, along with the

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Fig. 4. Temperature coefficient  $\alpha(T)$  down to 4 K. A peak takes place between 60 K and 100 K for all measures resistors.

4 K/min cooling rate of the cryo-cooler results in a temperature variation of 1 K with 3% error for each curve.

Fig. [2](#page-0-1) shows two colormaps of the temperature  $I-V$  sweeps of two of the measured resistors, representative of the behavior of a positive temperature coefficient (Fig. [2](#page-0-1) left) and a negative temperature coefficient (Fig. [2](#page-0-1) right) as the temperature is reduced to deep cryogenic.

## III. RESULTS AND DISCUSSION

Fig. [3](#page-1-1) shows the resistance values obtained for every resistor down to the deep cryogenic regime at 4 K. The curves show that the temperature coefficient, whether positive or negative, changes when reaching the deep cryogenic regime and for all resistors. A closer look at Fig. [3](#page-1-1) shows that when reaching the deep cryogenic regime of a few K, the rate of resistance change seems to stagnate or even reverse, which would translate in  $\alpha(T)$  having opposite sign.

<span id="page-1-5"></span><span id="page-1-4"></span>It is noteworthy that resistors R4 P+ and R1 P+, which are implemented with the same characteristics, show opposite behavior below 50 K. It has to be noted that in the deep cryogenic regime, the dispersion of electrons due to collisions with the atomic lattice of the conductive material is no longer dominated by the vibration of the lattice, since it has almost no thermal energy, but by the random collisions of the electrons, which activate the vibration of the lattice when they take place  $[11]$ ,  $[12]$ . R1 P+ has a smaller cross section than R4 P+ (widths of  $2 \mu m$  and  $5 \mu m$ , respectively), so a higher current density flows through R1 P+. This causes more random electron–lattice collisions and therefore the activation of more vibration modes in R1 P+ in comparison with R4 P+, which results in the observed earlier decrease in resistance in R4 P+.

To further analyze this, the dependency of  $\alpha(T)$  with temperature has been obtained from the resistance curves (Fig. [4\)](#page-1-2). It is noteworthy that the resistors implemented with silicide  $(R2 P+$ ,  $R3 P+$ , and R1 N+) have a relatively large positive temperature coefficient, whereas those implemented without silicide have either negative (R1 P+ and  $R4$  P+), or positive but relatively small  $(R2 N+)$  temperature coefficient, which agrees with the fact that the silicide layer adds up to behavior more resembling metal than a semiconductor.

Another aspect that can be seen in Fig. [4](#page-1-2) is that  $\alpha(T)$  whether positive or negative, reaches a maximum in its absolute value as the temperature is decreased, and from that point, its absolute value decreases to approach zero or even reverse sign for deep cryogenic temperatures. By computing the location of these peaks, we find that they happen for the temperatures indicated in Table [II.](#page-1-3) The peaks are located slightly below 100 K, which may be the combined result of changes in material proprieties (mechanical contractions/expansions) and of nonnegligible *e–e* scattering effects in highly doped silicon [\[13\],](#page-2-12) [\[14\].](#page-2-13)

### IV. CONCLUSION

<span id="page-2-15"></span><span id="page-2-14"></span>This work presents the experimental characterization down to 4 K of poly-silicon resistors in 65 nm CMOS. The resistors have been implemented with different bulk structures and in several sizes to achieve resistance values spanning from a few  $\Omega$  to some k $\Omega$ .

The experimental characterization has been carried out using a cryo-cooler unit to achieve temperatures down to 4 K with an accuracy of 0.1 K. The measurements have been automated to obtain the  $I-V$  curves of each resistor in a time span that results in a variation of only 0.5 K in temperature, thus allowing to interpret them as Temperature constant.

The analysis of the *I*-*V* curves obtained allows us to conclude that the trend of change of resistance with temperature is maintained as temperature decreases down to the cryogenic regime and also that only the resistors implemented for RF without a silicide layer show a negative thermal coefficient  $\alpha(T)$ . In addition, the observed different behavior of nonsilicide resistors has been analyzed based on the cryogenic properties of materials.

The thermal coefficient  $\alpha(T)$  has been obtained and represented against temperature. The values obtained for the thermal coefficient  $\alpha(T)$ , whether positive or negative, reach a maximum in their absolute value as the temperature is decreased. The location of these

maxima is close to the condensation temperature of nitrogen (77 K), which is a temperature regime in which materials are known to undergo changes in their thermal expansion.

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