# Estimation of Semiconductor Power Losses Through Automatic Thermal Modeling

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***Abstract*—Achieving the optimal design of power converters requires a deep understanding of the system's dissipation elements to meet the desired performance and safety standards. Once the power converter is designed, it is of key importance to estimate the actual power losses in the real setup, in order to redesign the power converter or monitor and control the semiconductor power losses. With that purpose, calorimetric techniques have outperformed electrical methods. However, they come with mechanical limitations and depend on analytical electrothermal equivalent circuits. These models are highly topology and technology dependent, often resulting in simplistic representations that underestimate thermal effects or complex sets of differential equations. To overcome these challenges, we present a novel post-design automatic method for characterizing semiconductor power losses through its converter thermal dynamics. Our method is rooted in an optimization program that identifies the optimal discrete-time linear model according to a set of power vs. temperature profiles. The proposed approach ensures accurate identification and integration of desired modeling requirements. The methodology is applicable to any power converter topology, and the derived linear model enables the use of standard control theory techniques for monitorization and control. Experiments with a real power converter validate the proposal's versatility and accuracy.**

***Index Terms*—Calorimetry, low voltage power semiconductors, thermal models, transient calorimetric measurement methods, semiconductor power losses, switching loss measurements, system identification.**

## I. Introduction

POWER converter design has received a significant boost with the advent of recent technologies such as wide-band gap (WBG) semiconductors or new substrate technologies. WBG semiconductors are beneficial due to their small die size, low conduction losses, and high-performance switching conditions [1], [2]. Similarly, new substrate technologies allow to improve the thermal dissipation of power devices [3], [4]. However, these advantages come with novel characterization challenges. In particular, current measurement for power losses calculation becomes unfeasible due to bandwidth limitations and its invasivity, which perturbs the real signal by the addition of parasitics from the measurement element [5], [6]. These issues have lead to the development of non-invasive thermal methods, mainly based on calorimeters [4]. However, calorimeter techniques rely on a physical based electrothermal equivalent circuit models, being necessary to thermally isolate part of the converter for its identification. These limitations do not allow for the estimation of power losses in applications where individual thermal isolation cannot be achieved and the differential equations of the thermal system become more complex. This is the case of modern industrial power converters, where the thermal coupling between components demands an accurate thermal characterization [7], [8] to ensure that the design of the power converter meets all the requirements in terms of performance [9], [10], robustness [11] and security [8], [12], [13]. The inherent complexity of the new technologies typically leads to the following design paths in a power converter: (1) use finite element methods or simplified electrothermal equivalents to evaluate a priori the power losses through simulations; (2) validate the design with the real device; (3) characterize the miss-match between the simulated power losses and the actual ones to redesign the power converter, monitor the power losses or control the power-temperature dynamics to achieve an optimal behavior. To address the second and third step, existing methods use calorimeter analytically simplified models as equivalent resistance and capacitors, underestimating more complex coupled thermal effects; or build analytical models formed by complex sets of differential equations that are not flexible to other topologies nor even tractable.

To cope with these issues, in this paper we propose a novel automatic thermal modeling technique to identify and estimate

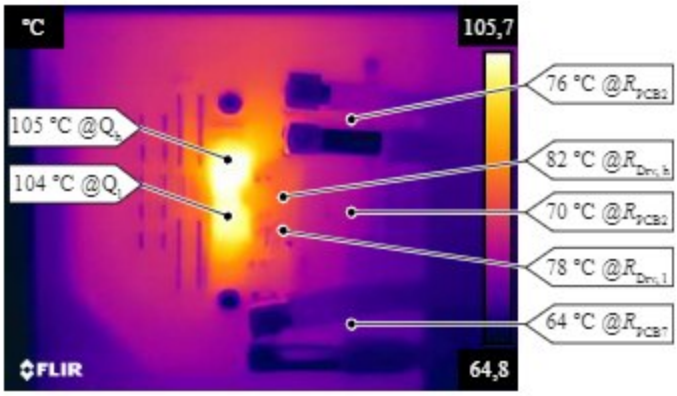


Fig. 1. Example of a frame from a thermal infrared camera. The camera is measuring the temperature of the power converter evaluated in Section V with semiconductors working in the linear region. Throughout the paper, we only use frames from thermal infrared cameras for illustrative purposes.

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the semiconductor total power losses that is accurate yet general, systematizing the thermal characterization of any power converter. Given a set of power-thermal trajectories recorded from any available measurement point, our solution obtains the linear model that best fits the data. In addition, due to the optimization formulation, we can add any desired restriction to the model, thus allowing designers to encode prior knowledge on the device. The methodology is based on the fact that the dynamics that relate power sources and their temperature is the same whether the system is excited in direct current (DC) or in alternating current (AC). Therefore, through DC calibration, our approach is able to characterize the semiconductor total power losses along any power converter during switching conditions from temperature measurements. Code and data is available on a GitHub repository[1].

*Related work.* Classical electrical characterization methods such as the double pulse test [14] do not satisfy the new high-speed switching conditions of devices, which require novel multiple pulse techniques [15] for an accurate characterization of power losses. These methods isolate the device from its desired used topology, therefore neglecting the overall parasitics and thermal coupling of the final target power converter [16], [17]. In this sense, thermal coupling, parasites, limited probe bandwidth and calibration problems lead to robust time-frequency characterization techniques [18].

A different line of research is to consider non-invasive methods based on indirect measurements. The most common approach is to take the difference between the measured input power and the output power [19]. However, this is strongly dependent on the precision of the power meter and the losses between the different components cannot be distinguished. Instead, calorimetric methods propose to estimate the power losses through thermal measurements [20]. Calorimetric methods have been applied not only to transistors [21], but also to inductors [22], capacitors [23], or microelectronic devices [24]. Despite the advantages in accuracy compared to other methods [25], typical calorimetric methods must enclose the device under test inside an insulated chamber, which is not always feasible due to size restrictions [26]. On the other hand, calorimetric methods need an equivalent analytical thermal-electric model of the power converter to relate the temperature and power losses [27], [28]. In the case that only the steady-state behavior is desired, the analytical models are based on equivalent thermal resistances [29]–[31]. If the dynamical model is desired, then thermal equivalent capacitors are included [28], [32], [33] [34]. Nevertheless, these models are highly dependent on the substrate [35] and the technology of the devices, as the coupling effects vary between the components, so these techniques are currently only suitable for simple circuits [4]. When the complexity of the circuit increases, the thermal model becomes more challenging as more power and coupling sources arise [36], [37].

Another alternative is to rely solely on a priori finite element analysis [38], [39]. These methods exploit complex computer tools [40] that implement physical electrothermal interactions [41] to model the effects of environmental temperature [42], control [43], or packaging conductivity analysis [38]. Despite its accuracy in single devices and potential model reduction [44], the complex parameterization hinders its flexible applicability in real power converters, where it is usually easier to obtain experimental temperature-power profiles that capture all thermal processes. Besides, specially in intricate topologies such as multi-level power converters, it is rather possible to forget to model coupling power-thermal factors, leading to a miss-match between a priori simulated power losses and the actual ones. Therefore, a post-design approach to characterize the actual power losses in the device from thermal measurements is necessary for optimal power converter design. As a target application case, with our a posteriori approach, the designer can model, verify and monitor the relationship between temperature and power losses from temperature measurements at key points of the converter.

In this context, we propose a novel non-invasive approach to characterize thermal dynamics and semiconductor power losses in power converters (Section II). Inspired by the recent emergence of automatic techniques for dynamics identification [45]–[47] [48], we propose an optimization-based identification method that obtains the best linear dynamical thermal-power model from experimental temperature-power profiles (Section III). In its simplest form, the solution can be recast as a least-squares problem, leading to accurate and fast identification of the linear dynamics. Nevertheless, the formulation allows one to include any desirable constraint and prior knowledge, facilitating the identification. Besides, the formulation avoids, by design, typical ill-posedness from resistance-capacitor identification. Experiments of the operating power converter (Section V) show the accurate performance of our proposal, including a comparison with other state-of-the-art thermal physical thermal models. Besides, we propose a novel method for studying the coupling between components on a power converter that leverages sensitivity analysis. Overall, we conclude that our propose approach is general and flexible to be applied to any power converter topology (Section VI).

## II. Problem Formulation

The device under study is a general power converter formed by dissipate power sources, like transistors, inductors, or printed circuit board (PCB) tracks. The topology of the power converter is not assumed a priori, so it can be a buck converter, a full-bridge resonant converter, etc. The power dissipation of the converter is characterized by temperature and power measurements, which can be acquired by any available means. For instance, in a transistor, the temperature might be measured from its top capsule surface, using a thermocouple or an infrared camera as in Fig. 1. On the other hand, the power of the devices is measured in DC, e.g., using low continuous current methods to decouple the effects of the tracks in the power measurements. Section IV details how to measure the power in the devices.

Formally, the power converter is characterized by a set of $n$ power measurement points $\mathcal{P} := \{1, \dots, i, \dots, n\}$ and a set of $m$ temperature measurement points $\mathcal{T} := \{1, \dots, j, \dots, m\}$.

[1]https://github.com/jm-sanz/Automatic-Thermal-Modeling

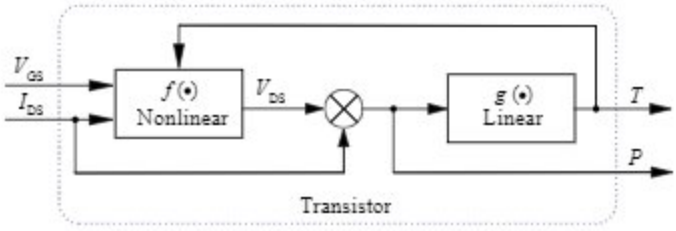


Fig. 2. Block diagram of the dynamics of a transistor. The dynamics can be decoupled in two terms, (i) a non-linear term that models the relationship between current, voltage and power, and (ii) a linear term that models the relationship between power and temperature. In this work we are interested in the latter.

We denote by $P^i \in \mathcal{P}$ and $T^j \in \mathcal{T}$ the power at measurement point $i$ and the temperature at measurement point $j$ respectively.

Given all these measurable quantities, we aim to identify the relationship between power and temperature in the power device as a linear discrete-time dynamical system. To do so, we define the state and input of the thermal dynamics of the power converter as

$$\begin{aligned}\mathbf{x} &= [P^1, \dots, P^i, \dots, P^n]^\top, \\ \mathbf{u} &= [T^1, \dots, T^j, \dots, T^m]^\top,\end{aligned} \tag{1}$$

where $\top$ denotes the transpose operator. The ordering of the quantities in $\mathbf{x}$ and $\mathbf{u}$ is arbitrary and does not affect the automatic modeling process. Then, the linear discrete-time power-temperature dynamics is defined as

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}\mathbf{u}(k). \tag{2}$$

In Eq. (2), $\mathbf{A}$ and $\mathbf{B}$ are unknown matrices, whereas $k \in \mathbb{N}$ denotes the discrete instants when the system is sampled, with $\Delta t > 0$ the sample time. This model can be considered as the Generalized Average Model [49], [50] of the relationship between the power and temperature in the converter elements in discrete time. The linear assumption is also supported by the fact that the relationship between temperature and power in a semiconductor device is dominated by linear dynamics, whereas the relationship between current, voltage and power is non-linear, as it is observed in Fig. 2. In this work we are interested in the power-temperature dynamics. Note that there is no assumption regarding the underlying structure of both matrices, in contrast to classical power losses identification techniques where the elements of these matrices are parameterized by equivalent resistance and capacitor parameters.

Now, assume that the quantities in $\mathbf{x}$ and $\mathbf{u}$ can be measured and recorded during $K > 0$ instants of time. We can build a set of data $\mathcal{D} = \{\mathbf{x}(k), \mathbf{u}(k)\}_{k=1}^{K}$. Given a collection of measurements $\mathcal{D}$, the goal of this paper is to identify the dynamics in (2) characterized by $\mathbf{A}$ and $\mathbf{B}$, such that the model is as accurate as possible in estimating the power losses and it fulfils any a priori constraint of the power converter. The a priori constraints can be, e.g., the sign of an element of matrix $\mathbf{B}$ or a rank condition over matrix $\mathbf{A}$ to ensure a well-conditioned identification. Formally, the problem to solve is the following:

$$\min_{\hat{\mathbf{A}},\hat{\mathbf{B}}} \ \mathcal{L}(\mathcal{D}) \tag{3a}$$

$$\text{s.t. } \mathbf{x}(k+1) = \hat{\mathbf{A}}\mathbf{x}(k) + \hat{\mathbf{B}}\mathbf{u}(k), \tag{3b}$$

$$g_{\mathbf{A}}(\hat{\mathbf{A}}) \leq 0, \ h_{\mathbf{A}}(\hat{\mathbf{A}}) = 0, \tag{3c}$$

$$g_{\mathbf{B}}(\hat{\mathbf{B}}) \leq 0, \ h_{\mathbf{B}}(\hat{\mathbf{B}}) = 0. \tag{3d}$$

In problem (3), $\mathcal{L}(\mathcal{D})$ is an objective function that measures the quality of the estimation accuracy of the identified model given by $\hat{\mathbf{A}}$ and $\hat{\mathbf{B}}$. Meanwhile, $g_{\mathbf{A}}(\hat{\mathbf{A}})$, $h_{\mathbf{A}}(\hat{\mathbf{A}})$, $g_{\mathbf{B}}(\hat{\mathbf{B}})$ and $h_{\mathbf{B}}(\hat{\mathbf{B}})$ are functions that model any constraint on $\hat{\mathbf{A}}$ and $\hat{\mathbf{B}}$. The next section proposes a general approach to solve problem (3), so that it automatically provides the best estimator to estimate the power losses of a power converter.

## III. Optimization-based Identification

To find the solution for problem (3) we need, first, to generate the dataset $\mathcal{D}$. Ideally, a temperature input $\mathbf{u}(k)$ would be applied to the power converter, measuring the evolution of the power $\mathbf{x}(k)$. However, in practice, this not practical because the temperature in the devices is a consequence of the power losses during the operation of the power converter. Thus, in real power converters, the power losses are generated from an electrical excitation and the temperature is allowed to evolve freely. More information is provided in Section IV. For now, the consequence is that problem (3) cannot directly be solved nor $\mathbf{A}$ and $\mathbf{B}$ identified from $\mathcal{D}$ and through $\hat{\mathbf{A}}$ and $\hat{\mathbf{B}}$, so an alternative method must be developed to estimate the power losses given the temperature of the power converter.

To do so, the first step is to identify the complementary dynamic temperature-power model. This is described by the following discrete-time linear dynamics:

$$\mathbf{u}(k+1) = \bar{\mathbf{A}}\mathbf{u}(k) + \bar{\mathbf{B}}\mathbf{x}(k). \tag{4}$$

This model is directly related to the collection of the dataset $\mathcal{D}$, where the power converter is excited with electrical signals such that power losses appear in the different components of the converter and the temperature evolves accordingly.

The next step is to identify $\bar{\mathbf{A}}$ and $\bar{\mathbf{B}}$ such that they can be used later to estimate power losses from temperature measurements, and the requirements in terms of accuracy and restrictions in problem (3) are accomplished. Let reformulate Eq. (4) as:

$$\mathbf{u}(k+1) = \begin{pmatrix}\bar{\mathbf{A}} & \bar{\mathbf{B}}\end{pmatrix} \begin{pmatrix}\mathbf{u}(k) \\ \mathbf{x}(k)\end{pmatrix} = \mathbf{W}\mathbf{z}(k). \tag{5}$$

The idea of this reformulation is to allow to frame the identification problem as a least-squares minimization. For that reason, we define $\hat{\mathbf{W}} = \begin{pmatrix}\hat{\bar{\mathbf{A}}} & \hat{\bar{\mathbf{B}}}\end{pmatrix}$ as the estimated temperature-power model, and we define the error (also called residual) between predicted and actual temperature as

$$\mathbf{e}(k) = \mathbf{u}(k) - \hat{\mathbf{W}}\mathbf{z}(k-1) \tag{6}$$

Then, to identify the most accurate model in terms of Mean Square Error (MSE), we have to minimize the sum of the norm of all the errors, leading to

$$\left(\hat{\mathbf{A}}^* \quad \hat{\mathbf{B}}^*\right) = \arg\min_{\hat{\mathbf{A}},\hat{\mathbf{B}}} \sum_{k=2}^{K} ||\mathbf{e}(k)||_2^2, \tag{7}$$

where $||\bullet||_2$ is the L2-norm. Under the assumption that no further requirements are needed, the solution of (7) is given by

$$\left(\hat{\mathbf{A}}^* \quad \hat{\mathbf{B}}^*\right) = (\mathbf{Z}^\top\mathbf{Z})^{-1}\mathbf{Z}^\top\mathbf{U} = \mathbf{Z}^\dagger\mathbf{U}. \tag{8}$$

Matrix $\mathbf{Z} = [\mathbf{z}(1), \mathbf{z}(2), \ldots, \mathbf{z}(K-1)]$ and matrix $\mathbf{U} = [\mathbf{u}(2), \mathbf{u}(3), \ldots, \mathbf{u}(K)]$ stack the $\mathbf{z}(k)$ and $\mathbf{u}(k)$ elements of the dataset $\mathcal{D}$ to form the input and output data matrices respectively. Meanwhile, $\mathbf{Z}^\dagger = (\mathbf{Z}^\top\mathbf{Z})^{-1}\mathbf{Z}^\top$ is the Moore-Penrose inverse of $\mathbf{Z}$.

Given the optimal $\hat{\mathbf{A}}^*, \hat{\mathbf{B}}^*$ in the MSE sense, the power losses can be estimated from temperature measurements using the identified dynamics from Eq. (4). The temperature-power dynamics leads to:

$$\begin{aligned} &\mathbf{x}(k) = ((\hat{\mathbf{B}}^*)^\top\hat{\mathbf{B}}^*)^{-1}(\hat{\mathbf{B}}^*)^\top(\mathbf{u}(k+1) - \hat{\mathbf{A}}^*\mathbf{u}(k)) \Rightarrow \\ &\mathbf{x}(k-1) = ((\hat{\mathbf{B}}^*)^\top\hat{\mathbf{B}}^*)^{-1}(\hat{\mathbf{B}}^*)^\top(\mathbf{u}(k) - \hat{\mathbf{A}}^*\mathbf{u}(k-1)) \end{aligned} \tag{9}$$

Equation (9) defines an estimator for the power losses given the temperature at the power converter.

At this point, a few considerations are in order. First, according to Eq. (9), the estimator has a delay of one discrete step. This is not a problem because matrices $((\hat{\mathbf{B}}^*)^\top\hat{\mathbf{B}}^*)^{-1}(\hat{\mathbf{B}}^*)^\top$ and $\hat{\mathbf{A}}^*$ can be pre-computed from the calibration data in $\mathcal{D}$, and a sufficiently small $\Delta t$ can be chosen to fit the application requirements. Second, Eqs. (8) and (9) include the Moore-Penrose inverse of the matrices $\mathbf{Z}$ and $\hat{\mathbf{B}}^*$. The Moore-Penrose inverse of any real $n \times m$ matrix $\mathbf{K}$ exists if and only if the rank of $\mathbf{K}$ is maximum, that is, if $\mathsf{rank}(\mathbf{K}) = \min(n, m)$. For Eq. (8), this means that there are as many linearly independent measurements $\mathbf{z}(k)$ as the number of temperature and power test points, which is easy to accomplish since, typically, $K >> (n+m)$. Another option is to use a regularizer that avoids ill-conditioned identification, so $(\mathbf{Z}^\top\mathbf{Z})^{-1}$ in Eq. (8) is replaced by $(\mathbf{Z}^\top\mathbf{Z} + \varepsilon\mathbf{I})^{-1}$, where $\varepsilon > 0$ is a small constant designed by the practitioner and $\mathbf{I}$ is the identity matrix. This regularizer penalizes large values of $\hat{\mathbf{A}}^*, \hat{\mathbf{B}}^*$ and, therefore, provides robustness against the noise or possible outliers in the measurements used for the identification. On the other hand, to ensure that $\hat{\mathbf{B}}^*$ in Eq. (8) has full rank, a constraint can be used, leading to the following reformulation of the optimization problem:

$$\left(\hat{\mathbf{A}}^* \quad \hat{\mathbf{B}}^*\right) = \arg\min_{\hat{\mathbf{A}},\hat{\mathbf{B}}} \sum_{k=2}^{K} ||\mathbf{e}(k)||_2^2 \tag{10a}$$

$$\text{s.t. } \mathsf{rank}(\hat{\mathbf{B}}) = n + m, \tag{10b}$$

Finally, we can include additional constraints to (10) from, e.g., a priori knowledge on the properties of the power converter. For instance, the element $(i, j)$ of $\hat{\mathbf{B}}^*$ is necessarily positive if we know that the power losses of the measurement point $i$ of vector $\mathbf{x}$ always increase the temperature at the measurement point $j$ of vector $\mathbf{u}$. Thus, with the additional constraints, problem (10) turns to be

$$\left(\hat{\mathbf{A}}^* \quad \hat{\mathbf{B}}^*\right) = \arg\min_{\hat{\mathbf{A}},\hat{\mathbf{B}}} \sum_{k=2}^{K} ||\mathbf{e}(k)||_2^2 \tag{11a}$$

$$\text{s.t. } \mathsf{rank}(\hat{\mathbf{B}}) = n + m, \tag{11b}$$

$$g_{\bar{\mathbf{A}}}(\hat{\mathbf{A}}) \leq 0,\ h_{\bar{\mathbf{A}}}(\hat{\mathbf{A}}) = 0, \tag{11c}$$

$$g_{\mathbf{B}}(\hat{\mathbf{B}}) \leq 0,\ h_{\mathbf{B}}(\hat{\mathbf{B}}) = 0. \tag{11d}$$

The optimization problem in (11) is non-convex due to constraint (11b). Nevertheless, there exist many solvers and optimization methods that find the local/global minima of (11) with guarantees of convergence to a local minima, including those based on convex relaxations [51], [52] or proximal-gradient-based methods [53].

Overall, our proposed approach solves the problem of estimating the total power losses of a power converter and its power semiconductors from calibration measurements by the automatic identification of the linear temperature-power discrete-time dynamics. Notice the similarity between the problem (3) and (11). Thanks to our proposed approach, the identification of $\mathbf{A}$ and $\mathbf{B}$ is bypassed, respecting the conditions of the calibration and collection of data in a power converter, where it is only possible to electrically excite the power losses and record the evolution of the temperature and not vice versa.

## IV. Characterization Methodology

After providing the theoretical foundation of the paper, in this section we illustrate the experimental procedure to characterize the thermal properties of a power converter. We recall that our goal is, given an already designed power converter, identify its actual power-thermal dynamics, with the main target on the semiconductor power losses estimation.

First, for a consistent characterization of a linear system, all the power sources are excited independently. In addition, all the components must remain connected and the different power sources cannot be removed for an independent characterization, because any change in the physical connection of the devices can modify the thermal behavior. Second, the complexity of the coupling thermal dynamics depends on the physical design of the converter. Typically, high-frequency low-power converters tend to have a more compact design, leading to greater couplings between components, whereas the design of the modules in high-power converters tends to be thermally isolated. In this sense, not all power sources have the same level of interest. Therefore, for every power converter, a study of the influence of the surrounding components on the semiconductors must be performed for a higher accuracy of the power estimation. As most power converters have transistors, PCB tracks, drivers and inductors, these are the target power sources in this work. To measure temperature with a low level of noise, a general rule is to choose representative points in terms of power loss sensitivity. For instance, the most representative point in a semiconductor is the junction; however, since the junction is usually inaccessible, a closed enough location can be used. Another example is the inductor:

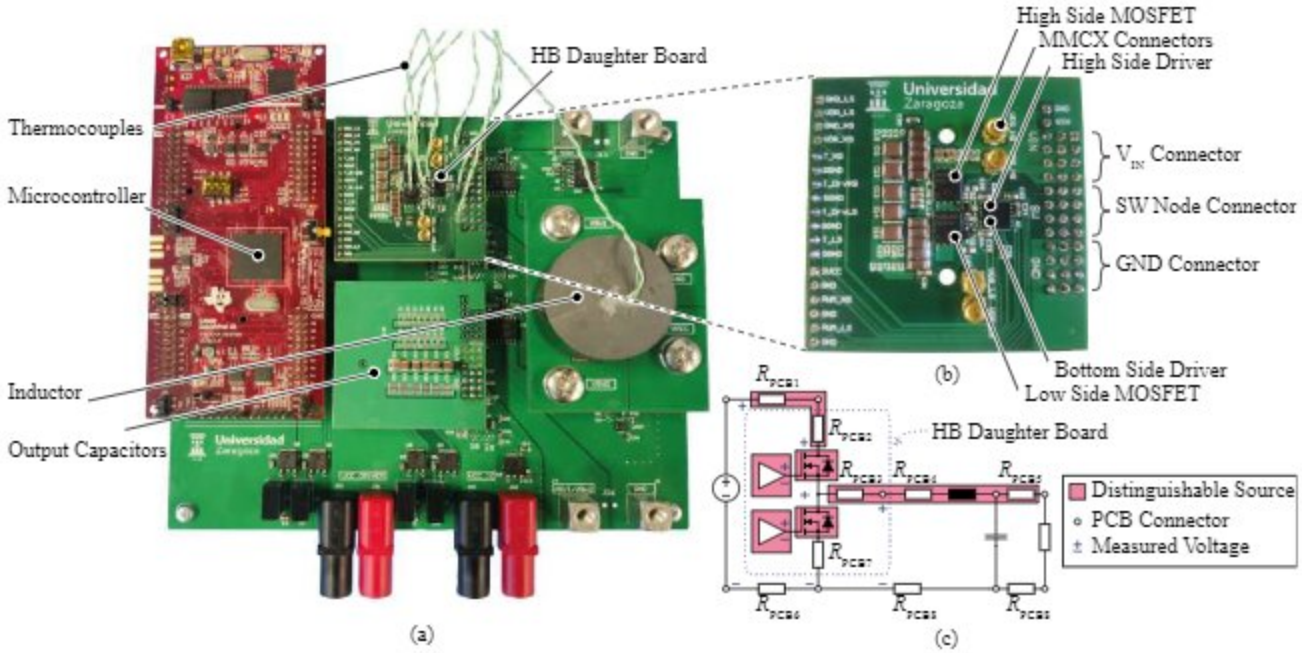


Fig. 3. Hardware design of the synchronous buck converter under study. (a) Illustration of the entire power converter, along with its main parts. (b) Half-bridge board, along with its main components. (c) Schematic circuit of the synchronous buck converter, highlighting the main thermal sources and connections.

depending on its geometry, different measurement points can be placed on the copper or the core.

We study a synchronous buck power converter to illustrate the approach proposed in the paper. The setup is shown in Fig. 3. To generate $\mathcal{D}$, thermocouples capture the thermal measurements, with a sampling rate of 1 s. In this section, we use thermal frames from an infrared camera for visually understanding the characterization process, they are not used as inputs of the model. It is noteworthy the importance of a proper attachment of the thermocouples to ensure the repeatability of the tests. In addition, the thermocouples may suffer from pickup noise in switching conditions. This depends on the specific power converter design; if necessary, screened extension cables, shielded thermocouples or other thermal measurements methods as infrared thermal cameras or optical fiber can be used.

On the other hand, the microcontroller's ADCs capture the electrical measurements with a sampling rate of 100 ms. Nonetheless, any other measurement means is valid. The DUTs are 100 V@ 3 mΩ Infineon OptiMOS™ 6 silicon transistors [54]. Fig. 3c presents the circuit diagram of the topology along with its PCB tracks and the available voltage measurement points. The different heat sources are highlighted in red. Ground PCB tracks are overlooked because they are designed as large copper planes, so they can be considered as an equipotential surface.

After describing the general practical background and the power converter under study, in the following subsections we detail how to calibrate each component.

### A. Transistors Calibration

In all power converters there exists a high thermal coupling between the transistors and the PCB tracks, which is crucial to characterized for an accurate thermal modeling. Typically, to calibrate the transistors, high currents are needed to generate large losses on the semiconductors since this calibration stage is done in DC. Instead, to isolate switching and DC losses from each other, the transistor gate voltage shall not be fully activated, forcing its operation in the saturation region. In this region, a low DC current is enough for bringing the transistor to its thermal limit without heating up the tracks. This method is universal as it is valid for any transistor technology [55]. On the other hand, the gate voltage shall be below the temperature compensation point to ensure that the temperature coefficient of the current, $\alpha = \frac{dI_D}{dT}$, is always positive. To avoid thermal instability, the transistor current must be limited.

The circuit diagram to calibrate the devices is shown in Fig. 4a, where the input power supply is used in current mode (1 A for the target converter). The probe test points (MMCX) in Fig. 3b are used as connectors for an external voltage supply. Due to transconductance effects, it is desirable to use a linear power supply such that ripples in the gate voltage do not provoke ripples in the power. On the other hand, a resistor $R_{\text{ext}}$ is placed externally to the PCB, in series between the gate and the power supply, to mitigate potential oscillations between the power supply and the parasitic capacitances of the MOSFET. The existing surface-mount gate resistors are removed to avoid undesirable current flows between driver and transistors. Furthermore, the converter load is removed to allow free DC current flow when its impedance is similar to $Q_l$ in the saturation region. This external supply injects gate voltages slightly above the threshold voltage of the device. For illustration purposes, Fig. 4a. shows thermal images of the low side transistor, $Q_l$ and the high side transistor, $Q_h$ when they are electrically excited independently. Tracks are heated up as a consequence of the transistors' thermal load and not because

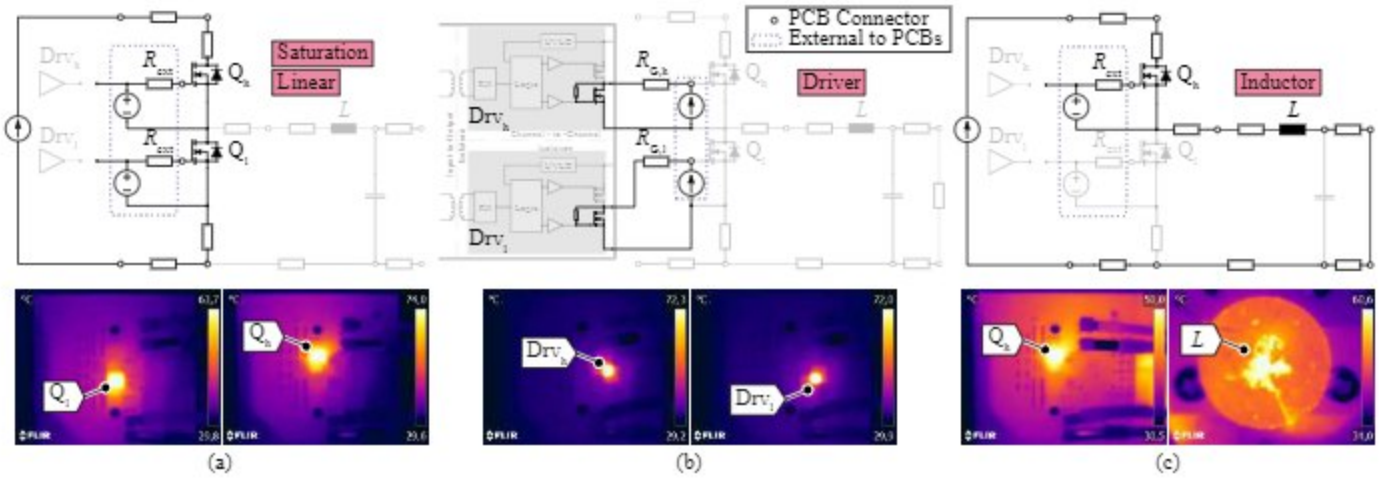


Fig. 4. Calibration circuit diagrams and associated calorimetric measurements. (a) Transistors (saturation configuration) and power loop tracks (linear configuration). (b) Driver (driver configuration). (c) Inductor and output tracks (inductor configuration). The infrared camera frames illustrate the main sources of thermal dissipation for each calibration circuit.

of their self-heating effect.

### *B. Power Loop Tracks Calibration*

Once the transistors are calibrated, it is possible to force large currents through them (up to 25 A for the target converter) to excite PCB power loop tracks, characterizing the thermal properties of the PCB by using the same setup of Fig. 4a, but with the gate voltage recommended by the manufacturer for switching in the linear region of the MOSFET (10 V). Since the calibration data already includes the individual excitation of the transistors, the temperature increase can only be due to the power loop tracks. These are $R_{\mathrm{PCB1}}$ and $R_{\mathrm{PCB2}}$, which have been grouped into a single power source ($R_{\mathrm{PCB1+PCB2}}$) as shown in Fig. 3c. For simplicity and without loss of generality, power losses that depend on the frequency, such as the skin effect, are overlooked, but could be included as a perturbation in the system dynamics. For illustration, Fig. 1 shows a thermal image where, compared to the previous transistor calibration, both transistors are heated simultaneously along with the power loop tracks.

### *C. Driver Calibration*

Simultaneous high switching speed and large semiconductors' gate current produce a self-heating effect on the driver output stage. To minimize the gate loop inductance, the distance between the drivers and the semiconductors is usually reduced as much as possible. Therefore, they are considered an additional power source that needs to be calibrated.

The mounted driver is the Infineon dual-channel isolated MOSFET gate-driver 2EDF7275K [56]. It is optimized for the driving of OptiMOS™ devices, being able to provide a 4 A/8 A source/sink from its output stage. This is possible thanks to two rail-to-rail output stages, built from complementary pairs of PMOS and NMOS transistors for the high side ($\mathrm{Drv_h}$) and low side ($\mathrm{Drv_l}$) inside the same package. When both $\mathrm{Q_l}$ and $\mathrm{Q_h}$ switches operate in the same regime, the shape of their current evolution is similar, and therefore it is hard to disambiguate their thermal behavior. In contrast, when they are in different operating conditions, the devices present differences in their thermal curves. Thus, it is recommended to consider them as independent power sources for a greater accuracy of the calibration stage.

A power supply can be used to limit the DC current and sweep it through each of the outputs pairs (up to 300 mA for the target converter). The output NMOS transistor is self-polarized due to the drain-source resistor and has the effect of thermal load, so there is no need of fixing the gate voltage as in the transistor calibration stage. This way, it is possible to generate the corresponding dataset of power and temperature for both output ports. To do so, we re-solder the $R_{\mathrm{G,h}}$ and $R_{\mathrm{G,l}}$ gate resistors with a value of 0 Ω and use the MMCX connector of $V_{\mathrm{GS}}$ for the current source connection, as shown in Fig. 4b. Current only flows in the direction of the driver due to the high input impedance of DUT MOSFETs. Fig. 4b also depicts the associated thermal images of this process. On the left, only the high side ($\mathrm{Drv_h}$) is excited, whereas on the right only the low side ($\mathrm{Drv_l}$) is excited.

### *D. Inductor and Output Tracks Calibration*

The ideal converter modeling entails the individual calibration of every power source. However, due to the importance of minimizing changes to the mechanical system, it is not possible to attach wires to the inductor [57] connectors, as this could introduce additional power sources or act as a heat sink. In addition, since our main goal is to estimate the semiconductor power losses, and the current that flows through the inductor also flows through its surrounding PCB tracks, then $R_{\mathrm{PCB3}}$, $R_{\mathrm{PCB4}}$ and $R_{\mathrm{PCB5}}$ are grouped into an individual power source ($R_{\mathrm{PCB3+PCB4+}L\mathrm{+PCB5}}$) as highlighted in Fig. 3c. For its calibration, we use the configuration illustrated in Fig. 4c, where a power supply is used in current mode and forced to circulate through the high side MOSFET (up to 15 A because of inductor thermal limitations). The effects of power loop tracks $R_{\mathrm{PCB1}}$, $R_{\mathrm{PCB2}}$, and $\mathrm{Q_h}$ have already been independently

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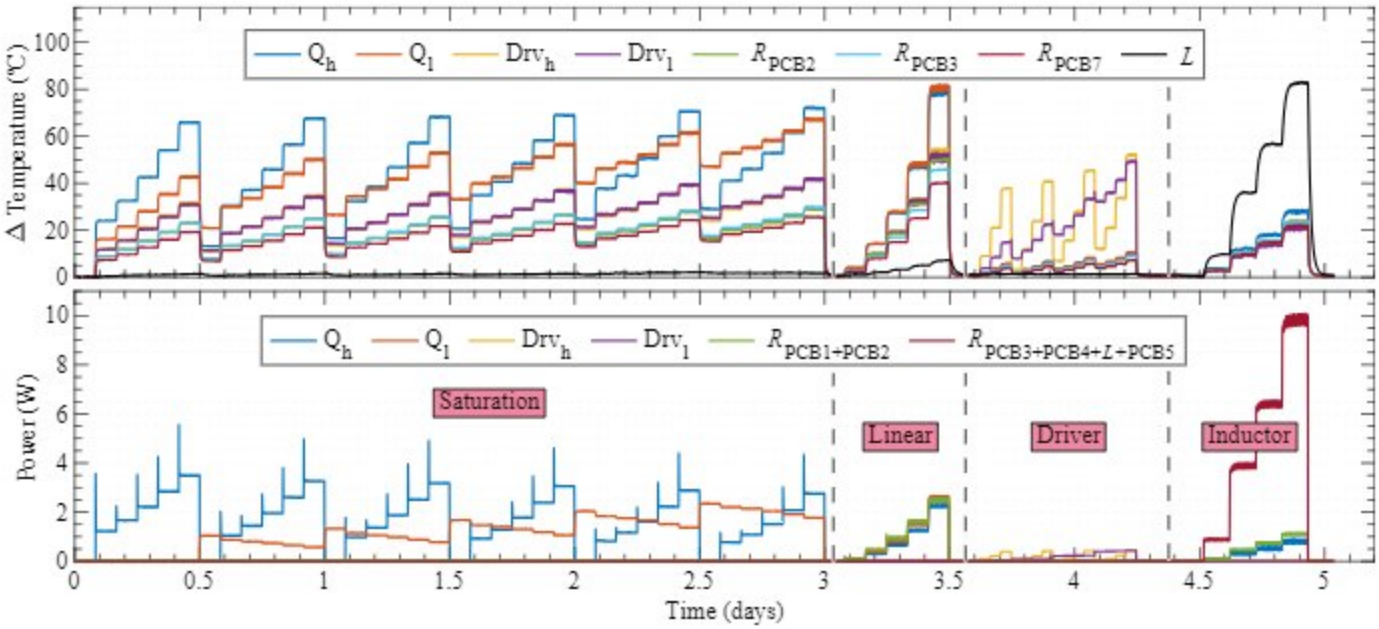


Fig. 5. Collected dataset to evaluate the synchronous buck converter under study. The four calibration steps are separated by dashed lines.

characterized in previous tests, so additional heat on the system is due to this new power source. Thermal images of Fig. 4c show the heating on the high side device ($Q_h$) while the resistance $R_{PCB4}$ is also heated up. The image on the right shows the heated inductor.

## V. Automatic Thermal Modeling Results

In this section, we evaluate the automatic approach proposed in Section III with the synchronous buck converter described in Section IV. Fig. 5 represents the collected data that builds the dataset $\mathcal{D}$. The temperature measurements are oversampled ($\times 10$) to match the available power data and represented as relative quantities with respect to measured ambient temperature. To generate the dataset, we sequentially conduct all the calibration steps detailed in Section IV, as depicted in Fig. 5. To ensure well-posedness in the generation of the dataset, we leave enough time between calibration steps to ensure that the boundary conditions are respected and steady-state is reached. In this sense, for each power converter configuration, we wait until the steady-state is also reached ($\approx$ 2h for the power converter under study).

Regarding the voltage measurements, in constant current conditions, we remark that its dynamics behavior changes along with the sign of $\alpha$ (value of $V_{GS}$) [55], which can be seen at the beginning of the transient interval in Fig. 5. Thus, in the saturation regime, the temperature in $Q_h$ increases while the power decreases. On the other hand, in the linear regime, the temperature in $Q_h$ increases when the power increases. This nonlinear behavior in the electrical data does not affect the linear relationship between temperature and power as illustrated in Fig. 2. The experiments also prove the importance of calibrating the PCB tracks: in the linear regime, the power losses are similar to those in the transistors, despite reaching different temperature values.

To evaluate the proposed approach, we split the dataset $\mathcal{D}$ in two different sets. The first set, $\mathcal{D}_1$, gathers most of $\mathcal{D}$ and is used for identifying the temperature-power dynamics of the power converter. The second dataset, $\mathcal{D}_2$, composed by the rest of $\mathcal{D}$, is used for evaluation. In particular, this split is conducted for each calibration step independently, so we ensure that both the identification and evaluation stages have data from all the calibration steps.

### A. Automatic identification of power-temperature dynamics

The results of the identification are shown in Fig. 6. To assess the model, we initialize the state and input vectors of the identified dynamics with the initial configuration of the test dataset $\mathcal{D}_2$. After that, we conduct two types of open-loop simulations. The first one assesses the accuracy of the identified $\hat{\mathbf{A}}$ and $\hat{\mathbf{B}}$. Using as input the sequence of power measurements $\mathbf{x} \in \mathcal{D}_2$, we leave the temperature $\hat{\mathbf{u}}$ evolve freely, comparing the obtained estimates with the associated real temperature measurements $\mathbf{u} \in \mathcal{D}_2$. However, the main goal of this work is to estimate power losses from temperature measurements. Therefore, the second type of open-loop simulations assesses the estimator proposed in Eq. (9). Using as input the sequence of temperature measurements $\mathbf{u} \in \mathcal{D}_2$, we leave the power losses $\hat{\mathbf{x}}$ evolve freely, comparing the obtained estimates with the associated real power losses $\mathbf{x} \in \mathcal{D}_2$. In Fig. 6, the real measurements are depicted in dashed lines while the estimates are represented with bold lines with less color opacity. Besides, for quantitative analysis, we compute the mean, the standard deviation and the normalized mean of the Root Mean Square Error (RMSE) across power losses as

$$\mu_{\text{RMSE}} = \frac{\sum_{i=1}^{n} ||\hat{\mathbf{x}}_i - \mathbf{x}_i||_2}{n}, \sigma_{\text{RMSE}} = \sqrt{\frac{\sum_{i=1}^{n} (\hat{\mathbf{x}}_i - \mu_{\text{RMSE}})}{\mu_{\text{RMSE}}}}$$

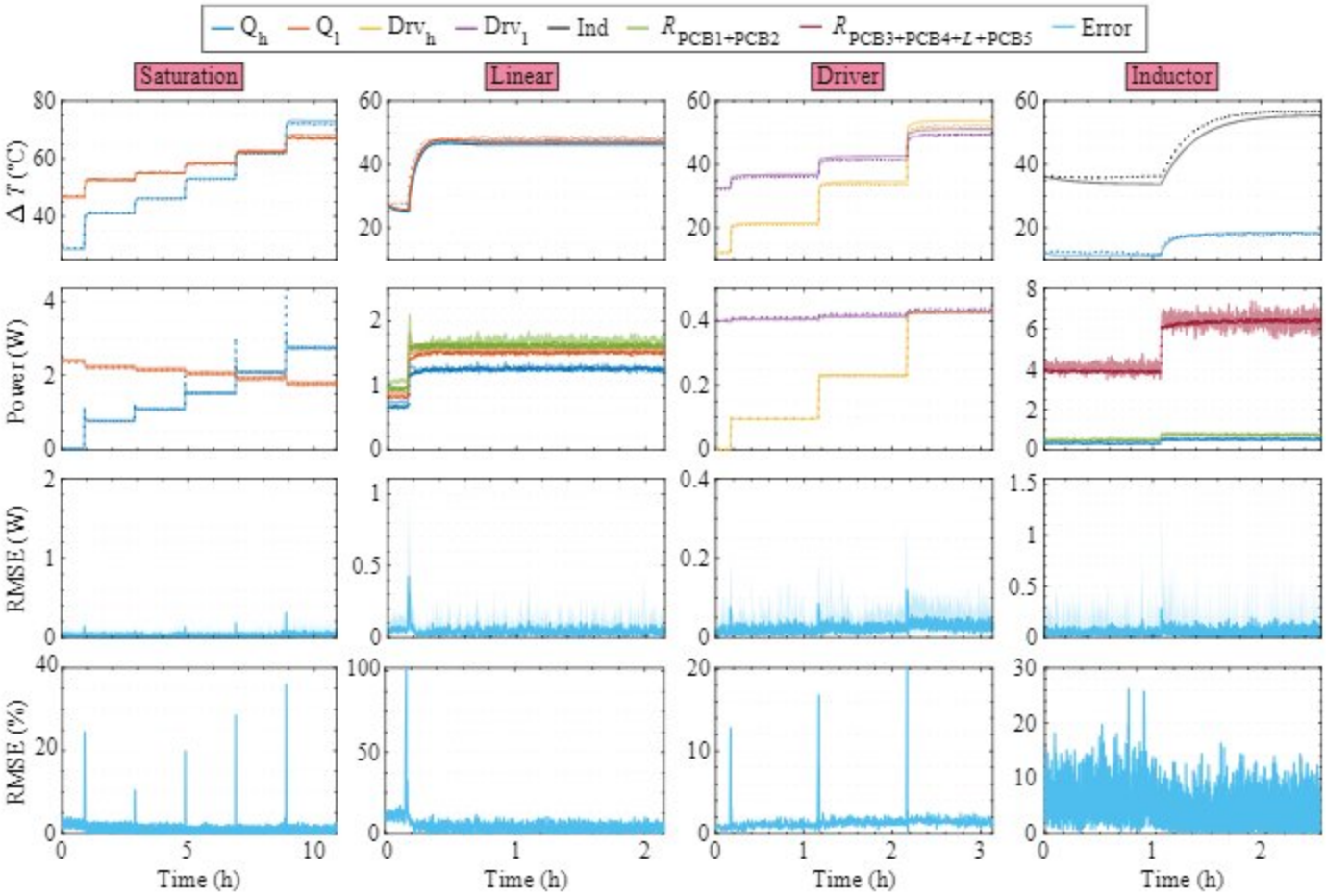


Fig. 6. Quantitative results. The figure shows, for the four different configurations, the following dynamic information, where dashed lines represent the measurement and bold lines the estimations: (first row) temperature estimation from the identified $\mathbf{A}$ and $\mathbf{B}$, obtained from the solution of (10); (second row) power losses estimation results from the estimator developed in Eq. (9), where each column depicts the relevant heating elements; (third row) evolution of the mean $\mu_{\text{RMSE}}$ and confidence interval between real and estimated power with time; (fourth row) evolution of the normalized mean $\tilde{\mu}_{\text{RMSE}}$ between real and estimated power with time. It is seen that, for all the regimes, both temperature and the power losses are accurately estimated.

and

$$\tilde{\mu}_{\text{RMSE}}(k) = \frac{\mu_{\text{RMSE}}}{||\mathbf{x}(k)||_2}.$$

The standard deviation is used to depict the 95 % confidence interval of the estimation ($\mu_{\text{RMSE}} + 2\sigma_{\text{RMSE}}$).

Success in power and temperature estimation can be verified from the dynamic results of Fig. 6 where, for the four configurations, low estimation error is achieved. For the case of temperature estimation, the model is able to accurately follow the real system dynamics for all situations. Slightly larger errors are found in the inductor configuration. This could be due to the reduced number of temperature measurement points in this area. On the other hand, to reduce the impact of noise measurement in the data, a moving average of 5 s was used. This filtering enhanced the estimation, but it can increase the instantaneous error in the transient due to the time delay inherent to the noise filtering. This effect seems to be more predominant in the semiconductors. To compensate these errors, it is enough to wait the delay time. Higher order filters can be applied to the measurements if larger noise is found.

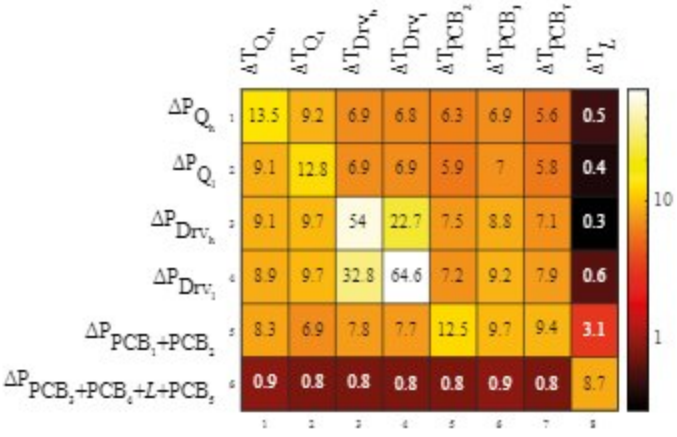


Fig. 7. Representation of the steady-state sensitivity matrix $\mathbf{S}$ of the identified model for the power converter.

Importantly, thanks to identifying the optimal linear discrete-time dynamic system in terms of the acquired data, systems theory tools can be used to analyze the behavior of the real power converter. Fig. 7 represents the sensitivity matrix

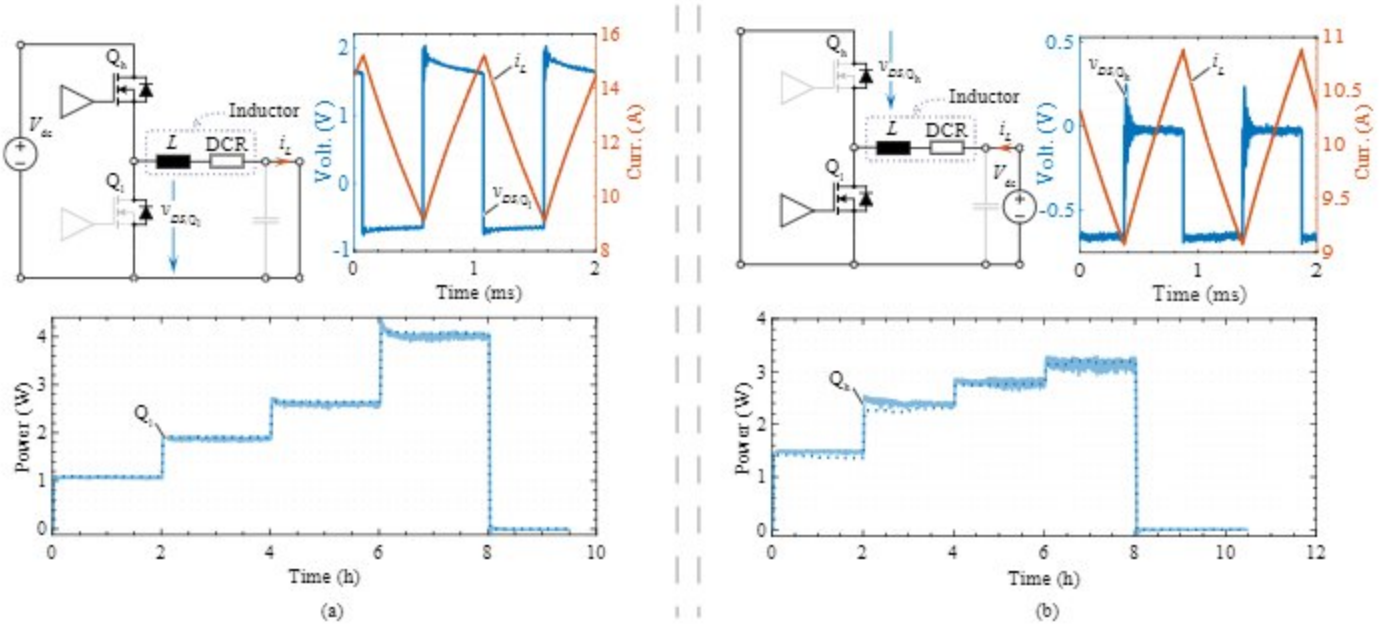


Fig. 8. Circuit diagram of each of the configurations needed to validate the power semiconductor losses in the (a) low side and (b) high side semiconductors. The figure displays power estimations and measured values for two different test operating points, along with an oscilloscope capture.

in steady-state given by

$$\mathbf{S} = (\mathbf{I} - \hat{\mathbf{A}}^*)^{-1}\hat{\mathbf{B}}^*$$

after identification. The element $(i, j)$ of matrix $\mathbf{S}$ expresses how sensitive is the power at measurement point $i$ to changes in the temperature at measurement point $j$

$$[\mathbf{S}]_{i,j} = \frac{\Delta P^i}{\Delta T^j},$$

where $\Delta P^i$ and $\Delta T^j$ denote an infinitesimal increment in $P^i$ and $T^j$ respectively. From matrix $\mathbf{S}$, as an example, we can see that $1\,\mathrm{W}$ of power dissipation on $\mathrm{Q_h}$ produce a $13.5\,^\circ\mathrm{C}$ increment on its own temperature and only $0.5\,^\circ\mathrm{C}$ on the inductor. Due to their small size, the drivers of the high and low sides are the two main sources of sensitivity to changes in power. On the other hand, it can be observed that the transistors and the PCB tracks are highly coupled to the other parts of the converters, proving that the coupling effects have a major impact in their power losses. It is also seen that the inductor is the most isolated part of the power converter. Our proposed approach can be directly used to conduct this kind of analyses without the need of complex analytical formulations, applicable to any power converter topology and configuration. By identifying a linear discrete-time dynamical system, our approach cannot only be used to analyze the sensitivity of the power converter, but also leverage other control theory tools to analyze the controllability and stability of the power-temperature dynamics. None of this is possible with a black-box model.

### *B. Validation through direct measurements*

The previous section has validated the performance in the estimation of semiconductor power losses through the novel automatic thermal modeling technique in static conditions. However, a validation in switching operating conditions is required to show the potential of the technique. Limitations on actual state-of-the-art methods for the switching losses measurements, as calorimetric or invasive current measurements, lead to a lack of a ground-truth model. Therefore, we validate the model with a switching power converter where almost all semiconductor dissipation is due to conduction losses and therefore easy to measure with conventional voltage and current probes. The converter switches at $1\,\mathrm{kHz}$ with a bus voltage from $1\,\mathrm{V}$ to $1.5\,\mathrm{V}$, so large power losses on the components are produced. Despite having high speed turn ON and OFF on the semiconductors ($7\,\mathrm{ns}$), the absence of high frequency switching and reduced bus voltage eliminates measurements complexities, such as possible switching effects from the output capacitance $C_{\mathrm{oss}}$. To do so, we enforce all losses to occur in the internal body diode of the MOSFET, as shown in Fig. 8.

The topology uses the internal DC resistance of the inductor (DCR, $21.5\,\mathrm{m\Omega}$) and shorts the output to produce a large current bias while keeping one of the semiconductors with zero gate voltage input. Fig. 8a shows the configuration where $\mathrm{Q_h}$ switches and $\mathrm{Q_l}$ is used as a diode. As it can be observed from the oscilloscope capture, when $\mathrm{Q_h}$ turns OFF, the current slope becomes negative along with a $12\,\mathrm{A}$ bias and the internal $\mathrm{Q_l}$ diode starts its conduction with forward voltage drop of around $0.65\,\mathrm{V}$. This operating point produces large losses that are only a consequence of conduction effects. Due to the large bias current, the inductor is also heated up so the model is fully validated as in a higher frequency point. Voltage variations on the ON state are provoked by a lack of decoupling capacitance; hence, for this low frequency operating point, an external $75\,\mathrm{mF}$ capacitance was included. The output capacitors are not relevant as most of the energy on the circuit is DC and not AC. Henceforth, the miss-match between the actual power losses

in the device and the ones predictable from the manufacturer data sheets is directly proportional to the forward voltage drop. We measured a forward voltage drop of $0.65\,\mathrm{V}$, whereas the manufacturer provides a value at room temperature of $0.82\,\mathrm{V}$. This non-linear variability in production stands out the need for experimental methods for power semiconductor losses estimation, because if the value of the manufacturer is used instead of the actual one, then we would have an error of $(0.82-0.65)/0.82\times 100 = 26\%$ with respect to the actual power losses. An error of $26\%$ is significant in power converters design and highlights the importance of our approach instead of purely relying on manufacturer's data sheets.

Similar effects take place when driving $\mathrm{Q_l}$ and forcing losses to occur on $\mathrm{Q_h}$. These are shown in Fig. 8b where the voltage supply along with its decoupling has been placed on the right side of the schematic. When $\mathrm{Q_l}$ turns OFF the current slope becomes negative and large losses are produced on both the high side device and the inductor. Alternately, when $\mathrm{Q_l}$ turns ON, the device stands no voltage due to the short-circuit.

Fig. 8 depicts the estimated and real power values for each of the two configurations for $\mathrm{Q_h}$ and $\mathrm{Q_l}$. For each of the operating points, four oscilloscope captures were processed and used for power representation. Estimates in Fig. 8a match the measured values with errors of less than $1\%$ in steady state. On the other hand, the error in Fig. 8b does not exceed the $3\%$. These results validate the performance of our approach for estimating the semiconductor losses on switching conditions. Moreover, the experiment also validates the superposition principle underpinning our approach, since the inductor, the PCB tracks, and one transistor (low-side in Fig. 8a, high-side in Fig. 8b) present significant thermal coupling, and still a worst-case accuracy below the $3\%$ of estimation error is achieved.

### C. Comparison with existing post-design approaches

This section compares the performance of our proposed method with to other existing a priori approaches. The state-of-the-art in physical-based thermal models either depart from Cauer or Foster models [58]. Although Cauer models provide more information about each layer of the thermal path, they are often complex to obtain, requiring FEM simulations. On the other hand, Foster models are more popular on power converters thermal modeling because they are based on the measurement of the temperature dynamics and are independent of the internal structure of the materials. Therefore, for this comparison, we extract a physical-based dynamic thermal model based on a Foster model [4]. The equivalent thermal circuit, shown in Fig. 9, contains the heat sources $P_{\mathrm{Q,h}}$ and $P_{\mathrm{Q,l}}$, which denote the power losses in each of the semiconductors; the thermal capacitance $C_{\mathrm{th,hs}}$ of the heat sink connected to $\mathrm{Q_h}$ and $\mathrm{Q_l}$; and the thermal resistance $R_{\mathrm{th,hs\text{-}a}}$ between the heat sink and the ambient; $T_{\mathrm{amb}}$ denotes the ambient temperature. In addition, it includes the thermal capacitances $C_{\mathrm{th,h}}$ and $C_{\mathrm{th,l}}$ of the case of $\mathrm{Q_h}$ and $\mathrm{Q_l}$, and the network of resistances formed by $R_{\mathrm{th,h}}$, $R_{\mathrm{th,l}}$ and $R_{\mathrm{th,m}}$. The resistances $R_{\mathrm{th,h}}$ and $R_{\mathrm{th,l}}$ denote the thermal resistance between the heat sink and the case of $\mathrm{Q_h}$ and $\mathrm{Q_l}$, respectively, while $R_{\mathrm{th,m}}$ models the thermal coupling between $\mathrm{Q_h}$ and $\mathrm{Q_l}$.

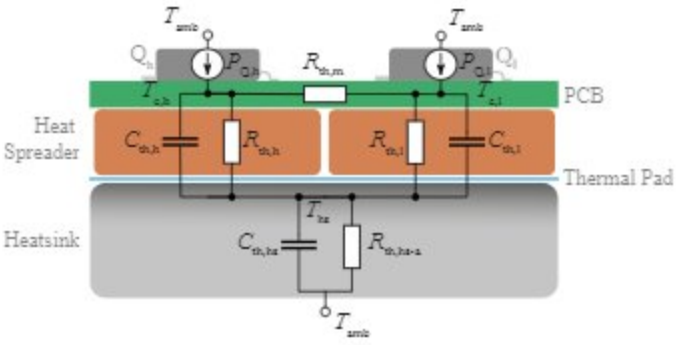


Fig. 9. Thermal equivalent circuit of the semiconductors power losses. The figure is inspired by [4].

The system of ordinary differential equations describing the evolution of $T_{\mathrm{c}}$ over time is

$$\begin{bmatrix}\dot{T}_{\mathrm{c,h}}\\ \dot{T}_{\mathrm{c,l}}\end{bmatrix}=\begin{bmatrix}-\frac{R_{\mathrm{th,h}}+R_{\mathrm{th,m}}}{C_{\mathrm{th,h}}R_{\mathrm{th,h}}R_{\mathrm{th,m}}} & \frac{1}{C_{\mathrm{th,h}}R_{\mathrm{th,h}}}\\ \frac{1}{C_{\mathrm{th,l}}R_{\mathrm{th,m}}} & -\frac{R_{\mathrm{th,l}}+R_{\mathrm{th,m}}}{C_{\mathrm{th,l}}R_{\mathrm{th,l}}R_{\mathrm{th,m}}}\end{bmatrix}\begin{bmatrix}T_{\mathrm{c,h}}\\ T_{\mathrm{c,l}}\end{bmatrix}+\begin{bmatrix}\frac{P_{\mathrm{Q,h}}}{C_{\mathrm{th,h}}}\\ \frac{P_{\mathrm{Q,l}}}{C_{\mathrm{th,l}}}\end{bmatrix} \quad (12)$$

where $R_{\mathrm{th,hs}}$ and $C_{\mathrm{th,hs}}$ are not included, as no heat sink was mounted on our setup. To proceed with the identification of $\mathcal{P}=\{R_{\mathrm{th,h}}, R_{\mathrm{th,l}}, R_{\mathrm{th,m}}, C_{\mathrm{th,h}}, C_{\mathrm{th,l}}\}$, we use a trust region reflective nonlinear optimization method [59] under the following cost function

$$\min_{\mathcal{P}}\sum_{k=2}^{K}||\mathbf{u}(k)-(\mathbf{I}-\Delta t\mathbf{F})\mathbf{u}(k-1)-\mathbf{G}\mathbf{x}(k-1)||_2^2, \quad (13)$$

where

$$\mathbf{F}=\begin{bmatrix}-\frac{R_{\mathrm{th,h}}+R_{\mathrm{th,m}}}{C_{\mathrm{th,h}}R_{\mathrm{th,h}}R_{\mathrm{th,m}}} & \frac{1}{C_{\mathrm{th,h}}R_{\mathrm{th,h}}}\\ \frac{1}{C_{\mathrm{th,l}}R_{\mathrm{th,m}}} & -\frac{R_{\mathrm{th,l}}+R_{\mathrm{th,m}}}{C_{\mathrm{th,l}}R_{\mathrm{th,l}}R_{\mathrm{th,m}}}\end{bmatrix},\ \mathbf{G}=\begin{bmatrix}\frac{1}{C_{\mathrm{th,h}}}\\ \frac{1}{C_{\mathrm{th,l}}}\end{bmatrix} \quad (14)$$

and $\Delta t = 1\,\mathrm{s}$. The expression $(\mathbf{I}-\Delta t\mathbf{F})\mathbf{u}(k-1)+\mathbf{G}\mathbf{x}(k-1)$ comes from the Euler-forward discretization of (12). Observe that the cost function of the optimization problem is nonlinear and nonconvex with respect to the parameters to be identified. Fig. 9 represents the dynamic equivalent circuit model that leads to (12).

Fig. 10 compares the identification error $\tilde{\mu}_{\mathrm{RMSE}}$ for our approach and that from [4] by using operating points from saturation regime. It can be seen that both methods achieve the same accuracy after only a few seconds from changing the working point, proving that, despite its generality, ours preserves the identification accuracy of state-of-the-art methods. Significantly, this is done without the need of physical and mathematical modeling, which is a key aspect for more intricate topologies. Besides, there is an additional caveat observed in [4]. Since the cost function is nonlinear and nonconvex in the parameters, the solution obtained by the trust region method is highly dependent on the initialization value. We tried two initialization shown in Table I.

In this sense, in TableI it can be observed that, after optimization, the final values can change dramatically depending on the initial seeds. Therefore, it is hard to extract a physical meaning from the method in [4]. In fact, Foster models do

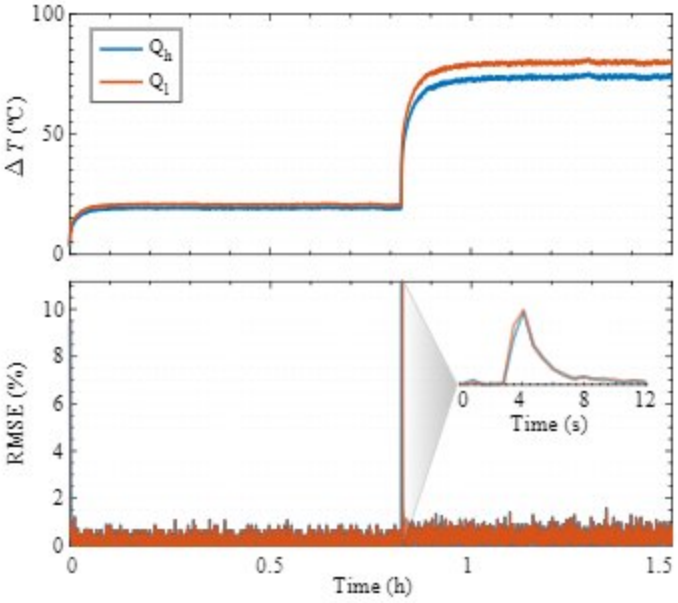


Fig. 10. Comparison of the equivalent circuit method and the automatic methods. Top figure shows one saturation regime operating point. Bottom figure shows the relative error results from the comparison of the equivalent circuit method and the automatic methods where a sectional zoom is applied to the transition stage for a better visualization. Automatic results are depicted in dashed lines while equivalent circuit method results are represented with bold lines with less color opacity.

TABLE I
PARAMETERS OF THE THERMAL EQUIVALENT CIRCUIT CONSIDERED TO PERFORM THE POWER LOSS ESTIMATION.

| | **Initial 1** | **Final 1** | **Initial 2** | **Final 2** |
|---|---|---|---|---|
| $R_{th,h}$(°C/W) | 3.9 | 87.1 | 0.8 | 3.4 |
| $R_{th,l}$(°C/W) | 3.3 | 96.0 | 0.1 | 1.2 |
| $R_{th,m}$(°C/W) | 30 | 41.4 | 0.6 | 2.9 |
| $C_{th,h}$(J/°C) | 1.5 | 3308.7 | 0.9 | 15699.0 |
| $C_{th,l}$(J/°C) | 1.8 | 393.6 | 0.9 | 13936.1 |

not provide a unique representation of a specific system. In contrast, our method, by proposing a linear method and a linear convex cost function, obtains the unique minimizer of the optimization function and, therefore, there is no dependence on the initialization of the parameters, leading to a unique representation.

## VI. CONCLUSION

This work has presented a novel automatic technique for the estimation of semiconductor power losses in power converters. The solution builds upon an optimization-based identification of the linear discrete-time dynamic system that best describes a set of power-temperature profiles. On the one hand, a least square objective finds the linear matrices that obtain the best accuracy. Additionally, the constraints of the optimization problem can be tuned to ensure desired requirements. For instance, by forcing full-rank of the matrices, the resulting model can be inverted, so the mapping of power to temperature can be inverted to predict the power losses in the different parts of the power converter given temperature measurements. Furthermore, the method accounts for noise in the measurements and other sources of uncertainty by means of regularizers. The experiments have shown that the proposal is general and accurate in a variety of scenarios, including switching operating conditions, and surpassing other post-design approaches in accuracy and interpretability. We have also provided different practical insights to characterize the temperature-power model of the converter, such as how to calibrate the different components of a power converter.

Future work will aim at developing an active identification version of the proposal. Instead of running several experiments to collect data, we can leverage information metrics to decide which is the next experiment that best improves the accuracy of the model. This can reduce the number and cost of the experiments, while avoiding the use of redundant data that can bias the identified dynamics. In addition, further work will be aimed to the split of switching and conduction losses on the semiconductor devices and on the study of external factor that could change the model through out its use as perturbations or device degradation.

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