PLANOS

Diseño de una PCB para monitorización de ganado mediante comunicación LoRa

Autor/es

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Director/es

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Escuela de Ingeniería y Arquitectura

2022

DATOS DEL PROYECTO

Título del proyecto	PCB para monitorización de ganado
Código del proyecto	TFG2022
Documento	Memoria
Número de volumen	Volumen 1
Cliente	Universidad de Zaragoza
Autor	Fernando Ferrer de Gonzalo
Firma Autor: 20/11/2022	Cliente: EINA - Universidad de Zaragoza

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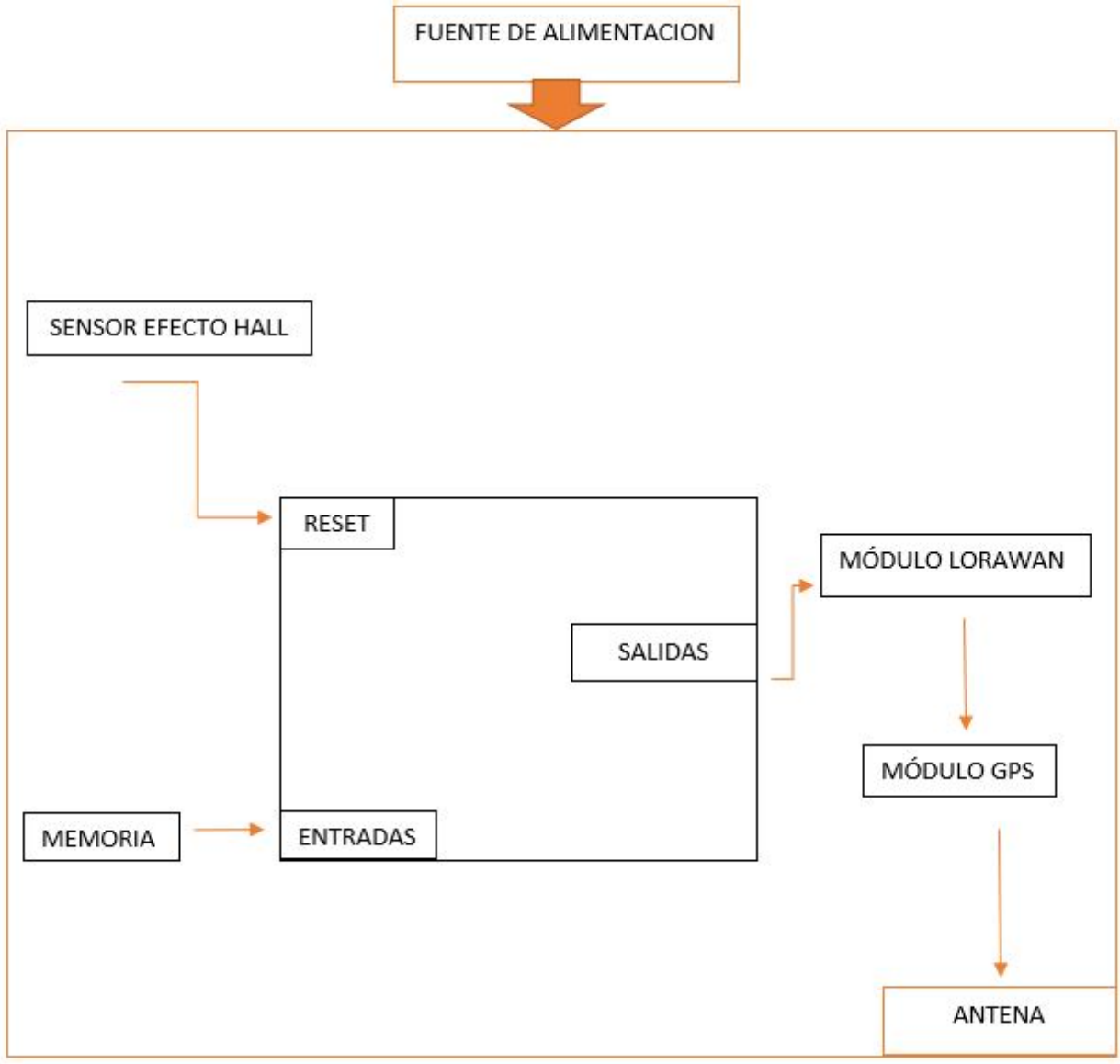

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Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo	DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Diagrama de bloques		Curso 2021/2022 Plano Nº 1

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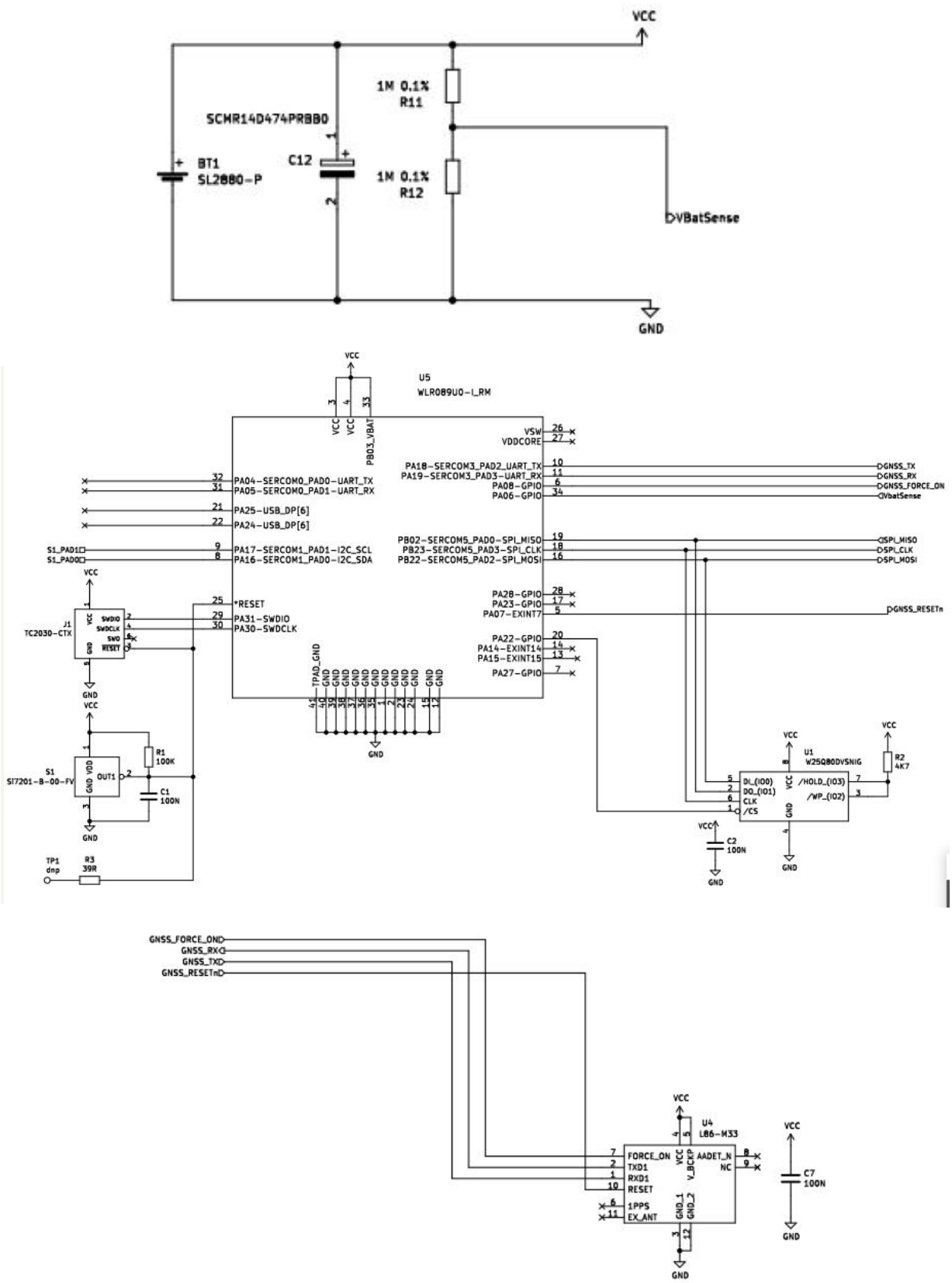

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Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo	DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de esquema general del circuito		Curso 2021/2022 Plano Nº 2

Identificación general	Encapsulado	X	Y	Valor
ANT1	0,1x100mm	119,24	129,46	
BT1	33,6x 59	-	-	19Ah
S1	SOT-23-3	109,08	101,52	-
U1	SOIC 8	116,7	106,6	-
U4	L86-M33	159,88	106,6	-
U5	41 PIN 13,5x17mm	121,78	121,84	-
R1	0603	106,54	104,06	100K
R2	0603	116,7	101,52	4K7
R3	0603	126,86	116,76	39R
R11	0805	109,08	126,92	1M
R12	0805	109,08	129,46	1M
C1	0603	114,16	101,52	100nF
C2	0603	115,35	101,52	100nF
C7	0603	172,58	109,14	100nF
C12	8X14mm	182,74	111,68	470mF
F1	0805	180,2	126,92	-
J1	-	104	111,68	-

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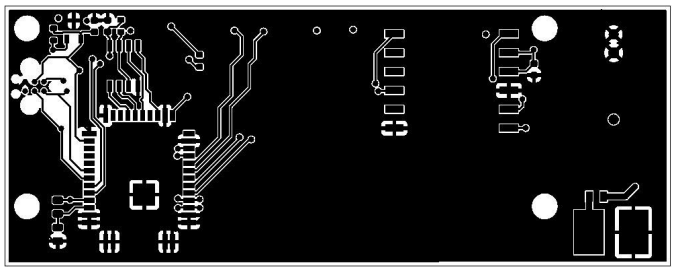
Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de listado de componentes de la placa base			Curso 2021/2022 Plano Nº 3



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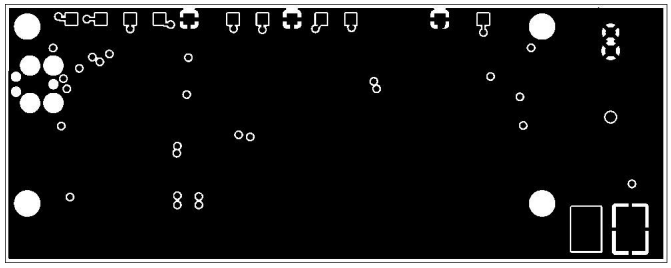
Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de circuito impreso de la placa base. Cara top			Curso 2021/2022 Plano Nº 4



	Fecha	Nombre	Firma:	
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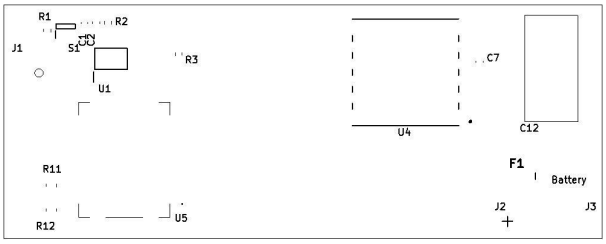
Comprobado				
Escala S/E	Titulo DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de circuito impreso de la placa base. Cara bot			Curso 2021/2022 Plano Nº 5



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Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de serigrafía de la placa. Cara top			Curso 2021/2022 Plano Nº 6

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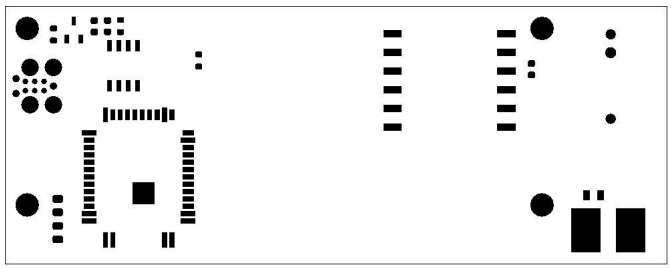

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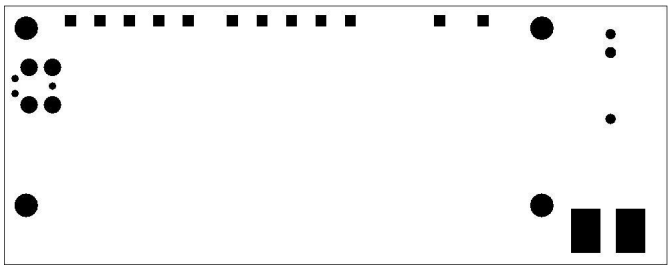
Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de mascarilla de la placa base. Cara top			Curso 2021/2022 Plano Nº 7



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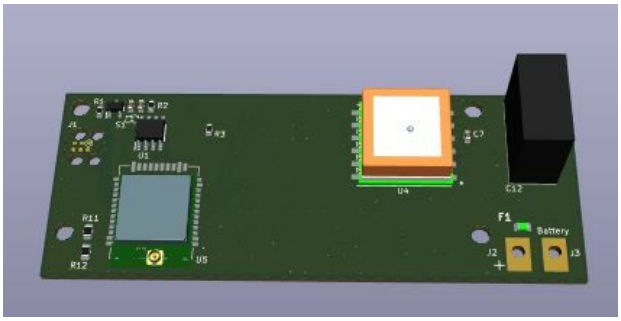
Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo	DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de mascarilla de la placa base. Cara bot		Curso 2021/2022 Plano Nº 8



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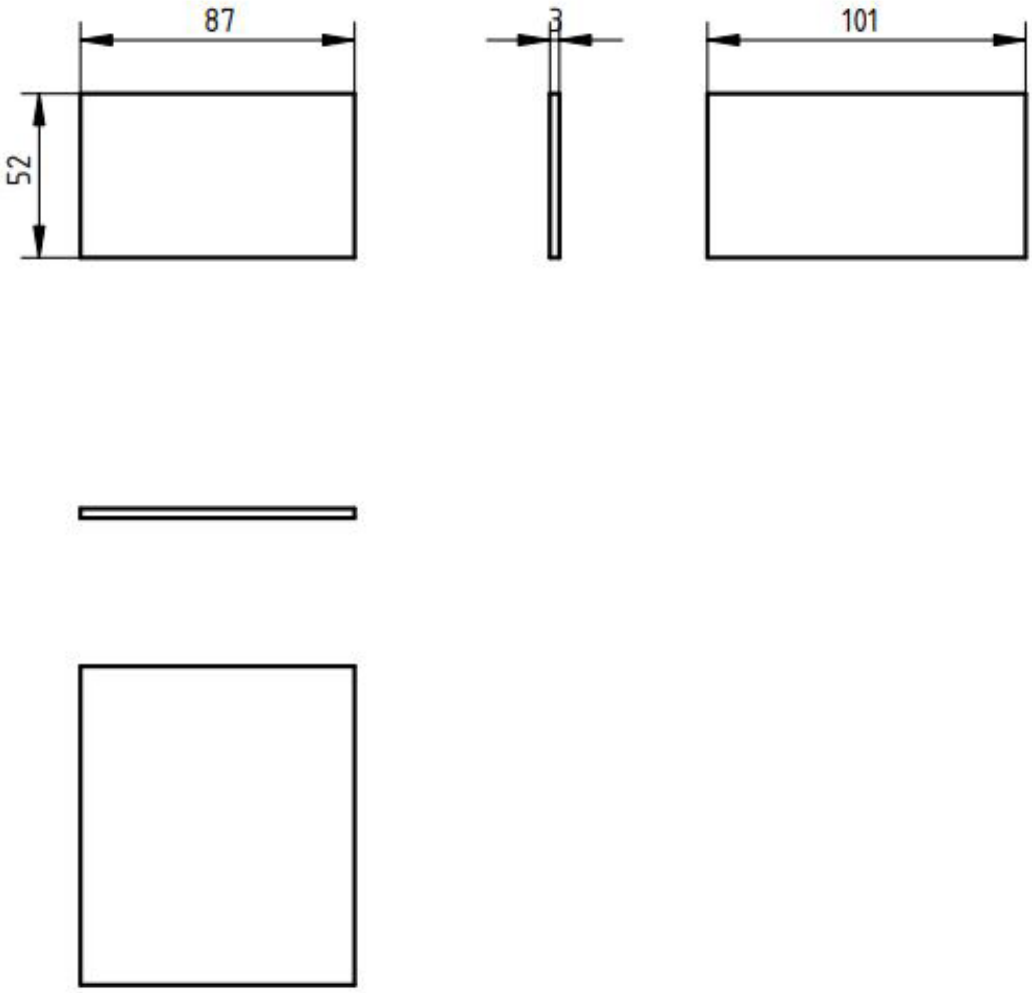
Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo	DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de modelado 3D de la placa base		Curso 2021/2022 Plano Nº 9

MATERIAL: PLA - ÁCIDO POLILÁCTICO



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Dibujado		Ferrer de Gonzalo, Fernando		Escuela de Ingeniería y Arquitectura Universidad Zaragoza
Comprobado				
Escala S/E	Titulo	DISEÑO DE UNA PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORA Plano de carcasa de la PCB		Curso 2021/2022 Plano Nº 10

A4

PRESUPUESTO

Diseño de una PCB para monitorización de ganado mediante comunicación LoRa

Autor/es

Fernando Ferrer de Gonzalo

Director/es

Miguel Ángel Torres Portero

Pablo Bosque Obón

Escuela de Ingeniería y Arquitectura

2022

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1. Introducción

Todos los precios que se muestran en este documento son en Euros como moneda y no incluyen el 21% de IVA. El precio total con IVA se mostrará en el último apartado de los presupuestos con el precio total del conjunto para fabricaciones y prototipos.

2. Prototipos

2.1 Componentes internos

Identificación general	Descripción	Proveedor	Precio unitario	Precio total
ANT1	Antena	Mouser	1,53	1,53
BT1	Batería	Mundilec	10,8	10,8
C12	Condensador	Mouser	2,6	2,6
S1	Sensor	Mouser	1,11	1,11
U1	Memoria	Mouser	0,515	0,515
U4	Módulo GPS	Mouser	12.81	12,81
U5	Módulo LoRa	Mouser	16,17	16,17
F1	Fusible	Mouser	0,46	0,46

Precio total de componentes internos 45,99€/unidad

2.2 Componentes externos

En esta placa no hay componentes externos que no vayan montados en la misma PCB.

2.3 Montaje y resto de componentes

Artículo	Proveedor	Precio/unidad
Gastos de industrialización del producto	Electrónica Falcón	537,16€
Componentes restantes, montaje de componentes y test visual	Electrónica Falcón	31,71€

El montador de la PCB proporcionará los componentes de menor valor, conocidos como "comodities". Además incluirá el circuito impreso y el montaje de todos los componentes (SMD y TH). Para iniciar el proyecto, deberemos abonar una cantidad en concepto de gastos de industrialización del producto, que se pagará solo una vez y será en el primer montaje. Por último la oferta, incluye barnizado y test visual del montaje para asegurar que la placa no contiene errores en cuanto al montaje.
Precio total del montaje y resto de componentes 58,57€/unidad

3. Fabricaciones

3.1 Componentes internos

Identificación general	Descripción	Proveedor	Precio unitario	Precio total
ANT1	Antena	Arrow	1,03	1,03
BT1	Batería	Mundilec	8,65	8,65
C12	Condensador	Arrow	1,75	1,75
S1	Sensor	Arrow	0,78	0,78
U1	Memoria	Arrow	0,37	0,37
U4	Módulo GPS	Arrow	9,6	9,6

U5	Módulo LoRa	Arrow	11,32	11,32
F1	Fusible	Mouser	0,34	0,34

Precio total de componentes internos 33,84€/unidad

3.2 Componentes externos

En esta placa no hay componentes externos que no vayan montados en la misma PCB.

3.3 Montaje y resto de componentes

Artículo	Proveedor	Precio/unidad
Componentes restantes, montaje de componentes y test visual	Electrónica Falcón	22,98€

Para la esta fabricación y las posteriores no se pagarán gastos de industrialización ya que estos solo se han de pagar en una ocasión al iniciar el proyecto. Estos gastos ya se habrán pagado en el montaje de los prototipos.
Precio total de montaje y resto de componentes 22,98€/unidad

4. Partida de pruebas y ensayos

4.1 Partida de pruebas

En este proyecto, tanto la verificación de la fabricación de la PCB como la del montaje están incluidas en el presupuesto de montaje de la empresa Electrónica Falcón.

4.2 Partida de ensayos

Ensayo	Normativa	Proveedor	Precio unitario	Precio total
Descarga electrostática	UNE-EN_61000-4-2	Dekra	82,25€	82,25€
Transitorios rápidos	UNE-EN_61000-4-4	Dekra	82,25€	82,25€
Tensión de radiofrecuencia	UNE-EN_61000-4-3	Dekra	82,25€	82,25€
Campos de radiofrecuencia	UNE-EN_61000-4-3	Dekra	82,25€	82,25€
Ondas de choque	UNE-EN_61000-4-5	Dekra	82,25€	82,25€
Campos magnéticos	UNE-EN_61000-4-8	Dekra	82,25€	82,25€
Emisiones conducidas	IEC 61000-4-3	Dekra	82,25€	82,25€
Huecos de tensión	UNE-EN_61000-4-11	Dekra	82,25€	82,25€
Emisiones radiadas	UNE-EN_61000-4-3	Dekra	82,25€	82,25€
Emisión baja frecuencia	UNE-EN_61000-4-3	Dekra	82,25€	82,25€
Choque eléctrico	UNE-EN_60068-2-27	Dekra	82,25€	82,25€
Resistencia aislamiento	UNE-EN_60881	Dekra	82,25€	82,25€
Puesta a tierra	UNE 20460-6-61	Dekra	82,25€	82,25€
Calentamientos	UNE-EN 1363-1	Dekra	82,25€	82,25€
Calor y corriente superficial	UNE-EN_60598-1	Dekra	82,25€	82,25€
Resistencia mecánica	UNE-EN-196-1	Dekra	82,25€	82,25€
Funcionamiento anormal	UNE-EN-60950-1	Dekra	82,25€	82,25€
IP	UNE-EN 60670-1, UNE-EN 61439-1 y UNE-EN 62208	Dekra	82,25€	82,25€
Marcado CE	Constituido por los ensayos realizados	Dekra	82,25€	82,25€

Precio total de ensayos 78,14€/unidad

5. Embalaje y logística

Artículo	Proveedor	Precio/unidad
Caja de cartón donde irá protegida la PCB	Cartonajes Santorromán	0,25

Aparte de los gastos mencionados relacionados con la PCB, nos proveerá las cajas de cartón donde irá cada PCB protegida la empresa calagurritana Cartonajes Santorromán.
Precio total de embalaje y logistica 0,25€/unidad

6. Valoración y presupuesto global

6.1 Prototipos

Partida		Precio/unidad
Materiales y componentes	Internos	45,99
	Externos	-
Montaje y resto de componentes		58,57
Embalaje y logística		0,25
Partida de pruebas y ensayos		78,14
Total		182,95

6.2 Fabricaciones

Partida		Precio/unidad
Materiales y componentes	Internos	33,84
	Externos	-
Montaje y resto de componentes		22,99
Embalaje y logística		0,25
Total		57,08

El presupuesto final de los prototipos resulta caro. Sin embargo, el precio elevado de los prototipos se debe en su mayor cuantía a los ensayos realizados para la certificación y verificación del producto. Esto además se puede ver en las fabricaciones, en las cuales se observa la reducción del precio para cada placa en dos tercios respecto a los prototipos. De esta forma, obtenemos un producto con un precio bastante razonable para fabricaciones teniendo en cuenta tanto los componentes tan específicos que usaremos como la fabricación y montaje de la PCB.

El beneficio económico de este proyecto es evidente. Al ser un producto de valor añadido, vendiéndolo con un 30% sobre el coste del producto tendríamos unos beneficios totales de 164,5€ en los 20 prototipos y de 42810€ en la primera fabricación de 2500 unidades.

Esto hace que sea un proyecto rentable desde la primera fabricación en masa y más aún en futuras fabricaciones ya que es un producto que tiene un amplio mercado teniendo en cuenta la cantidad de cabezas de ganado existentes.

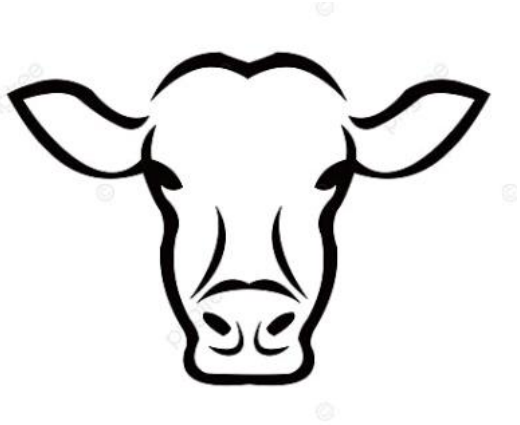
Por último cabe puntualizar que los precios que estamos manejando en este documento no incluyen IVA y que serán un 21% mayor que el valor indicado para cumplir con la normativa vigente del impuesto sobre el valor añadido.

PCB PARA MONITORIZACION DE GANADO MEDIANTE COMUNICACIÓN LORAWAN

MANUAL DE INSTRUCCIONES

SOBRE LA PCB

Mediante este dispositivo, podemos además de saber la posición cada pocos minutos de cada pieza de ganado, establecer patrones sobre el movimiento diario que cada animal realiza. Además, a través del conocimiento de la posición de cada animal, podemos alertarnos rápidamente si recibimos un reporte de una posición extraña, anticipándonos a perdidas o incluso ataques de algún otro animal.



Contenido por caja:

- **1 PCB para monitorización de ganado a través de comunicación LoRaWAN**
- **1 caja para protección de la PCB**

EN ESTE MANUAL ENCONTRARÁS:

SOBRE LA PCB PARA MONITORIZACION DE GANADO 1

ESPECIFICACIONES TÉCNICAS 3

CARACTERISTICAS ELECTRICAS 3

CARACTERISTICAS FISICAS 3

ADVERTENCIAS 3

PRECACIONES DE USO 3

DESECHO DEL PRODUCTO 4

FUNCIONAMIENTO 4

MANTENIMIENTO 5

GARANTÍA 5

ESPECIFICACIONES TÉCNICAS:

CARACTERISTICAS ELÉCTRICAS:

- Alimentación con una pila incluida a 3,6V
- Bajo consumo de energía
- Modo sleep cuando el sistema no está trabajando
- Posibilidad de reseteado mediante el acercamiento de un imán
- Marcado CE

CARACTERISTICAS FÍSICAS:

- Dimensiones
- Material de la carcasa PLA
- Color: Gris

ADVERTENCIAS DE USO:

PRECAUCIONES DE USO:

- No sumergir el dispositivo en agua u otros líquidos
- Producto resistente frente a la lluvia o salpicaduras
- No tratar de manipular el dispositivo situado en el interior de la carcasa. Toda reparación proveniente de esta práctica correrá a cuenta del cliente. En caso de fallo o funcionamiento anormal póngase en contacto con el servicio técnico
- Evitar golpear el dispositivo en la medida que sea posible

DESECHO DEL PRODUCTO:

Evitar arrojar a la basura el producto una vez este llega al final de su vida útil ya que contiene componentes electrónicos y una pila.

Todos los residuos eléctricos y/o electrónicos han de reciclarse aparte de la recogida municipal de basuras. Entréguese en los puntos oficiales designados por el gobierno y/o autoridades locales.

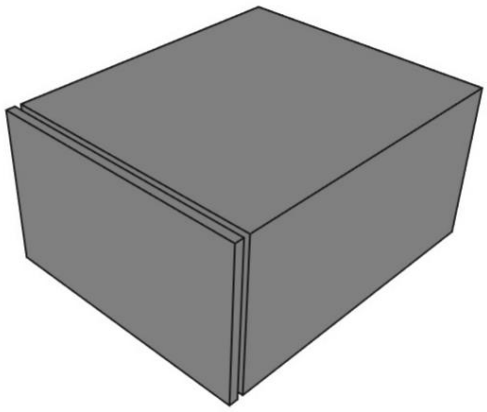
FUNCIONAMIENTO:

Para poner en funcionamiento este dispositivo, sencillamente asegúrese de ponerlo bien sujeto al animal que se desea geolocalizar. Una vez comprobado esto avisar al servicio técnico al que usted ha sido delegado.

Una vez avisado el servicio técnico, esperar durante 5 minutos para recibir en su móvil la primera ubicación del dispositivo y comprobar que coincide con la posición en la que está situado el dispositivo.

En caso de no coincidir la ubicación o de cualquier otro problema, contactar inmediatamente con el servicio técnico para la resolución del problema.

Una vez instalado el dispositivo y corroboradas la primera y/o primeras ubicaciones, este comienza a funcionar y usted podrá recibir la situación de su ganado cada cierta frecuencia de tiempo previamente establecida.



MANTENIMIENTO:

En situaciones en las que el dispositivo no este situado en el cuello del animal en cuestión, guardar el dispositivo en lugares situados lejos de altas frecuencias o con elevados campos magnéticos para evitar el reseteo del dispositivo o cualquier defecto que pueda ser causado por altas frecuencias.

En caso de cualquier defecto o rotura no manipular el dispositivo, avisar al servicio técnico encargado de reparaciones.

GARANTIA:

El dispositivo para monitorización de ganado mediante comunicación LoRaWAN adquirido, siempre y cuando se utilice según este manual de instrucciones, evitando su manipulación por parte del usuario en caso de mal funcionamiento o avería, está garantizado por el plazo de 24 meses a partir de la fecha de compra.

Cualquier apertura de la carcasa o desmonte del producto provoca la pérdida de la garantía, sin importar el problema causante del mal funcionamiento.

Para beneficiarse de esta garantía, será necesaria una aceptación previa por parte del departamento técnico encargado del producto, del defecto de fábrica, siendo necesario devolver el dispositivo con la documentación requerida y debidamente cumplimentada.

La garantía de este dispositivo cubre la reposición del material sin cargo alguno, amparando esta solo a defectos de fábrica.

La aparición de modelos nuevos o actualizados no obliga a la empresa a modificar dispositivos ya fabricados.

L86 Hardware Design

GNSS Module Series

Rev. L86_Hardware_Design_V1.0

Date: 2014-09-04

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History

Revision	Date	Author	Description
V1.0	2014-09-04	King HAO	Initial

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1 Introduction

This document defines and specifies L86 GNSS module. It describes L86 module hardware interfaces and its external application reference circuits, mechanical size and air interface.

This document can help you quickly understand the interface specifications, electrical and mechanical details of L86 module. Other documents such as L86 software application notes and user guider are also provided for you. These documents can ensure you use L86 module to design and set up applications quickly.

2 Description

2.1. General Description

L86 GNSS module with an embedded patch antenna (18.4mm × 18.4mm × 4mm) and LNA brings high performance of MTK positioning engine to the industrial applications. It is able to achieve the industry's highest level of sensitivity, accuracy and TTFF with the lowest power consumption in a small-footprint lead-free package. The embedded flash memory provides capacity for users to store some useful navigation data and allows for future updates.

L86 module combines with many advanced features including EASY, AIC, LOCUS, AlwaysLocate™ and Antenna Supervisor. These features are beneficial to accelerate TTFF, improve sensitivity, save consumption and detect antenna status for GNSS system. The module supports various location, navigation and industrial applications including autonomous GPS, GLONASS, SBAS (including WAAS, EGNOS, MSAS, and GAGAN), QZSS, and AGPS.

L86 module simplifies the device's design and cost because of embedded patch antenna and LNA. Furthermore, L86 module not only supports automatic antenna switching function, which can achieve switching between external active antenna and internal patch antenna, but also supports external active antenna detection and short protection. The detection and notification of different external active antenna status will be shown in the NMEA message including external active antenna connection, open circuit for antenna and antenna short-circuited. So host can query the external active antenna status timely and conveniently.

EASY technology as the key feature of L86 module is one kind of AGPS. Collecting and processing all internal aiding information like GPS time, Ephemeris, Last Position etc., the GNSS module will have a fast TTFF in either Hot or Warm start.

L86 module is a SMD type module with the compact 18.4mm × 18.4mm × 6.45mm form factor, which can be embedded in your applications through the 12-pin pads with 2.54mm pitch. It provides necessary hardware interfaces between the module and main board.

The module is fully ROHS compliant to EU regulation.

2.2. Key Features

Table 1: Module Key Features

Feature	Implementation
GNSS	● GPS+GLONASS
Power Supply	● Supply voltage: 3.0V~4.3V typical: 3.3V
Power Consumption	● Acquisition: 26mA @VCC=V_BCKP=3.3V (GPS) ● Tracking: 22mA @VCC=V_BCKP=3.3V (GPS) ● Acquisition: 30mA @VCC=V_BCKP=3.3V (GPS+GLONASS) ● Tracking: 26mA @VCC=V_BCKP=3.3V (GPS+GLONASS) ● Standby: 1mA @VCC=V_BCKP=3.3V ● Backup: 7uA @V_BCKP=3.3V
Receiver Type	● GPS L1 1575.42MHz C/A Code ● GLONASS L1 1598.0625~1605.375MHz C/A Code
Sensitivity	● Acquisition: -148dBm ● Re-acquisition: -160dBm ● Tracking: -165dBm
TTFF (EASY enabled)	● Cold start: 15s typ. @-130dBm ● Warm start: 5s typ. @-130dBm ● Hot start: 1s typ. @-130dBm
TTFF (EASY disabled)	● Cold start (Autonomous): 35s typ. @-130dBm ● Warm start (Autonomous): 30s typ. @-130dBm ● Hot start (Autonomous): 1s typ. @-130dBm
Horizontal Position Accuracy (Autonomous)	● <2.5m CEP @-130dBm
Max Update Rate	● Up to 10Hz, 1Hz by default
Accuracy of 1PPS Signal	● Typical accuracy <15ns (Time service is not supported) ● Time pulse width 100ms
Velocity Accuracy	● Without aid: 0.1m/s
Acceleration Accuracy	● Without aid: 0.1m/s²
Dynamic Performance	● Maximum altitude: 18,000m ● Maximum velocity: 515m/s Maximum ● Acceleration: 4G
UART Port	● UART Port: TXD1 and RXD1 ● Supports baud rate from 4800bps to 115200bps, 9600bps by default ● UART port is used for NMEA output, MTK proprietary commands input and firmware upgrade

Temperature Range	● Normal operation: -40°C ~ +85°C ● Storage temperature: -45°C ~ +125°C
Physical Characteristics	● Size: 18.4±0.15 × 18.4±0.15 × 6.45±0.1mm ● Weight: Approx. 7.6g

NOTES

1. The power consumption is measured in the open sky with internal patch antenna, meanwhile, EASY, AIC and SBAS are enabled.
2. If the external active antenna is used, VCC pin will supply power for external active antenna. The typical additional current consumption is about 10mA @3.3V.
3. The performance of external active antenna is similar to that of internal patch antenna expect for power consumption.

2.3. Block Diagram

The following figure shows a block diagram of L86 module. It consists of a single chip GNSS IC which includes RF part and Baseband part, a SPDT, a patch antenna, a LNA, a SAW filter, a TCXO, a crystal oscillator, and short protection and antenna detection circuit for active antenna.

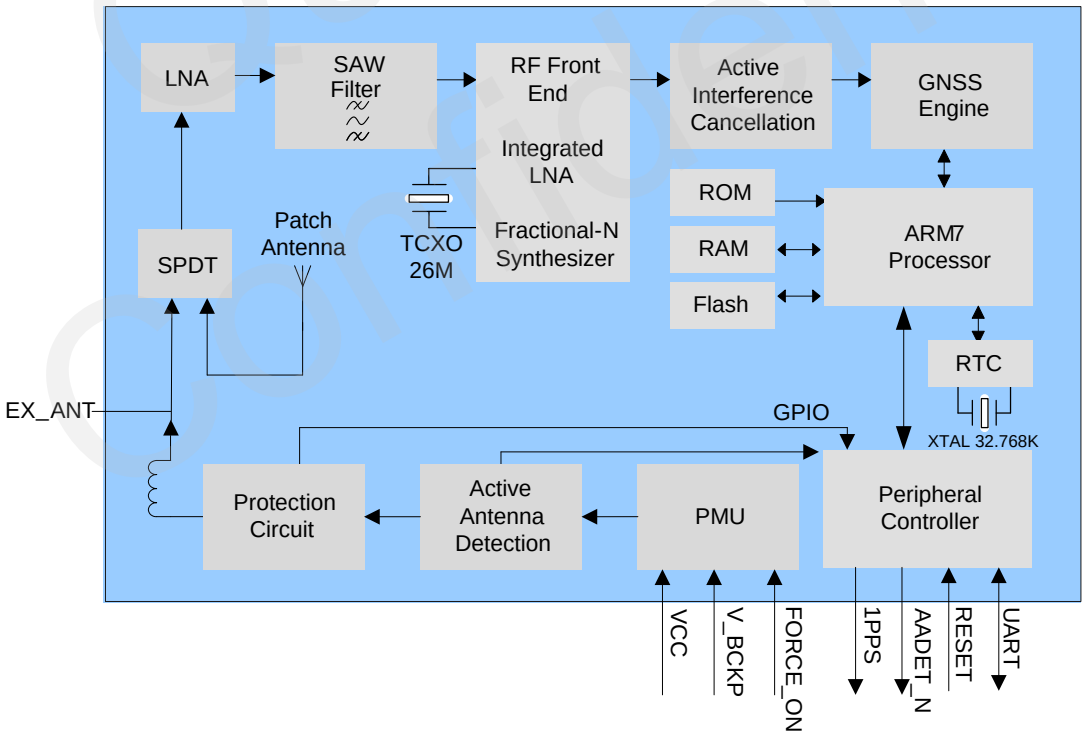


Figure 1: Block Diagram

WLR089U0 Low Power LoRa® Sub-GHz Module Data Sheet

Introduction

The WLR089U0 is a Long Range (LoRa) transceiver module for the sub-1GHz ISM bands such as 868 MHz (Europe) and 915 MHz (North America), optimized for ultra-low-power applications. This module combines the ATSAMR34J18B SiP (System-in-Package), 32.768 kHz crystal, 32 MHz TCXO, RF switch, lumped element harmonics rejection filter, impedance matching circuits, Low Pass Filter (LPF) and required RF shielding in a compact 17 mm x 13.5 mm design. The module supports LoRa® and FSK modulation.

The LoRa technology is a spread spectrum protocol optimized for low data-rate, ultra-long range signaling. It is ideal for battery-powered remote sensors and controls. The module also includes USB, making it suitable for USB dongle applications or for software updates via USB.

Note: For a detailed description on the supported peripherals, refer to the *SAM R34/R35 Low Power LoRa Sub-GHz SiP Datasheet (DS70005356)*.

Features

- Processor:
  - ARM Cortex -M0+ CPU running at up to 48 MHz (2.46CoreMark®/MHz)
    - Single-cycle hardware multiplier
    - Micro Trace Buffer (MTB)
- Memory:
  - In-system self-programmable 256 KB Flash memory
  - 32 KB Static Random Access Memory (SRAM)
  - 8 KB low power SRAM memory
- System:
  - Power-on Reset (POR) and Brown-out Reset (BOR)
  - Internal and external clock options with 48 MHz Digital Frequency Locked Loop (DFLL48M) and 48 MHz to 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - Up to 15 external interrupts
  - One Non-Maskable Interrupt (NMI)
  - 2-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Operating Voltage: 1.8V – 3.5V
- Low Power Consumption
  - Transceiver:
    - RX = 12.64 mA (typical)
    - RFO_HF = 41.54 mA (typical)
    - PA_BOOST = 114.68 mA (typical)
  - MCU:
    - Standby and Backup Sleep modes
    - SleepWalking peripherals
- Temperature Range: −40°C to +85°C (Industrial)

RF/Analog Features

- Integrated LoRa Technology Transceiver:
  - 863 MHz to 928 MHz dual-band coverage
  - +18.59 dBm maximum power (V_{CC} > 2.4 V_{DC})
- High Sensitivity:
  - -136 dBm (LoRaWAN® protocol compliant modes)
- Up to 154.59 dB Maximum Link Budget
- Robust Front-end: IIp3 = -11 dBm
- Excellent Blocking Immunity
- Fully Integrated Synthesizer with a Resolution of 61 Hz
- LoRa Technology and (G)FSK Modulations
- Preamble Detection
- 127 dB Dynamic Range RSSI
- Automatic RF Sense and Channel Activity Detection (CAD) with Ultra-Fast Automatic Frequency Control (AFC)
- Packet Engine up to 256 Bytes with Cyclic Redundancy Check (CRC)

Peripheral Information

- 16-Channel Direct Memory Access Controller (DMAC)
- 12-Channel Event System
- Three 16-bit Timer/Counters (TC), Configurable as Either of the Following:
  - One 8-bit TC with compare/capture channels
  - One 16-bit TC with compare/capture channels
  - One 32-bit TC with compare/capture channels, by using two TCs
- Two 24-bit and one 16-bit Timer/Counters for Control (TCC), with Extended Functions:
  - Up to four compare channels with optional complementary output
  - Generation of synchronized Pulse Width Modulation (PWM) pattern across port pins
  - Deterministic fault protection, fast decay and configurable dead-time between complementary output
  - Dithering that increases resolution with up to five bit and reduces quantization error
- 32-Bit Real Time Counter (RTC) with Clock/Calendar Function
- Watch-dog Timer (WDT)
- CRC-32 Generator
- One Full-speed (12 Mbps) Universal Serial Bus (USB) 2.0 Interface:
  - Embedded host and device function
  - Eight endpoints
- Up to Four Serial Communication Interfaces (SERCOM) Including One Low-Power SERCOM (SERCOM5(3)), Each Configurable to Operate as Either of the Following:
  - USART with full-duplex(1) or single-wire half-duplex configuration
  - I2C up to 3.4 MHz(2)
  - Serial Peripheral Interface (SPI)
  - Local Interconnect Network (LIN) client
- One 12-bit, 1 Msps Analog-To-Digital Converter (ADC) with up to Seven External Channels:
  - Differential and single-ended input
  - Automatic offset and gain error compensation
  - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
- Two Analog Comparators (AC) with Window Compare Function
- Peripheral Touch Controller (PTC)
  - 12-channel capacitive touch and proximity sensing
- 23 Programmable I/O Pins

Note:

1. SERCOM2 has only 2 interface lines for use so it can be used only for single-wire half-duplex configuration. USART Full duplex and SPI modes are not supported.
2. I2C support is available only in PA16, PA17, PA22 and PA23 pins.
3. SERCOM5, due to its location in Power Domain (PD0) in SAM L21, has a reduced feature set and does not support the following features:
   - DMA support
   - USART:
     - 3x or 8x oversampling
     - Flow control (RTS/CTS)
     - IrDA
     - Single wire UART according to EN54
     - Start of Frame (SOF)/End of Frame (EOF) function
   - I2C:
     - Fast mode plus (Fm+) and High-speed (Hs) mode
     - SMBus Serial Clock Low (SCL) timeout
     - 10-bit addressing
     - Power Management Bus (PMBus) group command support
   - SPI:
     - Hardware chip select
     - Wake on Serial Select (SS) assertion

1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

- *SAM R34-R35 Low Power LoRa Sub-GHz SiP Datasheet* (DS70005356)
- *SAM L21 Family Data Sheet* (DS60001477)
- *SAM R34/R35 Errata Sheet* (DS80000834)(1)
- *AN2468 Production Programming of Microchip AVR® and SAM Microcontrollers Application Note* (DS00002468)
- *Semtech SX1276/77/78/79 Low Power Long Range Transceiver Datasheet*
- *LoRaWAN® Regional Parameters*
- *WLR089U0 Module Reference Design Package* (available in www.microchip.com/WLR089U0)

Notes:

1. This Errata is also applicable for the WLR089U0 module.
2. For a complete list of development support tools and documentation, visit www.microchip.com/WLR089U0.

1.2 Acronyms/Abbreviations

Table 1-1. Acronyms/Abbreviations

Acronyms/Abbreviations	Description
AC	Analog Comparators
ADC	Analog-To-Digital Converter
AFC	Automatic Frequency Control
AHB	AMBA Advanced High-Performance Bus
AIN	Analog Inputs
AMBA	Advanced Microcontroller Bus Architecture
APB	AMBA Advanced Peripheral Bus
BOR	Brown-out Reset
BUPDIV	Backup Clock Division
BW	Bandwidth
CCL	Custom Control Logic
CPUDIV	CPU Clock Division
CRC	Cyclic Redundancy Check
CTS	Clear To Send
EC	Error Correction Code
EIC	External Interrupt Controller
EMI	Electro Magnetic Interference
FSK	Frequency Shift Keying
GCLK	Generic Clock Generator

.....continued

Acronyms/Abbreviations	Description
GPIO	General Purpose I/O pin
HVIN	Hardware Version Identification Number
IPA	Isopropyl alcohol
IrDA	Infrared Data Association
IRQ	Interrupt Request
ISM	Industrial, Scientific and Medical
LIN	Local Interconnect Network
LNA	Low Noise Amplifier
LoRa	Long Range
LoRaWAN®	Long Range Wide Area Network
LPDIV	Low Power Clock Division
MTB	Micro Trace Buffer
NMI	Non-Maskable Interrupt
OEM	Original Equipment Manufacturer
PA	Power Amplifier
PER	Packet Error Rate
PMN	Product Marketing Name
POR	Power-on Reset
PTC	Peripheral Touch Controller
RF	Radio frequency
RFI_HF	RF Input High Frequency
RFO_HF	RF Output High Frequency
RSSI	Received signal strength indication
RSTC	Reset Controller
RTC	Real Time Counter
RTS	Request To Send
RX	Receive/Receiver
SERCOM	Serial Communication
SF	Spreading Factor
SiP	System-in-package
SMBus	System Management Bus
SP3T	Single Pole Three Throw
SRAM	Static Random Access Memory
SUPC	Supply Controller
SWD	Serial Wire Debug

.....continued

Acronyms/Abbreviations	Description
TCXO	Temperature Compensated Crystal Oscillator
TRX	Transceiver
TX	Transmit/Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHF	Ultra-High Frequency
USART	Universal Synchronous and Asynchronous Receiver and Transmitter
USB	Universal Serial Bus
WDT	Watch-dog Timer
WiSUN	Wireless Smart Utility Network
WMBus	Wireless Meter Bus
WO	Waveform Outputs

2. Ordering Information

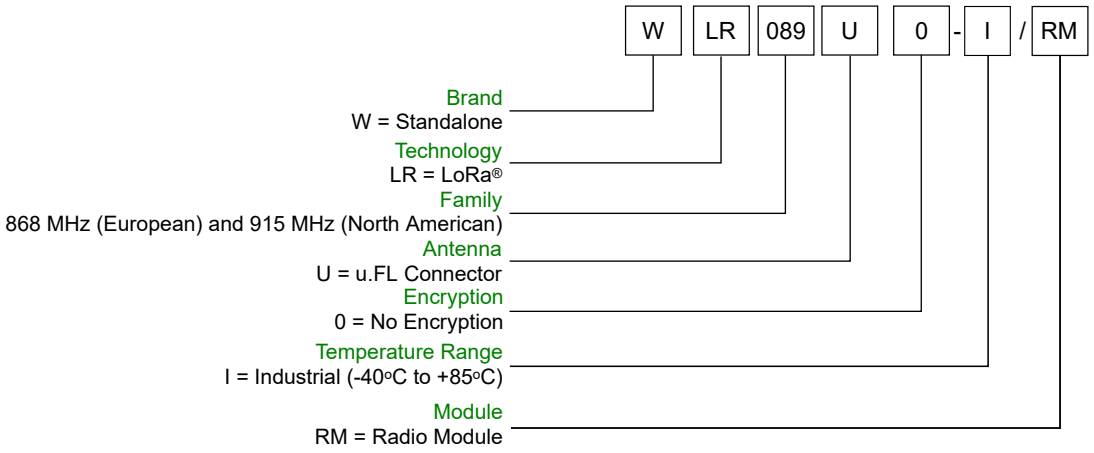
The following table provides the ordering details for the module.

Table 2-1. Ordering Information for WLR089U0

Model Number	IC Name	Description	Regulatory Approval	Ordering Code
WLR089U0	ATSAMR34J18B	Low Power Long Range (LoRa®) module with RF Shield CAN, u.FL connector for external antenna, castellated pads and available in Tray package.	FCC, ISED, CE, MIC, KC, NCC and Anatel	WLR089U0-I/RM

The following figure illustrates the module ordering code information.

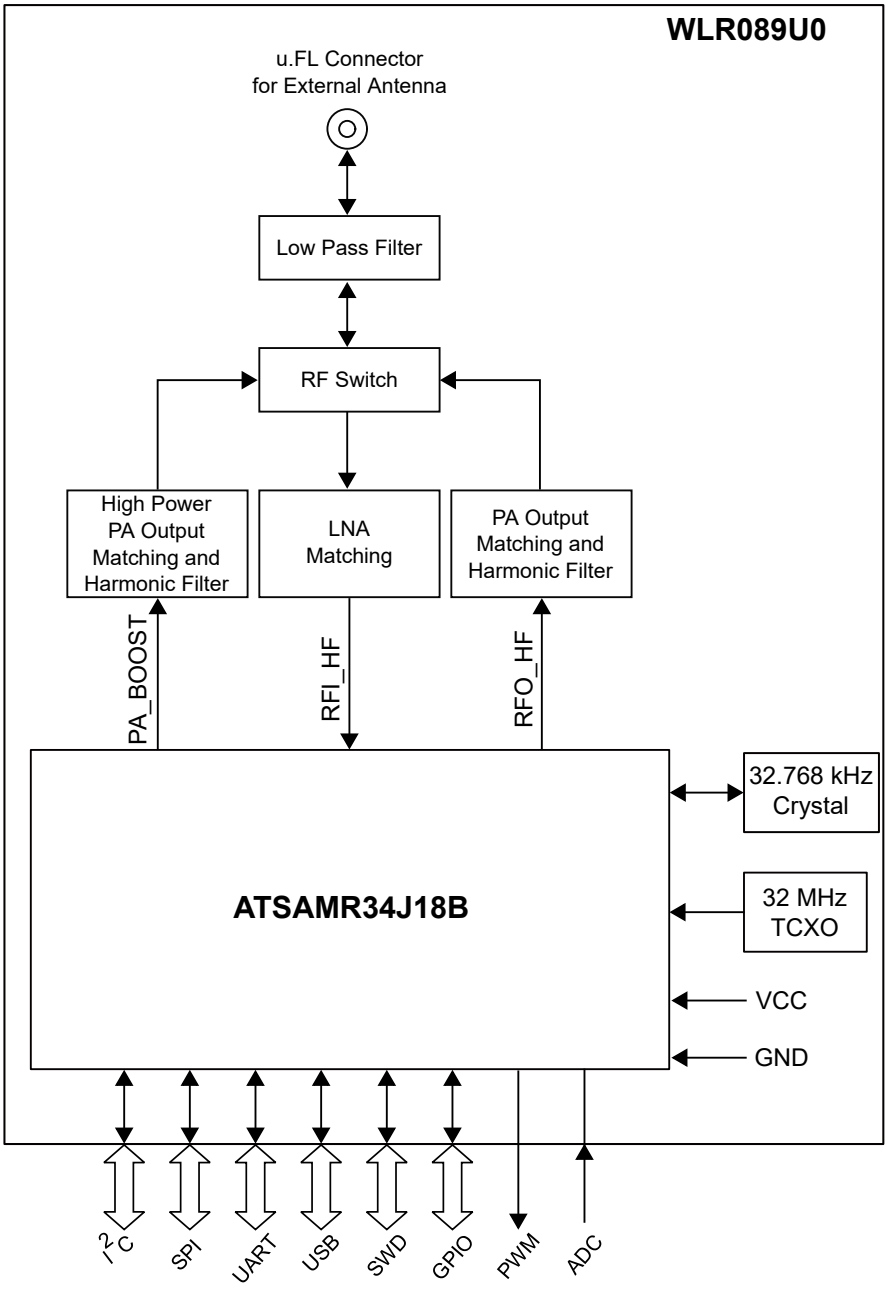
Figure 2-1. Module Ordering Code Information



3. Functional Overview

The WLR089U0 module contains ATSAMR34J18B SiP, 32.768 kHz crystal, 32 MHz TCXO, RF switch (SP3T), lumped element harmonic filter, RF matching components and a Low Pass Filter (LPF) (see the following figure).

Figure 3-1. WLR089U0 Module Block Diagram



Note: The ATSAMR34J18B SiP includes an ultra-low power SAM L21 ARM Cortex M0+ based microcontroller along with a low power long range transceiver.

3.1 ATSAMR34J18B SiP Description

The ATSAMR34J18B device is an ultra-low power microcontroller equipped with a UHF transceiver. It uses the 32-bit ARM Cortex-M0+ processor at the maximum 48 MHz (2.46 CoreMark/MHz) and offers 256 KB of Flash, 32 KB of SRAM and 8 KB of low power SRAM. Sophisticated power management technologies, such as power domain gating, SleepWalking, ultra-low power peripherals and more, allow for very low line-power consumptions.

The UHF transceiver supports LoRa and FSK modulation schemes. The LoRa technology is optimized for long-range communication with minimal line-power demand. The transceiver can work from 863 MHz to 928 MHz. The maximum transmit power is +18.59 dBm without an external amplification. Operational frequency bands and power limits are defined by local regulations and the LoRa Alliance. LoRa network stack regional options ensure compliance.

All devices have accurate low power external and internal oscillators. Different clock domains can be independently configured to run at different frequencies, enabling power-saving by running each peripheral at its optimal clock frequency, thus maintaining a high CPU frequency while reducing power consumption.

The ATSAMR34J18B device supports the following software-selectable sleep modes:

- Standby – All the clocks and functions are stopped except those selected to continue running, and all the RAMs and logic contents are retained.
- Backup – Allows achieving the lowest power consumption. In this mode, the device is entirely powered off except for the backup domain. The internal regulator is turned off and the power manager allows retaining the state of the I/O lines, preventing I/O lines from toggling during wake-up. The external wake-up function is active and the debounce counter is running if at least one external wake-up pin is enabled.

The ATSAMR34J18B device supports SleepWalking, which allows some peripherals to wake-up from sleep based on predefined conditions. Thus, allowing some internal operations like DMA transfer and/or the CPU to wake up only when needed; for example, when a threshold is crossed or a result is ready. The event system supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in Standby mode.

The ATSAMR34J18B device has two software selectable performance levels (PL0 and PL2), allowing the user to scale down to the lowest core voltage level that supports the operating frequency.

The device utilizes a power domain gating technique with retention to turn off some logic areas to minimize leakage current consumption while retaining their logic states. This technique is fully handled by hardware.

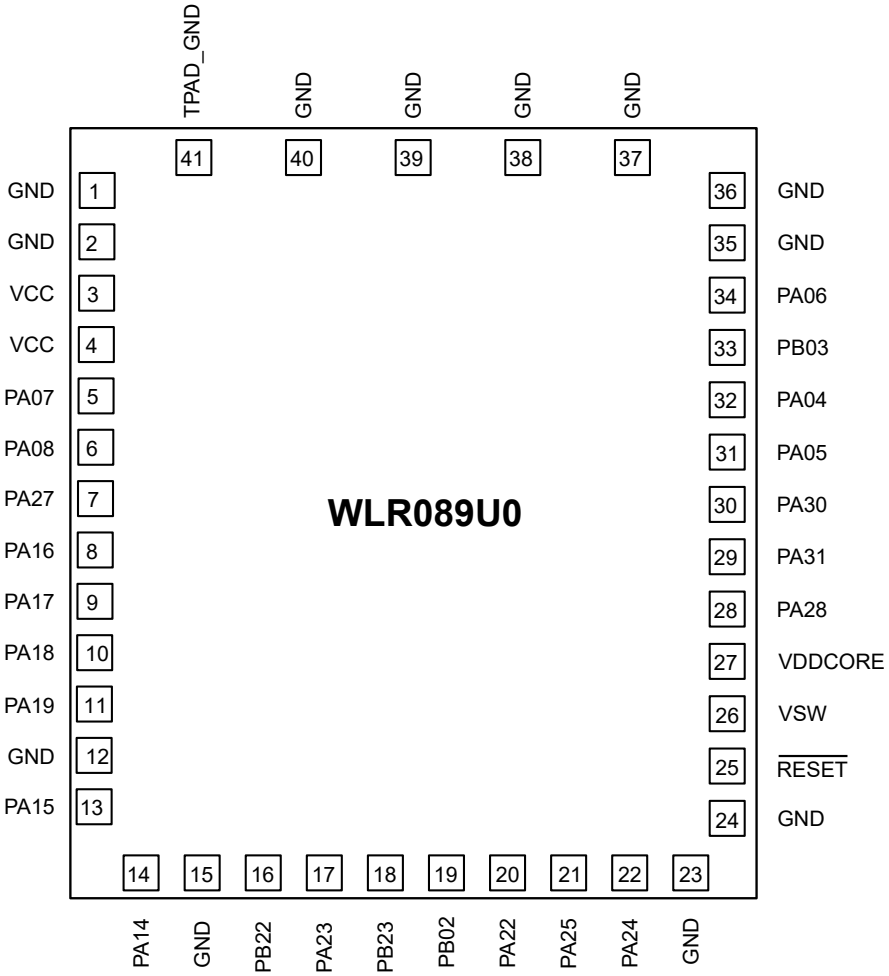
The Flash program memory can be reprogrammed through the Serial Wire Debug (SWD) interface. The same interface can also be used for non-intrusive, on-chip debugging of application code.

The ATSAMR34J18B device is supported with a full suite of programs and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

3.2 Pinout Diagram

The WLR089U0 module pinout diagram is shown in the following figure.

Figure 3-2. WLR089U0 Module Pinout Diagram



The following table describes the module pin assignment and descriptions. The ATSAMR34J18B pin numbers are added here for reference. For more details on the SiP pin descriptions, refer to *SAM R34/R35 Low Power LoRa Sub-GHz SiP Datasheet (DS70005356)*.

Table 3-1. WLR089U0 Module Pinout Assignment

WLR089U0 Module			ATSAMR34J18B SiP	
Pin No.	**Pin Name**	**Possible Peripheral Function(1)**	**SiP Pin No.**	**Pin Function**
1	GND	—	B5, B7, D4, D6, B3, E2, A2, B2, E1, F2, G2, G3, G5, G6, G7 and H5	Ground
2				
3	VCC	—	A7, A8, G4 and H8	VDDIN, VDDIO2, VDDIO1 and VBAT_DIG, respectively
4				

.....continued

WLR089U0 Module			ATSAMR34J18B SiP	
Pin No.	Pin Name	Possible Peripheral Function(1)	SiP Pin No.	Pin Function
5	PA07	ADC_AIN[7]	F3	EIC_EXTINT[7], RSTC_EXTWAKE[7], ADC_AIN[7], AC_AIN[3], SERCOM0/PAD[3], TCC1/WO[1], CCL0/OUT[0]
6	PA08	GPIO	F4	EIC_NMI, ADC_AIN[16], PTC_X[0], PTC_Y[6], SERCOM0/PAD[0], SERCOM2/PAD[0], TCC0/WO[0], TCC1/WO[2], CCL1/IN[3]
7	PA27	GPIO	E4	EIC_EXTINT[15], GCLK_IO[0]
8	PA16	SERCOM1_I2C_SDA	F7	EIC_EXTINT[0], PTC_X[4], SERCOM1/PAD[0], SERCOM3/PAD[0], TCC2/WO[0], TCC0/WO[6], GCLK_IO[2], CCL0/IN[0]
9	PA17	SERCOM1_I2C_SCL	E6	EIC_EXTINT[1], PTC_X[5], SERCOM1/PAD[1], SERCOM3/PAD[1], TCC2/WO[1], TCC0/WO[1], GCLK_IO[3], CCL0/IN[1]
10	PA18	PWM_T0_W2	E7	EIC_EXTINT[2], PTC_X[6], SERCOM1/PAD[2], SERCOM3/PAD[2], TC4/WO[0], TCC0/WO[2], AC/CMP[0], CCL0/ IN[2]
11	PA19	PWM_T0_W3	E8	EIC_EXTINT[3], PTC_X[7], SERCOM1/PAD[3], SERCOM3/PAD[3], TC4/WO[1], TCC0/WO[3], AC/CMP[1], CCL0/OUT[0]
12	GND	—	B5, B7, D4, D6, B3, E2, A2, B2, E1, F2, G2, G3, G5, G6, G7 and H5	Ground
13	PA15	GPIO	G8	EIC_EXTINT[15], SERCOM2/PAD[3], TC4/WO[1], TCC0/WO[5], GCLK_IO[1]
14	PA14	GPIO	F8	EIC_EXTINT[14], SERCOM2/PAD[2], TC4/WO[0], TCC0/WO[4], GCLK_IO[0]
15	GND	—	B5, B7, D4, D6, B3, E2, A2, B2, E1, F2, G2, G3, G5, G6, G7 and H5	Ground
16	PB22	SERCOM5_SPI_MOSI	E5	EIC_EXTINT[6], SERCOM5/PAD[2], TC3/WO[0], GCLK_IO[0], CCL0/IN[0]
17	PA23	SERCOM5_SPI_Serial_Select	D7	EIC_EXTINT[7], PTC_X[11], SERCOM3/PAD[1], SERCOM5/PAD[1], TC0/WO[1], TCC0/WO[5], USB/SOF 1kHz[6], GCLK_IO[7], CCL2/IN[1]
18	PB23	SERCOM5_SPI_CLK	C7	EIC_EXTINT[7], SERCOM5/PAD[3], TC3/WO[1], GCLK_IO[1], CCL0/OUT[0]

.....continued

WLR089U0 Module			ATSAMR34J18B SiP	
Pin No.	Pin Name	Possible Peripheral Function[1]	SiP Pin No.	Pin Function
19	PB02	SERCOM5_SPI_MISO	B4	EIC_EXTINT[2], ADC_AIN[10], SERCOM5/PAD[0], TC2/WO[0], SUPC/OUT[1], CCL0/OUT[0]
20	PA22	GPIO	D8	EIC_EXTINT[6], PTC_X[10], SERCOM3/PAD[0], SERCOM5/PAD[0], TC0/WO[0], TCC0/WO[4], GCLK_IO[6], CCL2/IN[0]
21	PA25	USB_DP[6]	C8	EIC_EXTINT[13], SERCOM3/PAD[3], SERCOM5/PAD[3], TC1/WO[1], TCC1/WO[3], USB/DP[6], CCL2/OUT[2]
22	PA24	USB_DM[6]	B8	EIC_EXTINT[12], SERCOM3/PAD[2], SERCOM5/PAD[2], TC1/WO[0], TCC1/WO[2], USB/DM[6], CCL2/IN[2]
23	GND	—	B5, B7, D4, D6, B3, E2, A2, B2, E1, F2, G2, G3, G5, G6, G7 and H5	Ground
24	GND	—		Ground
25	RESET	RESET_N	B6	RESET
26	VSW	VSW	A6	VSW
27	VDDCORE	VDDCORE	A5	VDDCORE
28	PA28	GPIO	C6	EIC_EXTINT[8], GCLK_IO[0]
29	PA31	SWDIO[2]	D5	EIC_EXTINT[11], SERCOM1/PAD[3], TCC1/WO[1], SWDIO[2], CCL1/OUT[1]
30	PA30	SWDCLK[2]	C5	EIC_EXTINT[10], SERCOM1/PAD[2], TCC1/WO[0], SWCLK[2], GCLK_IO[0], CCL1/IN[0]
31	PA05	SERCOM0_UART_RX	C4	EIC_EXTINT[5], RSTC_EXTWAKE[5], ADC_AIN[5], AC_AIN[1], SERCOM0/PAD[1], TCC0/WO[1], CCL0/IN[1]
32	PA04	SERCOM0_UART_TX	D3	EIC_EXTINT[4], RSTC_EXTWAKE[4], VREFB, ADC_AIN[4], AC_AIN[0], SERCOM0/PAD[0], TCC0/WO[0], CCL0/IN[0]
33	PB03	SUPC_VBAT	C3	EIC_EXTINT[3], ADC_AIN[11], SERCOM5/PAD[1], TC2/WO[1], SUPC/VBAT
34	PA06	PTC_Y4	E3	EIC_EXTINT[6], RSTC_EXTWAKE[6], ADC_AIN[6], AC_AIN[2], PTC_Y[4], SERCOM0/PAD[2], TCC1/WO[0], CCL0/IN[2]

.....continued				
WLR089U0 Module			**ATSAMR34J18B SiP**	
Pin No.	**Pin Name**	**Possible Peripheral Function(1)**	**SiP Pin No.**	**Pin Function**
35	GND	—	B5, B7, D4, D6, B3, E2, A2, B2, E1, F2, G2, G3, G5, G6, G7 and H5	Ground
36	GND	—		Ground
37	GND	—		Ground
38	GND	—		Ground
39	GND	—		Ground
40	GND	—		Ground
41	TPAD_GND	—		Thermal Pad Ground

Notes:

1. The peripheral function indicated in this column is based on the reference design. This is one of the possibilities as each WLR089U0 pin supports several multiplexed peripheral functions mentioned in the pin function column.
2. This function is only activated in the presence of a debugger.

3.3 Package Details

The following table provides the WLR089U0 module package details.

Table 3-2. WLR089U0 Package Information

Parameter	Value	Units
Package size	17x13.5	mm
Pad count	41	—
Total thickness	2.8	mm
Pad pitch	1	mm
Pad width	0.7	mm

Note: For more information on the package dimensions, refer to 10.2 Module Outline Drawings.

2.5V AND 3V 8M-BIT SERIAL FLASH MEMORY WITH DUAL AND QUAD SPI

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1. GENERAL DESCRIPTION

The W25Q80DV/DL (8M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The W25Q80DV operates on a single 2.7V to 3.6V and the W25Q80DL operateds on a single 2.3V to 3.6V power supply with current consumption as low as 1µA for power-down.

The W25Q80DV/DL array is organized into 4,096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q80DV/DL has 256 erasable sectors and 16 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q80DV supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. A Hold pin, Write Protect pin and programmable write protection, with top, bottom or complement array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of SpiFlash Memories**
  - W25Q80DV/DL: 8M-bit/1M-byte (1,048,576)
  - 256-byte per programmable page
  - Standard SPI: CLK,/CS,DI,DO,/WP,/Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Uniform 4KB Sectors, 32KB & 64KB Blocks
- **Highest Performance Serial Flash**
  - W25Q80DV
    104MHz Dual/Quad SPI clocks
    208/416MHz equivalent Dual/Quad SPI
    50MB/S continuous data transfer rate
  - W25Q80DL
    80MHz Dual/Quad SPI clocks
    160/320MHz equivalent Dual/Quad SPI
    40MB/S continuous data transfer rate
- **Software and Hardware Write Protection**
  - Write-Protect all or portion of memory
  - Enable/Disable protection with /WP pin
  - Top or bottom array protection
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4/32/64-kbytes)
  - Erase/Program Suspend & Resume
  - More than 100,000 erase/write cycles
  - More than 20-year data retention
- **Low Power, Wide Temperature Range**
  - W25Q80DV: Single 2.7 to 3.6V supply
  - W25Q80DL: Single 2.3 to 3.6V supply
  - <1µA Power-down(typ.)
- **Advanced Security & Identification Features**
  - Software and Hardware Write-Protect
  - Top/Bottom, 4KB complement array protection
  - Power Supply Lock-Down and OTP protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Byte Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging(1):**
  - 8-pin SOIC 150-mil/208mil, VSOP 150-mil
  - 8-pad WSON 6x5-mm, USON 2x3-mm
  - 8-pin PDIP 300-mil
  - 8-ball WLCSP
  - Contact Winbond for KGD and other options

Note 1. Some package types are special orders, please contact Winbond for ordering information.

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Configuration SOIC 150-MIL/208-mil AND VSOP 150-mil:

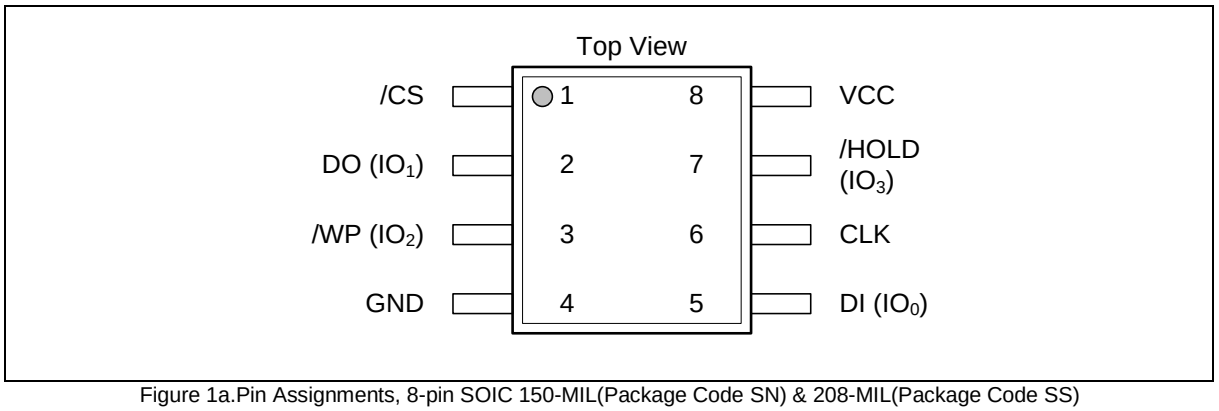


Figure 1a.Pin Assignments, 8-pin SOIC 150-MIL(Package Code SN) & 208-MIL(Package Code SS) & VSOP 150-mil (Package Code SV)

3.2 Pad Configuration WSON 6x5-mm, USON 2X3-mm

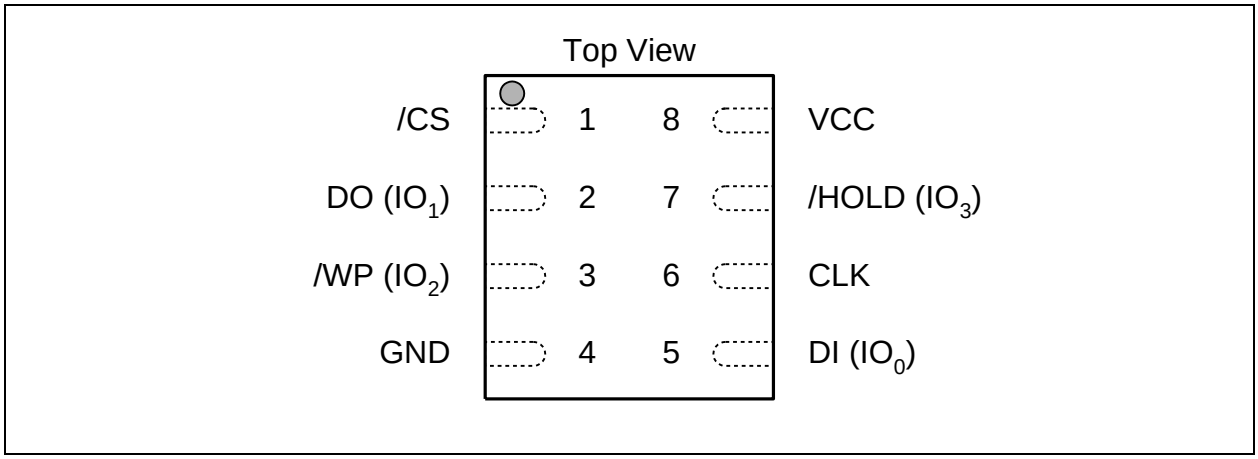


Figure 1b.Pad Assignments, 8-pad WSON 6x5-mm, USON 2x3-mm (Package Code ZP & UX)

3.3 Pin Configuration PDIP 300-mil

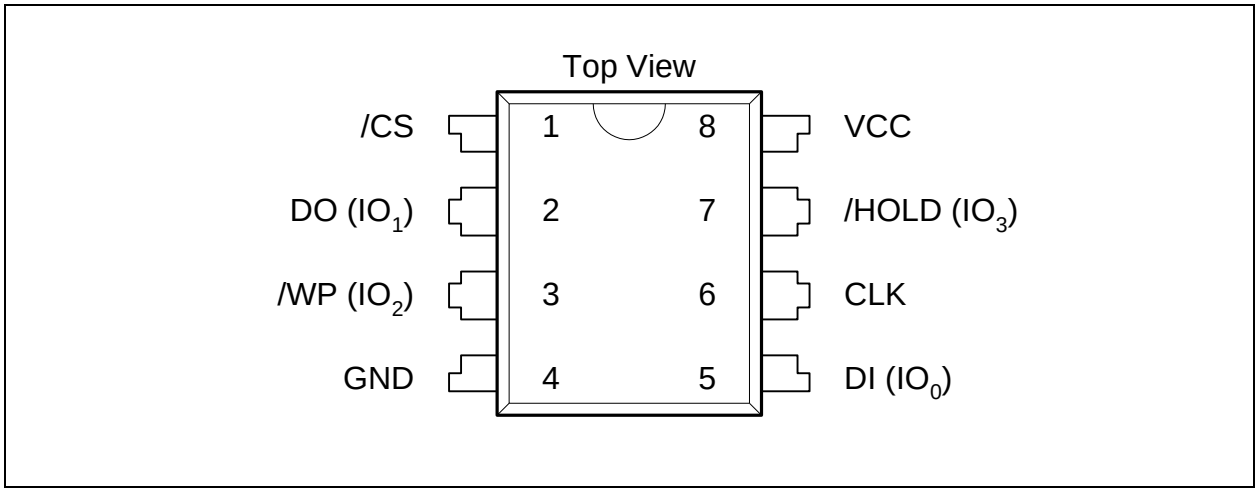


Figure 1c.Pin Assignments, 8-pin PDIP (Package Code DA)

3.4 Pin Description SOIC/VSOP , WSON/USON & PDIP 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
8	VCC		Power Supply

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

3.5 Ball Configuration WLCSP

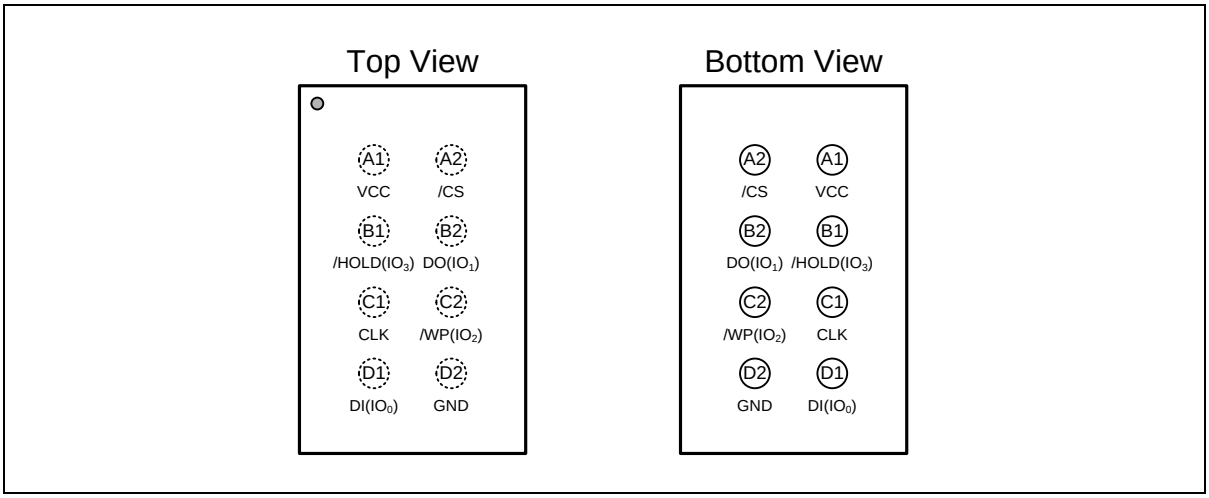


Figure 1d.Ball Assignments, 8-ball WLCSP (Package Code BY)

3.6 Ball Description WLCSP

BALL NO.	PIN NAME	I/O	FUNCTION
A1	VCC		Power Supply
A2	/CS	I	Chip Select Input
B1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
B2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
C1	CLK	I	Serial Clock Input
C2	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
D1	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
D2	GND		Ground

*1 IO0 and IO1 are used for Standard and Dual SPI instructions
*2 IO0 – IO3 are used for Quad SPI instructions

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see "Power-up Timing and Write inhibit threshold" and figure 45). If needed, a pull-up resister on /CS can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q80DV/DL support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register 2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP0) bits, a portion as small as 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See figure 1a and 1b for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

5. BLOCK DIAGRAM

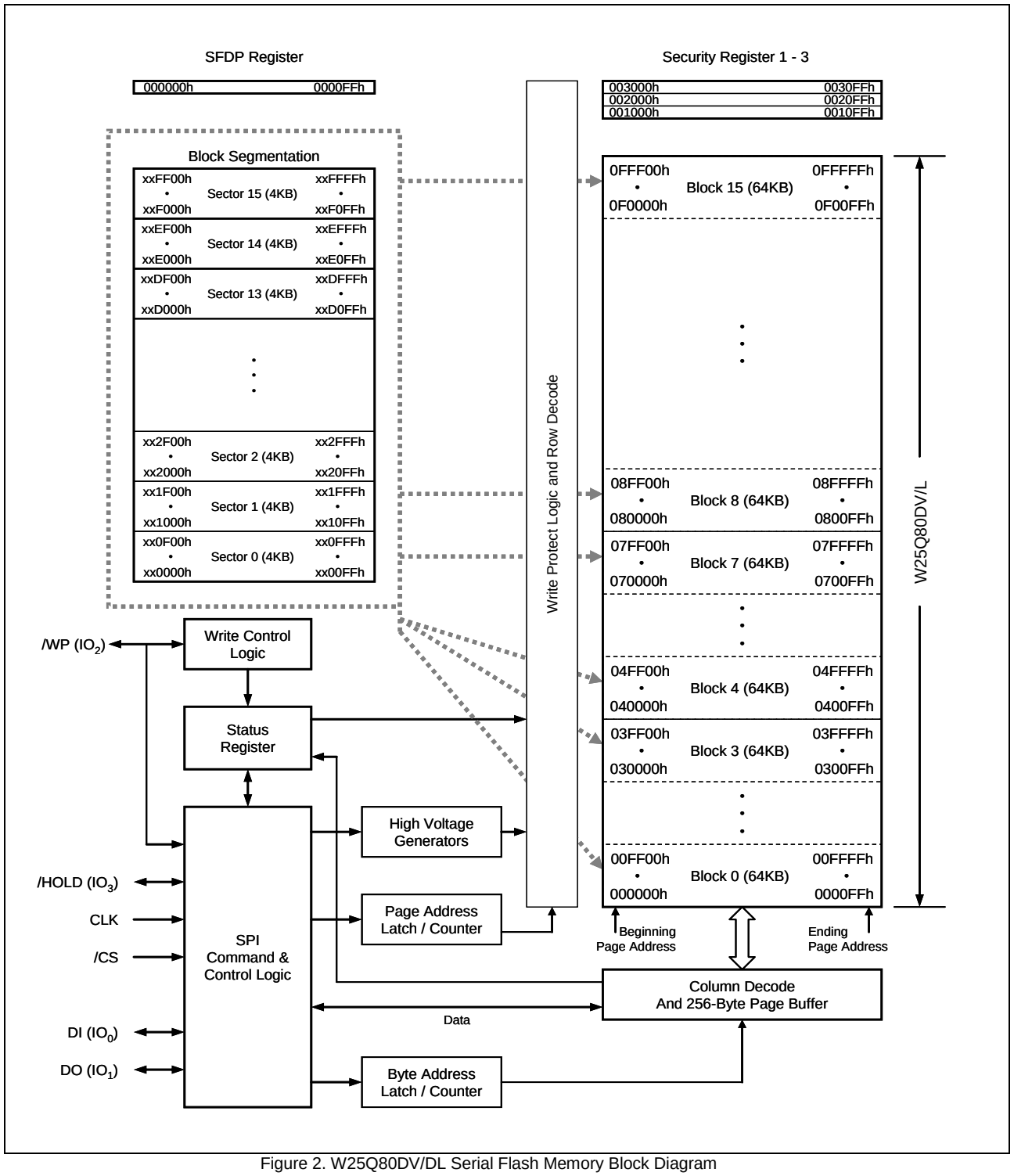


Figure 2. W25Q80DV/DL Serial Flash Memory Block Diagram

Si720x Switch/Latch Hall Effect Magnetic Position Sensor Data Sheet

The Si7201/2/3/4/5/6 family of Hall effect magnetic sensors switches and latches from Silicon Labs combines a chopper-stabilized Hall element with a low-noise analog amplifier, 13-bit analog-to-digital converter, and a flexible comparator circuit. Leveraging Silicon Labs' proven CMOS design techniques, the Si720x family incorporates digital signal processing to provide precise compensation for temperature and offset drift.

Compared with existing Hall effect sensors, the Si720x family offers industry-leading sensitivity, which enables use with larger air gaps and smaller magnets. For battery-powered applications, the Si720x family offers very low power consumption to improve operating life.

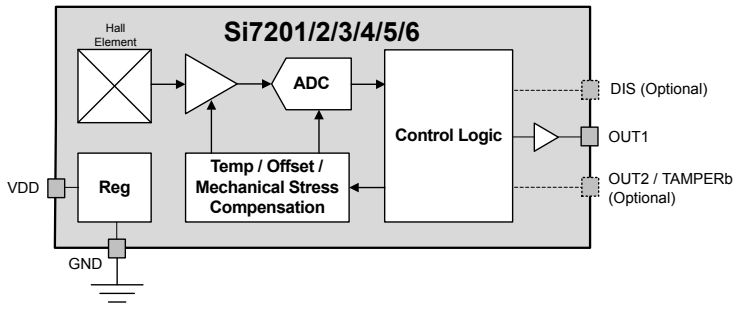
The Si720x devices are offered in 3-pin SOT23, 5-pin SOT23, and TO-92 packages, with power, ground, a single output pin that goes high or low as the magnetic field increases, and with the 5-pin parts a disable(sleep) pin, and a tamper output pin. With the three-pin package, tamper indication is by the pin going back to its zero field level at high magnetic field.

Applications:

- Replacement of reed switches in consumer, and security applications
- Position sensing of HVAC knob, door locks, windows, and other mechanical devices
- BLDC motor control
- Camera image stabilization, zoom, and autofocus
- Fluid level sensing
- Control knobs and selector switches
- General-purpose mechanical position sensing

FEATURES

- High-Sensitivity Hall Effect Sensor
  - Maximum B_{OP} operating point/minimum field strength of <1.1 mT
  - Omnipolar or unipolar operation
  - Integrated digital signal processing for temperature and offset drift compensation
- Low 400 nA Typical Current Consumption at 5 samples per second
- Selectable Sensitivity, Hysteresis, Output Polarity and Sample Rate
- Sensitivity Drift < ±3% over Temperature
- Wide Power Supply Voltage
  - 1.71 to 5.5 V
  - 3.3 to 26.5 V
- Selectable Output Options
  - Open-drain output
  - Digital high/low output
- Industry-Standard Packaging
  - Surface mount SOT-23 (3 or 5 pin)
  - Through hole TO-92 (3-pin)
  - 1.4 x 1.6 mm 8-pin DFN package (coming soon)



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1. Electrical Specifications

Unless otherwise specified, all min/max specifications apply over the recommended operating conditions.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply	V_{DD}	Si7201/2/3/4	1.71		5.5[1]	V
Power Supply	V_{DD}	Si7205/6	3.3		26.5	V
Temperature	T_A	I grade	-40		+125[2]	°C

Note:
1. 3.6 V for most sensitive parts (see Chapter 5. Ordering Guide).
2. 0-70°C for most sensitive parts (F grade) (see Chapter 5. Ordering Guide).

Table 1.2. General Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage High	V_{IH}	DIS pin	0.7 x V_{DD}	-	-	V
Input Voltage Low	V_{IL}	DIS pin	-	-	0.3 x V_{DD}	V
Input voltage Range	V_{IN}	DIS pin	0		V_{DD}	V
Input Leakage	I_{IL}	DIS pin			1	µA
Output Voltage Low	V_{OL}	TAMPERb pin I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		TAMPERb pin I_{OL} = 2 mA V_{DD} > 1.71 V			0.2	V
		TAMPERb pin I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Output Voltage High	V_{OH}	TAMPERb pin I_{OH} = 2 mA V_{DD} > 2.25 V	V_{DD} – 0.4			V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current Consumption Average power depends on the sample rate and percent of time spent sampling versus sleep mode or idle mode. See the ordering guide for average power calculations for specific devices.	I_{DD}	Sleep timer enabled average at V_{DD} = 3.3 V and 200 msec sleep time		0.4		µA
		Sleep mode V_{DD} = 3.3 V, T = 25 °C V_{DD} = 3.3 V, T = 70 °C V_{DD} = 5.5 V, T = 125 °C		50	 1000 5000	 nA nA nA
		Conversion in progress V_{DD} = 1.8V V_{DD} = 3.3 V V_{DD} = 5.5 V		 3.5 5 6.8	 5.5 6 8.0	mA
		Conversion in progress high voltage parts V_{DD} = 3.3 to 26.5 V		6.5	8.5	mA
		Idle mode low voltage parts V_{DD} = 1.71 to 5.5 V		0.6	1	mA
		Idle mode high voltage parts V_{DD} = 3.3 to 26.5 V		0.9	1.2	mA
Conversion Time	T_{CONV}	First conversion when waking from sleep or idle		11		µs
		Additional conversions in a burst		8.8		µs
Sample Rate	F_{SAMPLE}	Parts can be configured for sleep or idle between samples. Sleep is lower power, but the fastest sampling rate is 8 kHz. Idle allows sampling rate to be configured to be as high as 113 kHz. See the ordering guide for details.		-		
Wake Up Time	T_{WAKE}	Time from V_{DD} > 1.71 V to first measurement			1	msec

Note:

1. TAMPERb and DIS pin specifications apply when the pin is present (Si7203/4).
2. Idle time can be factory programmed from 13.2 µsec to 206 msec ±10% or set to zero in which case conversions are done every 8.8 µsec. Normally idle time is only used at higher sample speeds.
3. For high voltage parts (V_{DD} = 26.5 V maximum), the power on ramp should be faster than 10 V per second in the start-up region from 2 to 3 V.

Table 1.3. Output Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si7201/2/3/4						
Output Voltage Low Open Drain or Push Pull	V_{OL}	I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		I_{OL} = 2 mA V_{DD} > 1.71V			0.2	V
		I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Output Voltage High Output Pin Push Pull	V_{OH}	I_{OH} = 2 mA V_{DD} > 2.25 V	V_{DD} – 0.4			V
Slew Rate	T_{SLEW}			5		$\%V_{DD}$/ns
Si7205/6						
Output Voltage Low	V_{OL}	I_{OL} = 11.4 mA V_{DD} > 6 V			0.4	V
Safe Continuous Sink Current					20	mA
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Slew Rate Digital Output Mode	T_{SLEW}			5		$\%V_{DD}$/ns
Output Pin Shorted to V_{DD}	I_{SHORT}	V_{DD} = 12 V Average current as pin cycles		4		mA

The Si7205 and Si7206 can be configured to signal the status equivalent to output high or low by modulating the power supply current. If configured in this way, the following are the specifications for the amount of current that will be drawn for the “output high” state.

Table 1.4. I_{DD} Signaling

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I_{DD} Signaling Current	I_{DO}	V_{DDH} > 6 V	8	10	12	mA

Table 1.5. Magnetic Sensor[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	B_{OFF}	20 mT scale V_{DD} = 1.71 to 3.6 V 0-70°C		±150	±250	µT
		20 mT scale V_{DD} = 1.71 to 5.5 V Full temperature range		±250	+450, -350	µT
Gain Accuracy		0-70°C			5	%
		Full temperature range			10	%
RMS Noise[2]		Room temp, 20 mT range, V_{DD} = 5 V		30		µT rms

Note:

1. See the Magnetic Sensors Selector Guide for operating release points. These are defined as maximum operating point and minimum release point over the operating temperature range and do not include the effect of noise.
2. For a single conversion. This can be reduced by the square root of N by filtering over N samples. See ordering guide for samples taken per measurement.

Table 1.6. Temperature Compensation

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bop and Brp vs Temperature		Flat Tempco. 0-70°C		< ±0.05		%/°C
		Neodymium compensation		-0.12		%/°C
		Ceramic compensation		-0.2		%/°C

Table 1.7. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-5	212.8	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-5	45	°C/W
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-3	254.6	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-3	54.8	°C/W

Table 1.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature Under Bias			-55		125	°C
Storage Temperature			-65		150	°C
Si7201/2/3/4						
Voltage on I/O Pins			-0.3		V_{DD}+0.3	V
Voltage on V_{DD} with Respect to Ground			-0.3		6	V
ESD Tolerance		HBM			2	kV
		CDM			500	V
Si7205/6						
Voltage on Ouput pin[2]			-21		40	V
Voltage on V_{DD} with Respect to Ground[3]			-21		40	V
ESD Tolerance		HBM			8	kV
		CDM			500	V

Notes:

1. Absolute maximum ratings are stress ratings only, operation at or beyond these conditions is not implied and may shorten the life of the device or alter its performance.
2. The output pin can withstand EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω to a local bypass cap of 0.1 µF and additional 22 Ω between the capacitor and ground..
3. V_{DD} can withstand automotive EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω.

2. Functional Description

The Si7201/2/3/4/5/6 family of Hall Effect magnetic sensors digitize the component of the magnetic field in the z axis of the device (positive field is defined as pointing into the device from the bottom). The digitized field is compared to a pre-programmed threshold and the output pin goes high or low if the threshold is crossed. The parts are normally used to detect the presence or absence of a magnet in security systems, as position sensors or for counting revolutions.

Table 2.1. Part Ordering Guide

Part Number	Description
Si7201	Low voltage switches
Si7202	Low voltage latches
Si7203	Low voltage switch with tamper and/or disable pins
Si7204	Low voltage latches with tamper and/or disable pins
Si7205	High voltage switches
Si7206	High voltage latches

The output pin (push pull or open collector) can go high or low when the magnetic field crosses a threshold. The output pin configuration is determined by the type of part ordered.

The parts are preconfigured for the magnetic field measurement range, magnetic field operate and release points, sleep time, temperature compensation, tamper threshold and digital filtering and will wake into this mode when first powered. The specific configuration output type (open collector or push pull) are determined by the part number. See Magnetic Sensors Selector Guide for details.

Examples:

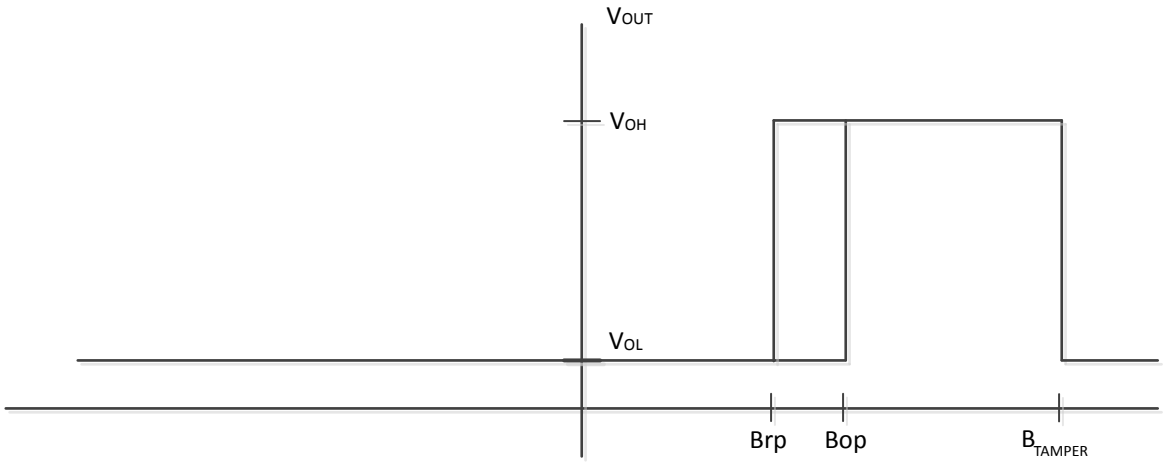

Figure 2.1. Unipolar Switch with Tamper

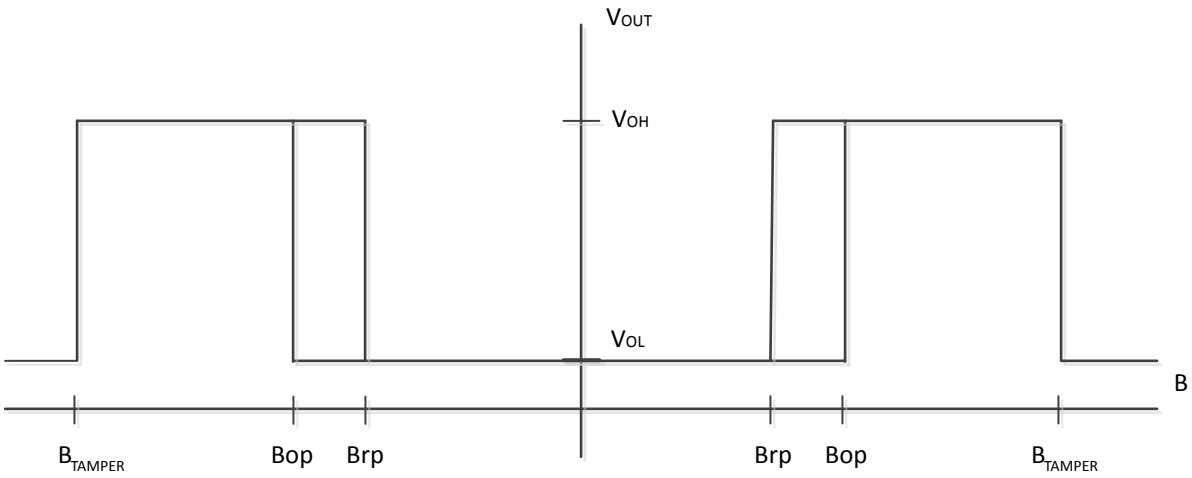

Figure 2.2. Omnipolar Swith with Tamper

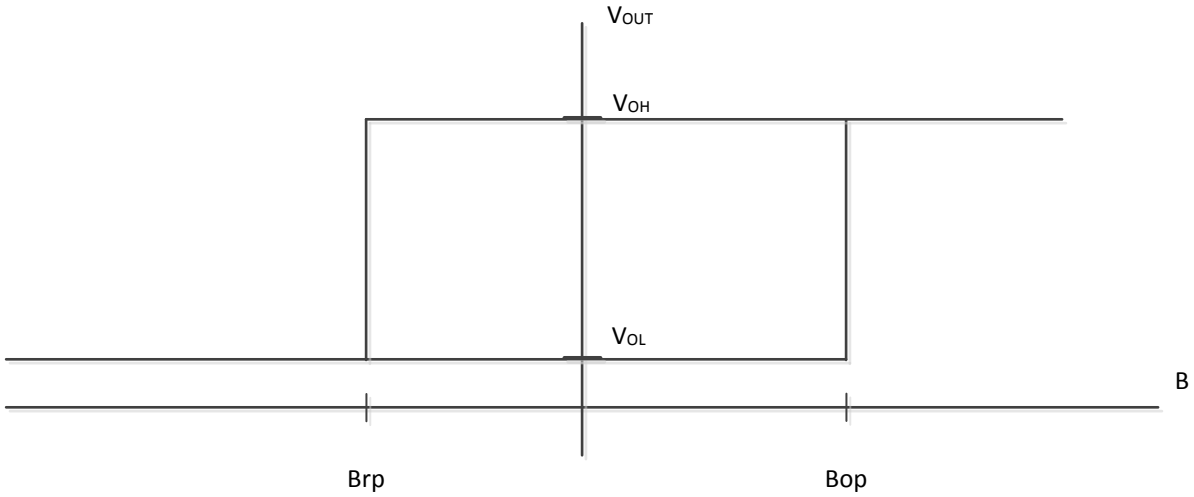

Figure 2.3. Latch

4. Pin Description

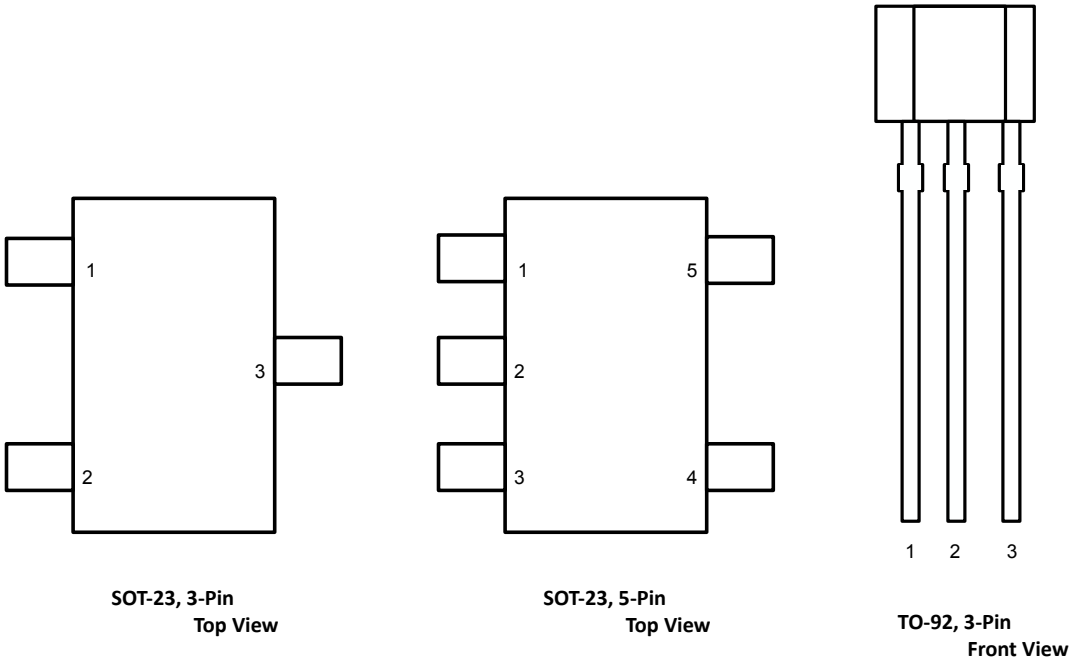

Figure 4.1. Si720xxx Pin Assignments

Note:

The 3-pin option includes part numbers: Si7201/2/5/6.

The SOT-23 5 pin option include part numbers: Si7203/4.

Table 4.1. Si7201/2/5/6 (SOT23 3-pin Package)

Pin Name	Pin Number	Description
VDD	1	Power 1.71 to 5.5 V or 3.3 to 26.5 V
OUT1	2	Switch/latch output
GND	3	Ground

Table 4.2. Si7203/4/5 (SOT23 5-pin Package Excluding Si7203-B-01-IV(R))

Pin Name	Pin Number	Description
OUT2/TAMPERb	1	OUT2/TAMPERb (tamper/high field indicator)
GND	2	Ground
DIS	3	Disables part (puts into sleep mode) when high. Measurement cycle will resume when pin goes low
VDD	4	Power 1.71 to 5.5 V
OUT1	5	Switch/latch output

Table 4.3. Si7203-B-01-IV(R) (SOT23 5-pin Package)

Pin Name	Pin Number	Description
TAMPER	1	TAMPER (tamper)
GND	2	Ground
FLOAT	3	Must be left floating for correct operation of the device
VDD	4	Power 1.71 to 5.5 V
OUT1	5	Switch output

Table 4.4. Si7201/2/5/6 (TO-92 Package)

Pin Name	Pin Number	Description
VDD	1	Power
GND	2	Ground
OUT1	3	Output

5. Ordering Guide

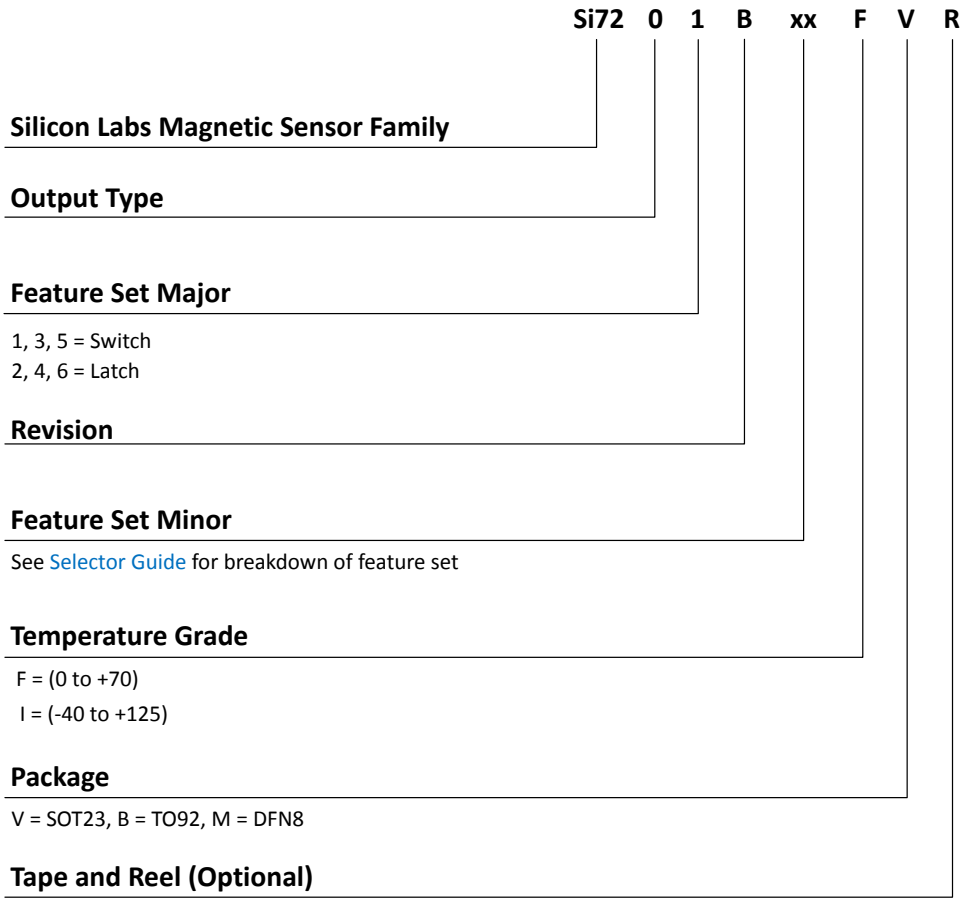

Figure 5.1. Si720x Part Numbering

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PLEASE CHECK WWW.MOLEX.COM FOR LATEST PART INFORMATION

Part Number: 2067640100

Status: Active

Overview: Industrial, Scientific and Medical (ISM) Antennas

Description: ISM 868/915MHz Dipole Flexible Antenna, 100.00mm Cable Length, Compatible with U.FL / I-PEX MHF Connectors

Series image - Reference only

Documents:

- 3D Model
- 3D Model (PDF)
- Drawing (PDF)
- Product Specification 2067640100-PS (PDF)
- Application Specification 2067640100-AS (PDF)
- Packaging Specification 2067640100-PK (PDF)
- Datasheet (PDF)
- RoHS Certificate of Compliance (PDF)

General

Product Family	Antennas
Series	206764
Component Type	Flexible Antenna with Cable
Function	Signal
Overview	Industrial, Scientific and Medical (ISM) Antennas
Product Name	ISM 868/915 MHz Stand Alone
Protocol	LoRa, Neul, SigFox, Z-Wave, Zigbee
Taxonomy	Antennas
Type	ISM Antenna, LPWAN
UPC	191128789165

Physical

Cable Length	100.00mm
Length	87.40mm
Mounting Style	Adhesive
Net Weight	0.872/g
Packaging Type	PET Film
Polarization	Linear
Radiation Pattern	Omnidirectional
Thickness	0.10mm
Width	12.40mm

Electrical

Band#1 F_End (MHz)	870
Band#1 F_Start (MHz)	863
Band#2 F_End (MHz)	928
Band#2 F_Start (MHz)	902
Electrical Connectivity	Cable
Peak Gain (dBi)	1.2 @ 868/915 MHz
Return Loss - S11 (dB)	< -9
Total Efficiency	>70% @ 868/915 MHz

Material Info

Reference - Drawing Numbers

Application Specification	2067640100-AS
Packaging Specification	2067640100-PK
Product Specification	2067640100-PS
Sales Drawing	2067640100-SD

EU ELV
Not Relevant

EU RoHS
Compliant

China RoHS

REACH SVHC
Not Contained Per - D(2022)4187-DC (10 June 2022)

Halogen-Free Status
Low-Halogen

For more information, please visit Contact US

China ROHS	Green Image
ELV	Not Relevant
RoHS Phthalates	Not Contained

Search Parts in this Series
206764 Series

Mates With
734120110 Microcoaxial RF, 50 Ohm

This document was generated on 10/28/2022

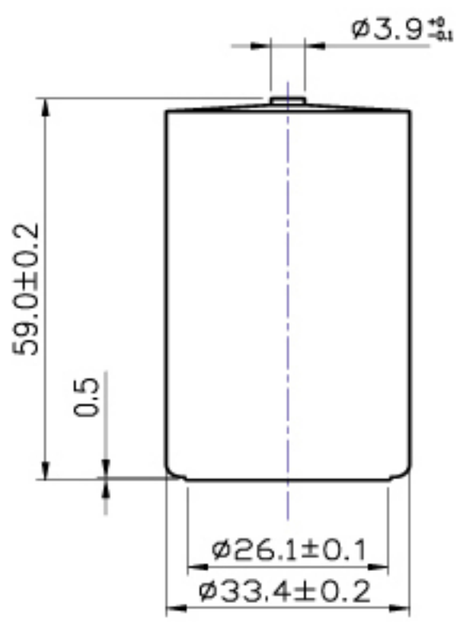
PLEASE CHECK WWW.MOLEX.COM FOR LATEST PART INFORMATION

SPECIFICATIONS

(Typical values for batteries stored at 20℃ for one year)

Nominal Capacity (At 5mA/20℃/68°F/2.0V Cut-Off)	19 Ah
Open Circuit Voltage (At 20℃/68°F)	3.67 V
Nominal Voltage (At 5mA/20℃/68°F)	3.6 V
Maximum Continuous Current	230 mA
Maximum Pulse Current Capability	500 mA
Operating Temperature Range	-55 ~ 85 ℃
Weight	97 g (3.42 oz)
Anode Surface Area	40 ㎠
Volume	51 ㎤
Diameter (Max)	33.6 mm
Height (Max)	60 mm

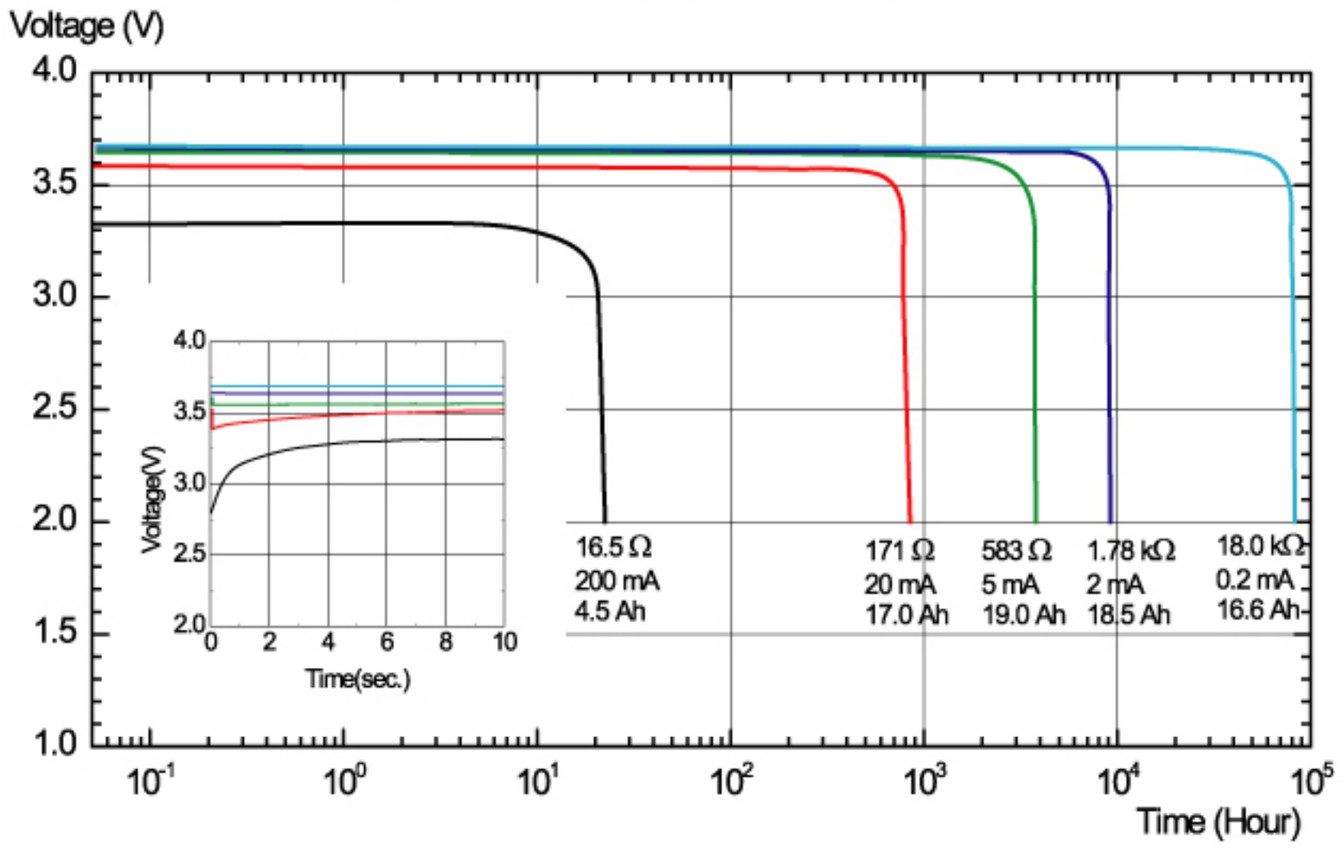
DIMENSIONS IN MM



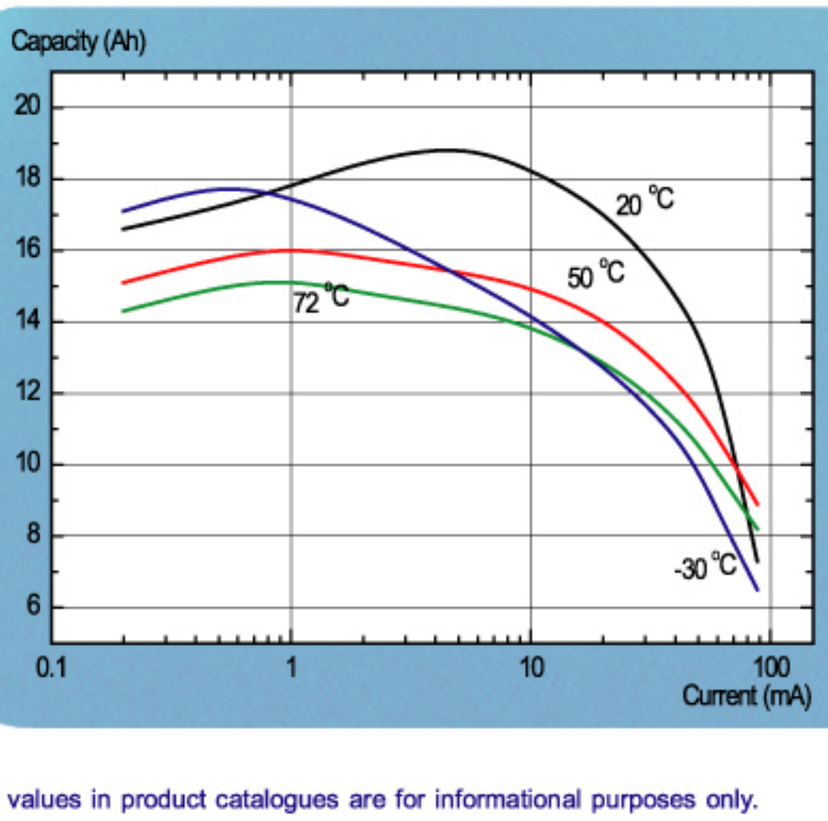
WARNING

Fire, Explosion And Severe Burn Hazard.
Do Not Recharge, Crush, Disassemble,
Heat Above 212°F(100℃), Incinerate
Or Expose Contents To Water

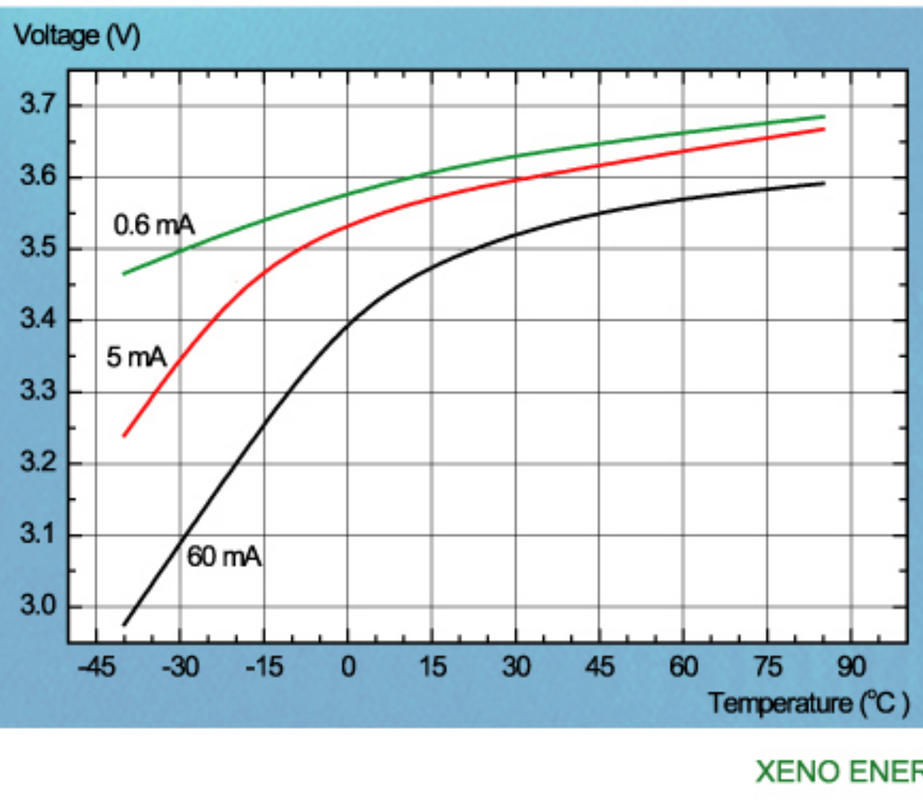
DISCHARGE CHARACTERISTICS AT +20°C



CAPACITY vs. CURRENT



OPERATING VOLTAGE



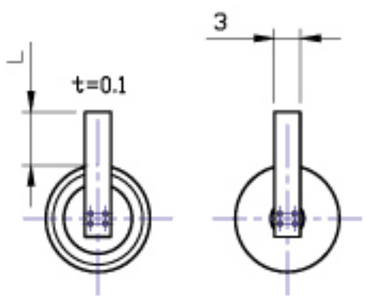
Any values in product catalogues are for informational purposes only.

They can also differ from actual conditions of usage and are not warranties of future performance.

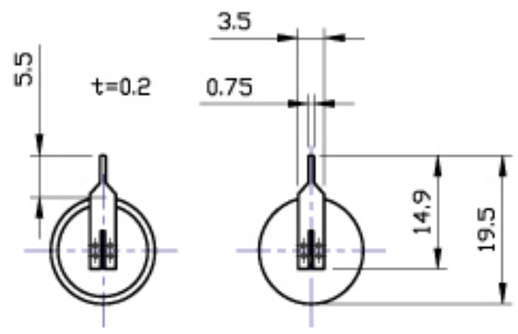
XenoEnergy Lithium Battery

Terminals

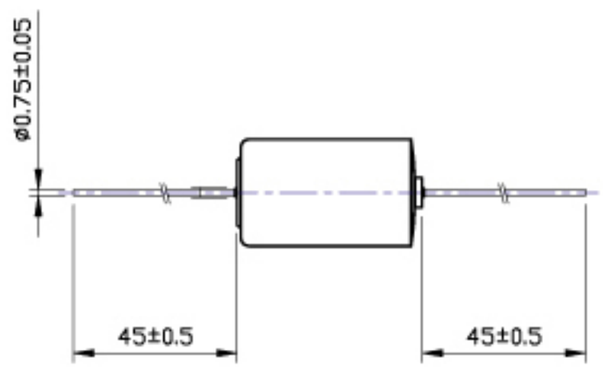
(Unit : mm)



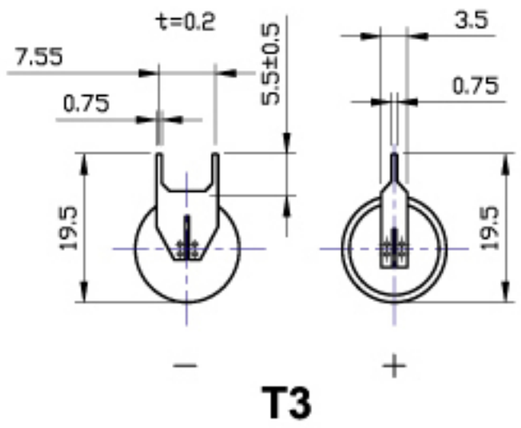
T1



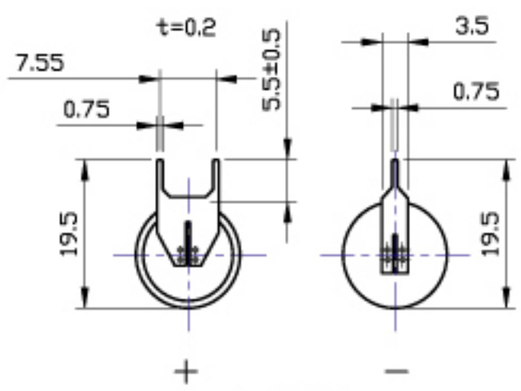
T2



AX

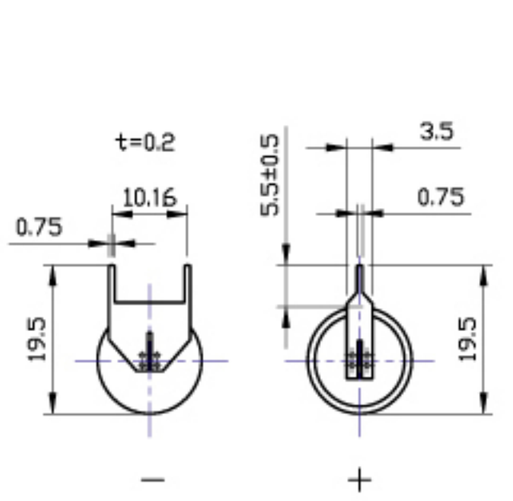


T3

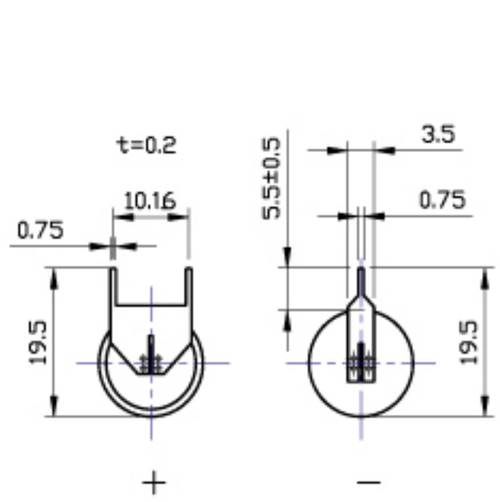


T3/R

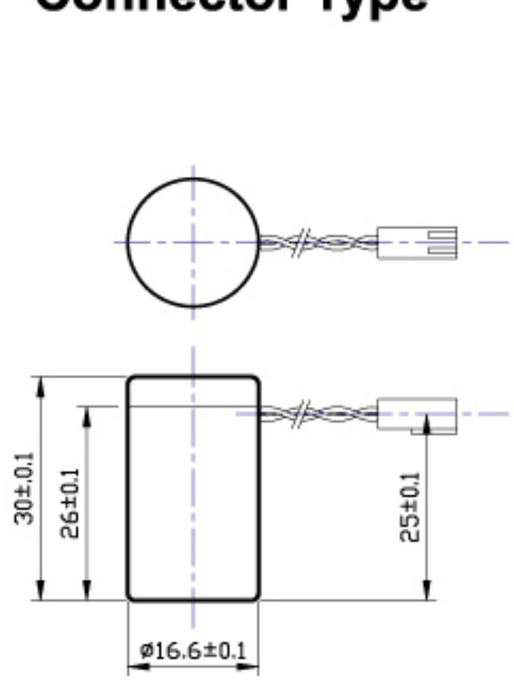
Connector Type



T3EU



T3EU/R



Case Type

Model	T1/L(mm)	T2	T3 & T3/R	T3EU & T3EU/R	AX	Connector Type	Case Type
XL-050F	○/(7±0.5)	○	○	○	○	○	○
XL-050H	○/(7±0.5)	○	○	○	○	○	○
XL-055F	○/(7±0.5)	○	○	○	○	○	
XL-060F	○/(7±0.5)	○	○	○	○	○	
XL-060H	○/(7±0.5)	○	○	○	○	○	
XL-140F	○/(16±1)				○	○	
XL-145F	○/(16±1)				○	○	
XL-200F	○/(16±1)				○	○	
XL-205F	○/(16±1)				○	○	
XL-210F					○		