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Pablo Guillén Moya

Multi-output matrix resonant power converters for domestic induction heating

Director/es
Sarnago Andía, Héctor
Lucía Gil, Óscar

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Tesis Doctoral

MULTI-OUTPUT MATRIX RESONANT POWER CONVERTERS FOR DOMESTIC INDUCTION HEATING

Autor

Pablo Guillén Moya

Director/es
Sarnago Andía, Héctor
Lucía Gil, Óscar

UNIVERSIDAD DE ZARAGOZA
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Ph.D. Dissertation

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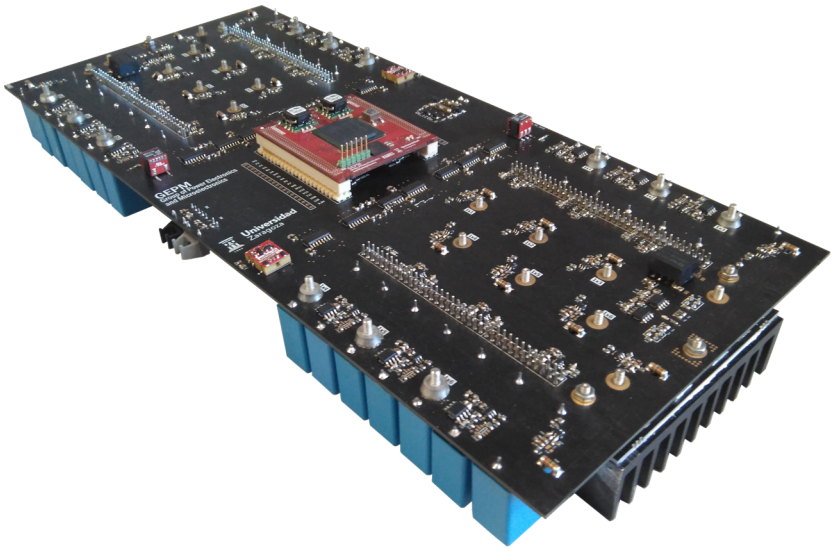

Author

Pablo Guillén Moya

Advisors

Héctor Sarnago Andía

Óscar Lucía Gil

Department of Electronic Engineering and Communications

School of Engineering and Architecture

UNIVERSIDAD DE ZARAGOZA

Zaragoza, Spain. September 2022.

A mi familia

A Clara

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Abstract

In this thesis a new family of multi-output resonant inverter topologies with matrix structure is presented. These designs are oriented to the powering of flexible-surface domestic induction systems, i.e. cooktops that present multi-inductor architectures.

In this document, the one-dimensional version of the ZVS matrix resonant converter topology is analyzed in depth. Its different operating modes and associated control strategies are presented, verifying them over several operating conditions. Multiplexation strategies, based on the alternative activation of inductors, have been designed to achieve a minimal fluctuation of the total power consumed by the equipment, and allow operation with fewer degrees of freedom. On the other hand, strategies based on the non-complementary activation of the transistors, which allow a continuous power transfer to the different loads, require the use of a greater number of degrees of freedom, but provide higher precision in the power transferred.

Considering the different operating conditions and taking into account the differential characteristics of the proposed control strategies, a series of prototypes have been designed and developed based on the single-column matrix-based ZVS resonant inverter topology. These power stages allow experimental verification of the strategies in an environment optimized in terms of flexibility and efficiency. These tests are intended to verify the suitability of the topology for the implementation of domestic induction heating systems with a high number of loads.

This PhD dissertation has been developed within the collaboration agreement between the BSH Home Appliances Group (BSH) and the Group of Power Electronics and Microelectronics (GEPM) of the Universidad de Zaragoza, Spain, in the framework of the BSH-UZ Innovation Chair.

Resumen

En esta tesis se presenta una nueva familia de topologías inversoras resonantes de salida múltiple con estructura matricial. Éstas se han orientado a la transferencia de potencia a sistemas de inducción domésticos que presentan superficies flexibles, es decir, que hacen uso de arquitecturas multi-inductor.

En este documento se analiza en profundidad la versión unidimensional de la topología ZVS. Se presentan sus diferentes modos de operación y las estrategias de control asociadas, verificándolos para distintas condiciones de operación. Las estrategias de multiplexación, basadas en la activación alternativa de inductores, se han diseñado partiendo de la minimización en la fluctuación de potencia total consumida por el equipo y permiten operar con menos grados de libertad. Por su parte, las estrategias basadas en la activación no complementaria de los transistores, que permiten la transferencia de potencia de forma continua a las distintas cargas, requieren del uso de un mayor número de grados de libertad, pero proporcionan una gran precisión en la potencia transferida.

Considerando las distintas condiciones de operación planteadas y teniendo en cuenta las características diferenciales de las estrategias de control propuestas se han implementado una serie de prototipos que presentan como base la topología matricial unidimensional ZVS. Estas etapas permiten verificar experimentalmente estas estrategias aplicadas en un entorno optimizado en términos de flexibilidad y eficiencia. Con estos ensayos se pretende comprobar la idoneidad de la topología para la implementación de sistemas de calentamiento por inducción domésticos de un elevado número de cargas.

Esta tesis ha sido desarrollada dentro del acuerdo de colaboración entre BSH Electrodomésticos España S.A. (BSH) y el Grupo de Electrónica de Potencia y Microelectrónica (GEPM) de la Universidad de Zaragoza, en el marco de la Cátedra de Innovación BSH-UZ.

List of acronyms

ADC	*Asymmetrical duty cycle*
ASIC	*Application specific integrated circuit*
AVC	*Asymmetrical voltage cancelation*
BSH	*BSH Home Appliances Group*
CSI	*Current source inverter*
EMC	*Electromagnetic compatibility*
FB	*Full bridge*
FEM	*Finite element model*
FPGA	*Field-programmable gate array*
GEPM	*Group of Power Electronics and Microelectronics*
HB	*Half bridge*
HF	*High frequency*
I3A	*Instituto de Investigación en Ingeniería de Aragón*
IGBT	*Insulated-gate bipolar transistor*
IH	*Induction heating*
LF	*Low frequency*
MOSFET	*Metal-oxide-semiconductor field-effect transistor*
MTBF	*Mean time between failures*
PCB	*Printed circuit board*
PDM	*Pulse density modulation*
PF	*Power factor*
PFC	*Power factor corrector*
PWM	*Pulse-width modulator*
RL	*Equivalent resistance and inductance*
RMS	*Root mean square*
SE	*Single-ended*
SiC	*Silicon Carbide*
SW	*Square wave*
THD	*Total harmonic distortion*
µC	*Microcontroller*
UZ	*Universidad de Zaragoza*

WBG	*Wide band gap*
ZCS	*Zero current switching*
ZVS	*Zero voltage switching*

List of symbols

α	*Activation delay*
γ	*Auxiliary angle*
δ	*Penetration depth*
η	*Efficiency*
θ	*Signal phase*
λ	*Logistic function slope*
μ_r	*Material permeability*
ξ	*Damping factor*
σ	*Material conductivity*
ϕ	*Magnetic flux*
φ	*Activation width*
ω	*Angular frequency*
ω_0	*Angular resonant frequency*
ω_n	*Angular natural frequency*
ω_{sw}	*Angular switching frequency*
Act_x	*Activation state of load x*
$A_{x,h}$	*Fourier cosine coefficient of x*
B	*Magnetic field*
$B_{x,h}$	*Fourier cosine coefficient of x*
C	*Capacitor*
C_b	*Bus capacitor*
C_r	*Resonant capacitor*
C_s	*Snubber capacitor*
D	*Duty cycle*
D_H	*High-side diode*
D_L	*Low-side diode*
D_S	*Series diode*
d_x	*PDM duty of load x*
E_{off}	*Turn-off switching energy*
E_{on}	*Turn-on switching energy*
f	*Frequency*

f_0	*Resonant frequency*
f_{ac}	*Mains frequency*
f_{sw}	*Switching frequency*
h	*Harmonic number*
i	*Current*
i_{ac}	*Mains current*
i_l	*Load current*
i_c	*Transistor collector current*
i_d	*Diode current*
i_x	*Instantaneous current value of x*
$i_{x\|t}$	*Instantaneous current value of x in the instant t*
I_x	*Average current value of x*
$I_{x,rms}$	*RMS current value of x*
ΔI_x	*Current variation of x*
i,j	*Number of the load in a multi-load system*
J	*Cost function*
K_i	*Integral constant of the regulator*
K_p	*Proportional constant of the regulator*
L	*Inductor*
L_s	*Current source inverter inductance*
L_{eq}	*Equivalent series inductance*
M	*Number of rows*
N	*Number of columns*
n	*Number of loads*
n_s	*Number of switching devices*
P	*Average power*
PF	*Power factor*
P_{in}	*Input power*
P_o	*Output power*
P_{obj}	*Power setpoint*
ΔP	*Power variation*
P_x	*Power losses of x*
$P_{x,on}$	*Conduction losses of x*

$P_{x,sw}$	*Switching losses of x*
Q	*Quality factor*
Q_{rr}	*Diode reverse recovery charge*
R	*Electromechanical Relay*
R_{eq}	*Equivalent series resistance*
R_x	*Resistance of x*
S_H	*High-side transistor*
S_L	*Low-side transistor*
T	*Temperature*
t	*Time*
T_{ac}	*Mains period*
THD	*Total Harmonic distortion of the current*
$t_{on,PDM,x}$	*PDM active time of load x*
T_{PDM}	*PDM period*
T_{sw}	*Switching period*
u	*Control imput*
v_{ac}	*Mains voltage*
v_b	*Bus voltage*
v_c	*Resonant capacitor voltage*
v_{ka}	*Diode cathode-anode voltage*
v_{ce}	*Transistor collector-emitter voltage*
v_o	*Output voltage*
V_{off}	*Fourier average voltage*
v_x	*Instantaneous voltage value of x*
$v_{x,pp}$	*Peak-to-peak voltage value of x*
V_x	*Average voltage value of x*
$\hat{V}_x$	*Peak voltage value of x*
$V_{x,rms}$	*Rms voltage value of x*
ΔV_x	*Voltage variation of x*
x	*State*
$\hat{x}$	*Current state*
Z	*Impedance*

Chapters

Chapter 1

Introduction

The electrothermal mechanisms of induction heating (IH) result on several advantages that justify the growth of the technology to its actual maturity. Moreover, the development of power electronics has encouraged the adoption of a technology with deep industrial roots in the domestic area, leading to the displacement of other heating technologies. As a result, the nowadays challenges in the domestic induction heating development find in the flexible cooking surfaces a high-risk high-gain research field.

This chapter presents the basics of IH, from the fundamentals to the electronics, orienting them to the domestic market. This serves as a start point for the state-of-the-art revision of the multi-output converters required to power the multi-coil structures of the flexible surfaces. Consistently with this presentation, the motivation of the dissertation, objectives, scope, and structure are presented.

Contents

1. Introduction

1.1. Induction heating

Electromagnetic induction phenomenon, in which induction heating (IH) relies, was extensively described during the XIX century. The experiments performed by Michael Faraday in the early 1800s resulted in the formulation of the principle of electromagnetic induction which states that the electromotive force around a closed path is proportional to the time rate of change of the magnetic flux enclosed by the path. This was later complemented by Henry Lenz who established that the induced current opposes the magnetic flux.

Several electric and magnetic studies followed [1], enabling James Clerk Maxwell to elaborate his theory of electromagnetism and to derive the equations to describe all electromagnetic behavior. Some of those studies, as the developed by James Prescott Joule, focused on the heat generation in electrical circuits, emphasizing on the negative effects of the process and aiming for their mitigation. However, soon after, recognizing the potential of this principle, research opened to the application of the phenomenon of induction heating.

1.1.1. IH Physical Phenomena

Typical induction heating applications use a medium frequency magnetic field to generate power losses, that transform into heat, directly on the target material. This contactless power transfer requires the material to be heated to present a conductive behavior, be ferromagnetic, or both simultaneously. Based on this properties, two main physical heat-generating mechanisms arise:

The induced currents (Fig. 1.1), which appear as a result of the induced electromotive force, are the main IH mechanism [2]. These currents, usually known as *Eddy currents* or *Foucault currents*, generate heat as a consequence of the resistive nature of the material by means of Joule effect.

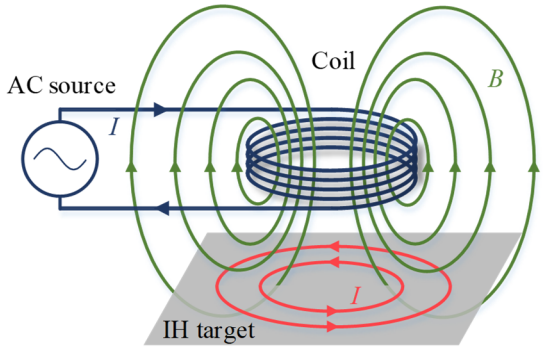


Fig. 1.1. Eddy currents (I, red) induced on the surface of a conductive material when applying an alternating magnetic field (B, green) generated by an ac current (I, blue).

Besides the induced currents, magnetic hysteresis [3] appears on materials with ferromagnetic properties, leading to additional power dissipation. Magnetic hysteresis losses represent the friction of the magnetic domains in the material when rearranged to be aligned with the applied medium frequency magnetic field (Fig. 1.2).

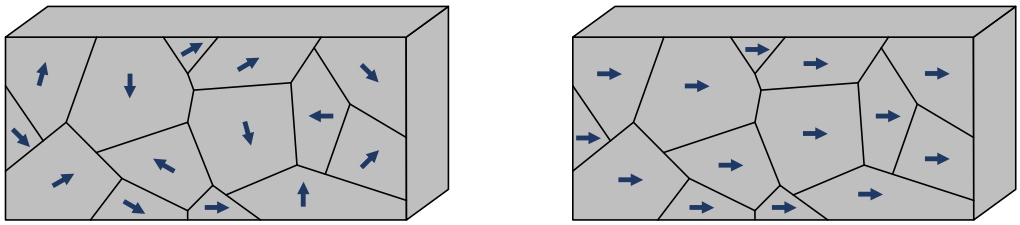


Fig. 1.2. Magnetic domain alignment without external magnetic field (a) and under the influence of a magnetic field (b).

1.1.2. History

The first induction heating applications, related to the industrial environment, date of late 1800s and early 1900s, and focused on metal melting. These early implementations were used to heat metallic crucibles but, soon after, direct-load-heating furnaces with non-conductive crucibles were developed. Both alternatives used a low frequency excitation voltage such as the one provided by the mains or AC transformers [4]. However, the extended use of this technology was possible with the development of high-frequency spark-gap generators and the subsequent use of motor generators, that allowed high power at frequencies up to 3 kHz [5-7].

The more advanced vacuum tube generators, reaching frequencies up to 50 kHz, and the favorable reception of induction melting, drove the progress of heating treatment of metallic components by means of IH. These treatments, such as surface hardening (Fig.

1.3), benefited from the fast and accurate process, leading to an important advance in the military industry during World War II [8, 9].

The increase of induction heating applications in industry relies on its multiple benefits. However, its outburst occurred during the 1960s with the development of high-efficiency solid-state power supplies, allowing more robust and versatile generators with higher operating frequencies, having a considerable influence in the IH technology [10, 11].

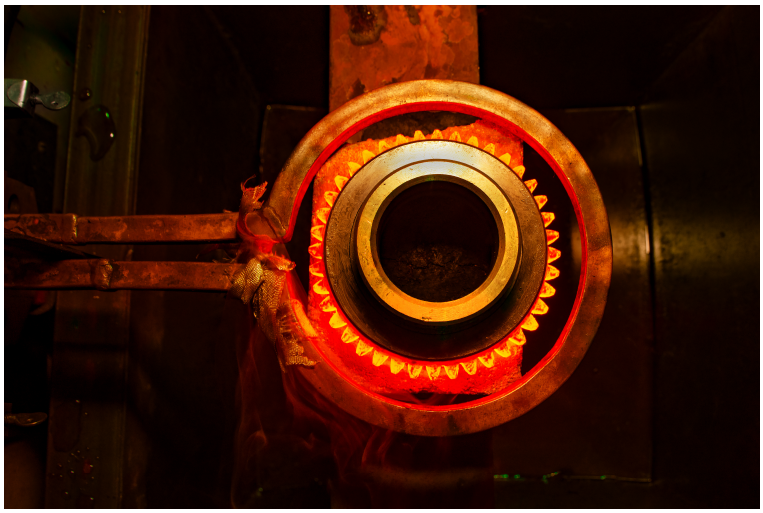


Fig. 1.3. Induction heating hardening of a gear.

The adoption in the domestic environment occurred during the 70's with the first non-industrialized induction heating appliance prototypes in Japan and the USA. In the late 80's, progresses in power semiconductors, especially with the introduction of the insulated-gate bipolar transistor technology (IGBT) [12-14], allowed the design of more efficient, reliable and cost-effective induction cooktops, that were in this case industrialized, introducing the technology to the European market.

Current developments aim to boost the user experience thanks to the differential advantages of induction heating (Fig. 1.4). To do so, reliance on the scientific effort to generate electronic technology improvements allow to overcome the challenges of avant-garde implementations.

Fig. 1.4. Flexible surface domestic IH cooktop.

1.2. Electronic technology applied to IH

As it has been described, the IH alternating magnetic field triggers the power losses mechanisms that produce the heat in the target material. In order to generate it, a medium frequency power converter is necessary. The main building blocks of an induction heating equipment are presented in Fig. 1.5. There, a two-stage conversion can be seen: firstly, a rectifier is used to obtain a dc voltage from the mains ac power supply and then, a medium-frequency inverter is used to generate the required alternating current which produces the magnetic field when circulating through the induction coil. Additionally, a filter stage is included to fulfill electromagnetic compatibility (EMC) regulations. Finally, the complete converter is controlled by means of a digital control stage.

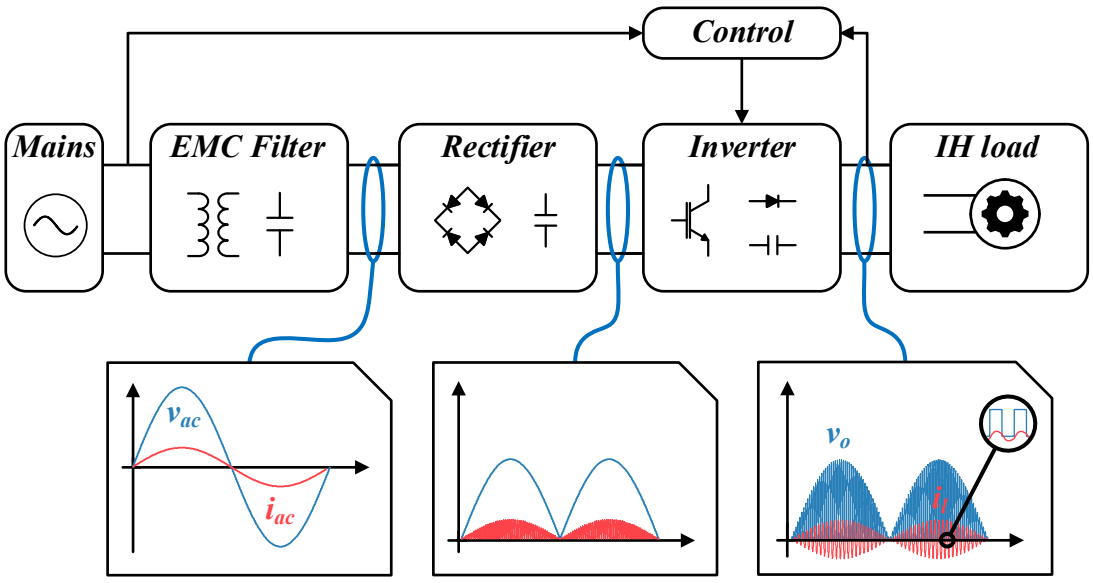


Fig. 1.5. Main elements of a typical IH equipment.

These blocks can be classified according to its functionality into the following groups: inductor-load system, power electronics, and control electronics. In order to obtain a cost-effective implementation with optimal performance, all blocks have to be properly and coordinately designed [15]. These groups are further explained in the next sub-sections.

1.2.1. Inductor-load system

The inductor-load system allows the transformation of the electrical energy into heat in the load. It consists of a coil, the target material, and several additional components to improve the IH equipment operation. The coil geometry is determined to produce the desired temperature profiles in the target material to fulfill the desired application, i.e. melting, sealing, welding, etc. [16-22], and is usually constructed by copper wires, bars, or even tubes if water cooling is needed, e.g. for the case of domestic induction cooktops a planar spiral coil of *Litz* wires [23-26] is shaped ensuring an homogeneous heat distribution on the pot base (Fig. 1.6 (a)). Usually, the inductor-load system includes ferrite pieces, that operate as flux concentrators to improve the magnetic coupling between the material and the coil, and also additional thermal or electromagnetic isolation layers, to minimize interference with the electronics.

(a) (b)

Fig. 1.6. Example of an inductor-load system (a) and equivalent electrical model (b).

With the development and improvement of finite elements modelling (FEM) techniques and the subsequent possibility of simulating increasingly complex models, the complete inductor-load system can be computationally analyzed considering the coil and material properties, geometries and operation parameters, i.e. coil and material temperature [27], magnetic field frequency [24, 28-31], magnetic field strength, etc.

However, given the key relevance of this system in the definition of the resonant tank, and in order to simplify its calculation, from the electrical point of view it has been traditionally simplified to the equivalent series connection of a resistance, R_{eq}, and an

inductance, L_{eq}, [32, 33] as presented in Fig. 1.6 (b). This simpler model eases the mathematical treatment of the converter and its simulation and the physical analysis of the power transfer, as the heat generated in the target material is represented by the power dissipated on the resistance.

Nevertheless, it is only valid for a single operation point as it presents a high dependency with the aforementioned parameters, which should be taken into account. In order to solve that, the parametrization of the equivalent values as a function of the operation parameters can be considered as:

$$L_{eq} = L_{eq}(f, T, I), \tag{1.1}$$

$$R_{eq} = R_{eq}(f, T, I), \tag{1.2}$$

were f is the excitation frequency, T is the temperature, and I is the current excitation level. This way, the accuracy of the model is increased but, as the excitation level is usually considered as an average level more than an instantaneous value, it still presents no dynamic variation within the switching cycle.

In the literature several structures based on inductances and resistances have been proposed to model this behavior, requiring more complex calculation and parameter fitting [28]. For this reason, and given that the converter design and analysis rely on its capacity to operate with different loads, it is considered not justified the increase in complexity for the development of this dissertation, and therefore, the parametrized RL series model will be used.

In this scenario, some useful additional numeric parameters to characterize the load that include the excitation frequency are the quality factor, Q, and the power factor, PF, defined by (1.3) and (1.4) respectively.

$$Q = \frac{\omega L_{eq}}{R_{eq}}, \tag{1.3}$$

$$PF = \frac{R_{eq}}{\sqrt{{R_{eq}}^2 + \left(\omega L_{eq}\right)^2}}, \tag{1.4}$$

being ω the angular frequency. These parameters allow a fast characterization of the load and, in some cases, reduce the dependencies with the operation parameters, e.g. in domestic induction heating.

Besides, given that the series resonant configuration is usually selected, the resonant frequency, f_0, and thus the angular resonant frequency, ω_0, can be obtained as a function of the resonant capacitor, C_r, as

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_{eq} C_r}}. \tag{1.5}$$

1.2.2. Power electronics

Most IH systems require an electronic power converter in order to transform the mains low-frequency ac voltage into a medium-frequency ac voltage to power the inductor-load system. Classically, a two-stage power conversion scheme, as the shown in the block diagram of Fig. 1.5, is preferred.

On the first stage, the mains is rectified to obtain the dc-link voltage, v_b. The most common and simple implementation of this block uses a diode full-bridge rectifier with a low value dc-link capacitor (Fig. 1.7 (a)) that filters the high frequency currents required by the inverter while ensures an input power factor close to unity [18, 34-37]. This allows to reduce the electromagnetic compatibility (EMC) filter requirements but results on a high-ripple dc voltage, decreasing the effective voltage and requiring higher current levels for a given output power. For this reason, lately, synchronous rectifiers with power factor correction (PFC) capabilities have been proposed for IH equipment (Fig. 1.7 (b) and (c)) [38-41].

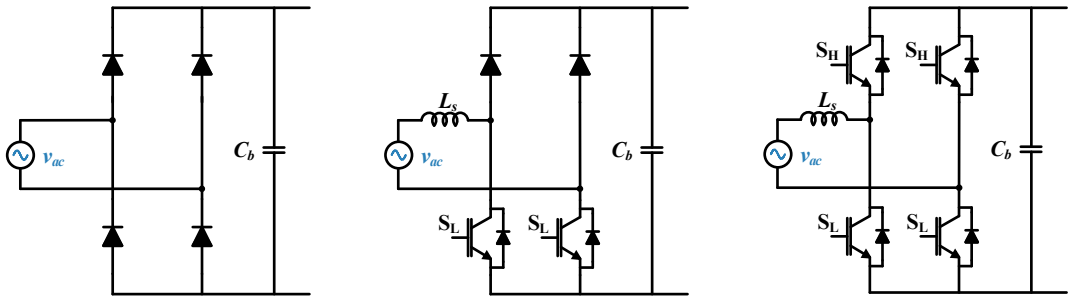


Fig. 1.7. Alternative rectifier blocks: single-phase full-bridge rectifier (a), totem-pole boost converter (b), and full bridge bidirectional PFC boost converter.

On the second stage, an inverter generates the medium-frequency voltage and current transferred to the inductor. Several inverter topologies have been proposed focusing on different aspects such as efficiency, component count, or control complexity, being resonant and quasi-resonant topologies the most used ones due to their higher efficiency

[42]. In the following lines, the most common single-load topologies for IH are presented, classified according to the number of switching devices:

- Quasi-resonant single-ended (SE), or single-switch, topologies present the lowest-possible power device count [43-47]. However, these devices require high voltage blocking capabilities as they operate up to 3 to 4 times the mains peak voltage. Fig. 1.8 shows the voltage source zero-voltage-switching (ZVS) inverter and current source zero-current-switching (ZCS) inverter implementations of this single-switch topology. Their main disadvantage is the reduced number of modulation parameters to control the transmitted power, being the on-time the control parameter for the ZVS implementation, and the off-time the control parameter for the ZCS one. This results in a reduced controllability range, highly dependent on the load, leading to decreased efficiency when operating outside the soft-switching region. Moreover, current source inverters (CSI) require additional bulky inductors and are considered not suitable for compact and cost-effective implementations, i.e. domestic IH on which this thesis focuses.

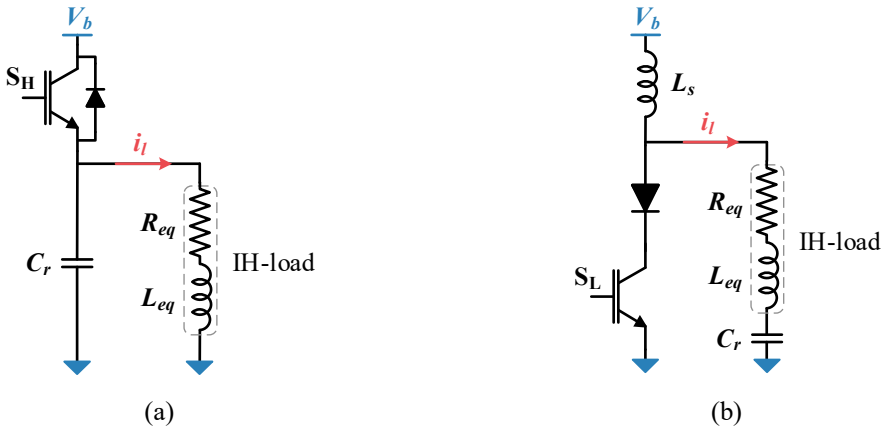


Fig. 1.8. Single-ended quasi-resonant inverters: voltage source zero-voltage-switching inverter (a), and current source zero-current-switching inverter (b).

- Half-bridge (HB) inverter topologies use two switching devices [48-53]. The half-bridge series resonant inverter is currently considered the best alternative in terms of performance, cost, and complexity for the power levels considered in this thesis. Consequently, the implementation using IGBTs and antiparallel diodes (Fig. 1.9) is used due its low cost and robustness. For this topology, the resonant capacitor is implemented in a split configuration to decrease the bus

current harmonics. Additionally, operation is preferred above resonant frequency to achieve a ZVS commutation and by means of snubber capacitors, C_s, in parallel with the switching devices, the turn-off losses can be mitigated.

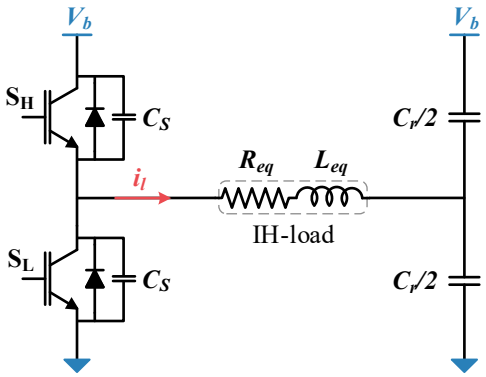


Fig. 1.9. Half-bridge series resonant inverter using split resonant capacitor and capacitive snubber networks.

- The full-bridge (FB) topology [54-57] requires four switching devices, as it is shown in Fig. 1.10. It allows a higher output power as the voltage applied to the load is doubled in comparison with the HB configuration. The high reliability and efficiency of this topology makes it the most suitable one for industrial applications [32]. For this reason, the first end-user commercial applications where proposed based on it.

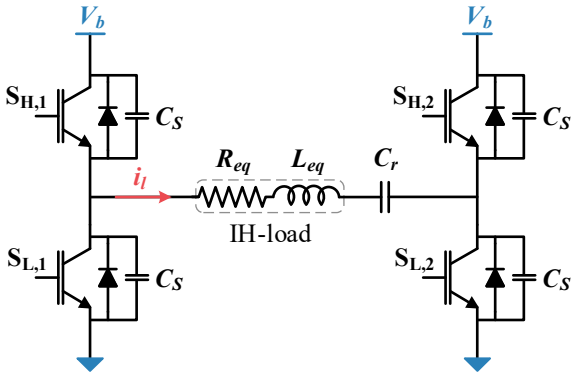


Fig. 1.10. Full-bridge series resonant inverter.

1.2.3. Control stage

The main purpose of the control stage is to control the transmitted power to the load based on the user input in a safe and efficient manner. To do so in a proper way, two main parts present great relevance: control electronics and modulation strategies.

1.2.3.1. Control electronics

Control electronics can be divided into three main blocks: the measurement system, the control logics, and the gate signal generation.

The measurement system samples the different signals of the power converter, such as the bus voltage, the inductor current, or the resonant tank applied voltage. It is composed by the sensing circuits and analog-to-digital converters [58, 59].

This information is transmitted to the control logic (Fig. 1.11), which is typically composed of a microcontroller (µC) [60], and the required additional specific hardware, which is usually implemented on an Application Specific Integrated Circuit (ASIC) or a Field-Programmable Gate Array (FPGA) [61-64]. Based on the selected control algorithm and the power level selected by the user, the µC generates the modulation parameters that define the gating signals.

With the modulation parameters as inputs, and using its parallelization capabilities [65, 66], the ASIC or FPGA manages the PWM modulations which are transmitted through a driving circuit to the transistor gate.

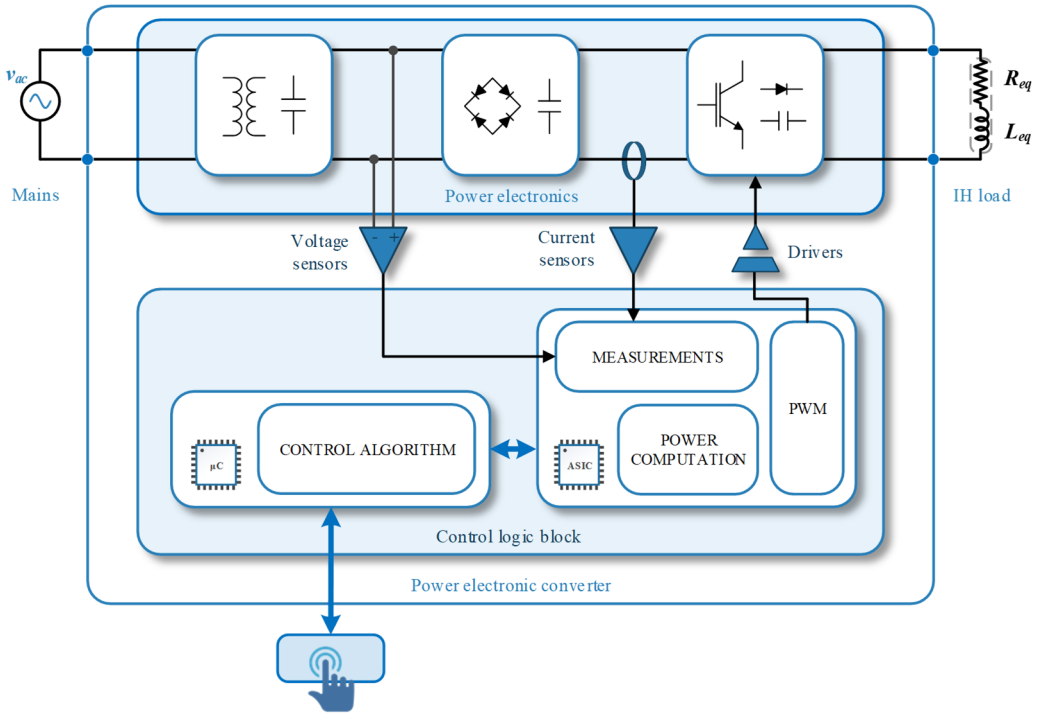


Fig. 1.11. Block diagram of the control stage of the IH converter.

1.2.3.2. Modulation strategies for power control

The activation and deactivation of the switching devices of the inverter allow to control the transmitted power while ensuring safe operation. The modulation strategies depend on the inverter topology and have a great responsibility in the overall performance of the induction heating equipment. When using the resonant HB and FB topologies, which are the ones that present a higher number of degrees of freedom, the most common modulation strategies are the following:

- Square Waveform (SW) uses the inverter switching frequency, f_{sw}, as the power control parameter [53, 67, 68] (Fig. 1.12 (a)). The evolution of the transmitted power can be seen in Fig. 1.12 (b) and the converter usually works over the resonant frequency to operate under ZVS condition, leading to an inductive behavior and decreasing the power with the frequency increase. Therefore, the efficiency decreases for lower powers as the switching frequency, and thus the switching power losses, are greater.

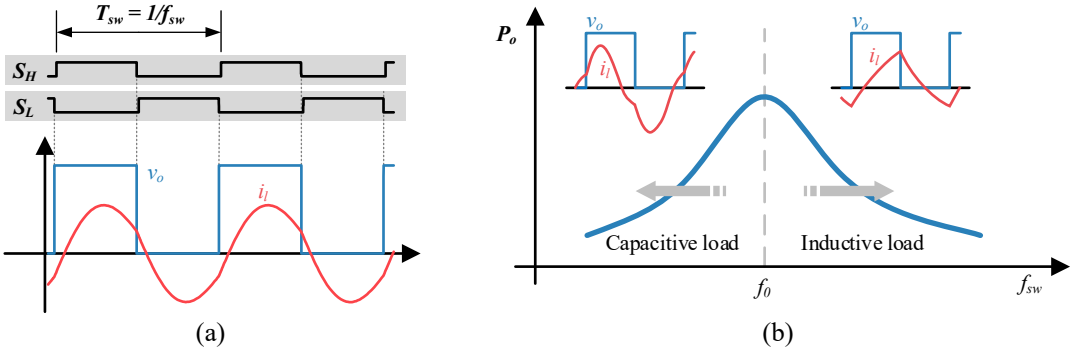


Fig. 1.12. Square waveform modulation parameters (a) and output power, P_o, and main waveforms of a resonant load as a function of the operation frequency, f_{sw} (b). The detailed waveforms depict the inverter output voltage, v_o, and current through the coil, i_l.

- Asymmetrical Duty Cycle (ADC) presents the duty cycle, D, as an additional control parameter, which results in an uneven voltage application (Fig. 1.13 (a)). This strategy allows to decrease the transmitted power without increasing the switching frequency, leading to good efficiency in the medium-low power range [68-70].

- Phase Shift Control and Asymmetrical Voltage Cancelation (AVC) require a FB inverter to be implemented. In both cases, the displacement between the leading and the lagging leg of the full bridge generates an additional 0V voltage level [55, 71-73]. This way it is possible to control the transmitted

power without changing the switching frequency or even the duty cycle (Fig. 1.13 (b)).

- Pulse Density Modulation (PDM) relies in the inverter alternative activation and can be used in combination with any of the aforementioned strategies to provide low power (Fig. 1.13 (c)). This is a very common and simple strategy as the output power is proportional to the active time, $t_{on,PDM}$, over the period, T_{PDM} [18, 74-76] However, power pulsation generates voltage fluctuation in the mains, which is limited by EMC standards.
- Discontinuous modulation strategies allow a non-complementary activation of the transistors of the inverter, leading to uncontrolled states where the voltage applied to the load depends on the current path [77-80] (Fig. 1.13 (d)). These strategies present a high dependency with the load quality factor, Q, to achieve current discontinuity and therefore the generalized denomination non-complementary modulation strategies is considered in this thesis.

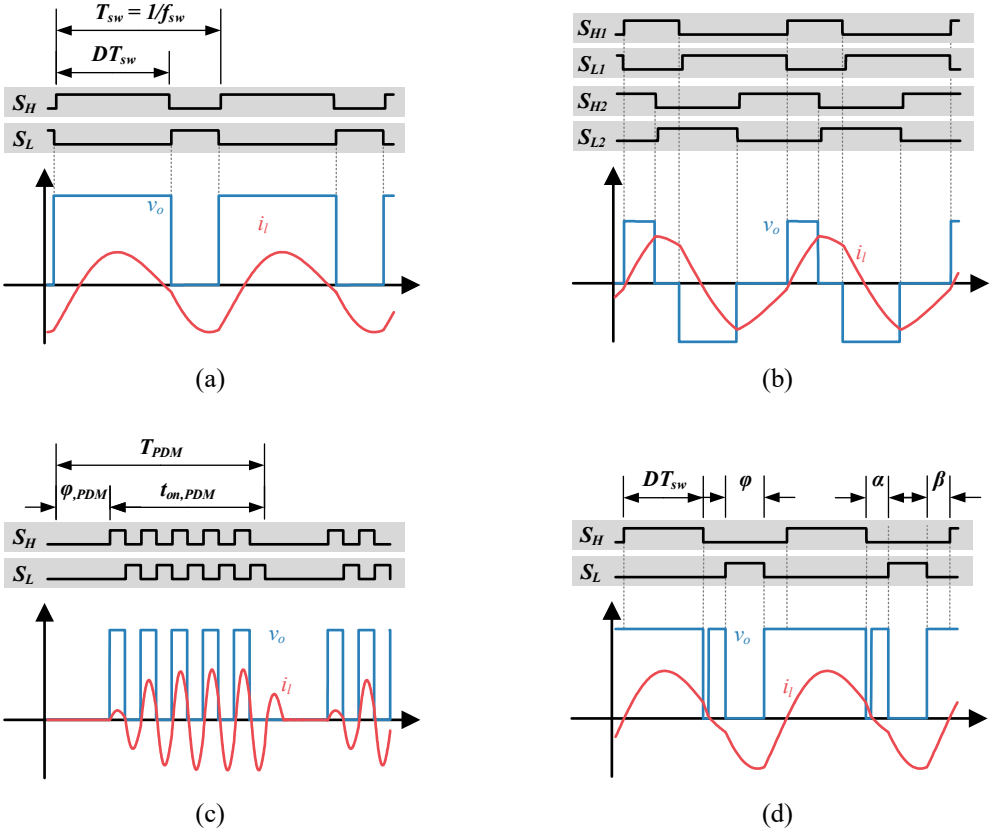


Fig. 1.13. Main modulation strategies: asymmetrical duty cycle (b), asymmetrical voltage cancelation (b), pulse density modulation (c), and non-complementary modulation (d).

1.3. Domestic IH

The structure of a commercial induction cooktop is presented in Fig. 1.5. The inductor-load system comprises a series of stacked layers being the pot, which is the target object, the top one. Below, the vitroceramic glass provides structural support and electrical isolation. An additional thermal and electric isolation layer is placed between the glass and the planar inductor, which is typically made of Litz wire. Moreover, a ferrite bead to concentrate the flux towards the pot and an aluminum shielding to enclose the electromagnetic fields are present. The power electronic system is located into the case and under the aluminum layer, and it requires a forced cooling system. The control stage is usually divided between the user interface that is placed directly under the glass and the control circuitry and microcontroller that are integrated in the power circuit board.

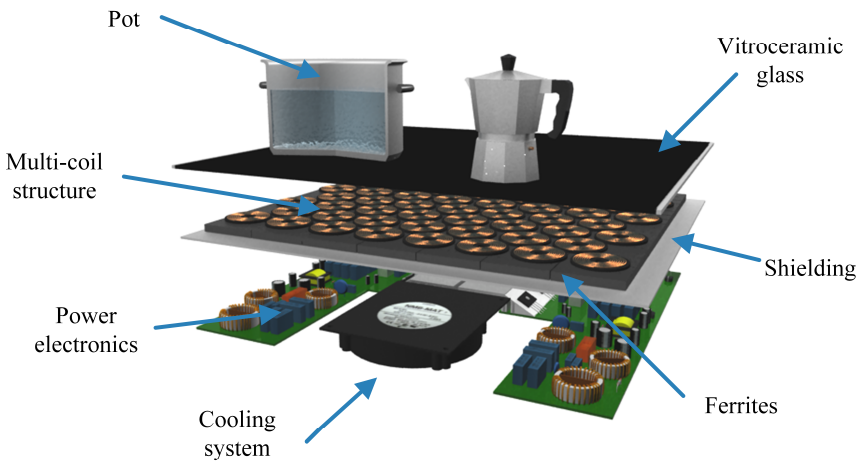


Fig. 1.14. Main elements of a typical commercial IH cooktop.

These structures are designed to provide low-cost compact and robust solutions that present multiple advantages over the competitors.

1.3.1. Advantages

The main advantages of domestic cooktops compared with classical heating technologies are a consequence of the direct power transmission to the pot:

- Reduced heating times due to lower system thermal inertia as the heat is directly generated in the pot base.
- Improved safety and cleanness due to lower glass surface temperature [16].

- Higher efficiency as a consequence of the direct energy transfer to the target and the power electronics developments.
- Improved thermal control is achieved since the applied power can be accurately controlled
- Automatic pot detection based on the variations of the current waveforms depending on the pot material and position.

1.3.2. Market and current developments

The induction heating technology application to the domestic environment has pushed the induction cooktops to lead the home appliances market against other heating technologies. Moreover, in recent years, several developments have been pursued to boost the product differentiation by creating a new cooking paradigm. Some of the most relevant are depicted in Fig. 1.15 and are:

(a) (b)

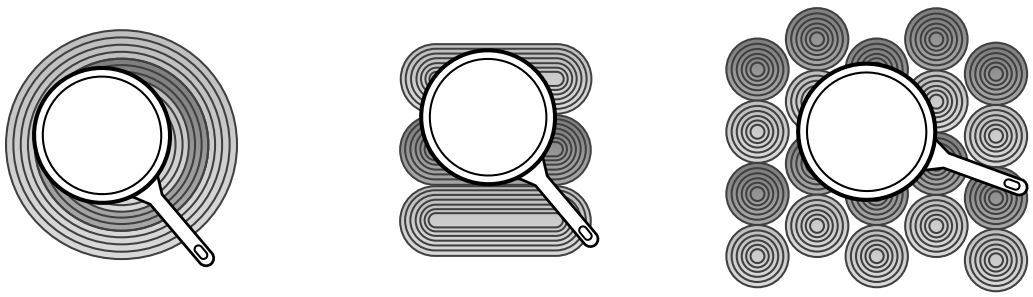
(c) (d)

Fig. 1.15. Prospective research field for future developments in domestic induction heating: Integrated venting (a), under worktop implementation (b), wireless power transfer (c), and flexible surfaces (d).

- Integrated venting: The lower temperatures on the vitroceramic glass and inside the cooktop case have permitted the inclusion of additional electronic

components. One of the most relevant due to its market acceptance has been the incorporation of the extractor structure in the center of the cooking zone.

- Under worktop: The improvements in the electronic power devices and inductor systems have allowed to increase the distance between the pot and the induction coil. Combining this with the transparency of the non-conductive materials to the influence of the magnetic field, the vitroceramic glass has been proposed to be replaced by the kitchen countertop, resulting in cleaner and more versatile cooking areas.
- Wireless power transmission: The similarities between the induction cooktops and the wireless power transfer converters have open the possibility to replace wired connections in small kitchen appliances with receiver coils and operating them directly over the cooking surface.
- Flexible surfaces: This alternative aims for improving the user experience with cooktops where pot placement is not constrained anymore [81]. These developments are the natural evolution of the multi-inductor architectures [82]. Firstly, concentric-coils systems, consisting of ring-type inductors, improved the adaptability to the pot size activating the coils covered by it [83-85]. Secondly, non-concentric coils allowed to configure heating area allowing the pot displacement in a certain axis. Finally, total-active surface systems allow free pot positioning over the cooktop [86, 87].



(a) (b) (c)

Fig. 1.16. Flexible induction heating alternative layouts. Size flexibility (a), vertical flexibility (b), and complete flexibility (c).

1.4. Multi-output topologies

1.4.1. Introduction

Total active surfaces are the most advanced flexibility level achievable. Their purpose is to allow the placement of any pot with any shape in any position over the cooking appliance. This proposal presents several challenges in order to provide robust, versatile, and cost-effective implementations aiming for improving the user experience.

The total active surface construction is done by tessellating the area with small or medium size coils (Fig. 1.17). Thus, the topologies have to present the capability of powering a medium to high number of coil-pot structures, or IH loads, being this quantity higher than the classical four hob structure.

Fig. 1.17. Total active surface implementation.

Additionally, the surface configuration eliminates pot positioning and, consequently, the pot-coil coupling can vary even between inductors under the same pot. This variation leads to different L_{eq} and R_{eq} parameters for each IH load. Combining this variation with the different pot power set-point, the inverters must allow independent power control in order to ensure safe operation for the topology and optimal power delivery.

To solve these constraints, the study of multi-output resonant converters has become one of the most prolific research fields in the development of induction-heating flexible-surface appliances [61].

1.4.2. State of the art

Several solutions of multiple output converters have been proposed from the industrial and academic point of view, focusing on different design principles. In order to present a detailed overview of the alternatives, the multi-output converter design procedure serve as a topology classification mechanism, leading to three different categories. The first one

includes the clustering of single output inverters that may share, or not, some building blocks, e.g. the rectifier or the filter. The second group, called load multiplexation, comprises the alternatives that use a single output inverter and a configuration method to select which IH load is connected. The third and most heterogeneous group, called multi-output topologies, includes those multi-output inverters that are controlled with different modulation strategies that operate at frequencies in the same order of magnitude as the excitation frequency applied to the coil (Fig. 1.18).

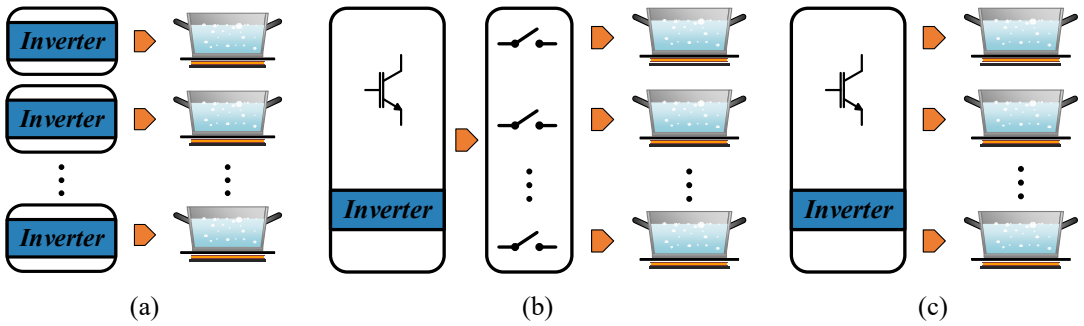


Fig. 1.18. Classification of the multiple output power converters for application with IH loads: single output inverter parallelization (a), load multiplexation (b), and multi-output inverters (c).

1.4.2.1. Single converter parallelization

The parallelization of single-output inverters is a straight-forward implementation for multi-coil IH systems [88]. A typical induction cooktop, that is comprised of two to four hobs, is then powered by the combination of classical resonant inverters such as the full-bridge (FB) [32, 54-57, 89-91], half-bridge (HB) [48-53, 92], single-ended – zero current switching (SE-ZCS) [43-47] or single-ended – zero voltage switching (SE-ZVS) [14, 93].

The use of well-known building blocks allows an easy topology design and implementation. Additionally, as a consequence of the extensive single inverter analysis, it is possible to control them with robust and efficient modulation strategies [53, 55].

However, when the coil count increases, the number of power devices grows linearly, being significant for the FB and HB inverters and, consequently, leading to bulky and expensive implementations. Additionally, independent load power control becomes more complex as switching frequency constraints appear. In order to avoid intermodulation noises [94], single frequency power control strategies increase their relevance and, especially for SE combinations, the calculation of resonant tanks with spaced enough resonant frequencies may be necessary [46]. Therefore, this group is usually used for a low IH-load count.

1.4.2.2. Multiplexation stage

Load multiplexation technique relies on the use of a single inverter to feed two or more IH loads by selecting the current path. As a consequence, the desired output power is reached by the combination of the modulation strategy, e.g. switching frequency variation, and the time averaging of the different IH-load activations.

The most commonly used topology in domestic IH is the series resonant half-bridge inverter with two multiplexed loads (Fig. 1.19) that may share, or not, the resonant capacitor [95-97]. For both cases, this topology can be extended to the desired number of loads. However, it must be considered that increasing the number of loads may compromise the correct output power control due to the more restricted multiplexed control.

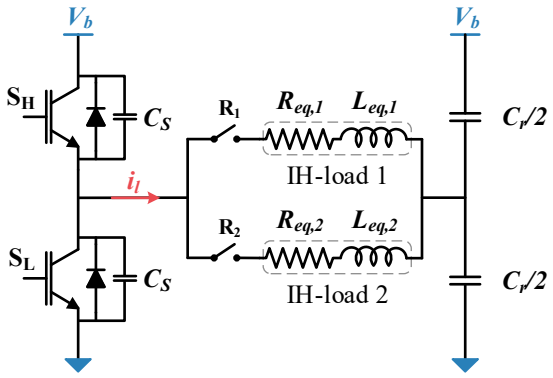


Fig. 1.19. HB inverter with two multiplexed loads.

Most of the reviewed architectures feature load connection and disconnection by means of electromechanical relays [28] due to their low power losses and reduced cost. Consequently, the IH load multiplexation is done at low frequency due to the long turn-on and turn-off relay settling times, that reduce the active times of the loads. This low frequency reduces the repetition of noisy relay switching [98] but leads to uneven boiling perceived by the user and power consumption restrictions, i.e. flicker regulations [99]. These are severe limitations of this approach that affect both the user experience and the technical performance of the final implementation.

In order to overcome these problems, [100] proposes a two-inverter topology with a half wave rectifier so that each HB is connected to a mains half-cycle and the remaining is used to reconfigure the relays. This approach solves additional problems as the non-zero current commutation of the relays but significantly reduces the load output power.

In addition to the presented topologies, the load multiplexation by means of an electromechanical relay can be combined with inverter parallelization. This way it is possible to increment the maximum power in the active load by connecting two inverters in parallel when one of them is not being used, as shown in Fig. 1.20. Additionally, this parallelization can improve the inverter efficiency and increase the lifecycle of the power devices [101]. However, the use of relays makes the pot detection system implementation even more challenging [102].

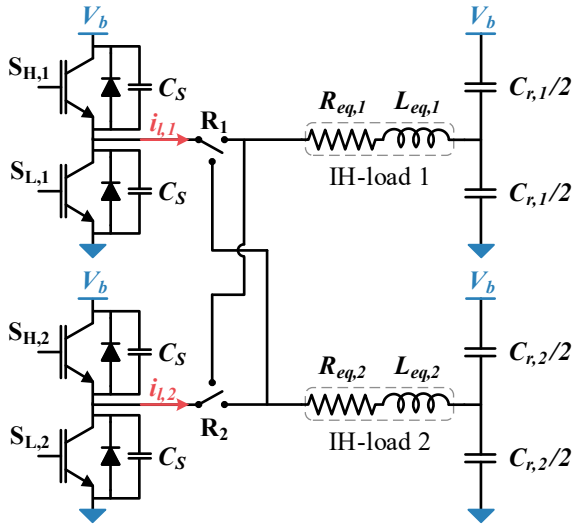


Fig. 1.20. Half-bridge inverters parallelization scheme to power a single load.

This recombination presents high advantages when the coil layout presents a hierarchy, as it occurs with the concentric layouts [103]. In Fig. 1.21, a concentric planar coil inverter combination is presented. Additionally, this topology shows a resonant capacitor compensation structure due to it being shared by different loads.

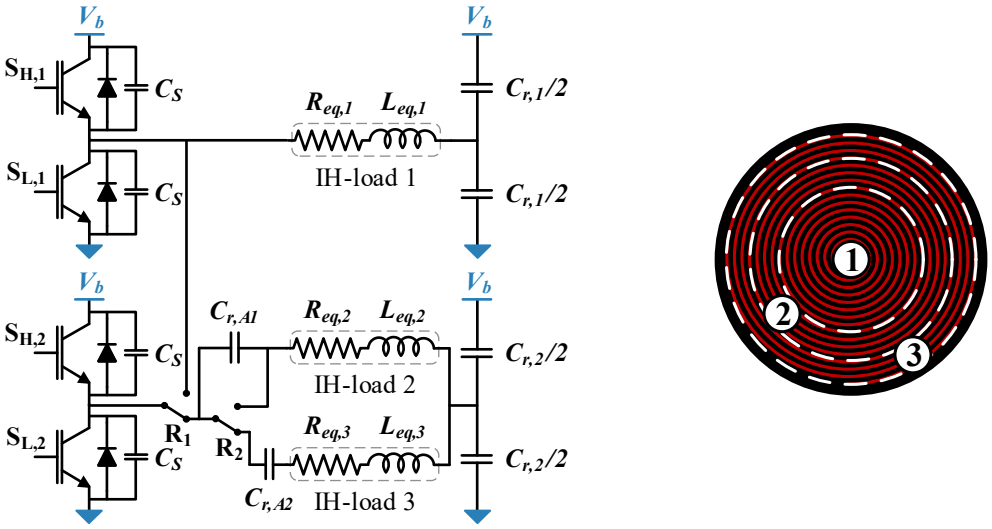


Fig. 1.21. Half-bridge inverters parallelization for usage with concentric planar coils.

1.4.2.3. Multi-output topologies

In order to solve the low frequency load multiplexation issues of the relay-based implementations, several multi-output topologies have been analyzed in the literature. Moreover, the proposed alternatives tend to present additional advantages to direct device substitution [104], such as reducing the device count or increasing the inverter versatility. As a consequence, this is the most promising group and, at the same time, the most heterogeneous one.

In [28], a HB topology with parallel IH loads uses frequency selection to choose the active load. This alternative relies on capacitor calculation to generate resonant tanks with spaced-enough resonant frequencies (Fig. 1.22). This way, power control of the active load can be selected by means of the switching frequency while the remaining resonant loads present high impedance paths. This topology presents several restrictions such as wide switching frequency range, non-ideal infinite impedance paths, and alternative load activation.

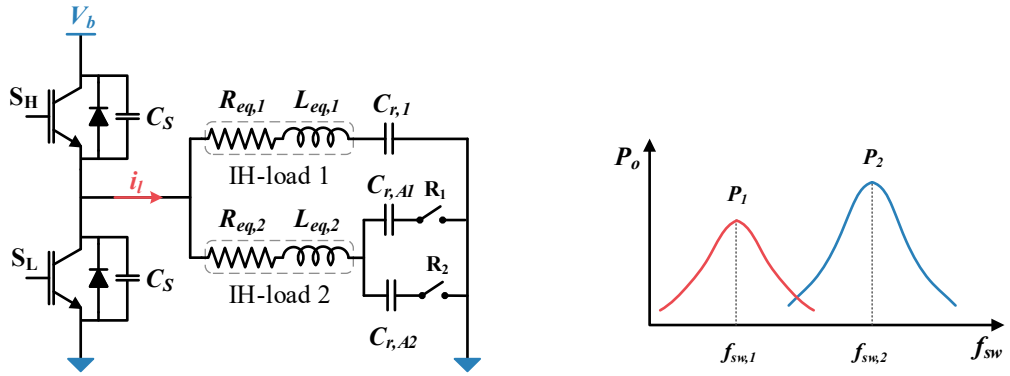


Fig. 1.22. Frequency-selection-based HB inverter.

In order to power both loads simultaneously, [105] proposes the FB inverter to allow dual frequency operation by using a different switching frequency in each of the legs. This technique is also used in industrial IH to improve heating processes in complex geometries [106].

A different synthesis method to obtain a two output FB inverter is utilized in [94]. The two-output three-leg FB inverter shown in Fig. 1.23 operates with asymmetrical voltage cancelation to obtain independent power control. In [107], a multiple load generalization is analyzed and the three load with configuration relays is proposed.

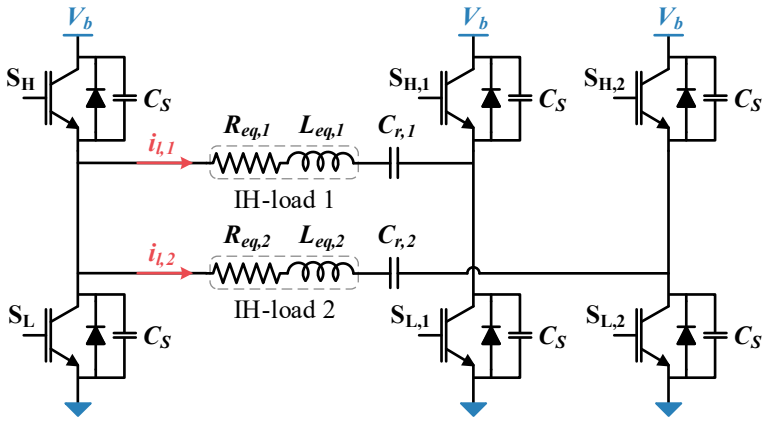


Fig. 1.23. Two-output three-leg FB inverter.

In [108], the common leg of the two-output three-leg FB inverter is used to implement a boost PFC stage (Fig. 1.24). This modification improves the mains current consumption without increasing the power device count. However, the new topology requires a series inductance and a more complex control.

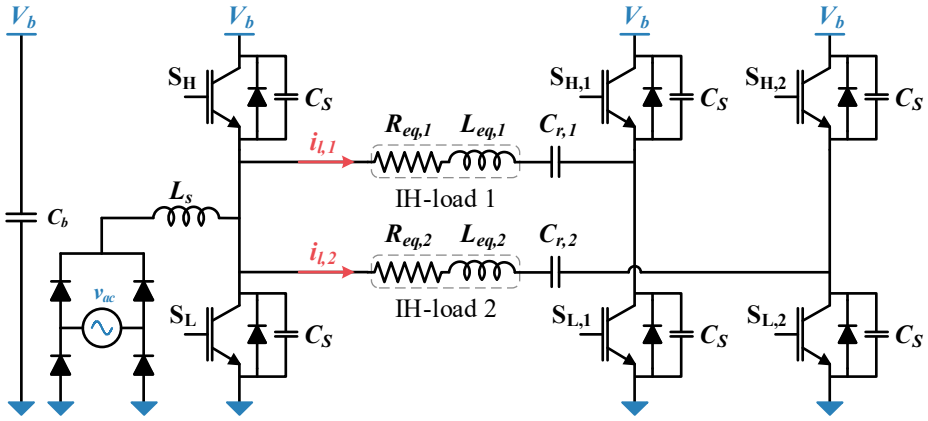


Fig. 1.24. Two-output three-leg boost-PFC FB inverter.

A similar boost approach to the two-output three-leg FB inverter is followed in [109, 110], obtaining a higher reduction of the device count (Fig. 1.25 (a)) as only two out of the four diodes of the rectifier are needed. Additionally, the inverter is proposed for any number of IH loads. An alternative form as a combination of paralleled HB inverters is proposed in [111] (Fig. 1.25 (b)).

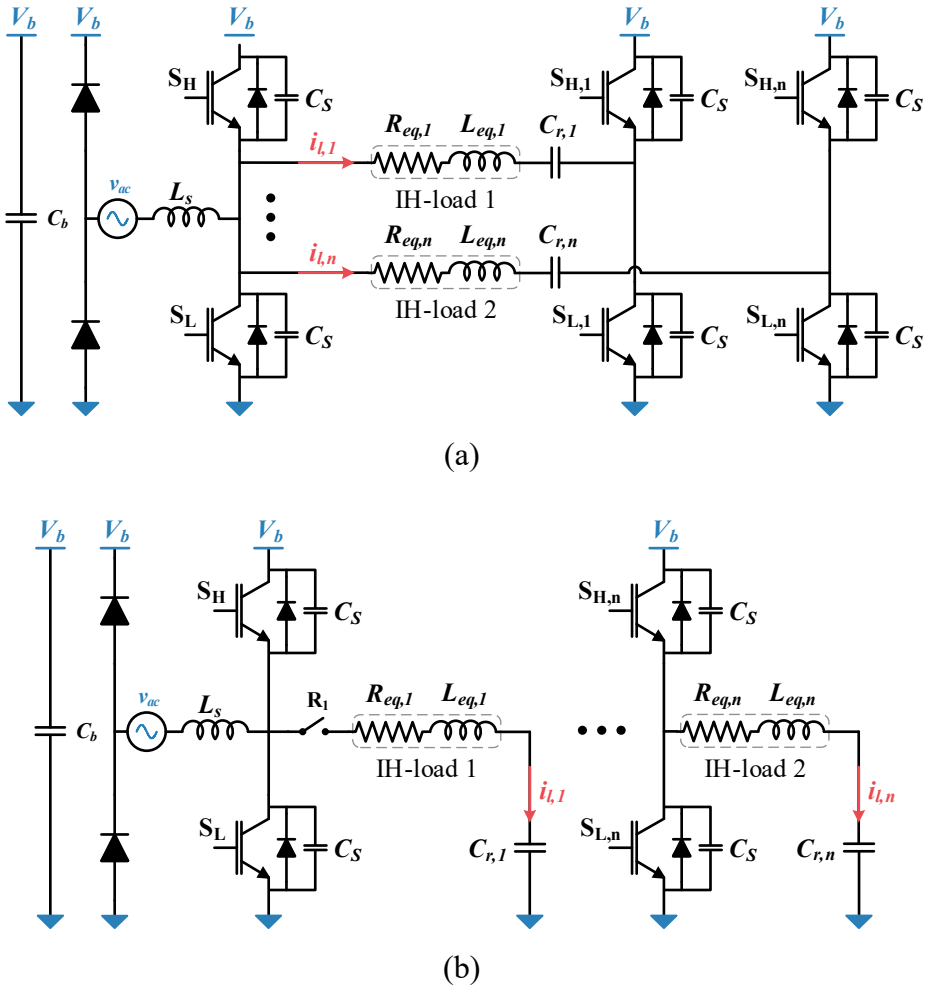


Fig. 1.25. Multi-output three-leg boost-HB-rectifier FB inverter (a) and HB inverter (b).

In [112], a three switch topology derived from the HB is proposed to power two loads. The inverter, depicted in Fig. 1.26, operates by creating an alternative path for the current. Thus, depending on the active switch, a HB series resonant structure is defined by the remaining. This inverter is compact and cost-effective and can be generalized to any number of loads. However, the load activation is necessarily alternative and the addition of semiconductor devices in series degrades the current path and increases the conduction power losses.

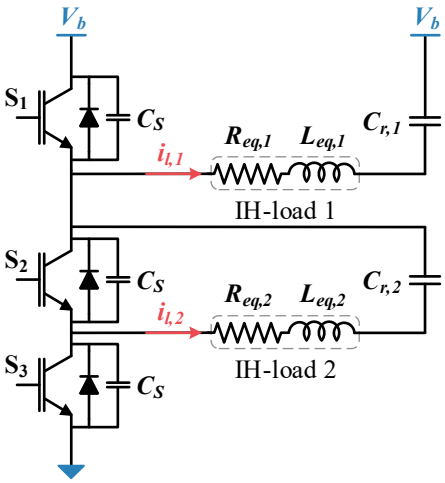


Fig. 1.26. Two-output three-switch HB-derived inverter.

Based on the same principle, [113] presents a FB structure to power two loads with a shared resonant capacitor and semiconductor devices to short circuit each coil (Fig. 1.27). As in the previous case, this structure leads to an alternative load activation and current path degradation but, in contrast, it comprises a higher number of power devices.

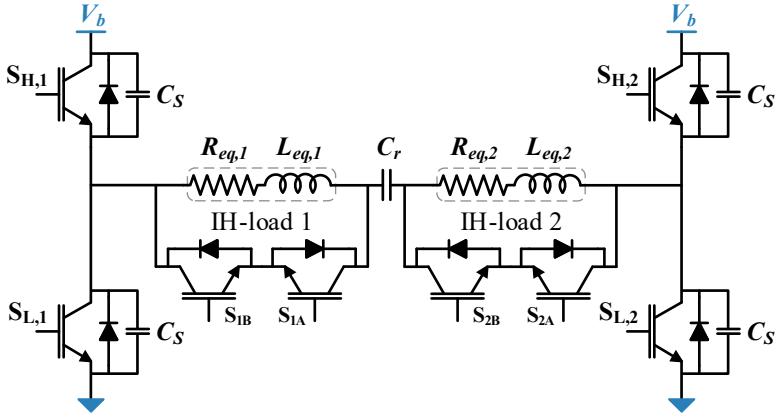


Fig. 1.27. Two-output series FB with coil short circuit devices.

Several multi-output resonant inverters derived from the HB are proposed in [29]. The first inverter, shown in Fig. 1.28, uses three switching devices to power two loads both alternatively and simultaneously with almost independent power control. For this topology, single coil activation relies in the coil short circuit. However, for multiple active coils, the power control is done by switching frequency selection and cascaded duty cycle. This master slave hierarchy in combination with ZVS limitations for asymmetrical control reduce the power control flexibility.

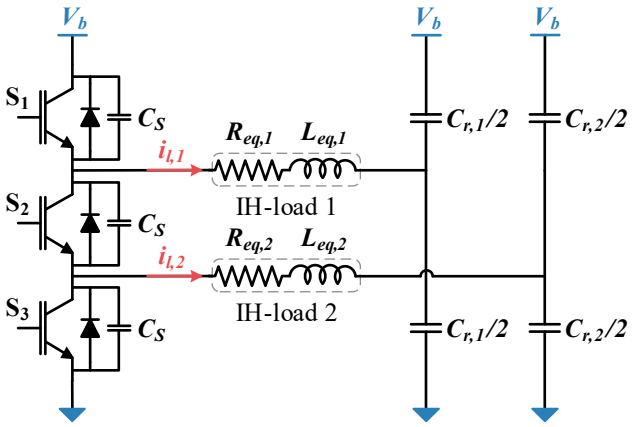


Fig. 1.28. Two-output three-switch HB-derived inverter with independent power control for two IH loads.

The second inverter (Fig. 1.29), uses two HB inverters to feed four different loads. Two of the IH loads are connected to the midpoint of the HB and their power is controlled by switching frequency selection while the remaining are connected in series between the middle point of the HB, forming a FB, and its power is selected by phase shift control. This topology greatly reduces the number of power devices but presents a complex control which can be only applied with similar IH loads.

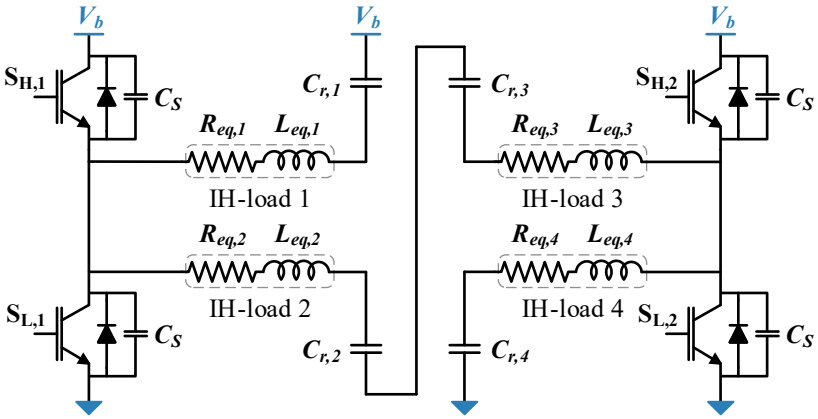


Fig. 1.29. Four-output two-HB inverter to power four similar IH loads.

The third topology proposed in [29] (Fig. 1.30), is described as a three-switch topology generalization. Even though it is a parallelization of single load half bridge topologies, it is included in this subsection because it presents an additional power transistor and an inductance to ensure ZVS commutation independently of the duty cycle. As a consequence, it allows power control operating with a single switching frequency.

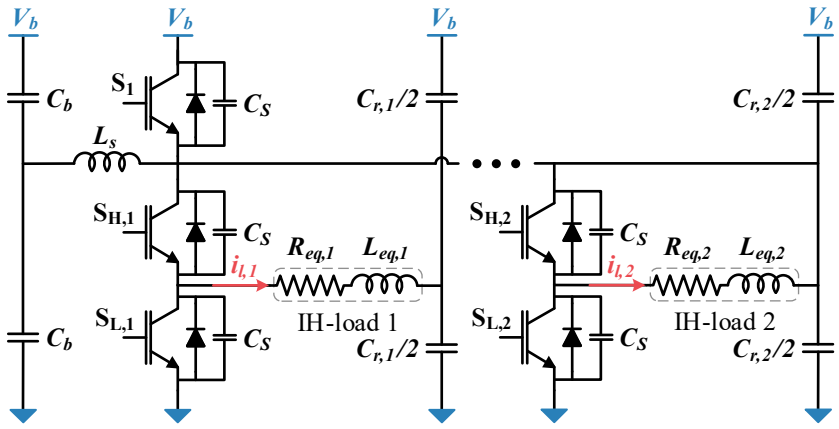


Fig. 1.30. Multi-output three-switch HB-derived inverter with series coil to ensure ZVS switching.

In [114, 115][116], a HB common block inverter with an independent load series transistor is proposed. This inverter can operate by multiplexing the loads but also with alternative control modes such as discontinuous control [80]. The topology is presented in Fig. 1.31 while its deployment to FB configuration is shown in Fig. 1.32 [91, 117].

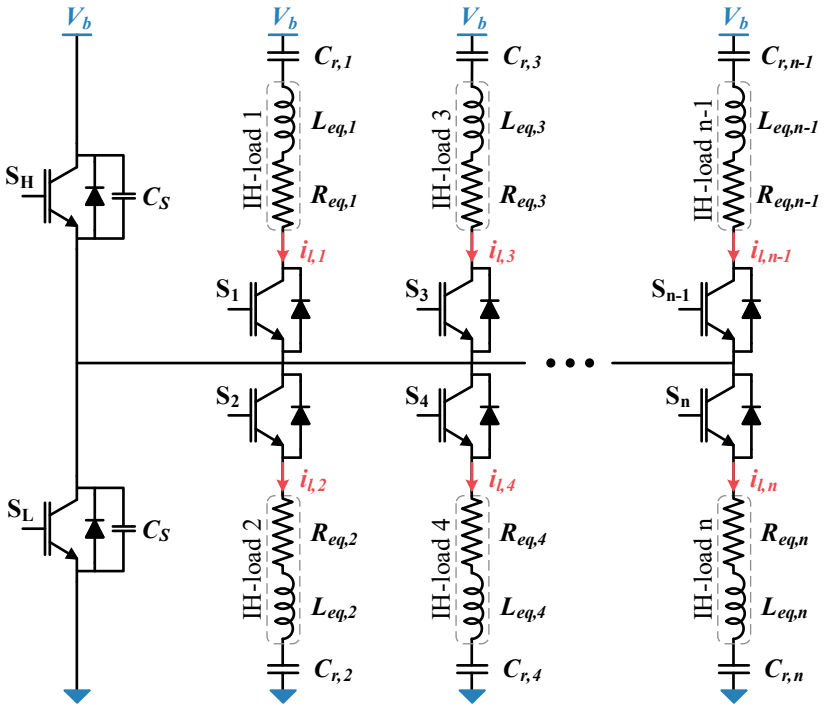


Fig. 1.31. Multi-output common-HB inverter with load-series transistor.

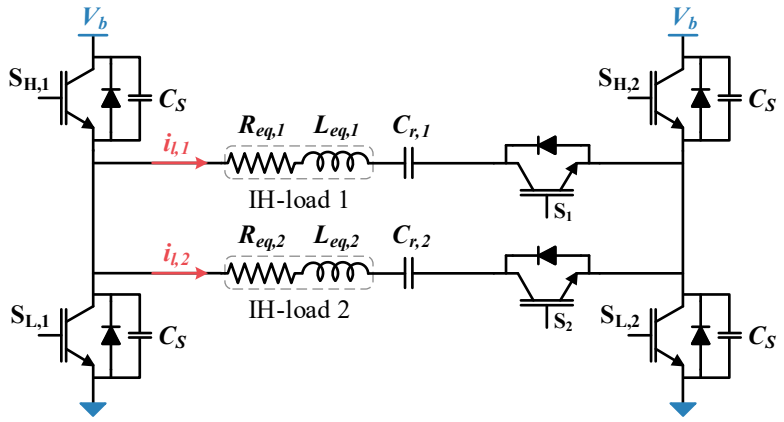


Fig. 1.32. Multi-output common-FB inverter with load-series transistor.

In order to obtain similar performance and device count without the need of high current rating in the common block, a time-sharing inverter is proposed in [118]. The converter, derived from the single switch topologies, can be seen in Fig. 1.33 and it is operated by phase shift control. Even though this topology presents low power device count, it requires the presence of relays to disconnect the inactive loads.

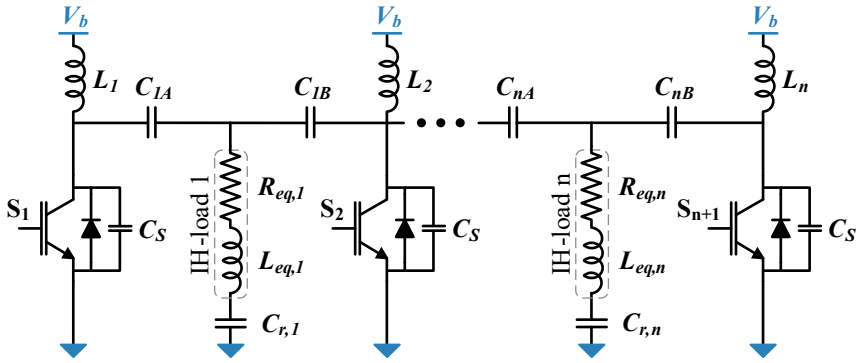


Fig. 1.33. Multi-output SE-derived time-sharing inverter.

1.4.3. Multi-output topologies challenges

After analyzing the most relevant topologies proposed in recent years, a comparison of the different topology groups based on its main characteristics is performed in TABLE 1.1. In general, multi-output inverters present a higher load maximum deliverable power and better power controllability. This performance is a consequence of the lower relevance of the base topology in the design process, as it can be inferred from the fact that most of the solutions are proposed based on more than one inverter: FB and HB or SE and HB.

TABLE 1.1. POWER CONVERTER GROUPS COMPARISON

	INVERTER PARALLELIZATION	LOAD MULTIPLEXATION	MULTI-OUTPUT TOPOLOGIES
Power control	++	−−	+
Device count	−−	++	+
Acoustic noise	+	−−	++
Mains power consumption	++	−−	+

Moreover, TABLE 1.2 compares the detailed topologies according to the required power device number, parametrized as a function of the number of loads, *n*. Additionally, this table presents the normalized mean power column which represents the maximum power, as a percentage of the power at the resonant frequency, i.e. the maximum available power, that is possible to transfer to a load while maintaining power control. This result is averaged between all the active loads.

As it can be seen, the latest developments in multi-output inverters outperform the classical single-output topologies. On the one hand, the parallelization of inverters is improved by converters that present simultaneous load activation and independent power control with reduced device count [94, 107-109]. On the other hand, load multiplexation is upgraded by high-frequency noiseless load activation [91, 114, 117].

Based on the presented state of the art, and given the actual commercial approach to induction heating appliances, it is clear the potential of the multi-output structures in the current context of modern induction heating appliances. Research opportunities have to focus on the development of topologies specifically designed for a high number of loads, i.e., higher than 10, and will be linked to:

Electromechanical relay elimination: The relay as a cost-effective alternative for reconfiguration of load and inverter connection is the main reason for its usage in commercial cooktops. However, they present significant drawbacks such as high settling times, noisy switching and limited life-time. In the literature, multi-output solutions eliminate them at the cost of degrading the current path and increasing the device count.

Thus, a future challenge is the prospection of inverter alternatives that minimize the solid-state devices in the current path.

TABLE 1.2. TOPOLOGY DEVICE COUNT AND POWER CONTROL COMPARISON

TOPOLOGY	POWER DEVICES			NORMALIZED MEAN POWER
	TRANSISTOR	*RELAY*	*DIODE*	
Parallel FB [54-57]	$4n$	0	4	1[a]
Parallel HB [48-53]	$2n$	0	4	1[ab]
Parallel SE [43-47]	n	0	4	1[a]
Multiplexed FB	4	n	4	$< (n\text{-}1)/n$
Multiplexed HB [101, 103]	2	n	4	$< (n\text{-}1)/n$
Multiplexed SE	1	n	4	$< (n\text{-}1)/n$
F. Forrest [28]	2	$n^2/2$	4	$1/n$[a]
S.K. Papani [105]	4	0	4	$2/n$[a]
J.M. Burdío S.H. Hosseini [107]	$2+2n$	0	4	1
S. Zenitani [108]	$2+2n$	0	4	1
H. Sarnago [109]	$2+2n$	0	2	1
H. Sarnago [111]	$2n$	0	2	1[b]
J. Yong-Chae [112]	$1+n$	0	4	$1/n$[c]
V. B. Devara [113]	$4+2n$	0	4	$1/n$[c]
F. Forest [29].(a)	$1+n$	0	4	1[bc]
F. Forest [29].(b)	n	0	4	1
F. Forest [29].(c)	$1+2n$	0	4	1
O. Lucía [114]	$2+n$	0	4	1
S.K. Papani [117] M. Perez-Tarragona [91]	$4+n$	0	4	$(n\text{-}1)/n$
T. Hirokawa [118]	$1+n$	0	4	1

[a] Limited power control due to switching frequency constraints.
[b] Limited power control due to specific IH reasons (ZVS limits, master-slave configuration, etc.)
[c] Lower efficiency current path due to series-connected power semiconductors.

Power device usage balance: In order to increase mean time between failures (MTBF) in the power converter, inverter design without critical components, such as shared inverters, is desired. The power balance is not restricted to a static topology layout but also to dynamic reconfiguration of non-used inverters, as in the case of HB parallelized with relays. The pursuing of these structures with solid state switches will improve the overall performance and reduce the overall inverter failures.

Bus voltage control: The inclusion of low device count PFC or boost structures has proved to increase inverter efficiency and improve mains power consumption. For this reason, the integration of this converters in multi-output inverters improve the performance by reducing the current through the load.

Wide Bandgap (WBG) devices implementation: The development of WBG devices has increased its relevance in induction heating applications [119-121]. Due to its characteristics, the implementation of multi-output topologies with SiC or GaN devices leads to an increased overall efficiency of the converter.

Ad-hoc modulation strategies: The adoption of classical modulation strategies in multi-output converters has proven to result in robust solutions. However, developing new control strategies that adapt to the operation restrictions and possibilities of the different multi-output converters allow better performance in terms of efficiency or power controllability.

1.5. Motivation and structure of this dissertation

The collaboration agreement between the Group of Power Electronics and Microelectronics (GEPM), of the Instituto de Investigación en Ingeniería de Aragón (I3A), and the BSH Home Appliances Group was established in the early 1980s and has led to the development and industrialization of six generations of IH appliances. In this framework, the research presented in this PhD dissertation aim to add to the significant industrial development and academic results responsible of the improved performance of the different generations of IH appliances.

1.5.1. Motivation

Modern home appliances are conceived to be high-performance products that provide a good user experience while achieving high efficiency and robust operation. For this reason, avant-garde developments in domestic induction heating advance towards increased flexibility in the cooktop, reducing the restrictions in the pot size, shape, and position.

The direct pot heating, and thus high efficiency, fast heating, and low glass temperature that results in ease of cleaning and safety are some of the main advantages of IH heating. Complementary, the possibility of load detection by measuring the current shape enables a more transparent interaction between the user and the cooktop. Combining both, the possibility of generating flexible cooking surfaces appears as one of

the main advantages of induction cooktops when compared with other heating technologies. On this scenario, several challenges arise, being the most relevant ones the design of small inductors with high mutual coupling, the development of suitable power converters, and the control of a high number of loads. More specifically, these units require the design of power converters capable of powering a large number of inductors in an efficient, versatile and cost-effective way, while complying with electromagnetic compatibility standards.

In the past, as it has been presented, several alternatives have been provided for the powering of cooktops with an increasing number of inductors, achieving a proper user experience. The inverter parallelization has proven to be the option that achieves better performance even if it requires a high number of power devices. Additionally, the load multiplexation limits the power device count and therefore is the preferred alternative from an industrialization point of view. However, these alternatives fade when translated to flexible surfaces that present a high number of coils. Therefore, research effort has focused on the development of high-efficiency multi-output converters that provide proper solutions to all these requirements [16, 52, 53, 80, 92, 109, 114, 122-129].

Consequently, the main motivation of this PhD dissertation is to contribute to solve these challenges from the electronic design point of view, developing solutions with low power device count and solid-state components implementation, and analyzing their capabilities in the power managing.

1.5.2. Goal definition

The main goal of this research is the design, analysis and optimization of high-efficiency high-performance matrix-based multi-output converters and the development of specific modulation and control strategies to increase their versatility and independent power control with a high number of IH loads.

In order to achieve this, several topologies are introduced, and different control strategies are analyzed simultaneously with the design and building of optimized prototypes.

1.5.3. Scope of the thesis

The following steps are considered in this thesis to accomplish the defined goal:

- Proposal of multi-output inverter topology

Considering the desired features, a matrix-based multi-output inverter is proposed for powering flexible surface induction cooktops. The evaluation of the topology includes its behavioral analysis, based on spice and analytical models, which allows to obtain the independent control parameters. Additionally, all the preceding and derived matrix-based converters are presented.

- Analysis of Modulation strategies

Based on the available independent control parameters, alternative modulation strategies, derived from the classical ones, are proposed to achieve high performance while ensuring safe and efficient operation of the inverter. The control methods are analyzed and developed, considering the optimized design of the topology, the required measurements systems, the control electronics, and the fulfillment of EMC standards.

- Experimental implementation

Several variants of the selected topology are implemented experimentally considering the different alternatives of the modulation strategies. For this, alternatives in the switching technology, snubber networks, or measurement systems are considered. These prototypes present enough versatility to complement the development of each modulation strategy, getting experimental measurements, and testing the proper operation of the converters.

- Discussion and conclusions

The simulations and experimental measurements of every combination of modulation strategy and designed converter allow to draw conclusions of the ideality of the solution.

1.5.4. Report structure

This document is divided into five Chapters. In Chapter 1, the domestic induction heating application has been presented and a review of the state-of-the-art of multi-output inverters has been performed. Chapter 2 presents and describes the new family of matrix-based multi-output resonant converters. Chapter 3 proposes and analyses different modulation strategies to control the selected converter topology. In Chapter 4, the experimental implementation of the multi-output resonant converter and its modulations strategies are described, and the main results are presented. Finally, the main conclusions of this dissertation are outlined in Chapter 5.

Chapter 2

New multi-output matrix-structured inverter topologies

Multi-output converters that share power devices among loads are the most promising topologies for induction cooktops due to their compromise between performance and cost. Among them, matrix structures achieve the greatest possible balance, leading to the minimum device count. Concurrently, unidimensional matrix structures present a slightly higher device count but unparalleled control flexibility, arising as a more valuable solution.

In this chapter the family of new multi-output matrix resonant inverters, designed for the usage on flexible-surface induction cooktops, is presented. An overview of the family and their design and operation principles is performed. The unidimensional ZVS matrix resonant inverter is described based on those principles to highlight its increased versatility that justifies its utilization as the cornerstone of this thesis.

Contents

2. New multi-output matrix-structured inverter topologies

Nowadays, a high number of applications require power converters that provide several voltages or power levels simultaneously. In order to do so, the device count and design complexity of the converter increases, leading to more expensive, and bulky implementations with statistically lower MTBF. This is the main reason why multi-output converters have been a prolific research field in the last decades.

Based on the analysis of the state-of-the-art and the pillars for future multi-output converter developments, topologies that combine high-frequency solid-state load selection with a low device count outperform the classical multi-output implementations. On this scenario, the multi-output converters that share power devices among loads [106, 116] achieve a good trade-off between performance and cost and are the most promising for future domestic IH application.

2.1. Matrix-based inverter topologies

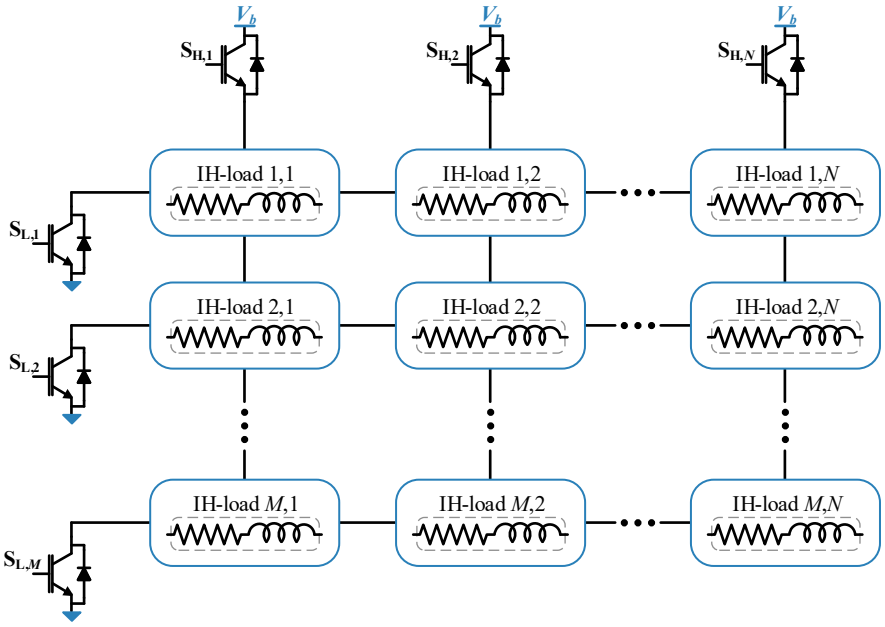


Fig. 2.1. General approach to HB-derived *MxN* matrix converters, being *M* the number of rows and *N* the number of columns.

The greatest available share ratio corresponds with half-bridge-derived matrix structures, presented in Fig. 2.1. This approach presents a row of high-side transistors, $S_{H,j}$, which allow the load connection to the dc-link voltage, and a column of low-side transistors, $S_{L,i}$, connected to ground, enabling powering the induction coils

corresponding to every resulting cell (*i*,*j*). Therefore, in order to implement a *n*-coil appliance the number of switching devices, n_s, can be reduced down to $n_s = 2\sqrt{n}$.

2.1.1. Multi-output ZCS matrix resonant inverter

Based on the aforementioned matrix idea, [130] derives a multi-output ZCS matrix resonant inverter (Fig. 2.2) from the ZCS half-bridge resonant inverter [131]. This approach requires, besides the high-side and low-side switching devices, two additional diodes per load: the series high-side diode, $D_{SH,i,j}$, and series low-side diode, $D_{SL,i,j}$. Their purpose is to block the voltage during the off times and enable independent load activation. As a consequence, it is possible to implement an appropriate modulation strategy that enables each coil independent output power control while ensuring soft-switching ZCS for the complete power range.

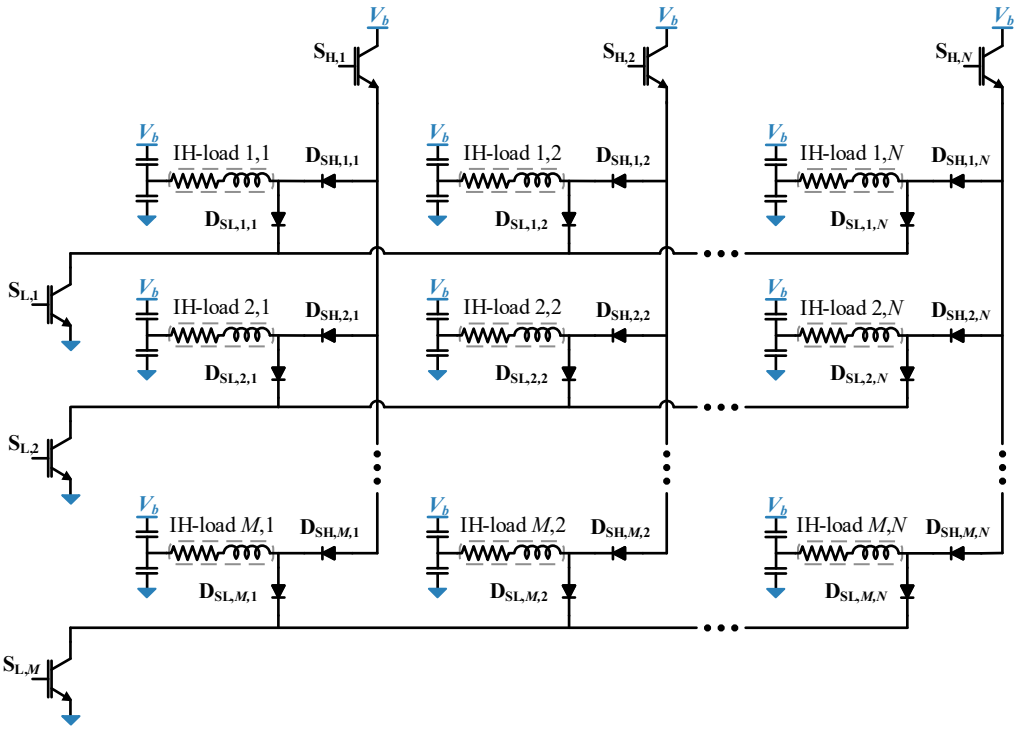


Fig. 2.2. Proposed multi-output *MxN* ZCS resonant inverter, being *M* the number of rows and *N* the number of columns.

In order to apply this modulation strategy, the complementary high-side and low-side transistor activation is required. Thus, the application in a single IH load *i*,*j* is shown in Fig. 2.3. As the associate $S_{H,j}$, $S_{L,i}$, are alternatively activated while the remaining transistors are deactivated, four different scenarios appear for the IH loads in the matrix structure.

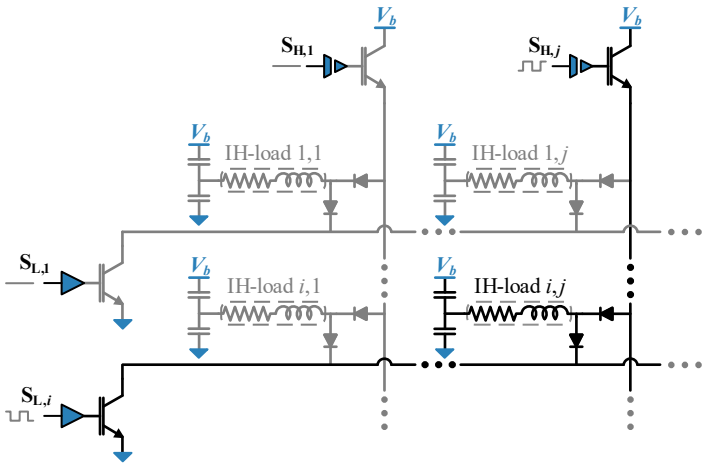


Fig. 2.3. Single load activation for the induction heating load (i, j).

Case A (Fig. 2.4 (a)): Occurs in IH load m,n where $m \neq i$ and $n \neq j$, i.e. the induction heating loads whose corresponding high-side and low-side transistors are deactivated. The transistors block the current path and therefore no current flows through the loads and no power is delivered. The middle point of the split resonant capacitor stabilizes at a voltage equal to half the dc-link voltage, $v_c = V_b/2$.

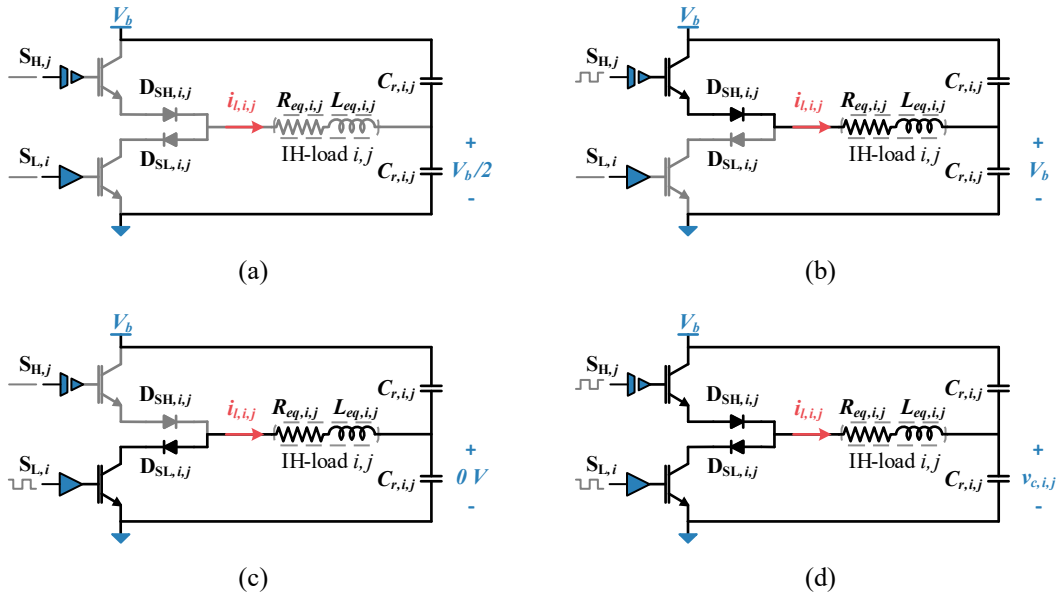


Fig. 2.4. Different scenarios depending on the associate high-side and low-side transistor activations. Unactive load due to both unactive transistors (a), unactive low-side transistor (b) unactive high-side transistor (c) and active load with transistors complementary activation (d).

Case B (Fig. 2.4 (b)): Occurs in IH load m,j where $m \neq i$, i.e. the induction heating loads whose low-side transistor is deactivated and the high-side one is periodically activated. Only a unidirectional path that connects the load with the dc-link voltage is periodically generated. Therefore, the circuit operates as a peak detector and the middle

point of the resonant capacitors is charged to the dc-link voltage. As a consequence, once the middle point voltage reaches steady state, i.e. $v_c = V_b$, the series high-side diode is reverse biased and no current flows through the IH load, leading to a zero output power.

Case C (Fig. 2.4 (c)): Occurs in IH load i,n where $n \neq j$, i.e. the induction heating loads whose low-side transistor is periodically activated and the high-side one deactivated. Symmetrically to the previous case, the middle point of the resonant capacitors is discharged through the low-side transistor unidirectional current path until $v_c = 0$ V. Thus, in steady-state operation no current is flowing through the IH load, and no power is transmitted.

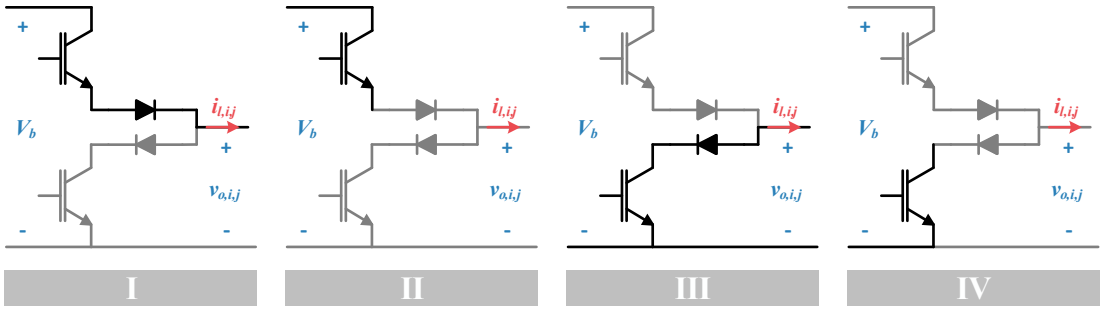
Case D (Fig. 2.4 (d)): Occurs in IH load i,j, i.e. the induction heating load whose low-side and high-side transistors are periodically activated in a complementary manner. In this case, power is transmitted to the induction load. The steady-state operation of the considered modulation strategy to control the transmitted power and ensure ZCS soft-switching commutation is presented in Fig. 2.5.

Initially, the high-side transistor $S_{H,j}$, is activated applying the dc-link voltage to the resonant tank (State I). A resonant current, i_l, flows through $S_{H,j}$ and the series high-side diode, $D_{SHi,j}$, increasing the resonant capacitor voltage, v_{Cr}. The state ends when the current reaches zero and the reverse biased $D_{SHi,j}$ turns off. Therefore, the duration is defined by the natural angular frequency, being $t_I = \pi/\omega_n$.

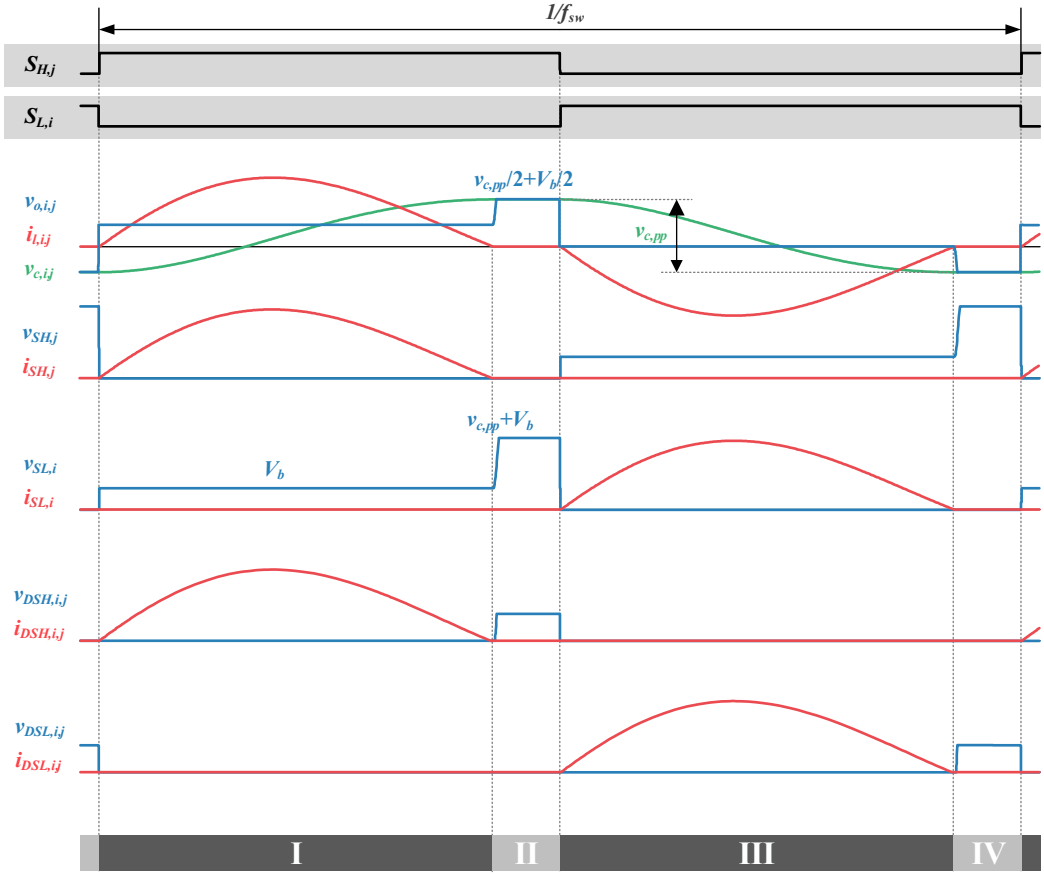
In State II, the current flow is blocked by the series high-side diode. This state duration depends on the column transistor on time and the duration of State I. Therefore, it can be calculated as a function of the duty cycle, D, switching frequency, f_{sw}, and natural angular frequency, resulting $t_{II} = D/f_{sw} - \pi/\omega_n$.

State III operates symmetrically to State I. The low-side transistor is activated, connecting the resonant tank to 0V. Thus, the resonant capacitor voltage is applied to the IH load creating a negative resonant current that flows through the series low-side diode and low-side transistor. When current reaches zero, the diode is deactivated and therefore the duration of this state is the same as *State I*, $t_{III} = t_I = \pi/\omega_n$.

To complete the switching cycle, State IV presents no current flow and therefore the resonant capacitor voltage is stable. This state ends with the high-side transistor activation. The duration of this state is complementary to State II, $t_{IV} = (1-D)/f_{sw} - \pi/\omega_n$.



(a)



(b)

Fig. 2.5. Converter states (a) and waveforms (b) when operating with the proposed modulation strategy. From top to bottom: load current, i_l, resonant capacitor voltage, v_c, high-side transistor voltage and current, $v_{ce,SH}$, $i_{c,SH}$, respectively, low-side transistor voltage and current, $v_{ce,SL}$, $i_{c,SL}$, respectively, series high-side diode voltage and current, $v_{ca,DSH}$, $i_{d,DSH}$, respectively, and series low-side diode voltage and current, $v_{ca,DSL}$ $i_{d,DSL}$, respectively.

With this modulation strategy both during turn-on, i.e. beginning of states I and III, and turn-off, i.e. end of states I and III, ZCS commutation is achieved in the complete power range, ensuring high efficiency.

In order to compute the resulting waveforms, the converter can be analytically modelled. Classically, resonant inverter behavior is approximated by an ideal RLC circuit response to the applied voltage, v_o. Therefore, it can be described as a function of the state

variables in each IH load, i.e. inductor current, i_l, and resonant capacitor voltage, v_c. Additionally, as in the state-of-the-art inverters, v_o in the proposed converter presents a dependency with the current path being able to take values of V_b and 0 V, making it a switched system.

In this thesis, the Fourier approach is used due to the possibility of discerning the contributions of the different harmonics. This way the precision of using the values of the equivalent parameters, L_{eq} and R_{eq}, at the switching frequency can be considered, as they present a strong dependency on the frequency.

Therefore, by performing Fourier analysis, the resonant capacitor voltage in each IH load $v_{c,i,j}(t)$ can be expressed as

$$v_{c,i,j}(t) = \sum_{h=0}^{\infty} \left(A_{h,i,j} \cos(h\omega_{sw} t) + B_{h,i,j} \sin(h\omega_{sw} t) \right), \tag{2.1}$$

where $\omega_{sw} = 2\pi f_{sw}$ and h is the harmonic number. And, consequently, the output current for each IH load $i_{l,i,j}(t)$ is

$$i_{l,i,j}(t) = \omega_{sw} C_r \sum_{h=1}^{\infty} \left(B_{h,i,j} h \cos(h\omega_{sw} t) - A_{h,i,j} h \sin(h\omega_{sw} t) \right). \tag{2.2}$$

The Fourier coefficients, $A_{h,i,j}$ and $B_{h,i,j}$, can be derived from the load impedance, $Z_{h,i,j}$, defined as

$$Z_{h,i,j} = R_{eq,i,j} + j \left(\omega_{sw} h L_{eq,i,j} - \frac{1}{\omega_{sw} h C_r} \right) \tag{2.3}$$

and the applied voltage,

$$v_{o,i,j}(t) = V_{off,i,j} + \sum_{h=1}^{\infty} \left(A_{V_o,h,i,j} \cos(h\omega_{sw} t) + B_{V_o,h,i,j} \sin(h\omega_{sw} t) \right). \tag{2.4}$$

Therefore, they result

$$A_{h,i,j} = -\frac{B_{V_o,h,i,j} \operatorname{Re}\left(Z_{h,i,j}\right) + A_{V_o,h,i,j} \left(Z_{h,i,j}\right)}{h\omega_{sw} C_r \left|Z_{h,i,j}\right|}, \tag{2.5}$$

$$B_{h,i,j} = \frac{A_{V_o,h,i,j} \operatorname{Re}\left(Z_{h,i,j}\right) - B_{V_o,h,i,j} \operatorname{Im}\left(Z_{h,i,j}\right)}{h\omega_{sw} C_r \left|Z_{h,i,j}\right|}. \tag{2.6}$$

Moreover, since the operation of each IH load is independent, the output power, $P_{o,i,j}$, can be calculated by

$$P_{o,i,j} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_{o,i,j}(t) i_{l,i,j}(t) dt. \tag{2.7}$$

When substituting the Fourier series, the power can be calculated by the contribution of each harmonic as

$$P_{o,i,j} = \sum_{h=1}^{\infty} R_{eq,i,j} I_{l,h,rms,i,j}^2 = \sum_{h=1}^{\infty} \frac{R_{eq,i,j} V_{o,h,rms,i,j}^2}{R_{eq,i,j}^2 + \left(h\omega_{sw} L_{eq,i,j} - \left(1/h\omega_{sw} C_r\right)\right)^2} \tag{2.8}$$

being $I_{l,h,rms,i,j}$ the RMS value of the harmonic h of the current through the load i,j, and $V_{o,h,rms,i,j}$ the RMS value of the harmonic h of the voltage applied to the load.

For the case of the proposed ZCS inverter, in order to achieve both ZCS turn-on and turn-off, the behavior depends directly on the natural frequency of the system. The current flow, i.e. States I and III, present V_b as the applied voltage and a duration equal to the natural frequency. Additionally, the current is zero the remaining time. Similarly, the resonant capacitor voltage remains constant when no current is flowing. Therefore, in order to obtain the maximum ratings of the current and the capacitor voltage, the Fourier coefficients can be derived as the resulting of applying a square waveform of the natural frequency as:

$$v_{o,i,j}(t) = V_{off} + \sum_{h=1}^{H} \left(A_{V_o,h,i,j} \cos\left(h\omega_n t\right) + B_{V_o,h,i,j} \sin\left(h\omega_n t\right) \right), \tag{2.9}$$

Where the average voltage, V_{off},

$$V_{off} = \frac{V_b}{2}, \tag{2.10}$$

and the coefficients, using the angular transformation,

$$\begin{cases} A_{V_o,h,i,j} = 0 \\ B_{V_o,h,i,j} = \dfrac{2V_b}{h\pi} \end{cases} \tag{2.11}$$

And therefore the current through the load, and voltage in the resonant capacitor can be expressed as

$$i_{l,i,j}(t) = \omega_n C_r \sum_{h=0}^{H} \left(B_{h,i,j} h \cos\left(h\omega_n t\right) + A_{h,i,j} h \sin\left(h\omega_n t\right) \right), \tag{2.12}$$

$$v_{c,i,j}(t) = \sum_{h=0}^{H} \left(A_{h,i,j} \cos(h\omega_n t) + B_{h,i,j} \sin(h\omega_n t) \right), \tag{2.13}$$

being

$$\begin{cases} A_{h,i,j} = -\dfrac{2V_b R_{eq,i,j}}{h^2 \pi \omega_n C_r \left({R_{eq,i,j}}^2 + \left(\omega_n h L_{eq,i,j} - \dfrac{1}{\omega_n h C_r} \right)^2 \right)} \\ B_{h,i,j} = -\dfrac{2V_s \left(\omega_n h L_{eq,i,j} - \dfrac{1}{\omega_n h C_r} \right)}{h^2 \pi \omega_n C_r \left({R_{eq,i,j}}^2 + \left(\omega_n h L_{eq,i,j} - \dfrac{1}{\omega_n h C_r} \right)^2 \right)} \end{cases} \tag{2.14}$$

Therefore, the transmitted power with the considered modulation strategy, when the current is flowing is

$$P_{o,i,j,on} = \sum_{h=1}^{\infty} \frac{2R_{eq,i,j} V_b^2 \big/ (h\pi)^2}{R_{eq,i,j}^2 + \left(h\omega_n L_{eq,i,j} - \left(1/h\omega_n C_r\right) \right)^2}, \tag{2.15}$$

And the total power in the switching cycle is

$$P_{o,i,j} = P_{o,i,j,on} \frac{\omega_{sw}}{\omega_n}. \tag{2.16}$$

Therefore, the total output power of the matrix inverter is calculated as the sum of the individual IH coil terms $P_o = \sum_i \sum_j P_{o,i,j}$.

2.1.2. Multi-output ZVS matrix resonant inverter

The previous matrix converter allows a proper independent power control of the different loads. However, the transistors require to block a high voltage dependent of the load characteristics. To solve this issue, a ZVS matrix inverter is developed in [132]. The idea behind this topology is to generate an alternative path for the current when the transistor is deactivated, limiting the blocking voltage to V_b. The resulting structure, presented in Fig. 2.6, includes additional high-side and low-side clamp/freewheeling diodes, $D_{H,i}$ and $D_{L,j}$, placed on each row and column respectively.

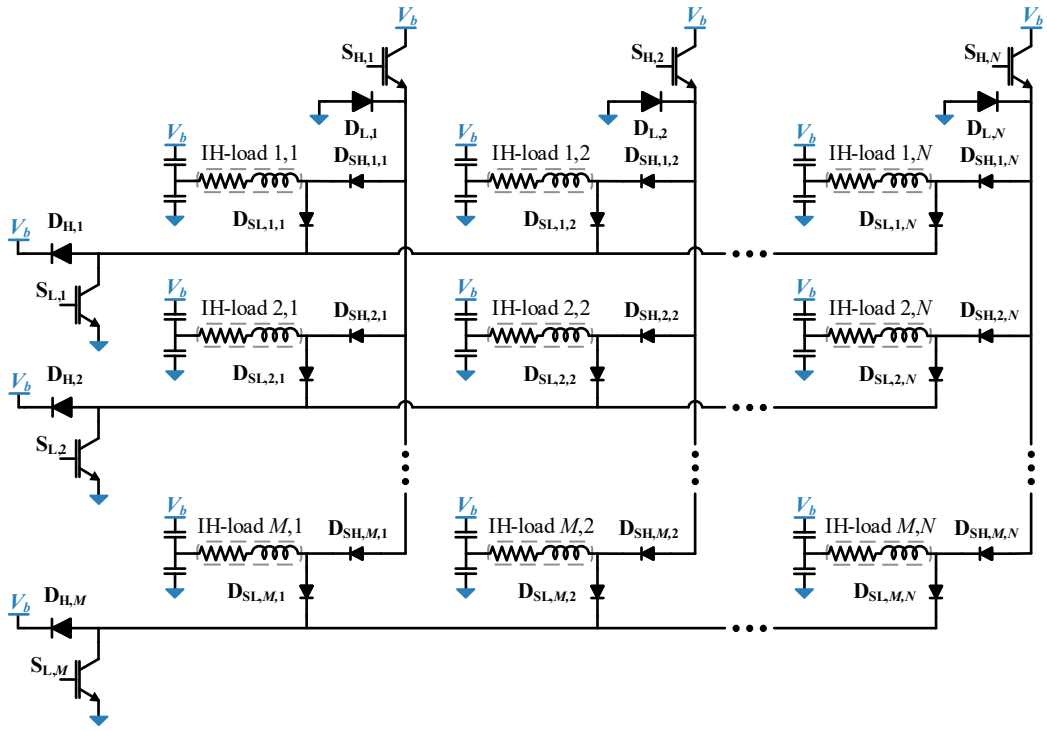


Fig. 2.6. Proposed multi-output *MxN* ZVS resonant inverter, being *M* the number of rows and *N* the number of columns.

Relying on the four possible scenarios presented in the previous subsection and depicted in Fig. 2.7 for the ZVS topology, the inclusion of the clamp/freewheeling diodes generates no alternative current path when the load is intended to be deactivated, i.e. the corresponding high-side transistor, low-side transistor or both are deactivated (Fig. 2.7 (a), (b), and (c)).

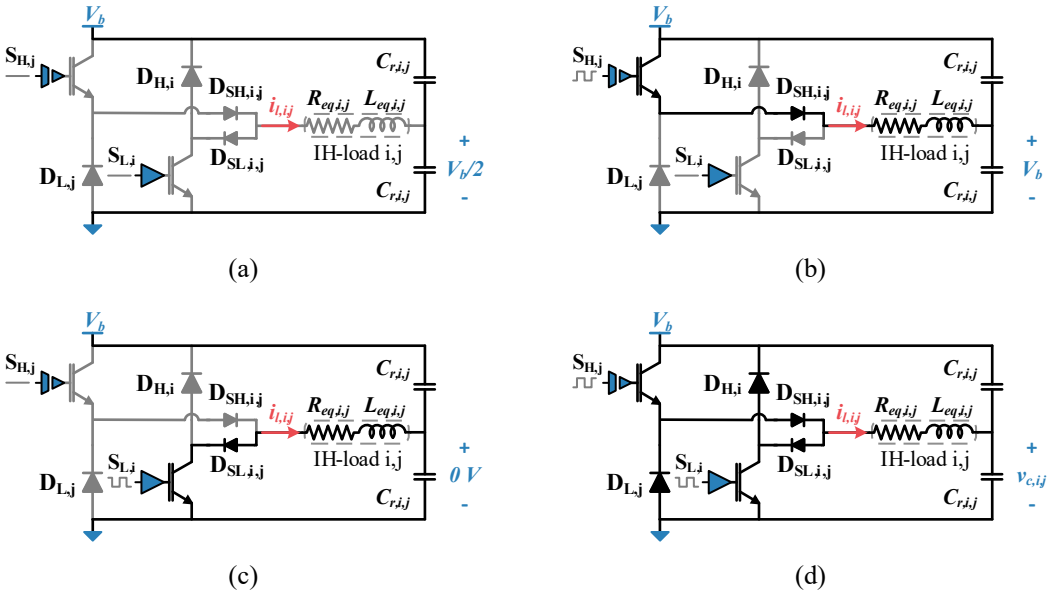


Fig. 2.7. Different scenarios depending on the associate high-side and low-side transistor activations. Unactive load due to both unactive transistors (a), unactive low-side transistor (b) unactive high-side transistor (c) and active load with transistors complementary activation (d).

In the case of both high-side and low-side transistors deactivated, the split resonant capacitor energy flows through the forward biased combination of the series and clamp diodes until the voltage stabilizes to a value between 0V and V_b. When this occurs, both combinations of diodes are reverse biased, and no current path exist (Fig. 2.7 (a)).

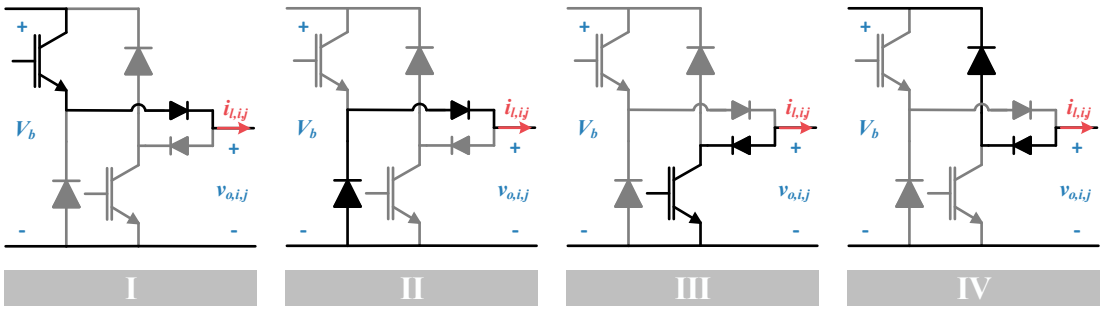
When only the high-side or low-side transistors are activated, the split capacitor middle point voltage is driven to 0 V or V_b respectively. This voltage leads to a combination of series and clamp diode being reverse biased and no voltage difference in the remaining one (Fig. 2.7 (b) and (c)).

For the active load, i.e. the one that presents alternative activation of the low-side and high-side transistors, the operation is similar to a half-bridge series resonant converter [124] (Fig. 2.7 (d)).

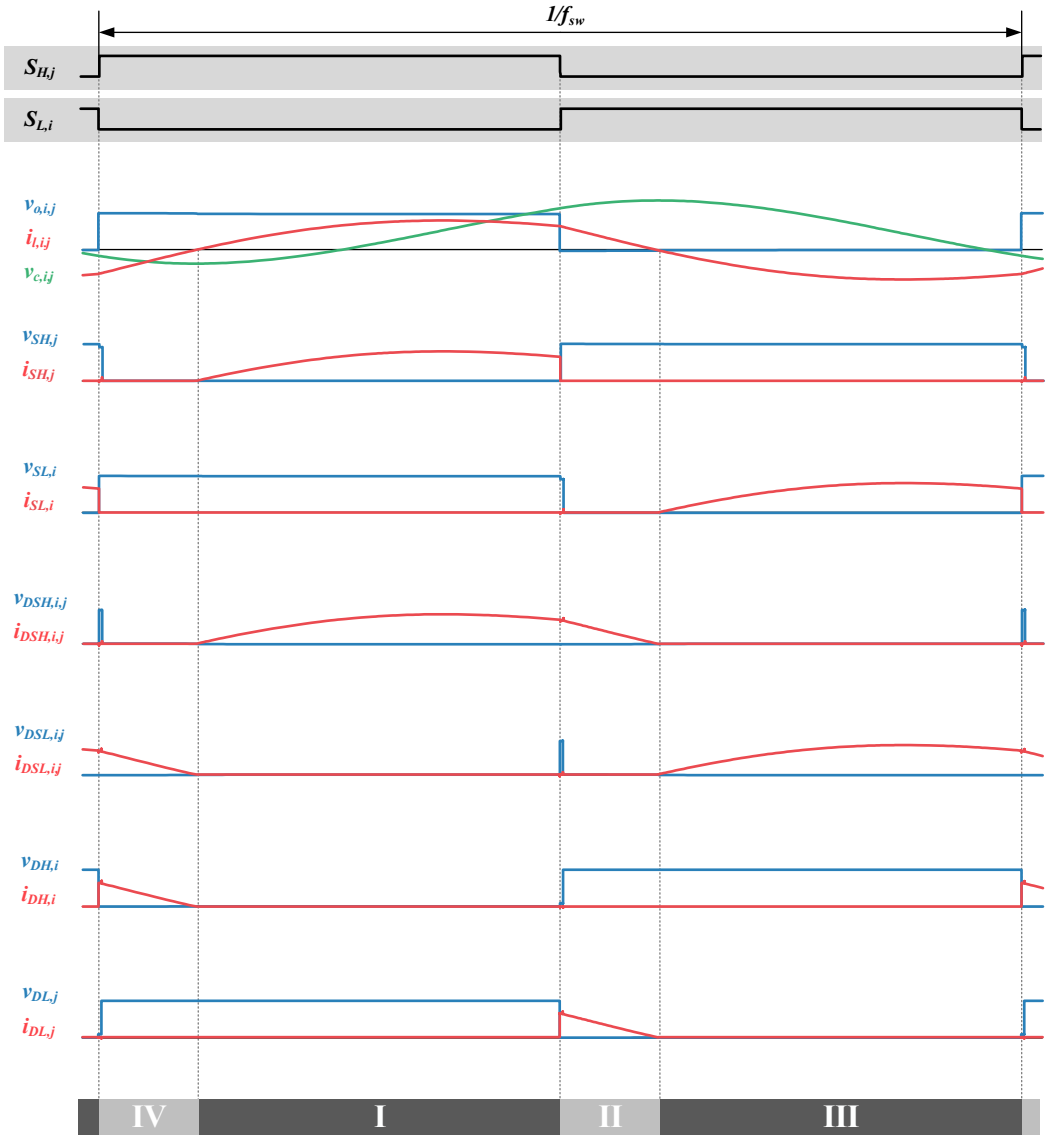
The proposed converter presents soft-switching turn on provided that it is operated above the resonant frequency and, consequently, the transistor turn-on losses can be neglected, leading to a high-efficiency operation. For this case (Fig. 2.8), when the current becomes positive, it flows firstly through the active $S_{H,j}$ transistor, which has been activated under soft-switching conditions. Once $S_{H,j}$ is deactivated, the current flows through $D_{L,j}$ (State II) until the current becomes negative due to the resonant behavior. The negative current flows then through $S_{L,i}$ (State III) until this switch is deactivated and the current flows through $D_{H,i}$ (State IV).

Complementarily, operation below resonant frequency is also possible, achieving transistor ZCS turn-off (Fig. 2.9). In this case, current flows through $S_{H,j}$ when the transistor is activated until it reaches zero (State I). Then, conduction through $D_{L,j}$ (State II) occurs, ensuring high side transistor ZCS turn-off. When $S_{L,i}$ is activated (State III) current flows through it until it reaches zero and the current path changes to $D_{H,i}$ (State IV).

For both cases, the transmitted power can be controlled, depending on the load equivalent parameters, based on the modulation of the switching frequency, f_{sw}, considering a symmetrical duty cycle, $D = 0.5$ [124]. Moreover, due to the presence of $D_{L,j}$ and $D_{H,i}$, the variation in the switching frequency does not only have an influence over the transferred power but also over the waveform.



(a)



(b)

Fig. 2.8. Converter states (a) and waveforms (b) when operating with SW modulation strategy over the resonant frequency. From top to bottom: load current, i_l, resonant capacitor voltage, v_c, high-side transistor voltage and current, $v_{ce,SH}$, $i_{c,SH}$, respectively, low-side transistor voltage and current, $v_{ce,SL}$, $i_{c,SL}$, respectively, series high-side diode voltage and current, $v_{ca,DSH}$, $i_{d,DSH}$, respectively, and series low-side diode voltage and current, $v_{ca,DSL}$ $i_{d,DSL}$, respectively, clamp high-side diode voltage and current, $v_{ca,DH}$, $i_{d,DH}$, respectively, and clamp low-side diode voltage and current, $v_{ca,DL}$ $i_{d,DL}$, respectively.

The square waveform voltage applied is dependent on the switching frequency as:

$$v_{o,i,j}(t) = V_{off} + \sum_{h=1}^{H}\left(A_{V_o,h,i,j}\cos\left(h\omega_{sw}t\right) + B_{V_o,h,i,j}\sin\left(h\omega_{sw}t\right)\right), \tag{2.17}$$

Remaining V_{off} and the coefficients equal as in the previous case, i.e.:

$$V_{off} = \frac{V_b}{2}, \tag{2.18}$$

and

$$\begin{cases} A_{V_o,h,i,j} = 0 \\ B_{V_o,h,i,j} = \dfrac{2V_b}{h\pi}. \end{cases} \tag{2.19}$$

Thus, the current through the load, and voltage in the resonant capacitor can be expressed as

$$i_{l,i,j}(t) = \omega_{sw}C_r\sum_{h=0}^{H}\left(B_{h,i,j}h\cos\left(h\omega_{sw}t\right) + A_{h,i,j}h\sin\left(h\omega_{sw}t\right)\right), \tag{2.20}$$

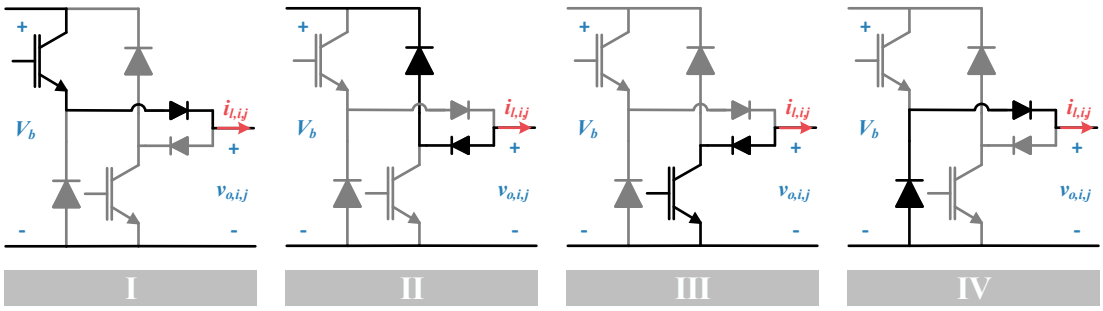
$$v_{c,i,j}(t) = \sum_{h=0}^{H}\left(A_{h,i,j}\cos(h\omega_{sw}t) + B_{h,i,j}\sin(h\omega_{sw}t)\right), \tag{2.21}$$

being

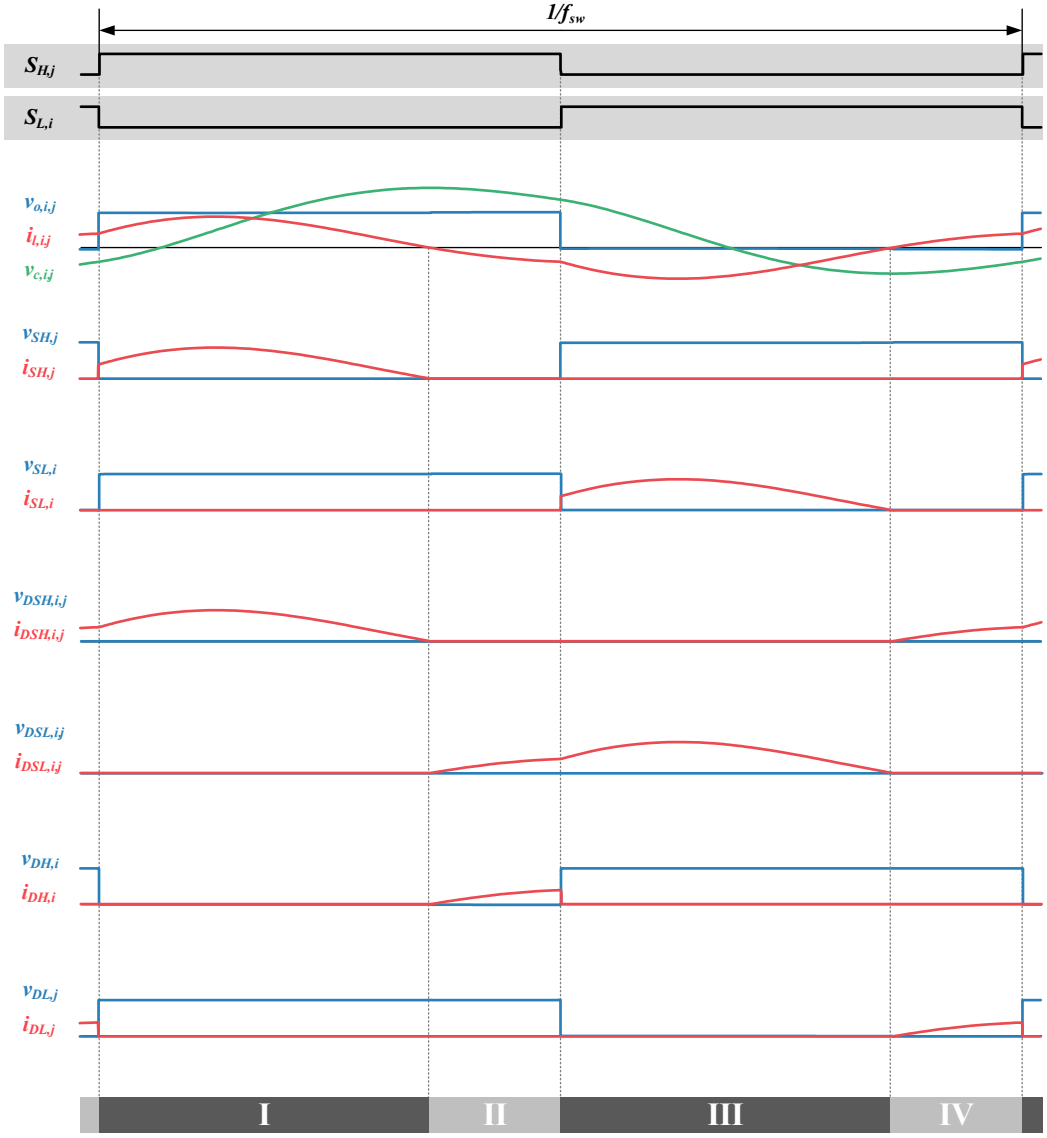
$$\begin{cases} A_{h,i,j} = -\dfrac{2V_bR_{eq,i,j}}{h^2\pi\omega_{sw}C_r\left(R_{eq,i,j}{}^2 + \left(\omega_{sw}hL_{eq,i,j} - \dfrac{1}{\omega_{sw}hC_r}\right)^2\right)} \\ B_{h,i,j} = -\dfrac{2V_s\left(\omega_{sw}hL_{eq,i,j} - \dfrac{1}{\omega_{sw}hC_r}\right)}{h^2\pi\omega_{sw}C_r\left(R_{eq,i,j}{}^2 + \left(\omega_{sw}hL_{eq,i,j} - \dfrac{1}{\omega_{sw}hC_r}\right)^2\right)} \end{cases} \tag{2.22}$$

Finally, the transmitted power based on the calculated current through the load is

$$P_{o,i,j,on} = \sum_{h=1}^{H}\frac{2R_{eq,i,j}V_b^2/(h\pi)^2}{R_{L,i}^2 + \left(h\omega_{sw}L_{r,i} - \left(1/h\omega_{sw}C_{r,i}\right)\right)^2}, \tag{2.23}$$



(a)



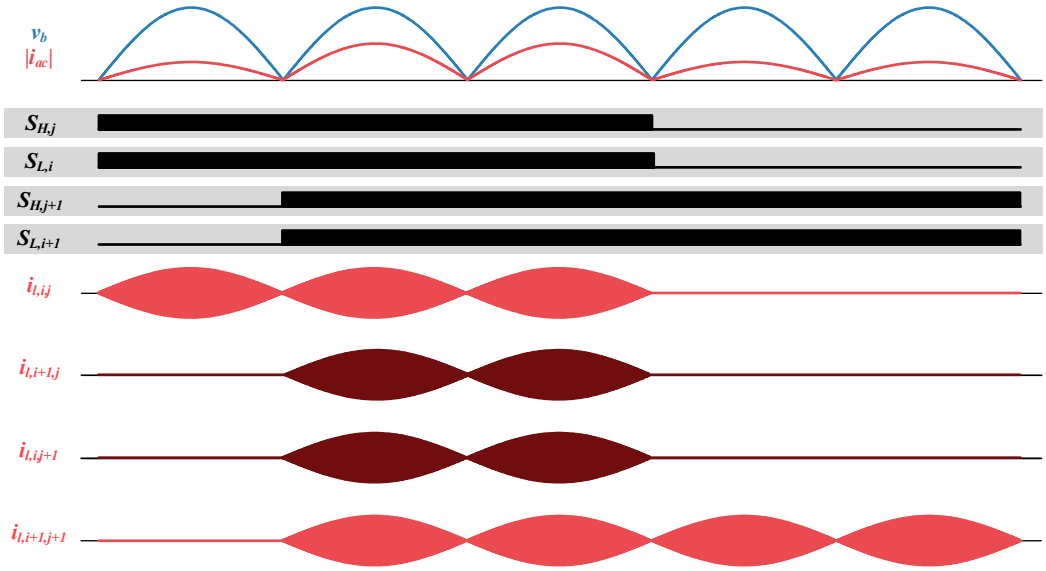
(b)

Fig. 2.9. Converter states (a) and waveforms (b) when operating with SW modulation strategy below the resonant frequency. From top to bottom: load current, i_l, resonant capacitor voltage, v_c, high-side transistor voltage and current, $v_{ce,\mathrm{SH}}$, $i_{c,\mathrm{SH}}$, respectively, low-side transistor voltage and current, $v_{ce,\mathrm{SL}}$, $i_{c,\mathrm{SL}}$, respectively, series high-side diode voltage and current, $v_{ca,\mathrm{DSH}}$, $i_{d,\mathrm{DSH}}$, respectively, and series low-side diode voltage and current, $v_{ca,\mathrm{DSL}}$ $i_{d,\mathrm{DSL}}$, respectively, clamp high-side diode voltage and current, $v_{ca,\mathrm{DH}}$, $i_{d,\mathrm{DH}}$, respectively, and clamp low-side diode voltage and current, $v_{ca,\mathrm{DL}}$ $i_{d,\mathrm{DL}}$, respectively.

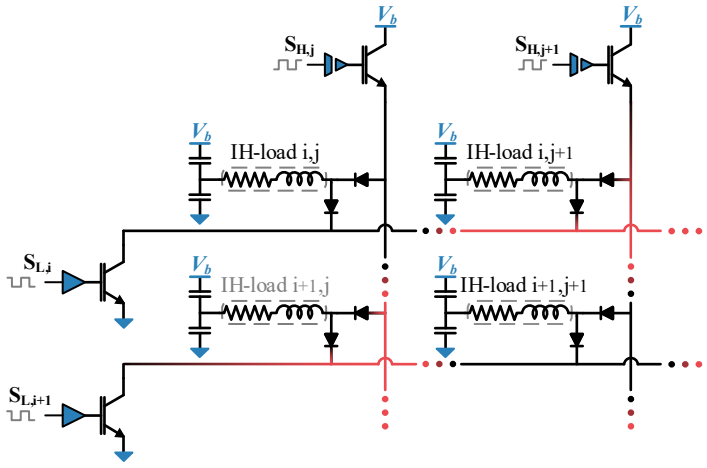
2.2. Single-column matrix-based ZVS resonant inverter

The proposed matrix converters present good operation when considering individual load activation. However, when powering a medium to high number of low-power loads, simultaneous activation is required in order to ensure maximum power transfer.

This operation presents limitations as the loads that present the corresponding $S_{H,j}$ and $S_{L,i}$ transistors active as a result of the remaining loads activation are consequently activated. Therefore, it is not possible to perform diagonal activations, i.e. activate simultaneously loads that do not share the row or column transistors, reducing the available combinations and leading to reduced maximum transmissible power. Fig. 2.10 presents an example of unwanted load activation.



(a)



(b)

Fig. 2.10. Unwanted load activation when activating loads (i,j) and (i+1,j+1). Waveforms (a) and active current paths (b).

Therefore, in order to increase the power control flexibility by preventing unwanted load activations, unidimensional matrix structures, which present an increased independence in the load activation [133], are considered.

Those structures implementation requires $n+1$ switching devices when considering a number, *n,* of IH loads. However, as a result of the unidimensional approach, the independent transistors withstand reduced currents as only the required for a single load flows through it.

2.2.1. Proposed topology

Taking into account this considerations, a ZVS resonant inverter topology is proposed in [134] following a unidimensional matrix structure. This solution is derived from the aforementioned ZVS matrix inverter as it presents greater flexibility in the switching frequency selection while ensuring reduced power losses. Additionally, this proposal presents a column structure as, from a holistic approach, control requirements are lower as there is only a single device that is not referenced to GND, simplifying the driving circuitry.

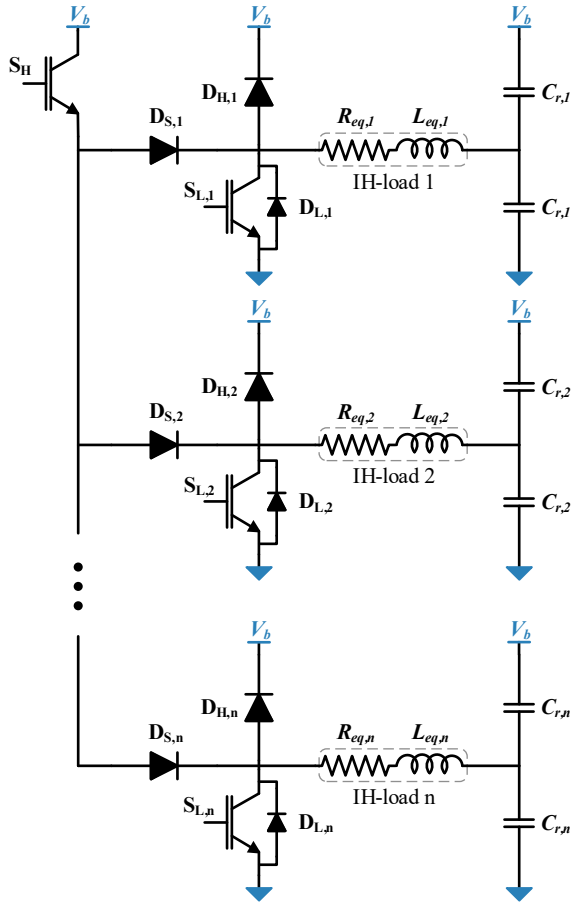


Fig. 2.11. Single-column ZVS matrix resonant converter.

The proposed topology is presented in Fig. 2.11. It is composed of a high-side transistor, S_H, and several output cells, each one of them associated to an IH load. Each cell contains a series diode, $D_{S,i}$, a high-side antiparallel diode, $D_{H,i}$, and a low-side transistor, $S_{L,i}$, with a built-in antiparallel diode, $D_{L,i}$.

Additionally, as the topology is designed to operate above the resonant frequency and in the ZVS region, snubber capacitors can be added in parallel with the low-side transistors, leading to reduced turn-off losses and controlled *dv/dt* (Fig. 2.12).

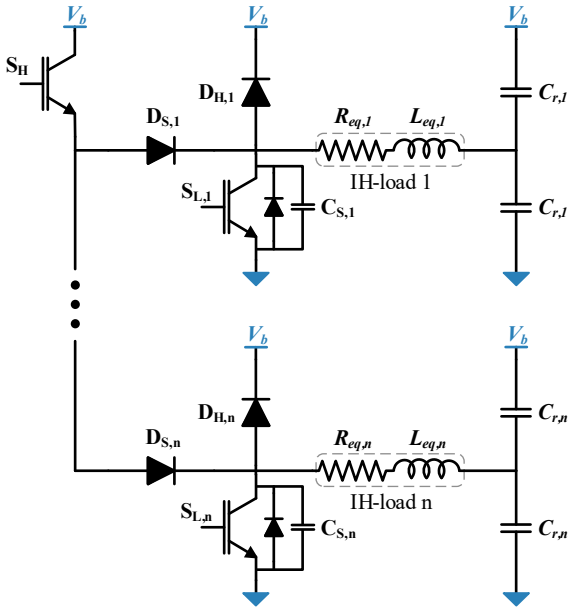


Fig. 2.12. Single-column ZVS matrix resonant converter with snubber capacitances.

2.2.2. Independent load deactivation

As a consequence of the multi-column structure elimination, only two activation scenarios remain. In Fig. 2.13 (a) the case of an unactive load is presented. There, the high-side transistor is being activated and deactivated periodically, leading to the charge of the resonant capacitor middle point to V_b as there is no discharge path. Fig. 2.13 (b), on the other hand, represents an active load with alternative activation of both transistors.

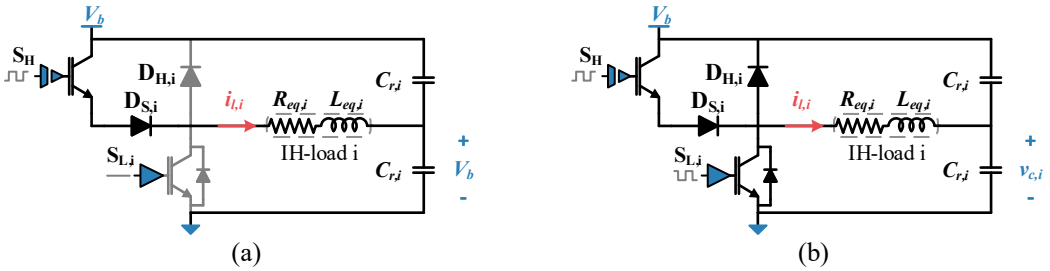


Fig. 2.13. Different operation scenarios depending on the associate lower-side transistor activations when the upper-side transistor is alternatively activated. Unactive low side transistor, and thus unactive load (a) and complementarily activated low side transistor, and thus active load (b).

2.2.3. Control versatility

Enhanced independent control over each inductor is necessary when considering the overall behavior of flexible surfaces. As previously discussed, their purpose is to ease the placement of pots of any shape and any size in any position in the cooktop. Therefore, not only pots of different materials, but also partially covered inductors, with different coupling between the inductor and the pot and thus different R_{eq} and L_{eq}, are to be powered with the same inverter. That means that different power requirements might not be only set by the user for the different pots, but also by the appliance in order to produce an even heating of the pot.

Therefore, one of the most relevant aspects of suitable IH multi-output topologies is the versatility in the independent power control, presenting a high number of degrees of freedom that can be used to implement variations of the classical control strategies presented on Chapter 1.

The degrees of freedom to configure the possible modulations of the ZVS unidimensional matrix inverter can be seen in Fig. 2.14. There, the parameters can be classified in two different groups: general parameters and individual parameters.

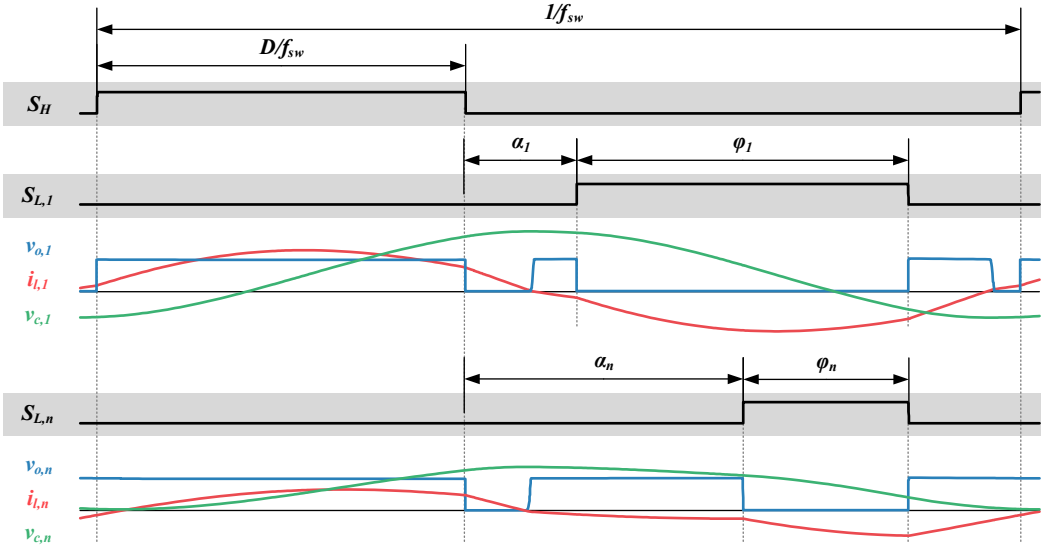


Fig. 2.14. Transistor activation parameters to define the modulation strategies.

The general parameters are the ones that affect to all the IH loads simultaneously. Those parameters are presented related to the high-side transistor but their influence sets boundaries in the low-side-transistor individual parameters.

- The switching frequency, f_{sw}, presents a high influence over the resonant circuit performance by selecting the system gain and the load inductive or capacitive behavior. Both are a function of each load equivalent parameters, leading to different operation depending on the characteristics of the load. Additionally, switching frequency also affects the load equivalent parameters values. It sets the boundaries of the maximum sum of high-side transistor and low-side transistor active time.

- The duty cycle, D, represents the fraction of switching period that the high side transistor is active. When D = 0.5 Square Waveform operation is expected, but the asymmetry leads to reduced power transfer. The combination of duty cycle and switching frequency set the boundaries of the low-side transistor active time.

The individual parameters are the ones related to the low-side transistor. They present influence only over the transistor-connected load:

- Activation width, φ_i, represents, symmetrically with D, the fraction of period that the low-side transistor is active. For the case where $\varphi_i = 1\text{-}D$ Asymmetrical Duty Cycle operation is achieved. However, when $\varphi_i < 1\text{-}D$, a Non-Complementary modulation strategy is applied. $\varphi_i = 0$ represents load deactivation, therefore leading to Pulse Density Modulation strategies, that can present high or low frequency implementations (Fig. 2.15).

- Activation delay, α_i, appears when $\varphi_i < 1\text{-}D$. It represents the time between the high-side transistor deactivation and the low-side transistor activation. When $\alpha_i + \varphi_i < 1\text{-}D$, an additional time between the low side transistor deactivation and the high side transistor deactivation appears.

Therefore, those four parameters allow the independent power transmission to the different IH loads.

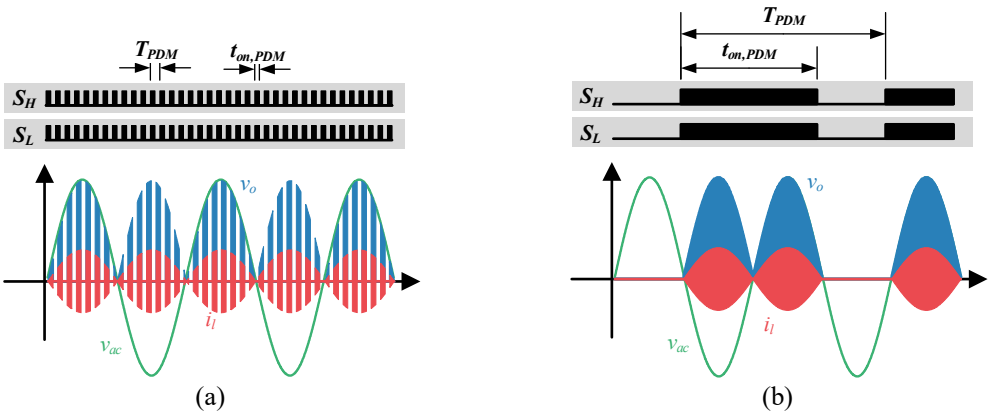


Fig. 2.15. High-frequency Pulse Density Modulation (a) and Low-Frequency Pulse Density Modulation (b).

Chapter 3

Multi-Output Modulation Strategies

Independent power control of each IH load connected to the inverter can be achieved by several modulation strategies. These strategies have to be versatile enough to provide the desired power simultaneously to loads that present different equivalent parameters or whose equivalent parameters vary during operation, leading to mismatches among the resonant circuits.

In this chapter, the modulation strategies that allow controlling the proposed ZVS multi-output resonant inverter are presented and analyzed. The main constraints when designing a modulation strategy are considered and solved for the different alternatives. Additionally, closed loop considerations to implement the modulation strategies are described and simulated.

Contents

3. Multi-Output Modulation Strategies

The proposed unidimensional ZVS matrix resonant multi-inverter presents a wide range of degrees of freedom that allow several modulation and control strategies. In this chapter, they are classified based on the approach and analyzed taking into account their capabilities.

3.1. Design and evaluation of control strategies

The design of control strategies must be performed considering the special operation characteristics of domestic IH. These specific considerations impose critical constraints to the multi-load control algorithm design that can be divided in three main groups: adequate multi-load operation, user experience, and EMC regulations.

3.1.1. Multi-load operation

Domestic IH environment presents a relatively high number of actors, being of special relevance the symbiotic relation between cooktop and pot manufacturers. Even if this association results in induction heating pots achieving a proper cooking performance, several designs are currently used by the manufacturers, leading to different pot materials and building structures, which present a high influence over each IH-load equivalent parameters.

Additionally, inductor distribution on flexible surfaces aims to reach a wide range of pot positions, fulfilling, at least, all the classical hob positions. Therefore, the shapes of the inductors, which allow to tessellate the surface, include circular [137], rectangular [29], hexagonal, and oval [87], and the size is selected in order to power small pots while obtaining a good coupling.

As a consequence, not only pots of different materials, but also partially covered inductors, with different coupling between the inductor and the pot, and thus different $R_{eq,i}$ and $L_{eq,i}$, are to be powered simultaneously with the same inverter in order to provide the user required power level to each pot.

3.1.2. User experience

User experience encompasses the perception by the user of the cooktop operation. It includes a wide range of subjective opinions and perceived features, but the modulation

strategy design can impact positively in three: acoustic noise, boiling perception, and even pot heating.

The absence of acoustic noise is necessary for the optimal usage of the cooktop in the home environment. Classically, the inverter operation outside of the audible range (20 Hz - 20 kHz) has been considered critical. However, considering the possibility of power pulsation, an additional constraint has to be taken into account. The connection and disconnection of the different IH-load produces a variation on the Lorentz forces depending on the bus capacitor charge at the moment, which generates a vibration on the pot and therefore acoustic noise [138-140].

The boiling perception is also associated with power pulsation, mainly when high multiplexation period is used. This problem arises as the counterpart of one of the main advantages of induction heating. As the heat is produced directly on the pot, the thermal inertia of the system is reduced, leading to high ripple in the pot temperature with the alternative powering and disconnection of the IH load, and therefore alternative boiling.

The last constraint is related with the absence of restrictions for pot positioning, which prevents the final user from being aware of inductor coverage areas leading to partially covered inductors with different coupling between the inductor and the pot and, consequently, different supplied power when each pot is operated as a unit.

3.1.3. Electromagnetic compatibility

Electromagnetic compatibility (EMC) regulations impose some constrains to the behavior of the electronic apparatus to ensure the proper operation and interrelation between them when connected to the same mains. The most restrictive regulations when designing the modulation strategy are voltage variation among the different mains half cycles, i.e. flicker [99], and low frequency harmonics [141].

Flicker considers the instability of the light emitted by a bulb due to variations in the mains voltage, depending on the severity and frequency of occurrence. Thus, when fast inductor activation and deactivation is performed to minimize the impact on the thermal inertia of the pot this restriction is highly relevant. Considering the test setup described in [99], the maximum voltage drop, $V_{d,max}$, can be transformed to power variation, ΔP_{in}, taking into account the equivalent mains resistance, R_A, and considering unity power factor for the inverter as

$$V_{d,\max} = \frac{\Delta V_{ac,rms}}{V_{ac,rms}} = \frac{\left|\Delta I_{ac,rms} R_A\right|}{V_{ac,rms}} = \frac{\left|\Delta P_{in} R_A\right|}{V_{ac,rms}^{\ 2}} \tag{3.1}$$

$$\Delta P_{in} = V_{d,\max} \frac{V_{ac,rms}^{\ 2}}{R_A} \tag{3.2}$$

being $\Delta V_{ac,rms}$ the RMS mains voltage and $\Delta I_{ac,rms}$ the RMS mains current variations between a mains half-cycle and the previous one.

Furthermore, pulsating power may affect low frequency harmonic contribution due the current consumption not being consistent for the whole mains cycle.

Additionally, low frequency harmonics present a big dependency on the physics of the IH load. The material penetration depth, $\delta = 1/\sqrt{\pi f \mu_r \sigma}$, changes with the frequency, f, conductivity, σ, and material permeability, μ_r, that is dependent on the magnetic flux, ϕ, meaning that it is not constant but varies with the coil current [142]. Considering a typical home appliance implementation, this current depends, among other factors, on the voltage applied to the IH load by means of the inverter, which equals the rectified mains voltage if the bus capacitor value is low enough, i.e. the power factor is close to unity. As a consequence, the penetration depth fluctuates along the mains cycle and, consequently, the IH load seen by the inverter varies [143].

This issue is a major concern when taking into account that is the final user the responsible to select the pot. A typical solution considered in the literature relies in using an offline calculated frequency sweep to compensate the aforementioned THD [66, 144-146]. Additionally, several topologies have been proposed in the literature to integrate the PFC stage in the inverter [108, 147-153] or externally [38-40, 154-156], leading to bulky solutions.

3.2. Classification of modulation strategies

The proposed converter can be controlled by means of two different multi-output modulation strategy sets, that can be classified according to the operation of all the active loads: pulsating solution and continuous solution.

The pulsating solution relies on the temporal connection and disconnection of the loads in order to provide the required power. Contrary to the literature, that aims to minimize the alternative activations [157], this multiplexation strategy takes advantage

of the solid-state implementation and focuses on minimizing the total power variation among the activations, to decrease greatly the power averaging period.

The continuous solution uses the low side transistor active time to control the resonant capacitor discharge and therefore the transmitted power to each of the loads, leading to reliance on non-complementary transistor activation. Several alternatives in the parameter combination have been considered in order to analyze its implications in the inverter operation.

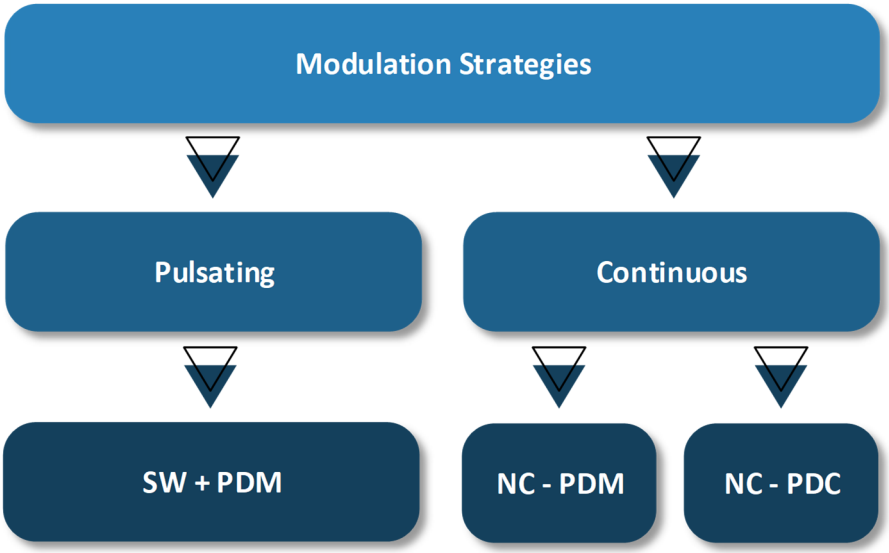


Fig. 3.1. Modulation strategies classification as a function of the operation mode.

3.3. Pulsating modulation strategy

As presented, the pulsating modulation strategy is based on the alternative activation of the different connected loads, making it a load multiplexation strategy. Therefore, it combines modulation strategies typically used in the half-bridge topology [53], as the presented on Chapter 2, and pulse density modulation (PDM).

These approximations, which increase the degrees of freedom to control the inverter [18, 75, 158-160] while achieving high efficiency for low power requirements [52, 153, 161], are typically analyzed in the literature from two different points of view that are not complementary. These solutions include high frequency PDM operating under constant voltage, which leads to big changes in the Lorentz forces and therefore noisy solutions, and low frequency PDM with minimal activation changes, which are consequence of the presence of electromechanical relays [98] and result in long multiplexation times and boiling perception.

For the case of the ZVS multi-output inverter, the application of those strategies lead to sub-optimal solutions, as the PDM period can be decreased, leading to lower heat ripple over the pot, and the activation can be mains synchronized, reducing the noise. However, the severity of the restrictions on mains power consumption regulations such as flicker [99], low frequency current harmonics [141] increases.

3.3.1. Operation modes

As a consequence of the similar operation of each branch with the half-bridge inverter, the ADC strategy [53] appears as a suitable option to control the output power. The single high-side transistor, S_H, of the inverter forces to set common ADC parameters, i.e. switching frequency, f_{sw}, and duty cycle, D, for all the active cells and thus this strategy has to be calculated to ensure proper inverter operation with loads that present mismatching resonant frequencies. This consideration presents a higher severity when studying the possibility to use capacitive snubber networks to minimize power losses.

On top of the ADC, multiplexation strategy operates each load PDM strategies complementarily to minimize the severity of the restrictions. This technique allows an independent power control over the pots while operating with a constant mains power consumption by taking advantage of the multiple connected loads. Thus, the proposed approach relies in low power pulsation, aiming to decrease the PDM period reducing the averaging times and improving the power control and the thermal performance of the cooktop, leading to an improved user experience.

3.3.1.1. Asymmetrical Duty Cycle

Considering the inverter implementation with capacitive snubbers, ADC modulation strategy requires to operate over the resonant frequency. The main waveforms and states for a single active branch are presented in Fig. 3.2. When the current is positive, it flows through the S_H transistor. When S_H is turned off, the current flows through $C_{s,i}$ (State II) and consecutively through $D_{L,i}$ (State III) when $C_{s,i}$ is charged. As the current becomes negative due to the resonant characteristics, current flows through $S_{L,i}$ (State IV) which presents ZVS turn-on. Once $S_{L,i}$ is deactivated, current flows through $C_{s,i}$ (State V) and $D_{H,i}$ (State VI) until the current becomes positive and S_H is activated with ZVS behavior.

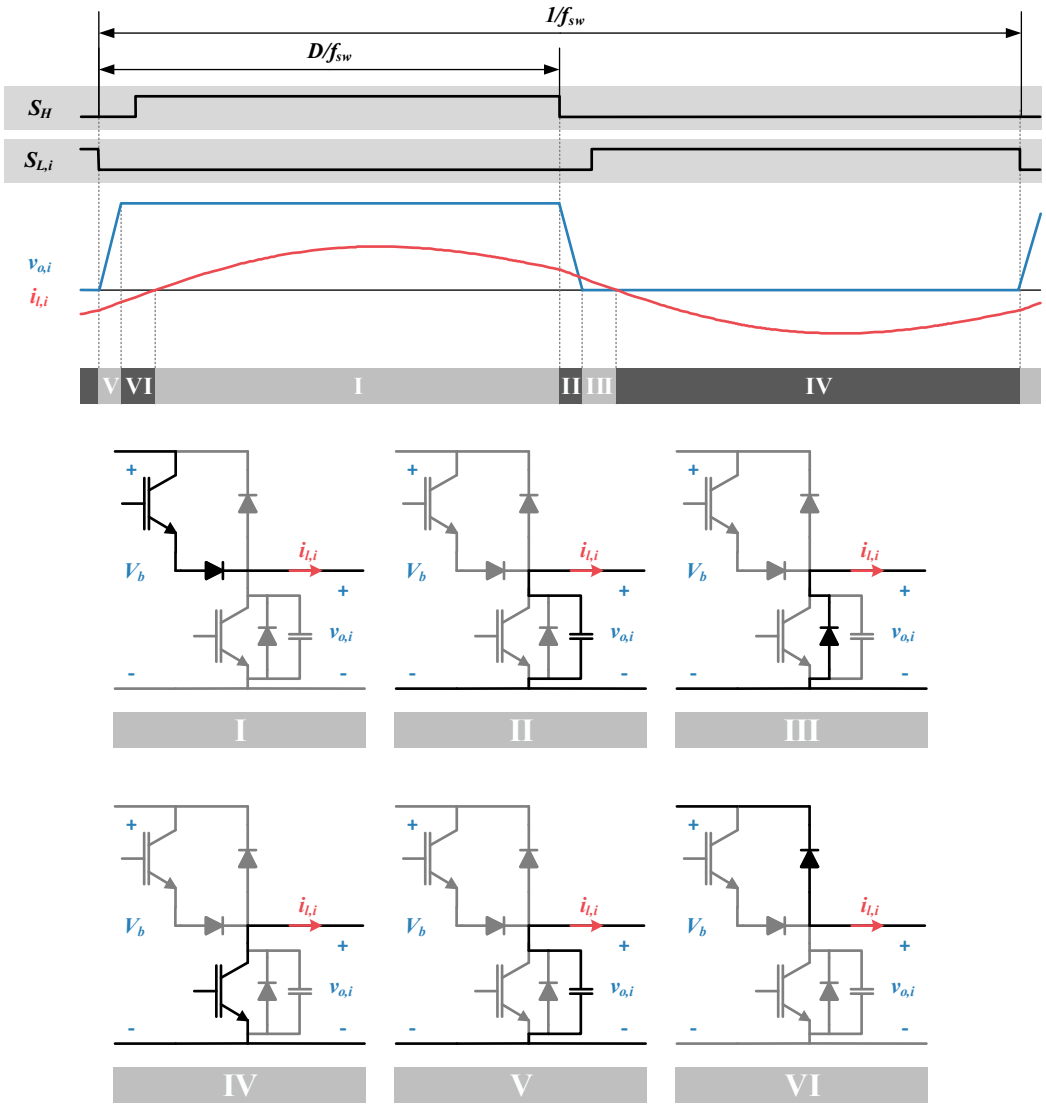


Fig. 3.2. ZVS matrix inverter with additional snubber capacitor main waveforms and circuit configurations for the different states when operating under ADC modulation strategy.

The voltage applied to the load, can be presented as a Fourier series as

$$v_{o,i}(t) = V_{off} + \sum_{h=1}^{H} \left(A_{V_o,h,i} \cos(h\omega_{sw} t) + B_{V_o,h,i} \sin(h\omega_{sw} t) \right), \tag{3.3}$$

with an average voltage, V_{off},

$$V_{off} = V_b D, \tag{3.4}$$

and the coefficients, using the angular transformation,

$$\begin{cases} A_{V_o,h,i} = \dfrac{2V_b \sin(h\pi D)\cos(h\pi D)}{h\pi} \\ B_{V_o,h,i} = \dfrac{2V_b \sin^2(h\pi D)}{h\pi} \end{cases} \tag{3.5}$$

And therefore the current through the load can be expressed as

$$i_{l,i}(t) = \omega_{sw} C_r \sum_{h=0}^{H} \left(B_h h \cos\left(h\omega_{sw} t\right) + A_h h \sin\left(h\omega_{sw} t\right) \right) \tag{3.6}$$

being

$$\begin{cases} A_{h,i} = -\dfrac{2V_b \sin(h\pi D)\cos(h\pi D)\left(R_{eq,i} \tan(h\pi D) + \left(\omega_s h L_{eq,i} - \dfrac{1}{\omega_{sw} h C_r} \right) \right)}{h^2 \pi \omega_{sw} C_r \left({R_{eq,i}}^2 + \left(\omega_{sw} h L_{eq,i} - \dfrac{1}{\omega_{sw} h C_r} \right)^2 \right)} \\ B_{h,i} = \dfrac{2V_b \sin(h\pi D)\cos(h\pi D)\left(R_{eq,i} - \tan(h\pi D)\left(\omega_{sw} h L_{eq,i} - \dfrac{1}{\omega_{sw} h C_r} \right) \right)}{h^2 \pi \omega_{sw} C_r \left({R_{eq,i}}^2 + \left(\omega_{sw} h L_{eq,i} - \dfrac{1}{\omega_{sw} h C_r} \right)^2 \right)} \end{cases} \tag{3.7}$$

This current has to be enough to charge and discharge the snubber capacitor. Given the small load times of the snubber capacitance, the current can be assumed constant, and the minimum necessary current can be derived from the IH load equivalent impedance, $L_{eq,i}$, and the snubber capacitance, C_s, as

$$i_{l,i|off} \geq V_b \sqrt{\frac{C_s}{L_{eq,i}}}. \tag{8}$$

Therefore, it is necessary to calculate the current at the low side transistor turn-off and the proportional part of the high side transistor turn-off

$$i_{l,H|t=D/f_{sw}} = \sum_{h=1}^{H} \left(\frac{2V_b \sin(h\pi D)\cos(h\pi D)}{h\pi \left({R_{eq,i}}^2 + \left(\omega_{sw} h L_{eq,i} - \dfrac{1}{\omega_s h C_r} \right)^2 \right)} \left(R_{eq,i} + \tan(h\pi D)\left(\omega_{sw} h L_{eq,i} - \frac{1}{\omega_{sw} h C_r} \right) \right) \right)$$

$$i_{l,i|t=0} = \sum_{h=1}^{H} \left(\frac{2V_b \sin(h\pi D)\cos(h\pi D)}{h\pi \left({R_{eq,i}}^2 + \left(\omega_{sw} h L_{eq,i} - \dfrac{1}{\omega_{sw} h C_r} \right)^2 \right)} \left(R_{eq,i} - \tan(h\pi D)\left(\omega_{sw} h L_{eq,i} - \frac{1}{\omega_{sw} h C_r} \right) \right) \right) \tag{3.9}$$

Based on this current, the output power of the IH load i, $P_{o,i}$, can be calculated as

$$P_{o,i} = \sum_{h=1}^{H} \frac{2R_{eq,i}V_b^2 \sin^2(h\pi D)/(h\pi)^2}{R_{eq,i}^2 + \left(h\omega_{sw}L_{eq,i} - \left(1/h\omega_{sw}C_r\right)\right)^2}, \tag{3.10}$$

In Fig. 3.3, a plot showing a superposition of the transmitted power and the ZVS regions for different C_s values is presented. There can be seen that switching frequency, f_{sw}, allows ZVS operation in the complete range of power contrary to duty cycle, leading to the disregard of this last.

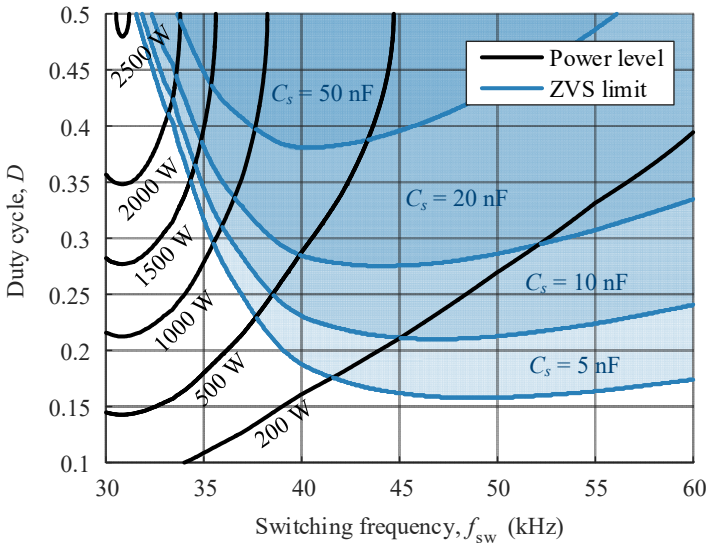


Fig. 3.3. Power levels and ZVS regions for different combinations of D and f_{sw} and different values of snubber capacitors.

3.3.1.2. Multi load HF-PDM

Assuming a common f_{sw} operation for all simultaneously active loads, to provide different power levels, the selective connection or disconnection of the different inductors lead to a power transmission to each of the IH loads comprising the inverter that can be calculated proportional to the active times

$$P_{o,i} = \frac{p_{oi}t_{on,PDM,i}}{T_{PDM}}. \tag{3.11}$$

From a power electronics point of view, this strategy is of direct implementation, being a low frequency pulse density modulation (LF-PDM) strategy a suitable solution. As depicted in Fig. 3.4 this strategy would be synchronized with the mains zero crossing in order to minimize the Lorentz force variation.

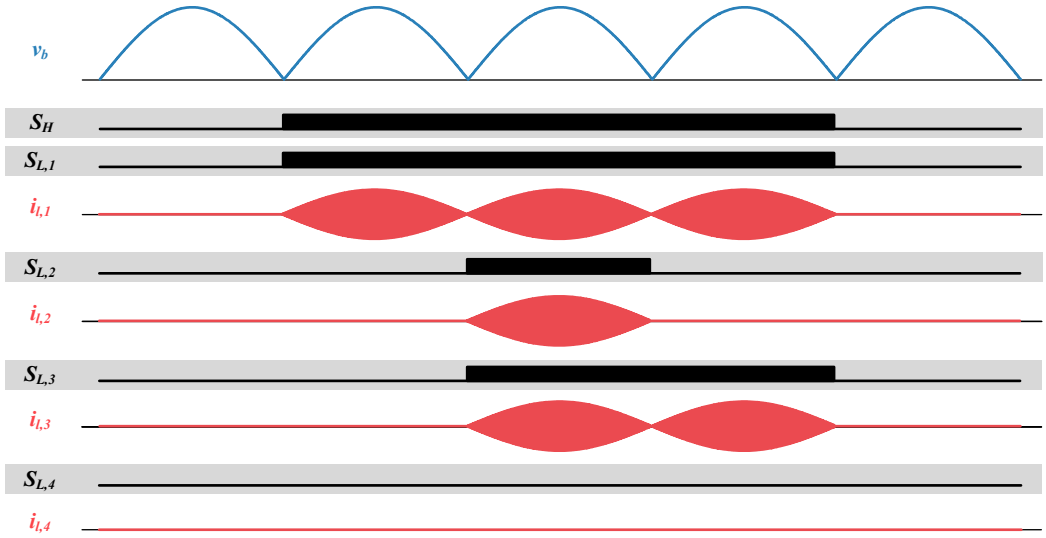


Fig. 3.4. Mains-synchronized PDM strategy.

Additionally, in order to prevent an uneven heating of the pot, each IH load is considered independent and provided a power proportional to the pot area over it [162].

Therefore, for a set of n IH loads, the number of different combinations of inductor activations, that present at least one active inductor, is $k = 2^n - 1$, as the possible inductor states are *on* and *off*. Based on that, and assuming a single operation point for each combination of inductor activations, the IH load power can be expressed as a function of $3k$ parameters: the activation vector, $Act_c = (Act_{1,c}, Act_{2,c}, \ldots, Act_{n,c})$, where $Act_{i,c}$ indicates if the IH load i is active, $Act_{i,c} = 1$, or not, $Act_{i,c} = 0$, in the combination c; the combination switching frequency, $f_{sw,c}$, which is selected as the ADC control parameter while the duty cycle remains symmetrical, $D = 0.5$, leading to SW operation; and the normalized active time of each combination, $d_c = t_{c,on}/T_{PDM}$. Being the equation system to solve the power distribution

$$\begin{matrix} P_{o,1}(f_{sw,1}) \cdot Act_{1,1} \cdot d_1 + & \ldots & + P_{o,1}(f_{sw,k}) \cdot Act_{1,k} \cdot d_k = P_{obj,1} \\ & \ldots & \\ P_{o,n}(f_{sw,1}) \cdot Act_{n,1} \cdot d_1 + & \ldots & + P_{o,n}(f_{sw,k}) \cdot Act_{n,k} \cdot d_k = P_{obj,n} \end{matrix} \quad . \tag{3.12}$$

Moreover, in order to keep at least one inductor active at all times, the extra equation

$$\sum_{c=1}^{k} d_c = 1 \tag{3.13}$$

is to be added.

These equations form a nonlinear equation system. In order to generate a linear equation system and simplify the resolution, the switching frequencies and activations can be selected in advance.

Frequency selection can be done to minimize power pulsation among the mains half cycles. For that, the sum of the n IH loads output power should be the same for all combinations of active inductors, and f_{sw} is selected to achieve that.

$$\begin{aligned} P_{o,1}(f_{sw,1}) \cdot Act_{1,1} + \quad ... \quad + P_{o,n}(f_{sw,1}) \cdot Act_{n,1} = P_{sum} \\ ... \\ P_{o,1}(f_{sw,k}) \cdot Act_{1,k} + \quad ... \quad + P_{o,n}(f_{sw,k}) \cdot Act_{n,k} = P_{sum} \end{aligned} \tag{3.14}$$

where

$$P_{sum} = \sum_{i=1}^{n} P_{obj,i} \tag{3.15}$$

can be obtained through the sum of the n equations in (3.12).

Additionally, this approach sets (3.13) as linearly dependent of the equations in (3.12) and, as a consequence, the number of parameters necessary to solve the equation system is reduced in one. Thus, an analysis to discard some of the combinations might result in faster equation system solution [157].

In order to avoid power limitations and ensure ZVS operation the minimum number of active inductors in each of the selected combinations should be

$$Act_{1,1} + \quad ... \quad + Act_{n,1} = \left\lceil P_{sum} / P_{design} \right\rceil \tag{3.16}$$

where P_{design} is the safe-operation maximum power for any material that the inductor is designed.

This activation choice also improves the efficiency by minimizing the number of active loads and thus increasing the power in each of them, moving the switching frequency closer to resonance.

To prove that the equation system is not overdetermined, the minimum number of parameters, k_{min}, can be expressed as the possible combinations of the active loads and has to be greater or equal than the number of total loads. Therefore

$$k_{\min} = \frac{n!}{\left\lceil P_{sum} / P_{design} \right\rceil! \left(n - \left\lceil P_{sum} / P_{design} \right\rceil \right)!} \geq n \tag{3.17}$$

which is true for $n \geq \lceil P_{sum} / P_{design} \rceil$.

This analysis works properly for IH loads with similar equivalent resonant tank. However, in the case of resonant capacitor miss-match or, given the flexibility of these systems, loads with different equivalent parameters, IH loads may require different operating frequencies to obtain P_{design}. In that case, some of the selected combinations may present power limitations.

In order to solve this problem, without varying the power between mains half cycles, limited combinations may be replaced by a combination with an extra active inductor to increase overall achievable power. This increase in active loads might lead to higher switching frequencies and therefore lower efficiency.

Additionally, for these cases, *flicker* solutions increase the control degrees of freedom. The maximum power variation among mains half cycles is calculated using (3.2) so it does not restrict the pulse density modulation period. As a consequence of the difference in power, the time equation is no longer linearly dependent and therefore an extra parameter is necessary.

3.3.2. Closed loop considerations

In order to implement the closed loop solution of the equation system in (3.12) with the selected combinations, an algorithm that ensures convergence even for underdetermined systems while maintaining $d_c > 0$, and $\sum d_c = 1$ has to be used. With this purpose Gauss-Seidel double randomized algorithm [163] is selected as its operation is not based on the power data manipulation, maintaining its physical sense and, thus, the capability of actualizing said data during operation due to variations in $L_{eq,i}$ and $R_{eq,i}$ equivalent parameters.

However, this algorithm presents a high dependence of the initial seed, $d_{c,0}$. As it can be seen in Fig. 3.5, precomputation of $d_{c,0}$ greatly improves the convergence. From this evaluation it should be noted that precomputations that assume general tendencies in power requirements, even if they are not completely correct, improve greatly the algorithm convergence.

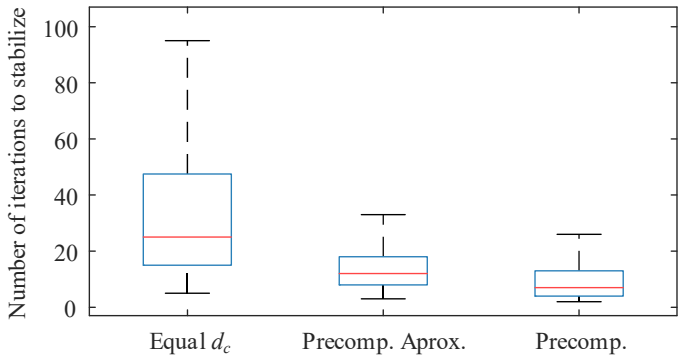


Fig. 3.5. Comparative chart of the number of iterations with different precomputed $d_{c,0}$ values for an unbalanced power requirement, i.e. $P_{obj,1}>P_{obj,2}$. "Equal d" presents the case of $d_{c,0} = 1/\sum c$, "Precomp." present the case of $d_{c,0}$ calculated assuming equal share among the different active inductors in each combination, $P_n(f_{sw,c})=P_{sum}/\sum Act_{n,c}$ and precise objective power levels. "Precomp. Aprox." is calculated with approximated objective power levels, i.e. low, medium, high.

Fig. 3.6 shows the proposed block diagram implementation for the domestic IH system under study. Load identification is performed to achieve useful control information [102], and the target output power selection is externally done by the user. The selection of the combinations of inductor activations is obtained by applying (3.12). The main control block is based on the Gauss-Seidel algorithm operating over the normalized transmitted power, which is actualized in each mains half-cycle.

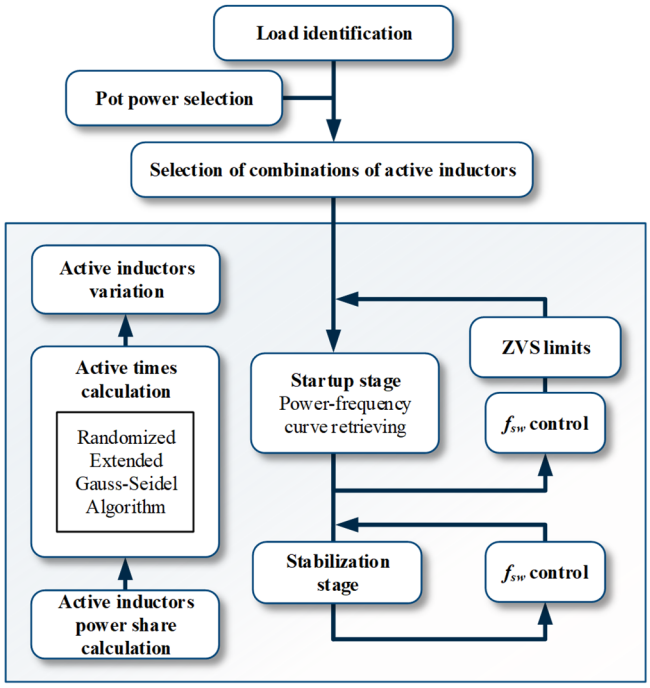


Fig. 3.6. Algorithm integration block diagram.

In order to optimize the operation, a division in the operation core is performed between startup and stabilization. During the startup, the main purpose is to store the

complete frequency-power curve data for all active inductors while providing the maximum percentage of the objective power with a proper power share. During the stabilization part, the transmitted power share should present slight variations as a consequence of pot heating. Additionally, once in stabilization, variations in the output power selected by the user can be recalculated.

3.4. Continuous modulation strategies

Seen the increasing complexity of load multiplexation to fulfill the complete set of constraints, and considering future implementations and regulations that may limit the flexibility of this method, e.g. small appliances powering or a narrowing of the available frequency bandwidth, it is interesting to consider non pulsating power control modes in order to improve cooktop performance.

Considering the available degrees of freedom of the ZVS matrix converter it is clear that ADC modulation does not achieve the necessary independent power control. Therefore, the usage of the low side transistor activation in the fancy of non-complementary modulations appear as a good solution. Those strategies present a highly independent and efficient power control even when operating with different pots simultaneously or partially covered inductors under the same one, allowing even heating of the pot and ensuring the proper converter operation.

3.4.1. Operation modes

The considered non-complementary strategies rely on the common high-side transistor to set the switching frequency and duty cycle, while the activation of the low-side ones will be controlled to transmit the required power. Therefore, the complete set of control parameters is used, as depicted in Fig. 3.7 the high- and low-side transistor gate voltage, and their main modulation parameters can be seen.

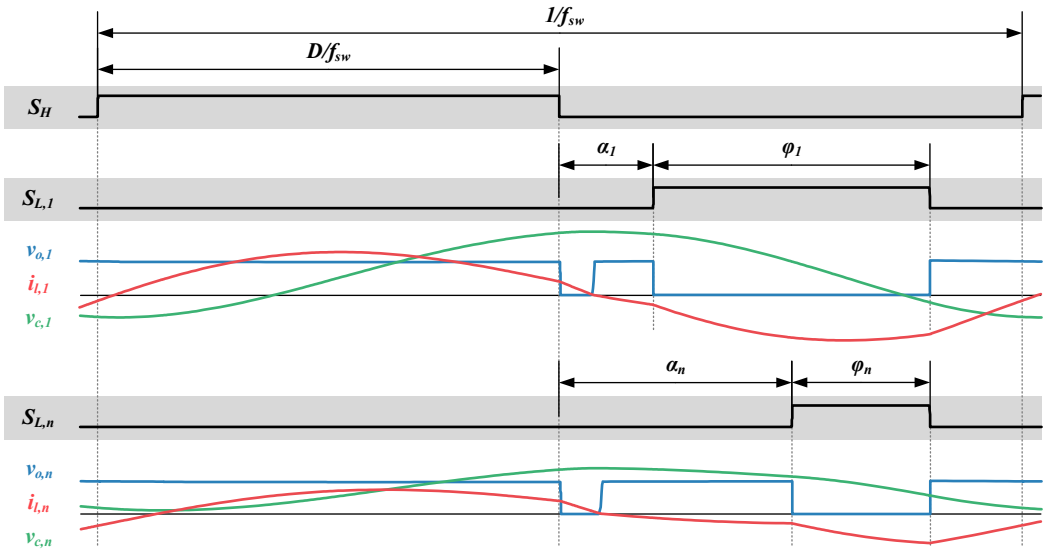


Fig. 3.7. Transistor activation parameters to define the modulation strategies.

In order to reduce the complexity of the control problem and achieve higher efficiency, strategies are derived from the SW operation i.e. the high side transistor is activated with $D = 0.5$. Therefore, the maximum output power is dependent of the switching frequency and the load.

Consequently, power control is achieved by modifying the low side transistor activation. This activation is therefore non-complementary, which means that there is a lag between each transistor deactivation and the activation of the following one. When considering single parameter variation, which facilitates the modulation implementation, two possibilities arise. If the lag is achieved increasing the delay of the activation of the low side transistor, α_i, the modulation strategy is identified as non-complementary pulse delay control (NC-PDC) whereas if the lag is derived of the reduction of the low side transistor conduction time, φ_i, is called non-complementary pulse width modulation (NC-PWM).

In the following section, both strategies are presented and analyzed in order to obtain its main operational parameters.

3.4.1.1. NC-PDC

The low-side transistor activation delay variation enables power control when $t_{\alpha_i} = \alpha_i / \omega_{sw}$ is higher than the current zero crossing time, i.e. the antiparallel diode $D_{L,i}$ conduction time. In Fig. 3.8 the comparison between SW and NC-PDC can be seen.

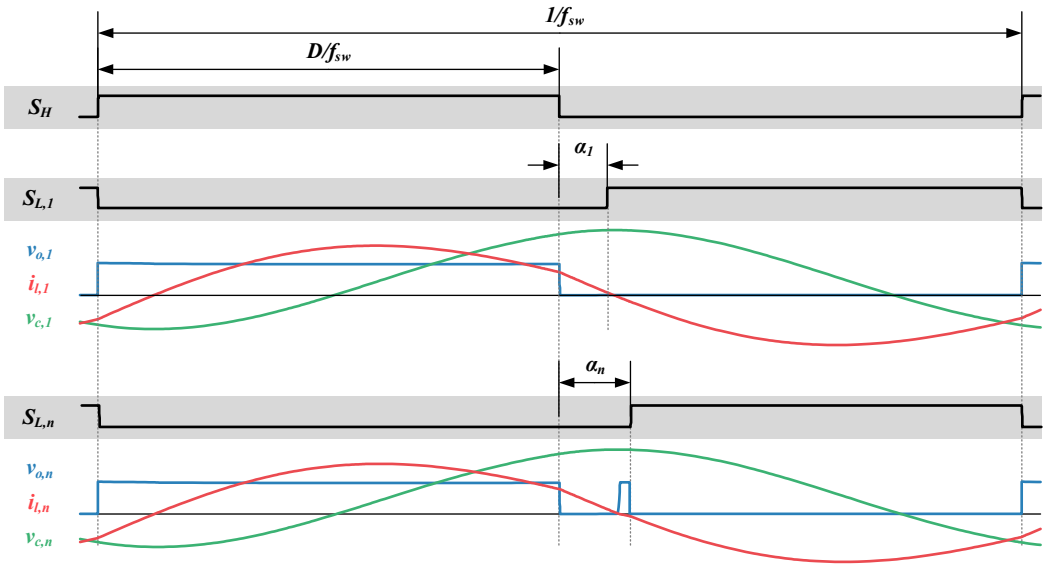


Fig. 3.8. SW operation for $t_{\alpha_i} < t\big|_{i_{o,i}(t)=0}$ and NC-PDC operation when $t_{\alpha_i} > t\big|_{i_{o,i}(t)=0}$.

To obtain this minimum delay, the load-current zero-crossing point can be calculated based on the Fourier series analysis,

$$i_{l,i}(t) = \omega_{sw} C_r \sum_{h=1}^{H} \left(B_{h,i} h \cos(h\omega_{sw} t) - A_{h,i} h \sin(h\omega_{sw} t) \right) = 0, \tag{3.18}$$

assuming first harmonic approximation and square waveform operation as

$$t_{\alpha_i} > t\big|_{i_{o,i}(t)=0} = \frac{\tan^{-1}\left(\frac{B_{h,i}}{A_{h,i}}\right)}{\omega_{sw}} = \frac{\tan^{-1}\left(\frac{\omega_{sw} L_{eq,i} - \frac{1}{\omega_{sw} C_{r,i}}}{R_{eq,i}}\right)}{\omega_{sw}}, \tag{3.19}$$

Summarizing, α_i, expressed in radians, is to be higher than the load impedance argument. As a consequence, power control resolution may be affected, being this aspect more relevant in the high frequency range.

Once $t_{\alpha_i} > t\big|_{i_{o,i}(t)=0}$ is assured, the converter operation in steady state is as described in Fig. 3.9. Current flows through S_H when it is activated (State I). When S_H is turned off, current flows through $D_{L,i}$ (State II) until it reaches zero. Then, due to the resonant nature of the load, $D_{H,i}$ is activated (State III). The stage after the current flows through $D_{H,i}$ depends on the low side transistor activation. For high power, $S_{L,i}$ would activate (State IV) before current through $D_{H,i}$ fades to zero while for low power current can be assumed

to become zero. When $S_{L,i}$ is deactivated, current flows through $D_{H,i}$ (State V) and S_H consecutively (State I).

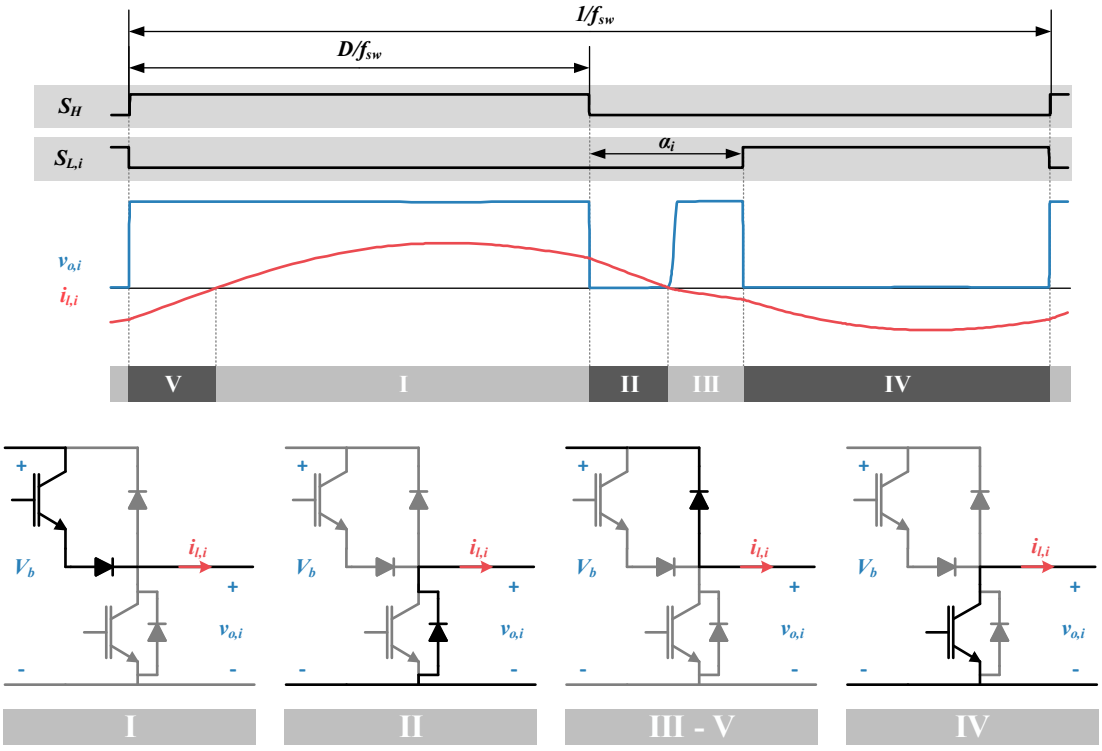


Fig. 3.9. Main waveforms and active devices for the NC-PDC strategy, being v_b the bus voltage, $v_{o,i}$ the voltage applied to the IH load i and $i_{l,i}$ the current through the load.

Ensuring this operation mode, the voltage applied to the load and the current though it can be also obtained by performing Fourier analysis.

The voltage, with $A_{Vo,h,i}$ and $B_{Vo,h,i}$ as Fourier coefficients is of the form

$$v_{o,i}(t) = V_{off} + \sum_{h=1}^{H}\left(A_{V_o,h,i}\cos(h\omega_{sw}t) + B_{V_o,h,i}\sin(h\omega_{sw}t)\right), \tag{3.20}$$

with an average voltage, V_{off},

$$V_{off} = V_b\frac{\pi + \alpha_i - \omega_{sw}t\big|_{i_{o,i}(t)=0}}{2\pi}. \tag{3.21}$$

The coefficients for both voltage and current can be expressed using the angular transformation as

$$\begin{cases} A_{V_o,h,i} = (-1)^h\dfrac{V_b}{h\pi}\left(\sin(h\alpha_i) - \sin(h\gamma_0)\right) \\ B_{V_o,h,i} = \dfrac{V_b}{h\pi}\left(-\cos(h\alpha_i) + \cos(h\gamma_0) - 1 + (-1)^h\right) \end{cases} \tag{3.22}$$

$$\begin{cases} A_{h,i} = \\ -\dfrac{V_{bus}\left(\left(-\cos\left(h\alpha_i\right)+\cos\left(h\gamma_0\right)-1+\left(-1\right)^h\right)R_{eq,i}+\left(\sin\left(h\alpha_i\right)-\sin\left(h\gamma_0\right)\right)\left(\omega_{sw}hL_{eq,i}-\dfrac{1}{\omega_s hC_r}\right)\right)}{h^2\omega_{sw}C_r\pi\left(R_{eq,i}{}^2+\left(\omega_{sw}hL_{eq,i}-\dfrac{1}{\omega_{sw}hC_r}\right)^2\right)} \\ B_{h,i} = \\ \dfrac{V_{bus}\left(\left(\sin\left(h\alpha_i\right)-\sin\left(h\gamma_0\right)\right)R_{eq,i}-\left(-\cos\left(h\alpha_i\right)+\cos\left(h\gamma_0\right)-1+\left(-1\right)^h\right)\left(\omega_{sw}hL_{eq,i}-\dfrac{1}{\omega_{sw}hC_r}\right)\right)}{h^2\omega_{sw}C_r\pi\left(R_{eq,i}{}^2+\left(\omega_{sw}hL_{eq,i}-\dfrac{1}{\omega_{sw}hC_r}\right)^2\right)} \end{cases} \tag{3.23}$$

being $\gamma_0 = \omega_{sw}\, t\big|_{i_{o,i}(t)=0}$.

The transmitted power can be calculated as

$$P_{o,i} = \sum_{h=1}^{H} R_{eq,i}\left(\frac{\hat{I}_{l,h}}{\sqrt{2}}\right)^2 = \sum_{h=1}^{H} R_{eq,i}\frac{\left(\left(A_{h,i}h\omega_{sw}C_r\right)^2+\left(B_{h,i}h\omega_{sw}C_r\right)^2\right)}{2} =$$
$$= V_b{}^2 R_{eq,i}\sum_{h=1}^{H}\left(\frac{\left(1-\left(-1\right)^h\right)\left(\cos\left(h\alpha_i\right)-\cos\left(h\gamma_0\right)+1\right)-\cos\left(h\alpha_i-h\gamma_0\right)}{h^2\pi^2\left(R_{eq,i}{}^2+\left(\omega_{sw}hL_{eq,i}-\dfrac{1}{\omega_{sw}hC_r}\right)^2\right)}\right). \tag{3.24}$$

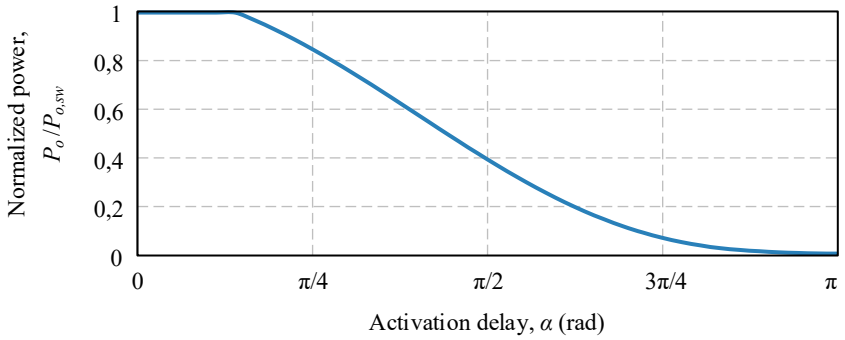


Fig. 3.10. Transmitted power dependency with NC-PDC modulation strategy normalized by SW transmitted power.

3.4.1.2. NC-PWM

For the case of non-complementary pulse width modulation, power control presents a dependency similar to duty cycle variation for high power and for low power, current reaches zero before S_H is activated (Fig. 3.11). Therefore, the power control offers full range resolution.

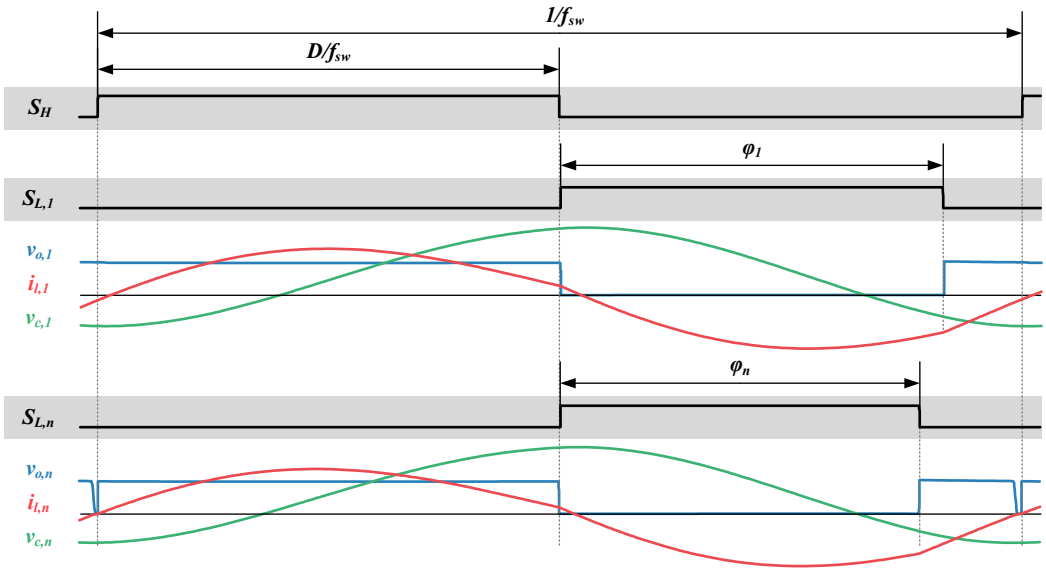


Fig. 3.11. ADC operation for $t_{\varphi_i} > t\big|_{i_{o,i}(t)=0}$ and NC-PWM operation when $t_{\varphi_i} < t\big|_{i_{o,i}(t)=0}$.

The $t_{\varphi_i} = \varphi_i / \omega_{sw}$ for which current flows through $D_{L,i}$ before S_H activation can be calculated assuming first harmonic approximation known that to reach zero current before S_H activation $t\big|_{i_{o,i}(t)=0}$ has to be at maximum $2\pi/\omega_{sw}$,

$$t_{\varphi_i} < t\big|_{i_{o,i}(t)=0} = \frac{\cos^{-1}\left(\dfrac{\omega_{sw}L_{eq,i} - \dfrac{1}{\omega_s C_r}}{\sqrt{R_{eq,i}{}^2 + \left(\omega_{sw}L_{eq,i} - \dfrac{1}{\omega_{sw}C_r}\right)^2}}\right) - \tan^{-1}\left(\dfrac{-R_{eq,i}}{\omega_{sw}L_{eq,i} - \dfrac{1}{\omega_{sw}C_r}}\right)}{\omega_{sw}}, \quad (3.25)$$

The converter steady state operation when $D_{L,i}$ is activated before S_H activation can be seen in Fig. 3.12. Current flows through S_H (State I). Once S_H is turned off, current flows through $D_{L,i}$ (State II). As it is already active, when current crosses zero it flows through $S_{L,i}$ (State III) and, when it is switched off, through $D_{H,i}$ (State IV). Once the current reaches zero, $D_{L,i}$ is activated again (State V) until S_H is switched on (State I).

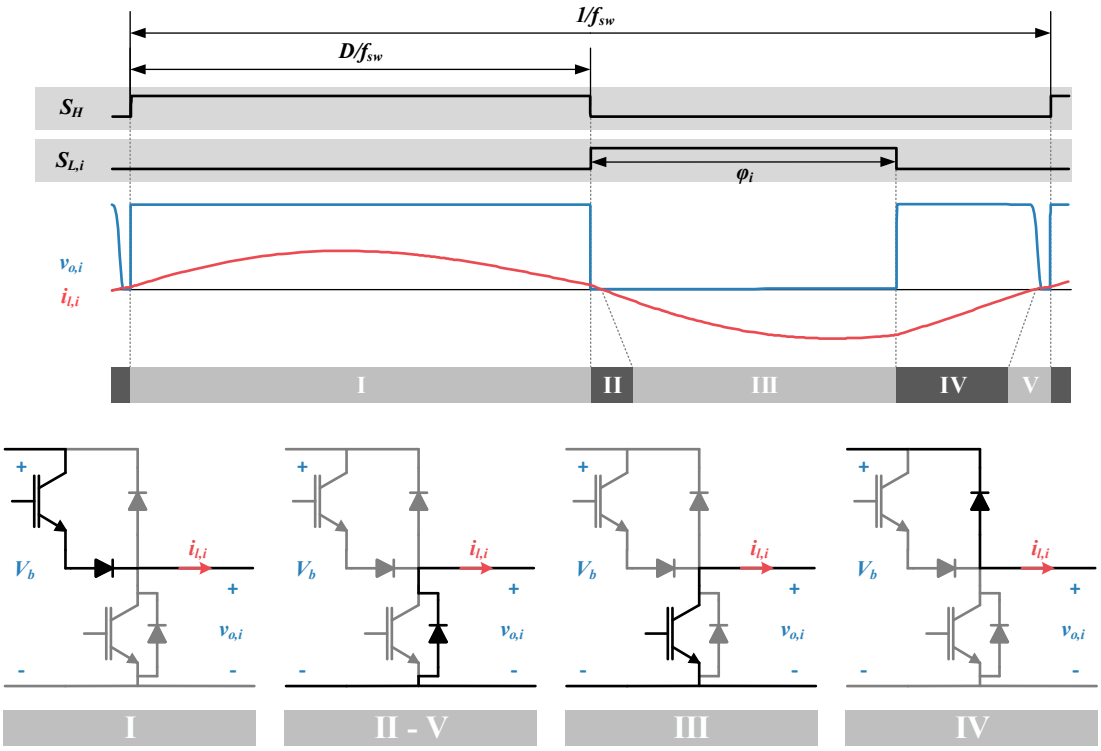


Fig. 3.12. Main waveforms and active devices for the NC-PWM strategy.

Contrary to the NC-PDC case, there is no requirement on the zero current crossing time $t\big|_{i_{o,i}(t)=0}$, leading to two different formulations.

For the case where $D_{L,i}$ is not activated the load voltage and current can be evaluated by assuming asymmetrical duty cycle, as in the previous subsection. For the case where $D_{L,i}$ is activated

$$V_{off} = V_b \frac{\pi + \omega_{sw} t\big|_{i_{l,i}(t)=0} - \varphi_i}{2\pi}, \tag{3.26}$$

and the coefficients

$$\begin{cases} A_{Vo,h,i} = \dfrac{V_b}{h\pi}\left(\sin\left(h\phi_0\right) - \sin\left(h\varphi_i\right)\right) \\ B_{Vo,h,i} = \dfrac{V_b}{h\pi}\left(-\cos\left(h\phi_0\right) + \cos\left(h\varphi_i\right) - 1 + \left(-1\right)^h\right) \end{cases} \tag{3.27}$$

$$\begin{cases} A_{h,i} = \\ -\dfrac{V_b\left(\left(-\cos\left(h\gamma_0\right)+\cos\left(h\varphi_i\right)-1+\left(-1\right)^h\right)R_L+\left(\sin\left(h\gamma_0\right)-\sin\left(h\varphi_i\right)\right)\left(\omega_{sw}hL_r-\dfrac{1}{\omega_{sw}hC_r}\right)\right)}{h^2\pi\omega_{sw}C_r\left(R_{eq}{}^2+\left(\omega_{sw}hL_{eq}-\dfrac{1}{\omega_{sw}hC_r}\right)^2\right)} \\ B_{h,i} = \\ \dfrac{V_b\left(\left(\sin\left(h\gamma_0\right)-\sin\left(h\varphi_i\right)\right)R_L-\left(-\cos\left(h\gamma_0\right)+\cos\left(h\varphi_i\right)-1+\left(-1\right)^h\right)\left(\omega_{sw}hL_r-\dfrac{1}{\omega_{sw}hC_r}\right)\right)}{h^2\pi\omega_{sw}C_r\left(R_{eq}{}^2+\left(\omega_{sw}hL_{eq}-\dfrac{1}{\omega_{sw}hC_r}\right)^2\right)} \end{cases} \tag{3.28}$$

being $\gamma_0 = \omega_{sw}\, t\big|_{i_{o,i}(t)=0}$.

The transmitted power can be calculated as

$$P_{o,i} = V_b{}^2 R_{eq,i}\sum_{h=1}^{H}\left(\frac{\left(1-\left(-1\right)^h\right)\left(\cos\left(h\gamma_0\right)-\cos\left(h\varphi_i\right)+1\right)-\cos\left(h\gamma_0-h\varphi_i\right)}{h^2\pi^2\left(R_{eq,i}{}^2+\left(\omega_{sw}hL_{eq,i}-\dfrac{1}{\omega_{sw}hC_r}\right)^2\right)}\right). \tag{3.29}$$

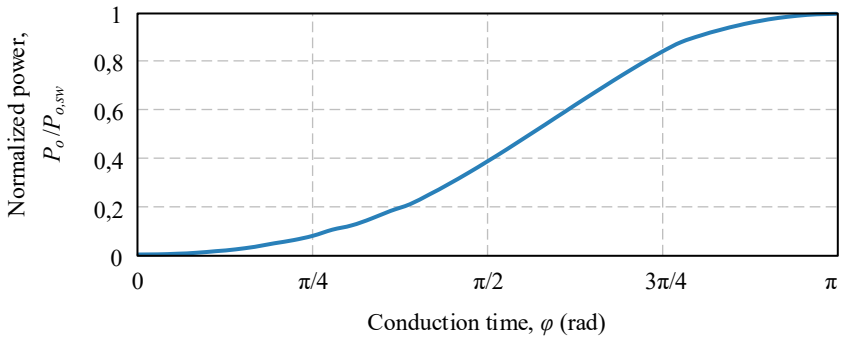


Fig. 3.13. Transmitted power dependency with NC-PDC modulation strategy normalized by SW transmitted power.

3.4.2. Closed loop considerations

The proposed non-complementary modulation strategies allow full-range power control, being the maximum power the transmitted with square waveform modulation, i.e. lowest α_i and highest φ_i, as

$$P_{o,i}(f_{sw},\alpha_i,\varphi_i) < P_{o,i}(f_{sw},0,\pi). \tag{3.30}$$

Therefore, they present an efficient and highly independent power control when the frequency is selected so that the maximum transmitted power is enough for all loads.

With this in mind, it is clear that multi-load operation is achieved independently of the inductor coverage and pot material which leads to different coupling between the inductor and the pot. Therefore, the final user perceives an even pot heating, leading to good user experience. Moreover, there is no fluctuation in the transmitted power as the modulation strategies are continuous, solving the flicker and the boiling perception problems.

As a consequence, by means of the control strategy it is possible to address other constraints presented on the introduction of the chapter. The reduction of the harmonic distortion due to the magnetic field strength, dependent on the applied voltage which correspond with the one of the mains, v_{ac}, is possible given that each inverter branch equivalent resistance as seen from the mains, $R_{ac,eq,i}$, can be defined as

$$R_{ac,eq,i}(v_{ac}) = \frac{V_{ac,rms}{}^2}{P_{o,i}(v_{ac},f_{sw},\alpha_i,\varphi_i)}. \tag{3.31}$$

Therefore, the total equivalent resistance of the complete inverter, $R_{ac,eq}$, is the parallelization of all independent resistances as

$$R_{ac,eq}(v_{ac}) = \frac{V_{ac,rms}{}^2}{\sum_{n=1}^{N} P_{o,i}(v_{ac},f_{sw},\alpha_i,\varphi_i)}. \tag{3.32}$$

Following this approach, the mains current, i_{ac}, can be described as

$$i_{ac}(t) = \frac{\hat{V}_{ac}}{R_{ac,eq}(v_{ac})}\sin\left(2\pi f_{ac}t\right), \tag{3.33}$$

where f_{ac} is the mains frequency.

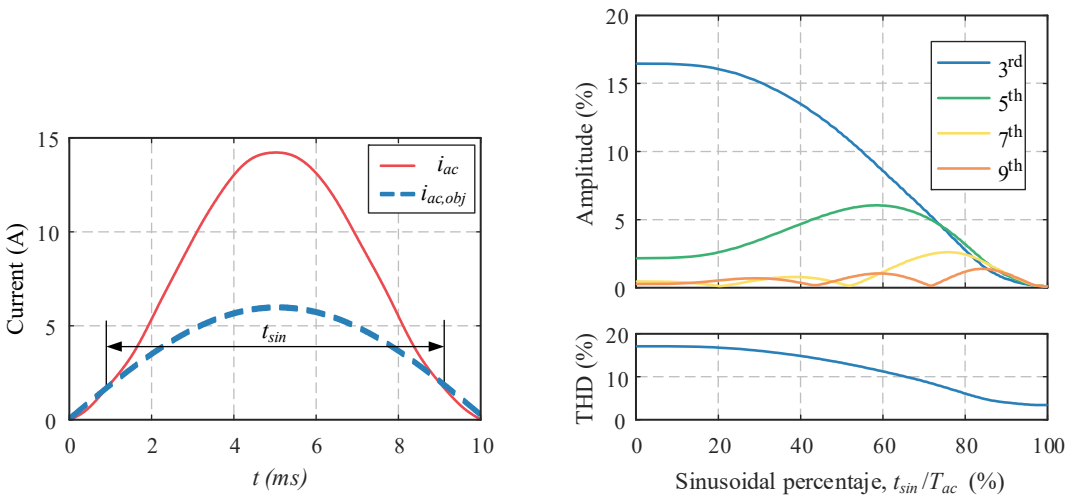
Therefore, it is possible to set different equi-resistances with constant value per branch, $R_{ac,obj,i}$, independently of the voltage fluctuation and transmit the desired power while ensuring a sinusoidal current, $i_{ac,obj}$, with unity power factor and reduced harmonic distortion.

In Fig. 3.14 (a) the consequence of (3.30) can be seen, showing that the correction is possible when $R_{ac,eq}$ is lower than $R_{ac,obj}$, i.e. i_{ac} is higher than the desired $i_{ac,obj}$. To do so, the originally distorted mains current, i_{ac}, is presented in comparison a $i_{ac,obj}$ curve corresponding with the desired $R_{ac,obj}$. This figure shows the mains period fraction where correction is possible, t_{sin}. Thus, the resulting non-distorted current, $i_{ac,nd}$, can be expressed as

$$i_{ac,nd}(t)=\begin{cases} i_{ac}(t) & t\le \dfrac{1}{4f_{ac}}-\dfrac{t_{sin}}{2} \\ \dfrac{\hat{V}_{ac}}{R_{ac,obj}}\sin(2\pi f_{ac}t) & \dfrac{1}{4f_{ac}}-\dfrac{t_{sin}}{2}<t\le \dfrac{1}{4f_{ac}}+\dfrac{t_{sin}}{2}, \\ i_{ac}(t) & t>\dfrac{1}{4f_{ac}}+\dfrac{t_{sin}}{2} \end{cases} \tag{3.34}$$

where

$$t_{sin}=t\big|_{R_{ac,eq}(v_{ac})<R_{ac,obj}=\left(\hat{V}_{ac}/\sqrt{2}\right)^2/P_{o,obj}}. \tag{3.35}$$



(a) (b)

Fig. 3.14. Comparison between the original distorted current, i_{ac}, and the desired sinusoidal current, $i_{ac,obj}$, which corresponds with a constant $R_{ac,obj}$ (a) and harmonic component variation depending on the i_{sin} share of the total period (b).

Consequently, the sinusoidal part of the current decreases with the increase of the desired transmitted power, $P_{o,obj}$. As a consequence, in order to maximize t_{sin}, $R_{ac,eq}$ can be reduced by approximating the switching frequency close to the resonant frequency while maintaining ZVS commutation. A comparison of the achieved THD reduction as a function of t_{sin} can be seen in Fig. 3.14 (b).

3.4.2.1. In-cycle parameter variation

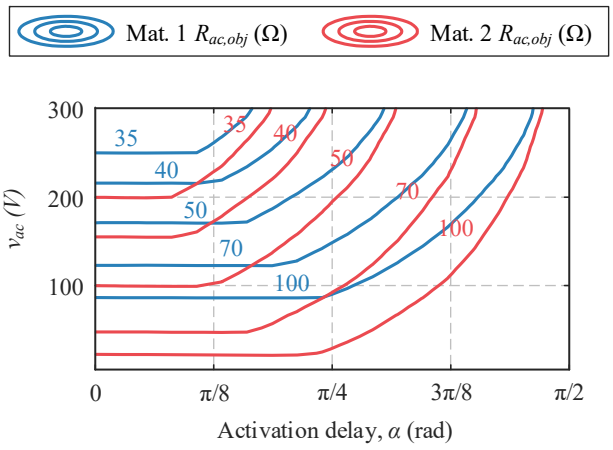
To achieve a constant $R_{ac,obj}$, the control parameter has to adapt the load $R_{eq,i}(v_{ac})$ and $L_{eq,i}(v_{ac})$ variation. Analytically, the different $R_{ac,eq,i}$ as a function of the control parameter can be derived from equation (3.31). For the case of the NC-PDC strategy, it can be calculated as

$$R_{ac,eq,i,\alpha_i}(v_{ac}) = \frac{1}{R_{eq,i}(v_{ac})\sum_{h=1}^{H}\left(\frac{\left(1-(-1)^h\right)\left(\cos(h\alpha_i)-\cos(h\gamma_0(v_{ac}))+1\right)-\cos(h\alpha_i-h\gamma_0(v_{ac}))}{h^2\pi^2\left(R_{eq,i}(v_{ac})^2+\left(\omega_{sw}hL_{eq,i}(v_{ac})-\frac{1}{\omega_{sw}hC_r}\right)^2\right)}\right)} \tag{3.36}$$

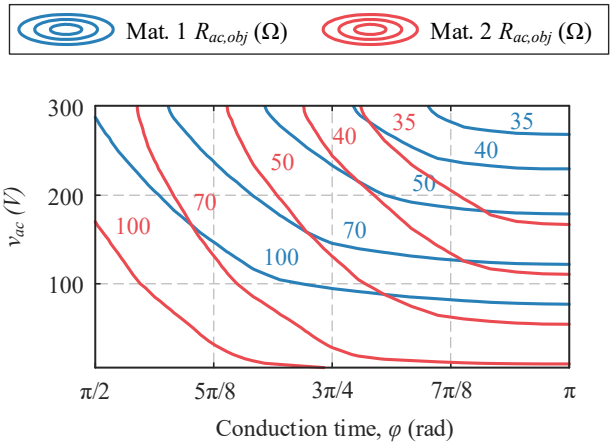
For the NC-PWC strategy, the equivalent resistance is calculated as

$$R_{ac,eq,i,\varphi_i}(v_{ac}) = \frac{1}{R_{eq,i}(v_{ac})\sum_{h=1}^{H}\left(\frac{\left(1-(-1)^h\right)\left(\cos(h\gamma_0(v_{ac}))-\cos(h\varphi_i)+1\right)-\cos(h\gamma_0(v_{ac})-h\varphi_i)}{h^2\pi^2\left(R_{eq,i}(v_{ac})^2+\left(\omega_s hL_{eq,i}(v_{ac})-\frac{1}{\omega_s hC_r}\right)^2\right)}\right)} \tag{3.37}$$

The selection of the $R_{ac,obj,i}$ depends on the power that is desired to transmit to each load. The curves for various levels of $R_{ac,obj,i}$ and the two pot materials can be compared in Fig. 3.15. In this figure, differences in the voltage range that allow parameter change can be seen, corresponding with the differences on t_{sin}.



(a)



(b)

Fig. 3.15. Equal resistance curves for two pot materials operating the inverter at the same f_{sw} and with the non-complementary pulse delay control (NC-PDC) strategy (a), and the non-complementary pulse width modulation (NC-PWM) strategy (b).

To calculate the objective equivalent resistance, it can be estimated substituting the desired power, $P_{obj,i}$, in equation (3.31) as

$$R_{ac,obj,i} = \frac{\hat{V}_{ac}^{\,2}}{P_{obj,i}}. \tag{3.38}$$

However, the controlled transmitted power corresponds only with the sinusoidal part of the current

$$P_{cntr,i} = 2f_{ac}\int_{\frac{1}{4f_{ac}}-\frac{t_{sin}}{2}}^{\frac{1}{4f_{ac}}+\frac{t_{sin}}{2}} \frac{\left(\hat{V}_{ac}\sin\left(2\pi f_{ac}t\right)\right)^2}{R_{ac,obj,i}}dt = \frac{\hat{V}_{ac}^{\,2}\left(\sin\left(2\pi f_{ac}t_{sin}\right)+2\pi f_{ac}t_{sin}\right)}{R_{ac,obj,i}}, \tag{3.39}$$

meaning that the mains cycle power should be measured and $R_{ac,obj,i}$ modified accordingly.

3.4.2.2. Control algorithm

The proposed control system can be seen in Fig. 3.16. It is divided into two main blocks: branch equivalent resistance recalculation, and branch constant resistance control. This structure achieves the power factor correction with a precise control in the transferred power. The first block operates at the mains frequency, f_{ac}, while the second one operates at switching frequency.

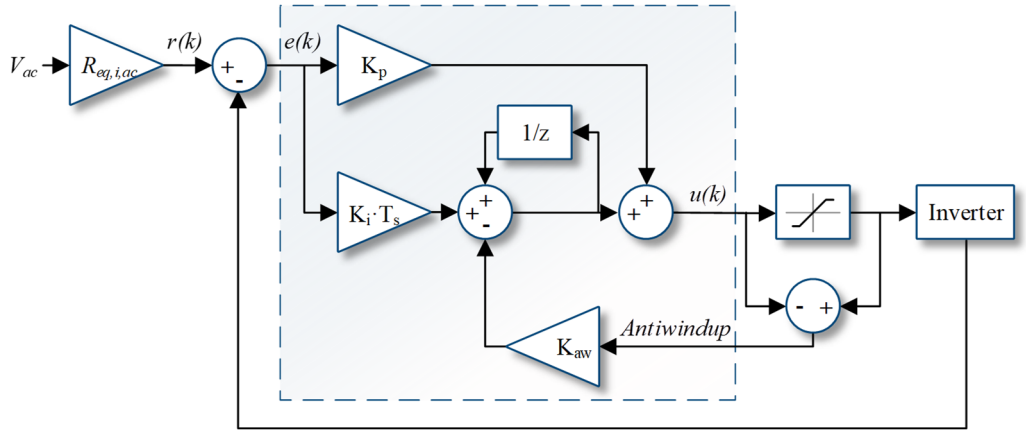
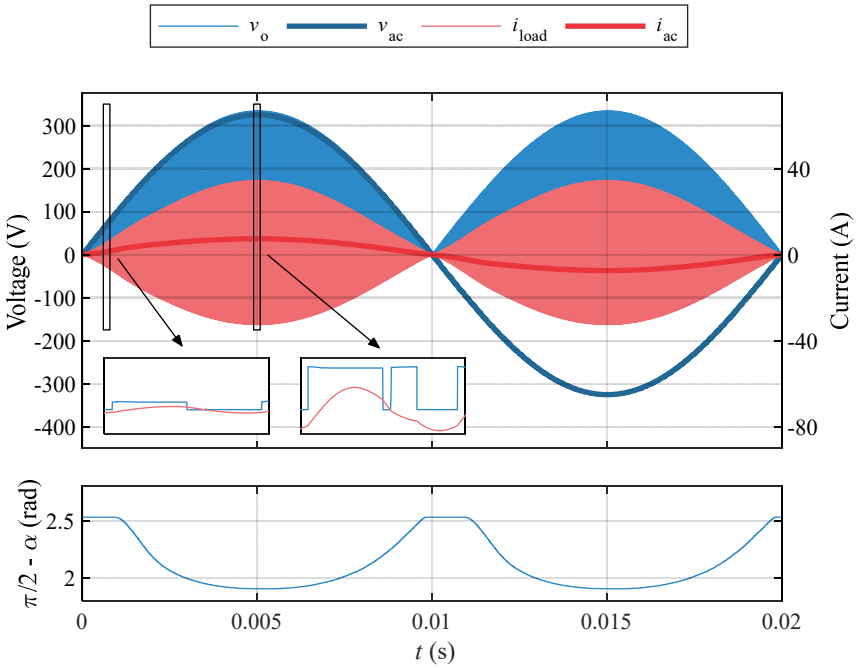


Fig. 3.16. Control block schematic.

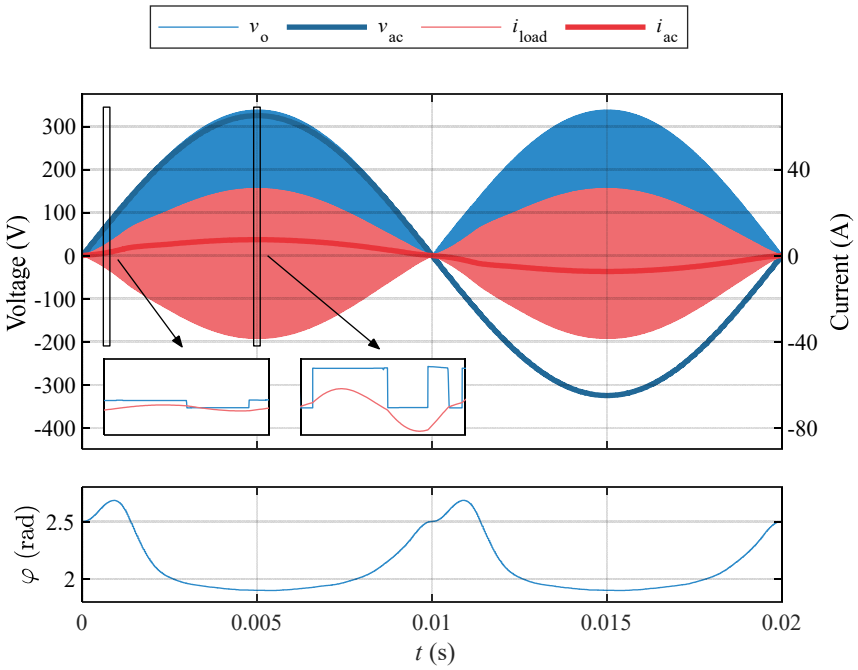
The $R_{ac,obj,i}$ recalculation part operates by calculating the difference between the real transmitted power to the load, $P_{o,i}$, and the expected power, $P_{o,obj,i}$ and then including the error in equation (3.38).

The constant resistance control is comprised by a PI controller with an anti-windup block. The latter is necessary as the action variation, i.e. α or φ parameter, is limited for both modulation strategies. Between 0 and π radians for the case of φ, and between the diode conduction time and π for the variation of parameter α.

Simulation results for the algorithm with both parameter variations and a single load are shown in Fig. 3.17. Both alternatives present and appropriate THD reduction of approximately the 70%. Additionally, in both simulations, it is important to note the asymmetrical parameter variation, as the PI controller also compensates the incomplete bus capacitor discharge.



(a)



(b)

Fig. 3.17. Asymmetrical modulations for power factor correction: Non-complementary pulse delay control (NC-PDC) (a) and Non-complementary pulse width modulation (NC-PWM) (b).

3.5. Advanced MPC applied to NC-PDC

Considering the high number of control parameters and the presence of several non-lineal constraints, the usage of classical control techniques, as the previously proposed PI, is limited. In this context, advanced control techniques arise as effective solutions. In this case, model predictive control (MPC) is considered, as it appears as an effective tool to control multi-in multi-out complex systems [164], with a high applicability in the field of power electronics [165-168] and resonant inverters as it can deal with nonlinear systems and include constraints both on inputs and states.

MPC uses a model of the system in order to predict its behavior. Therefore, standard MPC implementations calculate a series of optimal control inputs (u_0, …, u_{N-1}) of the system within a prediction horizon, N, based on the solving of an optimization problem that minimizes a certain cost function, J. This problem, which is solved at each control instance when new states data is available, can be formulated as

$$\begin{aligned} \underset{u_k}{\text{minimize}} \quad & \sum_{k=0}^{N-1} J\left(x_k, u_k\right) \\ \text{subject to} \quad & x_{k+1} = f\left(x_k, u_k\right),\ x_0 = \hat{x}, \\ & g\left(x_k, u_k\right) \le 0, \\ & \text{for } k = 0, \ldots, N-1. \end{aligned} \tag{3.40}$$

where x_k and u_k are the states and the control inputs of the system at step k, respectively. Function $f(x_k,u_k)$ denotes the discrete-time model of the system and g are general constraints to be satisfied during operation. The current state of the system is $\hat{x}$, which needs to be measured or estimated.

3.5.1. Single output model

In order to improve the optimization problem resolution, the analytical model has to be generated to take advantage of the solver mathematical formulation. Therefore, it is based on the differential equations of the resonant circuit

$$\begin{aligned} \frac{di_{l,i}}{dt} &= \frac{1}{L_{eq,i}}\left(v_{o,i} - R_{eq,i} i_{l,i} - v_{c,i}\right), \\ \frac{dv_{c,i}}{dt} &= \frac{1}{C_r} i_{l,i}, \end{aligned} \tag{3.41}$$

besides, a double time transformation, as the proposed in [169], is used to overcome the challenge of efficiently solving an optimization problem that includes a switching

systems, i.e. a system where $v_{o,i}$ changes between 0V and V_b. However, this system is only useful when $v_{o,i}$ is known in advance, and on this case, as a consequence of using a non-complementary modulation, while no transistor is active, $v_{o,i}$, depends on the current path as follows:

$$v_{o,i} = \begin{cases} V_b & \text{if } i_{l,i} \leq 0 \\ 0 & \text{if } i_{l,i} > 0. \end{cases} \tag{3.42}$$

Therefore, a more advanced time transformation is performed to divide each switching cycle into three optimization intervals, according to the modulation strategy considered which in this case is NC-PDC, which are depicted in Fig. 3.18:

$$\begin{aligned} x_{k+1}^{[\mathrm{I}]} &= \frac{D_k}{f_{sw,k}} f^{[\mathrm{I}]}\left(x_k, u_k\right), \\ x_{k+1}^{[\mathrm{II}]} &= \frac{\left(1-D_k\right)\alpha_{i,k}}{f_{sw,k}} f^{[\mathrm{II}]}\left(x_k, u_k\right), \\ x_{k+1}^{[\mathrm{III}]} &= \frac{\left(1-D_k\right)\left(1-\alpha_{i,k}\right)}{f_{sw,k}} f^{[\mathrm{III}]}\left(x_k, u_k\right), \end{aligned} \tag{3.43}$$

where $f^{[\mathrm{I}]}$ and $f^{[\mathrm{III}]}$ refer to the model defined in (3.41) with the signal $v_{o,i}$ set to V_{cc} and 0 V respectively. $f^{[\mathrm{II}]}$ also denotes the model defined in (3.41) but in this case, the signal $v_{o,i}$ is defined by its dependence on the current.

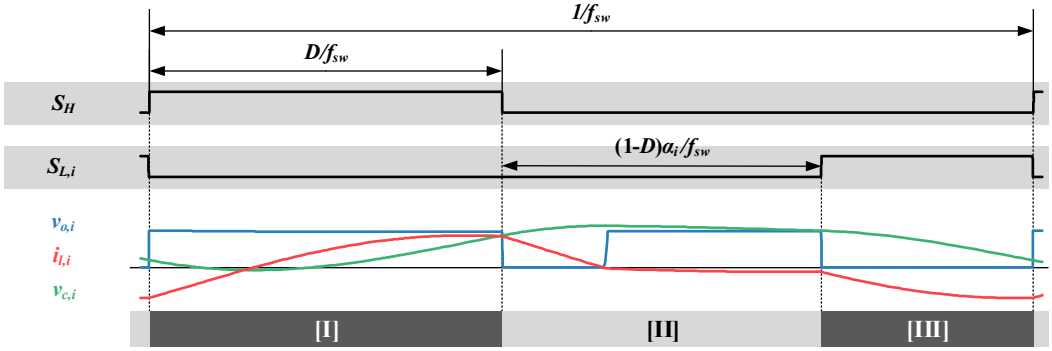


Fig. 3.18. Optimization of the interval division of a switching cycle and reformulation of the control parameters.

This voltage change has been modelled in the literature by a sigmoid function in order to achieve continuity [170]. $v_{o,i}$ in $f^{[\mathrm{II}]}$ is approximated by a logistic function with a certain slope, λ, which is adjusted by the time transformation:

$$v_{o,i} = \frac{1}{1+e^{-\lambda\left(\left(1-D_k\right)\alpha_{i,k}/f_{sw,k}\right) i_{l,i}}}. \tag{3.44}$$

The sigmoid slope is critical for the efficient solving of the optimization problem as steep approximations, which fits closely the real behavior (Fig. 3.19), present big changes for small optimizer steps. TABLE 3.1 shows the tradeoff between real behavior fitting and steepness.

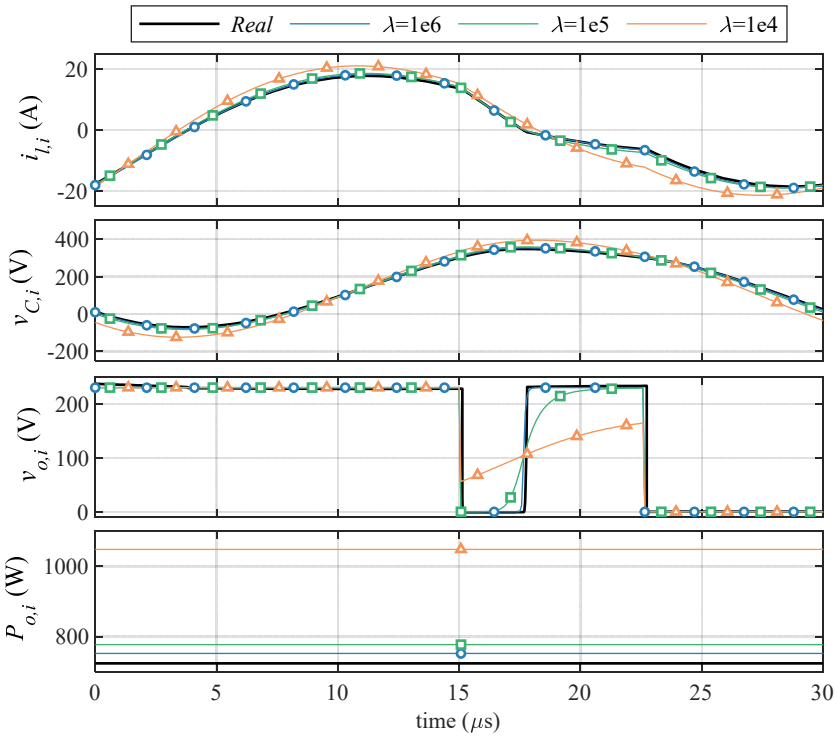


Fig. 3.19. Sigmoid steepness and state behavior.

TABLE 3.1. SIGMOID APPROXIMATION ERROR COMPARISON

MODEL SLOPE, λ	OPTIMIZER RUNTIME (ms)	SIMULATOR ERROR AT SAMPLING POINT		
		$i_{l,i}$ (A)	$v_{c,i}$ (V)	$P_{o,i}$ (W)
1e6	750	0.26	3.83	25.32
1e5	656	0.73	11.21	44.03
1e4	629	2.10	30.31	126.71

The complete MPC model formulation can be obtained by concatenating the optimizer intervals and assuming that the control parameters are constant during a switching cycle:

$$x_{k+1}^{[mpc]} = \begin{cases} \dfrac{D_k}{f_{sw,k}} f^{[\mathrm{I}]}\left(x_k, u_k\right) & \text{if } \mathrm{mod}(k,3) = 0 \\ \dfrac{\left(1-D_k\right)\alpha_{i,k}}{f_{sw,k}} f^{[\mathrm{II}]}\left(x_k, u_k\right) & \text{if } \mathrm{mod}(k,3) = 1 \\ \dfrac{\left(1-D_k\right)\left(1-\alpha_{i,k}\right)}{f_{sw,k}} f^{[\mathrm{III}]}\left(x_k, u_k\right) & \text{if } \mathrm{mod}(k,3) = 2 \end{cases} \tag{3.45}$$

To incorporate the continuous time ordinary differential equations (3.45) in our discrete MPC formulation (3.40), a discretization with orthogonal collocation on finite elements has been performed [171].

As a consequence of this discretization, the average transmitted power, $P_{o,i}$, which is the controller tracking parameter, requires a two-step calculation. The average power at each control interval is obtained by using the value of the states at the collocation points, c:

$$P_{o,i,k} = \sum_{c=1}^{n_{col}} v_{o,i,k}^{[c]} i_{l,i,k}^{[c]} \left(\tau_k^{[c]} - \tau_k^{[c-1]}\right), \tag{3.46}$$

where n_{col} denotes the number of collocation points and the integral is approximated by a numerical integration in which $\tau_k^{[c]}$ denotes the time of collocation point c in the control interval k. And the average power for the switching cycle is calculated by applying the previously described time transformation to each of the non-zero $v_{o,i}$ control intervals:

$$P_{o,i} = P_{o,i,k|\mathrm{mod}(k,3)=0} D_k + P_{o,i,k|\mathrm{mod}(k,3)=1} \left(1-D_k\right)\alpha_{i,k}. \tag{3.47}$$

3.5.2. MPC of the multi-output inverter

The complete MPC problem is intended to represent a multi-output inverter with any number of branches and to achieve proper efficiency-oriented power tracking.

The optimization problem to solve at the beginning of each switching cycle can be presented as follows:

$$
\begin{aligned}
\underset{f_{sw,k},D_k,\alpha_{i,k}}{\text{minimize}} \quad & \sum_{k=0}^{N}\sum_{i=0}^{n_{branch}}\left(\left(P_{o,i,k}-P_{obj,i}\right)^2+C_1\alpha_{i,k}\right. \\
& \left.+C_2 f_{sw,k}\left(i_{l,i,k|\text{mod}(k,3)=1}-i_{l,i,k|\text{mod}(k,3)=0}\right)\right) \\
\text{subject to} \quad & \text{model in (5)} \\
& 30 \le f_{sw,k} \le 70 \text{ kHz}, \\
& 0.1 \le D_k \le 0.9, \\
& 0.05 \le \alpha_{i,k} \le 0.9, \\
& f_{sw,k} = f_{sw,k-1}, \text{ if mod}(k,3) = 1,2, \\
& D_k = D_{k-1}, \text{ if mod}(k,3) = 1,2, \\
& \alpha_{i,k} = \alpha_{i,k-1}, \text{ if mod}(k,3) = 1,2, \\
& i_{l,i,k} \ge 0, \text{ if mod}(k,3) = 1, \\
& i_{l,i,k} \le 0, \text{ if mod}(k,3) = 0.
\end{aligned}
\tag{3.48}
$$

On (3.48), the cost function includes three terms with weighting parameters, C_1 and C_2, to set the relative relevance of each of them. The power tracking term is squared as it penalizes negative and positive deviations equally. The second term is related to the cohexistence of low side transistor ZVS and α_i as control parameter. Lastly, the product of f_{sw} and $i_{l,i,k|\text{mod}(k,3)=1}$ and $-i_{l,i,k|\text{mod}(k,3)=2}$ represent a figure of merit (FOM) for the power loses due to the transisor turn off. This FOM is always positive as it is constrained by the ZVS imposition.

The constraints included in (3.48) can be divided in different groups. The input constraints to limit the optimizer solution to feasible ones, the input constraints to ensure thet the inputs are kept constant within each switching cycle, and constraints to achieve an overall high efficiency solution.

The efficiency constraints are related to ZVS transistor activation, which eliminates transistor turn-on losses, and is achieved by ensuring the correct current sign at the beginning of control interval. This is especially relevant for S_H as it is a shared activation component with higher current levels, thus ZVS achievement is straightforward by setting $i_{l,i,k} \le 0$ if mod(k,3) = 0. However, as NC-PDM modulation strategy principle requires $D_{H,i}$ conduction and thus negative current in $S_{L,i}$ activation, this ZVS condition is implemented as a soft constraint. In order to do so, $i_{l,i,k} \ge 0$ if mod(k,3) = 1 and the α_i term is added to the cost function.

Additionally, as the MPC controller is conceived for a DNN implementation, a constraint that ensures that S_H on time is enough to evaluate the DNN can be added in the form of $f_{sw,k}D_k \geq t_{NN}$.

The optimization problems are solved by using an interior point algorithm which is implemented in IPOPT. All the derivative information is computed using automatic differentiation via CasADi [172] and the MPC is implemented using the toolbox do-mpc [173].

The prediction horizon is set to five switching intervals, i.e. $N = 15$, as it is considered enough for the system to reach the steady state. The tuning parameters are chosen as $C_1 = 1 \cdot 10^4$ and $C_2 = 1 \cdot 10^{-3}$ in order to balance the relative contributions in the cost function.

The parameters for the MPC model consider equal pot material in all branches. Thus, $V_b = 230$ V, $L_{eq,i} = 68.5$ µH, $R_{eq,i} = 4.6$ Ω, and $C_r = 400$ nF.

Additionally, the sigmoid slope is λ = 1e5 to achieve faster resolution, which is required for the DNN data generation. In order to minimize the approximation error, an additional proportional controller, with a proportionality constant, K, can be implemented, which varies the setpoint given to the MPC, $P_{MPC,i}$, based on the difference between the desired power, $P_{obj,i}$, and the measured one, $P_{meas,i}$.

$$P_{MPC,i} = P_{MPC,i} + K\left(P_{obj,i} - P_{meas,i}\right) \tag{3.49}$$

The controller simulation is performed considering a two-branch inverter. In order to increase the simulation precision a spice model is used. Therefore, LTspice is launched every switching cycle with the calculated control parameters and the previous value of the state variables and provides the new values of the state variables and an accurate power calculation.

The load equivalent parameters for the spice model are $L_{eq,i} = 68.5$ µH, and $R_{eq,i} = 2\pi f_{sw} L_{eq,i}/Q_i$ with Q_i=3.27, which is a more accurate approximation of the IH load behavior.

The simulation of a setpoint change is shown in Fig. 3.20. There can be seen a proper power tracking that respects the S_H ZVS constraints and presents at least one branch with $S_{L,i}$ ZVS behavior during the steady state. In TABLE 3.2 the results for a longer simulation with more setpoint variations are shown. This table also includes a robustness analysis to

show the controller proper behavior with low accuracy in an IH load equivalent parameter estimation.

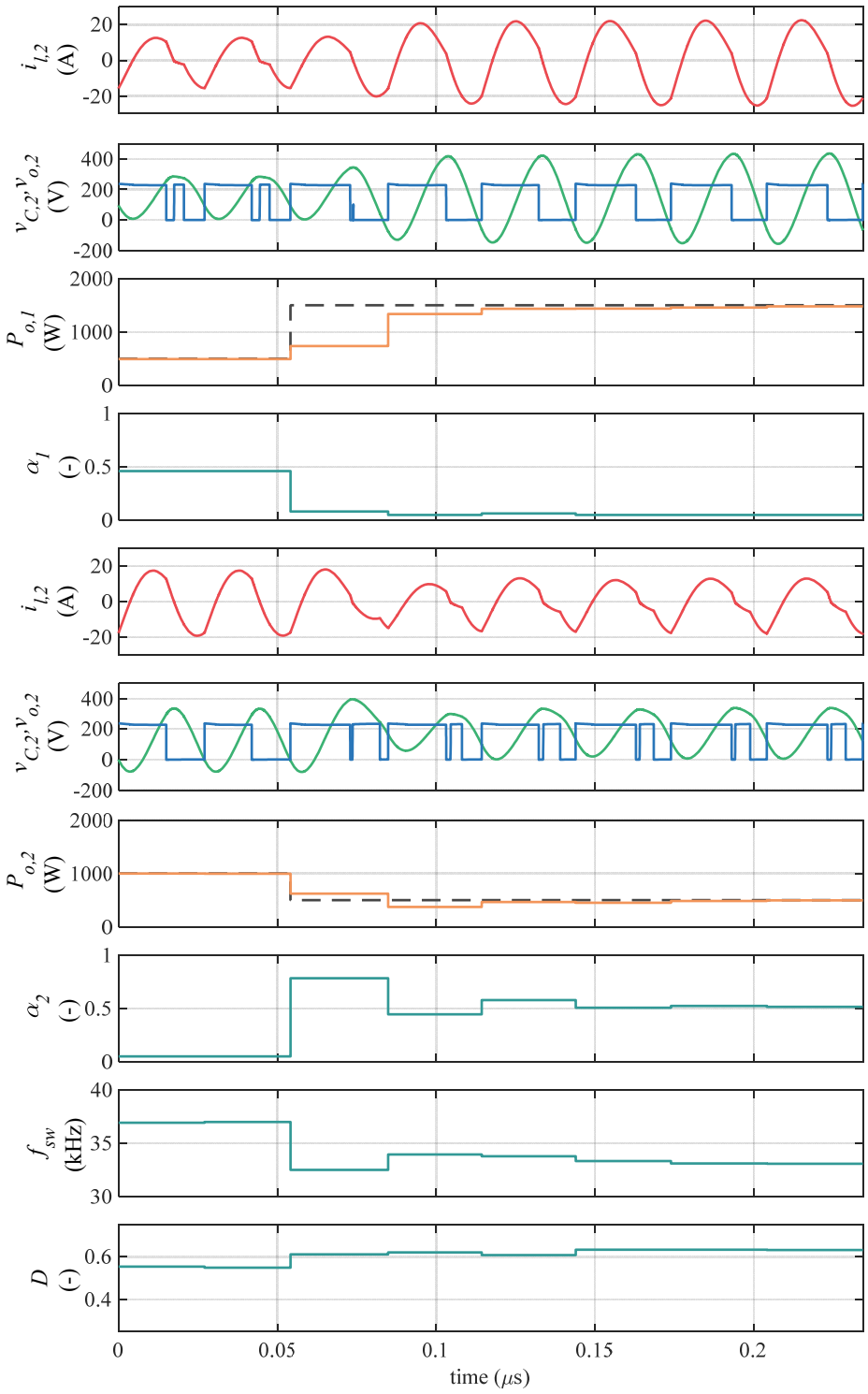


Fig. 3.20. Performance of the proposed MPC+P controller during a setpoint change, from $P_{obj,1}$ = 500 W $P_{obj,2}$ = 1000 W to $P_{obj,1}$ = 1500 W $P_{obj,2}$ = 500 W.

TABLE 3.2. LOAD UNCERTANITY ERROR

LOAD EQUIVALENT PARAMETERS	AVERAGE TRACKING ERROR (%)		AVERAGE SH ZVS (%)	AVERAGE SL ZVS (%)
Base simulation	7.84	8.19	100	93.56
$1.15L_{eq,1}$	32.28	8.40	100	95.47
$1.15R_{eq,1}$	14.11	9.06	100	92.59
$0.85L_{eq,1}$	7.91	11.07	100	64.24
$0.85R_{eq,1}$	3.50	8.13	100	91.09
With P controller (3.49)	0.73	0.76	100	92.05
$1.15L_{eq,1}$	9.99	1.66	100	91.50
$1.15R_{eq,1}$	1.46	0.85	100	90.54
$0.85L_{eq,1}$	1.69	1.17	100	67.26
$0.85R_{eq,1}$	0.75	1.00	100	89.45

3.5.2.1. Neural network implementation

The online solution of the optimization problem presents limitations when applied to high frequency power electronics, leading to solutions that require strong simplifications [167]. However, at its core, the MPC problem can be seen as an implicit function, mapping the current state to an optimal control input. Therefore, with the widespread development of deep learning, approaches that solve rigorous nonlinear MPC and accelerate the solution calculation by means of a deep neural network (DNN) have been proposed in the literature [174-176], being applicable to resonant converters [169, 177]. The selected neural network operates with the current state of the system, i.e. the measured state variables $v_{c,i}$ and $i_{l,i}$, and the desired power, $P_{obj,i}$ as inputs and provides the optimal control inputs for the current switching cycle, f_{sw}, D, and α_i as outputs. Thus, the neural network computation has to be done during S_H active time.

The chosen DNN presents $L = 4$ hidden layers, $M = 30$ neurons per layer and *tanh* is selected as the activation function.

As the intended behavior of the DNN is to approximate the control law, the data pairs for training are generated by the simulation of closed loop operation with various setpoint changes between random $P_{obj,i}$ within the interval [0 2000] W. Therefore, the state variables are dependent of the previous setpoint and MPC solution. The generated training inputs can be seen in Fig. 3.21 where the different power setpoints are represented for the different states, $i_{l,i}$ and $v_{c,i}$, showing a complete coverage of the operation region and an a non-homogeneous distribution that improves stead-state stability.

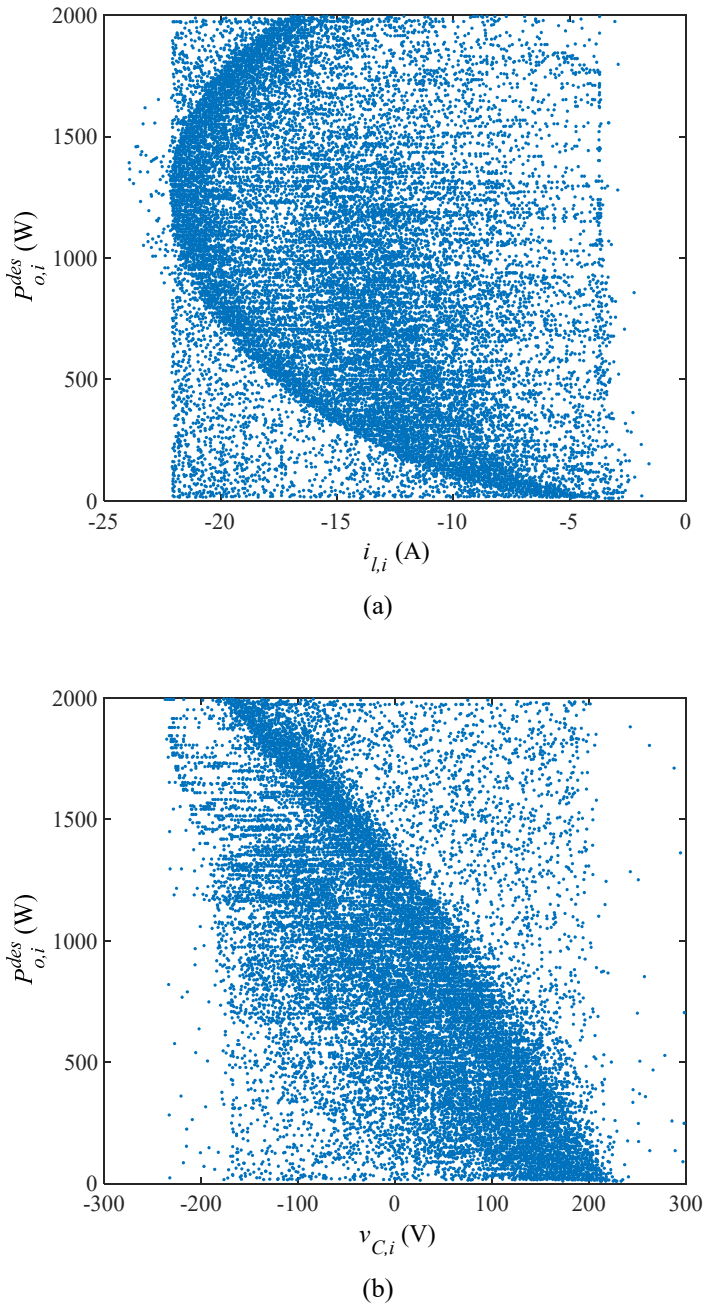


Fig. 3.21. Operation region sweep for DNN training data generation. Power setpoint vs the different states, $i_{l,i}$ (a) and $v_{c,i}$ (b).

The model used for the simulation matches the MPC one but with a steeper sigmoid slope and Q_i based $R_{eq,i}$ calculation. Additionally, as load simulation parameters are known during training data generation, instead of being cost-function dependent, $S_{L,i}$ ZVS is added as a constraint for the more power-demanding of the branches, improving performance. Finally, a filtering of the training pairs is performed to avoid learning steady state oscillating scenarios.

TABLE 3.3. TRAINING PAIRS SHAPE INFLUENCE

DATA POSTPROCESSING	AVERAGE TEST ERROR			
	f_{sw} (kHz)	D (-)	α_1 (-)	α_2 (-)
Sim. format.	0.4361	0.0063	0.0143	0.0160
Comp. format	0.3092	0.0055	0.0152	0.0165

Two strategies for the training data have been evaluated. Firstly, the direct learning of the control parameters as they have been simulated, i.e. f_{sw}, D, and α_i, and, secondly, the use of a PWM modulator parameters, implemented as a counter and comparator, i.e. converting the control parameters into comparator instants as: D/f_{sw}, $(D+(1-D)\alpha_i)/f_{sw}$, and $1/f_{sw}$.

The training of the neural network is performed using Keras in Tensorflow [178]. In TABLE 3.3 the results for the training with the different control parameter approach can be seen. There, comparator based DNN achieves better results for f_{sw} and the learning differences between the remaining parameters are not significant.

TABLE 3.4. TRAINING PAIRS GENERATION PERFORMANCE

LOAD EQUIVALENT PARAMETERS	AVERAGE TRACKING ERROR (%)		AVERAGE SH ZVS (%)	AVERAGE SL ZVS (%)
Ideal setpoint	10.66	9.52	100	99.72
Real setpoint	1.82	1.73	100	99.45

The simulation testbench corresponds with the used for the standard MPC controller. In TABLE 3.4 the performance results for two training data sets can be seen. The first one considers zero power error in reaching $P_{obj,i}$ when generating the training data and the second one assumes real steady state $P_{o,i}$ as the setpoint. As it can be seen, both cases maintain S_H ZVS and achieve good $S_{L,i}$ ZVS performance, but, additionally, the second approach is able to correct the error due to the model simplification. In Fig. 3.22 the same setpoint change as in the MPC case has been represented to show the proper operation with the real setpoint approximation, i.e. the one that uses $P_{o,i}$.

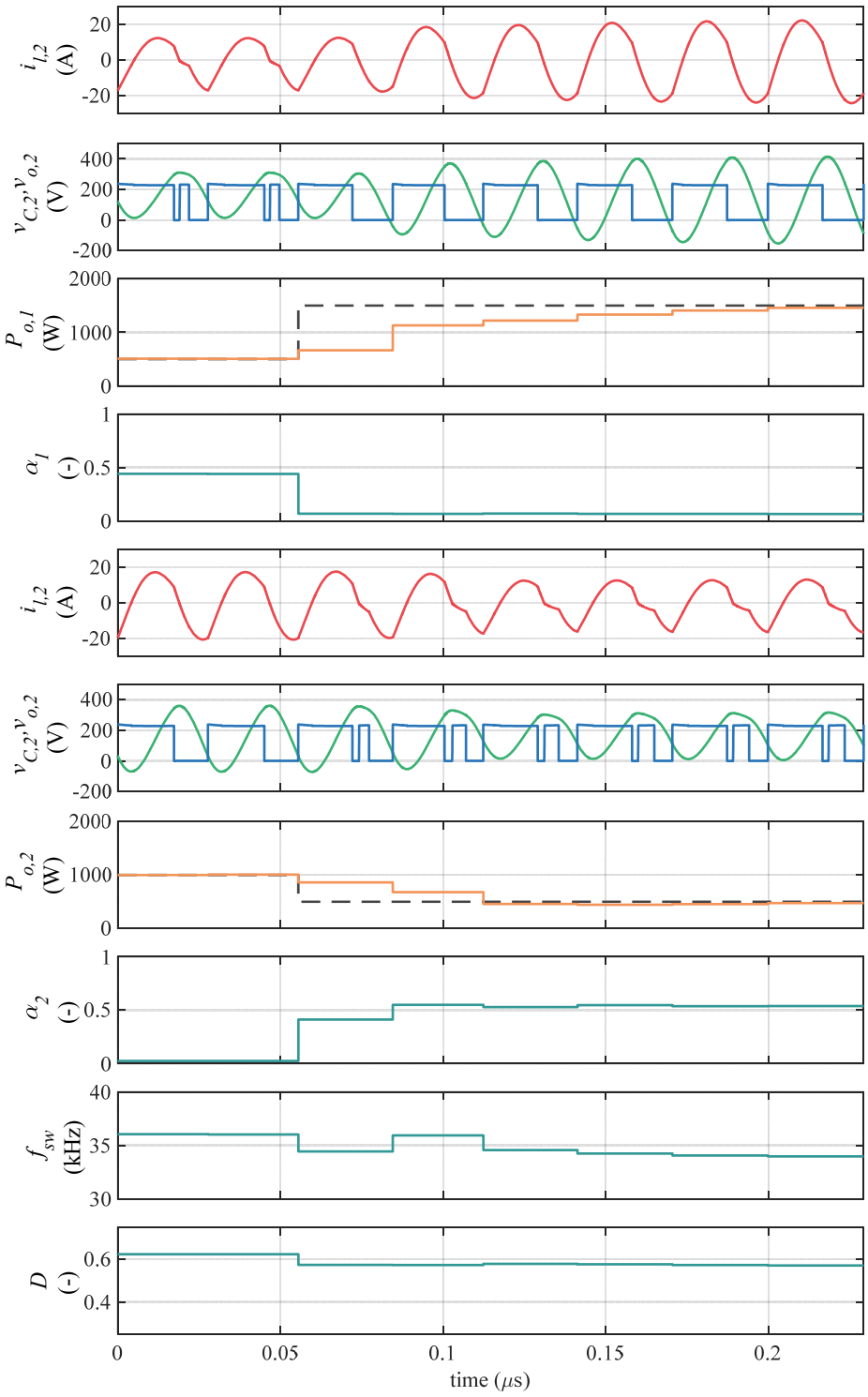


Fig. 3.22. Performance of the DNN implementation of the MPC controller during a setpoint change, from $P_{obj,1}$ = 500 W $P_{obj,2}$ = 1000 W to $P_{obj,1}$ = 1500 W $P_{obj,2}$ = 500 W.

Chapter 4

Implementation and Experimental Results

Experimental prototyping allows verifying the correct performance of the proposed topology when operating under the different modulations. In order to do so, the operation characteristics and restrictions of the modulations have to be evaluated in order to make an optimum selection of power device technologies, driving circuitry and measurement systems, leading to improved solutions.

In this chapter, several prototypes have been implemented following the single-column matrix-based ZVS resonant inverter topology, and according to different design considerations that include, among others, the IH load characteristics or the power device technology. The main waveforms of each prototype are presented showing the viability of the proposed topology and the proper operation with the different modulation strategies. Additionally, closed-loop operation with each modulation has been implemented on the most suitable prototype.

Contents

4. Implementation and Experimental Results

The theoretical performance of the proposed single-column matrix-based ZVS resonant inverter operating under the evaluated modulation strategies, and the advantages provided by the detailed closed loop considerations, require an experimental verification. In order to do so, several prototypes have been designed, developed, and built to achieve optimal operation within a specific set of parameters.

Each prototype design integrates the circuitry of the power and control electronics. The first one includes the rectifier and bus capacitor, the multi-inverter, and the split resonant capacitors. The second one is composed of the driving and sensing circuitry, a FPGA to implement the digital control, and the communication with the user through a PC. Additionally, in some cases, ancillary circuitry to allow independence in the activation of power and control electronics is also included. The remaining components, i.e. inductors, EMC filter, and cooktop structure, are chosen among the commercial possibilities in order to simplify the implementation process. Besides, this commercial selection ensures a prototype design process that, while presenting a holistic approach gives independency to the design of each of the parts, leading to a simplified adaptability.

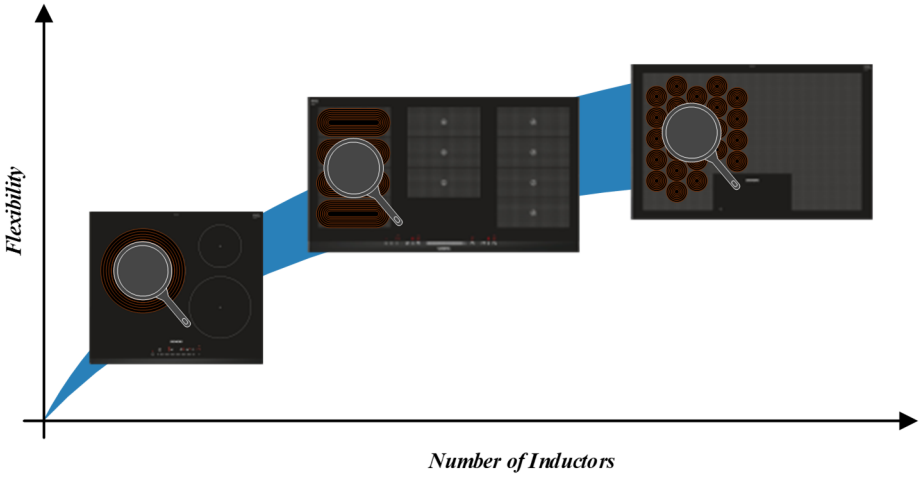


Fig. 4.1. Flexibility levels as a function of the number of coils. From left to right: concentric coils, flexible surface, and total active surface.

The inductor selection entail numerous implications over the versatility of the different modulation strategies. The equivalent IH load parameters are dependent of the coil magnetic design and the coupling with the different considered pots. For the complete experimental verification, three family of differently built pots are used, leading to a range of values to be considered during the design. Additionally, this range is widened by pot

placement, which leads to more limiting situations. In Fig. 4.1 a representation of the commercial flexibility level vs the number of coils can be seen.

Consequently, the different IH loads, understood as external operation parameters, are independent of the topology selection and is the main driving force for the prototype design. The flexibility level and thus the coils size and distribution, is used for a first classification of the proposed prototypes (Fig. 4.2).

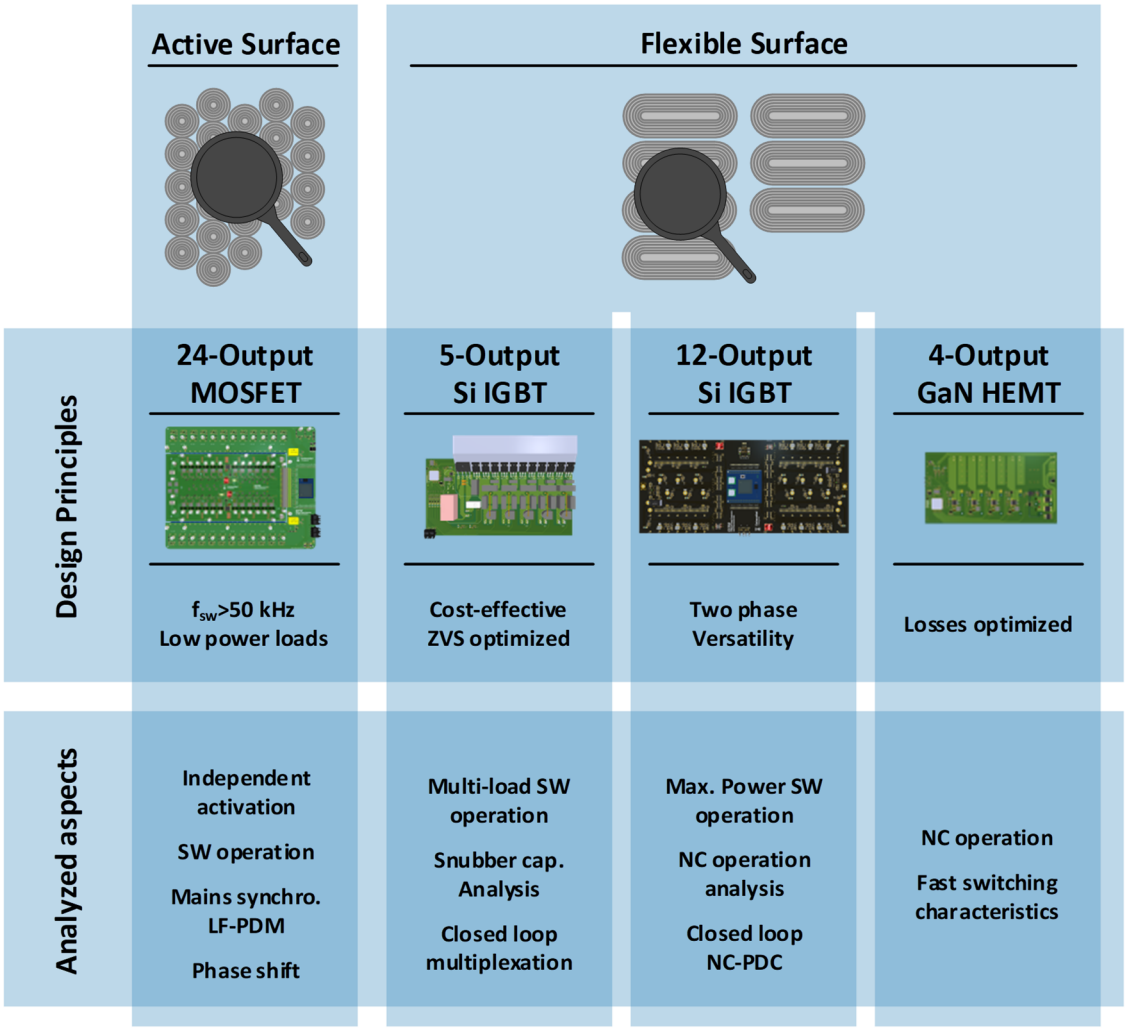


Fig. 4.2. Structure of the chapter and verifications carried out.

Therefore, each prototype is optimized for the selected multi-coil structure. Besides, additional parameters are to be considered in the prototype design, such as the restrictions of the selected modulation strategy.

The prototype for its application in total active surface is designed for 24 low-power IH loads, rated 600 W each. The operation frequencies are above 50 kHz and thus, MOSFET is selected as the switching device technology. This prototype allows the

verification of high-efficiency independent load activation with square waveform operation and as a consequence, the possibility of implementing mains synchronized LF-PDM. Besides, the design presents 2 independent inverters, and the controllability of the phase shift among them to minimize high frequency current consumption is also verified.

The remaining prototypes are applied to general flexible surface cooktops, with a lower number of inductors of higher rated power, 1800 W.

The 5-output IGBT implementation is designed to verify the proper adaptation of the topology to the considered IH loads. In order to do so in a cost-effective manner, a benchmarking process has been carried out considering ZVS operation and therefore turn-off snubber networks. With this prototype, multi-load operation with SW modulation is tested confirming the influence on current ratings of the usage of different number of loads for the same output power. Moreover, the snubber capacitor behavior is verified for SW and the undesired associated power losses with NC strategies are presented. Based on the proper operation under the presented SW conditions, closed loop operation with a mains-synchronized multiplexation strategy, following the considerations in 3.3.2, is verified.

To increase the topology control versatility by eliminating the snubber capacitors, the 12-output IGBT prototype is implemented. This prototype considers a connection to two mains phases, as it is usual with commercial cooktops, in order to achieve higher overall power. The prototype implementation allows to verify the power transmission of 7.2 kW with SW operation. Moreover, as the design is focused on versatility, it is used to test the NC strategies and validate the high efficiency of the prototype operating with this modulation. Additionally, based on the good results in terms of transmitted power accuracy, two closed loop implementations are tested. First, the in-cycle parameter variation to improve PFC and secondly and advanced MPC controller focused on efficiency.

Based on the previous results and taking into account the contribution of switching losses, the 4-output GaN HEMT implementation has been proposed to minimize the switching times and thus the power losses. This prototype is validated through NC modulation, showing the main switching *dv/dt*.

4.1. Total active surface

Total active surfaces achieve the higher level of flexibility but represents a small share of the flexible cooktops in the market. These structures present a high number of small-size inductors in order to allow the placement of a pot of any shape and size without restrictions. The coils size selection presents a trade-off between the adaptability to the pot shape or size, being especially relevant a high percentage of inductor coverage with small pots, and the number of coils, and therefore the complexity of the power electronics. As a consequence, the considered coils present reduced power rating as a combination of a medium to high number of coils is available to power a single pot.

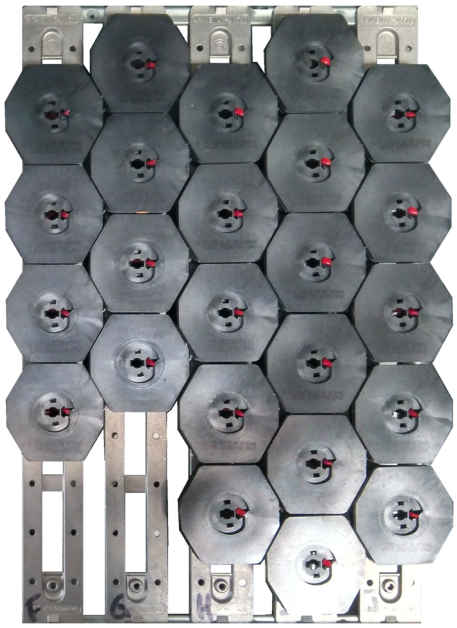


Fig. 4.3. Small inductor distribution over the cooktop surface and reference measurements.

When considering this inductor structure, the main design specifications are summarized on TABLE 4.1. The required maximum power per IH load is set in 600 W, which is available at frequencies over 50 kHz for this inductor design. Additionally, the load equivalent parameters are limited to a 30% inductor coverage in order to achieve a balance between the required flexibility and the inverter maximum ratings.

Moreover, most of the commercial cooktops are designed for connecting to two mains phases. Therefore, when considering the proposed inductor distribution for its connection to European mains, its overall current consumption is limited [141] to 16 A per phase.

The proposed prototype is therefore designed to a maximum power of 3600 W by means of up to 24 inductors with a rated power of 600 W. Hence, when proposing an implementation based on the single-column ZVS matrix converter for this application,

several considerations have to be taken into account to achieve a cost-effective and high-performance implementation.

TABLE 4.1. MAIN DESIGN SPECIFICATIONS

PARAMETER	VALUE
Supply voltage, v_{ac}	230 V, 50 Hz
Rectified peak voltage, V_b	325 V
Inductor power, $P_{o,i}$	0 – 600W
Number of inductors, n	24
Total power, $P_{o,max}$	0 – 3600 W
Load 1 quality factor, Q	2.83 (2.83 – 8.73)
Load 1 equivalent inductance, L_{eq}	142 uH (142 – 187 uH)
Load 2 quality factor, Q	2.96 (2.96 – 7.12)
Load 2 equivalent inductance, L_{eq}	167 uH (167 – 200 uH)
Load 3 quality factor, Q	3.52 (3.52 – 7.51)
Load 3 equivalent inductance, L_{eq}	202 uH (202 – 206 uH)
Switching frequency range, f_{sw}	25 – 100 kHz

4.1.1. 24-output MOSFET prototype

The most prominent advantage of this solution is the reduction in the number of switching devices achieved, being more relevant when considering that the low side transistor and, based on the expected transmitted power by each coil, the complete output branch devices can be selected with lower current ratings. Additionally, the high-side transistor is dimensioned based on the maximum cooktop power, i.e. 3600W per phase, and not the sum of all the connected loads, leading to contained ratings. However, the number of output branches per inverter, i.e. per high-side transistor, should be considered so the reduction of the power factor due to the parallelization of loads does not greatly increase the high-side transistor current ratings.

4.1.1.1. Implementation

The schematic of the proposed prototype is depicted in Fig. 4.4. It includes the components selected during the design process: the rectifier, a distributed bus capacitor, two inverters of 12 outputs each, and the required resonant capacitors per coil.

MOSFET are selected as the transistor technology in order to minimize the switching losses which otherwise would be elevated due to the requirements on switching frequency. Moreover, high-side transistor, is chosen to present a low C_{oss} capacitance, as

due to the presence of $D_{S,i}$ no current path is available for discharge and the accumulated energy is transformed to additional turn-on power losses. Additionally, an hyperfast $D_{H,i}$ diode is selected to minimize the reverse recovery contribution to the switching losses.

Besides the switching considerations, the high imbalance between the ratings of the high side transistor and each low side one allow an optimized device selection based on its $R_{DS,on}$. The high-side transistor is chosen with 33 mΩ while the low side ones present 115 mΩ, due to the expected current flow.

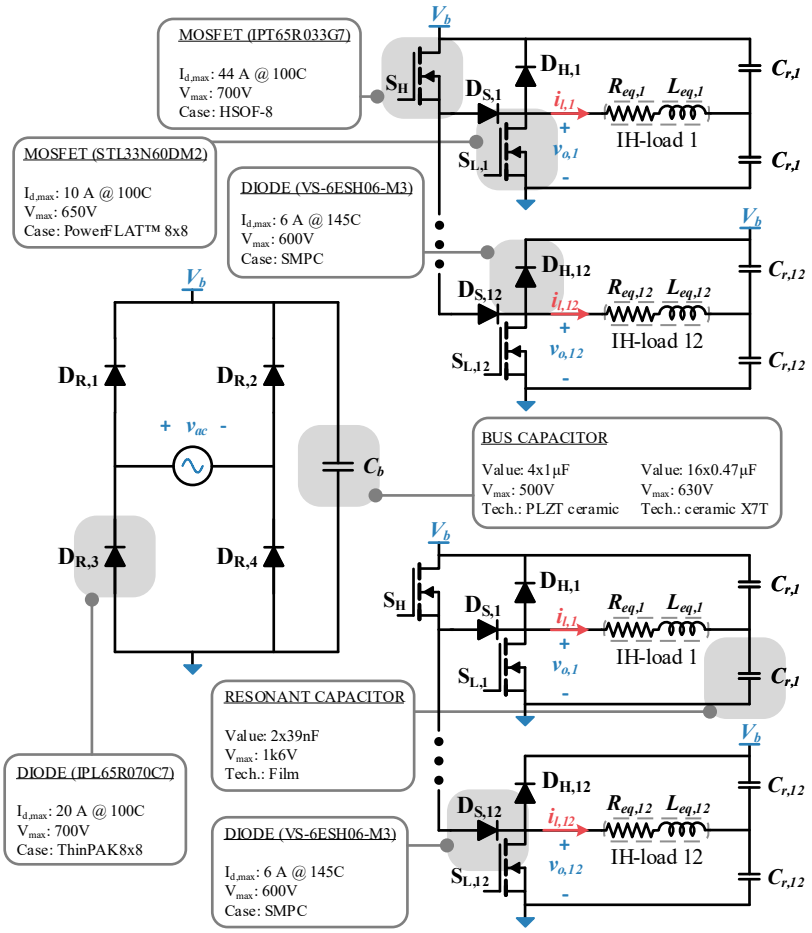


Fig. 4.4. Topology of the converter including the commercial devices used: diode bridge rectifier, bus capacitor, two 12-output ZVS resonant matrix inverters and resonant capacitors.

The driving circuit selection benefits of the single-column structure. Therefore, each low side transistor, which is referenced to GND, uses the commercial non-isolated driver UCC27532. The high side one, that requires isolation, is composed by the combination of the SI8261 optocoupled driver that operates as isolation barrier and the non-isolated IXDN609SI driver. Both transistors are activated at 12 V for minimizing channel resistance.

Each branch independent sensing circuitry presents a cost-effective implementation to minimize the requirements due to the high number of IH loads (Fig. 4.5). Resonant capacitor voltage sensing is considered for each branch to calculate transmitted power and load equivalent parameters as presented in [179]. Complementarily, a general current sensor placed on each inverter ground return is used to calibrate the considered constant values in the capacitor voltage derived power equation. The capacitor voltage values are adjusted to the measurement scale by means of a resistive divider and connected, with high impedance, by means of the AD8065 operational amplifier to the ADCS7476. The current measurement is implemented by the CDS4025 magnetoresistive current sensor whose output voltage is transmitted to the FPGA, that controls the prototype, by means also of a ADCS7476 integrated circuit. The measurements are complemented with a mains zero crossing detection circuit.

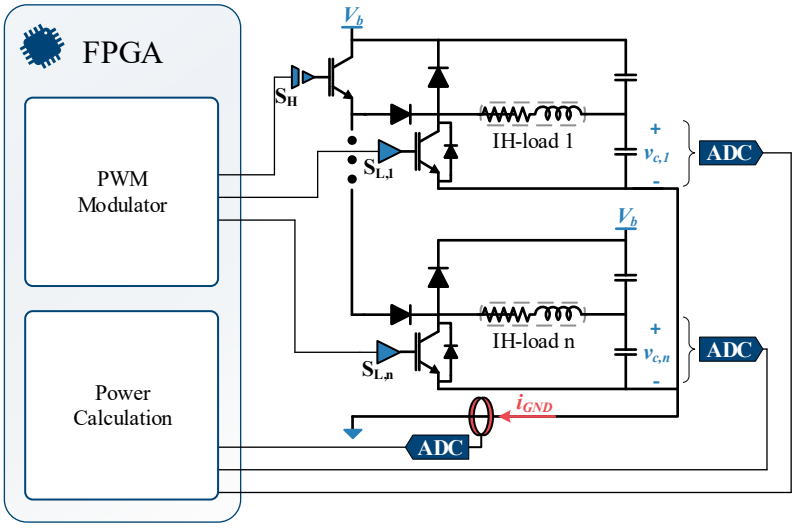


Fig. 4.5. Measurement system.

The prototype construction acknowledges the high number of semiconductor devices that require heat dissipation. Therefore, an implementation of the main power devices presented in Fig. 4.4 in an insulated metal substrate (IMS) printed circuit board (PCB) is selected to ensure an efficient cooling (Fig. 4.6 (a)). In order to do so, the devices require a surface mount (SMD) package. To minimize the parasitic inductances in the device gates, the driving circuitry are also placed over the IMS, ensuring proper control.

To minimize the routing complexity, the sensing circuitry and the resonant capacitors are mounted on an external FR4 PCB that is connected at the same level in order not to increase the vertical dimension and fit into a commercial cooktop case. The converter

prototype is shown in Fig. 4.6 (b), and the integration into the cooktop presented in Fig. 4.6 (c).

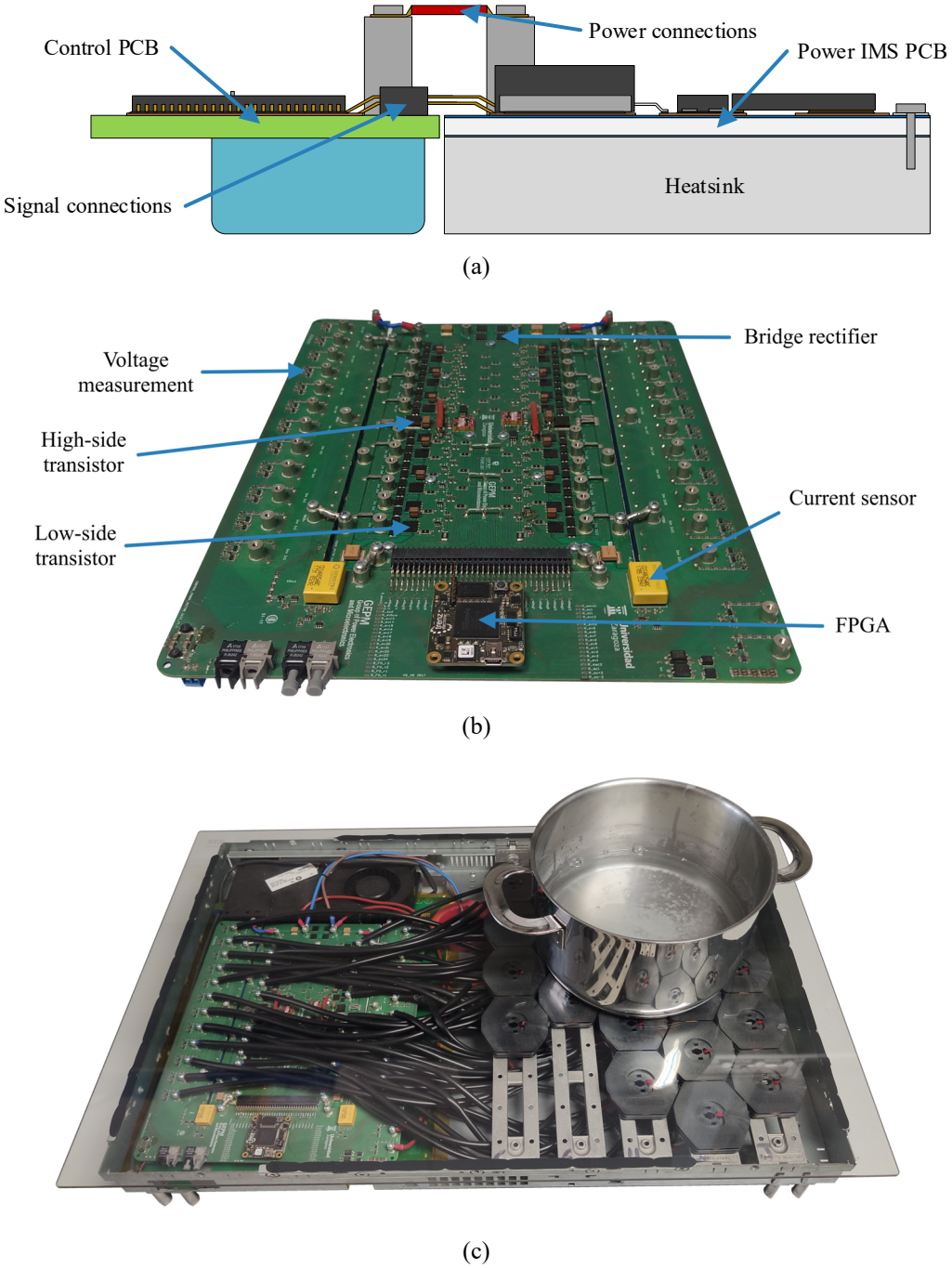


Fig. 4.6. Heat dissipation and construction of the prototype (a), functioning experimental prototype (b), and prototype integration in the cooktop (c).

4.1.1.2. Open loop evaluation

As it has been presented, the management of the complete inverter is done through an FPGA which enables a high frequency operation, by means of paralleling tasks, and versatile reconfiguration for the diverse test performed. The main hardware blocks

programmed in the FPGA to achieve a proper open loop control of the inverter are a PWM modulator, load identification block, power measurement block, IH load current measurement block, zero crossing detection, and UART communication with the PC.

All the data measured by the FPGA is transmitted to the user by means of user interface presented in Fig. 4.7. which shows the aforementioned parameters. Additionally, the operation mode menu allows to select the IH-load switching frequency and the active mains half-cycles.

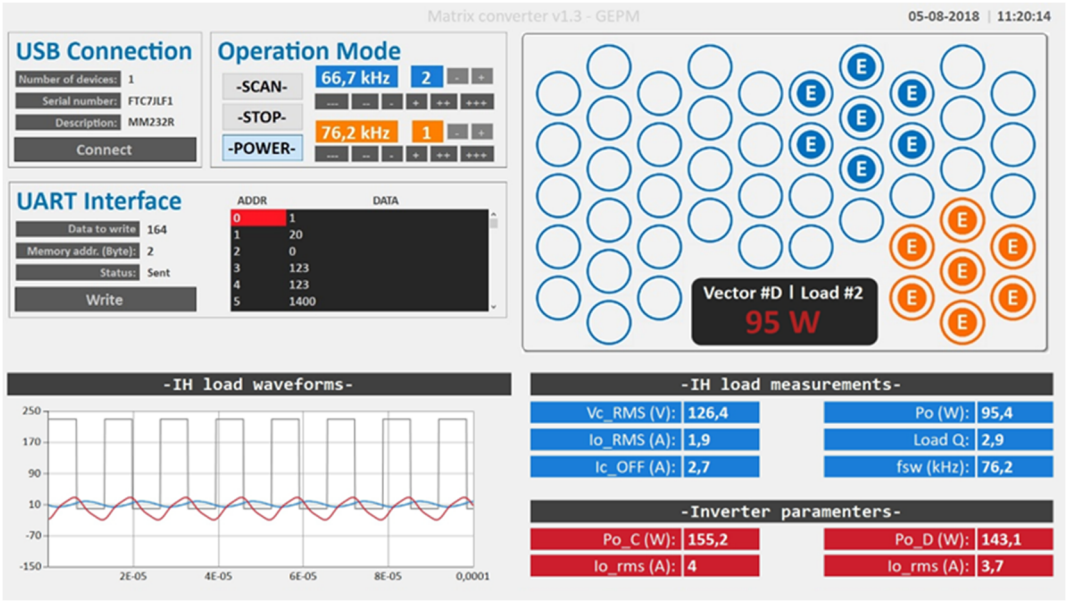


Fig. 4.7. User interface for the PC-FPGA communication.

Fig. 4.8 shows the main experimental waveforms of the proposed inverter operating with square waveform modulation and two different loads simultaneously at f_{sw} = 52 kHz.

The top side plot pane presents the high side transistor blocking voltage, $v_{DS,SH}$, and current, $i_{D,SH}$. There can be seen a voltage drop in $v_{DS,SH}$ during the dead time after the low side transistors $S_{L,1}$ and $S_{L,2}$ deactivate. This voltage drop occurs due to the current charging the parasitic capacitance of the series diode, $D_{S,1}$ and $D_{S,2}$, before starting to flow through $D_{H,1}$ and $D_{H,2}$ respectively. As the series diode opposes the current flow to the high side transistor, S_H source is floating mounted over V_b minus D_S parasitic capacitor charge.

The bottom side plot pane presents the applied voltage and the current trough both loads. There, the correct operation and low side transistor ZVS activation can be seen. Additionally, the mismatch between the equivalent parameters of the different pots can be qualitatively observed.

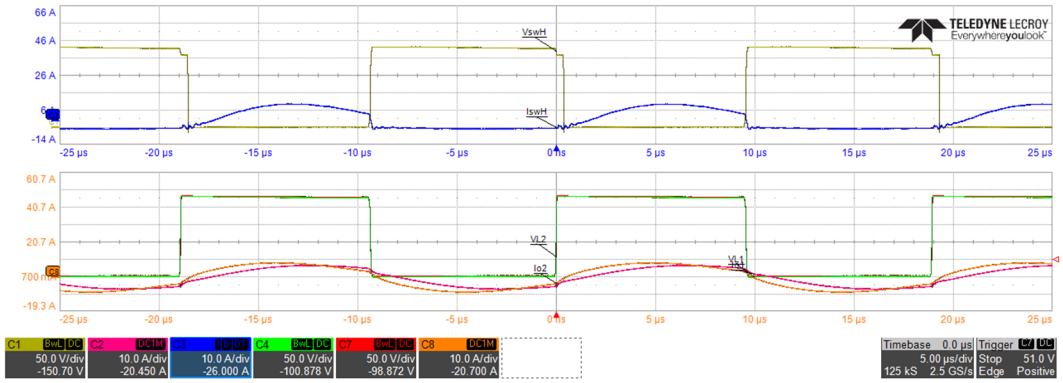


Fig. 4.8. Square waveform operation of the proposed converter at 52 kHz (a) and 90 kHz (b). From top to bottom: S_H blocking voltage, $v_{DS,SH}$, (50 V/div, yellow), SH current, $i_{D,SH}$, (10 A/div, dark blue), IH load 1 $v_{o,1}$ (50 V/div, red), $i_{l,1}$ (10 A/div, pink), and IH load 2 $v_{o,2}$ (50 V/div, green), $i_{l,2}$ (10 A/div, orange). Time axis: 5 µs/div.

Under SW modulation, efficiency of the proposed solution is also evaluated for a different number of same-pot IH loads. The results, presented in Fig. 4.9, show high efficiency for the full power range and a variety of loads. As it can be seen, low power presents the lower efficiency, which is still over 92.5% due to the high frequency requirement to achieve this power levels. For higher power and different number of loads, the parallelization implies a lower power share per load and therefore higher frequencies to provide the same overall power. This leads to more inductive behavior of the loads and therefore slightly lower efficiencies, as the turn-off current and the associated turn-off losses increase.

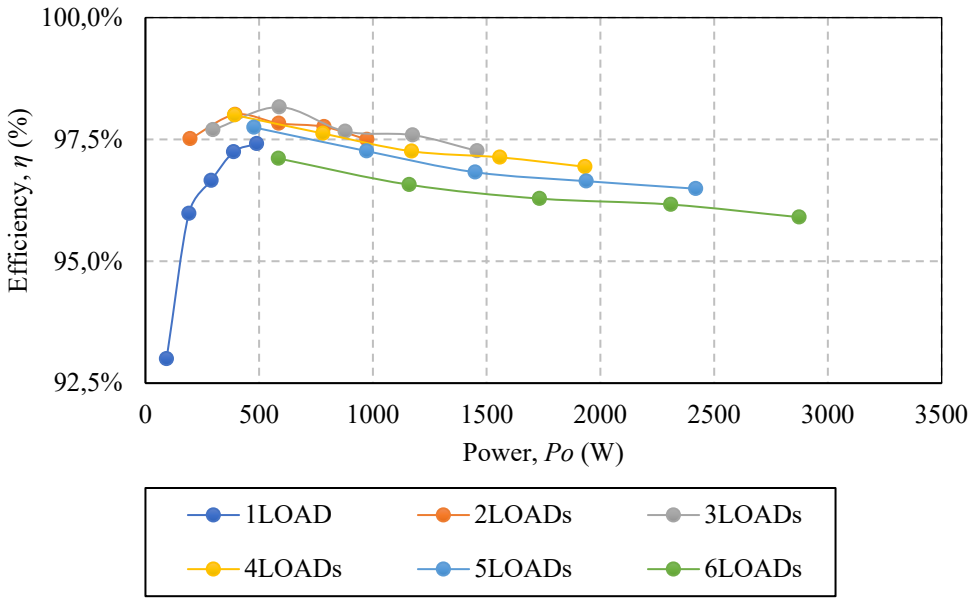
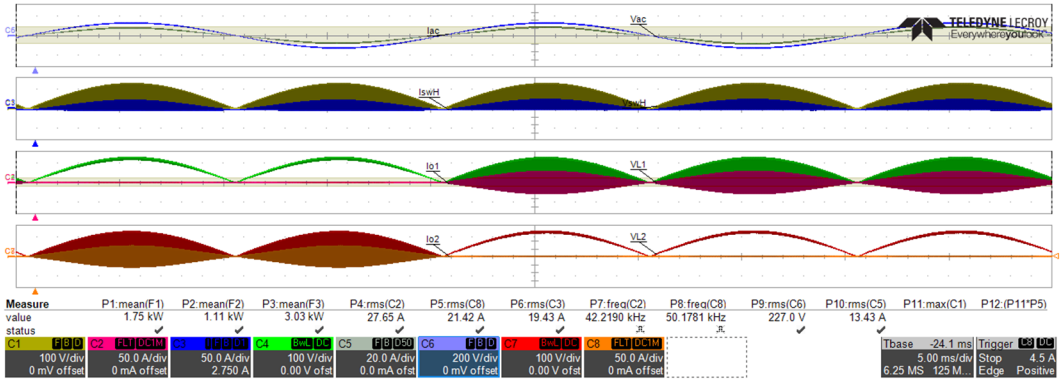
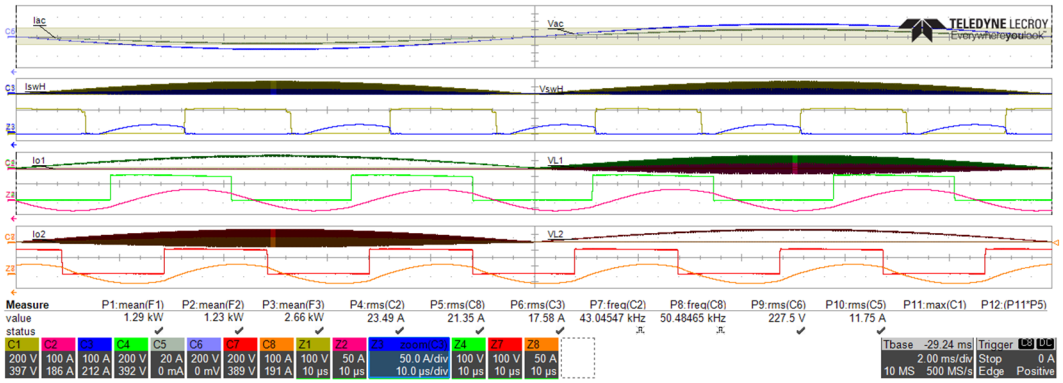


Fig. 4.9. Efficiency results of the proposed converter with up to 6 simultaneously connected IH loads.

Moreover, in order to achieve independent load power control, it is possible operate a mains synchronized LF-PDM complementarily to the SW modulation strategy presented on the previous captures. Fig. 4.10 shows the main waveforms of a two-load pulsating strategy (a) and the same results zoomed to different areas showing the different switching frequency depending on the active loads (b) to achieve a homogeneous power consumption.



(a)



(b)

Fig. 4.10. Mains synchronized LF-PDM + SW modulation strategies with unbalanced power transmission focusing on LF-PDM (a) and close loop to the SW waveforms (b). On each oscilloscope capture, from top to bottom: mains voltage, v_{ac}, (200 V/div, purple), mains current, i_{ac}, (20 A/div, grey), S_H blocking voltage, $v_{DS,SH}$, (100 V/div, yellow), SH current, $i_{D,SH}$, (50 A/div, dark blue), IH load 1 $v_{o,1}$ (100 V/div, red), $i_{l,1}$ (50 A/div, pink), and IH load 2 $v_{o,2}$ (100 V/div, green), $i_{l,2}$ (50 A/div, orange). Time axis: 5 ms/div.

Additionally, as both inverters are connected to the same bus, it is possible to phase shift their activation in order to improve the power consumption and therefore reduce the high frequency currents provided by the bus capacitor. In Fig. 4.11 the operation at 75 kHz with phase shift can be seen.

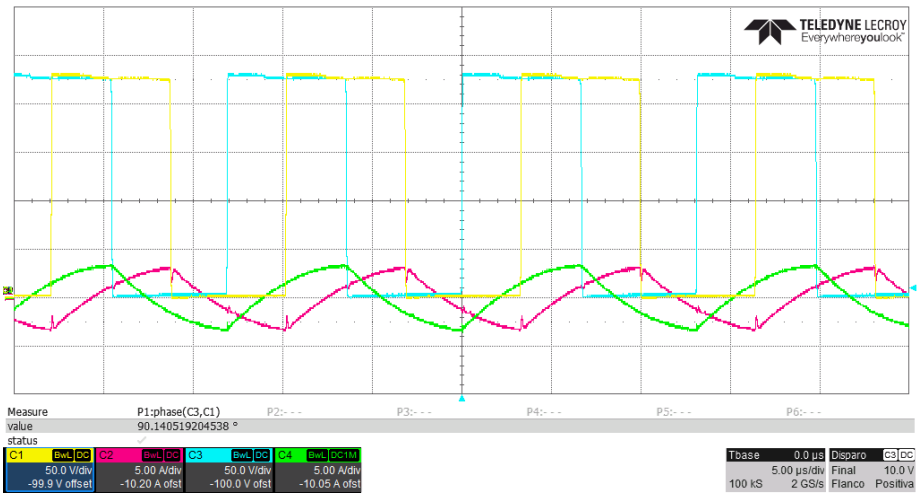


Fig. 4.11. Square waveform operation at 75 kHz with a phase between inverters of 90º. From top to bottom: IH load 1 $v_{o,1}$ (50 V/div, yellow), $i_{l,1}$ (5 A/div, pink), and IH load 2 $v_{o,2}$ (50 V/div, light blue), $i_{l,2}$ (5 A/div, green). Time axis: 5 µs/div.

Besides the correct power transfer, one of the most relevant circuits tested on the prototype implementation has been the load identification method by means of the resonant capacitor voltage. The results obtained have proven to present an accuracy comparable to the results obtained by first harmonic approximation. Additionally, considering independent IH load characterization parameters, a DNN has been proposed and trained, using the experimental results, to detect the complete pot [162].

4.2. Flexible surface

Flexible surface cooktops present a reduced number of coils and therefore lower control complexity, leading to cost-effective implementations and thus bigger market share. The principle behind them is the usage of inductors without rotational symmetry so that medium-big pots cover more of one inductor in a certain axis, usually the cooktop depth, allowing the free positioning of the pot. This leads to a more comfortable cooking experience and the possibility to select pots with different shapes. The coils are developed to present a good proportion between width and depth to cover the maximum of the surface while providing an adequate heating profile in the pot.

The design specifications for these commercial inductors are presented on TABLE 4.2. One of the main differences that should be taken into account is the higher power rating of the inductors. Considering the 1800 W maximum output, any pot that covers at least two inductors can receive the maximum total power. As a consequence, the activation of the remaining inductors, that present lower percentual coverages, can be neglected, leading to less variation on the equivalent parameters.

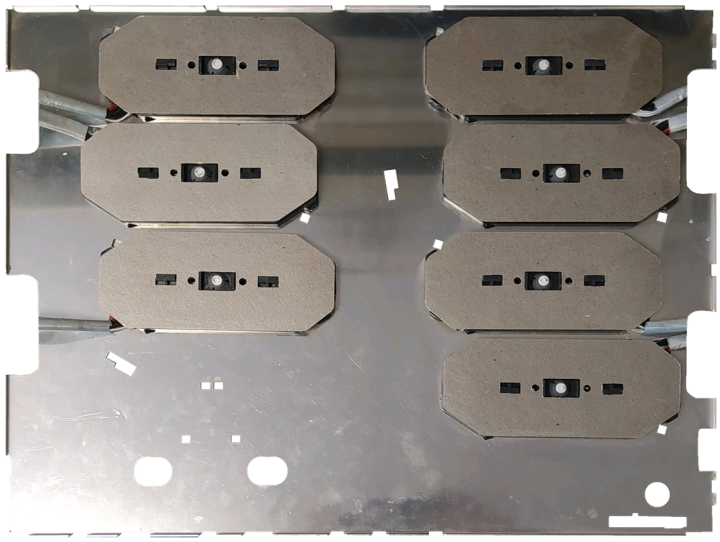


Fig. 4.12. Freeinductor oval inductor distribution over the cooktop surface.

The inductor distribution of Fig. 4.12 is usually powered by means of two mains phases since the number of coils to be powered from the same phase oscillates around 4, depending on the cooktop. Therefore, the proposed prototypes may vary in the number of outputs in order to fulfill the requirements while achieving high power density implementations.

TABLE 4.2. MAIN DESIGN SPECIFICATIONS

PARAMETER	VALUE
Supply voltage, v_{ac}	230 V, 50 Hz
Rectified peak voltage, V_b	325 V
Inductor power, $P_{o,i}$	0 – 1800 W
Total power, $P_{o,max}$	0 – 3600 W
Load 1 quality factor, Q	2.15 (2.15 – 3.69)
Load 1 equivalent inductance, L_{eq}	60 uH (60 – 82 uH)
Load 2 quality factor, Q	2.28 (2.28 – 4.30)
Load 2 equivalent inductance, L_{eq}	64 uH (64 – 117 uH)
Load 3 quality factor, Q	2.59 (2.59 – 4.59)
Load 3 equivalent inductance, L_{eq}	67 uH (67 – 109 uH)
Switching frequency range, f_{sw}	25 – 75 kHz

4.2.1. 5-output Si IGBT prototype

In order to evaluate the adaptability of the single-column matrix-based ZVS resonant inverter to be integrated in a commercial platform with a medium number of 1800 W inductors, a 5-output prototype is selected.

To achieve a fair comparison with the power stage of the cooktops in the market, the proposed prototype relies on similar technology, i.e. power devices, measurements, and driving circuits. Therefore, the uncertainties faced are reduced to the new topology implementation, and the results would also prove its adaptability to mature technologies on the market, such as the high-side bootstrap supply.

4.2.1.1. Implementation

The proposed devices for the designed prototype are included in the schematic of Fig. 4.4. In this case, the transistor technology is IGBT in order to achieve a cost-effective implementation. Additionally, due to the lower imbalance between each branch rated power and the total power of 3600 W, both high-side and low-side transistors are selected to be equal.

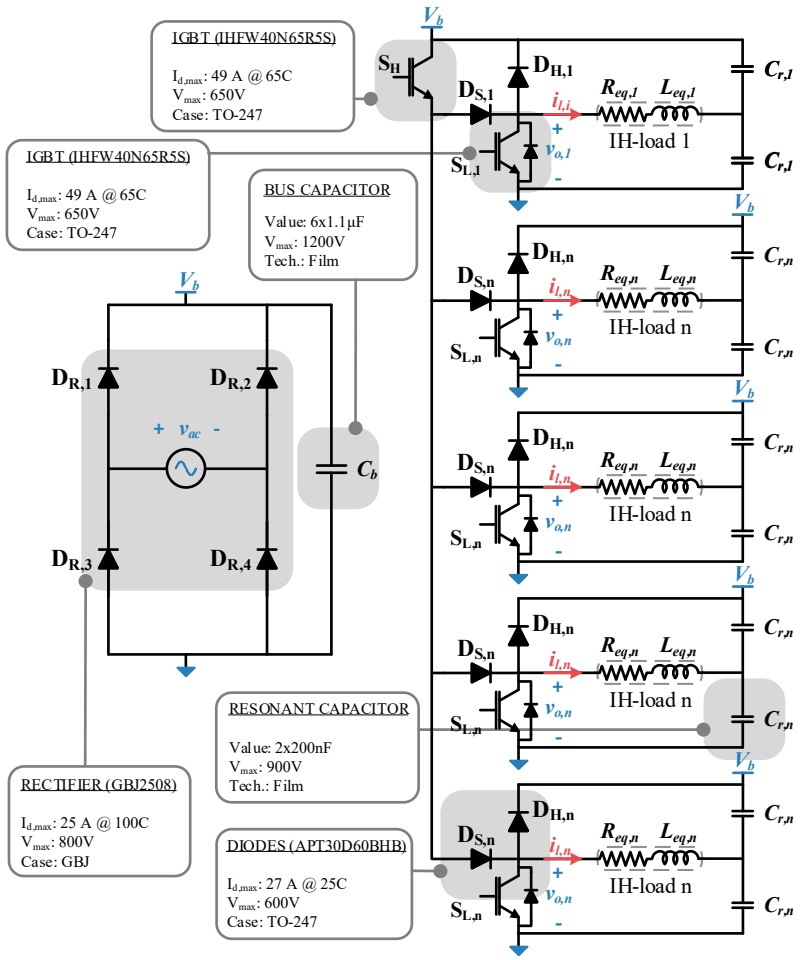
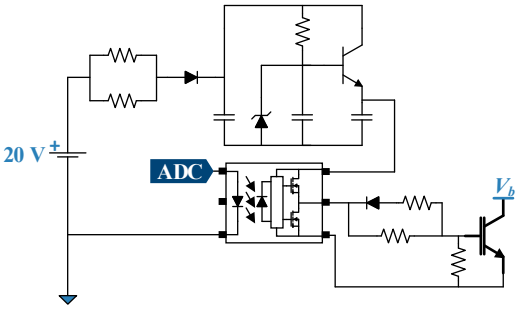


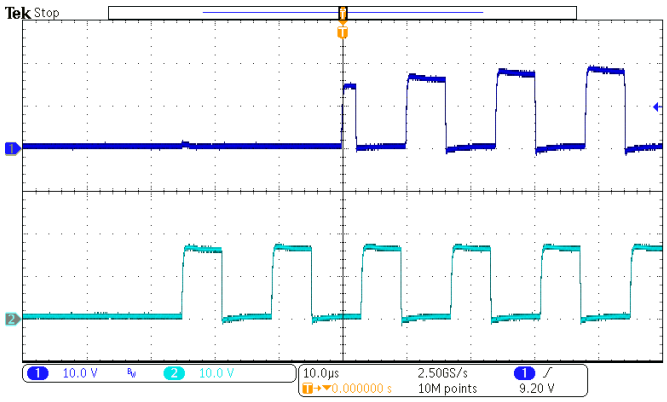
Fig. 4.13. Topology of the converter including the commercial devices used: diode bridge rectifier, bus capacitor, 5-output ZVS resonant matrix inverter, and resonant capacitors.

This technology allows to minimize the output capacitance of the high-side transistor and thus its contribution to the power losses. In addition, to minimize turn-off losses, a capacitive snubber network is included on each branch, provided that the low-side diode generates the required discharge path.

The diode selection follows a holistic approach. It combines in the same packaging the high-side diode and the series diode, balancing the higher $D_{S,i}$ losses with the lower $D_{H,i}$ losses and achieving an acceptable level for the considered package and thus proper cooling. To do so, a tradeoff between switching properties and forward voltage has to be achieved.



(a)

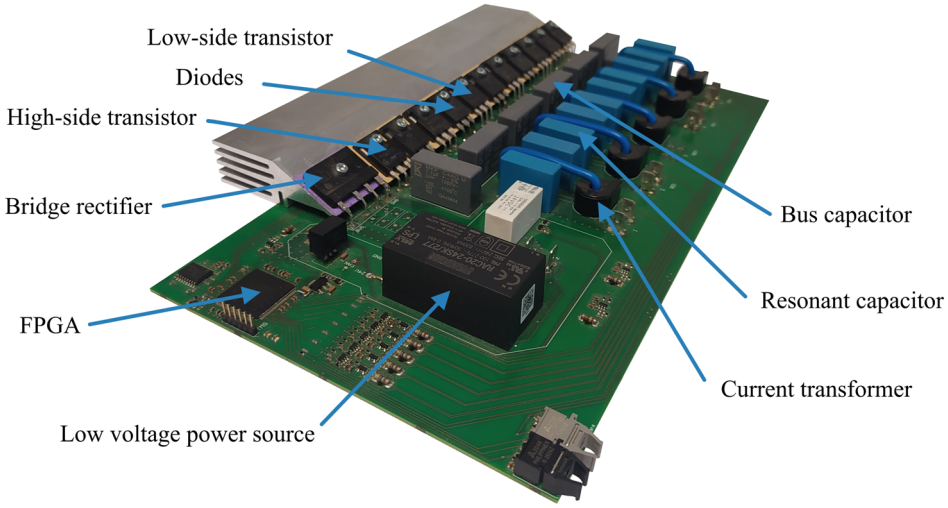


(b)

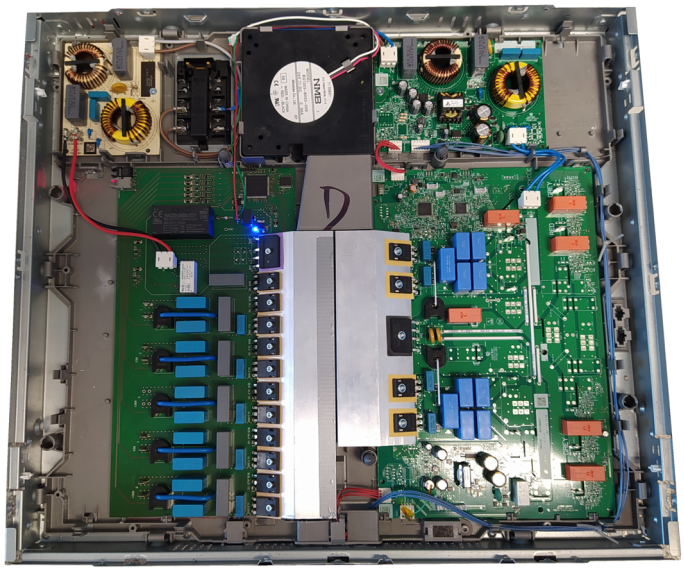
Fig. 4.14. Bootstrap circuit used for the triggering of the high-side transistor (a) and bootstrap operation waveforms (b). On the oscilloscope capture, from top to bottom: S_H gate voltage, $v_{GS,SH}$, (10 V/div, dark blue), S_L gate voltage, $v_{GS,SL}$, (10 V/div, light blue). Time axis: 10 µs/div.

Following a similar approach as with the switching technology, the driving circuit uses the ACPL-P341 optocoupled driver for both the high side and low side transistors to provide additional isolation and because of economies of scale reasons. The high side transistor isolated gate voltage is achieved by means of a bootstrap circuit that includes a voltage regulator (Fig. 4.14 (a)). In Fig. 4.14 (b) the bootstrap proper operation can be seen, proving that the proposed topology generates a charging path for the bootstrap

structure during the activation of any of the low-side transistors. However, high side gate voltage is limited to 20 V minus the voltage drop in the series diode and low-side transistor.



(a)



(b)

Fig. 4.15. Complete experimental prototype (a) and prototype integration in the cooktop (b).

The considered measurement system performs current sensing through a current transformer and the ADC ADCS7476 to convert the voltage. Additionally, two voltage measurements connected to the mains input allow to generate the mains synchronization signal.

The prototype implementation follows the same principle as the technology selection. Therefore, the base PCB is a two-layer FR4 where the components are organized

according to its branch in order to minimize the current loops. The bus capacitor is distributed, with a capacitor at the output of the rectifier and the remaining close to each of the branches. The power devices are placed over a heatsink with forced cooling. The converter prototype is shown in Fig. 4.15 (a), and the integration into the cooktop presented in Fig. 4.15 (b).

4.2.1.2. Open loop evaluation

Both measurement and control are implemented in a FPGA integrated in the PCB. The main blocks integrated are the PWM modulator, IH load power and current measurement blocks, mains zero crossing detection, and communication with the PC.

To verify the proper operation, the main experimental waveforms of the converter supplying 3.6 kW to two IH loads are shown in Fig. 4.16.

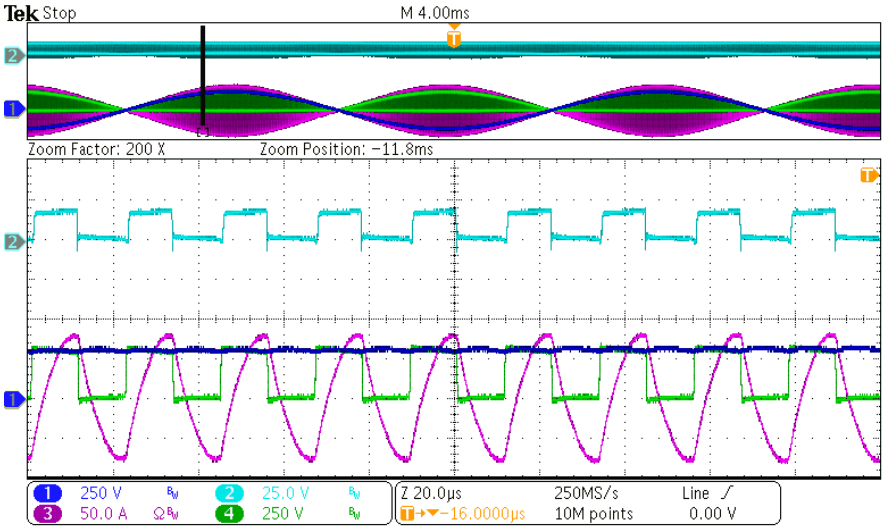
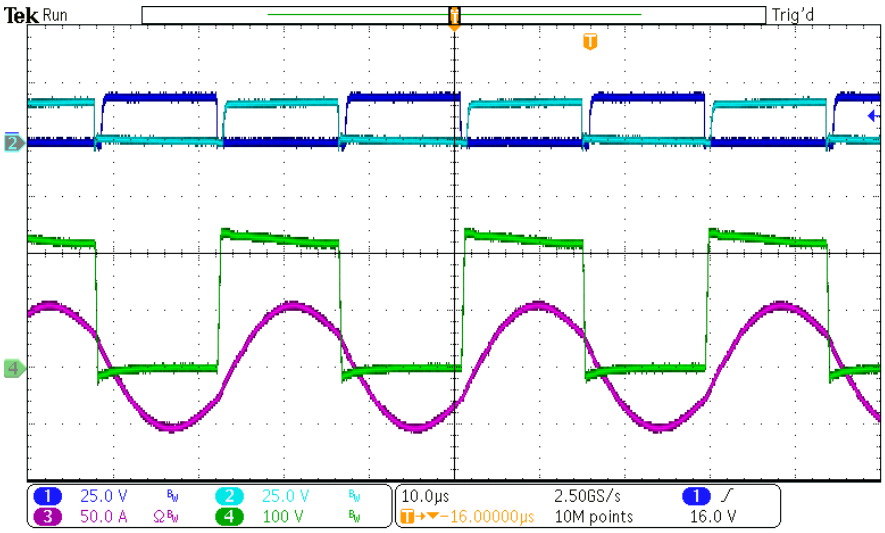
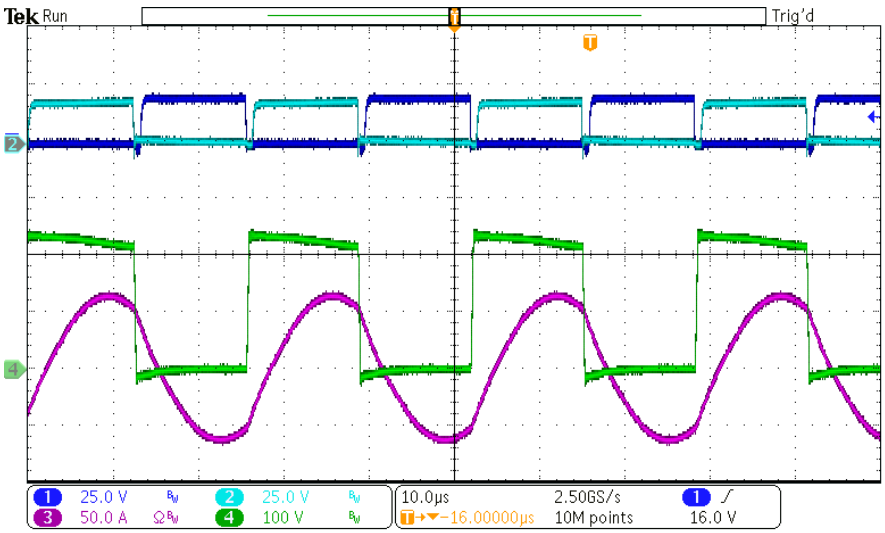


Fig. 4.16. Main experimental waveforms of the converter. On the oscilloscope capture, from top to bottom: S_H gate voltage, $v_{GS,SH}$, (25 V/div, light blue), mains voltage, v_{ac}, (250 V/div, dark blue), common rail $v_{o,1}$ and $v_{o,2}$ voltages (250 V/div, green), and $i_{l,1} + i_{l,2}$ (50 A/div, pink). Time axis: 20 µs/div.

Additionally, the evaluation of the increase in the overall current due to the parallelization of branches can be observed in Fig. 4.17. The comparison between both operation modes providing 3.6 kW to two (a) or three (b) different loads show that, in order to provide the same power to a higher number of loads, the individual power is necessarily reduced and therefore the selected switching frequency should increase further from resonance. As a consequence of the frequency displacement, the loads present a more inductive behavior and therefore the current levels are higher for the same total transmitted power.



(a)



(b)

Fig. 4.17. Main experimental waveforms of the converter when providing 3600 W to two (a) or three (b) loads. On each oscilloscope capture, from top to bottom: S_H gate voltage, $v_{GS,SH}$, (25 V/div, light blue), S_L gate voltage, $v_{GS,SL}$, (25 V/div, dark blue), common rail v_o voltage (250 V/div, green), and total load current i_l (50 A/div, pink). Time axis: 10 µs/div.

The snubber operation is also evaluated to ensure proper power losses reduction and reduced *dv/dt*. The current flow through a 15 nF snubber capacitor can be seen in Fig. 4.18 for 1800 W transmission with SW operation, showing that a proper path is generated for the capacitor discharge at the low side transistor turn off.

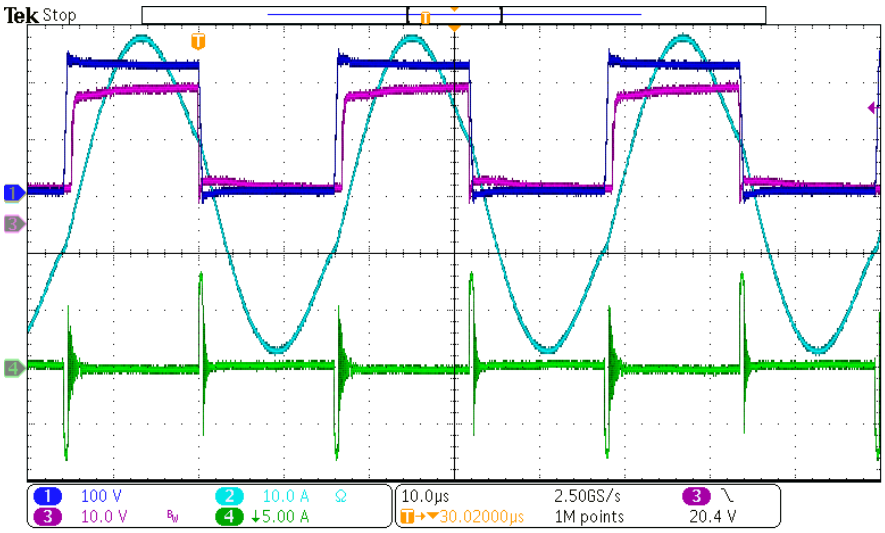


Fig. 4.18. Current flow through a branch snubber capacitor when providing 1800 W. From top to bottom: S_H gate voltage, $v_{GS,SH}$, (10 V/div, pink), IH load voltage, $v_{o,1}$, (100 V/div, dark blue), IH load current $i_{l,1}$ (10 A/div, light blue), and snubber capacitor current (5 A/div, green). Time axis: 10 µs/div.

However, when using non-complementary strategies, the snubber discharge path is not generated prior to the subsequent transistor activation, leading to increased turn-on losses. For example, for the case of NC-PDC depicted in Fig. 4.19, the snubber operates correctly on the high-side transistor activation and deactivation. Nevertheless, as the capacitor charges during the high side diode conduction time, it is discharged through the low-side transistor on its activation, increasing the power losses.

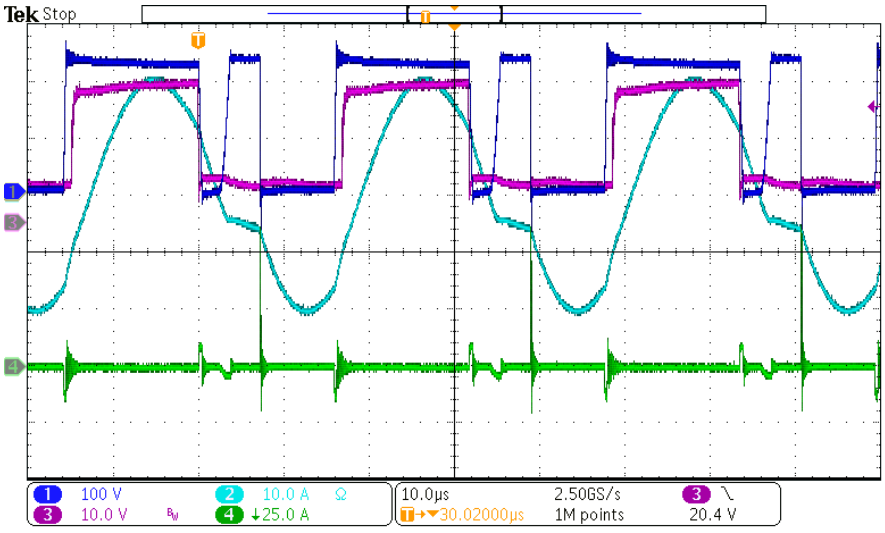


Fig. 4.19. Current flow through a branch snubber capacitor when providing 1000 W and operating with a NC-PDC strategy. From top to bottom: S_H gate voltage, $v_{GS,SH}$, (10 V/div, pink), IH load voltage, $v_{o,1}$, (100 V/div, dark blue), IH load current $i_{l,1}$ (10 A/div, light blue), and snubber capacitor current (5 A/div, green). Time axis: 10 µs/div.

If snubber capacitances are required for its use in combination with NC strategies to reduce *dv/dt* of the converter, they must be implemented by means of dissipative snubber networks, with a high penalty over efficiency and, consequently, are not considered on this thesis.

4.2.1.3. Closed loop evaluation

Once the inverter is validated in open loop, closed loop operation can be tested. In order to do so, an additional controller block is coded into the FPGA. It implements a multiplexation strategy following the considerations on Section 3.3, which is the operation considered during the prototype proposal and design.

In Fig. 4.20 the startup sequence is presented. This sequence uses the combinations that require a minimum number of IH loads active simultaneously to transmit the total power and calculates the switching frequency of each combination to minimize the input power fluctuation. As it can be seen, due to the power rating of the inductors, only two IH loads are necessary to be activated simultaneously, reducing the switching frequency and therefore the overall current, and improving efficiency. Subsequently, the algorithm calculates the duration, in number of cycles, of each combination so that the desired power is transmitted to each load. This process is done iteratively as it can be seen.

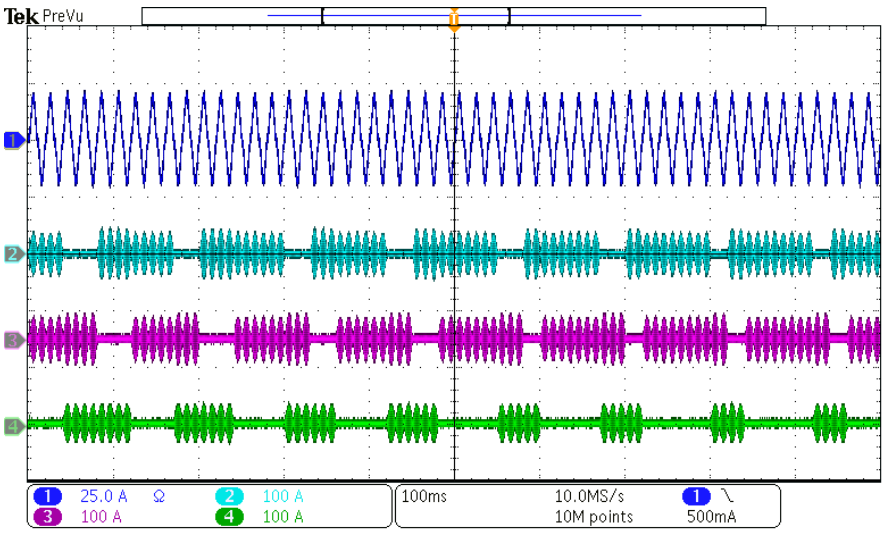
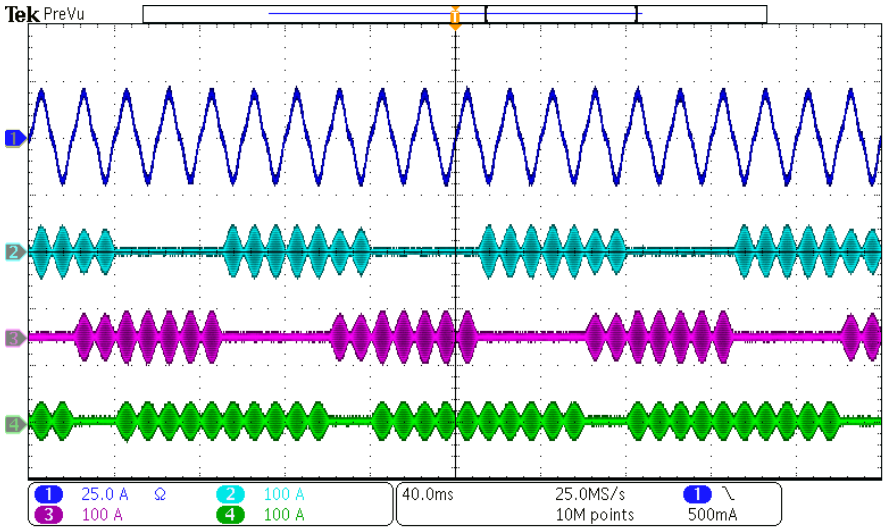
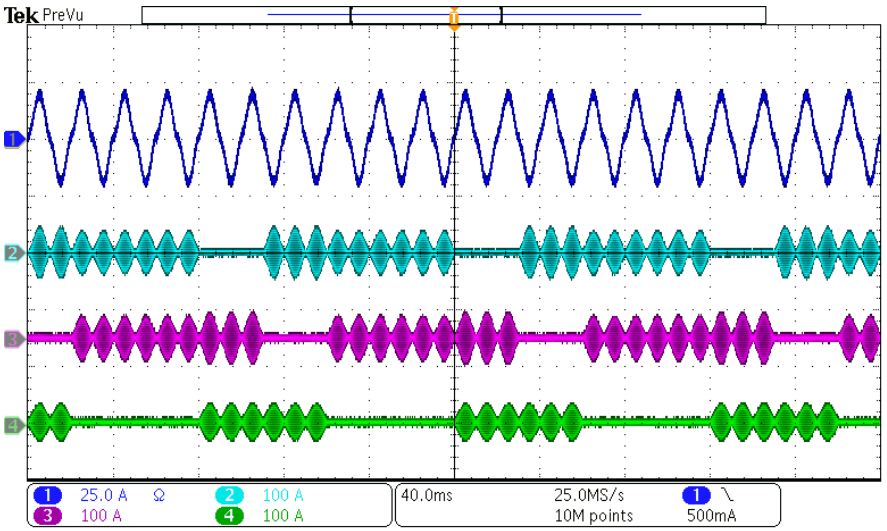


Fig. 4.20. Initial transient waveforms of the pulse density modulation strategy powering two pots that cover three inductors for an unbalanced objective power. From top to bottom: Input current, i_{ac}, (25 A/div, dark blue), IH load 1 inductor current, $i_{l,1}$, (100 A/div, cyan), IH load 2 inductor current, $i_{l,2}$, (100 A/div, pink), IH load 3 inductor current, $i_{l,3}$, (100 A/div, green). Time axis: 100 ms/div. Starting parameters: $Act_{i,1} = (1,1,0)$, $f_{sw,1} = 35.2$ kHz, $d_1 = 0.33$, $Act_{i,2} = (0,1,1)$, $f_{sw,2} = 34.0$ kHz, $d_2 = 0.33$, $Act_{i,3} = (1,0,1)$, $f_{sw,3} = 34.0$ kHz, $d_3 = 0.33$, and ending parameters: $Act_{i,1} = (1,1,0)$, $f_{sw,1} = 35.2$ kHz, $d_1 = 0.5$, $Act_{i,2} = (0,1,1)$, $f_{sw,2} = 34.0$ kHz, $d_2 = 0.25$, $Act_{i,3} = (1,0,1)$, $f_{sw,3} = 34.0$ kHz, $d_3 = 0.25$.

The steady-state for a balanced objective power (a) and unbalanced objective power (b) are presented in Fig. 4.21. In both cases it can be seen that the switching frequencies depend only on the combination of active loads, decoupling the problem of input power fluctuation from the one of the transmitted power.



(a)



(b)

Fig. 4.21. Stationary stage waveforms of the pulse density modulation strategy powering two pots that cover three inductors. For a balanced objective power (a) and unbalanced objective power (b). In each image, from top to bottom: Input current, i_{ac}, (25 a/div, dark blue), IH load 1 inductor current, $i_{l,1}$, (100 A/div, cyan), IH load 2 inductor current, $i_{l,2}$, (100 A/div, pink), IH load 3 inductor current, $i_{l,3}$, (100 A/div, green). Time axis: 40 ms/div. Parameters for (a): $Act_{i,1} = (1,0,1)$, $f_{sw,1} = 34.0$ kHz, $d_1 = 0.42$, $Act_{i,2} = (1,1,0)$, $f_{sw,2} = 35.2$ kHz, $d_2 = 0.14$, $Act_{i,3} = (0,1,1)$, $f_{sw,3} = 34.0$ kHz, $d_3 = 0.42$, and for (b): $Act_{i,1} = (1,0,1)$, $f_{sw,1} = 34.0$ kHz, $d_1 = 0.25$, $Act_{i,2} = (1,1,0)$, $f_{sw,2} = 35.2$ kHz, $d_2 = 0.5$, $Act_{i,3} = (0,1,1)$, $f_{sw,3} = 34.0$ kHz, $d_3 = 0.25$.

4.2.2. 12-output Si IGBT prototype

The previously proposed prototype proves the proper operation of the topology when powering medium power loads. However, the need of snubber circuits to control the power losses level limits the application of alternative modulation strategies. In order to improve the control versatility and provide a high power density implementation, a two phase prototype has been designed and developed to control a complete cooktop irrespective of its size.

4.2.2.1. Implementation

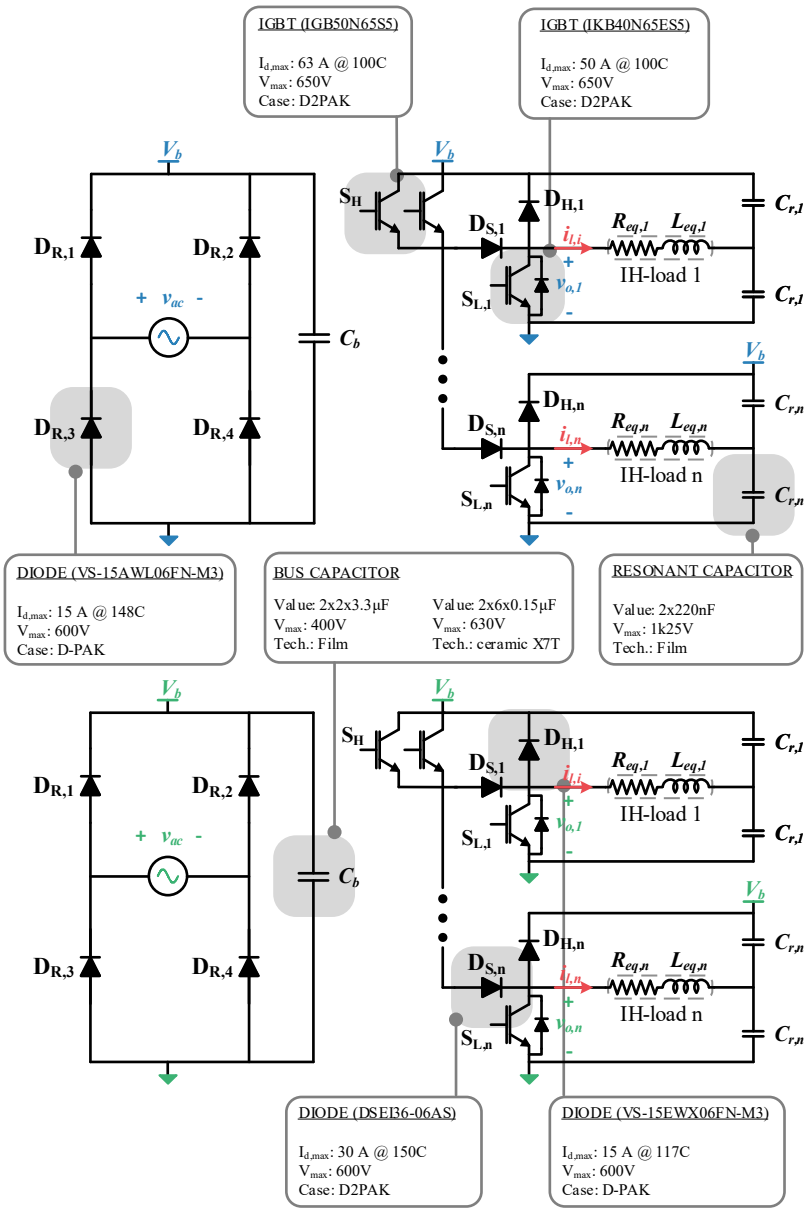


Fig. 4.22. Topology of the converter including the commercial devices used: diode bridge rectifiers, bus capacitors, two 6-output ZVS resonant matrix inverter and resonant capacitors.

The proposed converter is based on IGBT technology and presents a device selection that ensures high efficiency even operating without requiring additional snubber networks. The schematic, which includes the selected power devices, is depicted in Fig. 4.22.

One of the main differences in the prototype design is that the diodes are selected individually to improve its performance. The high-side diode present fast dynamics to provide proper commutation while the series diode, whose deactivation is driven by the high-side transistor, is optimized for conduction while presenting fast dynamics to ensure independent load activation.

Additionally, the topology presents a duplicity of the high-side transistor. This provides a robust implementation by sharing the current and therefore minimizing the power losses. However, in order to evaluate the operation with the minimal amount of switching devices the selected transistor is calculated not to require parallelization for the considered number of IH loads. This transistor presents no antiparallel diode as it is not required for the application.

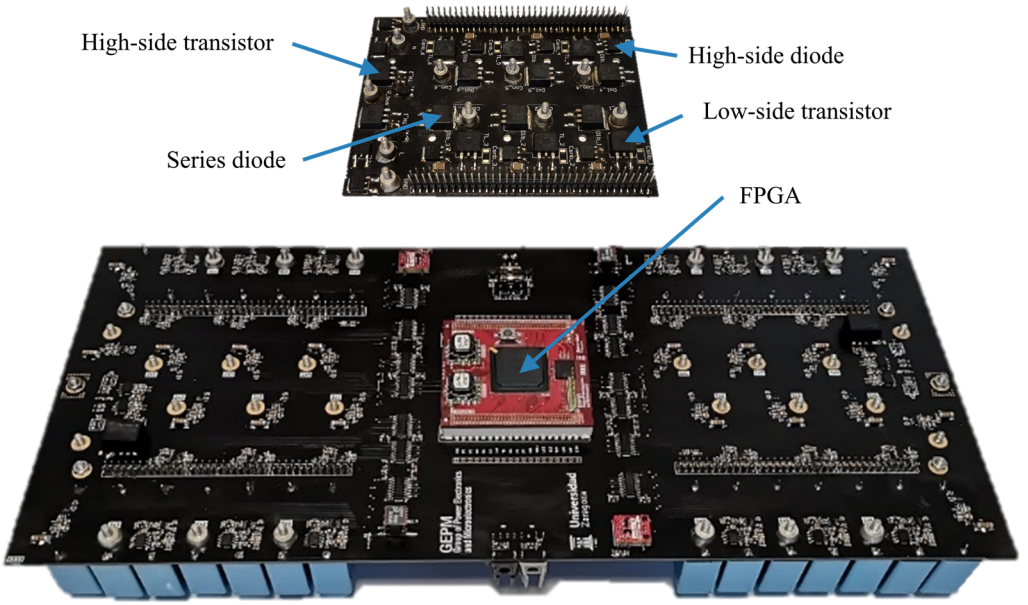
The driving circuit benefits from the column structure and thus uses commercial non isolated driver 1EDN8511B for the low-side transistor and isolated 1EDI60N12AF for the high-side one.

However, given the two-phase implementation, isolation among them and with the control and communications is required. The FPGA is connected to the measurements and driving circuits trough SI8660BC-B-IS1 isolators. The 5V required for powering ADC and sensors are provided from the control section trough the MTU2S0505MC isolated DCDC and the 15 V for the driving circuitry trough the converter NXE2S1212MC.

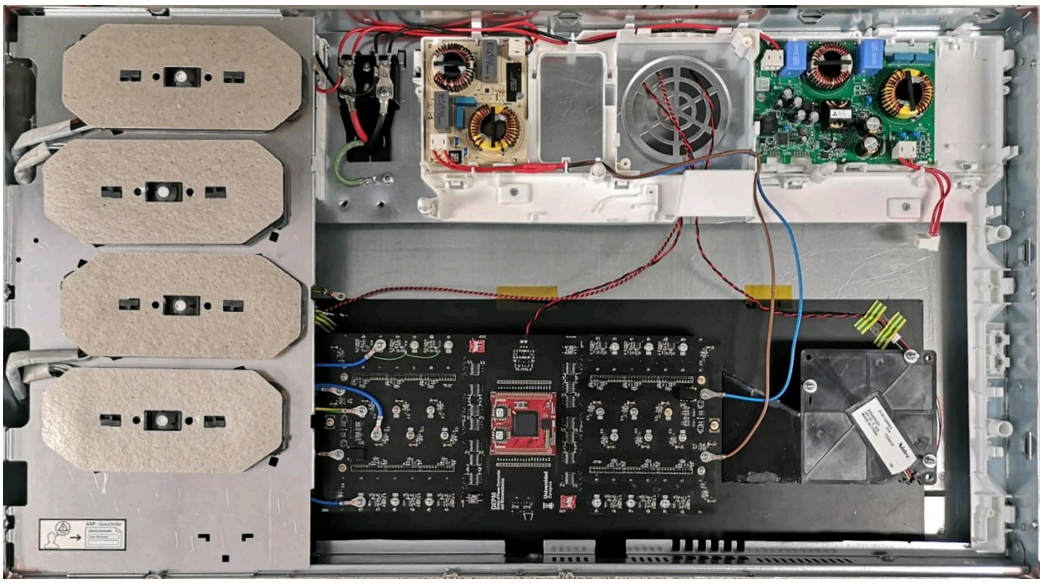
The measurement system presents both load voltage and load current measurements in order to increase power calculation precision. Additionally, external resonant capacitor voltage sensing modules have been designed in order to implement some of the more complex control strategies. The selected current sensor is ACS730KLCTR-40AB-T and the voltage is directly feed from the resistive divider to the ADCS7476 ADC.

The prototype construction aims for a high power density and it therefore includes all the phase power devices into a single IMS PCB, requiring an area of 110 cm^2. This implementation achieves a good heat dissipation (1,27ºC/W) but requires the power flow

through the control PCB. This PCB presents the driving, sensing, control, and capacitances and provides structural support. The converter prototype is shown in Fig. 4.23 (a), and the integration into the cooktop presented in Fig. 4.23 (b).



(a)



(b)

Fig. 4.23. Complete experimental prototype (a) and prototype integration in the cooktop (b).

4.2.2.2. Open loop evaluation

The converter control is implemented in a custom FPGA module. The main hardware blocks programmed in the FPGA are the same as the ones of the previous prototypes,

taking advantage of the modularity and flexibility of the reprogrammable implementation. A PWM modulator, a IH load power and current measurement block, a mains zero crossing detection, and UART communication with the PC are the basic blocks.

In order to control the inverter operation through the modulation parameters, and to measure the overall and independent transmitted power, a user interface has been developed focusing on the power devices (Fig. 4.7). It presents an overview of the topology, and it allows to modify the general modulation parameters, such as the switching frequency, and the independent low-side transistor parameters. In order allow this non-complementary modulation, a more complex PWM modulator has been implemented.

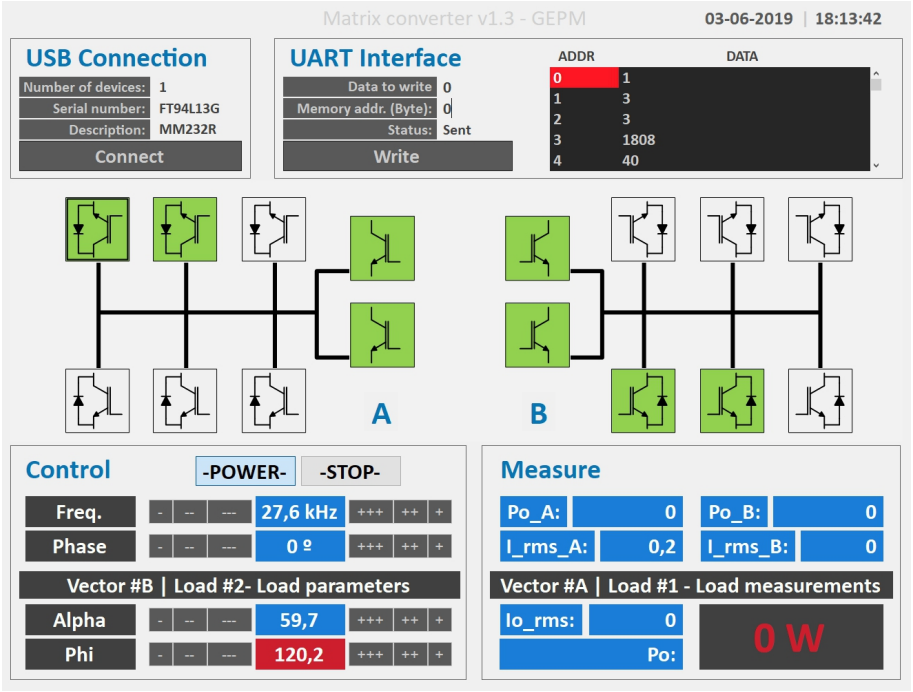


Fig. 4.24. User interface to control the 12-output two-phase inverter.

The proper operation of the converter is presented in Fig. 4.25, where the maximum rated power of 7.2 kW is transferred to two different loads connected each to a different phase. The waveforms show the SW applied voltage to the load and the current through the pair of inductors that power each load.

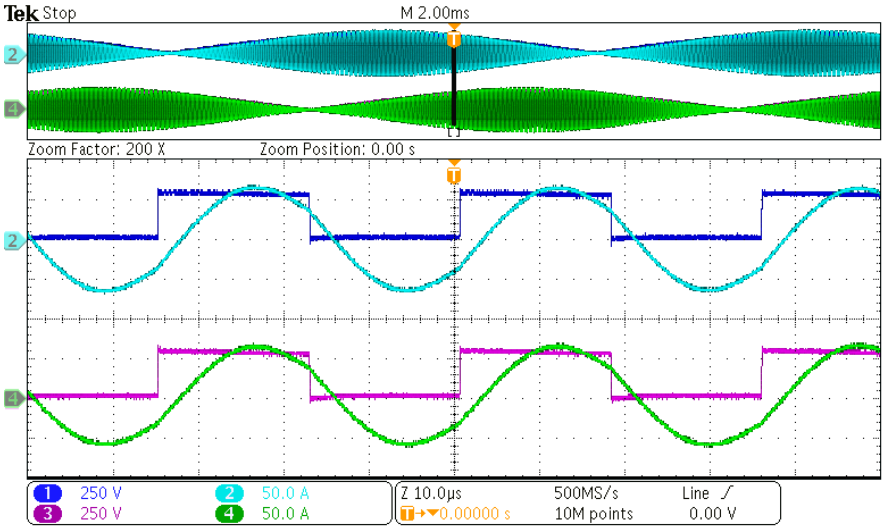


Fig. 4.25. Waveforms for 4 IH loads powered from two phases each at full power. From top to bottom: Phase 1 output voltage, $v_{o,1}$, (250 V/div, dark blue), Phase 1 inductor current, i_1, (50 A/div, cyan), Phase 2 output voltage, $v_{o,2}$, (250 V/div, pink), Phase 2 inductor current, i_2, (50 A/div, green). Time axis: 50 µs/div.

Once SW operation is validated, and given that the objective of this prototype proposal is to increase the versatility, the non-complementary modulation strategies, presented on Section 3.4, have been tested. As it can be seen in Fig. 4.26 the flexibility of this strategies enable independent application for different IH loads of the same inverter.

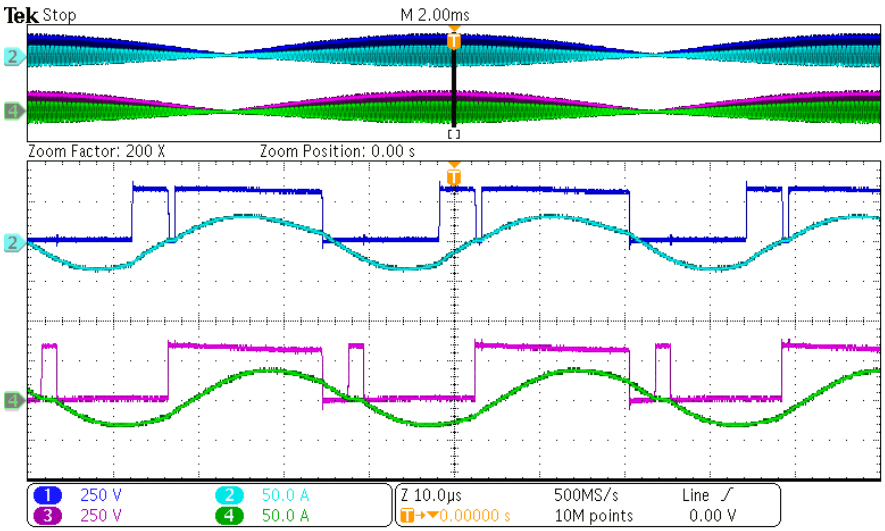
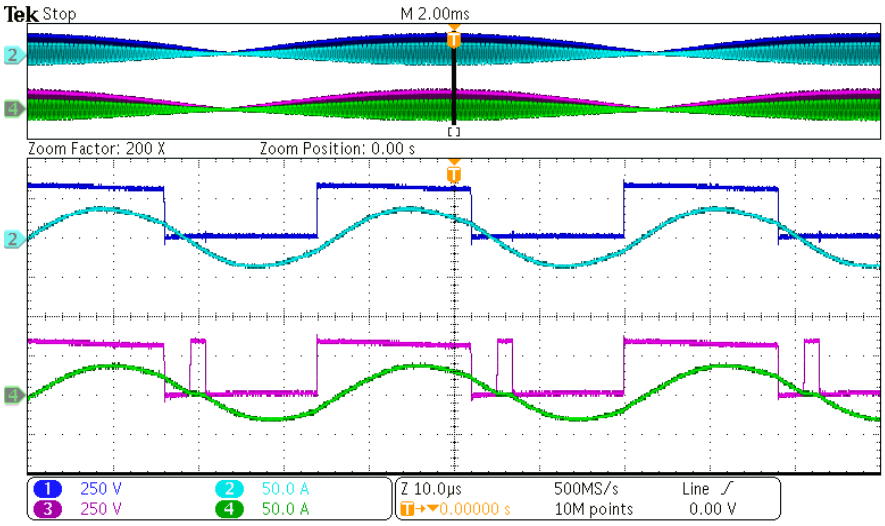


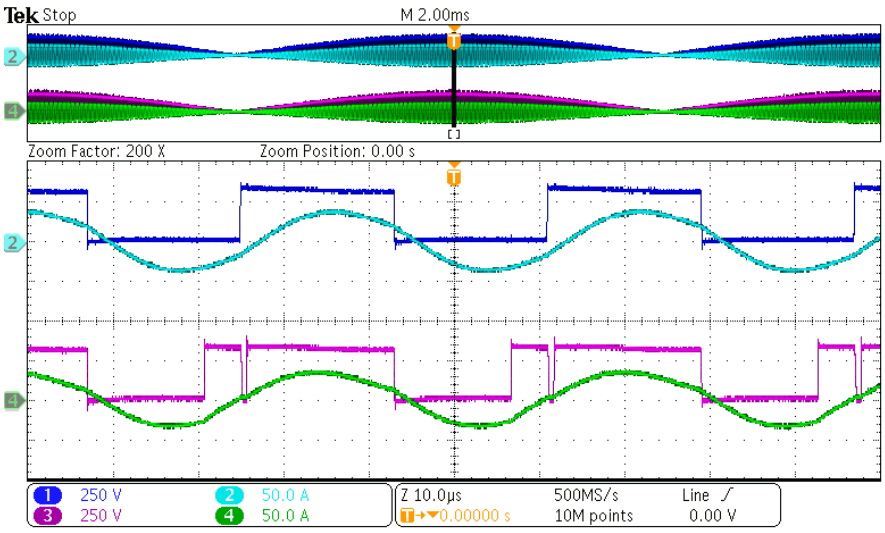
Fig. 4.26. Waveforms for two IH loads powered simultaneously with NC-PDC strategy and NC-PDC strategy, being P_o = 1600 W for both. From top to bottom: Load 1 output voltage, $v_{o,1}$, (250 V/div, dark blue), Load 1 inductor current, $i_{l,1}$, (50 A/div, cyan), Load 2 output voltage, $v_{o,2}$, (250 V/div, pink), Load 2 inductor current, $i_{l,2}$, (50 A/div, green). Time axis: 10 µs/div.

Besides the independency on the control, the application of these strategies allows a full-range-controlled precise power transfer to the different loads. The maximum power

is the transmitted with square waveform modulation, i.e. lowest α_i or highest φ_i. In Fig. 4.27 two power levels transferred simultaneously to two different loads are presented.



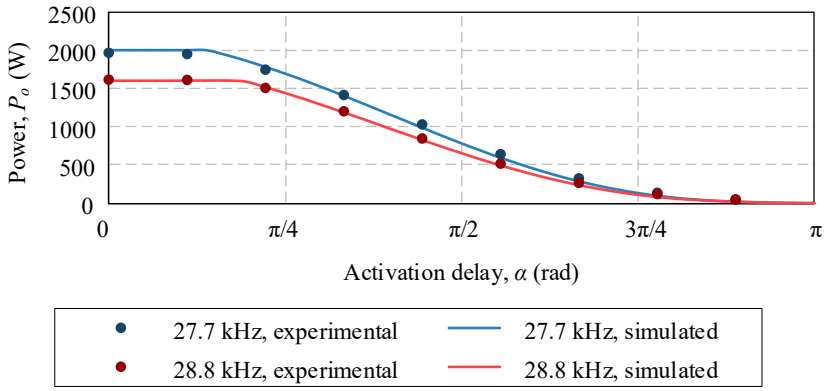
(a)



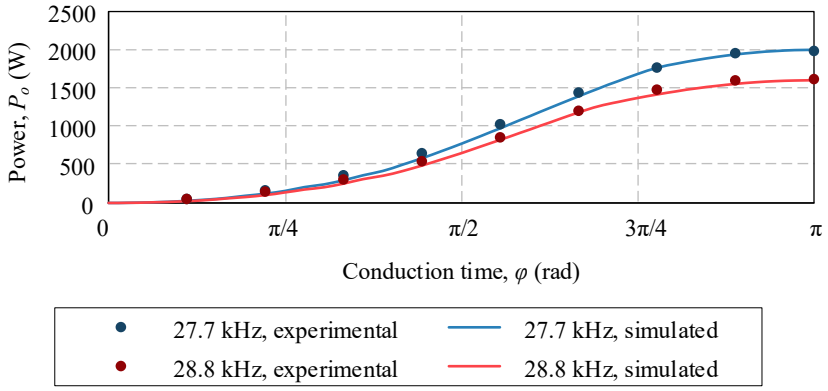
(b)

Fig. 4.27. Waveforms for two IH loads powered simultaneously with different modulation strategies and power levels. Square waveform, 2000 W, and NC-PDC strategy, 1600 W, (a). Square waveform, 2000 W, and NC-PWM strategy, 1600 W, (b). On each capture, from top to bottom: Load 1 output voltage, $v_{o,1}$, (250 V/div, dark blue), Load 1 inductor current, $i_{l,1}$, (50 A/div, cyan), Load 2 output voltage, $v_{o,2}$, (250 V/div, pink), Load 2 inductor current, $i_{l,2}$, (50 A/div, green). Time axis: 10 µs/div.

The experimental results validate both the expected waveforms and the simulated transmitted power. In Fig. 4.18, the results for both strategies are presented for two different switching frequencies. NC-PDC modulation presents a reduction of the resolution for higher frequencies as the load present a more inductive behavior and therefore the low-side diode conduction time is longer.



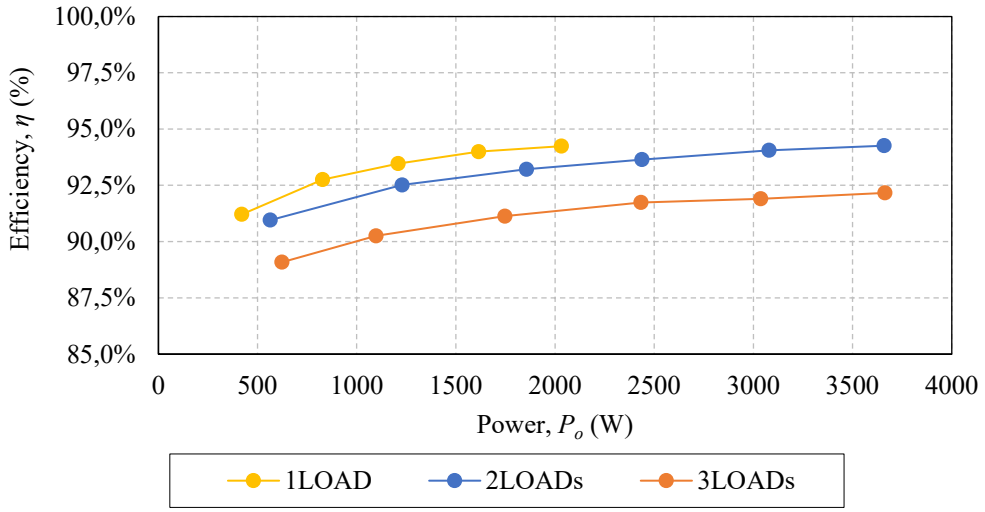
(a)



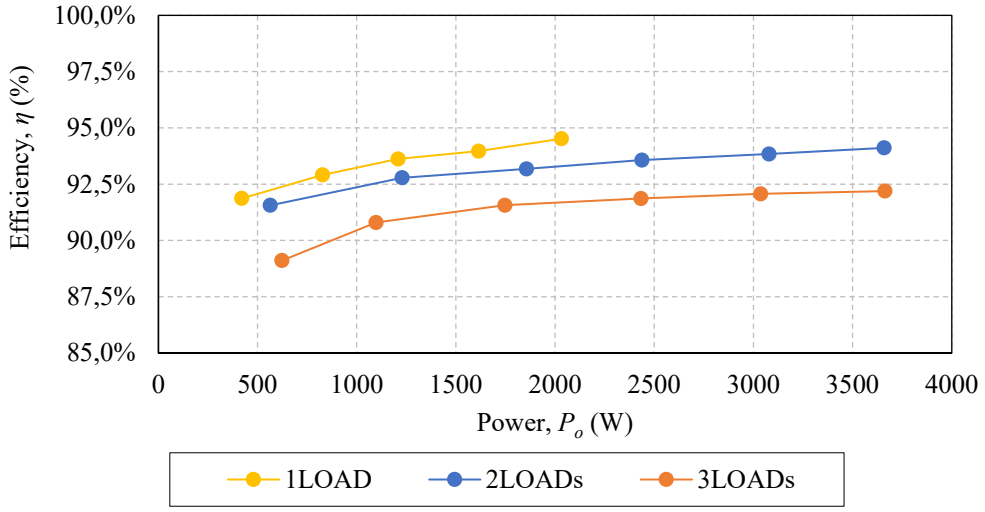
(b)

Fig. 4.28. Power output control achieved by NC-PDC strategy (a) and NC-PWM strategy.

Provided proper power transmission and control versatility is verified, the overall converter efficiency when operating with a different number of loads under the proposed NC modulation strategies is evaluated. In Fig. 4.29, the results for up to 3 loads can be seen. The total efficiency is over 89% when operating with 3 active IH loads and over 91% with 2, and it is similar for both modulation strategies. In this case, the reduction of efficiency with a higher number of loads is a consequence of the higher turn-on current associated with the displacement of the transistor activation relatively to the zero crossing.



(a)

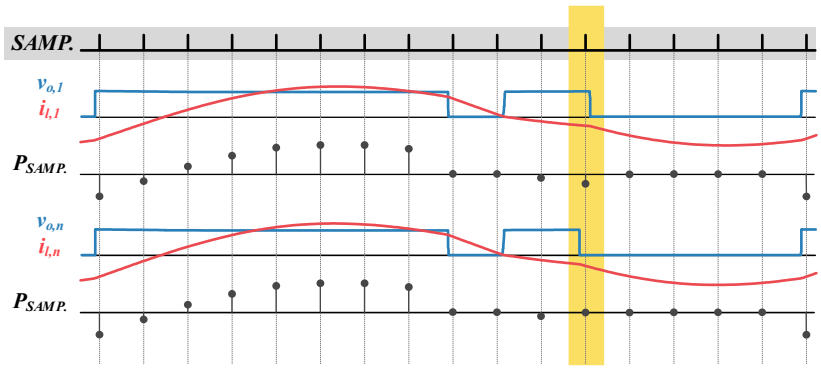


(b)

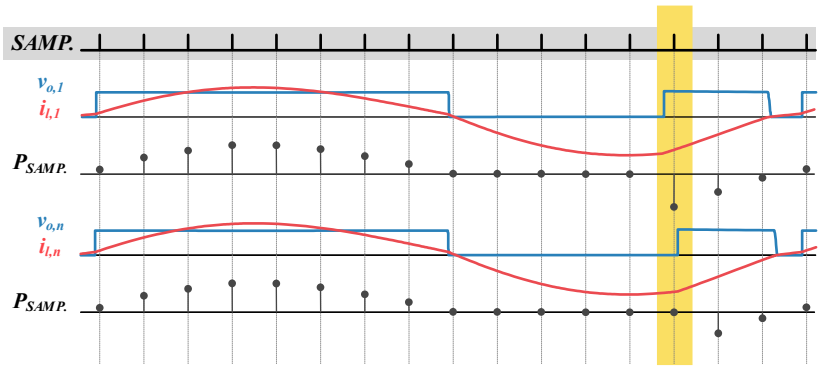
Fig. 4.29. Efficiency curves for different IH load count and with a base frequency of 27.7 kHz, i.e. maximum rated frequency of 2000 W for the NC-PDC strategy (a) and the NC-PWM strategy (b).

4.2.2.3. Closed loop evaluation

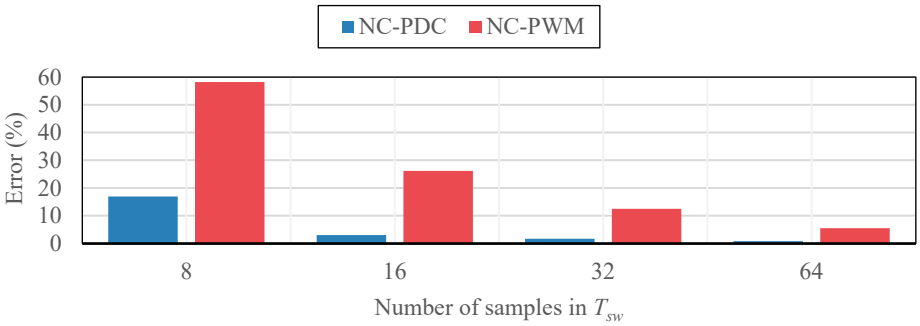
Based on the previous modulation strategies implemented with open loop operation, closed loop control can be achieved. The less complex implementation is the done by means of a power tracking PI controller. This controller, as presented in 3.4.2, allows power tracking and, additionally, enables PFC improvement. However, it presents limitations in the power calculation precision regarding the fluctuation of the sampling points along the switching cycle (Fig. 4.30). Therefore, only NC-PDC is considered for closed loop implementation with this prototype.



(a)



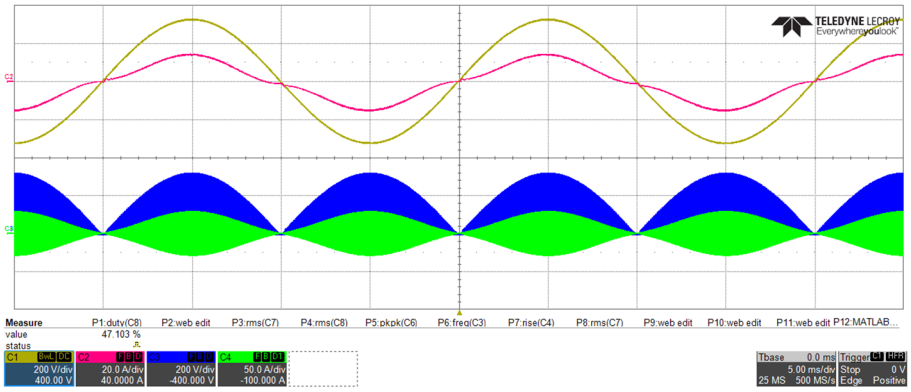
(b)



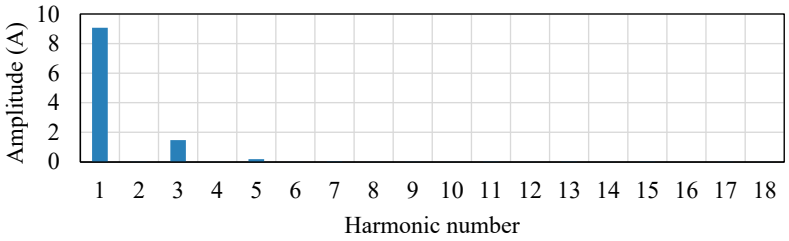
(c)

Fig. 4.30. Power calculation error examples when using the NC-PDC strategy (a) and the NC-PWM strategy (b) and relative error depending on the number of samples on a switching cycle.

When considering highly non-linear pots, as the presented in Fig. 4.31, the 3rd harmonic content of the mains current is close to the limits of the regulations as a consequence of $R_{eq,i}$ and $L_{eq,i}$ variation with the magnetic field intensity. Additionally, due to the uneven bus capacitor charge and discharge, high asymmetry and zero crossing distortion appear. In order to solve the problem, offline calculated frequency sweep profiles are commercially implemented. However, it is possible to reduce the severity of the problem with the proposed PI controller.



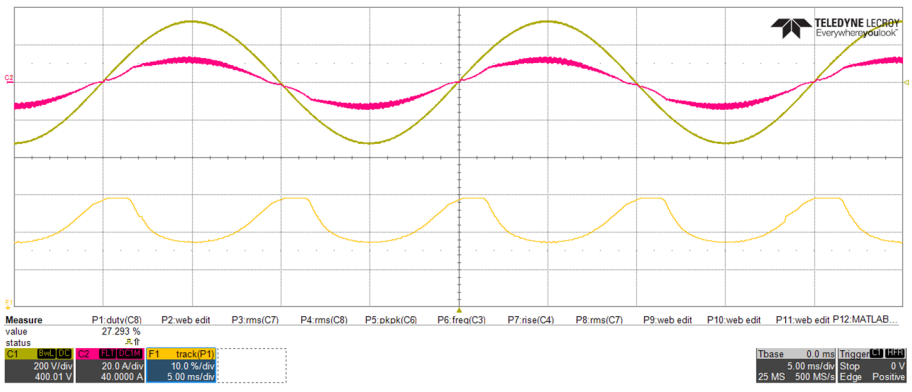
(a)



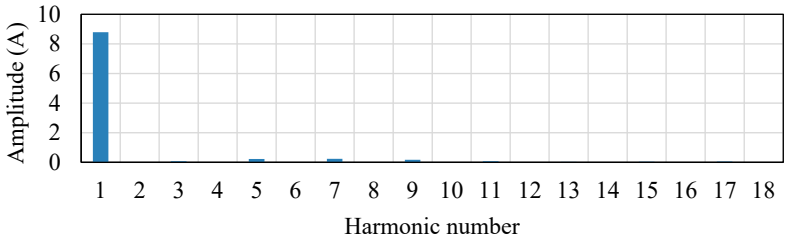
(b)

Fig. 4.31. Experimental results of the cooktop operating at nominal power, i.e. 2000 W, with a highly non-linear pot and without PFC modulation. Main waveforms (a) and harmonic contribution (b). On the oscilloscope capture, from top to bottom: mains voltage, v_{ac}, (200 V/div, yellow), mains current, i_{ac}, (20 A/div, pink), active loads output voltage, v_o, (200 V/div, blue), active loads current, i_l, (50 A/div, green). Time axis: 5 ms/div.

In contrast with the previous results, the usage of the proposed NC-PDC modulation strategy can be seen in Fig. 4.32. There, voltage and current are represented as well as the control parameter fluctuation along the mains cycle. The α variation profile reduces i_{ac} in the vicinity of the mains peak and due to its asymmetry is capable of compensating the mismatch between the bus voltage and the rectified mains voltage. By doing this, a reduction of the 3rd harmonic can be seen.



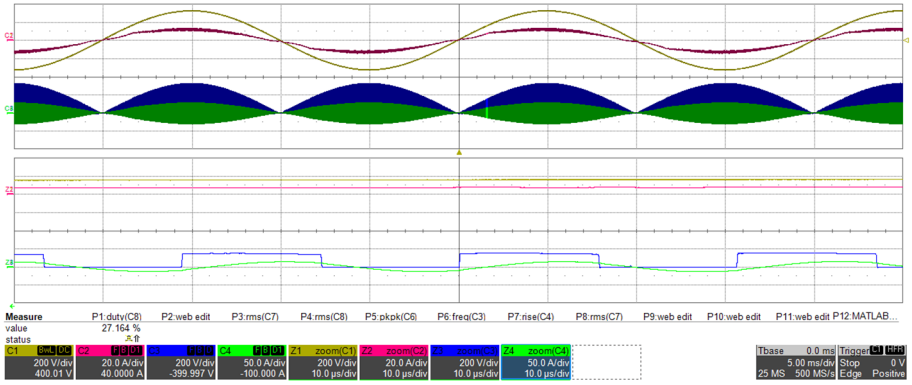
(a)



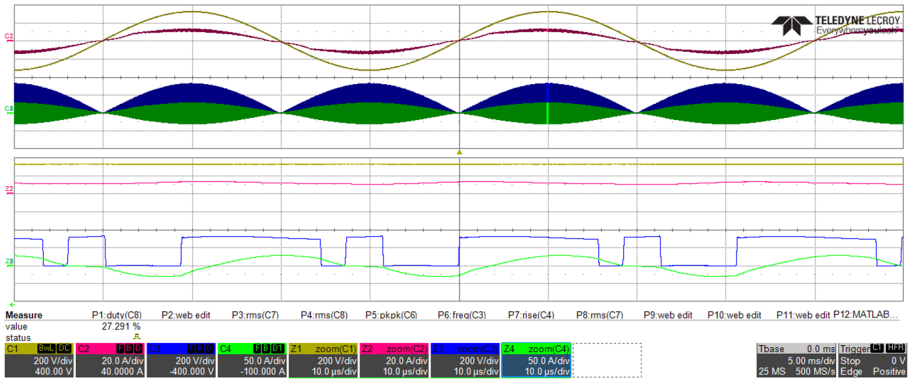
(b)

Fig. 4.32. Experimental results of the cooktop operating at nominal power, i.e. 2000 W, with NC-PDC PFC modulation and a highly non-linear pot. Main waveforms (a) and harmonic contribution (b). In (a), from top to bottom: mains voltage, v_{ac}, (200 V/div, yellow), mains current, i_{ac}, (20 A/div, pink), low side transistor active time percentage, *50%-α*, (10 %/div, dark yellow). Time axis: 5 ms/div.

The NC-PDC parameter fluctuation effect over the load waveforms can be seen in Fig. 4.33, where SW operation occurs near the zero crossing when α_i is lower than $D_{H,i}$ conduction time and high non-complementarity occurs near the mains peak.



(a)



(b)

Fig. 4.33. Detailed waveforms of the cooktop operating at nominal power with NC-PDC PFC modulation and a highly non-linear pot. Zoom near the zero crossing (a) and the mains peak (b). On each capture, from top to bottom: mains voltage, v_{ac}, (200 V/div, yellow), mains current, i_{ac}, (20 A/div, pink), active loads output voltage, v_o, (200 V/div, blue), active loads current, i_l, (50 A/div, green). Time axis: 5 ms/div, 10us/div.

Finally, the numerical results for the PI controller implementation with the non-linear material can be seen on TABLE 4.1, where the 3rd harmonic reduction and the improvement of the PF can be seen. Additionally, this table includes the results for 3000 W, which is closer to the maximum rated power and therefore presents a lower margin in the input current, showing the improvement on both THD and PF.

TABLE 4.1. PF, THD, AND HARMONIC CONTENT WITH AND WITHOUT THE PROPOSED MODULATION FOR A HIGHLY NON-LINEAR MATERIAL

	2000 W No-PFC Modulation	2000 W NC-PDC PFC modulation	3000 W NC-PDC PFC modulation
PF	0.984	0.992	0.991
THD (%)	16.18	4.58	10.83
Harmonic content	Normalized value (%)	Normalized value (%)	Normalized value (%)
Fundamental	100	100	100
2	0.16	0.16	0.17
3	16.21	0.89	8.60
4	0.04	0.10	0.04
5	2.05	2.59	6.27
6	0.01	0.07	0.03
7	0.36	2.73	1.91
8	0.02	0.07	0.03
9	0.16	1.96	0.81
10	0.02	0.22	0.02

To validate the operation of the controller for the complete range of pot materials, results have been also obtained for a slightly non-linear material. The results shown on TABLE 4.2 present improvement in THD and PF.

TABLE 4.2. PF, THD, AND HARMONIC CONTENT WITH AND WITHOUT THE PROPOSED MODULATION FOR A SLIGHTLY NON-LINEAR MATERIAL

	2000 W NO-PFC MODULATION	2000 W NC-PDC PFC MODULATION	3000 W NC-PDC PFC MODULATION
PF	0.995	0.994	0.997
THD (%)	6.77	2.28	3.30
Harmonic content	Normalized value (%)	Normalized value (%)	Normalized value (%)
Fundamental	100	100	100
2	0.15	0.14	0.10
3	6.67	0.62	2.13
4	0.02	0.12	0.02
5	0.78	1.31	1.81
6	0.02	0.12	0.05
7	0.12	1.16	1.35
8	0.02	0.03	0.01
9	0.14	0.70	0.73
10	0.01	0.05	0.01

4.2.2.4. Advanced MPC closed loop implementation

Additionally, considering the medium number of outputs and the high number of associated parameters, a MPC technique was proposed in Section 3.5. In order to implement it on the proposed converter, additional capacitor voltage measurements have to be implemented. Also, a DNN has to be embedded on the FPGA.

Fig. 4.34 presents the flags related to the different calculation steps. The upper two are the transistor gate signals, the subsequent two are related to the data acquisition, i.e. measure synchronization and available ADC data, and the last one corresponds with the DNN solution end of calculation. As it can be seen, the ADC sample is synchronized with S_L turn off and ADC data transmission and DNN evaluation occur, as expected, during S_H on time so the results can be applied in the same switching cycle.

Fig. 4.35 shows the main waveforms in a power stepdown change and a power stepup change starting in equal power transmission. These waveforms show that ZVS is achieved in S_H turn on and in $S_{L,i}$ turn on when possible, i.e. when both load transmitted power is equal and at least for one branch when the desired power is different. Additionally, both captures include the power measurements corresponding to differently spaced switching cycles, where the power setpoint change can be appreciated.

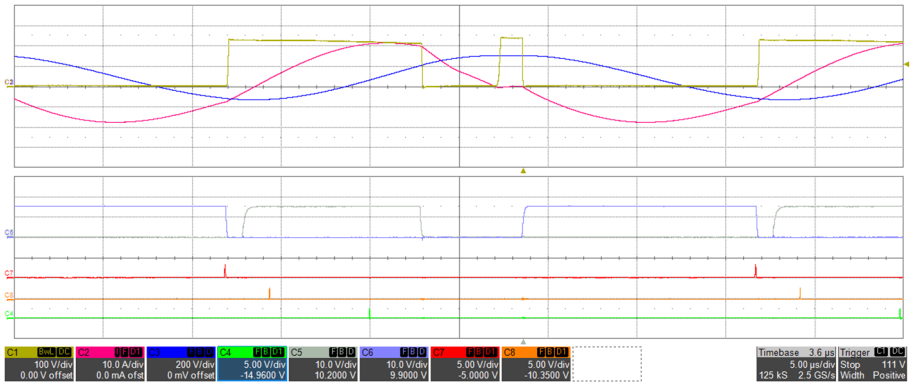
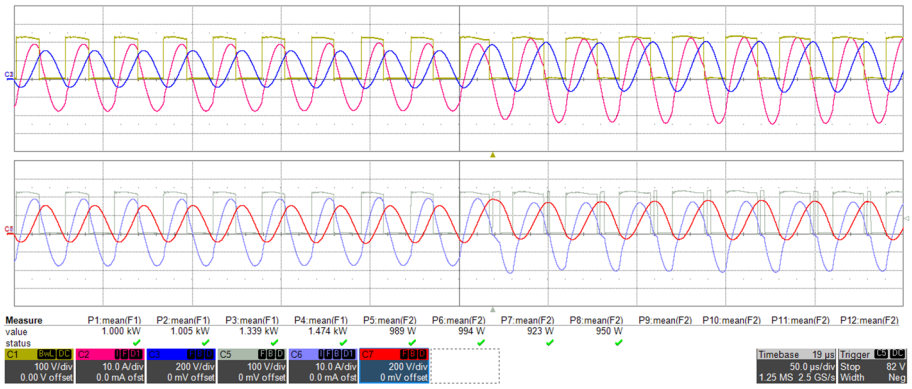
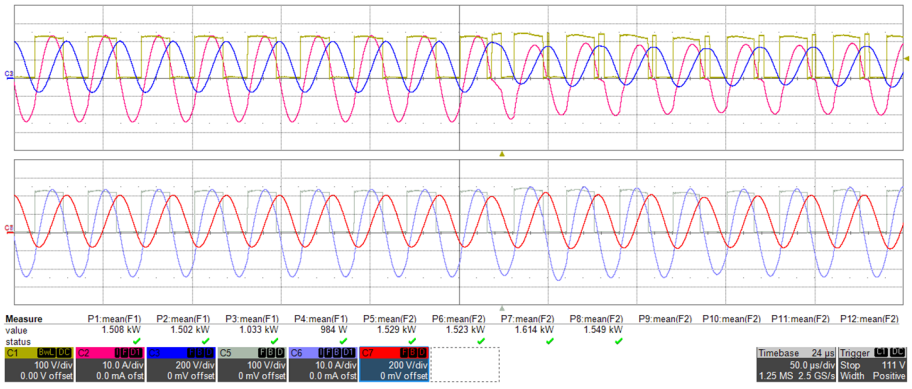


Fig. 4.34. Ready signal of the different implementation blocks. From top to bottom: IH load 1 $v_{o,1}$ (100 V/div, yellow), $i_{l,1}$ (10 A/div, pink), and $v_{c,1}$ (200 V/div, dark blue), S_H gate signal, G_{SH} (10 V/div, grey), $S_{L,1}$ gate signal, $G_{SL,1}$ (10 V/div, light blue), ADC capture signal, ADC_{CS} (5 V/div, red), ADC new data signal, ADC_{ND} (5 V/div, orange), and DNN new result signal, DNN_{RDY} (5 V/div, green). Time axis: 5 µs/div.



(a)



(b)

Fig. 4.35. Setpoint change to a higher (a) and lower (b) desired power. On each oscilloscope capture, from top to bottom: IH load 1 $v_{o,1}$ (100 V/div, yellow), $i_{l,1}$ (10 A/div, pink), and $v_{c,1}$ (200 V/div, dark blue), and IH load 2 $v_{o,1}$ (100 V/div, grey), $i_{l,1}$ (10 A/div, light blue), and $v_{c,1}$ (200 V/div, red). Time axis: 50 µs/div. Measures P1 to P4 represent the temporal evolution of the transmitted power to IH load 1, $P_{o,1}$, and P5 to P8 represent the temporal evolution of the transmitted power to IH load 2, $P_{o,2}$.

When compared with the simulation results, the main differences arise on the transmitted power error increase, which is a consequence of the mismatch between the

real induction load and the simulation model. For example, while equivalent parameters $R_{eq,i}$ and $L_{eq,i}$ are considered constant for simulation, they present a high dependency on the pot temperature.

4.2.3. 4-output Gan HEMT prototype

Switching losses represent a non-negligible percentage of the total converter losses. Based on that, wide bandgap devices are considered as a proper implementation that minimizes the switching losses of the converter by decreasing switching times, enabling a high power density implementation.

4.2.3.1. Implementation

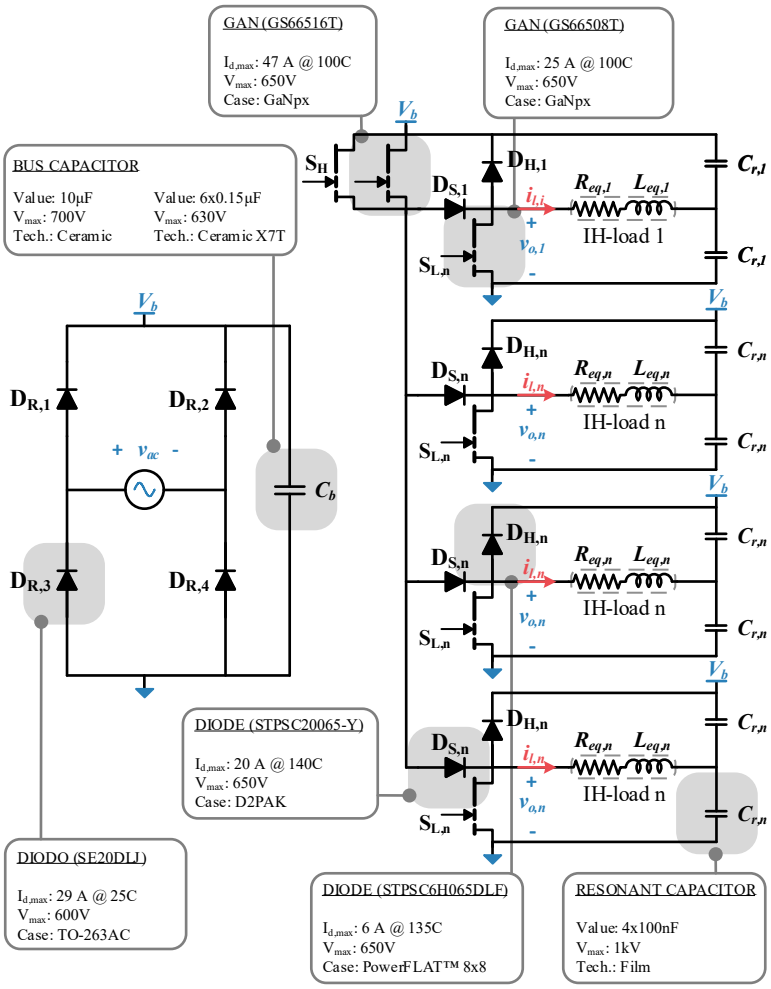
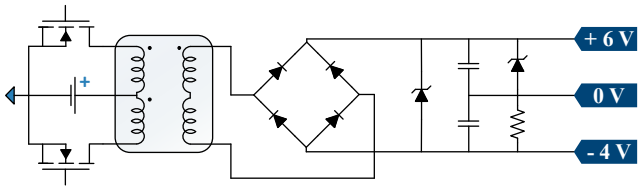


Fig. 4.36. Topology of the converter including the commercial devices used: diode bridge rectifier, bus capacitor, 4-output ZVS resonant matrix inverter and resonant capacitors.

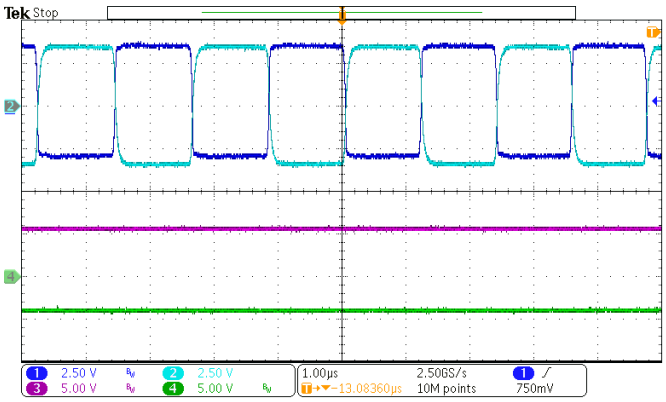
The proposed prototype technology presents GaN as the transistor technology and SiC for the high-frequency diodes, i.e. $D_{S,i}$ and $D_{H,i}$. Given the maximum current ratings of the high side transistor, the number of outputs is selected to be 4 to minimize the

parallelization influence. Additionally, as it can be seen on the complete inverter schematic of Fig. 4.36, the high side transistor present parallelized devices in order to make a more robust implementation, however, as in the previous case, the transistor is selected to withstand the current requirements alone.

Due to low threshold voltage of the selected GaN HEMTs, the driving circuit is selected to provide +6 V on voltage and -4 V off voltage to improve noise immunity. Both high-side and low side driving circuits use a power source based on a push-pull structure with the SN6505A IC and a full bridge voltage multiplier at the output. The isolated driver used for both transistors is the UCC5350.



(a)



(b)

Fig. 4.37. Push-pull isolated voltage source (a) and push-pull operation waveforms (b). On the oscilloscope capture, from top to bottom: high side coil voltage drop (2.5 V/div, dark blue), low side coil voltage drop (2.5 V/div, light blue), output positive voltage rail (5 V/div, pink), output negative voltage rail (5 V/div, green). Time axis: 1 µs/div.

The measurement circuitry is equivalent to the one of the previous prototype. It includes applied voltage and current through the load measurements.

The prototype construction aims for a single PCB with high power density in order to allow the implementation on a commercial cooktop. Therefore, heat dissipation becomes a key challenge. Given the different devices and the associated power losses, several implementations have been used [86]. GaN transistors present the possibility of being top cooled and therefore can be placed on the bottom of the PCB, directly over the heatsink.

The rectifier and series diodes, which present higher conduction losses, are cooled via metal inlay, which provides a low thermal resistance conductive path to the heatsink. Last, the high side diode, as present lower losses, is cooled through thermal vias (Fig. 4.38 (b)).

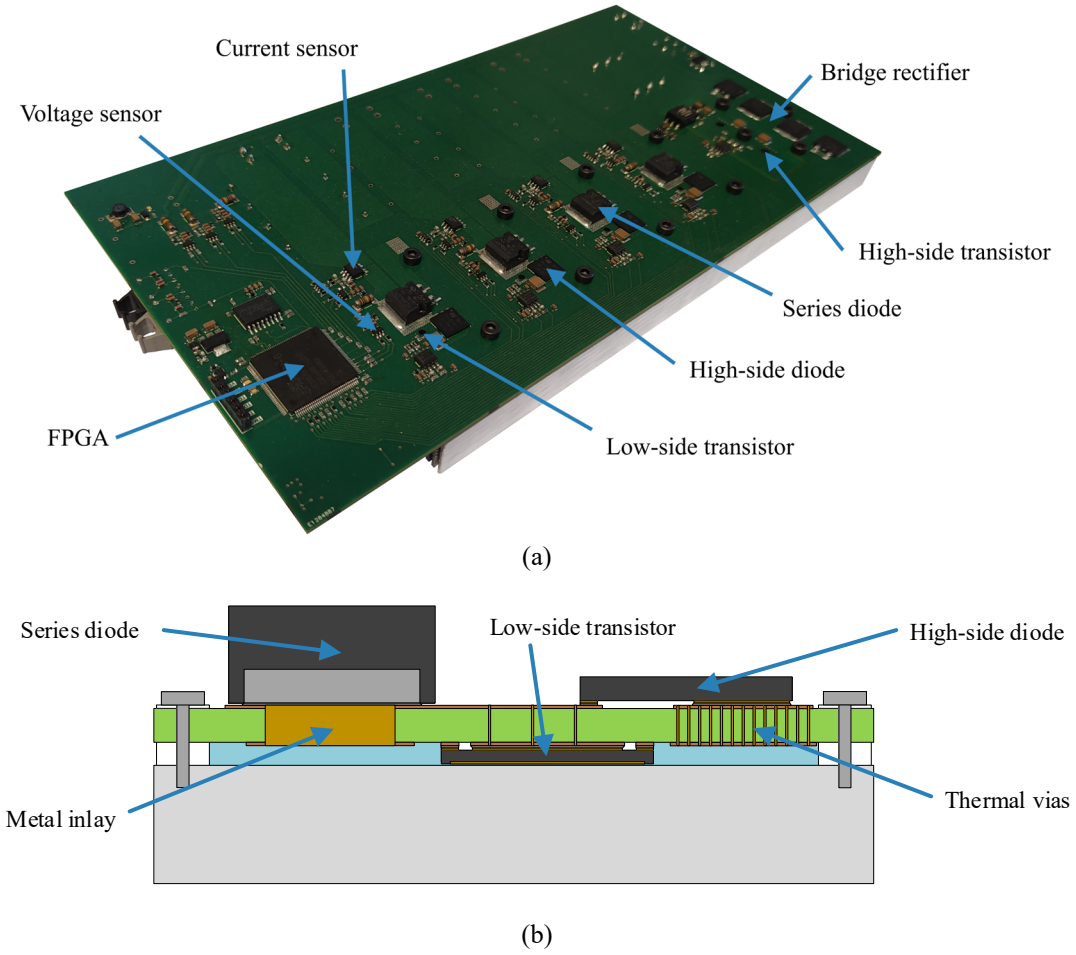


Fig. 4.38. Complete experimental prototype (a) and prototype cooling structure (b).

4.2.3.2. Open loop evaluation

In this case, the FPGA that includes the PWM modulator, IH load power and current measurement, mains zero crossing detection, and communication with the PC blocks is directly integrated on the PCB in order to minimize the required area. The PWM modulator is defined so that it can generate non-complementary modulations.

Therefore, in order to evaluate the converter operation, NC-PDC strategy has been selected as it has been proved as the most promising. In Fig. 4.39 the proper behavior of the converter can be seen.

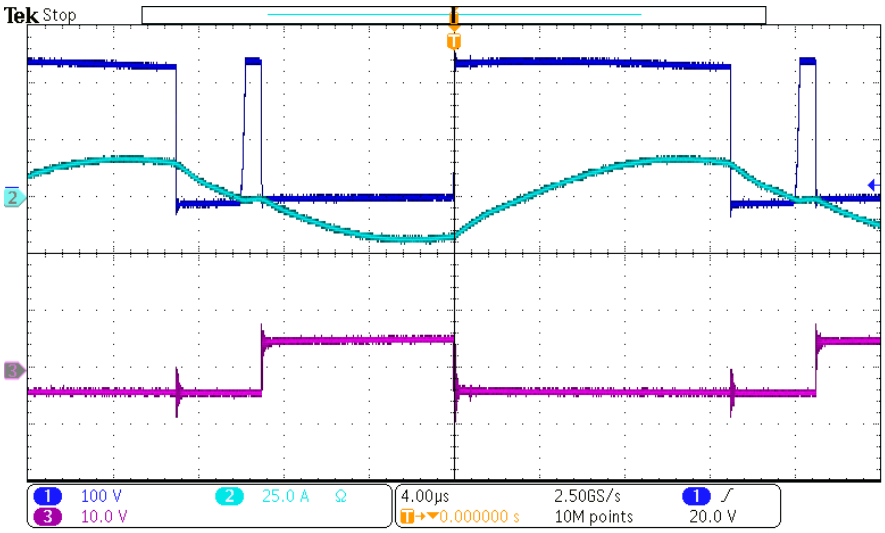


Fig. 4.39. Waveforms of a load at 1000 W using NC-PDC strategy. From top to bottom: IH load 1 applied voltage, $v_{o,1}$, (100 V/div, dark blue), IH load 1 inductor current, i_1, (25 A/div, cyan), SL gate voltage, $v_{GS,SL,1}$, (10 V/div, pink). Time axis: 4 µs/div.

Additionally, as the main advantage of the WBG implementation is the fast switching, close up captures of the transitions are presented in Fig. 4.40 to Fig. 4.42. There, fast switching can be seen irrespective of the device that drives the commutation. Fig. 4.40 presents the hard-switching low-side transistor turn on which is consequence of the NC-PDC modulation strategy. It depends on the transistor rise time and $D_{H,i}$ reverse recovery which, due to the SiC technology selection, is reduced.

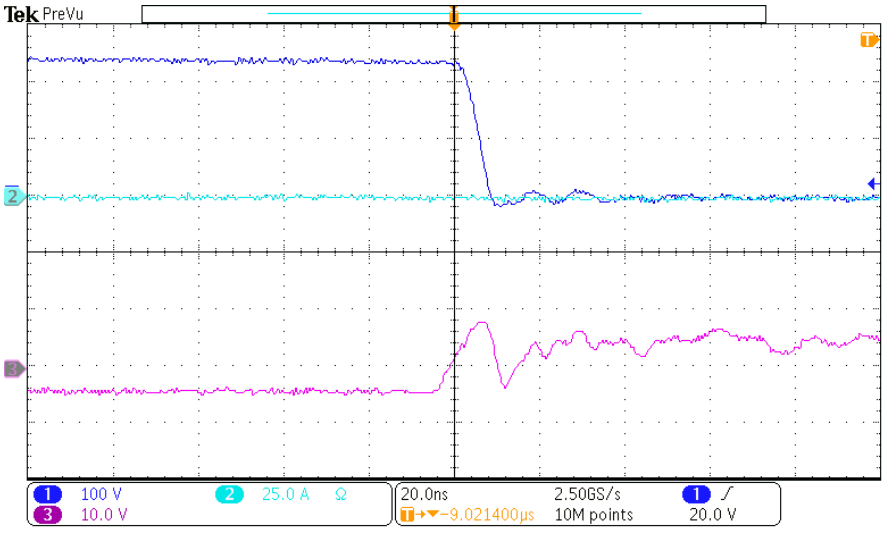
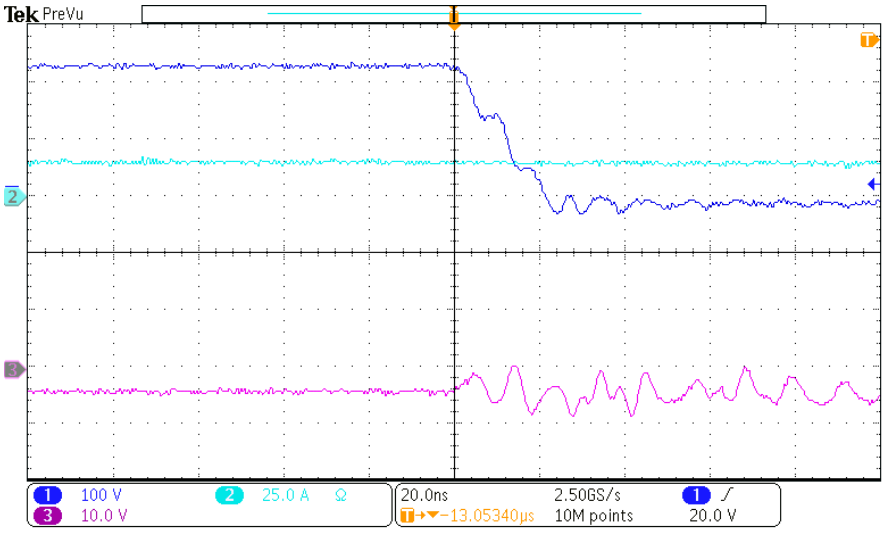
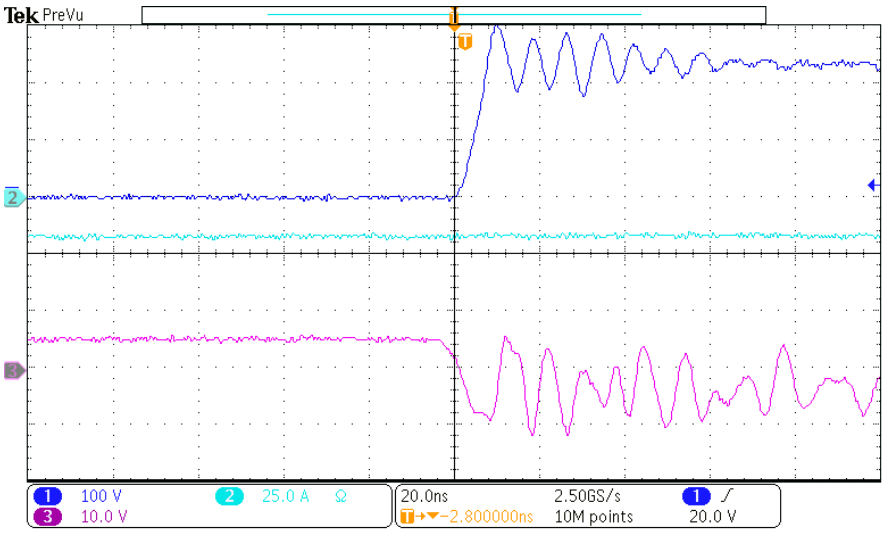


Fig. 4.40. Close-up capture of the waveforms of the low-side transistor turn on with a load at 1000 W using NC-PDC strategy. From top to bottom: IH load 1 applied voltage, $v_{o,1}$, (100 V/div, dark blue), IH load 1 inductor current, i_1, (25 A/div, cyan), SL gate voltage, $v_{GS,SL,1}$, (10 V/div, pink). Time axis: 20n µs/div.

Fig. 4.41 (a) shows the high-side transistor turn off and therefore the voltage drop depend on both the GaN HEMTS, the high-side one through fall time and the low side one through reverse conduction dynamics. Fig. 4.41 (b) presents low side transistor turn-off sequence.



(a)



(b)

Fig. 4.41. Close-up captures of the waveforms of the high-side (a) and low-side (b) transistors turn off with a load at 1000 W using NC-PDC strategy. From top to bottom: IH load 1 applied voltage, $v_{o,1}$, (100 V/div, dark blue), IH load 1 inductor current, i_1, (25 A/div, cyan), SL gate voltage, $v_{GS,SL,1}$, (10 V/div, pink). Time axis: 20n µs/div.

Last, Fig. 4.42 shows the freewheeling diode, i.e. $D_{H,i}$, conduction due to the change in the current sign.

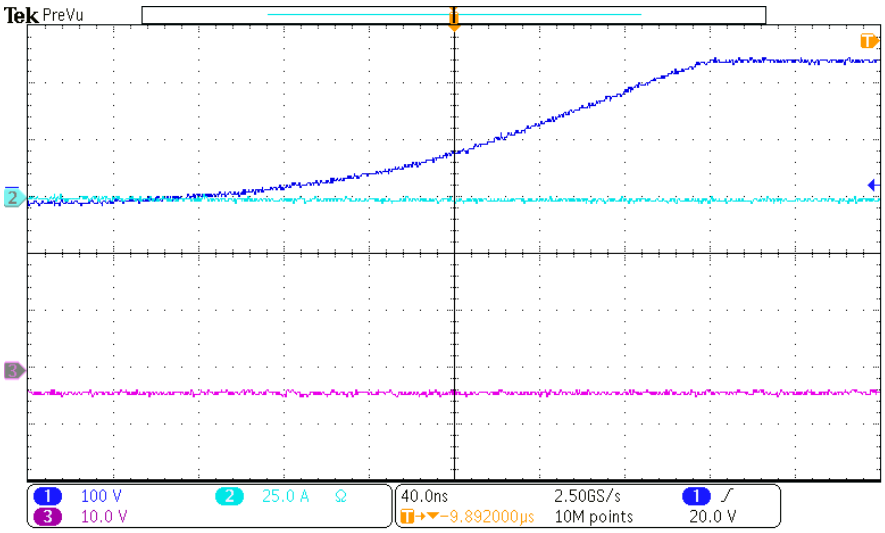


Fig. 4.42. Close-up capture of the waveforms of the high side diode, $D_{H,i}$, activation with a load at 1000 W using NC-PDC strategy. From top to bottom: IH load 1 applied voltage, $v_{o,1}$, (100 V/div, dark blue), IH load 1 inductor current, i_1, (25 A/div, cyan), SL gate voltage, $v_{GS,SL,1}$, (10 V/div, pink). Time axis: 20n µs/div.

4.2.4. Comparative analysis

As it has been shown, each of the prototypes is optimized for certain operating conditions, such as the coil size and distribution and the modulation strategy to be evaluated. Due to this procedure, good results in terms of performance are achieved. However, given that all the prototypes are intended for a similar application and based on the same topology, certain comparisons can be performed. In order to do so, power losses comparison is carried out, and a comparative of the EMC conduced emissions based on the *dv/dt* is also presented.

4.2.4.1. Efficiency and power loss distribution

Efficiency of the converter is key in the proper design of an induction cooktop as it is expected to operate in small spaces with high ambient temperatures. Therefore, proper device losses calculations are necessary in order to design the required thermal management, being especially relevant for this case due to the complete solid-state implementation of the inverter.

Efficiency has been measured to validate certain prototypes under concrete operation modes. In order to enhance the comparison, power losses evaluation can be performed from the parameters provided by the manufacturers in the data sheets [136].

- Transistor losses

The transistor losses, P_S, are calculated as the sum of conduction losses, $P_{S,on}$, and switching losses, $P_{S,sw}$.

$$P_S = P_{S,on} + P_{S,sw} \tag{3.50}$$

Conduction losses are the consequence of the non-zero on-state voltage drop. Assuming that the device technology datasheet allows to approximate this voltage by a collector-emitter voltage drop, $v_{CE,on}$, and the channel resistance, $r_{CE,on}$, it can be calculated as a function of the transistor current, i_C, as

$$P_{S,on} = v_{CE,on} I_C + r_{CE,on} I_{C,RMS}^{\ 2}, \tag{3.51}$$

where I_C and $I_{C,RMS}$ are the transistor average and rms currents respectively.

Switching losses are calculated based on the datasheet curves

$$P_{S,sw} = \left(E_{on}\left(i_{C|on}\right) + E_{off}\left(i_{C|off}\right)\right) f_{sw}, \tag{3.52}$$

where E_{on} and E_{off} the turn-on and turn-off energy losses provided by the manufacturer as a function of $i_{C|on}$ and $i_{C|off}$, which are the collector current in the turn-on and turn-off transition respectively.

Note that the current in the column, i.e. the high-side transistor, will be the sum of the current through the active loads.

- Diode losses

Symmetrically with the transistor losses, diode losses can be calculated as the sum of conduction losses, $P_{D,on}$, and switching losses, $P_{D,sw}$, that correspond with the diode turn-off losses.

$$P_D = P_{D,on} + P_{D,off} \tag{3.53}$$

Conduction losses are a function of the anode-cathode voltage drop, $v_{AK,on}$, channel resistance, $r_{AK,on}$, and diode current, i_D, it can be calculated as

$$P_{T,on} = v_{AK,on} I_D + r_{AK,on} I_{D,RMS}^{\ 2}, \tag{3.54}$$

Being in this case I_D and $I_{D,RMS}$ are diode average and rms currents respectively.

Switching losses correspond with the turn off of the diode and therefore are a function of the reverse recovery capacitance

$$P_{D,sw} = \frac{V_b Q_{rr}}{2} f_{sw}, \tag{3.55}$$

where Q_{rr} is the reverse recovery charge of the diode and V_b the bus voltage. It is important to note that the series diodes $D_{s,i}$ are completely driven by the transistors and therefore the current is extinguished by them, leading to depreciable reverse recovery power losses.

- Comparative setup and results

As the prototypes are focused on different inductor distributions, in order to achieve a common reference, a 21 cm pot size placed with a homogeneous coil distribution is selected, as shown in Fig. 4.43.

(a) (b)

Fig. 4.43. Pot estimated placement to achieve comparable results between the different inverter prototypes.

Additionally, to achieve comparable results, SW and NC strategies are used. PDM is not considered due to the pulsating power dependencies on the number of inductors and power rating, linking it to external factors such as the flicker regulations.

In Fig. 4.44, nominal power transmitted to a single pot, 2000 W, is considered. The switching frequency for SW is the one that provides the desired power and a slightly lower one is considered for NC modulation. This frequency is selected as the one that, with SW operation, provides the inductor rated power.

As it can be seen, SW present higher efficiencies for all cases, as ZVS turn-on is achieved. Besides, comparison between NC-PDC and NC-PWM show a high dependency on the implementation. For the case NC-PWM, due to the characteristics of the modulation, turn-off losses are reduced for S_H. However, the hard switching turn-on sequence, for S_H with NC-PWM strategy and $S_{L,i}$ with NC-PDM strategy, present additional losses that include the contribution of the opposite diode reverse recovery

current, and, in case of snubber capacitor presence, the energy stored on it. Therefore, the MOSFET and the IGBT with snubber capacitor implementations are the ones more penalized by the S_H turn-on losses. Moreover, even for the cases NC-PWM present higher efficiency, it is important to note that the considered power losses are produced and need to be dissipated in a single power device.

When focusing on the implementations instead of modulation strategies, it can be seen the big advantage in terms of switching losses of the MOSFET implementation even though it operates at higher frequencies. Additionally, in this prototype, the proper choice of low current rated $S_{L,i}$ allow to minimize its conduction losses. However, the use of equal diodes and the subsequent trade-of between switching and conduction characteristics lead to a suboptimal choice.

The same occurs for the case of the 5-output Si IGBT implementation, which is designed to include a snubber network, as it can be seen in the SW efficiency, but has also been evaluated without it. The proper snubber operation can be seen linked to the additional losses that it produces when hard switching turn-on appears.

The more optimized device selection of the 12-output Si IGBT implementation presents reduced power losses in all four devices. In comparison with implementations with reduced switching losses, this solution achieves comparable efficiency as the conduction losses are reduced.

The last implementation, based on WBG devices, achieves the lower efficiency penalty as the switching losses of both transistors and diodes are minimal, leading to almost no additional contribution even with NC strategies.

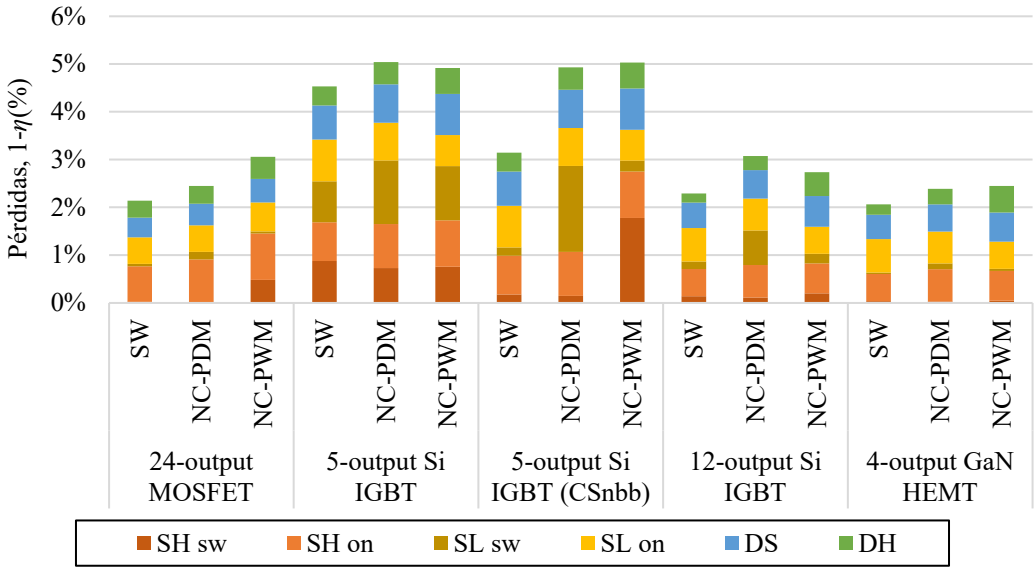


Fig. 4.44. Estimated power loss share, expressed as efficiency penalty, of the implemented inverters operating with the different modulation strategies. The switching frequency corresponds with the required one for SW operation and the calculated to provide the rated power with each coil for NC. The transmitted power is 2000 W to a single pot.

This evaluation can be completed by presenting the equivalent results for the cooktop maximum rated power transmission, in this case to two different pots in order to be able to apply NC modulation strategies. In Fig. 4.45 the results can be seen. The main differences are due to the lower transmitted power per coil, which leads to higher switching frequencies in the case of SW and higher turn-on currents in the case of NC strategies.

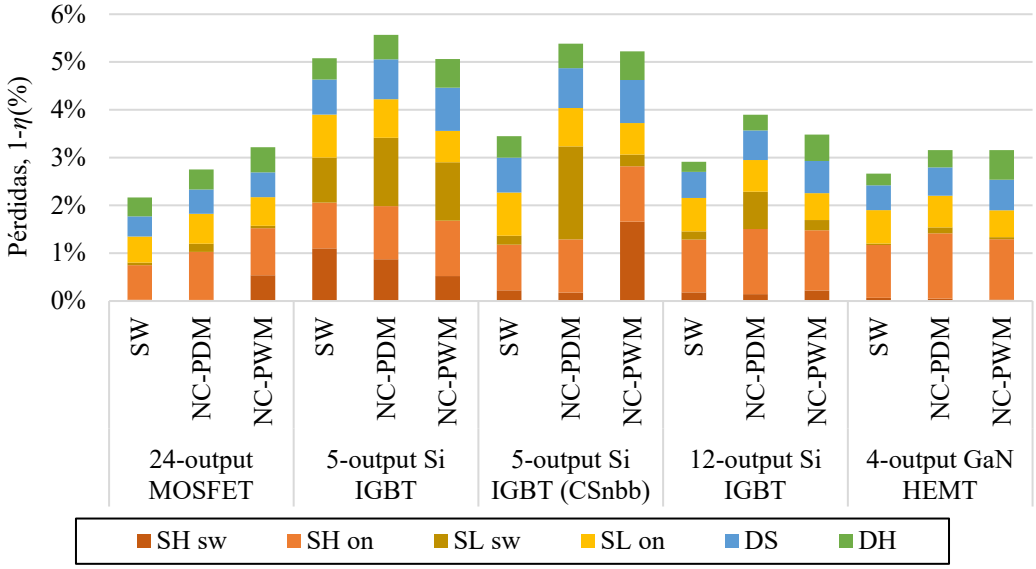
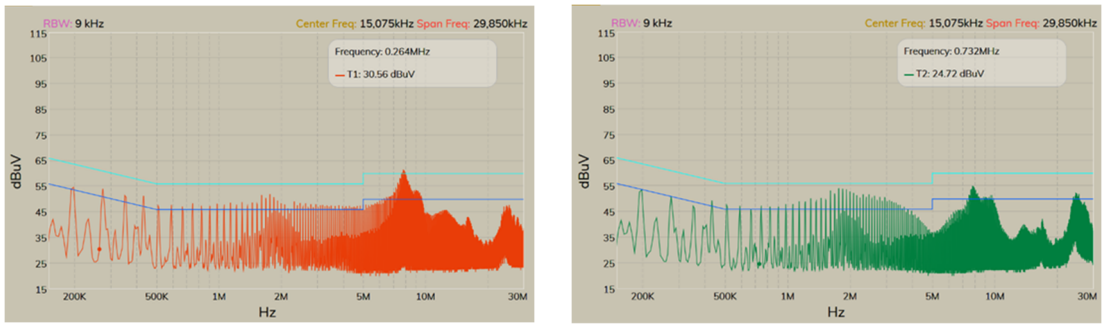


Fig. 4.45. Estimated power loss share, expressed as efficiency penalty, of the implemented inverters operating with the different modulation strategies. The switching frequency corresponds with the required one for SW operation and the calculated to provide the rated power with each coil for NC. The transmitted power is 3600 W to two pots simultaneously.

4.2.4.2. EMC results

In addition to the implication in the power losses, the different switching speeds and associated *dv/dt* achieved with the implemented technologies result in electromagnetic disturbances at different frequencies. A comparison of different snubber capacitors and thus different *dv/dt* has been evaluated for SW and NC-PDC modulation strategies.

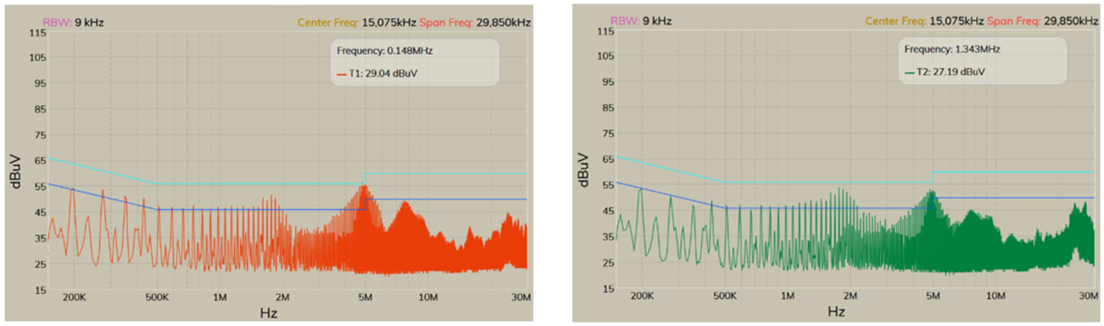
In Fig. 4.46 the conducted EMC measurements for 5.6 nF snubber capacitor can be seen. There, the peak around 8 MHz is consequence of the transistor switching.



(a) (b)

Fig. 4.46. Line (a) and neutral (b) conduced EMC perturbations for 1500 W power transmission and a 5.6 nF snubber operating with SW.

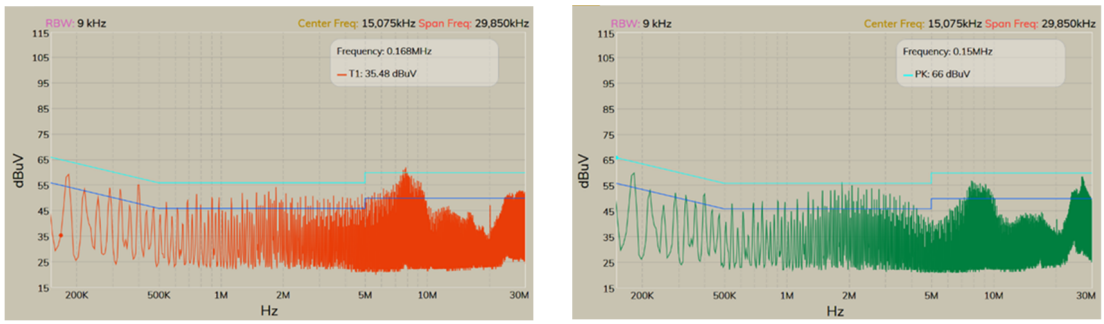
In order to offer a comparison, a 15 nF implementation has been evaluated and the results are presented in Fig. 4.47. There the peak has moved to 5 MHz, where a higher influence of the EMC filter helps to reduce the noise levels.



(a) (b)

Fig. 4.47. Line (a) and neutral (b) conduced EMC perturbations for 1500 W power transmission and a 15 nF snubber operating with SW.

Finally, the usage of NC-PDC strategy can be seen in Fig. 4.48. In this case the peak of 8 MHz is also present but, as a consequence of the non-amortiguated turn-on transition that depends only of the transistor characteristics and not of the diode, higher perturbation levels appear around 28 MHz.



(a) (b)

Fig. 4.48. Line (a) and neutral (b) conduced EMC perturbations for 1500 W power transmission and a 5.6 nF snubber operating with NC-PDC.

Chapter 5

Conclusions

This thesis evaluates a family of multi-output matrix-based inverter topologies developed for its application to induction heating. In order to do so, the literature has been comprehensively studied, the different topologies have been analyzed, several modulation strategies have been proposed and experimental prototypes have been built for its evaluation.

In this final chapter, the main conclusions of this dissertation are presented. Firstly, the most relevant conclusions and contributions of each chapter of this dissertation are summarized. Afterwards, the main academic results are highlighted. Finally, the future research lines motivated by this dissertation are briefly explained.

Contents

5. Conclusions

In the following chapter, the main conclusions of this dissertation and its scientific results are summarized according to the chapter division of the document. The main novel contributions of each chapter are highlighted at the end of the conclusion section, in TABLE 5.1. Finally, prospective future research possibilities, that arise as a continuation of this research, are discussed.

5.1. Conclusions

This dissertation focuses on the evaluation of a family of multi-output matrix-based topologies for flexible-surface domestic IH applications. To offer a complete overview of the problem and the alternatives to provide feasible solutions, the document has been structured after an additive fashion, serving each chapter as the baseline for the building of the next one.

5.1.1. Multi-output topologies

Chapter 1 has introduced induction heating, the applied technology, and the domestic applications for cooking towards the most avant-garde products. Using it as a starting point, the efforts towards powering the multi-coil structures of flexible-surface implementations are addressed.

The commercial implementation of flexible-surface cooktops requires up to 48 coils whose power rating is proportional to its size and can vary between 1800 W and 600 W. Therefore, the challenge of powering a large number of inductors in an efficient, versatile and cost-effective way, while complying with electromagnetic compatibility and providing a good user experience motivates the research of multi-output inverters. In order to provide new solutions, a state-of-the-art overview of the alternative multi-output inverter topologies is summarized in this chapter.

Several approaches have been followed to generate the required converters. Inverter parallelization, i.e. a single inverter per coil, achieves good controllability performance but requires a high number of power devices. Load multiplexation, on the contrary, aims for minimizing the number of inverters by adding an additional relay mesh which allow to select the connection between inverter and coil, presenting limited controllability due to the relays dynamics. Finally, a more heterogeneous group of multi-output converters include the solutions that present ad-hoc implementations aiming for reducing the number

of power devices, increasing the control flexibility, or boosting the inverter performance. Among this last group, the solutions that present low power device count, solid state components implementation and good controllability, achieving a good trade-off between performance and cost, are the most promising future domestic IH application.

5.1.2. Matrix-based multi-output resonant inverters

Even though several multi-output inverters have been proposed on the literature, they are usually focused on reducing the device count, leading to solutions whose performance usually fades when increasing the number of IH loads. Therefore, the possibility of designing topologies that maintain the control versatility while powering a high number of IH loads simultaneously with few power devices justifies the development of such systems. In Chapter 2, three matrix-based topologies, derived from the half-bridge topology, have been proposed and analyzed based on its behavior.

The multi-output ZCS matrix resonant inverter presents the lower possible device count for a number n of IH loads: $\sqrt{n}$ transistors and $2n$ diodes. Its operation is defined by each IH load and resonant tank parameters, and therefore the waveforms are independent of the modulation, provided that the switching frequency is under the resonant one. As a consequence, the current flowing time is fixed, and it is possible to operate with both transistor turn-on and turn-off sequences under ZCS conditions. Considering the fixed current flowing time, it is possible to control the transmitted power to each load by reducing the switching frequency, i.e. increasing the time between active periods, from the resonant one, which provides maximum power. This can present some restrictions, when considering domestic IH, as acoustic noise, and therefore operation under 20 kHz, is to be avoided. Additionally, one of the main disadvantages of the topology is that the transistor blocking voltage is also dependent on the load parameters, leading to increased values.

In order to solve this problem, the multi-output ZCS matrix resonant inverter incorporates clamp diodes, leading to an implementation that requires $\sqrt{n}$ transistors and $2n+\sqrt{n}$ diodes. These diodes operate as antiparallel diodes of the corresponding transistors, enabling current reverse flow and therefore soft-switching turn-on when operating over the resonant frequency. Additionally, ZCS turn-off operation is also possible when under the resonant frequency, leading to a behavior on each active load similar to the one of the resonant half bridge.

Both topologies provide good performance for single load operation and several cases of multi-load activation. However, the available combinations are limited by diagonal activation, i.e. the unwanted activation of loads that share high-side and low-side transistors with active loads. Therefore, same column or same row activations are preferred.

In order to ensure single row or single column activation, the proposal of unidimensional matrix structures arise. In particular, the following lines summarize the main reasons for implementing a unidimensional structure:

- It requires n+1 transistors and 2n diodes.
- Load activation, deactivation, and even power control depend only on the low side transistor modulation.
- The behavior of the converter as seen from the active IH loads is similar to the one of the HB
- Fixed path connection ease the load detection and equivalent parameter calculation based on the current waveform.
- Built in antiparallel diode allow to include capacitive snubber networks to minimize losses and *dv/dt* on the corresponding transistor.
- The column structure implementation reduces the driving requirements as the transistors are referenced to GND.

All these benefits motivate and justify the proposal of a single-column matrix-based ZVS resonant inverter. Moreover, the increased flexibility of the topology allows to implement both classical and more complex modulation strategies to provide the required power to the different IH loads.

5.1.3. Single-column matrix-based ZVS resonant inverter modulation strategies

Independent load power control can be achieved using several modulation strategies. Each one of these present different advantages and constraints. In Chapter 3, the proposed modulation strategies are divided in continuous, if power transfer to all the active loads occur every switching cycle, or discontinuous if otherwise.

The discontinuous approach is chosen as a SW-based mains-synchronized multiplexation strategy in order to fulfill most of the constraints. Additionally,

mathematical solution to minimize the input power fluctuation and closed loop considerations to achieve a proper implementation have been presented.

The continuous power control is achieved by means of non-complementary strategies. The analytical approach for achieving the non-complementarity by means of modulation of two different parameters has been presented. Moreover, closed loop considerations to benefit from the modulation versatility and achieve improved PFC are presented. Last, and based on NC-PDM strategy, an advanced controller using MPC has been proposed to obtain proper power tracking while achieving optimal efficiency.

5.1.4. Implementation and experimental results

In Chapter 4, the proposed topology has been implemented for different operation considerations. This includes the typology of the selected loads, the number of phases or the modulation strategy considered for power control.

In order to power 24 600-W induction coils corresponding with a single-phase implementation, a prototype using MOSFET has been developed. This prototype presents two independent inverters with 12 output each and capacitor-voltage-based power and load characterization measurements. The converter allows power control based on mains synchronized PDM and achieves an efficiency over 92%.

When the topology is transferred to power between 4 and 6 coils of 1800 W rated power three different prototypes have been built.

A first approach based on the benchmarking process of commercial cooktops and thus using market-ready technologies is designed. The topology uses IGBT devices which are selected equal due to the low imbalance between the total power of 3600 W and the coil rated power. Closely related with the technology selection, the modulation strategy is chosen. In order to benefit from the possibility of implementing snubber capacitors in the low-side transistors, increasing the efficiency, a SW-based mains synchronized multiplexation strategy is selected. The strategy is validated to achieve independent power control with low input power ripple, by considering each IH coil as an independent load, allowing a reduced PDM period, and thus low temperature ripple in the pot.

In order to increase control versatility, a two phase 6-output-per-phase prototype has been proposed. It is designed using IGBT technology and the power devices are selected to achieve reduced power losses while operating without snubber capacitors. This design has enabled the usage of non-complementary modulation strategies for a precise power

transfer to the different loads, achieving efficiencies over 89%. Additionally, and based on NC-PDC strategy, closed loop controllers have been implemented. PFC controller achieves a PF increase of up to 0.07 points and a THD reduction of up to the 80% by addressing the 3rd harmonic component excess. Additionally, advanced MPC controller achieves fast response and optimal control in terms of efficiency

Last, based on the contribution of the switching losses to the overall losses of the converter, a 4-output prototype based on GaN transistors and SiC diodes has been proposed, showing proper operation and short switching times and therefore reduced power losses.

TABLE 5.1 below summarizes the main novel contribution of this dissertation.

TABLE 5.1. SUMMARY OF THE MAIN NOVEL CONTRIBUTIONS

CHAPTER	CONTRIBUTIONS
1	• Study of the state of the art of multi-output topologies for flexible surfaces in domestic IH.
2	• Multi-output matrix ZVS inverter. • Single-column matrix-based multi-output ZVS inverter. • Study of the main advantages of multi-output matrix-based inverters for flexible-surfaces in domestic IH applications. • Analysis configuration, waveforms, and modulation degrees of freedom of the proposed inverters.
3	• Multi-load independent power control modulation strategy based on low-pulsating-power load multiplexation for single-column matrix-based multi-output ZVS inverter. • Closed-loop controller considerations for implementing the low-pulsating-power load multiplexation. • Multi-load independent power control modulation strategies based on non-complementary transistor activation for single-column matrix-based multi-output ZVS inverter. • Considerations for implementing a PFC closed-loop controller using non-complementary modulation as the control parameters. • Advanced high-efficiency controller by means of a model predictive controller.
4	• 3.6-kW and 600-W-24-output converter prototype. • 3.6-kW and 1800-W-5-output converter prototype. • 7.4-kW-two-phase and 1800-W-12-output converter prototype. • 3.6-kW and 1800-W-4-output WBG converter prototype.

5.2. Scientific results

This dissertation has been developed in the framework of several joint research and development projects between university and industry, as well as visits to other research centers and universities. The main results of this dissertation have been published in peer reviewed international journals, patents, international conferences, and national conferences. The most relevant results are summarized below.

5.2.1. International journals

[1] H. Sarnago, P. Guillén, J. M. Burdío, and O. Lucía, "Multiple-Output ZVS Resonant Inverter Architecture for Flexible Induction Heating Appliances," IEEE Access, vol. 7, pp. 157046-157056, 2019.

[2] O. Lucía, D. Navarro, P. Guillén, H. Sarnago, and S. Lucía, "Deep Learning-Based Magnetic Coupling Detection for Advanced Induction Heating Appliances," IEEE Access, vol. 7, pp. 181668-181677, 2019.

[3] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Acoustic noise analysis of multiplexed strategies in multi-output converters for induction cooktops," International Journal of Applied Electromagnetics and Mechanics, vol. Preprint, pp. 1-10, 2020.

[4] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Mains-Synchronized Pulse Density Modulation Strategy Applied to a ZVS Resonant Matrix Inverter," IEEE Transactions on Industrial Electronics, vol. 68, no. 11, pp. 10835-10844, 2021.

[5] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Asymmetrical Noncomplementary Modulation Strategies for Independent Power Control in Multioutput Resonant Inverters," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 1, pp. 629-637, 2021.

[6] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Series-Resonant Matrix Inverter with Asymmetrical Modulation for Improved Power Factor Correction in Flexible Induction Heating Appliances," IEEE Transactions on Industrial Electronics, pp. 1-1, 2022.

[7] P. Guillén, F. Fiedler, H. Sarnago, S. Lucía, and O. Lucía, "Deep Learning Implementation of Model Predictive Control for Multioutput Resonant Converters," IEEE Access, vol. 10, pp. 65228-65237, 2022.

5.2.2. Patents

[1] J. M. Burdio Pinilla, T. Cabeza Gozalo, P. Guillén Moya, S. Llorente Gil, O. Lucía Gil, D. Puyal Puente and H. Sarnago Andía, "Cooking Appliance," Patent WO2021069219, 2021.

[2] J. M. Burdio Pinilla, T. Cabeza Gozalo, P. Guillén Moya, S. Llorente Gil, O. Lucía Gil, and H. Sarnago Andía, "Induction Energy Transmission System," Patent WO2021122000, 2021.

5.2.3. International conferences

[1] H. Sarnago, O. Lucía, P. Guillén, and J. M. Burdio, "Bidirectional inductorless Dc-Dc converter for improved home appliance operation," in IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, 2017, pp. 916-921.

[2] P. Guillén, H. Sarnago, O. Lucia, and J. M. Burdío, "Acoustic noise analysis in multi-output converters for induction cooktops," in International Symposium on Heating by Electromagnetic Sources 2019 (HES-19), Padova, Italy, 2019, vol. 1, pp. 315-320.

[3] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Output-power multiplexation strategies for induction cooktops," in International Symposium on Heating by Electromagnetic Sources 2019 (HES-19), Padova, Italy, 2019, vol. 1, pp. 339-344.

[4] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Asymmetrical Modulation Strategies for Partially Covered Inductors in Flexible Induction Heating Appliances," in IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, 2019, vol. 1, pp. 5065-5069.

[5] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Multi-Output Resonant Power Converters for Domestic Induction Heating," in IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, 2020, pp. 4320-4327.

[6] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Power Factor Correction using Asymmetrical Modulation for Flexible Induction Heating Appliances," in 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 2021, pp. 753-757.

[7] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Efficiency-Oriented Comparison of Modulation Strategies of a Multi-Output ZVS Resonant Inverter for Domestic Induction Heating," in Proceeding of UIE 2021: XIX International UIE

Congress on Evolution and New Trends in Electrothermal Processes., Pilsen, Faculty of Electrical Engineering, University of West Bohemia, Czech Republic, 2021, pp. 37-38.

5.2.4. National conferences

[1] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Análisis de emisiones acústicas en convertidores de salida múltiple para calentamiento por inducción doméstico," in Actas del Seminario anual de automática, electrónica industrial e instrumentación 2018 (SAAEI'18), Barcelona, 2018.

[2] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Etapas electrónicas de potencia resonantes multi-salida para calentamiento por inducción doméstico," in Vol. 8: Actas de la IX Jornada de Jóvenes Investigadores del I3A - 11 de diciembre de 2020, Zaragoza, 2020.

[3] P. Guillén, F. Fiedler, H. Sarnago, S. Lucía, and O. Lucía, "Control Mediante Redes Neuronales de un Convertidor Resonante Multi-Salida para Calentamiento por Inducción," presented at the IX Jornadas Doctorales G-9, Bilbao, 2022.

[4] P. Guillén, H. Sarnago, O. Lucía, and J. M. Burdío, "Implementación de multi-inversor resonante mediante dispositivos de banda ancha para calentamiento por inducción doméstico," presented at the XI Jornada de Jóvenes Investigadores del I3A, Zaragoza, 2022.

5.2.5. Scholarships and additional merits

The author of this dissertation has been a visiting scholar on the following research centers, contributing to the results of this dissertation. These visits are listed and briefly described below:

- Research Engineer Internship at BSH Home Appliances Group, Zaragoza, Spain, from February 2, 2017 to August 31, 2017 and sporadically to May 9, 2019. Advisors: Dr. Sergio Llorente, Dr. Diego Puyal.
- Academic Internship at the Laboratory of Process Automation Systems, Technische Universität Dortmund, Dortmund, Germany, from August 1, 2021 to October 31, 2021. Advisor: Prof. Sergio Lucia.

The most relevant additional merits are also summarized below:

- PhD scholarship of the Ministerio de economía, industria y competitividad, Spanish Government (FPI grant - BES-2017-081065). July 1, 2018 – August 31, 2018.
- PhD scholarship of the Ministerio de educación y formación profesional, Spanish Government (FPU grant – FPU17/01442). September 1, 2018 – November 30, 2022.
- Short term mobility funding for FPU scholarships of the Ministerio de educación y formación profesional, Spanish Government (EST21/00298). August 1, 2021 – October 31, 2021.

5.3. Future research lines

This dissertation is focused on the study of a family of matrix-based multi-output inverters for domestic IH applications. As a result of this work, a single-column matrix-based ZVS resonant inverter and its modulation strategies have been proposed, analyzed, and experimentally implemented. Future research lines are oriented towards a further analysis of the cost, filter development to ensure complying with EMC standards, the generation of high-efficiency multi-output inverters for long-distance IH implementation, and the application of continuous non-complementary modulation strategies for wireless power transfer (WPT).

- Cost analysis

In this dissertation the technical approach to the proposed topology has focused on its behavior, the suitable modulation strategies and control strategies, and the performance result analysis. However, having in mind the direct application of this research field on consumer electronics the commercial viability analysis of this approach is justified. As it has been presented the implementation of the converter using current technology components is possible, enabling a rough cost comparison, but an in-depth cost analysis is necessary, taking into account additional advantages and disadvantages of an industrialized solution.

- Snubberless compliance of EMC standards

The promising results of non-complementary modulations for the independent power control of the different loads present the drawback of the incompatibility with regenerative snubber networks based on capacitors. In this thesis several prototypes that

present a device technology selection to minimize the efficiency reduction produced by this absence can be seen. However, the change in technology or the selection of fast-switching devices implies the increase of *dv/dt* of the square waveforms, leading to electromagnetic noise that can be injected into the mains or even radiated. The proposal of alternative snubber networks is a prospective field in order to minimize this inconvenience. Additionally, the design of EMC filters with higher cutoff frequencies can be addressed.

- Multi-output underworktop implementations

Long distance power transfer requires higher currents to achieve similar heating of the objective load. Moreover, small inductors present lower efficiencies. However, underworktop implementations provide a flexibility level never seen and would greatly benefit from multi coil implementations. In order to do so the development of high-efficiency multi-output converters that withstand high current is a prospective field that would benefit the user experience.

- NC modulation strategies for WPT

Future research trends in the field of domestic IH propose the utilization of IH cooktops to wireless power small kitchen appliances. Besides the manufacturing of a completely new line of wireless products, this approach presents implications from the power converter point of view. Two main fields related with this thesis can be prospected: the continuous power transfer and the multi-coil to single-coil power transmission. The first one is required in order to achieve simultaneous operation of different equipment or even while heating a IH load. The transferred power can be controlled with the same inverter applying continuous non-complementary modulation strategies, ensuring a continuous operation and thus no need of energy storage. Additionally, the second one boost the flexibility of the kitchen, eliminating the device placement position.

Capítulo 5

Conclusiones

En esta tesis se evalúa una familia de topologías inversoras matriciales multisalida que han sido desarrolladas para su utilización en calentamiento por inducción. Para ello, se ha realizado un estudio exhaustivo de la literatura, analizado las diferentes topologías, propuesto varias estrategias de modulación y construido prototipos experimentales para su validación.

En este capítulo final se presentan las principales conclusiones de este trabajo. En primer lugar, se resumen las conclusiones y aportaciones más relevantes de cada capítulo. Posteriormente, se destacan los principales resultados académicos. Por último, se explican brevemente las líneas de investigación futuras motivadas por esta tesis.

Contenidos

5. Conclusiones

En el siguiente capítulo se resumen las principales conclusiones de esta tesis y sus resultados científicos, siguiendo la división por capítulos del documento. Las principales aportaciones de cada capítulo se destacan al final de la sección de conclusiones, en la TABLE 5.1. Por último, se discuten las posibles líneas de investigación que surgen como continuación de este trabajo.

5.1. Conclusiones

Esta tesis se centra en la evaluación de una familia de topologías de salida multiple, con estructura matricial, para aplicaciones de calentamiento por inducción doméstico en cocinas de superficie flexible. Para ofrecer una visión completa del problema y de las alternativas que permiten alcanzar soluciones viables, el documento presenta la información de forma progresiva, sirviendo cada capítulo como base para la construcción del siguiente.

5.1.1. Topologías multisalida

En el capítulo 1 se ha presentado el fenómeno de calentamiento por inducción, la tecnología utilizada y las aplicaciones de cocinado a nivel doméstico, alcanzando los productos más vanguardistas. Tomando esto como base, se han abordado los esfuerzos investigadores para alimentar las estructuras de varias bobinas que presentan las superficies flexibles.

Las placas de cocción de superficie flexible, en su implementación comercial, presentan hasta 48 bobinas cuya potencia es proporcional a su tamaño y puede variar entre 1800 W y 600 W. Por lo tanto, el reto de alimentar un gran número de inductores de forma eficiente y versátil, cumpliendo con la normativa de compatibilidad electromagnética, proporcionando una buena experiencia de usuario y manteniendo un coste contenido motiva la investigación en inversores multisalida. Con el fin de ofrecer nuevas soluciones, en este capítulo se realiza un estudio del estado del arte de las distintas topologías inversoras multisalida.

Estos convertidores se han diseñado siguiendo distintos enfoques. La paralelización de inversores, es decir, el uso de un único inversor por bobina, consigue un buen nivel de controlabilidad pero requiere un elevado número de dispositivos de potencia. La multiplexación de cargas, por el contrario, pretende minimizar el número de inversores

añadiendo una etapa de relés adicional para seleccionar la conexión entre inversor y bobina, lo que da lugar a una controlabilidad limitada debido a la dinámica de los relés. Por último, un grupo más heterogéneo de convertidores multisalida incluye las soluciones que presentan diseños específicos con el objetivo de reducir el número de dispositivos de potencia, aumentar la flexibilidad de control o potenciar el rendimiento del inversor. Dentro de este último grupo, las soluciones que presentan un bajo número de dispositivos de potencia, están construidas con componentes de estado sólido y tienen una alta flexibilidad en el control, logrando un buen equilibrio entre rendimiento y coste, son las más prometedoras para la aplicación doméstica de calentamiento por inducción.

5.1.2. Inversores resonantes multisalida con estructura matricial

Aunque en la literatura se han propuesto varios inversores multisalida, éstos normalmente se centran en reducir el número de dispositivos de potencia, lo que lleva a soluciones cuyo funcionamiento se ve penalizado al aumentar el número de cargas de inducción. Por tanto, la posibilidad de diseñar topologías que mantengan la versatilidad en el control mientras se alimenta un elevado número de cargas de inducción simultáneamente con pocos dispositivos de potencia justifica el desarrollo de dichos sistemas. En el capítulo 2, se han propuesto tres topologías matriciales, derivadas de la topología semipuente, y se han analizado en base a su comportamiento.

El inversor resonante matricial multisalida ZCS presenta el menor número de dispositivos posible para un número n de cargas IH: $\sqrt{n}$ transistores y $2n$ diodos. Su operación está definida por los parámetros de cada carga de inducción y el tanque resonante, por lo que las formas de onda son independientes de la modulación, siempre que la frecuencia de conmutación esté por debajo de la de resonancia. En consecuencia, el tiempo durante el cual la corriente circula por la carga es fijo, y es posible operar encendiendo y apagando los transistores en condiciones de ZCS. Teniendo en cuenta este tiempo de operación determinado, es posible controlar la potencia transmitida a cada carga reduciendo la frecuencia de conmutación, es decir, aumentando el tiempo entre periodos activos, desde la resonante, que proporciona la máxima potencia. Esto puede presentar algunas restricciones, cuando se considera el calentamiento por inducción doméstico, ya que hay que evitar el ruido acústico y, por tanto, el funcionamiento por debajo de 20 kHz. Además, una de las principales desventajas de la topología es que la tensión de bloqueo del transistor también depende de los parámetros de la carga, lo que hace que presente valores elevados.

Para solucionar este problema, se ha propuesto la inclusión de diodos de *clamp* en cada una de las filas y columnas, dando lugar al inversor resonante matricial multisalida ZVS, con una implementación que requiere $\sqrt{n}$ transistores y $2n+\sqrt{n}$ diodos. Estos diodos funcionan como diodos en antiparalelo de los transistores correspondientes, lo que permite el flujo inverso de corriente y, por tanto, el encendido suave cuando se opera por encima de la frecuencia de resonancia. Además, también es posible operar por debajo de la frecuencia de resonancia, consiguiéndose en este caso el apagado ZCS, lo que conduce a un comportamiento en cada carga activa similar al del semipuente resonante.

Ambas topologías proporcionan un buen rendimiento para el funcionamiento con una única carga activa y varios casos de activación con varias cargas. Sin embargo, las combinaciones disponibles están limitadas por la activación diagonal, es decir, la activación no deseada de cargas que comparten transistores de lado alto y bajo con las cargas activas. Por lo tanto, se prefieren las activaciones de la misma columna o de la misma fila.

Para garantizar la activación de una sola fila o una sola columna, surge la propuesta de estructuras matriciales unidimensionales. En concreto, las siguientes líneas resumen las principales razones para implementar una estructura unidimensional:

- Requiere n+1 transistores y 2n diodos.
- La activación y desactivación de la carga, e incluso el control de la potencia, dependen únicamente de la modulación del transistor del lado bajo.
- El comportamiento del convertidor visto desde las cargas de inducción activas es similar al del semipuente.
- La conexión fija de la carga facilita la detección de la misma y el cálculo de sus parámetros equivalentes basados en la forma de onda de la corriente.
- El diodo antiparalelo incorporado permite incluir redes de *snubber* capacitivas para minimizar las pérdidas y el *dv/dt* en el transistor correspondiente.
- La estructura en columna reduce los requisitos en cuanto a circuitería de disparo ya que los transistores están referenciados a GND.

Todas estas ventajas motivan y justifican la propuesta de un inversor resonante ZVS de una sola columna. Además, la mayor flexibilidad de la topología permite implementar

estrategias de modulación tanto clásicas como más complejas para proporcionar la potencia necesaria a las diferentes cargas de inducción.

5.1.3. Estrategias de modulación del inversor resonante multisalida ZVS con estructura de columna

El control independiente de la potencia de cada una de las cargas puede lograrse utilizando varias estrategias de modulación, presentando cada una de ellas diferentes ventajas y limitaciones. En el capítulo 3, las estrategias de modulación propuestas se dividen en continuas, si se produce transferencia de potencia a todas las cargas activas en cada ciclo de conmutación, o discontinuas, en caso contrario.

Desde el enfoque discontinuo se elige como estrategia la multiplexación de cargas sincronizada con la red para cumplir con la mayoría de las restricciones, siendo la estrategia de modulación base el control de onda cuadrada. Además, se ha presentado una solución matemática para minimizar la fluctuación de la potencia de entrada y se han planteado distintas consideraciones para lograr una implementación adecuada del control en bucle cerrado.

El control continuo de la potencia se consigue mediante estrategias no complementarias. En el documento se ha presentado el enfoque analítico para lograr la no complementariedad mediante la modulación de dos parámetros diferentes. Además, se presentan consideraciones de lazo cerrado para beneficiarse de la versatilidad de la modulación y lograr una mejora del PFC. Por último, y basándose en la estrategia NC-PDM, se ha propuesto un controlador avanzado que utiliza MPC para obtener un seguimiento adecuado de la potencia optimizando la eficiencia.

5.1.4. Implementación y resultados experimentales

En el capítulo 4, se han propuesto implementaciones de la topología propuesta para diferentes condiciones de operación. Esto incluye la tipología de las cargas seleccionadas, el número de fases o la estrategia de modulación considerada para el control de potencia.

Para alimentar 24 bobinas de inducción de 600 W correspondientes a una implementación monofásica, se ha desarrollado un prototipo utilizando MOSFET. Este prototipo presenta dos inversores independientes con 12 salidas cada uno y medidas de potencia transmitida y caracterización de la carga basadas en el voltaje del condensador. El convertidor permite el control de potencia basado en una estrategia de multiplexación sincronizado con la red y alcanza una eficiencia superior al 92%.

En el caso de la utilización de la topología para alimentar entre 4 y 6 bobinas de 1800 W de potencia nominal se han construido tres prototipos diferentes.

Se ha diseñado una primera aproximación que permite una evaluación comparativa con las cocinas comerciales y que, por tanto, presenta tecnologías electrónicas actualmente en el mercado. El prototipo utiliza dispositivos IGBT con las mismas características en el lado alto y el lado bajo debido al bajo desequilibrio entre la potencia total de 3600 W y la potencia nominal de la bobina. Por su parte, la estrategia de modulación se elige estrechamente relacionada con la selección de la tecnología. Para beneficiarse de la posibilidad de implementar condensadores *snubber* en los transistores del lado bajo, aumentando la eficiencia, se selecciona una estrategia de multiplexación sincronizada con la red basada en control de onda cuadrada. Esta estrategia se valida considerando cada bobina como una carga independiente, consiguiendo un control de potencia independiente con un bajo rizado de potencia de entrada, lo que permite un periodo reducido y, por tanto, una baja fluctuación de temperatura en la olla.

Para aumentar la versatilidad del control, se ha propuesto un prototipo bifásico de 6 salidas por fase. Se ha diseñado utilizando la tecnología IGBT y los dispositivos de potencia se han seleccionado para conseguir unas pérdidas de potencia reducidas operando sin condensadores de *snubber*. Este diseño ha permitido el uso de estrategias de modulación no complementarias para una transferencia de potencia precisa a las diferentes cargas, logrando eficiencias superiores al 89%. Además, y basándose en la estrategia NC-PDC, se han implementado controles en lazo cerrado. El control en bucle cerrado con capacidad de corregir el factor de potencia consigue un aumento del factor de potencia de hasta 0,07 puntos y una reducción de la distorsión armónica de hasta el 80% al abordar el exceso de componentes armónicos. Además, el controlador avanzado basado en *Model Predictive Control* consigue una respuesta rápida y un control óptimo en términos de eficiencia.

Por último, basándose en la contribución de las pérdidas de conmutación a las pérdidas globales del convertidor, se ha propuesto un prototipo de 4 salidas que utiliza transistores de GaN y diodos de SiC, y muestra un funcionamiento adecuado, tiempos de conmutación cortos y, por tanto, pérdidas de potencia reducidas.

A continuación se presenta la TABLE 5.1, que resume las principales aportaciones de esta tesis.

TABLA 5.1. RESUMEN DE LAS PRINCIPALES CONTRIBUCIONES

CAPÍTULO	CONTRIBUCIONES
1	• Estudio del estado del arte de las topologías multisalida para superficies de inducción flexibles en inducción doméstica.
2	• Inversor matricial multisalida ZVS. • Inversor matricial multisalida ZVS con estructura de columna. • Estudio de las ventajas principales de los inversores matriciales multisalida para superficies flexibles para calentamiento por inducción doméstico. • Análisis de las configuraciones, formas de onda y grados de libertad para el diseño de estrategias de modulación de los inversores propuestos.
3	• Estrategia de modulación multisalida para el control independiente de la potencia, basada en la multiplexación de cargas con fluctuación reducida de la potencia pulsada, adaptada al inversor matricial multisalida ZVS con estructura de columna. • Consideraciones para la implementación de un control en bucle cerrado basado en la estrategia de multiplexación de cargas con fluctuación reducida de la potencia pulsada. • Estrategia de modulación multisalida para el control independiente de la potencia, basada en la activación no complementaria de los transistores, adaptada al inversor matricial multisalida ZVS con estructura de columna. • Consideraciones para la implementación de un control en bucle cerrado con capacidad de corrección del factor de potencia, basado en el control de los parámetros de las estrategias de modulación no complementarias. • Controlador avanzado de alta eficiencia basado en *Model Predictive Control* y las estrategias de modulación no complementarias.
4	• Prototipo de convertidor de 3.6 kW con 24 salidas de 600 W. • Prototipo de convertidor de 3.6 kW con 5 salidas de 1800. • Prototipo de convertidor de dos fases y 7.2 kW con 12 salidas de 1800 W. • Prototipo de convertidor de 3.6 kW con 4 salidas de 1800 W, con dispositivos de WBG.

5.2. Resultados científicos

Esta tesis se ha desarrollado en el marco de varios proyectos de investigación y desarrollo conjuntamente entre la universidad y la industria, así como de visitas a otros centros de investigación y universidades. Los principales resultados de esta tesis han sido publicados en revistas internacionales con revisión por pares, patentes, conferencias internacionales y conferencias nacionales. Los resultados más relevantes se resumen a continuación.

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5.2.5. Becas y méritos adicionales

El autor de esta tesis ha sido estudiante visitante en los siguientes centros de investigación, lo que ha contribuido a los resultados de esta disertación. Estas visitas se enumeran y describen brevemente a continuación:

- Becario en el departamento de predesarrollo, BSH Electrodomésticos España S.A., Zaragoza, España, desde el 2 de febrero de 2017 al 31 de agosto de 2017 y, esporádicamente, hasta el 9 de mayo de 2019. Supervisores: Dr. Sergio Llorente, Dr. Diego Puyal.
- Investigador visitante en el Laboratory of Process Automation Systems, Technische Universität Dortmund, Dortmund, Alemania, desde el 1 de agosto 2021 al 31 de octubre de 2021. Supervisor: Prof. Sergio Lucia.

Adicionalmente, otros méritos relevantes se resumen a continuación:

- Beca para la realización de los estudios de doctorado del Ministerio de economía, industria y competitividad, Gobierno de España (FPI - BES-2017-081065). Del 1 de julio de 2018 al 31 de agosto de 2018.
- Beca para la realización de los estudios de doctorado del Ministerio de educación y formación profesional, Gobierno de España (FPU - FPU17/01442). Del 1 de septiembre de 2018 al 30 de noviembre de 2022.

- Beca para la realización de estancias breves para beneficiarios de la ayuda FPU del Ministerio de educación y formación profesional, Gobierno de España (EST21/00298). Del 1 de agosto de 2021 al 31 de octubre de 2021.

5.3. Líneas de trabajo futuras

Esta tesis se centra en el estudio de una familia de inversores multisalida de estructura matricial para calentamiento por inducción doméstico. Como resultado de este trabajo, se ha propuesto, analizado e implementado experimentalmente un inversor resonante multisalida ZVS con estructura de columna y sus estrategias de modulación. Las líneas de trabajo futuras se orientan a un mayor análisis del coste, al desarrollo de filtros para asegurar el cumplimiento de la normativa de EMC, a la generación de inversores multisalida de alta eficiencia para la implementación de calentamiento por inducción a larga distancia, y a la aplicación de estrategias de modulación continua no complementaria para la transferencia inalámbrica de potencia (WPT).

- Análisis de coste

En esta tesis el planteamiento técnico de la topología propuesta se ha centrado en su comportamiento, en el diseño de estrategias de modulación y control adecuadas y en el análisis de los resultados de operación. Sin embargo, teniendo en cuenta la aplicación directa de este campo de investigación en productos de electrónica de consumo, queda justificad el análisis de la viabilidad comercial de estas topologías. Tal y como se ha presentado, la implementación del convertidor utilizando componentes actualmente en el mercado es posible, lo que permite una comparación de costes aproximada, pero es necesario un análisis de costes en profundidad, teniendo en cuenta las ventajas e inconvenientes adicionales de una solución industrializada.

- Cumplimiento de la normativa de compatibilidad electromagnética sin *snubbers*

Los prometedores resultados de las modulaciones no complementarias para el control independiente de potencia de las diferentes cargas presentan el inconveniente de la incompatibilidad con las redes de *snubber* regenerativas basadas en condensadores. En esta tesis se presentan varios prototipos con una selección de tecnología de dispositivos que pretende minimizar la penalización en la eficiencia producida por esta ausencia. Sin embargo, el cambio de tecnología o la selección de dispositivos de conmutación rápida implica el aumento del *dv/dt* de las formas de onda cuadradas, dando lugar a ruido electromagnético que puede ser inyectado a la red o incluso radiado. La propuesta de

redes *snubber* alternativas es un campo de investigación interesante para minimizar este inconveniente. Además, se puede abordar el diseño de filtros con frecuencias de corte más altas.

- Implementaciones bajo encimera de etapas multisalida

La transferencia de energía a larga distancia requiere corrientes más altas para lograr un calentamiento similar de la carga objetivo. Además, los inductores pequeños presentan eficiencias más bajas. Sin embargo, las implementaciones bajo encimera ofrecen un nivel de flexibilidad nunca visto y se beneficiarían enormemente de las distribuciones multibobina. Para ello, el desarrollo de convertidores multisalida de alta eficiencia que soporten altas corrientes es un campo que mejoraría la percepción del producto por el usuario.

- Estrategias de modulación no complementarias para transferencia de energía sin contacto.

Las tendencias de investigación en el campo del calentamiento por inducción doméstico proponen la utilización de las cocinas de inducción para alimentar de forma inalámbrica pequeños electrodomésticos. Además de la fabricación de una línea completamente nueva de electrodomésticos inalámbricos, este enfoque presenta implicaciones desde el punto de vista del convertidor de potencia. Se puede investigar en dos campos principales relacionados con esta tesis: la transferencia de potencia continua y la transmisión de potencia de bobina múltiple a bobina simple. La primera es necesaria para conseguir el funcionamiento simultáneo de diferentes equipos o incluso mientras se calienta una carga de inducción, es decir, una olla. La potencia transferida puede controlarse con el mismo inversor aplicando estrategias de modulación no complementarias, asegurando un funcionamiento continuo y, por tanto, sin necesidad de almacenamiento de energía. Además, el segundo potencia la flexibilidad de la cocina, eliminando la posición de colocación de los equipos.

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