Integrated Multi-Bit All-Optical NOR Gate for High Speed Data Processing

Miguel Cabezón, Asier Villafranca, Juan J. Martínez, David Izquierdo, and Ignacio Garcés

***Abstract*— In this paper, we study the use of integrated semiconductor optical amplifiers as the basic building block for larger-scale programmable photonic circuits. Making use of the non-linear response of these devices, we study the performance of 4-bit all-optical NOR gates based on fully integrable components for high speed all-optical look up tables. Feasibility of the proposed architecture is demonstrated by proof-of-concept experiments using both commercially available devices and photonic integrated circuits.**

***Index Terms*—Logic gates, optical wavelength conversion, photonic integrated circuits, programmable logic devices, semiconductor optical amplifiers.**

I. Introduction

All-optical data processing is a highly desirable technology for optical telecom, since it may allow avoiding opto-electronic and electro-optic conversion in non-terminal network nodes. Nowadays some degree of processing can be present in optical networks, such as wavelength conversion and optical regeneration but their applications are very limited due to the lack of interaction with the signal data. In the last years photonics have demonstrated the capability of performing simple logic operations at very high-speed, mainly by exploiting different non-linear effects of semiconductor optical amplifiers (SOA) [1]–[5] such as Four-Wave Mixing [6], Cross Gain Modulation [3], [6]–[12] and Cross Phase Modulation [4], [13], [14] and, although they make SOAs a non-ideal solution for pure amplifying purposes, have proved to be helpful for all-optical logic processing reaching rates of 40 Gbps and above [13], [15]–[17]. Based on these effects, some logic gates such as NOT [18], AND [18], XOR [13], [14], [19]–[21], XNOR [6], NOR [9], [15], [22] and NAND [8], [14] have been demonstrated so far using SOAs, solely or in combination with other SOAs, in parallel or in cascade and there is extensive research to improve the nonlinear performance of these devices [23]. Fast logic gates have also been implemented using other optical elements such as PPLN waveguides [24] and silicon nanowires [25]. However, these logic gates can only perform simple operations and efforts towards higher-scale processing are very scarce in literature.

We consider that, in parallel to the necessary research to enhance the performance of the devices and the fabrication processes, it is also the moment to start researching feasible approaches and architectures for larger-scale optical data processing, which may include multi-bit data processing. 4-bit minterms and maxterms generation reconfigurable logic was demonstrated with DPSK signals in [26], [27]. Also, in a previous work [7], we introduced the architecture for the construction of an all-optical 4-bit programmable logic device, being the basic building block of a FPGA and based on the use of multi-bit all-optical NOR gates. However there are some considerations to be made when moving to photonic integrated circuits (PICs), as described in the following sections. In Section II we present a careful evaluation of the use of SOAs as multi-bit, high speed NOR gates able to be used in the proposed Look-up Table (LUT). We evaluate the XGM effect of the SOAs and will discuss their operation as multi-bit NOR gates. In Sections III and IV we will report the results from proof of concept experiments for a 4-bit NOR gate using commercial devices and an integrated design respectively. Conclusions derived from our work will be discussed in Section V.

II. NOR-Based Look-Up Table

NOR logic in SOAs is performed by exploiting Cross Gain Modulation (XGM) nonlinear effect. XGM takes place inside the SOA cavity when two inputs, a high-power signal (pump) and a lower-power signal (probe), are combined inside the device. Carriers in the active region of the SOA are depleted by the amplification of the high-power signal (pump) and thus the probe suffers from absorption in the absence of carriers. When pump and probe are amplitude modulated signals the output of the SOA can be seen as the logic function AND over the probe and the negative of the pump. This effect has been broadly studied in literature and has two main set-up approaches: counter-propagating [18] and co-propagating signals [9], as can be seen in Figs. 1(a) and (b). Propagation in both directions is analyzed in [28].

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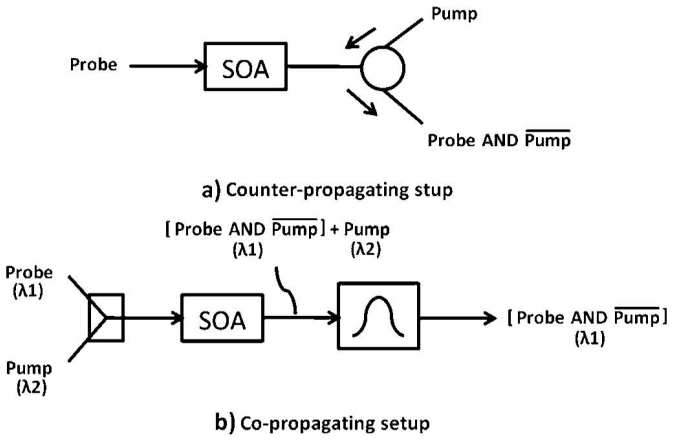

Fig. 1. XGM basic set-up: (a) counter-propagation, (b) co-propagation.

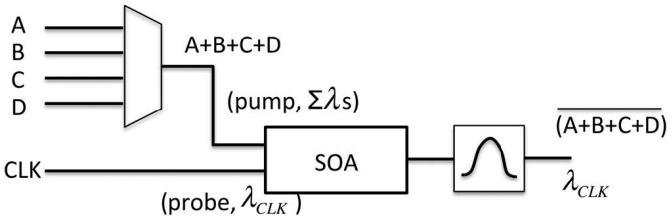

Fig. 2. Scheme of operation of a 4-bit NOR gate.

Both setups have advantages and disadvantages, and some considerations have to be taken in account, especially in the integrated design. Counter-propagating set-up can work using the same wavelength for both pump and probe signals, which is its main advantage. However, since the differentiation of signals is achieved by their direction of propagation, a circulator device is needed to separate them, increasing the setup complexity. Moreover, circulators are rarely found in integrated circuits since they are big, lossy and difficult to reproduce [29]. The use of filters removes part of the ASE and can be helpful in this configuration but is not necessary.

On the other hand co-propagating setups need the signals to be in different wavelengths and a bandpass filter is needed at the output to discard the pump wavelengths. However, as for the counter-propagating scheme, it also improves the signal to noise ratio. The architecture chosen for our NOR gate will use a co-propagating scheme due to the impossibility to include circulators in our integrated device.

Fig. 2 shows a scheme of the operation of a SOA acting as a NOR gate for 4 inputs A, B, C and D. Only when all inputs are simultaneously '0', the combination of the XGM inside the SOA plus the filter gives '1' at the wavelength of the clock signal that acts as a probe (always a logic '1'). Therefore, is necessary to configure the response of the SOA versus pump and probe in such a way that for all the possible levels of optical power of the pump (which is variable depending on the number of '1's) the XGM effect suppresses the probe signal. In this work every data stream will have a different wavelength to avoid interference effects into the SOA. Clock's wavelength will also be different from the pumps in order to be effectively filtered at the output of the SOA. It should be noted that the NOT(A+B+C+D) signal is equivalent to

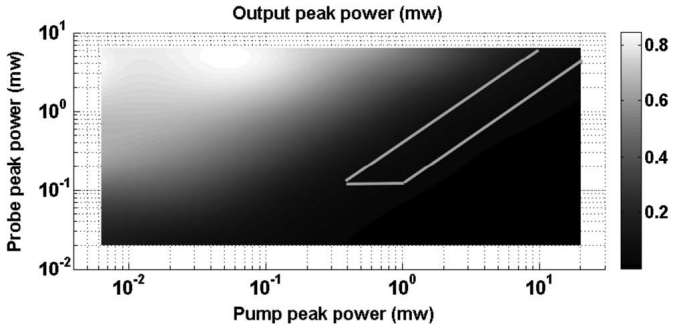

Fig. 3. Measured output suppression against pump power for different probe powers.

NOR(A,B,C,D). In fact, it is possible to build a LUT using all possible combination of the 4 bits and their negative values and using the NOR gate as a switch.

XGM characterization was performed in different samples of commercially available non-linear SOAs. Both pump and probe were modulated using a 10 GHz clock, presenting a bandwidth similar to a 10 Gbps RZ all-one bit stream. The SOA gain is modulated by the pump and is inversely proportional to it, but output power is also dependent on the probe. A low probe '1' level will have low power at the output even when pump is '0'. A basic characterization for different pump and probe optical power has been performed to show the best range for which an optimum XGM interaction can be achieved. It should be emphasized that the probe pulses must be suppressed if any of the data streams A, B, C, or D has optical power (any of them are '1') but they must pass through when the optical power is low enough (all of them are simultaneously '0'). For that reason output power is shown in Fig. 3 as a function of both pump and probe obtained for a SOA-XN-OEC-1550 model from CIP and using the co-propagating setup showed in Fig. 1(b). It can be observed that the output is rapidly reduced as the pump increases: the lowest output power is achieved, as expected, for the lowest probe and highest pump. Roughly half of the graph surface, corresponding to the darkest area shows an acceptable output power for the "0" level and therefore we can consider probe pulses to be enough suppressed. However, it is also necessary to have a relatively high probe power in order to achieve a good "1" level at the output.

For higher pump peaks the suppression is better for any probe optical power. Therefore, the extinction ratio of the output pulses will be also better if we achieve high output pulse levels. But if pump increases too much, all probe pulses will be suppressed, including those that should appear as "1" at the output.

For that reason we estimate the optimum working point is more likely to be in the area within the grey lines, close to the transition region and for probe powers higher than 10^{-1} mW. This characterization of XGM in the SOA lets us set an initial power balance for the N-input setup. Previously mentioned NOR function is achieved by using a pump signal which is the optical sum of a number of different data signals. This means that pump pulses can show several different power levels. The key factor is that all those pulses must have the same effect

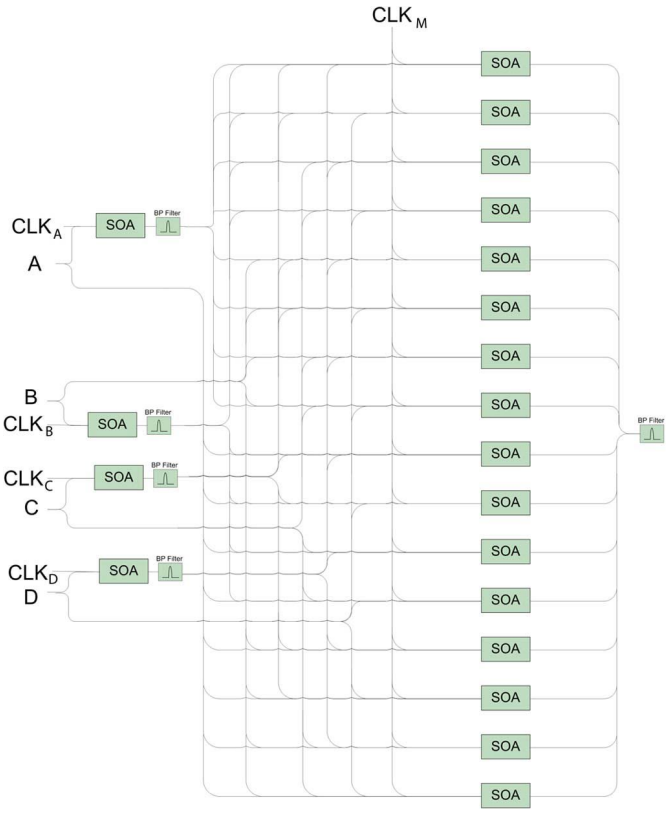

Fig. 4. Scheme for the proposed architecture of a 4-bit LUT.

over the probe signal; so we take advantage of the wide range of pump powers that can produce enough gain suppression in a simple 1-pump setup to make it work with different pump levels; which will allow us to prove LUT architecture.

A 4-bit LUT is a logic device, equivalent to a binary decoder whose 16 outputs can be combined in an arbitrary way to achieve any logic function with 4-bit input and 1-bit output. Its truth table has 16 different positions that are addressed by all the possible combinations of the 4-bit input data streams and their negatives. When each of these combinations is introduced in the LUT input, it returns the logic value programmed in the correspondent address. According to Boolean logic, any logic function can be expressed as a sum of NOR gates, where each NOR corresponds to one position of the truth table combination of the input signals and those inverted (A/not(A), B/not(B), C/not(C), D/not(D)).

In the purposed architecture the programming of the LUT can be made by just controlling the bias current of each address SOA. When biased, the SOA will act as a 4-bit NOR gate, letting CLK through the gate only when all inputs are a logic '0', and obtaining a logic '1' at the output only for an all-zero input. If not biased, the SOA will absorb both the CLK and the signals and a '0' level will be the output at the corresponding address. For the construction of a 4-bit LUT using SOAs acting as NOR gates, we would need 16 gates to get all possible output combinations for a 4-bit input, as can be seen from Fig. 4. In addition, we would need 4 gates acting as NOT gates to generate all possible bit combinations. That would mean 20 gates, and thus 20 SOAs would be needed for a complete circuit, although every input data stream will pass only through one or two SOAs.

III. SINGLE NOR GATE USING COMMERCIALLY AVAILABLE SOAS

In this section the process and proof-of-concept experiment to obtain a 4-input NOR gate using a single SOA commercial device at 10 Gbps is presented.

A. Experimental Setup

After checking the XGM effect in the SOA at different input optical powers we are able to build the NOR gate. As previous mentioned, XGM effect for two signals pump and probe produces the function (probe) AND [NOT(pump)]. When the pump is the sum of 4 different data signals (A,B,C and D) and the probe is a clock signal (equivalent to an all-one RZ signal) synchronized at the same bitrate, we can get the logic function NOT(A+B+C+D) which is equivalent to NOR(A,B,C,D).

The experimental setup used to create and test the NOR gate is shown in Fig. 5. Most of this setup is arranged to create and synchronize the four data streams and the clock signal. Four tunable laser sources (TLSs) are used for the four different pumps, while another TLS is used as a CW source for the probe clock. The four pumps are coupled into an amplifier in order to control their optical powers with respect to that of the probe and then intensity-modulated by a 10 Gbps NRZ 2^7-1 PRBS signal by a Mach Zenhder Modulator (MZM). All modulated NRZ pumps and the source probe are coupled and modulated again with a 10 GHz clock

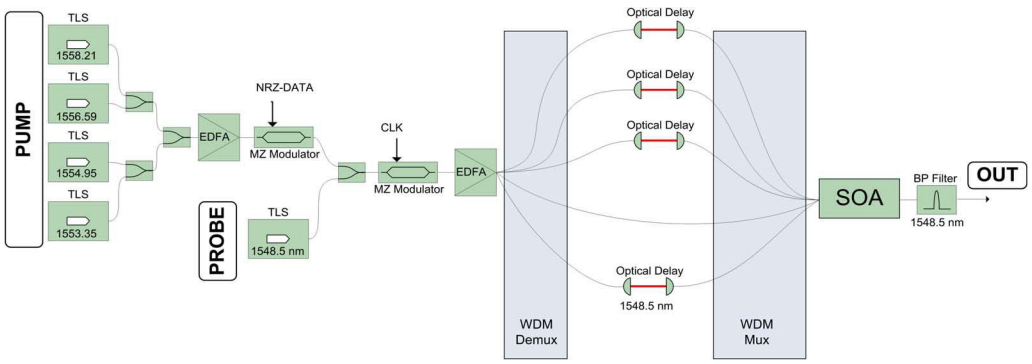

Fig. 5. Experimental setup for the generation of the 4-bit data streams and the NOR gate.

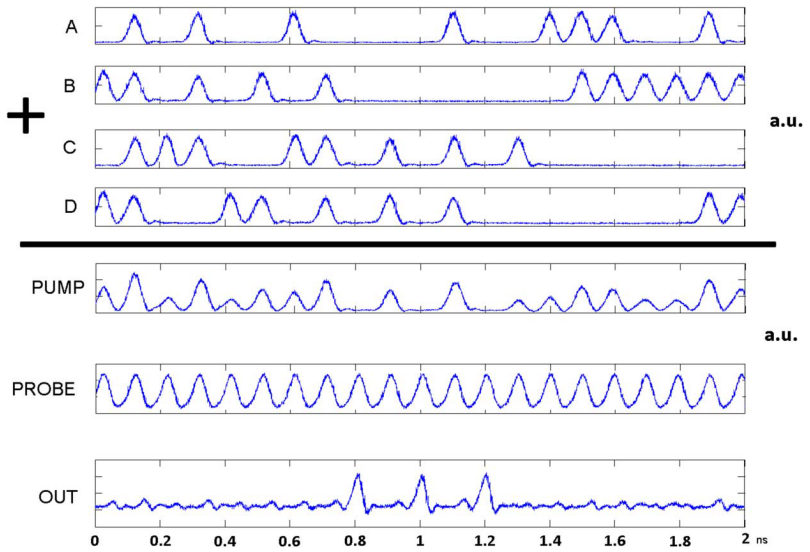

Fig. 6. Multi-bit pump, probe and output traces at the NOR gate. Pump signal is made by the sum of A, B, C and D signals.

synchronized to perform a RZ carving over the already existing NRZ modulation. In this way we have in the same fiber five different wavelengths being four of them 10 Gbps RZ modulated pump signals and an all-one RZ clock signal probe. Signals are separated using a WDM demultiplexer and delayed several bits to get four different synchronized pump RZ signals and then coupled again in the same fiber with the WDM multiplexer. The probe is also delayed to adjust its bit-timing with respect to the pumps. Finally, once all signals are coupled using the WDM multiplexer, they reach the SOA, where the logic function is performed. After the SOA a filter centered at the wavelength of the probe is placed to discard the pumps and obtain the expected NOR output. It must be noted that the WDM multiplexer and demultiplexer are necessary in this particular method to generate the signals, but they would not be necessary if each of the four signals (A,B,C,D) were generated independently or came from other optical gates.

B. Results

The behavior of the experimental scheme is shown in Fig. 6. The sum of the 4 different data-modulated pumps gives total pump pulses of different sizes, depending on the number of them that are '1' at each bit period. The key issue is that all these pulses, regardless of their size, must cause enough gain reduction in the SOA to get a '0' level at the output. Only when all pump signals are simultaneously '0', a '1' is obtained at the output.

Experimental results have shown that the best behavior in the output is achieved when the probe pulses arrive at the SOA slightly later than the pump ones, according to the gain variation profile and its recovery time. This extra delay can be easily controlled using the optical delay line in the probe wavelength and it would be a design parameter for the synchronization of the signals.

Spectra of the different signals at the input and output of the SOA, measured using a high resolution OSA, can be seen in Fig. 7. At the input, it can be seen the typical spectrum of the PRBS signals in every pump wavelength, while the probe

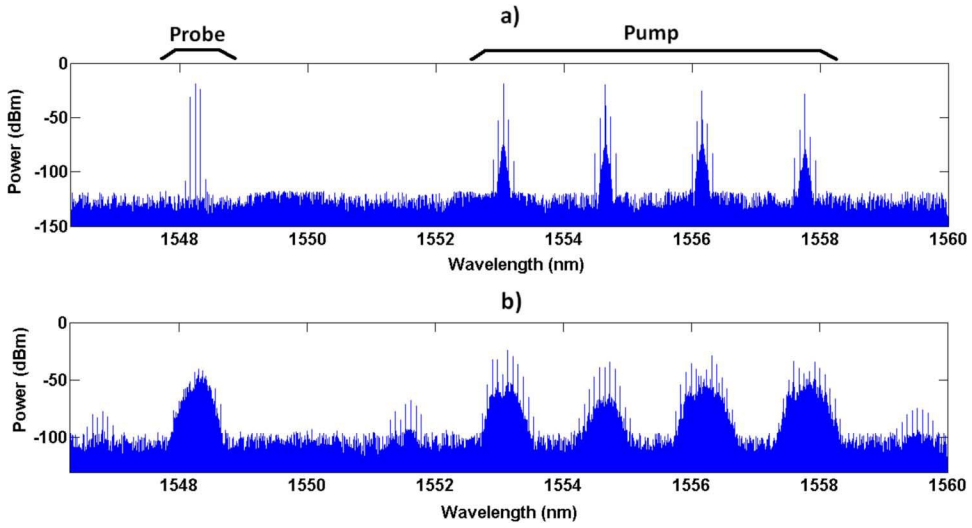

Fig. 7. Signals spectra at the (a) SOA input and (b) SOA output.

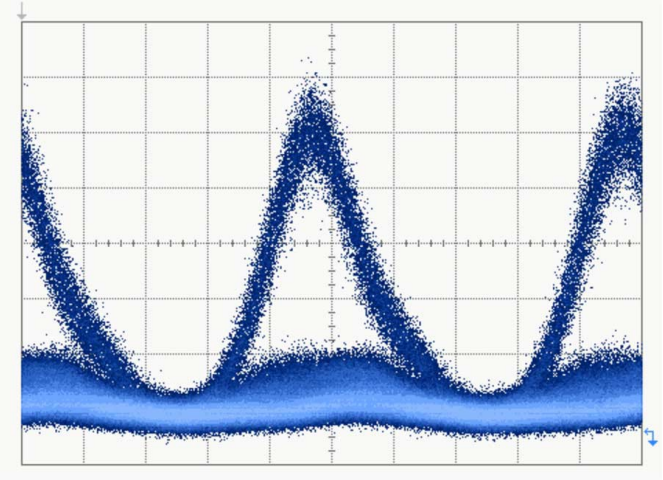

Fig. 8. Eye diagram of NOR output (Y: Power [a.u.]; X: time [20 ps/div]).

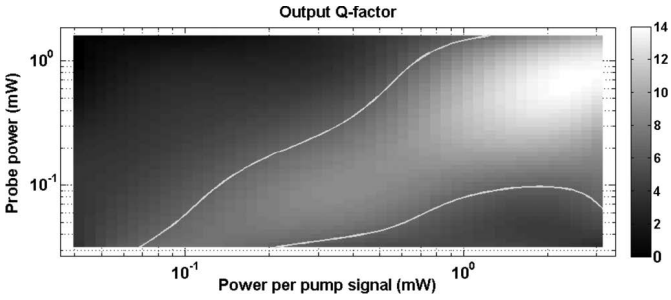

Fig. 9. Q-factor of 4-bit NOR output with respect to input powers.

shows the spectrum of a clock signal. Spectra of all signals at the output are clearly widened due to chirp, but as can be seen from Fig. 6 it does not degrade the quality of the output pulses. It can be also seen FourWave Mixing (FWM) signals produced at the SOA at different wavelengths but they will be filtered, as the probe wavelength is the only one at the output. Therefore, it is needed to choose a probe wavelength out of band from FWM wavelengths, which is easy because we have freedom to choose pump and probe wavelengths in the gain spectrum of the device.

There are two aspects that have to be verified to confirm the proper functioning of the logic gate. First is the behaviour of the NOR logic function itself, which means that the output can only be '1' when all the pump inputs are '0' and must be '0' for all the other possible inputs. Using 2^7-1 PRBS traces for the data patterns (short enough to check all possible combinations) the correct response of the NOR gate has been successfully checked as can be seen for a small portion of the traces in Fig. 6.

Once we have checked that the logic gate is working as we expected the next step is to determine the quality of the output signal by means of an eye diagram aperture, which is showed in Fig. 8. This time 2^{31}-1 PRBS pumps were used (with no visible change from the shorter PRBS appreciated). After diverse test the ideal output eyes can be seen when using a power balance of 0.6 mW of peak pulse optical power for probe and 2.5 mW of peak pulse optical power for each pump signal. According to the logic function and with the pump

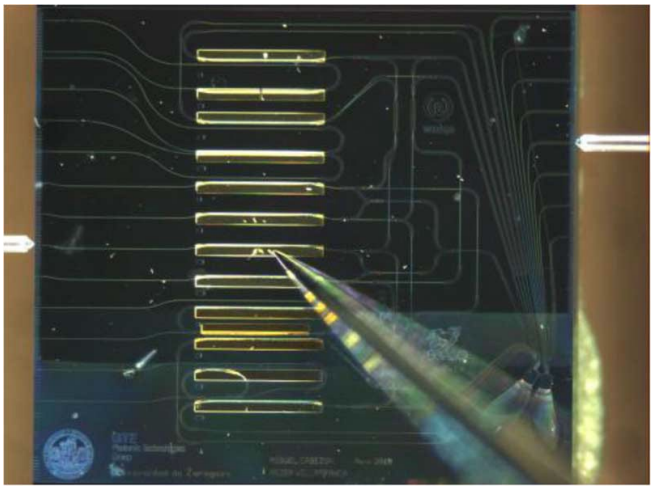

Fig. 10. Fabricated chip with different SOAs and the AWG filtering element. It can also be seen input and output lensed fibers at both sides of the PIC.

PRBSs having 50% of ones and zeros we can expect an output of only 6.25% of ones. For this reason measurements are presented in terms of pulse peak optical power rather than the mean optical power of the signal.

A slight power variation can be observed in the zero level due to the different combinations of the input pump bits. Depending on how many of them are '1', the total pump power will be different and so the resulting suppression of the given probe. However, it shows a clear aperture that allows error-free operation. It also shows a more intense lower level since only one out of the 16 possible inputs is a '1' at the output.

Although power required for optimum balance is relatively high, there is a relation between probe and pump powers for which a quasi-optimum output signal can be achieved. Evolution of output signal quality as a function of input powers can be observed in Fig. 9.

With the reduction of both pump and probe signals the logic function is still performed. Q-factor, measured over the eye diagrams, can be maintained above 9 if we reduce input powers down to 0.25 and 0.065 mW for pump and probe respectively; and even lower power can give an output Q>7, which corresponds to the area within the white line in Fig. 9 and is still considered as error free. This wide input range implies great flexibility and allows the possibility of cascading logic gates, since a 0.6 or 0.7-mW pulse is large enough to pump other NOR gates.

IV. INTEGRATED ALL-OPTICAL GATE

After testing the response for a 10 Gbps 4-input NOR gate using discrete commercial devices, the next step in the evolution of our proposal is implement the logic gate using an integrated device at a higher bitrate. So, we designed and tested a photonic integrated circuit (PIC) where an integrated SOA and a filtering element used to discriminate the pumps at the output are the basis to obtain an integrated all optical NOR gate at 25 Gbps.

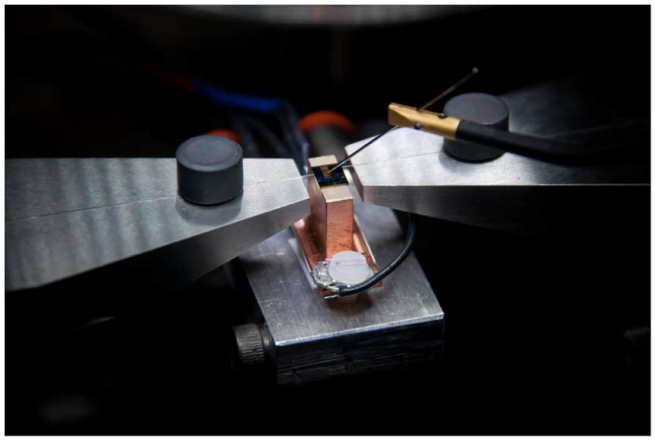

Fig. 11. Experimental setup for temperature control and current and light injection in the chip.

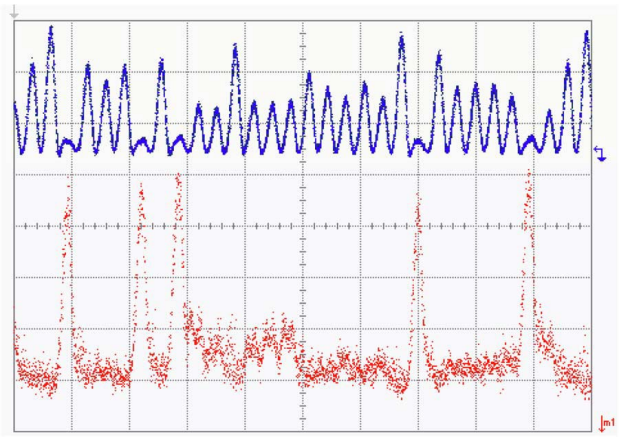

Fig. 12. Traces for pump input signal (upper trace) and output signal from the NOR gate (lower trace) (Y: Power [a.u.]; X: time [120 ps/div]).

A. Integrated Circuit Design and Fabrication

The PIC used in the experiments has been designed and fabricated in the framework of the JePPIX platform using InP active-passive integration technology. The design of the PIC is more complicated than a single NOR gate: up to 12 SOAs have been integrated in the device and there are different connections to obtain a proof of concept for the LUT shown in Fig. 4. One of this SOAs, connected to the filtering element, has been used to obtain the NOR gate integrated in the chip. The central channel of a 9-channel AWG with a 3 dB bandwidth of 0.7 nm per channel was used as filtering element. An image of the final integrated circuit can be seen in Fig. 10. Rectangular waveguides of 2×1 μm were used to propagate the light on-chip. All inputs and outputs are orthogonal to the chip facets and an antireflection coating was used to improve injection efficiency. The maximum length available in JePPIX platform for the active region, where the SOA is placed, (1 mm) was selected to increase nonlinear effects in the amplifier, with the intention of enhance the XGM used to perform the logic operation. An input angle of 7° was used in the transitions between active and passive zones to avoid reflections and lasing effects in the cavity.

A non-linear gain of 15 dB in a bandwidth of 80 nm centered in the C band was measured for the fabricated SOA, which was enough to perform the logic operations in the device. One of the key differences from the commercial SOA is the polarization dependent loss (PDL): while the commercial amplifier has less than 1 dB PDL, the integrated circuit was optimized for TE mode and presents a PDL of around 20 dB. Therefore, in the experimental setup the polarization of the signals entering the PIC must be controlled, adding complexity to the experiment.

B. Experimental Setup

The experimental configuration will be similar to the previous experiment (Section III) regarding light sources and signal management. The higher bitrate implies adding higher bandwidth MZM and electronics to achieve the desired 25 Gbps. A probe needle was used to apply a constant current of 260 mA was applied to the SOA. The chip rests on a copper chuck, as seen on Fig. 11. A thermistor inside the chuck monitors the temperature and a Peltier module was placed underneath to control it. The aluminum plate at the bottom contains a water-cooling circuit and acts as a heat sink.

Optical power levels coming out from the PIC are in the range of 20 dB lower than these of the discrete experiment, due mainly to optical losses on chip i.e. optical insertion losses, propagation losses, splitting and crossing waveguide losses and the own AWG insertion losses. So it was necessary to amplify output signals from the PIC by means of an EDFA.

The distribution of the wavelengths has been also modified to use the central channel of the AWG as an effective output filter, being able to slightly tune the pass wavelength by temperature control.

C. Results

25-Gbps operation of the device can be seen in the traces presented in Fig. 12. On the upper part of the graph, the sum of the four different 2^7-1 PRBS pump signals at the input is presented, while the resulting output of the NOR gate at the wavelength of the probe signal can be seen in the lower trace.

Input pump signal shows a multi-level optical power caused by the sum of four data streams that can present different levels of high (‘1’) values, or even a low optical power value

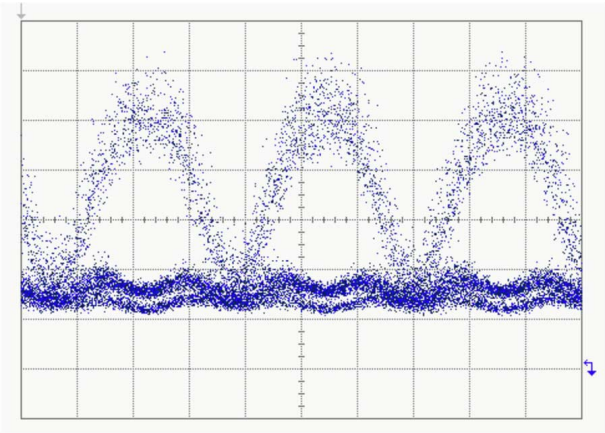

Fig. 13. Eye diagram measured for the amplified output of the all optical NOR gate at 25 Gbps (Y: Power [a.u.]; X: time [12 ps/div]).

when all data streams have simultaneously a low power value (‘0’).

Output signal presents the behaviour expected for the NOR logic gate, where it can be clearly seen that only when the input pump is ‘0’ there is a ‘1’ at the output, and for any other value of the pump the output remains ‘0’. As mentioned in the case of commercial devices, the output signal shows significantly less pulses per unit-time than the input, since only one input combination out of 16 must give a ‘1’ at the output for such logic function.

This can be appreciated in the correspondent eye diagram presented in Fig. 13, which shows a darker lower level and traces presenting reasonably open RZ pulses. It can also be observed a double level for zeros, probably due to misadjustments in the optical power of the different pump signals that lead to different levels of gain suppression. A CW level can also be seen in the eye diagram due to the ASE coming from the output signal amplification, needed to observe it in the Digital Communication Analyser (DCA) oscilloscope.

V. CONCLUSION

Multi-bit data streams are expected to be used in the next generation of all-optical data processing architectures, although we are aware that great challenges have to be addressed in terms of integration, synchronization and scalability. However, we think that multi-bit processing should help to build simpler and lower power devices, which is the base to future architectures and technologies.

In this work, the viability of an integrated all optical multi-bit NOR gate operating at high rates (25 Gbps) able to be used in a LUT design has been proved. Using a commercially available SOA in a discrete experimental setup we have studied the characteristics of the device for XGM operation in terms of pump and probe optical power. The operation of the SOA plus an optical filter as a 4-bit NOR gate at 10 Gbps has been shown. Once the logic gate behavior has been proved, both parts of the NOR (SOA and optical filter) have been integrated into a single PIC and at the same time the processing speed has increased to bitrates far from the standard electronic processing speed. The PIC was designed and successfully fabricated under the framework of the JePPIX platform using InP technology, and using it we have demonstrated its operation as an integrated all-optical 4-bit NOR gate functioning at 25 Gbps.

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