

# Gigabit Receiver over 1-mm SI-POF for Home Area Networks

Francisco Aznar, Carlos Sánchez-Azqueta, Santiago Celma and Belén Calvo, *Member, IEEE*

**Abstract**— A novel receiver front-end is proposed for short-range optical communications over low-cost polymer optical fiber and, in particular, for home area networks. This paper focuses on the experimental verification of the IC prototype POFchip-II, implemented in a standard 0.18- $\mu\text{m}$  CMOS technology plus a commercial Si-PIN photodetector and a 1-mm SI-POF transmission channel. A 1.25 Gb/s data transmission rate is attained for POF lengths ranging from 10 to 50 m thanks to a continuous-time adaptive equalizer included in the receiver chain that compensates the limited and length-dependent speed of POF. The measured sensitivity of the receiver leads to an eye-safety approach up to almost 30-m reach.

**Index Terms**—Electronic equalization, home area network, optical receiver, step-index polymer optical fiber.

## I. INTRODUCTION

SHORT-RANGE optical communications is the most promising solution to achieve gigabit transmission for single-user applications. Because economic viability is a must to compete with their electrical counterparts, 1-mm core step-index plastic optical fiber (SI-POF) [1] and standard complementary metal oxide semiconductor (CMOS) technology are proposed as a cost-effective combination. In addition to the reduction of the overall cost, this approach offers a number of advantages over copper cabling – total immunity to electromagnetic interference, the possibility of being deployed in power-line ducts or thinner cables – and also over glass optical fiber – much simpler optoelectronic connections or compatibility with RCLED and VCSEL based light emitters [2] –.

In fact, the reliability of a POF channel is demonstrated in already commercially available solutions for industries, the automotive sector [3] and low-cost home area networks (HANs) at speeds of up to 100 Mb/s over 50 m. As consumers demand more multimedia services requiring higher transmission speed for in-car and in-home networks, designers are challenged to develop improvements in optical channels and new receiver architectures [4].

In particular, this approach is very attractive for in-home networks [5] due to an overall ease of installation and maintenance, which can be carried out even by do-it-yourself installers. However, manipulation requires an eye-safety operation that limits the highest optical power given out by the laser depending on several factors, such as protective case, exposure time or numerical aperture [6]. Thus, the sensitivity of the receiver becomes a very stringent parameter due to several penalty sources, and therefore the design of the POF receiver targeting a sensitivity compatible with eye-safe laser power is a real challenge due to the limitations of standard POF.

To efficiently detect the light transmitted along a cost-effective SI-POF, the designed CMOS receiver must deal with a large-area photodiode, i.e., a high photodiode capacitance due to the large core diameter of such a fiber. In addition, this kind of fiber shows an inherent frequency limitation characterized by a bandwidth–distance product of 45 MHz · 100 m [7], not suitable for gigabit NRZ transmission without boosting the fiber bandwidth. To maximize the POF channel capacity, some research is addressed towards increasing the fiber bandwidth by using the more expensive graded index channels or exploring techniques such as frequency division modulation. Both alternatives are proposed for multi-gigabit transmission over POF [8]; however, they worsen the feasibility of a widespread use for in-home networks due to higher fabrication costs and a more complex signal processing, respectively.

Instead, this work proposes the use of electronic equalization to attain gigabit NRZ transmission over SI-POF. This approach has been integrated successfully in many applications, such as audio and television lines, and data transmission over copper wires. Equalizers can be classified according to signal processing (discrete-time and continuous-time) and hardware (analog and digital). Digital equalizers have proved the feasibility of enhancing the bandwidth of SI-POF [9]. In particular, decision feedback equalizers have been successfully implemented in a FPGA platform [10]. Alternatively, analog equalizers save power consumption and chip area since they avoid the power-hungry high-speed circuitry required by discrete-time (sample and hold circuit) and digital approaches (analog to digital converter). One of the first analog equalizers targeting gigabit speed for SI-POF was reported in [11]. Thus, the preferred POF receiver architecture

Manuscript received January 31, 2012. Revised May 9, 2012. This work has been partially supported by MICINN-FEDER (TEC2008-05455/TEC and TEC2011-23211).

F. Aznar, C. Sánchez-Azqueta, S. Celma, and B. Calvo are with Group of Electronic Design, University of Zaragoza, Pedro Cerbuna 12, 50009, Zaragoza, Spain (e-mail: faznar@unizar.es).

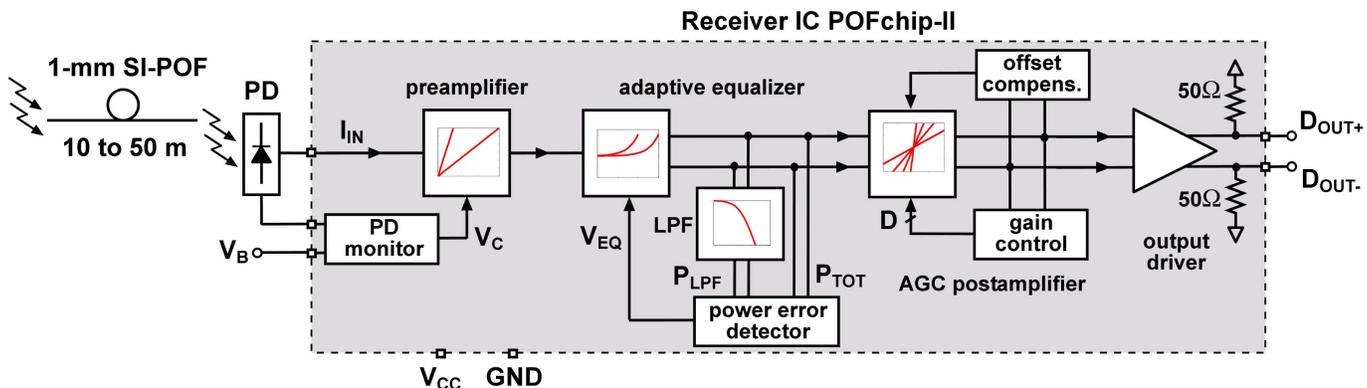


Fig. 1. Block diagram of the proposed CMOS receiver front-end and experimental setup including fiber and external commercial photodiode (PD).

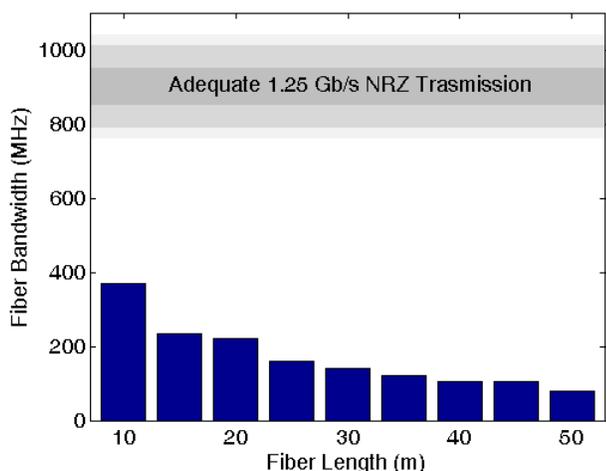


Fig. 2. Measured bandwidth at different lengths of SI-POF (Mitsubishi GH) with a laser diode (Sanyo DL-3147-021) compared to theoretical bandwidth range for adequate 1.25 Gb/s NRZ transmission.

includes an integrated analog continuous-time equalizer [4]. Furthermore, the equalizer should be adaptive to take into account variations due to temperature, aging or any other effect which may affect the channel response [7].

Following these motivations, a novel CMOS receiver front-end has been designed, fabricated and verified for short-range optical communications over 1-mm SI-POF channels. The paper is laid out as follows. Section II describes the design of the proposed receiver front-end. The most important experimental performances are summarized in Section III. Finally, main conclusions are drawn in Section IV.

## II. RECEIVER DESIGN

The proposed front-end architecture is illustrated in Fig. 1. It is formed by four building blocks: a variable-gain transimpedance preamplifier, a continuous-time adaptive equalizer, a postamplifier with automatic gain control and a 50- $\Omega$  output driver to perform experimental measurements.

The design of the first stage of the receiver, based on the common shunt-feedback architecture, is crucial to achieve good performances in sensitivity and speed as the noise generated in this block will be amplified in subsequent stages

and its input resistance must deal with a large photodiode capacitance. In addition, the overload input power, which defines the upper limit of dynamic range, has to be taken into account in the design stage. To optimize the noise performance, the preamplifier is implemented as a single-input single-output architecture, avoiding having to duplicate the noise sources to achieve a differential structure. The designed preamplifier, formed by a three-stage inverting amplifier and a shunt-feedback resistance, achieves a transimpedance of 59.6 dB $\Omega$  with a bandwidth of 1.1 GHz and a good noise performance, attaining a sensitivity of  $-18.3$  dBm characterized with a photodiode of  $C_{PD} = 3$  pF. The PD monitor biases the photodiode in the inverse region by means of the voltage  $V_B$  while generating the control voltage  $V_C$ , able to modify the preamplifier operation to properly process high input currents. Thus, the input dynamic range is increased, attaining an overload input power higher than 0 dBm thanks to a technique [12] based on input signal compression. Furthermore, a linear input-output response is obtained, preserving signal integrity.

As it has been previously mentioned, a channel using a cost-effective POF shows a limited bandwidth that, in addition, depends on the fiber length. The bandwidth has been measured for several lengths of the selected fiber following the method described in [13]. The obtained results are displayed in Fig. 2 along with the appropriate bandwidth range that achieves a good trade-off between ISI and noise for 1.25 Gb/s NRZ transmission [14]. Electronic equalization has been included to compensate the roll-off frequency caused by the POF, achieving a flat response for the combination of the channel and the equalizer over the bandwidth of interest for fiber lengths ranging from 10 to 50 m.

A continuous-time adaptive equalizer is selected, which exhibits good performances for low-power high-speed applications, and relaxes the complexity and sample-and-hold speed required by discrete time or purely digital approaches [15]. An adaptive equalizer in the receiver chain is mandatory to provide a wide range of POF lengths as well as to compensate other effects, such as temperature and aging, which may affect the channel response. The designed equalizer is based on a very simple topology, denoted the source

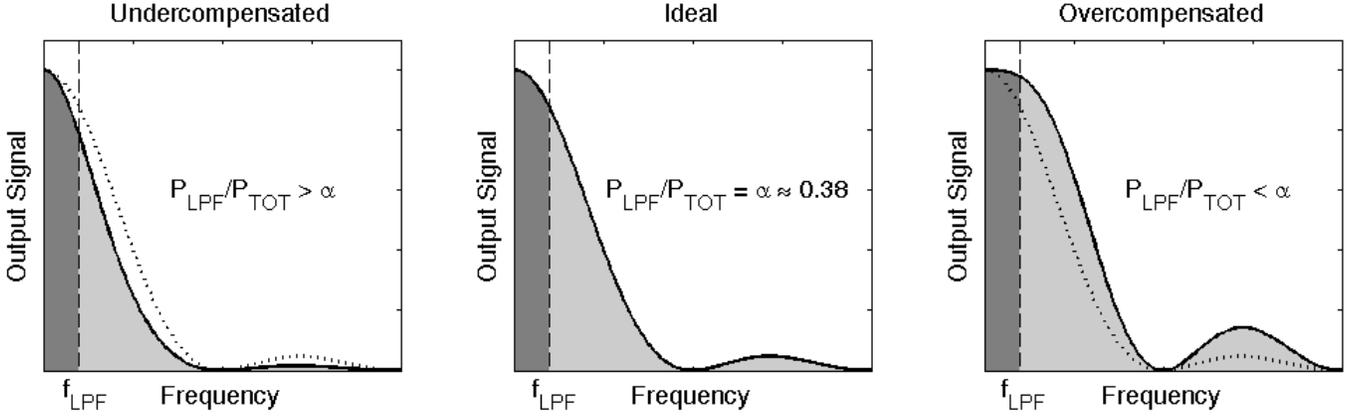


Fig. 3. Normalized power spectrum of the transmitted signal under different compensations caused by equalizer, indicating the low-pass to entire power ratio  $\alpha$  for a passive brick-wall filter with a  $f_{LPF}$  cut-off frequency equal to 0.2 times bit rate.

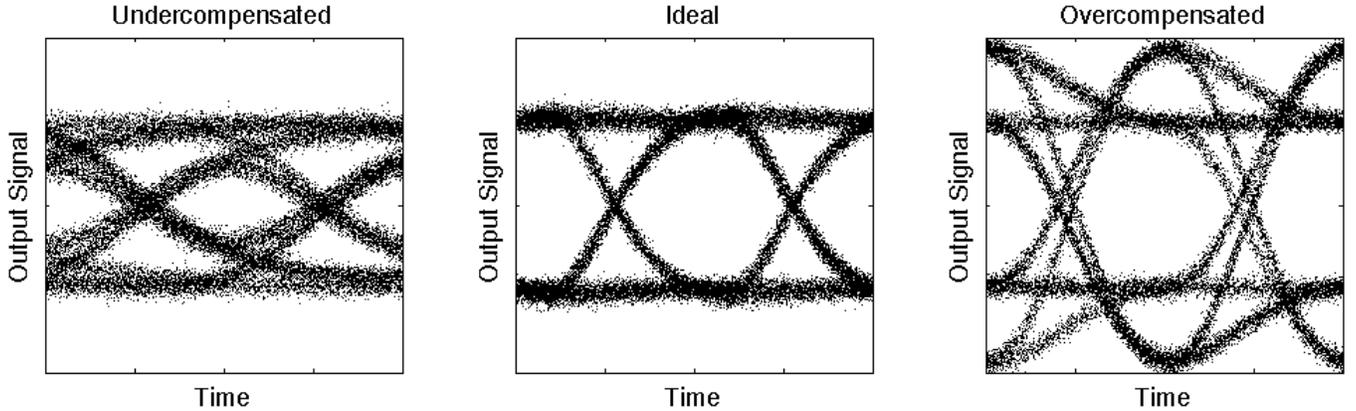


Fig. 4. Eye diagrams derived from different compensations caused by equalizer.

degenerated structure. Its main assignment is boosting the high-frequency component of the signal, which has been previously degraded by the POF channel. Different frequency compensations can be performed thanks to a varactor controlled by the voltage  $V_{EQ}$  generated by the adaptation loop. The frequency position of the zero can be adjusted from 125 to 385 MHz with a highest relative peaking of 10 dB, attaining an overall frequency response suitable for gigabit NRZ transmission. Finally, it converts the single signal from the preamplifier to a fully differential output signal, facilitating the subsequent amplification.

The adaptation loop is based on the spectrum-balancing technique [16]; illustrated in Fig. 3, it consists in comparing two different ranges of the spectrum. To do this, only a low-pass filter (LPF) is included, and the entire signal power  $P_{TOT}$  is compared with the filtered signal power  $P_{LPF}$ . Then, as the expected power spectrum of the desired transmitted signal is known and can be written as

$$P_{TOT}(f) = \text{sinc}^2(f) = \left( \frac{\sin(\pi f)}{\pi f} \right)^2 \quad (1)$$

where  $f$  is the frequency normalized to units of bit rate. The  $P_{LPF}/P_{TOT}$  ratio, denoted as  $\alpha$ , establishes whether the high-

frequency part is under- or over-compensated compared to the ideal spectrum. The eye diagrams corresponding to these situations are illustrated in Fig. 4. Thus, this decision mechanism avoids using the extremely high slew-rate and power-hungry comparator of the adaptive techniques based on time domain operation [17]. In addition, compared to approaches including two different filters [16], this implementation shows sufficient accuracy while saving power consumption. Finally, to facilitate the power spectrum comparison, the designed first-order active LPF provides, for adequate transmission, the same power as the entire signal, as the high-frequency power losses caused by filtering are compensated by the amplification of the low-frequency power spectrum. Therefore, the bandwidth  $BW$  and low-frequency gain  $G$  of the LPF are connected by

$$P_{TOT} = P_{LPF} \Rightarrow \int_0^{\infty} \text{sinc}^2(x) dx = \int_0^{\infty} \text{sinc}^2(x) \frac{G^2 \cdot BW^2}{x^2 + BW^2} dx \quad (2)$$

Under this restriction, the design of the power error detector is substantially facilitated, as a symmetrical architecture must be implemented. The power detector circuit is based on the

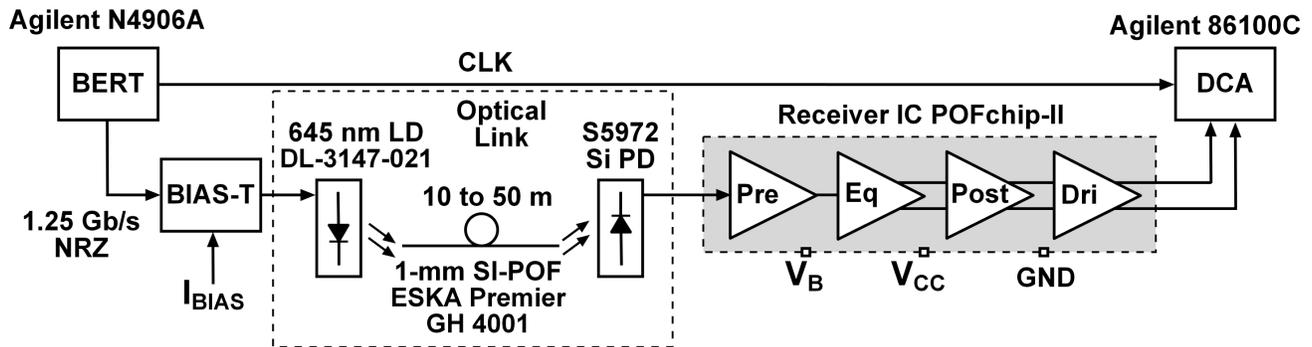


Fig. 5. Experimental setup.

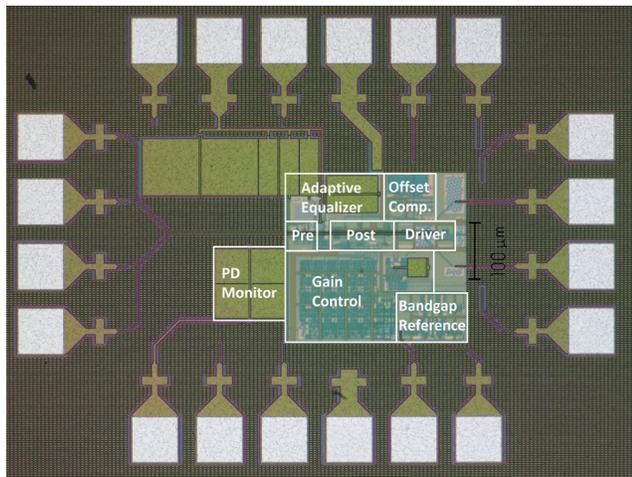


Fig. 6. Microphotograph of the receiver IC POFchip-II.

MOS coupled pair [18].

The main assignment of the postamplifier consists in boosting the signal for the decision circuit to properly discern between digital levels. Our proposal, detailed in [19], is formed by three cascaded gain stages that relax the stringent gain-bandwidth product requirement [14], a programmable gain controlled by the 6-bit digital word  $D$ , several broadband techniques such as inverse scaling, negative capacitances, inter-stage buffering and zero-pole cancellation to enhance the bandwidth of the postamplifier, and two feedback loops implementing automatic gain control and offset compensation that generate the digital word  $D$  and ensure the proper operation of this high-gain building block in spite of the typical input offset of CMOS devices.

Thus, the postamplifier works in the linear region within the entire input dynamic range of the preamplifier, amplifying the transmitted signal up to logical levels, while the noise from the postamplifier degrades the overall noise performance just slightly. Experimental verification of the stand-alone postamplifier demonstrates a linear-in-dB gain distribution from 33 to  $-3$  dB with 6 dB steps with a maximum gain error of 1 dB and a bandwidth superior to 2 GHz for all gain states, that is, it fulfills the requirements in terms of gain and bandwidth for 1.25 Gb/s transmission.

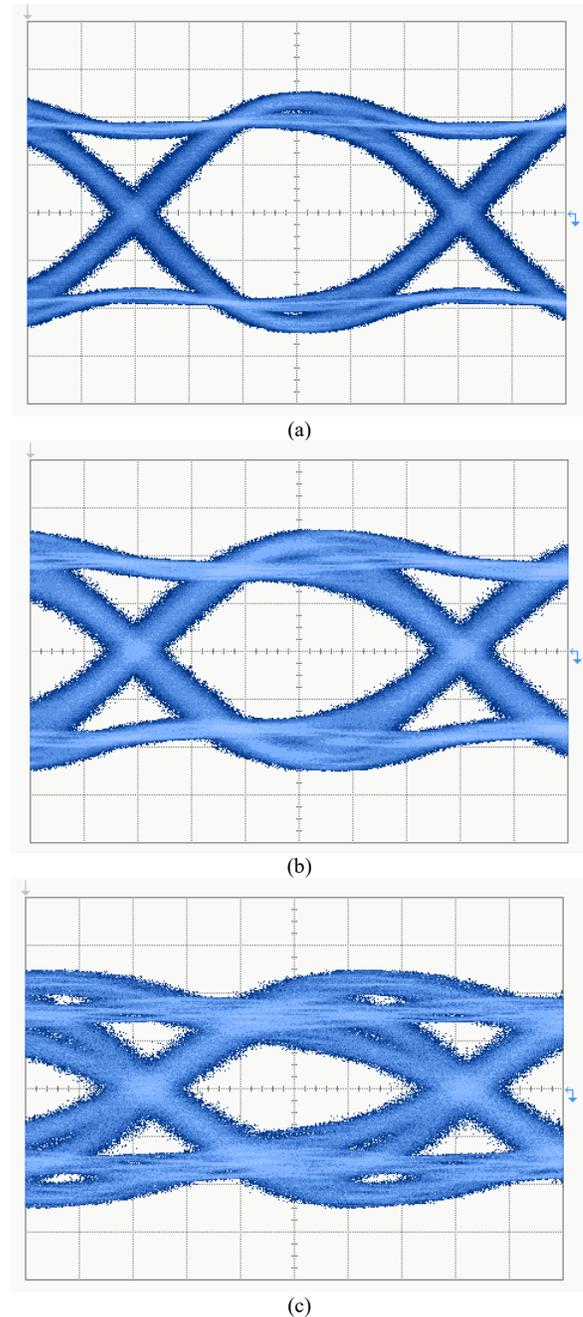


Fig. 7. Eye diagrams for 1.25 Gb/s NRZ PRBS  $2^{31}-1$  along (a) 10 m, (b) 30 m and (c) 50 m POF length for an optical input power of  $-16$ ,  $-15$  and  $-13$  dBm, respectively.

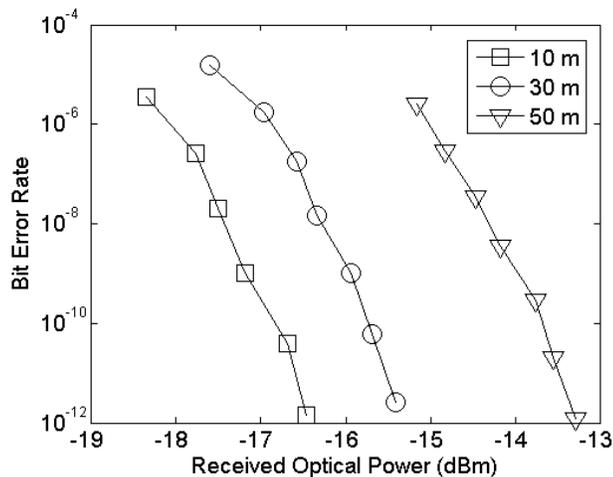


Fig. 8. Measured bit error ratio depending on input optical power.

### III. MEASUREMENT RESULTS

The optical receiver has been implemented in a standard 0.18- $\mu\text{m}$  CMOS technology. A first receiver IC prototype (POFchip-I) and its preliminary characterization were presented at ESSCIRC 2010 [20]. This paper details the optical setup and definitive experimental verification of an improved integrated circuit (POFchip-II) whose microphotograph is shown in Fig. 6.

Time-domain measurements were performed on-board for a bit rate of 1.25 Gb/s with an NRZ PRBS ( $2^{31}-1$ ) pattern. The optical devices involved were a Mitsubishi SI-POF (ESKA Premier GH 4001,  $\sim 0.17$  dB/m at 645 nm and NA = 0.5), a S5972 silicon PD from Hamamatsu (0.8 mm diameter, 0.44 A/W responsivity at 660 nm) and a red laser diode, model DL-3147-021 from Sanyo (645 nm lasing wavelength, 5 mW highest output power). The experimental setup, illustrated in Fig. 5, includes an Agilent 86100C digital communications analyzer (DCA) and an Agilent N4906A bit error ratio tester (BERT).

The eye diagrams obtained for three different fiber lengths (10, 30 and 50 m) are shown in Fig. 7. These measurements demonstrate the proper operation of the whole receiver and, in particular, the adequate compensation of the limited frequency response of the POF. From the plot of the measured bit error rate as a function of the input optical power, shown in Fig. 8, an error-free ( $\text{BER}=10^{-12}$ ) sensitivity of  $-16.4$ ,  $-15.3$  and  $-13.2$  dBm is attained for 10, 30 and 50-m POF lengths. The sensitivity is degraded due to the higher boosting of the preamplifier noise caused by the equalizer, as an increase of the POF length demands a higher boosting of the equalizer frequency response to compensate the roll-off frequency limitation of the POF. This, together with the length-dependent fiber losses, makes it necessary to increase the demanded laser output power for error-free transmission. The required laser output power is represented in Fig. 9, estimated from the measured sensitivity, fiber losses (0.17 dB/m) and penalties caused by fiber coupling (2 dB), receiver coupling (3 dB) and

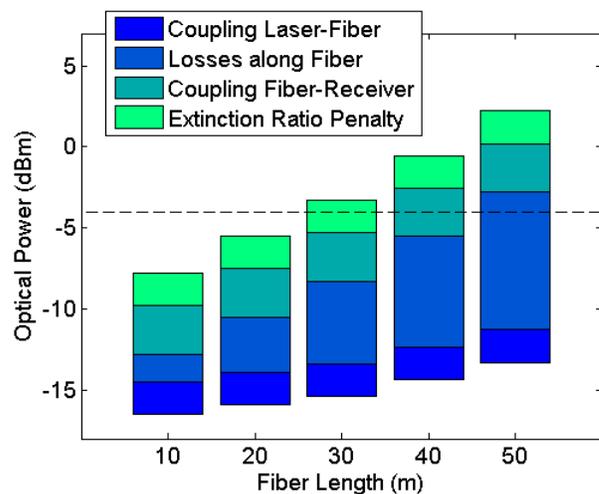


Fig. 9. Required laser output power, estimated by measured sensitivity and nominal penalty sources. Dashed line indicates the eye-safety power level.

extinction ratio (2 dB) [7, 21]. Eye-safe operation, considered as output power below  $-4$  dBm limited to class 1 lasers [6], is achieved up to almost 30-m length.

The main performances of this work are compared to previous publications in Table I. The proposed receiver is integrated in low-cost CMOS technology as a system-in-package (SiP) approach with an external photodiode, while [11] only implements the equalizer and [22] takes advantage of a superior 65 nm CMOS technology and optimized (graded-index) POF channel. Reference [23] includes an integrated CMOS photodiode; however, the extremely high photodiode capacitance leads to a limited bit rate below gigabit speed. The receiver front-end reported in [24] is designed under 1-V supply restriction to attain compatibility with shorter channel length CMOS technologies and to reduce the power consumption. Finally, reference [25] presents a front-end receiver implemented in BiCMOS technology. This proposal offers a single power supply of 3.3V and includes a 400- $\mu\text{m}$  diameter integrated photodiode.

Our experimental results show superior performances in terms of sensitivity compared to [22]-[24], attaining eye-safety operation with low-cost CMOS technology, whereas [11] does not report sensitivity; however, it also performs measurements with an optical output power not suitable for eye-safety. The sensitivity reported in [25] is 2.3 dB better than our proposal; however, a BiCMOS technology is more expensive and less compatible with a single-chip fully integrated low-cost solution, as the subsequent digital circuitry (CDR, DEMUX, etc.) is widely implemented in standard CMOS technology. Additionally, the fiber-receiver coupling is worse (6 dB) due to the smaller photodiode diameter, demanding higher output laser power.

### IV. CONCLUSIONS

The experimental verification of a CMOS approach integrated in standard 0.18- $\mu\text{m}$  technology for short-range optical transmission over 1-mm SI-POF is presented. The

TABLE I  
COMPARISON OF POF RECEIVER PERFORMANCES

Design	[11], 2009	[23], 2010	[22], 2011	[24], 2012	[25], 2012	This Work
Optical Channel	1-mm SI-POF	1-mm POF	GI-POF	1-mm SI-POF	1-mm SI-POF	1-mm SI-POF
Technology	0.35 $\mu\text{m}$ CMOS	0.18 $\mu\text{m}$ CMOS	65 nm CMOS	0.18 $\mu\text{m}$ CMOS	0.6 $\mu\text{m}$ BiCMOS	0.18 $\mu\text{m}$ CMOS
Wavelength	650 nm	660 nm	670 nm	645 nm	655 nm	645 nm
Bit Rate	1 Gb/s	0.4 Gb/s	3.125 Gb/s	1.25 Gb/s	1.25 Gb/s	1.25 Gb/s
PD Capacitance	4 pF	64 pF	14 pF	3 pF	–	3 pF
Error-Free Sensitivity	–	–13.6 dBm	–3.8 dBm	–8.2 dBm	–15.5 dBm	–13.2 dBm
POF Length	50 m	–	–	50 m	50 m	50 m
Power Dissipation	165 mW	39 mW	50 mW	23 mW	100 mW	108 mW

prototype achieves a 1.25-Gb/s speed up to 50-m reach thanks to an adaptive equalizer included in the receiver chain. Therefore, this approach is really attractive to implement gigabit transmission demanded by in-home networks. Compared to the state of the art, the proposed receiver offers a cost-effective solution compatible with the subsequent digital circuitry, as well as an improvement of the sensitivity that leads to a wide eye-safe reach. We are currently working on further improving the sensitivity of the receiver to provide full eye-safety operation.

#### ACKNOWLEDGMENT

The authors would like to thank Dr. Javier Mateo, member of Photonic Technologies Group (GTF) of I3A, for the characterization of the optical fiber and fruitful discussions.

#### REFERENCES

- [1] IEC 60793-2-40 International Standard. Edition 3.0, 2009.
- [2] P. Polishuk, "Plastic optical fiber branch out", *IEEE Communications Magazine*, vol. 44, no.9, pp. 140-148, Sept. 2006.
- [3] T. Kibler, S. Pofel, G. Böck, H.-P. Huber and E. Zeeb, "Optical data buses for automotive applications", *IEEE Journal of Lightwave Technology*, vol. 22, no.9, pp. 2184-2199, Sep. 2004.
- [4] F. Aznar, S. Celma and B. Calvo, *CMOS Receiver Front-ends for Gigabit Short-Range Optical Communications*, Springer, to be published.
- [5] A. M. J. Koonen *et al.*, "A look into the future of in-building networks: radmapping the fiber invasion," in *Proc. of 20<sup>th</sup> International Conference on Plastic Optical Fibers*, pp. 41-46, Sept. 2011.
- [6] IEC 60825-1 International Standard. Edition 2.0, 2007.
- [7] O. Ziemann, J. Kranser, P. E. Zamzow and W. Daum, *POF Handbook Optical Short Range Transmission Systems*, Springer, 2008.
- [8] D. Visani *et al.*, "Beyond 1 Gbit/s transmission over 1 mm diameter plastic optical fiber employing DMT for in-home communications systems", *IEEE Journal of Lightwave Technology*, vol. 29, no. 4, pp. 622-628, Feb. 2011.
- [9] M. Schüppert and C.-A. Bunge, "Feasibility Analysis of Decision Feedback Equalizers for Gbit/s POF Transmission due to Error Propagation" in *Proc. of 20<sup>th</sup> International Conference on Plastic Optical Fibers*, pp. 13-18, Sept. 2011.
- [10] A. Nespola *et al.*, "First Demonstration of Real-Time LED-based Gigabit Ethernet Transmission on 50m of A4a.2 SI-POF with Significant System Margin", in *Proc. of 36<sup>th</sup> European Conference and Exhibition on Optical Communication*, pp. 1-3, Sept. 2010.
- [11] J. Sundermeyer, C. Zerna and J. Tan, "Integrated analogue adaptive equalizer for gigabit transmission over standard step index plastic optical fibre (SI-POF)," in *Proc. of 22<sup>nd</sup> LEOS Annual Meeting Conference*, Dec. 2009.
- [12] F. Aznar, W. Gaberl and H. Zimmermann, "A 0.18  $\mu\text{m}$  CMOS transimpedance amplifier with 26 dB dynamic range at 2.5 Gb/s", *Microelectronics Journal*, vol. 42, no. 10, pp. 1136-1142, Oct. 2011.
- [13] J. Mateo, M.A. Losada, J. Zubia, "Frequency response in step index plastic optical fibers obtained from the generalized power flow equation", in *Optics Express*, vol. 17, no. 4, pp. 2850-2860, Feb. 2009.
- [14] E. Sackinger, *Broadband Circuits for Optical Fiber Communication*, John Wiley & Sons, 2005.
- [15] Liu J and Lin X, "Equalization in high-speed communication systems", *IEEE Circuits and Systems Magazine*, vol. 4 no. 2, pp. 4-17, Sept. 2004.
- [16] K-H. Cheng, Y-C. Tsai, Y-H. Wu and Y-F. Lin, "A 5-Gb/s inductorless CMOS adaptive equalizer for PCI express generation II applications", *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 57, no. 5, pp. 324- 328, May 2010.
- [17] J. N. Babanezhad, "A 3.3 V analog adaptive line-equalizer for fast ethernet data communication", in *Proc. of IEEE Custom Integrated Circuits Conference*, pp. 343-346, May 1998.
- [18] Y. Zhou and M. C. Y. Wah, "A wide band CMOS RF power detector," in *Proc. of the 2006 IEEE International Symposium on Circuits and Systems*, pp. 4228-4231, May 2006.
- [19] F. Aznar, S. Celma and B. Calvo, "A 0.18  $\mu\text{m}$  CMOS linear-in-dB AGC post-amplifier for optical communications", *Microelectronics Reliability*, vol. 51, no. 5, pp. 959-964, May 2011.
- [20] F. Aznar, S. Celma and B. Calvo, "A 0.18- $\mu\text{m}$  CMOS 1.25-Gbps front-end receiver for low-cost short reach optical communications," in *Proc. of European Solid State Circuits Conference*, pp. 554-557, Sept. 2010.
- [21] Y. Dong and K. Martin, "Gigabit Communications over Plastic Optical Fiber", *IEEE Solid-State Circuits Magazine*, vol. 3, no. 1, pp. 60-69, Jan. 2011.
- [22] Y. Dong and K. Martin, "A monolithic 3.125 Gbps fiber optic receiver front-end for POF applications in 65 nm CMOS" in *Proc. of IEEE Custom Integrated Circuits Conference*, pp. 1-4, Sept. 2011.
- [23] F. Tavernier and M. Steyaert, "A high-speed POF receiver with 1 mm integrated photodiode in 180 nm CMOS" in *Proc. of 36<sup>th</sup> European Conference and Exhibition of Optical Communications*, P2.04, Sept. 2010.
- [24] C. Gimeno, C. Aldea, S. Celma and F. Aznar, "A cost-effective 1.25-Gb/s CMOS receiver for 50-m large-core SI-POF links," *IEEE Photonics Technology Letters*, vol. 24, no.6, pp. 485-487, Mar. 2012.
- [25] M. Atef, R. Swoboda and H. Zimmermann, "1.25 Gbit/s Over 50 m Step-Index Plastic Optical Fiber Using a Fully Integrated Optical

Receiver With an Integrated Equalizer”, *IEEE Journal of Lightwave Technology*, vol. 30, no. 1, pp. 118-122, Jan. 2012.

**Francisco Aznar** was born in Zaragoza, Spain. He received the B.Sc. degree in 2006, the M.Sc. degree in 2007 and the Ph.D. degree in 2011, all in Physics from the University of Zaragoza, Spain. Currently, he is a member of the Group of Electronic Design (GDE-I3A) at the Aragon Institute for Engineering Research of the University of Zaragoza. His research interests include mixed analog-digital microelectronic circuit design, high-frequency signal processing, CMOS integrated optical receivers and optical fiber communications.

**Carlos Sánchez-Azqueta** was born in Zaragoza, Spain. He received the B.Sc. degree in 2006, the M.Sc. degree in 2010 and the Ph.D. degree in 2012, all in Physics from the University of Zaragoza, and the Dipl.-Ing. degree in 2009, in Electronic Engineering from the Complutense University of Madrid. He is currently a member of the Group of Electronic Design (GDE-I3A) at the Aragon Institute of Engineering Research of the University of Zaragoza. His research interests include mixed-signal integrated circuits and high-frequency communication circuits.

**Santiago Celma** was born in Zaragoza, Spain. He received the B.Sc. degree in 1987, the M.Sc. degree in 1989 and the Ph.D. degree in 1993, all in Physics from University of Zaragoza, Spain. Currently, he is a full professor of the Group of Electronic Design (GDE-I3A) at the Aragon Institute of Engineering Research of the University of Zaragoza. He has co-authored more than 80 technical papers and 270 international conference contributions. He is the holder of 4 patents. He appears as principal investigator in more than 25 Spanish and international research projects. His research interests include circuit theory, mixed-signal integrated circuits, high-frequency communication circuits and wireless sensor networks.

**Belén Calvo** received the B.Sc. degree in Physics and the Ph.D. degree in Electronic Engineering from the University of Zaragoza, Zaragoza, Spain, in 1999 and 2004, respectively. She is currently Senior researcher within the Group of Electronic Design, Aragon Institute of Engineering Research (GDE-I3A), University of Zaragoza. Her research interests include analog and mixed-mode CMOS IC design, on-chip programmable circuits, integrated optical receivers, low-voltage low-power monolithic sensor interfaces, and wireless sensor networks.