Cost-Effective 1.25-Gb/s CMOS Receiver for 50-m Large-Core SI-POF Links

Cecilia Gimeno, Concepción Aldea, Santiago Celma, *Member, IEEE*, and Francisco Aznar

***Abstract*— This letter proposes a new analog front end for short-reach high-speed optical communications that compensates the limited bandwidth of 1-mm step-index polymer optical fiber (SI-POF) transmission systems. In particular, the front end has been fabricated using a cost-effective digital 0.18-µm complementary metal–oxide–semiconductor (CMOS) technology and fed with only 1V. The prototype contains a transimpedance amplifier, a continuous-time equalizer, and an output driver. Experimentally, we have obtained 1.25 Gb/s transmission for a simple nonreturn-to-zero modulation in an optical link composed of 50 m of SI-POF and a large area Si PIN photodetector.**

***Index Terms*—Electronic equalization, home networking, low power, low voltage, step-index polymer optical fiber (SI-POF).**

I. Introduction

THE standard 1-mm core step-index plastic optical fiber (SI-POF) is already commercially used in industries, automotive sector [1], and as a low-cost home networking solution at speeds of up to 100 Mb/s over 50-m length. In fact, the goal set by some operators is to outperform the copper-based and all radio-based solutions in the future. As the need for higher data rates grows, more effort is being put into the development of high-speed POF solutions [2].

The motivation for using this kind of fiber for future gigabit home networking is explained in detail in [3]. Besides being cost competitive, it also offers several advantages over other transmission media, such as an overall ease of installation and maintenance due to its large diameter. However, the SI-POF exhibits high modal dispersion and hence an inherent frequency limitation (as low as 45 MHz · 100 m) quite inappropriate for gigabit communications [4].

Therefore, to achieve 1.25 Gb/s over this waveguide, equalization is mandatory to reduce intersymbol interference (ISI), which affects the bit error rate (BER) of the whole communication system. Moreover, as a typical POF diameter is close to 1 mm, the PIN photodiode (PD) required by the cost-effective viability should have a large active area for high-efficiency light coupling. However, it supposes a huge parasitic capacitance C_{PD}.

Manuscript received October 18, 2011; revised December 16, 2011; accepted December 21, 2011. This work has been partially supported by MICINN-FEDER (TEC2008-05455/TEC) and FPU fellowship program from the MCINN to C. Gimeno.

C. Gimeno, C. Aldea, S. Celma, and F. Aznar are with Group of Electronic Design, University of Zaragoza, Pedro Cerbuna 12, 50009, Zaragoza, Spain (e-mail: cegimeno@unizar.es).

For these very reasons, we have designed a new low-voltage low-power analog front end for short-reach high-speed optical communications in CMOS technology that compensates the limited bandwidth of POF channels. The paper is laid out as follows. Section II describes the main blocks of the proposed front-end. The most important experimental performances are summarized in Section III. Finally, main conclusions are drawn in Section IV.

II. The Proposed Front End

The proposed front end can be seen in Fig. 1. It consists of a high-speed low-voltage pseudodifferential transimpedance preamplifier (TIA), a continuous-time equalizer, and a 50-Ω output driver to perform experimental measurements.

The TIA receives current signal from a PD and converts it to voltage; its first stage provides a very low input impedance to achieve high-speed performance in combination with the large C_{PD} (up to 3 pF) and a three-stage voltage amplifier has been added to increase the gain-bandwidth product. Thus, it provides 3.2-Ω input resistance and 60-dBΩ transimpedance with a bandwidth of 1.3 GHz, which suffices for our application.

Ideally, the equalizer should provide the inverse frequency response of the channel to achieve a flat response of the channel-equalizer combination over the bandwidth of interest. Thus, we choose a continuous-time adaptive equalizer at the receiver, which exhibits a good power-speed tradeoff for these applications, requiring less complexity and area than discrete time or purely digital approaches that need clocks and high bandwidth sample-and-hold circuits working at several gigahertzs [5]. Hence, the equalizer consists of two parts: the line equalizer, which boosts the high-frequency component of the signal; and the adaptation loop, which provides an error signal to control the line equalizer.

The line equalizer provides a tunable zero, and a relative peaking up to 12 dB, to compensate for the roll-off frequency caused by the SI-POF and, as shown in Fig. 1, it is based in a split-path scheme where the output signal is the combination of a high-frequency boosting path and a gain path. Moreover, the proposed line equalizer can control the gain and the zero in a completely decoupled way. For more details of the electronic circuit itself, see [6].

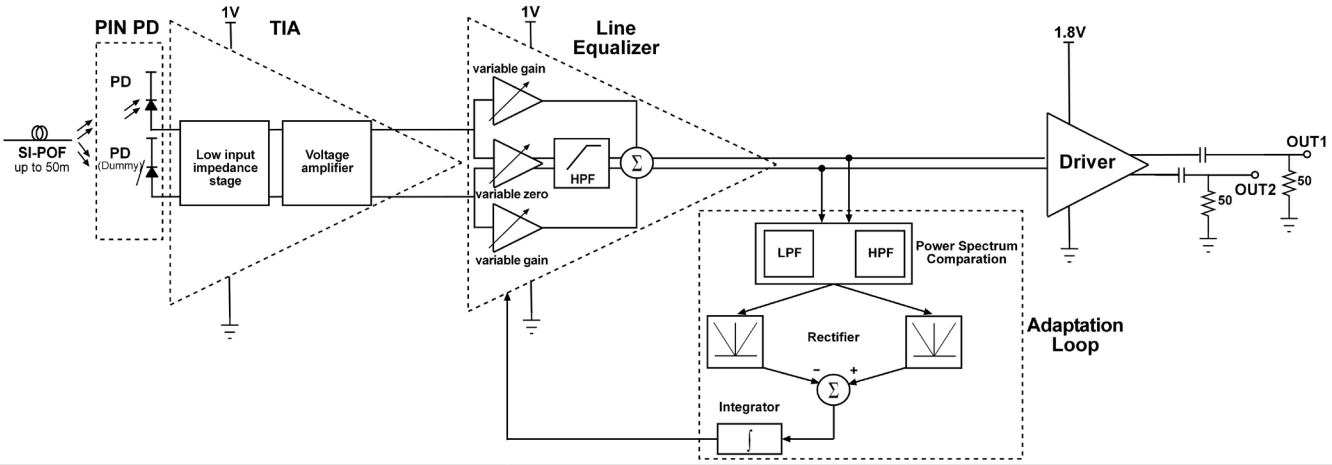

Fig. 1. Block diagram of the proposed front-end.

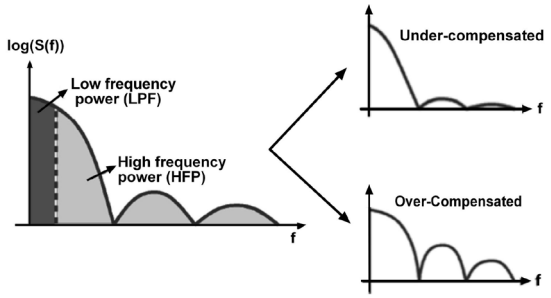

Fig. 2. Spectrum of an ideal random sequence and the effect of different compensations.

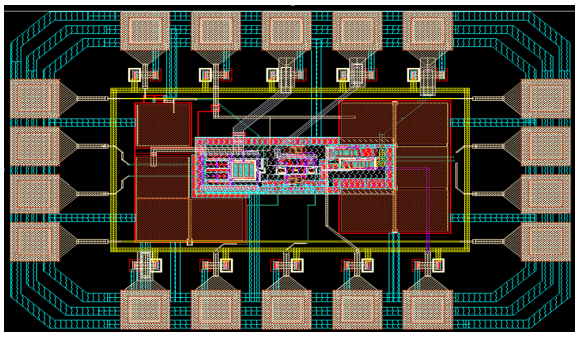

Fig. 3. Chip layout.

To implement the adaptation loop, we use the spectrum-balancing technique [7]. Unlike the adaptive techniques based in time domain operation, this decision mechanism obviates the need for a comparator which has high slew rate and is power-hungry [8]. As the ratio of the signal power within two different frequency ranges should be constant, the proposed adaptation loop, shown in Fig. 1, examines the power spectrum at the output of the equalizer, determines if the high-frequency part is under- or overcompensated, as shown in Fig. 2, and adjusts the boost accordingly. We use a low-pass filter and a high-pass filter to compare the power between the low- and the high-frequency portions of the signal.

A dummy PD has been used to subtract for the response of the illuminated PD the dark current. Thus, the signal is processed in a balanced way to minimize the noise from supply voltage and ground, and disturbance and coupling from

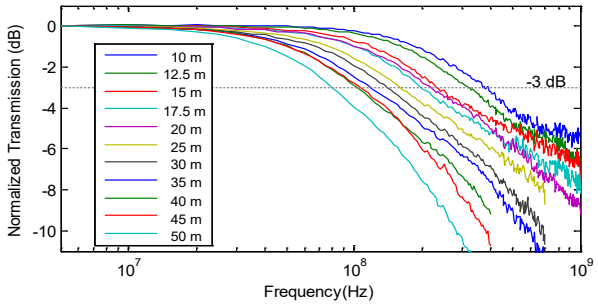

Fig. 4. Normalized frequency response of different lengths of SI-POF (Mitsubishi GH).

the layout. It also increases the signal-noise ratio and duplicates the maximum variation range of the signals.

Finally, note that the TIA and the equalizer have been fed with a supply voltage of only 1 V to search for the compatibility with the operation voltage of low-cost standard digital nano-CMOS technologies, which imposes to operate with 1 V in mixed analog-digital front ends. This has caused a real challenge in the design of the front end because most of the structures proposed so far in the literature lose their advantages when operated with such a low-voltage supply [9] or require the use of more advanced and, therefore, more expensive technologies [10].

III. Experimental Results

The prototype of the optical receiver front-end has been implemented in a digital 0.18-µm CMOS technology. The preamplifier-equalizer combination is fed with 1 V and the output driver with 1.8 V. The complete chip layout is shown in Fig. 3.

The circuit power consumption is 96.78 mW for 50-m POF where the TIA consumes 18.6 mW, the line equalizer 3.8 mW, and the output driver 74.34 mW. For 10-m POF, the power consumption of the line equalizer increases up to 4.16 mW.

The design is tested for 1.25 Gb/s with an NRZ PRBS (2^{31}-1) pattern. Experimental measurements include a Mitsubishi GH SI-POF, whose bandwidth depends greatly on the length as shown in Fig. 4, and the S5972 silicon PD from Hamamatsu (0.8 mm diameter, 0.44 A/W responsivity at 650 nm).

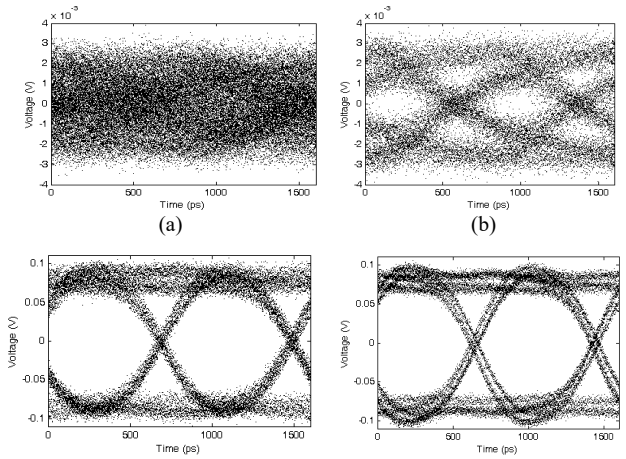

Fig. 5. Eye diagrams for 1.25 Gb/s NRZ PRBS 2^{31}-1: (a) 50m and (b) 10 m POF unequalized for an optical input power of -6 dBm; (c) 50m and (d) 10 m POF equalized for an optical input power of -7.5 dBm.

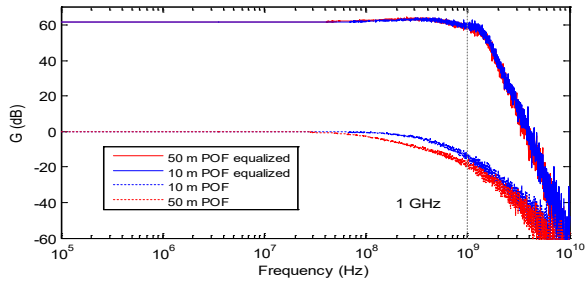

Fig. 6. Bandwidth improvement for 50 m (blue) and 10 m (red) POF.

In the following, we will call "unequalized" the normalized results including the POF and the PD loaded with the 50-Ω input resistor of the measurement equipment. As shown in Fig. 5 (a) and (b) for 50 m and 10 m, respectively, the unequalized eye diagrams are almost closed due to the limited bandwidth available (~ 100 MHz for 50-m and 300 MHz for 10-m POF).

We thus use the proposed front end. The obtained equalized eye diagrams are shown in Fig. 4 (c) and (d) for 50 m and 10 m POF, respectively; these results include the POF, the PD, and the proposed front end. Note that, as shown in Fig. 6, the bandwidth of the received signal can be enhanced from 100 MHz to 1.03 GHz and from 300 MHz to 1.25 GHz for 50-m and 10-m POF, respectively. This important result validates the effectiveness of the proposed architecture.

Furthermore, the proposed circuit shows a sufficiently high transimpedance of 62 dBΩ for the POF application. An error-free sensitivity of -8.2 dBm@BER=10^{-12} is achieved in the 50-m POF case and -10.2 dBm@BER=10^{-12} for 10-m POF, which is suitable for the most widely used communications standards.

To compare with other solutions, a possible figure-of-merit (*FOM*) would be the following:

$$FOM = \frac{Bit\ rate(Gb/s)\cdot Fiber\ length(m)\cdot\left|Sensitivity\ (dBm)\right|}{Power(mW)} \quad (1)$$

In this way, our proposed front end provides a *FOM* of 5.3, considering also the output driver. To the knowledge of the authors, there is not much in the literature to compare with. An analog equalizer proposed in [11] targets 1 Gb/s through 50-m SI-POF with a consumption of 165 mW (without taking into account the TIA) and assuming the same sensitivity (no available) providing a *FOM* of 2.7. Another analog front-end for a 3.125 Gb/s receiver [12] exhibits a *FOM* of 4.8 at the cost of a more expensive 65 nm CMOS technology and graded index POF. Therefore, our proposed front-end provides a good *FOM* owing to significantly lower power consumption (although we consider also the TIA and the driver) and similar results in terms of bit rate and fiber length.

IV. Conclusion

This paper shows a low-voltage high-frequency front end very effective in gigabit short-range transmission over 1-mm SI-POF, targeting 1.25 Gb/s through a 50-m Mitsubishi GH POF. It operates with a supply voltage of only 1 V, compatible with most modern nano-CMOS technologies, and consumes less than 22.8 mW excluding the output driver.

The high bandwidth of the front-end shows the feasibility of using this architecture in multigigabit application if the characteristics of the fiber or the modulation schemes are improved.

Acknowledgment

The authors would like to thank Dr. Javier Mateo for providing the experimental optical set-up used in this work.

References

[1] T. Freeman, "Plastic optical fibre tackles automotive requirements," in *Proc. FibreSyst. Eur./Lightw. Eur.*, 2004, pp. 14–16.

[2] A. M. J. Koonen, et.al, "A look into the future of in-building networks: radmapping the fiber invasion," in *Proc. 20th Intern. Conf. Plastic Optical Fibers (POF 2011)*, Bilbao, 2011, pp. 41-46.

[3] P. Polishuk, "Plastic optical fiber branch out", *IEEE Commun. Mag.*, vol. 44, no.9, pp. 140-148, Sep. 2006.

[4] *Part 2–40: Product Specifications – Sectional Specification for Category A4 Multimode Fibres*, IEC Standard 60793-2-40, 2009.

[5] Liu J and Lin X, "Equalization in high-speed communication systems", *IEEE Circuits and Systems Magazine*, vol. 4 no. 2, pp. 4-17, Sep. 2004.

[6] C. Gimeno, C. Aldea, S. Celma and F. Aznar, "High-speed CMOS front-end architecture for SI-POF," in *POF 2011 Conf. Proc.*, pp. 437-442, Sept. 2011.

[7] K-H. Cheng, Y-C. Tsai, Y-H. Wu and Y-F. Lin, "A 5-Gb/s inductorless CMOS adaptive equalizer for PCI express generation II applications", *IEEE Trans. Circuits and Systems-II: Express Briefs*, vol. 57, no. 5, pp. 324- 328, May 2010.

[8] J. N. Babanezhad, "A 3.3 V analog adaptive line-equalizer for fast ethernet data communication", in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1998, pp. 343-346.

[9] J.M. García del Pozo, S. Celma, M.T. Sanz and J.P. Alegre, "CMOS tunable TIA for 1.25 Gbit/s optical gigabit ethernet," *Electronics Letters*, vol. 43, no. 23 , pp. 1303-1305, Nov. 2007.

[10] F. Aznar, S. Celma and B. Calvo, "A 0.18-µm CMOS 1.25-Gbps front-end receiver for low-cost short reach optical communications," in *Proc. of ESSCIRC 2010*, pp. 554-557, Sept. 2010.

[11] J. Sundermeyer, C. Zerna and J. Tan, "Integrated analogue adaptive equalizer for gigabit transmission over standard step index plastic optical fibre (SI-POF)," in *Proc. of LEOS Ann. Meet. Conf.*, Dec. 2009, pp. 195–196.

[12] Y. Dong and K. Martin, "Monolithic 3.125 Gbps fiber optic receiver front-end for POF applications in 65 nm CMOS" in *Proc. of IEEE Custom Integ. Circ. Conf.*, Sep. 2011, pp. 1–4.