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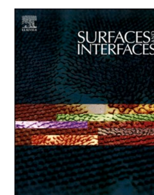

Electrical gating based on ion and electron beam irradiation of PdAc films: Application to superconducting nanowires

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ABSTRACT

Focused ion beam (FIB) is a nanopatterning technique commonly used for material removal, but in combination with a precursor material it gives rise to additive nanomanufacturing, of great interest in nanotechnology and semiconductor applications. The precursor material can be delivered onto the substrate either in the gas form, through a gas-injection system, or in thin-film form, through spin coating. Recently, it has been found that the electrical resistance of spin-coated PdAc organometallic films submitted to FIB irradiation can be metallic at an optimized ion dose, without the need of any post-processing purification step. On the other hand, if such PdAc films are submitted to low-dose focused electron beam irradiation (FEB), they become an insulating material. Here, we combine the use of FIB and FEB irradiation to produce (additively) micro- and nano-structured materials that act as gates in electronic devices. Three different gate configurations have been explored and applied to suppress superconductivity in metallic nanowires through electric-field effects, including lateral and top gating. This new fabrication technique for investigation of electrical gating effects at the micro- and nano-scales stands out by its precision and resolution (due to the use of focused charged beams), by the absence of sacrificial resist layers, and by the process speed.

1. Introduction

Due to the capability for tuning the amount of charge carriers and the intensity of applied electric fields, electrical gating is fundamental to the current technology of electronic devices as well as in fundamental aspects of surface and interface science. A good example of this technology is a metal-oxide-semiconductor field-effect transistor (MOSFET), in which an insulating/metallic bilayer on the active channel allows for carrier modulation leading to a high on/off electrical current ratio between drain and source [1]. Beyond well-established applications in silicon microelectronics and high-mobility semiconductor heterostructures [2], emergent technologies also rely on electrical gating. For example, carrier modulation through electrical gating is also observed in two-dimensional (2D) materials such as graphene, leading to the fine tuning of the Dirac point exhibiting the highest electrical resistance [3]. Also, it has been observed that, in the case of strongly-correlated materials such as VO_2 and Fe_3O_4, the low-temperature insulating state can be controlled by an external electrical field [4,5]. Interestingly, some materials show topotactic transformations by application of high electrical fields, which can be used for neuromorphic devices [6]. On the other hand, topological qubits based on high-mobility semiconducting nanowires also need dedicated gating electrodes to tune the topological state [7]. Moreover, the magnetic anisotropy in ultra-thin FePt and FePd magnetic films was found to be tuneable by application of an electric field [8]. In the field of superconductivity, it was shown that the tuning of the carrier concentration in ultrathin superconducting films can lead to significant changes in their superconducting state [9]. More surprisingly, recent work has shown a high degree of tunability of the superconducting properties of metallic nanowires [10], which could eventually lead to the creation of high-frequency superconducting transistors [11]. Whether this behaviour is intrinsic or extrinsic, however, remains under strong debate in the field [12–16]. All previous examples demonstrate that electrical gating is crucial in modern technology due to its broad range of applications, and exploring new fabrication routes to produce electrical gating is definitely worthwhile.

Regarding the existing technologies to achieve electrical gating, the

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most common one consists in the growth of an insulating/metallic bilayer by thin-film growth techniques. Thus, Al_2O_3 and HfO_2 are frequently used as the insulating layer due their high dielectric constant and homogeneous growth [17,18]. As for the metallic film, Au, Pd or Pt are frequently used. However, the disadvantage of this common fabrication approach is that, after the film growth, a lithography process is required to define the selected position of the gates. Lithography is generally a multi-step technique that involves resists and adds complexity and time to the fabrication process [19]. Besides, lithography should be performed in clean room environment and is not available everywhere. For that reason, a simpler technique for electrical gating that has been developed in the last years is ionic gating [20,21], where either an ionic liquid [22], a polymer electrolyte [23] or an ion gel [24] are placed on the sample of interest and the application of a voltage causes charge mobility and the generation of an overall electric field. Whereas this kind of approach is useful for proof-of-concept demonstrations, its implementation in highly-integrated microelectronic devices can be difficult. Similarly, overall bottom gating by application of a voltage through the substrate can be used only for niche applications [25]. Ferroelectric materials can be wisely used, too, to produce substantial electric fields [26]. However, the integration of ferroelectric materials with other functional materials is not straightforward and also calls for lithography processes in integrated devices.

Given the importance of electrical gating in existing technology and the few options available for their fabrication, this article explores the use of palladium acetate (PdAc) organometallic spin-coated films in combination with focused electron and ion beam techniques to achieve electrical gating in both lateral and top gating configurations. This new method leverages from our previous studies of the effects produced by focused electron and ion beams (FEB and FIB, respectively) on PdAc spin-coated films [27,28]. The procedure involves the spread of a PdAc solution onto Si/SiO_2 subtrates by spin coating, giving rise to a thin film that is subsequently irradiated by the focused charged-particle beam. The irradiation provokes the film decomposition and leaves a Pd-based planar structure with the Pd content depending on the type of irradiation and fluence applied. In such previous work, it was found that metallic structures can be grown through Ga-FIB irradiation due to the formation of Pd films with large Pd content [28], whereas non-conductive structures can be grown through FEB irradiation due to the formation of Pd films with low Pd content [27].

In order to apply the new gating technique to a practical application, we have chosen the fabrication of electrical gate contacts to superconducting metallic nanowires, which is currently a matter of intense research. In fact, our group has studied in the past this kind of devices [29], with the W-C superconducting nanowires being grown by means of Focused Ion Beam Induced Deposition (FIBID) and the gating contacts being fabricated by electron beam lithography and FIB milling. The devices studied in this contribution, which will be presented hereafter, are of three types, as illustrated in Fig. 1. Devices 1 and 2 are lateral-gating devices where the metallic gates are first created with a gap in the center, of size in the range of 600–700 nm, and the W-C nanowire is subsequently grown in the center. The difference between Devices 1 and 2 lies in their dielectric materials: Device 1 uses the vacuum, while Device 2 employs a low-Pd-content film that behaves as an insulating material. Device 3 corresponds to a top gate contact in which, firstly, an insulating layer is grown on the W-C nanowire through the electron irradiation of a PdAc thin film and, subsequently, the metallic top contact is fabricated through the Ga^+ irradiation of a second PdAc thin film. These gate contacts will serve to produce an intense electrical field with the aim of modifying the superconducting state of the W-C nanowires, as will be shown in the next sections.

2. Materials and methods

2.1. Spin coating of the PdAc films

The fabrication of each Pd-based layer involves the following steps: 1) Preparation of the solution containing the organometallic precursor, palladium (II) acetate trimer, $Pd_3(OAc)_6$, which was purchased from Alfa Aesar and used as received. A fresh 0.2 M solution of $Pd_3(OAc)_6$ in $CHCl_3$ (CromAR® HPLC) was prepared and subsequently filtered through a Nylon filter (pore 0.45 μm, 13 mm diameter). 2) A volume of 15 μL of the filtered solution was spread onto a freshly cleaned Si/SiO_2 substrate using a Delta+ 20T2 spin-coater from Süss Microtec. 3) The spin-coating process, including two sequential steps; (i) 10 s at 3000 rpm, as a solvent removal step and (ii) 40 s at 4000 rpm, where the solution was dynamically spread and homogeneously distributed upon the surface. The film thicknesses were measured in a profilometer (KLA-Tencor P-6, Milpitas, CA, USA) performing a scratch on the sample unveiling the Si/SiO_2 substrate, obtaining values in the 200 – 350 nm

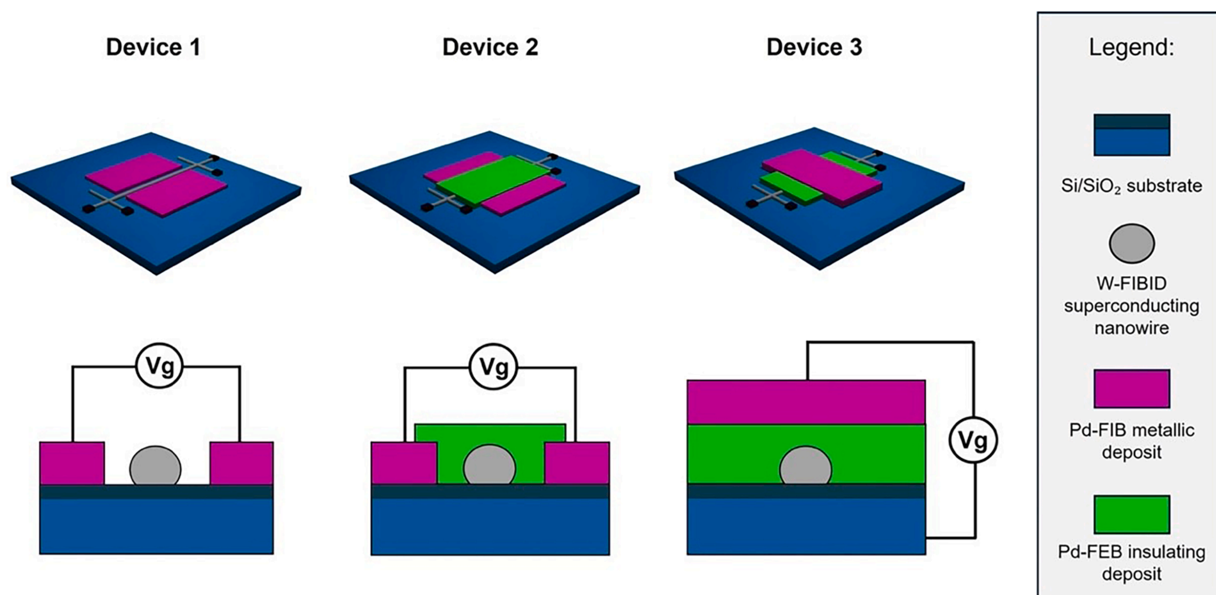

Fig. 1. Sketch with the three types of devices studied in order to produce an electric-field effect on superconducting nanowires. For each device, the top panel shows the top view and the bottom panel shows the side view.

range.

2.2. Irradiation of the PdAc films and washing step in $CHCl_3$

The organometallic films were irradiated by means of focused Ga^+ and electron beams using a Helios 650 Dual Beam FIB-SEM (Focused Ion Beam – Scanning Electron Microscope) instrument from Thermofisher/ FEI Company equipped with a 30 kV field-emission electron column and a 30 kV Ga^+column. FEB irradiation was used to obtain non-conductive layers, whereas FIB irradiation was used to obtain metallic layers. Unless other way stated, the FEB irradiation was performed with 5 kV voltage, 170 pA current, 1 μs dwell time, 50 % overlap and 1000 $\mu C/cm^2$ fluence, parameters that were previously optimized [27]. The FIB irradiation was performed with 30 kV voltage, 1.5 pA current, 200 ns dwell time, 0 % overlap and 20 $\mu C/cm^2$ fluence, parameters that were previously optimized [28]. After irradiation, samples were developed in $CHCl_3$ for 30 s to dissolve the unexposed areas, whilst the irradiated regions remained on the substrate.

2.3. Growth by FIBID of W-C superconducting nanowires and Pt-C metallic nanowires

The W-C superconducting nanowires were grown by FIBID using $W(CO)_6$ as the precursor material [30]. During growth, the nozzle used to deliver the precursor was positioned 50 μm away from the irradiation point in the vertical direction, and 100 μm away in the in-plane direction. As previously optimized in our group [29,31], we used the following growth parameters: 30 kV voltage, 1.5 pA, 500 μs dwell time, 0 % overlap and growth time corresponding to a volume per dose of 0.082 $\mu m^3/nC$. These parameters result in tungsten-based micro--structurally amorphous nanowires with an atomic composition of 55 % W, 25 % C, 11 % Ga, and 9 % O. In order to make electrical contacts from the W-C nanowire to the Cr/Au contact pads for subsequent electrical transport experiments, FIBID was applied using $(CH_3)_3(CpCH_3)Pt$ as the precursor material [32]. The following growth parameters were used: 30 kV voltage, 7.7 pA, 200 ns dwell time, 0 % overlap and growth time corresponding to a volume per dose of 0.5 $\mu m^3/nC$.

2.4. Transport experiments, including the application of a gate voltage

In order to perform electrical transport measurements, the devices are glued to a sample holder by means of G varnish and Al microwires are wire bonded (Kulicke and Soffa, model 4526) to connect to the electrical wires of a PPMS (Physical Properties Measurement System, by Quantum Design). This equipment uses a current/voltage source and allows decreasing the temperature down to 2 K and applying magnetic fields up to 9 T. In order to apply a gate voltage, an external voltage source is used.

2.5. Transmission electron microscopy characterization

Transmission electron microscopy (TEM) with high-angle annular dark-field (HAADF) imaging and energy-dispersive X-ray spectroscopy (EDS) compositional measurements were carried out in an analytical 300 kV Titan low-base instrument (Thermofisher/FEI Company). The HAADF images were obtained at 300 keV, and the energy resolution of the EDS experiments was ~125 eV using the scanning transmission electron microscopy (STEM) mode.

3. Results and discussions

In the following, four different devices will be discussed. Whereas in Device 1, only Ga-FIB irradiation is performed to create metallic structures very close to the superconducting nanowire for subsequent application of a high electric field laterally through the vacuum, in Device 2, the dielectric part will be grown by FEB irradiation. Devices 3A and 3B are more complex as the top gating implies the combination of both types of irradiations in order to create a metallic layer on top of an insulating one covering the superconducting nanowire. The difference between them is the thickness of the dielectric layer. The dielectric layer in Device 3A is thinner than in Device 3B because the FEB irradiation is carried out only once during the fabrication process of Device 3A, but twice for Device 3B.

3.1. Device 1

Device 1 has been designed and fabricated to produce the lateral gating on a superconducting nanowire, as shown in Fig. 2. In the first step, the gates are grown through the spin coating of the PdAc solution and FIB irradiation under the conditions reported in Section 2.2. Two large ($8 \times 7\ \mu m^2$) metallic rectangles remain after 7.5 s of FIB irradiation and the washing step, with a gap of 640 nm in between, where the W-C superconducting nanowire (85 nm in diameter) is subsequently grown by FIBID using the conditions reported in Section 2.3. The Pt-C connection leads are grown by FIBID in the last step to allow the magnetotransport characterization, with two current contacts (I^+, I^-), two voltage contacts (V^+, V^-), and two gate contacts (Vg^+, Vg^-).

As reported in Section 2.4, the device resistance is measured in a PPMS equipment as a function of temperature and gate voltage. The electrical resistivity at room temperature of this nanowire is estimated to be 240 μΩ·cm. This estimate takes into account the cross-sectional areas obtained in the rest of the nanowires measured in Devices 2, 3A and 3B, which take values from 2000 to 3300 nm^2. Fig. 3a indicates that the W-C nanowire becomes superconducting below $T_c = 4.1$ K (where the critical temperature is defined here as the temperature in which the resistance of the nanowire is 1 % of its normal-state resistance). At $T = 2$ K, a voltage difference up to 5 V is applied between the two gates in order to investigate if the electric field between the Pd-FIB gate pads is able to suppress the superconductivity in the nanowires, as previously reported when the gate pads are fabricated by electron beam lithography [29]. Fig. 3b indicates that this is the case, and the critical current (I_c) for the crossover from the superconducting to the normal state is found to decrease as a function of the applied gate voltage. I_c is a conventional value in a superconductor that represents the maximum current that can flow through it before it switches to the normal state, and its origin has been strongly debated in literature [33]. I_c is calculated as the value of the current that corresponds to the resistance of the nanowire that is 1 % of its normal-state value, which is a good criterium in the case of not applying external magnetic fields [34]. Whereas I_c is 8.2 μA without application of a gate voltage (V_g), this value decreases to 5.2 μA when V_g is 2.5 V, and the superconducting state is totally suppressed when V_g is 5 V, which corresponds to an absolute value of the electric field (E_g) of $7.8 \cdot 10^6$ V/m. These values are in the same range as the values for superconductivity suppression for a narrow 40-nm-wide W-C nanowire with gates patterned by EBL ($V_g = 3$ V and $E_g = 1.5 \cdot 10^7$ V/m) [29]. Voltage versus current curves under application of gate voltage in the range between 0 – 5 V are represented in Figure S1a in the Supplementary Materials. Summarizing, Pd-FIB gate pads offer a viable approach to create lateral gates on nanowires.

3.2. Device 2

Device 2 was conceived as an evolution with respect to Device 1 and involves an additional step to fill in the gap between the Pd-FIB side gate contacts. For that, once the gate contacts and the W-C nanowire are grown, a second PdAc thin film is spin coated and submitted to FEB irradiation. The FEB irradiation conditions are described in Section 2.2. After 2 s of FEB irradiation and the washing step, an insulating layer remains on the active part of the device. This layer serves the purpose of protecting the nanowire from ageing and oxidation. In addition, this layer can change the dielectric constant in the space between the gate contacts, which can modify the value of V_g required to suppress the

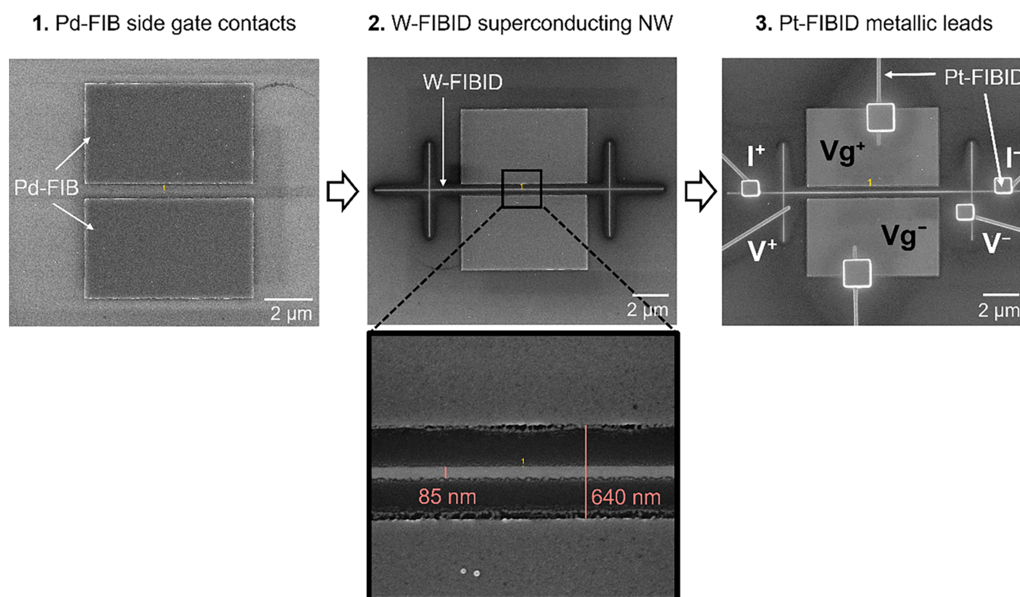

Fig. 2. SEM micrographs of the various steps leading to Device 1: growth of the Pd-FIB gate contacts, growth of the W-C nanowire by FIBID (with the zoom-in of the central part of the device) and growth of the Pt-C leads by FIBID.

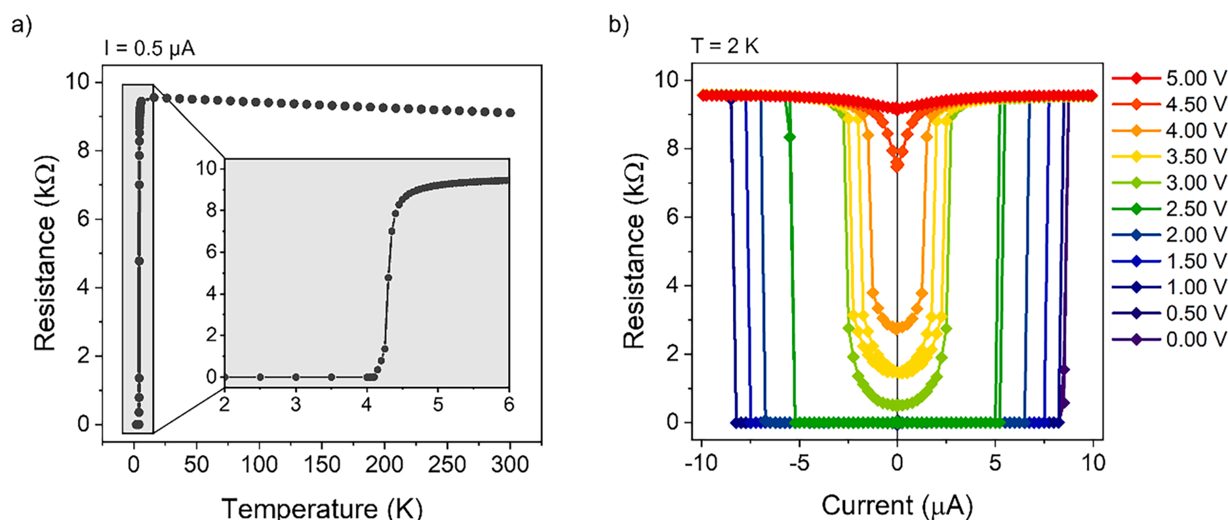

Fig. 3. a) Resistance versus temperature of Device 1 when applying a longitudinal current of 0.5 μA (the inset displays a zoom-in of the data below 6 K). **b)** Resistance versus current of Device 1 under application of gate voltage up to 5 V at 2 K.

superconducting state of the nanowire. The SEM micrographs shown in Fig. 4 indicate that the gap between the gate contacts (675 nm) and the nanowire diameter (71 nm) are similar to those in Device 1.

The electrical measurements on Device 2 are displayed in Fig. 5. The electrical resistivity at room temperature of this nanowire results in a value of 195 μΩ·cm, considering the cross-sectional area of the nanowire of 2000 nm^2 (determined after TEM characterization in Fig. 6). They show that the electrical resistance of the studied nanowire is similar to that in Device 1, but slightly higher given its smaller diameter (16 %). This nanowire displays T_c = 4.5 K, value slightly higher than the one displayed by the nanowire of Device 1, generally attributed to minor compositional differences. The I_c value at 2 K without applying any gate voltage is 5 μA. Such I_c value is lower than that of the nanowire in Device 1. This is expected due to its smaller diameter and therefore higher current density for the same applied current, because it is well known that the critical current density is the key parameter governing the crossover to the normal state [34]. On the other hand, it is worth mentioning that some physical effects such as self-heating can affect the transition to the normal state [35]. Interestingly, the value of V_g required in Device 2 to suppress the superconducting state of the nanowire is 3 V, which is lower than that for Device 1. This can be explained by the fact that in direct current mode, all materials have a dielectric constant (κ) larger than 1, which is the value in air/vacuum. Thus, it is tempting to propose that the value of κ in Pd-FEB, which is a composite material mainly formed out of amorphous carbon [31], will be around 1.6. This value is obtained taking into account that the dielectric constant is generally defined as $\kappa = E_0/E$, which is the ratio of the electric field in vacuum to that of the electric field in the corresponding dielectric material. Considering V = E·d, being V the gate voltage, and d the distance between the gate contacts, which is substantially the same in Device 1 (E_0) and Device 2 (E), we obtain κ ≈ V (Device1)/V(Device2) = 1.6. Voltage versus current curves under application of gate voltage in the range between 0 – 3 V are represented in Figure S1b in the Supplementary Materials. Nevertheless, this should be taken as a rough approximation, given the slight differences in the geometrical values and physical properties of both devices.

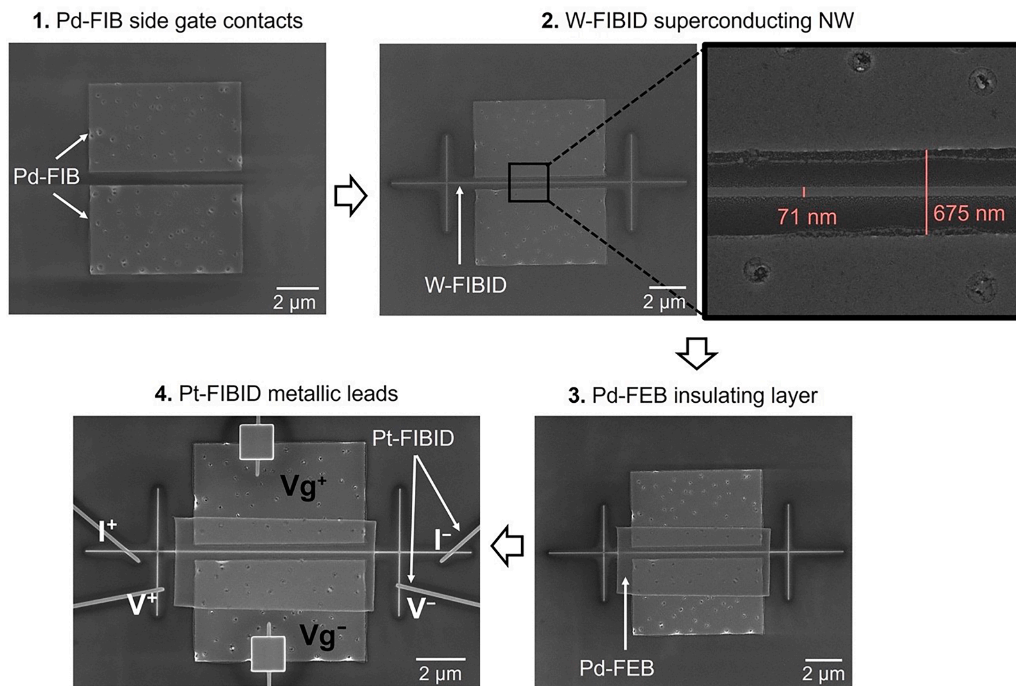

Fig. 4. SEM micrographs of the various steps leading to Device 2: growth of the Pd-FIB gate contacts (1), growth of the W-C nanowire by FIBID (with the zoom-in of the central part of the device) (2), growth of the Pd-FEB insulating layer (3), and growth of the Pt-C leads by FIBID (4).

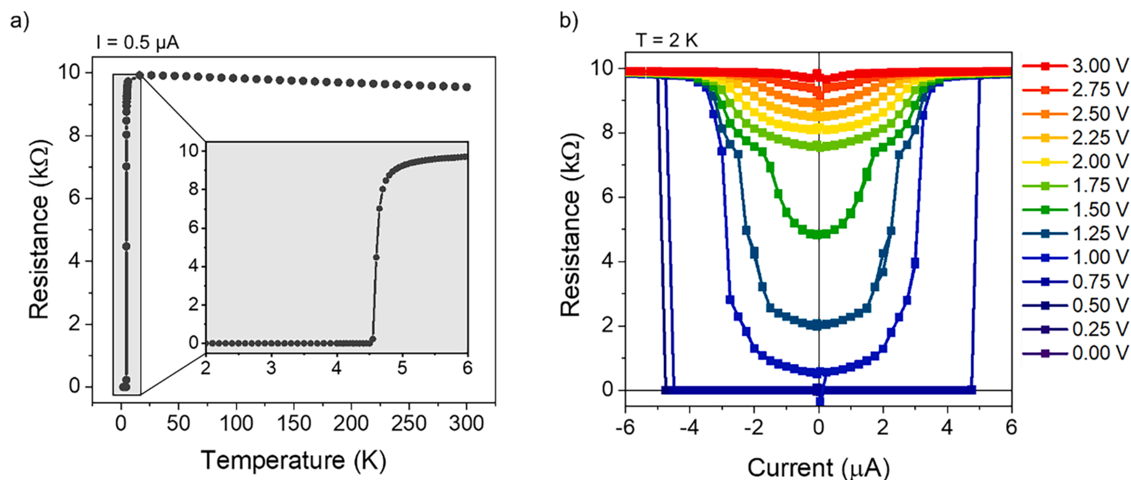

Fig. 5. a) Resistance versus temperature of Device 2 (the inset displays a zoom-in of the data below 6 K) when applying a longitudinal current of 0.5 µA. **b)** Resistance versus current of Device 2 under application of gate voltage up to 3 V at 2 K.

In order to verify that the geometry and composition of Device 2 correspond to the expected values, TEM experiments (details described in Section 2.5) were carried out on this device once the transport experiments had been concluded. The cross-sectional HAADF image displayed in Fig. 6 shows that the geometrical dimensions of the W-C nanowire and the Pd-FIB and Pd-FEB layers and their distance correspond well with the SEM micrographs shown in Fig. 4. A clear contrast is observed between the W-C nanowire, the Pd-FIB and the Pd-FEB layers in the HAADF image, as expected due to their different composition. The brightness of the different regions decreases in the following order: W-C nanowire, the Pd-FIB layer and the Pd-FEB layer, following the decrease of the average atomic number of the corresponding material. The composition of the Pd-FIB and Pd-FEB layers have been quantitatively analyzed through EDX in the areas marked with blue and red colour in Fig. 6. The obtained average Pd content (at. %) in the regions marked with numbers 1, 2, and 3 in the blue square is 14 %, as expected for a Pd-FEB layer obtained with low electron irradiation, which gives rise to a non-metallic material [27]. The obtained average Pd content in the regions marked with numbers 6 and 7 in the red square is 54 %, as expected for a Pd-FIB layer obtained with optimized ion irradiation, which gives rise to a metallic material [28]. The obtained average Pd content in the regions marked with numbers 4 and 5 in the red square is 35 %, but this value cannot be trusted due to the close proximity of the Pd-FIB layer (similar elements) and the unavoidable delocalization and electron beam broadening effects previously reported in this type of TEM experiments [36,37].

3.3. Device 3A

In this section, we discuss our efforts to apply this technique to the fabrication of top gates. Top gating is of great interest for tuning the carrier concentration of 2D electron gases [2] and MOSFET transistors

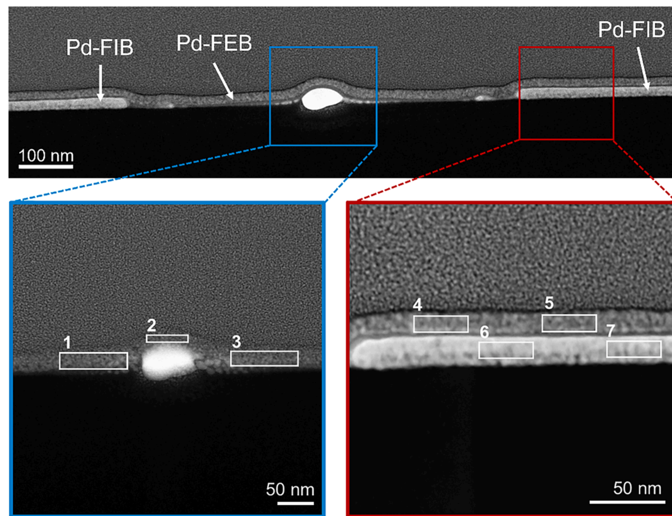

Fig. 6. HAADF-STEM images corresponding to the cross-sectional view of Device 2. Two areas of the device, those corresponding to the W-C nanowire (blue square) and to the Pd-FIB/Pd-FEB layers (red square), respectively, are zoomed in.

[1], and has enabled the miniaturization of microelectronic devices as predicted by Moore's Law [38]. Nowadays, cutting-edge lithography processes have led to FinFET devices with gating all around the conduction channel (in three dimensions) [39]. Nevertheless, top gating is in general very challenging because it is difficult to avoid short circuits between the gate and the conduction channel. Moreover, small leakage currents between the gate and the conduction channel can ruin the performance of the device. Having this in mind, we designed the following processing steps. First, the W-C nanowire is grown by FIBID. Secondly, the Pd-FEB insulating layer is fabricated using an irradiation time of 1.6 s, covering the central part of this nanowire. In the next step, the metallic Pd-FIB layer is produced with an irradiation time of 6.2 s. In the final step, Pt-C metallic contacts are grown by FIBID to allow the electrical measurements. In Fig. 7, SEM micrographs after all these steps are displayed.

In Fig. 8, the electrical results obtained for Device 3A are shown. The resistivity of this nanowire at room temperature has a value of 197 μΩ·cm, taking the cross-sectional area of the nanowire as ~ 1800 nm^2 (determined after TEM characterization in Fig. 9). At room temperature, we already noticed that the nanowire resistance decreased significantly when the gate voltage source was connected, even before any finite gate voltage was applied. This gave us evidence of the unsuccessful electrical insulation produced by the fabricated Pd-FEB layer, probably due to its insufficient thickness (20 nm) as TEM experiments showed. Fig. 8a shows the temperature dependence of the nanowire resistance without connecting the gate voltage source (V_{ext} off) and when the gate voltage source is connected but no finite gate voltage is applied (V_{ext} on). In both cases the superconducting transition is detected around the same temperature, but the normal resistance is lower with the gate voltage source connected. This indicates that a part of the electrical current applied between the nanowire source and drain contacts is diverted towards the gate contact due to the lack of appropriate electrical insulation of the Pd-FEB layer. In Fig. 8b, the measurements of the nanowire critical current at 2 K also give evidence for the same effect.

3.4. Device 3B

In order to circumvent the lack of electrical insulation of a single Pd-FEB layer observed in Device 3A, a new design was explored, in which two Pd-FEB layers are grown to increase the thickness of the insulation layer. SEM micrographs illustrating the fabrication steps to obtain Device 3B are displayed in Fig. 9.

The electrical measurements of Device 3B are shown in Fig. 10, which includes the temperature dependence of the resistance of the nanowire and the current dependence of the resistance of the nanowire at 2 K, without connecting the gate voltage source (V_{ext} off) and when the gate voltage source is connected but no finite gate voltage is applied (V_{ext} on). The electrical resistivity at room temperature of this nanowire

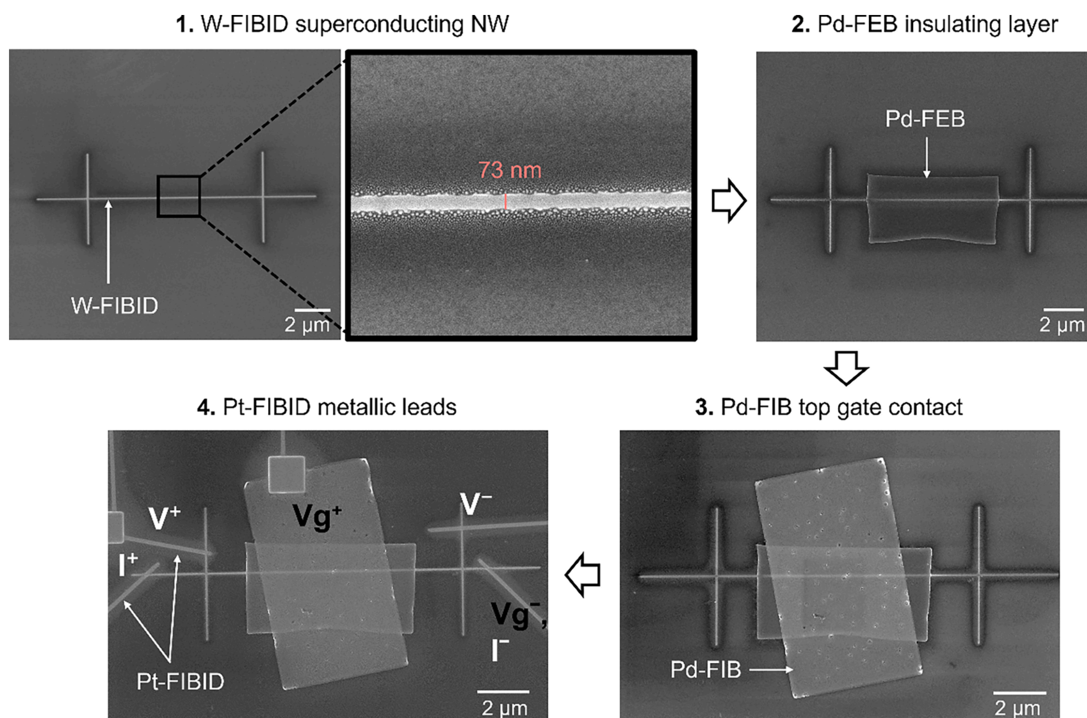

Fig. 7. SEM micrographs of the various steps leading to Device 3A: growth of the W-C nanowire by FIBID (with the zoom-in of the central part of the device) (1), growth of the Pd-FEB insulating layer (2), growth of the Pd-FIB top gate contact (3), and growth of the Pt-C leads by FIBID (4).

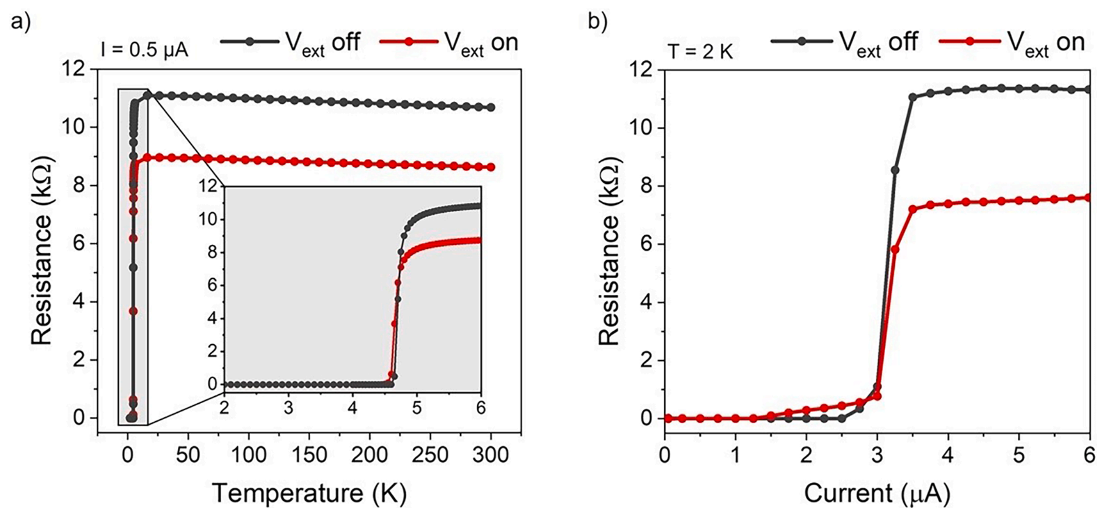

Fig. 8. For Device 3A, **a)** Temperature dependence of the W-C nanowire resistance without connecting the gate voltage source (V_{ext} off) and when the gate voltage source is connected but no finite gate voltage is applied (V_{ext} on) under the application of a longitudinal current of 0.5 μA. **b)** Measurement of the critical current at $T = 2$ K.

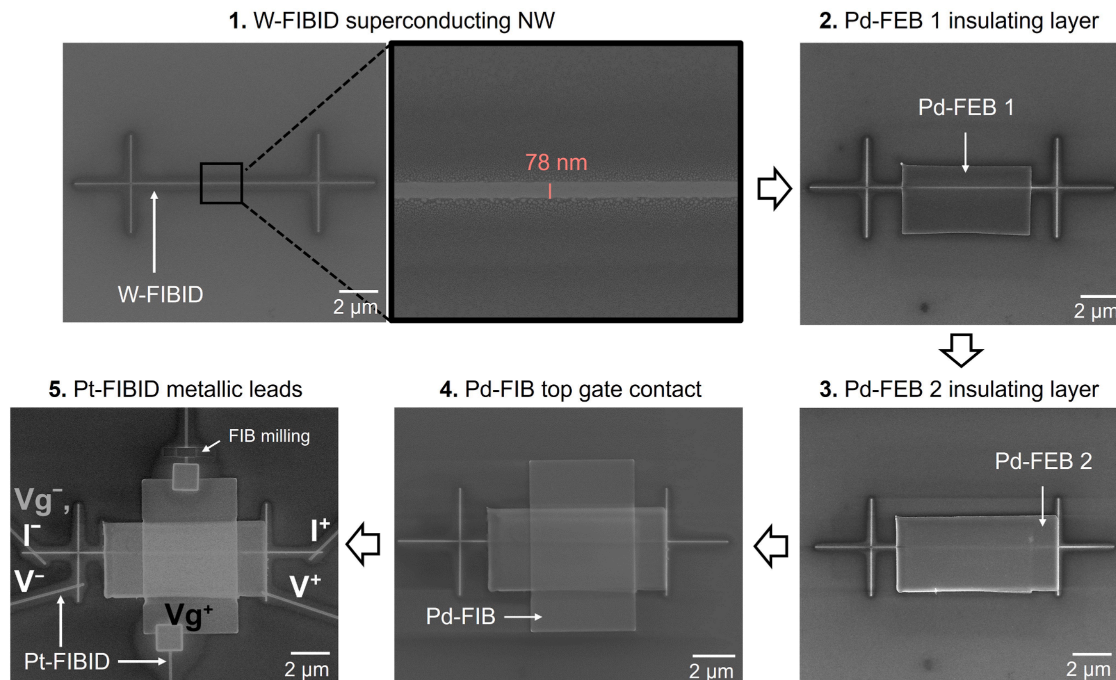

Fig. 9. SEM micrographs of the various steps leading to Device 3B: growth of the W-C nanowire by FIBID (with the zoom-in of the central part of the device) (1), growth of the first Pd-FEB insulating layer (2), growth of the second Pd-FEB insulating layer (3), growth of the Pd-FIB top gate contact (4), and growth of the Pt-C leads by FIBID (5).

results in a value of 288 μΩ·cm, after determining the cross-sectional area of ~ 3500 nm^2 in Fig. 12. In sharp contrast with the behaviour of Device 3A, the electrical properties are now much less affected when the gate voltage source is connected. As shown in Fig. 10a, below 50 K, the resistance coincides before and after connecting the gate voltage source. These measurements are performed using a low current of 0.5 μA. The measurements of the critical current at 2 K, displayed in Fig. 10b, indicate some difference in the normal-state resistance, which is a consequence of the higher current, around 6 μA. In fact, the curves begin to separate around 2 μA. We can draw the conclusion that at low applied current (0.5 μA) the use of two Pd-FEB layers works quite well for electrical insulation, but this is no longer the case at higher currents (> 2 μA).

Afterwards, the effect caused by the application of a finite top gate voltage was studied in Device 3B. In Fig. 11, the corresponding results obtained at 2 K are displayed. Remarkably, a strong top gating effect is measured, which indicates that, in first approximation, the double Pd-FEB layer is able to insulate adequately the W-C nanowire from the top metallic gate layer. Under 4.5 V, the superconducting state is suppressed, similarly to the gating effect under lateral configuration (Device 1 and 2). A closer inspection of the results in Fig. 11 indicates that some unwanted effects are observed, such as the asymmetry between the data under positive and negative applied current. This effect is not understood in detail, but it could arise from the asymmetry in the geometry of the device itself owing to a non-perfect alignment of the Pd-FEB layers, which could lead to inhomogeneous local gate voltages along the device.

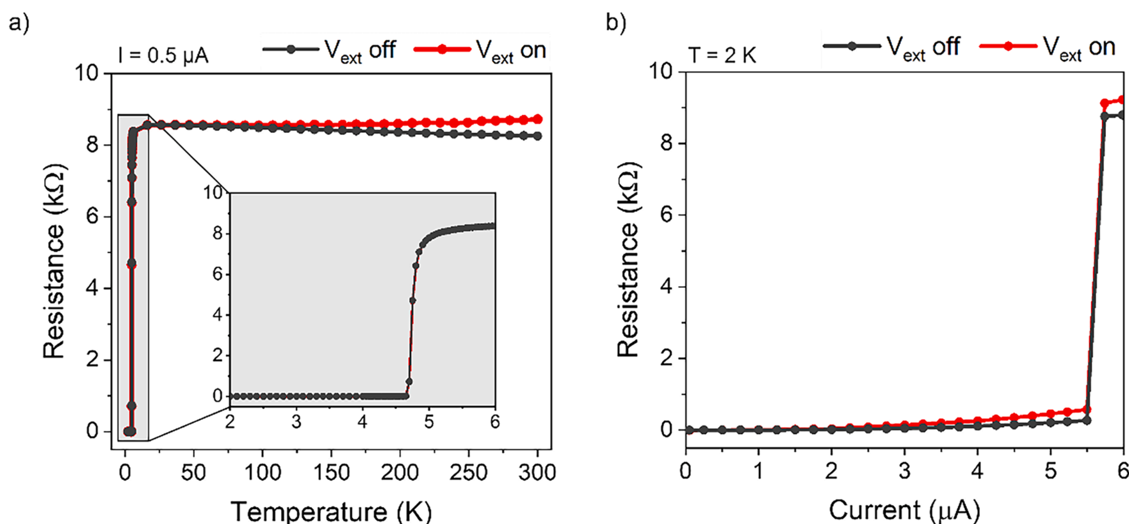

Fig. 10. For Device 3B, **a)** Temperature dependence of the W-C nanowire resistance without connecting the gate voltage source (V_{ext} off) and when the gate voltage source is connected but no finite gate voltage is applied (V_{ext} on) under the application of a longitudinal current of 0.5 μA. **b)** Measurement of the critical current at $T = 2$ K.

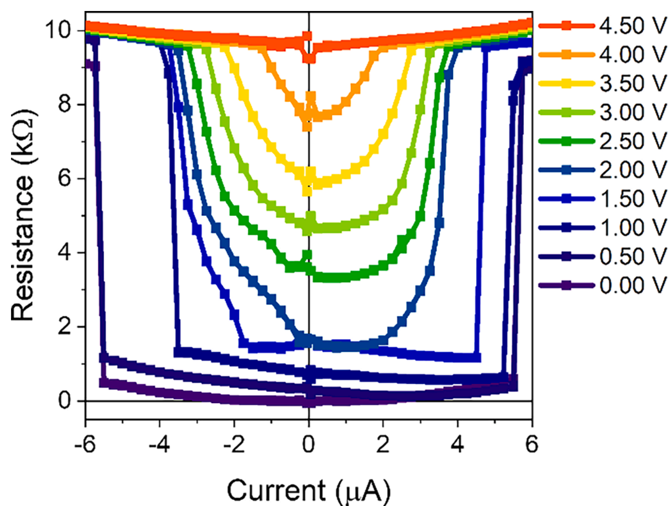

Fig. 11. Measurements in Device 3B, at $T = 2$ K, of the critical current under applied gate voltage up to 4.5 V.

Also, the existence of small leakage currents between the W-C nanowire and the gate contact should be considered, especially under application of electrical currents > 2 μA, as noticed in Fig. 10. Voltage versus current curves under application of gate voltage in the range between 0 – 4.5 V are represented in Figure S1c in the Supplementary Materials.

In order to characterize the thickness of the various layers grown on the W-C nanowire and their composition, HAADF-STEM experiments were conducted on Device 3B, as shown in Fig. 12a. The two Pd-FEB layers and the Pd-FIB layer are clearly distinguished above the W-C nanowire, with respective thicknesses of ~ 55 nm, 16 nm and 45 nm. Interestingly, the compositional analysis by EDX of the Pd-FEB layer in contact with the top surface of the W-C nanowire, shown in Fig. 12b, indicates that the % Pd atomic content is very low, 13.4 %, favouring its insulating behaviour. The Pd-FIB layer contains 36.1 % of Pd, as expected for a metallic structure. The intermediate layer, Pd-FEB 2, exhibits an intermediate Pd content.

The set of sucessful results obtained for Devices 1, 2 and 3B indicates that the use of PdAc thin films in combination with focused electron and ion beams allows the fabrication of gate contacts on nanowires in various configurations. A certain asymmetry with respect to the current direction noticed in Device 3B suggests that the fabrication of top gate contacts presents some room for further optimization. To achieve this, we propose to improve the symmetry of the device geometry, to increase the thickness of the Pd-FEB layer and increase its electrical resistance by the fabrication of a layer with a lower Pd content.

On the other hand, it is pertinent to discuss the implications of the obtained results with regard to the origin of the suppression of the superconductivity in W-C nanowires by application of a gate voltage. The results found in Device 1 and 2, which correspond to a lateral gate configuration, are in qualitative agreement with those previously found in similar devices with conventional EBL-fabricated gates [29]. If we calculate the critical electric fields that correspond to the critical voltage in Device 1 and 2 at 2 K, we obtain a value that is lower by a factor of 2 compared to the previous work, $1.5 \cdot 10^7$ V/m [29]. In the top gate configuration, the obtained critical field has a value 6 times larger compared to that value. Such significant difference points towards an extrinsic origin of the effect, maybe related with weak leakage currents that trigger the crossover to the normal state, as previously proposed [12]. It is thus suggested that the origin of the effect in these W-C devices is not intrinsically linked to a physical phenomenon with a well-defined critical electric field value, but rather connected with uncontrolled weak leakage currents that trigger the crossover to the normal state. Anyhow, further dedicated experiments focusing on the investigation of the origin of the effect could shed more light on this fundamental issue.

4. Conclusions

In conclusion, we report a new technique to manufacture electrical gates on nanowires. This technique, which is based on the use of spin-coated PdAc thin films and focused electron and ion irradiation, can be applied to create gates in lateral configuration and in top gate configuration, with high time efficiency. Some virtues of the proposed technique are the few steps required, the high resolution, the short irradiation times and the scalability. As a proof of concept to test the technique, we have chosen W-C superconducting nanowires, given that in this material the superconductivity can be suppressed by application of a gate voltage. Incidentally, the set of results obtained suggests an extrinsic origin of the phenomenon, possibly linked to small leakage currents between the nanowire and the gate contact. The new method discussed in this article stands out as a valuable approach in surface and interface science to fabricate electrical gate contacts on other materials and on devices with different geometries, extending beyond those

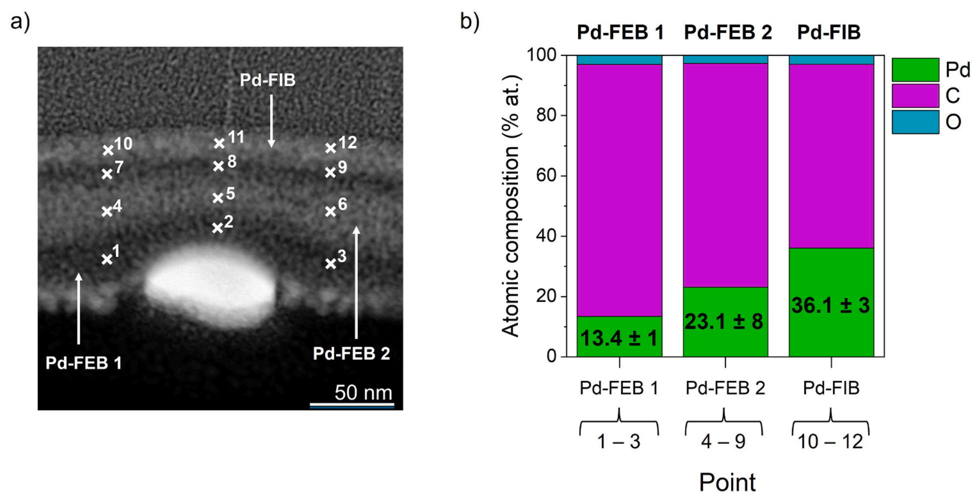

Fig. 12. In Device 3B, **a)** HAADF-STEM image of the W-C nanowire (brighter ellipsoid), covered by two Pd-FEB layers and one Pd-FIB layer. The numbers indicate the points where the EDX experiments have been performed. **b)** Average composition of various grouped points that correspond to the EDX experiments in the three Pd-based layers.

specifically investigated here. Given the few competing methods for electrical gating and their complexity, the use of spin-coated PdAc thin films in combination with focused electron and ion irradiation should be considered at the same foot as other methods for technological applications as well as for fundamental studies of transport properties governed by surface or interface charge carriers.

CRediT authorship contribution statement

Alba Salvador-Porroche: Writing – original draft, Validation, Methodology, Investigation. **Lucía Herrer:** Writing – review & editing, Validation, Methodology, Investigation. **Soraya Sangiao:** Writing – review & editing, Validation, Software, Methodology, Investigation, Funding acquisition. **Pilar Cea:** Writing – review & editing, Validation, Supervision, Methodology, Investigation, Funding acquisition. **José María De Teresa:** Writing – original draft, Validation, Supervision, Methodology, Investigation, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors have a patent pending of approval.

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Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.surfin.2024.105598.

Data availability

Data will be made available on request.

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