Behavioral Model for High-Speed SAR ADCs With On-Chip References

Carlos Dominguez-Matas, Antonio Gines, Aranzazu Otin, *Member, IEEE*, Valentín Gutiérrez, Gildas Leger, and Eduardo Peralias

***Abstract*— This article proposes a behavioral model, based on closed-form equations, of the dynamic errors in high-speed high-accuracy successive approximation register (SAR) analog-to-digital converters (ADCs) with charge-redistribution capacitor-based digital-to-analog converters (CDACs). To deal with incomplete settling of references and overcoming *LC* package parasitics, on-chip generation of the references must be considered in high-performance applications. This architecture, in combination with a bit-redundant conversion scheme, improves conversion speed while relaxing power consumption. The main challenge in this approach is that the reference settling and the resulting redundancy tolerance are signal-dependent, not only on the current error magnitude but also on the previous conversion cycle history and parasitics. This requires costly postlayout transistor-level simulations for performance evaluation (in the order of days), making not always feasible a systematic exploration of design space before integration due to computation time. To overcome this bottleneck, this work will show that the dynamic behavior can be theoretically predicted using a time-varying effective reference, the behavior of which is analytically described compactly. The accuracy of the proposed dynamic model is verified with a comparison with a 1.2-V 13-bit 65-nm SAR ADC characterized between 10 and 60 Msps at the postlayout level.**

***Index Terms*— Closed-form dynamic model, parasitics, redundancy analysis, reference settling, successive approximation register (SAR) analog-to-digital converters (ADCs).**

I. Introduction

OVER the last decade, successive approximation register (SAR)-type analog-to-digital converters (ADCs) have shown impressive figures of merit in medium-to-high-resolution and ultralow-power applications [1]. These improvements can be justified in the use of capacitor-based digital-to-analog converters (CDACs) and latch-type dynamic comparators, which take advantage of their digital architecture specially adapted to modern CMOS technologies.

In a conventional N-bit architecture with 1 bit per conversion, the SAR ADC uses M cycles ($M \geq N$) to digitize the analog input signal x, using the weighted sum of the obtained M bits, $\mathbf{D} = [D_1, \ldots, D_M]$. Hence, the final digital code z is evaluated through a simple arithmetic logic. However, the effective accuracy is determined by the nonidealities in the CDAC and the reference generator. Actually, in a high-speed high-resolution scenario, the settling behavior of the reference becomes one of the more limiting factors in performance. Although this issue is omitted in most of the research publications (just focusing on the ADC core), its importance has led to a growing interest in recent years, particularly in applications where the settling time associated with the package LC-resonance parasitics makes external voltage regulation no feasible [2], [3]. Although this problem can be partially mitigated using an internal buffer [4] or a huge on-chip decoupling capacitor [5], the tendency toward full on-chip integration of the references is increasing to optimize power and area consumption in SAR ADCs [6], [7], [8], [9].

On-chip reference generation is combined with CDAC redundancy to reduce power consumption and increase conversion speed [10], [11], [12], [13], [14]. This technique consists of the implementation of a binary search algorithm in which the number of cycles M is greater than the resolution of the converter N, so that if an error occurs in the first cycles, there is a margin for correction (against the case without redundancy with no margin). The redundant implementation is such that all errors within the i-th cycle, which are equivalent to a comparator decision error within the redundancy interval, can be compensated by the correction logic without interrupting the operation of the ADC. Despite the extra comparison cycles, the introduction of redundancy improves the conversion speed for a given resolution and reduces the power consumption by relaxing the settling requirements in the references and CDAC [10], [15].

Despite these advantages, several challenges arise in predicting the final impact on the SAR ADC performance since both the reference settling and the sizes of the redundant intervals become signal-dependent and sensitive to the history due to the transient evolution of the previous SAR cycles and layout parasitics. Moreover, the tolerable error for a single conversion results also scaled from cycle to cycle, from the most significant bit (MSB) with $i = 1$

Manuscript received 19 July 2023; revised 5 September 2023; accepted 6 September 2023. Date of publication 10 October 2023; date of current version 28 November 2023. This work was supported by the Spanish Government project RTI2018-098513-B-I00, cofinanced by the European FEDER (Fondo Europeo de Desarrollo Regional) program. *(Corresponding author: Antonio Gines.)*

Carlos Dominguez-Matas, Antonio Gines, Valentín Gutiérrez, Gildas Leger, and Eduardo Peralias are with the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Universidad de Sevilla, CSIC, 41092 Seville, Spain (e-mail: cmanuel@imse-cnm.csic.es; gines@imse-cnm.csic.es; valentin@imse-cnm.csic.es; leger@imse-cnm.csic.es; peralias@imse-cnm.csic.es).

Aranzazu Otin is with the Instituto Universitario de Investigación en Ingeniería de Aragón (I3A), Universidad de Zaragoza, 50018 Zaragoza, Spain (e-mail: aranotin@unizar.es).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TVLSI.2023.3314067.

Digital Object Identifier 10.1109/TVLSI.2023.3314067

to the least significant bit (LSB) with $i = M$, increasing the complexity of the problem. This issue is typically addressed by costly postlayout simulations at the transistor level since a theoretical analysis of the dynamic implications of references and redundancy is missing in the SAR bibliography [16], [17], [18], [19], [20], [21], [22], [23], [24].

Most of the works on SAR ADC modeling, such as [16], [17], and [18], assume static conditions in which only the impact of the CDAC parasitics and capacitor mismatch on performance is considered. In [19], [20], and [21], the nonideal settling due to switches is incorporated with a first-order RC model, but the reference generator is considered ideal. Even with the inclusion of more sophisticated descriptions, the issue of redundancy in SAR ADCs is not specifically addressed [22], [23], [24]. In this sense, the work in [22] introduces the nonideal effect of switches, charge injection, and feed-through in conventional SAR ADCs, but without any analysis of the implications on the conversion speed and still not covering the reference settling. In [23], the reference effects are incorporated using Thevenin's equivalent of the generator and analyzing the effect of switch resistances on the resulting CDAC dominant pole. Closed-form equations and useful guidelines for the design are then derived, but without any development on predicting the effective number of bits (ENOB) or accounting for history impact (from cycle to cycle) on the reference transients and redundancy tolerance. Although the reference behavior can be incorporated following the simulation strategy based on the matrix exponential in [24], this article just focuses on reducing numerical computation time.

To deal with signal-dependent dynamic effects in high-speed high-accuracy SAR ADCs, a novel analytical description is presented in this work. The developed model is based on closed-form equations in the time domain, which capture the incomplete settling behavior due to the reference generator, parasitic contributions of the switches (resistive, capacitive, and charge injection), as well as detrimental comparator effects (capacitive parasitics and kick-back noise). As a case study, the tradeoff between accuracy and speed is analyzed in a 1.2-V 13-bit 65-nm SAR ADC prototype operating between 10 Ms/s and 60 Ms/s sampling frequencies, showing a good agreement between the model performance predictions and the postlayout simulations. To the best of the authors' knowledge, this is the first time that such a reliable comparison in terms of ENOB (with an explicit analysis of signal-dependent errors in reference and redundancy intervals) has been achieved.

This article is organized as follows. Section II introduces the key concepts in high-speed high-accuracy SAR ADCs and the considered formulation. Section III presents the proposed dynamic model based on time-domain closed-form expressions. In Section IV, transistor-level effects associated with the real implementation of switches, comparators, and the reference generator, including postlayout parasitics, are incorporated. We continue in Section V with the model validation compared to the postlayout simulations. Finally, the discussion, conclusions, as well as two appendixes with additional details close this article.

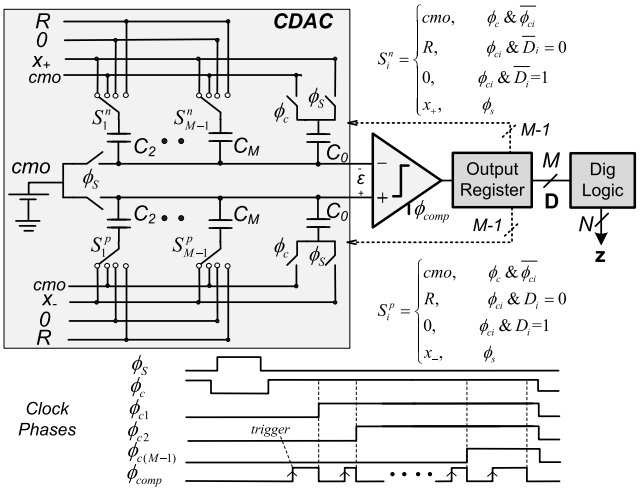

Fig. 1. Fully differential implementation of an asynchronous IMCS SAR ADC. Phase ϕ_s is the sampling phase, and ϕ_{ci} are the conversion phases.

II. SAR ADCs With Charge-Redistribution CDACs

Fig. 1 shows a simplified block diagram of a fully differential SAR ADC with charge-redistribution CDAC. For illustration purposes, the asynchronous inverted merged capacitor (IMCS) topology is presented [25], but the results herein derived can be applied without lack of generality to most bottom-sampling architectures in high-accuracy applications [23], considering both synchronous/asynchronous timing with or without redundancy. The circuit comprises the CDAC itself, a voltage comparator, and an output register that feeds the conversion bits back to the CDAC and stores the M-bit digital output $\mathbf{D}$ at the end of the conversion operation. The CDAC has M capacitors, C_i, and an extra branch C_0 to control the full-scale (FS) range, $[-R, +R]$, being R the ideal reference. The differential analog input, $x = x_+ - x_-$, is sampled on the conversion start at the end of phase ϕ_s. The sampled voltage is then shifted to the input of the comparator (ε) with phase ϕ_c.

In conventional SAR ADCs, the comparator outputs D_i control the voltage at the different capacitors C_i, from the MSB to the LSB. However, in a differential implementation, the first capacitor C_1 can be omitted since the sign of the injected signal produces directly the MSB, D_1. According to this scheme, the signal D_i controls the set voltage at the capacitors C_{i+1} depending on the comparator decision. At the end of the $M - 1$ cycles, the CDAC provides an estimation of the input that should be less than the ADC N-bit LSB, i.e., $|\varepsilon_M| \leq \text{LSB} \equiv 2R/2^N$. Notice that the last comparator bit D_M is not fed back to the CDAC, and hence, its conversion residue ε_{M+1} is not physically generated but virtually considered.

In static conditions, the amplitude of the conversion residue available at the comparator inputs can be related to the output code D_i in each conversion phase as follows:

$$\underset{(i\leq M)}{\varepsilon_i} = x - \sum_{k=1}^{i-1} \frac{(2D_k - 1)C_{k+1}}{C_t} \cdot R \quad \text{and} \quad D_i = \begin{cases} 1, & \varepsilon_i \geq 0 \\ 0, & \varepsilon_i < 0 \end{cases} \tag{1}$$

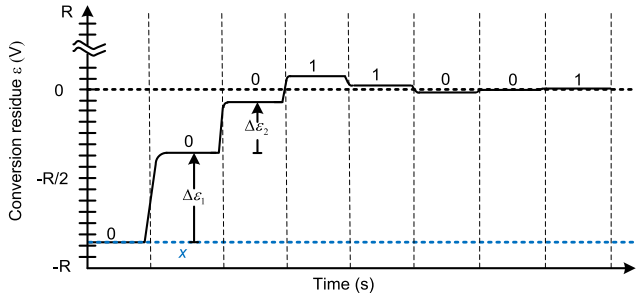

Fig. 2. Transient evolution of the CDAC output residue with details of the updating steps in the two MSB cycles.

where C_t is the total sampling capacitance expressed as the integer scale factors p_i and the unitary capacitance C as

$$C_t = C_0 + \sum_{i=2}^{M} C_i = C \cdot \left(p_0 + \sum_{i=2}^{M} p_i \right) \quad \text{with} \quad C_i = p_i C. \tag{2}$$

The value of the last virtual residue, ε_{M+1}, must be the following to be the ideal quantization error at the N-bit level:

$$|\varepsilon_{M+1}| \leq \text{LSB}/2 \rightarrow \varepsilon_{M+1} = \varepsilon_M - (2D_M - 1) \cdot \text{LSB}/2. \tag{3}$$

Based on the previous equations, the relationship between the updating step $\Delta\varepsilon_i$ and the capacitor scale factors p_i can be derived. This magnitude defines, as shown in Fig. 2, the amount of change in the CDAC between two consecutive cycles according to the comparator decision. Considering (1), it follows:

$$\underset{(i<M)}{\Delta\varepsilon_i} = \varepsilon_{i+1} - \varepsilon_i = \frac{(1-2D_i)p_{i+1}R}{p_0 + \sum_{k=2}^{M} p_k} = \begin{cases} +p_{i+1} \cdot \text{LSB}, & \text{if } D_i = 0 \\ -p_{i+1} \cdot \text{LSB}, & \text{if } D_i = 1 \end{cases} \tag{4}$$

while, according to (3), the virtual last step becomes

$$\Delta\varepsilon_M = \varepsilon_{M+1} - \varepsilon_M = \begin{cases} +\text{LSB}/2, & \text{if } D_i = 0 \\ -\text{LSB}/2, & \text{if } D_i = 1. \end{cases} \tag{5}$$

Using the M-th value of (1) in (3) and working out the sampled input signal x, the final output code z in offset binary form can be evaluated as

$$x = (z + 1/2) \cdot \text{LSB} - R + \varepsilon_{M+1} \quad \text{with}$$
$$z = 2^{N-1} + \sum_{i=1}^{M-1} (2D_i - 1)p_{i+1} + (D_M - 1) \tag{6}$$

where the LSB in the A/D conversion must verify

$$\text{LSB} = \frac{R}{p_0 + \sum_{i=2}^{M} p_i} = \frac{R}{2^{N-1}}. \tag{7}$$

If the constant offset terms in (6) are grouped in variable z_o, the output code can be finally expressed as the wanted weighted sum of the comparator output bits

$$z = \sum_{i=1}^{M} W_i \cdot D_i + z_o \quad \text{with} \quad W_i = 2p_{i+1}, \; W_M \equiv 1$$
$$z_o = 2^{N-1} - \sum_{i=2}^{M} p_i - 1 = p_0 - 1. \tag{8}$$

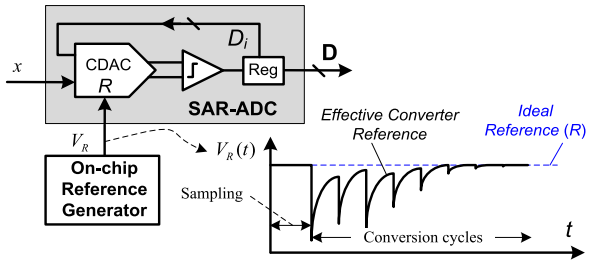

Fig. 3. Effect of the limited driving capability of the reference generator during the conversion process.

These expressions are fully general and suitable for both designs without and with redundancy, being the difference found in the radix selection (binary and nonbinary, respectively). In what follows, we will focus on the redundant case because it is more general, and it can be particularized to a nonredundant design when a binary radix is used.

In the presence of redundancy, the comparator characteristic is not univocally defined in terms of conversion residue. Actually, it is possible to define an interval at the comparator input, $[-Q_i, +Q_i]$, such that if decision ambiguity is allowed only within this interval, then the digital conversion remains perfect and identical to (8). This behavior of the comparator decisions can be mathematically expressed as

$$D_i = \begin{cases} 1, & \text{if } \varepsilon_i > +Q_i \\ 0, & \text{if } \varepsilon_i < -Q_i \\ 1 \text{ or } 0, & \text{if } |\varepsilon_i| \leq Q_i \end{cases} \tag{9}$$

where the amplitudes of the required redundancy intervals, Q_i, are related to the capacitor scale factors, p_i, as demonstrated in Appendix A, in the form

$$\underset{(i \leq M)}{Q_i} = q_i \cdot \text{LSB} \quad \text{with} \quad \begin{cases} q_i = -p_{i+1} + 1 + \sum_{k=i+2}^{M} p_k \\ q_M \equiv 0. \end{cases} \tag{10}$$

III. Proposed SAR ADC Model

The previous description implicitly assumes static conditions in the evaluation of the conversion residue and, hence, in the corresponding output code and redundancy tolerance. In practice, the incomplete settling in the references and CDAC, as well as time-variant errors in the comparator, introduces a signal-dependent error that is not properly captured.

In general, this time-varying error can be modeled by considering a transient reference, $V_R = V_R(t)$, at the output of the reference generator, as shown in Fig. 3, which changes dynamically during the conversion process. This transient behavior leads to comparison decisions that depend on the actual reference at the comparison instants according to the previous history. In this scenario expressions (1) and (10) are not valid anymore since only dc conditions were considered, and an alternative SAR ADC formulation is mandatory to accurately predict the achievable accuracy and realize the full potential of a high-speed design, especially (but not restricted) when on-chip reference and redundancy are considered.

A. Nonideal Reference Modeling

Before analyzing the implications of the dynamic errors, let us make a revision of the SAR operation based on (4) and (5). In such ideal static conditions, the absolute value of the updating step depends only on the capacitor scale factors p_i and not on the comparator output. Actually, as shown in the transient evolution of Fig. 2, the magnitudes of the jumps from a specific cycle should remain constant, determining the comparator output whether this magnitude is added or subtracted.

This situation will be completely different if the generator reference $V_R(t)$ does not remain constant since any time dependence on this signal results in a modification of the step magnitude itself. As a consequence, the evaluation of the output code should consider the actual transient residue available at the comparison trigger instant $t_{trigger}$, given by the rising edge of phase ϕ_{comp} in the example of Fig. 1

$$D_i = \begin{cases} 1, & \text{if } \varepsilon_i\left(t_{trigger}\right) + \eta_i \geq 0 \\ 0, & \text{if } \varepsilon_i\left(t_{trigger}\right) + \eta_i < 0 \end{cases} \tag{11}$$

where variable η_i groups any deviation on the effective comparator threshold due to random noise and offset in the i-th cycle.

In this situation, the generator reference $V_R(t)$ generally presents, as shown in Fig. 4(a), a transient sawtooth curve. The initial conditions at the beginning of each conversion cycle $V_{Ro}^{(i)}$ (see red circles at the falling edge of the comparator phase ϕ_{comp}) are produced by the charge redistribution due to CDAC kick-back when the comparator output is fed back, while the leading settling is motivated by the limited response of the analog reference generator.

To introduce the proposed model, let us first assume an ideal comparator and ideal switches in the CDAC without layout parasitics. Moreover, the reference generator is modeled as shown in Fig. 4(b) as a nonideal voltage source with an output resistance, R_{ref}, and an output capacitance, $C_{ref} = p_{ref}C$– the real effects associated with the switches and reference generator including postlayout parasitics–will be addressed in Section IV. According to this model, the generator-ADC system exhibits a first-order behavior, and the transient evolution of the reference becomes

$$V_R^{(i)}\left(t'\right) = R - \left(R - V_{Ro}^{(i)}\right) \cdot e^{-t'/\tau_{ref}^{(i)}}, \quad t' \in \left[0, t_{CDAC}^{(i)}\right], \ i \geq 2 \tag{12}$$

where the time variable t' is referenced to the beginning of the cycle when ϕ_{comp} falls (as highlighted in the example of Fig. 4(a) for the fourth conversion, $i = 4$); the signal $V_R^{(i)}(t')$ is the effective comparison reference within the i-th conversion cycle; and $\tau_{ref}^{(i)}$ is the time constant in the exponential function that models the settling of this cycle.

The available CDAC settling time in each cycle $t_{CDAC}^{(i)}$ comprises two contributions

$$t_{CDAC}^{(i)} = t_{trigger} + t_{comp}^{(i)}. \tag{13}$$

The first term $t_{trigger}$ is related to the time interval up to the comparator trigger from the fall of ϕ_{comp}, which is typically a constant value defined by the SAR logic implementation. The second term $t_{comp}^{(i)}$ is related to the decision time associated with the comparator. This could be also constant, as in a synchronous design, or it can be optimized following an asynchronous timing, as a function of the residue amplitude (to take advantage of the faster decision for greater amplitudes) [26].

At the i-th conversion cycle, the time constant $\tau_{ref}^{(i)}$ depends on the output resistance R_{ref} and the effective capacitance at the reference net $C_{out}^{(i)}$

$$\tau_{ref}^{(i)} = 1/\left(R_{ref}C_{out}^{(i)}\right). \tag{14}$$

The value of $C_{out}^{(i)}$ can be evaluated as the parallel connection of C_{ref} and the capacitor in series between the capacitors sampling the reference directly connected to the driver, $C_{sR}^{(i)}$, and the remaining no-sampling capacitances, $C_{nsR}^{(i)}$

$$C_{out}^{(i)} = C_{ref} + \frac{C_{sR}^{(i)} \cdot C_{nsR}^{(i)}}{C_{sR}^{(i)} + C_{nsR}^{(i)}} = C_{ref} + \frac{C_{sR}^{(i)} \cdot C_{nsR}^{(i)}}{C_{tot}} \quad \text{with}$$
$$C_{sR}^{(i)} = \sum_{k=1}^{i} C_{k+1} \quad \text{and} \quad C_{nsR}^{(i)} = \sum_{k=i+1}^{M-1} C_{k+1} + C_0 + C_{comp} \tag{15}$$

which also includes the comparator parasitic contribution ($C_{comp} = p_{comp}C$) for greater generality. Notice that the denominator of the second term in $C_{out}^{(i)}$ represents the total capacitance at the comparator input, given by

$$C_{tot} = C_{sR}^{(i)} + C_{nsR}^{(i)} = p_{tot} \cdot C = \left(p_0 + p_{comp} + \sum_{i=2}^{M} p_i\right) \cdot C. \tag{16}$$

The transient behavior given by (12) in our proposal is based, as in [23], on the dynamic evolution of a first-order system, being the time constant $\tau_{ref}^{(i)}$ and initial conditions $V_{Ro}^{(i)}$ the high-level model parameters. The model differences between our work and [23] are precisely found in how these parameters are determined. Thus, in [23], the effects of switches were considered in the evaluation of the dominant pole, i.e., $1/\tau_{ref}^{(i)}$, but without any development on the evaluation of the initial conditions after the first conversion cycle, where the signal-dependent impact of the CDAC kick-back is significant. Without this information, the term $V_{Ro}^{(i)}$ in (12) is undefined, and therefore, the model is incomplete. Although in that conditions, (12) is still useful for deriving design guidelines under worst case scenarios of the initial conditions, it does not have the capability of predicting performance, for instance, compared to postlayout transistor-level simulations, nor less the impact of dynamic errors on redundancy.

In order to fill this theoretical gap, these issues are herein addressed with a novel study of the CDAC kick-back depending on the previous history. This is achieved by determining the initial conditions $V_{Ro}^{(i)}$ in (12) for all conversion cycles as a function of the conversion bits D_i, to complement the missing information on the transient model. This study will allow predicting performance as demonstrated next, as well as studying the impact of the transient error on redundancy (see details in Appendix A).

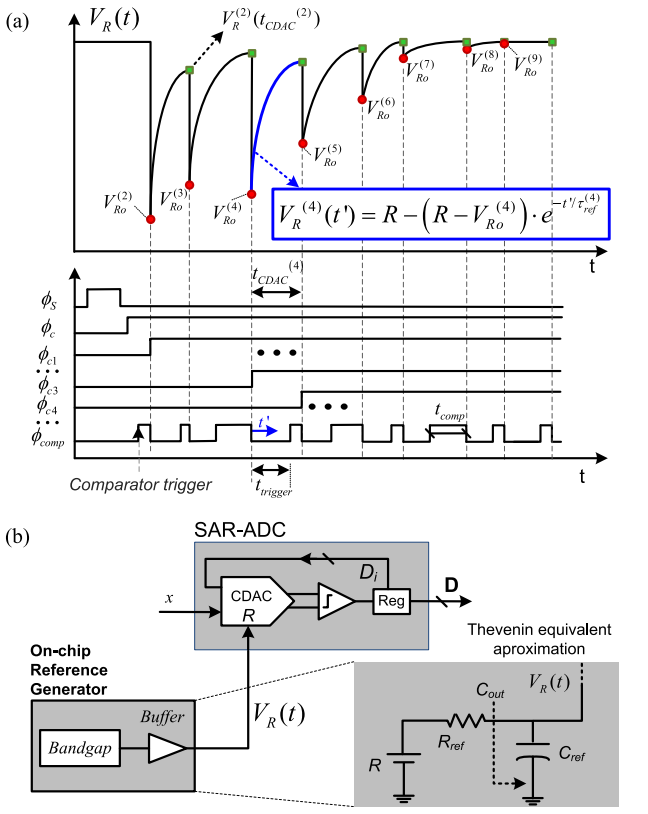

Fig. 4. (a) Transient evolution of the references considering a nonideal reference generator. (b) Simplified block diagram of the generator-ADC system.

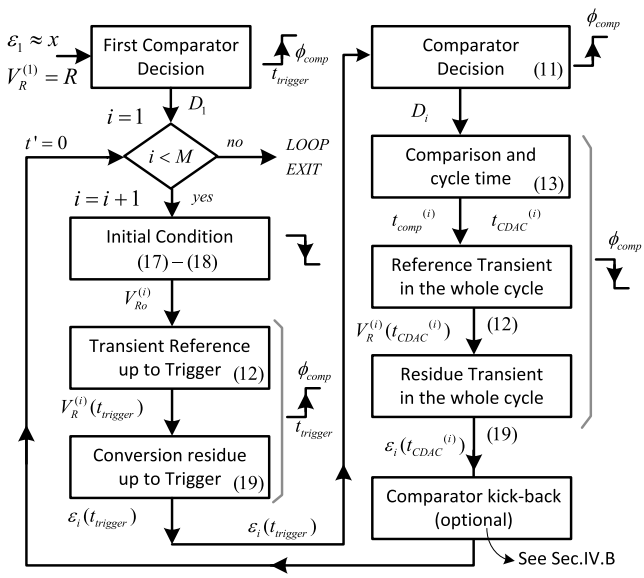

Fig. 5. Computation flow diagram of the proposed behavioral model.

B. Analysis of the CDAC Signal-Dependent Kick-Back

The initial conditions $V_{Ro}^{(i)}$ due to CDAC kick-back can be evaluated by imposing the charge redistribution just after the comparator decision is taken (and a new conversion cycle starts) since the generator buffer cannot deliver instantaneous current. The application of charge redistribution considers the generator and the CDAC outputs as high-impedance nets. This leads, as detailed in Appendix B, to an algebraic second-order equation system from which both the initial conditions for the conversion reference and the comparator input are derived. In the case of the reference, the value for the first conversion cycle can be particularized for the IMCS topology in Fig. 1 as

$$V_{Ro}^{(2)} = \frac{p_{ref}}{p_{ref} + p_2(1 - p_2/p_{tot})} \cdot R. \tag{17}$$

From this value, the initial conditions for the rest of the cycles are iteratively evaluated as

$$V_{Ro}^{(i)} = \frac{p_{ref} + \sum_{k=2}^{i-1} p_k - h_{i-1}h_i/p_{tot}}{p_{ref} + \sum_{k=2}^{i} p_k - h_i^2/p_{tot}} \cdot V_R^{(i-1)}\left(t_{CDAC}^{(i)}\right) \quad \text{with}$$

$$h_i = \sum_{k=1}^{i-1} p_{k+1}(1 - 2D_k), \quad i \geq 2, \; V_R^{(1)}\left(t_{CDAC}^{(1)}\right) = R \tag{18}$$

where $V_R^{(i)}(t_{CDAC}^{(i)})$, represented by the green squares in Fig. 4(a), is the voltage at the end of the previous cycle evaluated from (12), and variable h_i is the signed code, which captures the history of comparisons within the conversion process.

Once the evolution of the effective comparison reference is determined, the CDAC transient behavior can be finally evaluated by applying the charge conservation as in (1) considering that now that the real reference is $V_R^{(i)}(t')$

$$\varepsilon_i(t') = x - \left(\sum_{k=1}^{i-1} \frac{(2D_k - 1)p_{k+1}}{p_{tot}}\right) \cdot V_R^{(i)}(t'). \tag{19}$$

This equation of the conversion residue at the comparator input is the core of our behavioral model, together with the decision rule (11) and the description of the effective reference evolution by (12), (17), and (18).

C. Computation Flow of the Proposed Model

The transient evolution of a given stimulus can be computed according to the flow diagram in Fig. 5. The first comparison is done after inversion (when ϕ_{comp} rises) considering that the reference is properly settled at initial conditions. Based on the comparator bit D_1, the CDAC is reconfigured and a first event due to CDAC kick-back on the reference generator occurs. At this instant, the voltage jump $V_{Ro}^{(2)}$ is computed according to (17). Once the initial condition is determined, the transient evolution of the reference is computed with (12) up to the first trigger instant $t' = t_{trigger}$. With the information of the effective reference at this instant $V_R^{(2)}(t_{trigger})$, the residue and the new comparator decision, that is, D_2 and $\varepsilon_2(t_{trigger})$, are evaluated according to (11) and (19), respectively.

As commented before, the comparison time $t_{comp}^{(i)}$ in (13) could be considered fixed as in synchronous topologies or variable as in asynchronous implementations, incorporating the signal-dependent delay in the decision as a function of the residue amplitude $\varepsilon_2(t_{trigger})$ at the comparator input [26]. The delay information is used according to (13) to determine the CDAC settling time, $t_{CDAC}^{(2)}$, and to define the value of the reference at the end of the second conversion

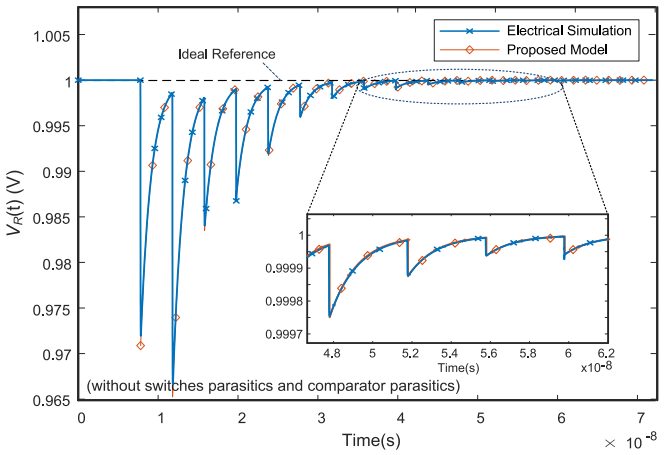

Fig. 6. Comparison of the effective transient analog reference between the proposed theoretical model and electrical simulations in a 2-V FS 13-bit SAR ADC case study operating at 15 Ms/s using the IMCS structure.

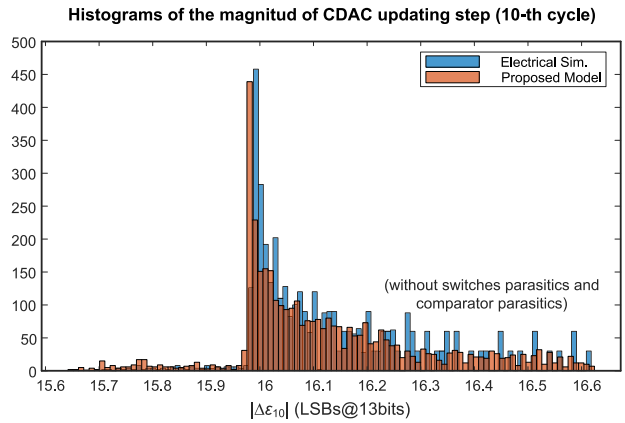

Fig. 7. Histogram comparison of the updating step amplitude at the 10th step between the proposed theoretical model and electrical simulations in a 2-V FS 13-bit 15-Ms/s SAR ADC case study with nonideal references.

cycle, $V_R^{(2)}(t_{CDAC}^{(2)})$. Based on this value, the effect of CDAC kick-back in the cycle can be evaluated using (18), and a new cycle evolution starts. This process is then iteratively performed until the last decision. At the end of the conversion instant, all the comparator bits, $\mathbf{D} = [D_1, \ldots, D_M]$, would be available and the final ADC output code can be evaluated using (8).

D. Model Comparison With Electrical Simulations

The quality of the proposed model has been verified by extensive simulations, which compares the agreement between the behavioral model implemented in MATLAB and an equivalent electrical simulation with Spectre within Cadence DesignFrameWork II, in terms of dynamic evolution and achieved performance in the ENOB. As an example, Fig. 6 shows the transient associated with the references $V_R(t)$ using the proposed theoretical model and the electrical simulations for a differential amplitude $x = 0$ V.

As a case study, a 2-V FS 13-bit SAR ADC fully differential implementation based on the IMCS topology in Fig. 1 is considered. As mandatory in high-accuracy applications, the architecture uses bottom sampling to reduce the signal-dependent errors associated with the comparator and to increase immunity against nonlinear parasitic capacitance at its input. For dealing with dynamic settling errors, the case study uses three extra bits for redundancy. Hence, 16 cycles ($M = 16$) are required for a single conversion after inversion. The implementation has a unitary capacitance $C = 1.26$ fF being the digital weights in (8), $\mathbf{W} = [3584, 2048, 1024, 512, 448, 256, 128, 64, 60, 32, 16, 8, 4, 4, 2, 1]$ and the redundant interval in (10), $\mathbf{q} = [512, 256, 256, 256, 64, 32, 32, 32, 4, 2, 2, 2, 2, 0, 0, 0]$ LSBs.

The simulations in Fig. 6 consider the following conditions: 1) the SAR logic uses a synchronous implementation with 15-Ms/s sampling frequency and conversion cycle $t_{CDAC}^{(i)}$ of 4 ns; 2) the CDAC includes no mismatch and an ideal model of switches with low-ON and high-OFF resistances; 2) the reference generator parameters are $R_{out} = 30\ \Omega$ and $C_{ref} = 32$ pF; and 3) the comparator considers an event-driven model in Verilog-A with zero parasitic input capacitance $C_{comp} = 0$ (i.e., $p_{comp} = 0$), a comparison time $t_{comp}^{(i)}$ of 850 ps and an input-referred comparison noise of 0.2 LSB_{rms}.

Notice that the agreement between our theoretical model and the electrical simulations is very good, being the marginal discrepancies motivated by the considered charge-redistribution approach: 1) ideal one in our situation and 2) small but nonnegligible effect of switches resistances in simulations. Although omitted in Fig. 6, the same level of correspondence is found in terms of performance using a full-scale 4.9-MHz sinusoidal input, being the ENOB in both cases around 12.5 bits.

The advantages of the proposed model become even more relevant when analyzing the tolerances of redundancy. As an example, Fig. 7 shows a histogram comparison between electrical simulations and the proposed model of the absolute updating step $|\Delta\varepsilon_i|$ for the 10th conversion cycle (using the previous sinusoidal input). In a static situation, we should expect, according to (4), a constant value given by half the weighting expressed in LSBs, that is, $|\Delta\varepsilon_{10}|$ (in LSBs) $= W_{10}/2 = 16$. However, this behavior is not anymore present when dynamic errors are included. As predicted with (19), the distribution still has a higher probability of occurrence around the ideal value of 16 LSBs, but it shows a nonnegligible dispersion due to the settling errors. In any case, the maximum deviation around the mean value at 15 Ms/s is well below the redundancy tolerance ($q_{10} = 2$), and hence, they can be robustly addressed by the considered scheme without affecting performance—this justifies in concordance with comparator noise level (in the order of 12.5 bit), why an almost ideal situation is achieved when operating at 15 Ms/s.

Compared to electrical simulations, the proposed behavioral model provides a significant reduction in the computation time. In this sense, it is worth noticing that even in this simple example (with ideal switches and comparator), the CPU time in the electrical simulations is more than 39 h (using a state-of-the-art Xenon-based computation server) due to the small integration step needed to resolve differential equations with enough accuracy to reach 13-bit effective resolution. This time is reduced below 0.6 s with the proposed behavioral model.

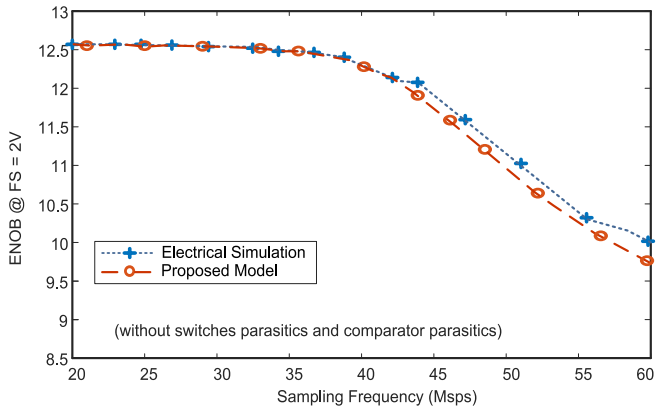

Fig. 8. Evolution of the SAR ADC ENOB with the sampling frequency for the 2-V FS 13-bit SAR ADC case study with nonideal references.

To complement the study, Fig. 8 shows a situation in which the limits of redundancy are stressed due to dynamic errors. It presents the evolution of SAR ADC effective resolution for a full-scale input sine wave versus the sampling frequency $f_s \in [20, 60]$ Ms/s for both the proposed behavioral model and the electrical simulations. Up to 37 Ms/s, the considered redundancy scheme can deal with dynamic errors due to the incomplete settling in the reference. The behavioral model correctly identifies the onset of performance degradation in terms of ENOB. Above this frequency, both the behavioral and the electrical simulation show the same trends with very low differences between them. Notice that the model is actually conservative, in the sense that it tends to overestimate the degradation, which is safer for design exploration purposes.

IV. Modeling of Transistor and Postlayout Effects

Up to now, the proposed behavioral model only relies on high-level parameters linked to the SAR architecture (the redundancy scheme and the distribution of the CDAC weights) and to the first-order response of the reference driver (R_{ref} and C_{ref}). It is thus suitable for the exploration of the design space and the identification of architectural tradeoffs, in a purely top-down approach. However, this model can also be refined to incorporate the effects associated with the physical transistor-level implementation: namely, the signal-dependent charge injected by real implementation of switches, comparator, and reference generator including postlayout parasitics. This extended model lends itself well to bottom-up approaches, where real building blocks are available down to the transistor and physical levels to fine-tune a model that can predict system-level performance.

A. Impact of Switches in the CDAC Kick-Back

Let us first focus on the charge injection due to switches commutation (from ON- to OFF-states and vice versa), which introduces a nonnegligible effect on the SAR ADC transient response. Phenomenologically, the charge injection lowers the initial conditions $V_{Ro}^{(i)}$ [the red dots in Fig. 4(a)], which causes a greater jump in each conversion cycle. Hence, it leads to greater settling requirements in the generator buffer to achieve the target resolution. The decrement, which is related

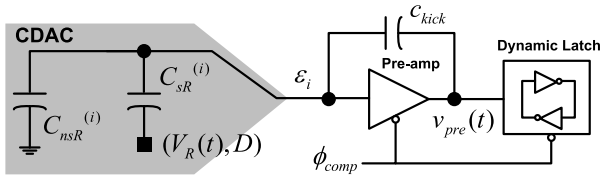

Fig. 9. Simplified kick-back single-ended model of the CDAC and comparator interface.

to the switches size and supply voltage (V_{DD}), can be evaluated similar to the case in Section III-A. Applying the charge-redistribution technique, the initial condition for the second cycle from (17) should be modified as

$$V_{Ro}^{(2)} = \frac{p_{ref}R - \alpha p_{sw,2} V_{DD}}{p_{ref} + p_{sw,2} + p_2(1 - p_2/p_{tot})} \tag{20}$$

where the scale factor $p_{sw,2}$ is related to the switches capacitive parasitics, $C_{sw,2} = p_{sw,2}C$, and the parameter α considers the contribution of the nMOS and pMOS transistors. In our case study, the designs of switches were done to assure the same transistor contributions, and hence, $\alpha \approx 2$.

Similarly, the rest of the initial conditions after each comparator decision are modified from (18) in the form

$$\begin{aligned} V_{Ro}^{(i)} &= \left[\left(p_{ref} + \sum_{k=2}^{i-1}(p_k + p_{sw,k}) - \frac{h_{i-1}h_i}{p_{tot}}\right) \cdot V_R^{(i-1)}\left(t_{CDAC}^{(i-1)}\right) \cdots \right. \\ &\quad \left. - \alpha p_{sw,(i)} V_{DD}\right] \Bigg/ \left[p_{ref} + \sum_{k=2}^{i}(p_k + p_{sw,k}) - h_i^2/p_{tot}\right]. \end{aligned} \tag{21}$$

Notice that these initial conditions are computed iteratively—they are signal-dependent since they rely on the conversion history of the cycle, through the terms h_i in (18). The additional contributions in (20) and (21) with respect to (17) and (18) are dominated by the term $p_{sw,i}$ in the numerator, which decreases the value of the reference and thus increases the voltage peak due to CDAC kick-back. This additional term should also be compensated by the generator buffer at the end of the conversion phase, leading to greater settling requirements when compared to the ideal situation for a given accuracy and, hence, extra power consumption.

B. Comparator Kick-Back

In high-performance SAR ADC designs, it is essential to control the kick-back of comparator [27], [28]. To achieve this, multistage architectures are commonly used, which involve at least one preamplifier, working as a clocked integrator to reduce power consumption, followed by a dynamic latch for fast output value reconstruction [28], [29]. Since the disturbance of the dynamic latch referred to the input is divided by the front-end preamplifier's gain, its contribution is of second order. Therefore, the global kick-back will be mainly dominated in practical cases by the preamplifier contribution.

As shown in Fig. 9, the comparator kick-back can be analyzed considering the effective aggressor capacitance c_{kick} of the comparator, which modifies the CDAC residue ε_i at its inputs. The differential voltage at the output of the preamplifier

v_{pre} is a signal, which tends to 0 at the end of each conversion cycle, since the clocked integrator-based preamplifier is always rested to V_{DD} or ground V_{SS} depending on if an nMOS or pMOS input pair, respectively [28].

In this situation, the residue suffers two different aggression events: 1) a first voltage jump at the trigger instant ($t_{trigger}$) and 2) a second step in the opposite direction when the comparator is reset at the end of the conversion after comparator decision is taken at $t_{CDAC}^{(i)}$. In this way, the net differential kick-back contribution $\varepsilon_{KB,i}$ at the end of i-th conversion cycle becomes

$$\varepsilon_{KB,i} = \frac{c_{kick}}{C_{tot} + c_{kick}} \cdot \left[v_{pre}\left(t_{CDAC}^{(i)}\right) - v_{pre}\left(t_{trigger}\right) \right] \tag{22}$$

where the aggressor voltage v_{pre} difference between the two events results scaled by the capacitive divider in the structure being C_{tot} the total capacitance in (16).

This contribution can be added in the flow diagram of Fig. 5 in additional step by simple replacing the residue generation in (19) by the perturbed one with the kick-back term

$$\varepsilon_i = \varepsilon_i^{(eq.(19))} + \varepsilon_{KB,i}. \tag{23}$$

It is worth highlighting that the contribution of kick-back tends to be negligible at the end of the conversion process when the preamplifier output is completely set $v_{pre}\ (t_{CDAC}^{(i)}) \approx v_{pre}\ (t_{trigger}) \approx 0$, and hence, $\varepsilon_i \approx \varepsilon_i^{(eq.(19))}$. Actually, in the behavioral simulations results of Section V, we omitted the kick-back effect and no limitations in performance predictions were observed compared to the electrical ones with kick-back. Under this considerations, the impact of the real comparator implementation will be mostly concentrated in defining the comparison time $t_{comp}^{(i)}$ in (13) and the parasitic capacitance at its inputs $C_{comp} = p_{comp}\mathrm{C}$ in (16).

C. Impact of Switches in the Settling Time

The inclusion of switch parasitics (both resistive and capacitive) is a really challenging task in SAR modeling since, strictly speaking, the generator-CDAC system is a high-order dynamic system [24]—actually, for the SAR ADC case study of the previous example, the order is greater than thirty: 15 branches, factor (×2) due to the differential structure, plus the reference, the common mode, and the comparator nets. To handle such complexity, several strategies are needed to make the closed-form expression feasible, trying to reduce the order of the system. Thus, in [23], a second-order equivalent is developed under some circuit simplifications based on the ON-resistance of switches and neglecting their capacitive contribution. Even with this drastic reduction (which could be not feasible at high speed), the time-domain solution is finally simplified to a first-order system, being the time constant defined by the resulting dominant pole.

Aware of this modeling problem, in our work, we have taken a different approach. Instead of analyzing the complete structure (assuming a simplified model for the switches), we have a priori imposed the functional form of (12) as starting point, being the impact of switch parasitics (resistive, but also capacitive) concentrated in a modification of the time constant $\tau_{ref}^{(i)}$ with respect to the ideal values in (14). In that way, the impact of switch parasitics would be effectively captured by

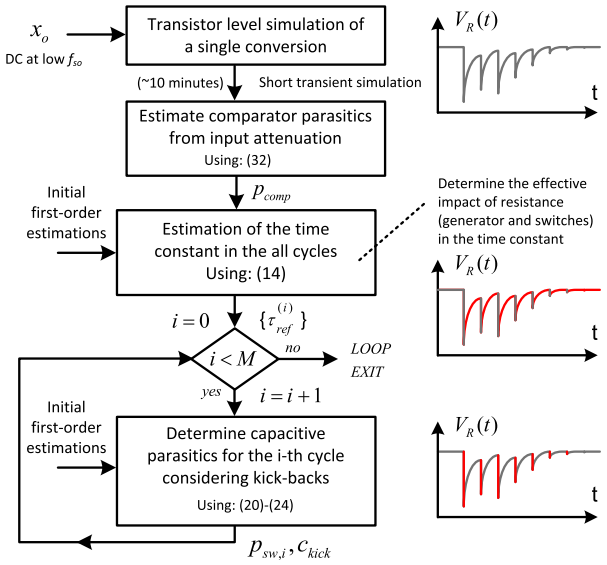

Fig. 10. Adaptive procedure for estimating the effects of resistive and capacitive parasitics at the transistor level.

two different parameters: 1) the effective time constants $\tau_{ref}^{(i)}$ in each segment and 2) the modification of the initial conditions in (20) and (21) through the switches factor $p_{sw,i}$.

As shown in Section V, the high accuracy of this approach has been confirmed in a practical integration in a 65-nm process. The question arising now is how we can perform the extraction of these parameters to achieve such a level of accuracy. This issue is addressed next.

D. High-Precision Extraction of SAR ADC Parameters

The values of the time constants $\tau_{ref}^{(i)}$ for each segment and the switch parasitics $p_{sw,i}$ can be initially set according to the designer's expertise, evaluated by block-level simulations, or taking first-order estimations based on device sizes. As an example, the capacitive term can be estimated assuming that the transistors are biased in the ohmic region, in the form

$$p_{sw,i} \approx \gamma \cdot \left(W \cdot L \cdot C'_{ox} + C_{j,D\text{-}S}\right)/C \tag{24}$$

where (W, L) defines the transistor size, C'_{ox} is the gate capacitance per surface, $C_{j,D\text{-}S}$ is the drain/diode junction capacitance, and γ is a factor depending on the switch implementation and the charge, which is effectively transferred. Similarly, the impact of switch resistance in time constant $\tau_{ref}^{(i)}$ can be incorporated using the simplified expressions in [23] as an initial guess.

However, in this work, we opted to follow a realistic bottom-up approach in which the switches parameters ($\tau_{ref}^{(i)}$, $p_{sw,i}$) as well as the comparator parasitics (p_{comp} and c_{kick}) in (16) and (22) are estimated with high precision from one electrical simulation with extremely low-computation time. This is achieved by stimulating the ADC with a dc input stimulus, $x = x_o$, over a single conversion cycle at a low sampling frequency, f_{so}. For this simulation, we record the reference voltage $V_R(t)$, the comparator input $\varepsilon(t)$, and the comparator output code set $\mathbf{D}$. Then, the initial parameter values ($\tau_{ref}^{(i)}$, $p_{sw,i}$, p_{comp}, and c_{kick}) are refined to minimize

the error between the electrical simulations and the proposed model, as shown in Fig. 10.

The minimization procedure focuses not only on the quiescent value but also on the whole transient response during the different segments through the conversion cycle. In such a way, the complete dynamic response, even high-speed effects, which would be relevant at a higher sampling frequency (i.e., $f_s \gg f_{so}$) results, captured. In the first step, the attenuation of the input signal at the comparator input after the inversion phase is used to estimate the comparator input capacitor factor p_{comp}. Next, the effective time constants are estimated from the derivative of $V_R(t)$ in each segment before the comparator trigger. Afterward, the initial conditions $V_{Ro}^{(i)}$ are calculated by fitting the exponential segments according to (12) with the obtained $\tau_{ref}^{(i)}$ to match the residue $\varepsilon_i(t_{trigger})$ at the comparator trigger instant. We then use the recorded comparator decisions to build the history (h_i) and determine in an iterative manner the switches parameters $p_{sw,i}$ using (20) and (21).

Notice that although this model-tuning approach is based on one electrical simulation at the transistor level, the computation time is quite reduced since a unique dc input level is used at a low sampling frequency, and it is repeated only once for a given switch selection. Moreover, we will see the validity of this hypothesis, in the simulation results at the full transistor level, thus allowing a direct extrapolation to any signal within the complete full scale.

E. Effects of Reference Buffer and Postlayout Parasitics

Following the same strategy as for the SAR ADC parameters, the effects of the reference buffer and postlayout parasitics can be incorporated in the proposed description. This is especially relevant for high-speed high-resolution applications, and it is practically by: 1) imposing the functional form (12) as starting point and 2) adjusting the model parameters—these are the buffer and switches effective time constant, $\tau_{ref}^{(i)}$, as well as the terms associated with switches ($p_{sw,i}$), comparator (p_{comp} and c_{kick}), and buffer (C_{ref})—to minimize the errors between the actual transient response of the complete system and the model response. These parameters are again estimated based on the adaptive procedure in Fig. 10 using a short transient simulation for a single dc stimulus.

V. Model Validation at the Postlayout Transistor Level

This section presents the validation results of the proposed model at full transistor level with postlayout parasitic backannotation. The transient and performance predictions given by the model are compared to a 1.2-V 65-nm prototype of the SAR ADC previously introduced in Section III-D. The aim of this comparison is double: 1) to provide a reliable estimation of the achievable accuracy in terms of ENOB using the model computation flow in Fig. 5 and 2) to validate the robustness of the parasitic extraction procedure in Fig. 10 in an SAR ADC design, using a unique dc test stimulus, down to the physical level. In this sense, the herein presented results are based on a single characterization run with $f_{so} = 10$ Ms/s and $x_o = 0$ V, being the total accumulated time around 20 min.

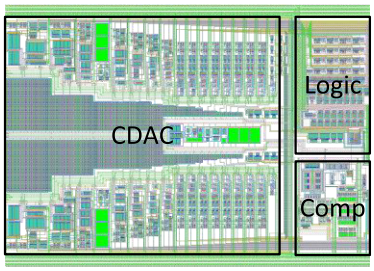

Fig. 11. Layout of the core of the 1.2-V 65-nm SAR ADC prototype integrated in a one-poly nine-metal TSMC CMOS process.

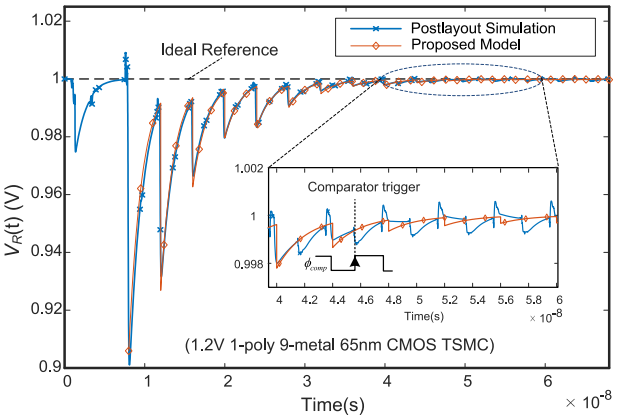

Fig. 12. Analog reference evolution during the SAR ADC operation considering the transistor effect of the CDAC switches and comparator kick-back.

The prototype, currently under fabrication in a 65-nm CMOS process, has a resolution of 13 bits, a full scale of 2 V with 0.5-V common mode, a unitary capacitor $C = 1.26$ fF, and three extra cycles for redundancy, i.e., $M = 16$. It can be reconfigured in both synchronous and asynchronous modes. For simplicity, we focus now on the synchronous case, but the asynchronous approach can be analogously studied incorporating the signal-dependent comparator delay [26].

The redundancy scheme was derived following the split-capacitor approach for redundancy distribution in [11], [12], and [13]. This approach starts from the classical (binary radix) capacitor scale factors without redundancy, in our case $N = 13$ bits. Then, it distributes the scale factor associated with the capacitor C_2 within the rest of the SAR ADC queue performing a binary expansion. In that way, the complexity of the digital correction logic is reduced while avoiding over-ranging [13].

The core of the SAR ADC, shown in Fig. 11, has an occupied die of 0.28 mm^2, while the reference generator is based on an open-loop source follower with an on-chip replica input voltage stabilization for a robust generation. Its silicon area and power consumption are 0.6 mm^2 and 4.8 mW, respectively. The switches in the CDAC use a CMOS topology to control the charge injection and clock feedthrough, except the input and bottom-sampling switches that are bootstrapping to assure that the sampling is not limiting in performance up to the second Nyquist's band. The comparator design, based on the two-stage architecture in [28], comprises a switchable low-power preamplifier integrator with zero bias current followed by a strong-arm dynamic latch.

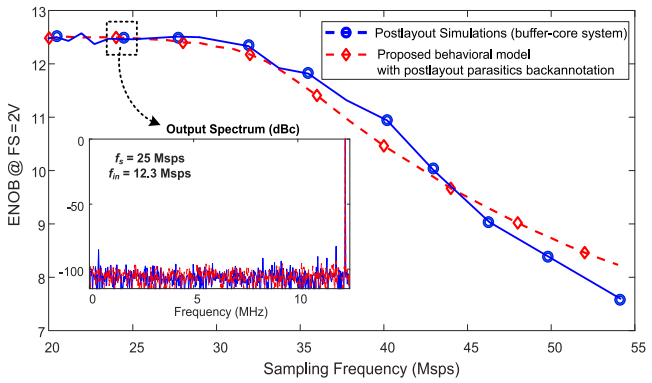

Fig. 13. Comparison of performance between the proposed model and the postlayout transistor-level simulations with Cadence Spectre in a 1.2-V 13-bit 65-nm SAR ADC prototype.

A. Time-Domain Comparison

Fig. 12 shows a comparison of the transient evolution of the proposed model and the postlayout transistor-level simulations. The reference at the output of the generator is depicted during a complete conversion process, showing a notable agreement between theoretical predictions and simulation results. The inset in Fig. 12 illustrates how the comparator kick-back, which occurs at the trigger edge, is translated to the reference. For the MSBs, the comparator perturbation is completely restored after reset. For the LSBs, the induced perturbation by the comparator can alter the transient matching of the procedure in Fig. 10, but with negligible impact on performance at the end of conversion since the CDAC is almost in a quiescent situation (in consonance with our previous analysis in Section IV-B).

B. Performance Comparison

This section presents the validation results for the proposed model and the postlayout transistor-level simulations. As a figure of merit, the ENOB is considered for a reliable comparison. The results as a function of the sampling frequency are shown in Fig. 13 (the inset presents the 25-Ms/s output spectrums as a particular case). In all the cases, the ENOB was evaluated from a full-scale sinusoidal input stimulus at Nyquist's frequency. Again, the proposed model can accurately describe the degradation in performance when increasing the sampling speed. This degradation is a consequent of the reduction of the available CDAC settling time in each cycle, $t_{CDAC}^{(i)}$ in (12), when increasing sampling frequency. In the best knowledge of the authors, this is the first time that a behavioral model based on closed-form expressions with low-computation resources achieves such a level of accuracy in the ENOB prediction at the transistor level, even more when postlayout effects are considered.

To make the computation time feasible at postlayout and transistor levels due to a great number of devices (24 543 bsim transistors, 124 poly-silicon resistors, two BJTs, and parasitics), several simulation strategies were considered: 1) the number of the points in the FFT was decreased down to 1024; 2) coherent sampling was considered to avoid windowing; 3) the transient noise was disabled; and 4) a random noise source with an equivalent 0.2 LSB_{rms} distribution was included at the input of the comparator at transistor level for a trustworthy comparison with the behavioral model. Despite these strategies for speeding up simulation, the accumulated CPU time in the electrical simulations was greater than 20 days, compared to less than 5 s for our proposal.

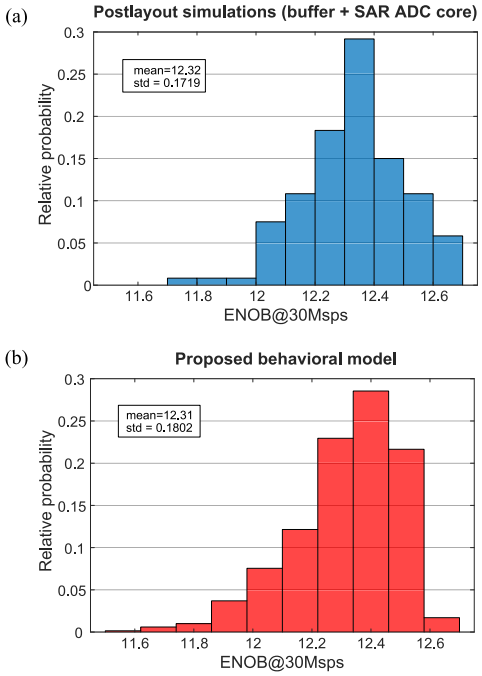

Fig. 14. Monte Carlo mismatch analysis of a 1.2 V 13-bit 65 nm SAR ADC prototype considering post-layout transistor-level simulations with Cadence Spectre and the propose model. (a) Post-layout simulations. (b) Proposed model.

In all these simulations, it is worth reminding that parasitic extraction of the model according to the procedure in Fig. 10 was carried out using a single 20-min simulation with a dc input stimulus at 10 Ms/s. This means that the complete curves from 20 to 55 Ms/s were estimated by the model based on pure theoretical extrapolated predictions, as an additional indicator of the quality and robustness of the proposal.

VI. Discussion and Future Work

This article focuses on the presentation and validation of the behavioral model in a realistic design scenario at the postlayout transistor-level simulation. Although the development of a complete design methodology from the proposed model is beyond the scope of this article, the accuracy and simplicity of the model open the door to multiple applications ranging from the evaluation of tradeoffs when considering mismatch, process, voltage and temperature (PVT) variations, redundancy, and calibration, up to the systematic exploration of wider design space, including other redundant schemes due to the reduced simulation time.

As an illustrative example, Fig. 14(a) and (b) shows a Monte Carlo mismatch analysis of the SAR ADC of the previous section at 30 Ms/s using postlayout transistor-level simulations and our proposed model, respectively. In electrical simulations (#runs = 120), mismatching was considered in all devices, being the performance dominated by the CDAC capacitor array as usual in high-speed high-resolution designs. In our

model (#runs = 2000), mismatching was introduced using an error term in the scale factor, $p_i\ (1 + e_{pi})$, where random variable e_{pi} was generated according to the technology mismatch report. The agreement between theory and simulation results is quite remarkable, all with a significant reduction in accumulated computational costs, from several weeks to just seconds.

Similarly, the proposed dynamic model can also be used in a top-down/bottom-up design optimization loop in which first, a suitable set of settling requirements are determined based on behavioral simulations and preliminary parasitics estimations, then, these values are used as target specifications to size the reference generator and switches at the transistor level, and if needed, the parasitic estimations can be refined in a new iteration following the proposed modeling procedure in this article.

VII. Conclusion

This article presents a behavioral model based on closed-form expressions for high-speed high-accuracy SAR ADCs with charge-redistribution CDACs and on-chip reference generation. The model can capture the incomplete settling behavior due to the reference generator, switches parasitic contributions (resistive, capacitive, and charge injection), and considers comparator effects (capacitive parasitics and kick-back noise), as well as layout parasitics in the physical implementation. It provides an efficient platform to explore the impact of design specifications on the achievable ENOB, overcoming current computation bottlenecks when analyzing complex tradeoffs between performance, redundancy, and operation speed for a given target resolution at the transistor level, especially when postlayout parasitcs are included. The proposed description is complemented with a theoretical analysis of signal-dependent errors due to CDAC and comparator kick-back on the reference and redundancy intervals.

As a case study, the tradeoff between accuracy and conversion speed is analyzed in a 1.2-V 13-bit 65-nm SAR ADC at the postlayout level characterized between 20- and 60-Ms/s sampling frequencies, showing negligible discrepancies between the ENOB model predictions and the postlayout transistor-level simulations with a notable reduction in computation time (from several weeks to seconds). To the best authors' knowledge, this is the first time that such a reliable comparison has been achieved.

Appendix A
Dynamic Redundancy Intervals

One advantage of the proposed model is that as the dynamic evolution is completely resolved in the time domain, it is possible to estimate the impact of signal-dependent settling errors on the amplitude of the redundant intervals themselves.

For clarity, let us analyze first the effect of redundancy if the dynamic errors are neglected. In static conditions, a decision error occurred within the redundancy interval at the i-th cycle, i.e., $D_i = 1$ when $\varepsilon_i < 0$ or $D_i = 0$ when $\varepsilon_i \geq 0$, can be only recovered if the magnitude of the error, i.e., the updating step $\Delta\varepsilon_i$, in (4) can be compensated by the remaining steps driving a final residue in the N-bit quantization error, i.e.,

$$\begin{aligned}&\text{if } (D_i = 0 \text{ when } 0 \leq \varepsilon_i \leq +Q_i) \text{ or}\\ &\quad (D_i = 1 \text{ when } -Q_i \leq \varepsilon_i < 0)\\ &\rightarrow |\varepsilon_{M+1}| = \left|\varepsilon_i + \boldsymbol{\Delta\varepsilon}_i + \sum_{k=i+1}^{M} \Delta\varepsilon_k\right| \leq \text{LSB}/2. \end{aligned} \tag{25}$$

The correctable worst case situation is found when an error occurs at the i-th cycle, which is followed by a streak of comparator decision with the opposite value, i.e., $D_k = \text{not}(D_i)$ with $k \in [i+1, M]$. In these conditions, the amplitude of the redundancy interval for the i-th cycle is such that the residue precisely lies on the boundary $\varepsilon_i = \pm Q_i$, and the residue at the end of the M-th cycles takes its maximum or minimum values—that is, $\varepsilon_{M+1} = \pm\text{LSB}/2$. In accordance with this, using (25), the following expressions as a function of the incorrect decisions in red are derived:

$$\begin{aligned}\varepsilon_i &= +Q_i \rightarrow +Q_i + \Delta\varepsilon_i\left|_{D_i=0} + \sum_{k=i+1}^{M} \Delta\varepsilon_k\right|_{D_k=1}\\ &= +\text{LSB}/2\\ \varepsilon_i &= -Q_i \rightarrow -Q_i + \Delta\varepsilon_i\left|_{D_i=1} + \sum_{k=i+1}^{M} \Delta\varepsilon_k\right|_{D_k=0}\\ &= -\text{LSB}/2 \end{aligned} \tag{26}$$

which considering (4) and (5) directly lead to the demonstration of the relationship between Q_i and p_i in (10) in static conditions.

To find an equivalent relationship when settling errors cannot be neglected, let us define the redundant interval as $[-Q_i^{(-)}, +Q_i^{(+)}]$, where the superscripts account for any possible dissymmetry in the upper and lower limits due to dynamic errors. Under the same considerations as in (26), when an error in the i-th cycle is followed by a streak of comparator decisions with the opposite value, the following expression is obtained for the upper limit:

$$\begin{aligned}&\text{Being} \quad \mathbf{D} = \{\mathbf{D}^{(i-1)}, \underset{(i)}{0}, 1, \ldots, \underset{(M)}{1}\}\\ &Q_i^{(+)} = \varepsilon_i\left(t_{CDAC}, \mathbf{D}^{(i-1)}\right) - \varepsilon_{M+1}\left(\mathbf{D}^{(i-1)}, \underset{(i)}{0}, 1, \ldots, \underset{(M)}{1}\right)\\ &\qquad + \text{LSB}/2 \end{aligned} \tag{27}$$

while for the lower limits, it produces

$$\begin{aligned}&\text{Being} \quad \mathbf{D} = \{\mathbf{D}^{(i-1)}, \underset{(i)}{1}, 0, \ldots, \underset{(M)}{0}\}\\ &-Q_i^{(-)} = \varepsilon_i\left(t_{CDAC}, \mathbf{D}^{(i-1)}\right) - \varepsilon_{M+1}\left(\mathbf{D}^{(i-1)}, \underset{(i)}{1}, 0, \ldots, \underset{(M)}{0}\right)\\ &\qquad - \text{LSB}/2. \end{aligned} \tag{28}$$

Once evaluated the transient evolution according to the procedure in Fig. 5, these equations predict the dynamic behavior of the effective redundant interval. However, it could be interesting to relate them to the ideal values in static conditions, denoted as $[-Q_i^{(id)}, +Q_i^{(id)}]$. To do that, let us introduce the error between the actual and the ideal reference

at the i-th cycle, $\Delta e_R^{(i)}$, i.e., $V_R^{(i)} = R - \Delta e_R^{(i)}$. With this definition, if we assume that this error is practically null at the M-th cycle, where the quiescent situation is expected, the following expressions of the redundancy boundaries depending on the previous history can be determined:

$$Q_i^{(\pm)} \approx Q_i^{(id)} \pm \left(\sum_{k=1}^{i-1} \frac{(2D_k - 1)p_{k+1}}{p_{tot}} \right) \cdot \Delta e_R^{(i)}\left(t_{CDAC}, \mathbf{D}^{(i-1)}\right). \tag{29}$$

The redundancy interval would be, therefore, signal-dependent. The worst case is found when the history produces all "0" for the upper limit or all "1" for the lower limit, since in these cases, there is a constructive addition. In this situation, the redundant interval is also symmetric as in (10).

Appendix B
Evaluation of the CDAC Kick-Back

The impact of CDAC kick-back on the effective converter reference can be described considering the charge injection that occurs when the capacitors in the CDAC sample the references. In each conversion step, the initial conditions are derived based on the charge redistribution before and after the comparator feedback to the CDAC.

The network has two coupled nodes: 1) the comparator inputs and 2) the buffer output providing the reference $V_R(t)$ in Fig. 1. The charge distribution in the reference node can be applied at the beginning of the conversion phase since the buffer cannot deliver the required charge instantaneously, hence establishing a suitable for determining the initial conditions $V_{Ro}^{(i)}$ in (12).

In this way, for the first conversion cycle ($i = 1$), the following two equations must be initially satisfied:

$$\left(\sum_{k=1}^{M-1} C_{k+1} + C_0 + C_{comp} \right) \varepsilon_1 = C_2 \left(\varepsilon_2^{0+} - (1 - 2D_1) V_{R0}^{(2)} \right) + \left(\sum_{k=2}^{M-1} C_{k+1} + C_0 + C_{comp} \right) \varepsilon_2^{0+} \tag{30}$$

$$C_2 \varepsilon_1 (1 - 2D_1) - C_{REF} R = C_2 \left(\varepsilon_2^{0+} (1 - 2D_1) - V_{Ro}^{(2)} \right) - C_{REF} V_{Ro}^{(2)} \tag{31}$$

where ${\varepsilon_i}^{0+}$ is the initial residue in the i-th cycle, that is, $\varepsilon_i^{0+} = \varepsilon_i(t' = 0^+)$ and ε_1 is the attenuated input signal due to the capacitive divided when C_{comp} is considered, given by

$$\varepsilon_1 = x \cdot C_t / C_{tot}. \tag{32}$$

Using this and the definitions of C_{tot} and C_t in (2) and (16), (30) and (31) can be rewritten as follows:

$$\begin{aligned} C_t x = C_{tot} \frac{C_t x}{C_{tot}} &= C_{tot} \varepsilon_2^{0+} \\ &\quad - C_2 (1 - 2D_1) V_{R0}^{(2)} (1 - 2D_1) \left(C_2 \frac{C_t x}{C_{tot}} - C_2 \varepsilon_2^{0+} \right) \\ &\quad - C_{REF} R \\ &= -V_{Ro}^{(2)} (C_2 + C_{REF}) \end{aligned} \tag{33}$$

from which, working out the input signal x, the size of the first step is determined as

$$V_{Ro}^{(2)} = \frac{C_{REF}}{C_{REF} + C_2 - C_2^2 / C_{tot}} \cdot R \tag{34}$$

which can be directly rewritten as (17) considering the scale factors with respect to the unitary capacitance C.

Repeating the same process for the rest of the conversion cycle, $i \in [2, M-1]$, two additional relationships are derived for the unknowns $\{V_{Ro}^{(i+1)}, \varepsilon_{i+1}^{0+}\}$

$$\begin{aligned} &\sum_{k=1}^{i-1} C_{k+1} \left((1 - 2D_k) \varepsilon_i^{end} - V_{R,end}^{(i)} \right) + C_{i+1} (1 - 2D_k) \varepsilon_i^{end} \\ &\quad - C_{REF} V_{R,end}^{(i)} \\ &= \sum_{k=1}^{i} C_{k+1} \left((1 - 2D_k) \varepsilon_{i+1}^{0+} - V_{Ro}^{(i+1)} \right) - C_{REF} V_{Ro}^{(i+1)} \end{aligned} \tag{35}$$

$$\begin{aligned} &\sum_{k=1}^{i-1} C_{k+1} \left(\varepsilon_i^{end} - (1 - 2D_k) V_{R,end}^{(i)} \right) \\ &\quad + \left(\sum_{k=i}^{M-1} C_{k+1} + C_0 + C_{comp} \right) \varepsilon_i^{end} \\ &= \sum_{k=1}^{i} C_{k+1} \left(\varepsilon_{i+1}^{0+} - (1 - 2D_k) V_{Ro}^{(i+1)} \right) \\ &\quad + \left(\sum_{k=i+1}^{M-1} C_{k+1} + C_0 + C_{comp} \right) \varepsilon_{i+1}^{0+} \end{aligned} \tag{36}$$

where $\varepsilon_i^{end} = \varepsilon_i(t' = t_{CDAC}^{(i)})$ is the final value of the residue and $V_{R,end}^{(i)} = V_R^{(i)}(t' = t_{CDAC}^{(i)})$ is the reference in the i-th cycle.

From these relationships, expression (18) can be directly evaluated for the rest of the cycles considering again the introduced scaled factors with respect to C.

Acknowledgment

The authors would like to thank the Instituto Universitario de Investigación en Ingeniería de Aragón (I3A), Universidad de Zaragoza, Zaragoza, Spain, for the support and help given to Carlos Dominguez-Matas during his one-month doctoral internship at this institution, where part of this work was carried out.

References

[1] X. Tang et al., "Low-power SAR ADC design: Overview and survey of state-of-the-art techniques," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 6, pp. 2249–2262, Jun. 2022.

[2] B. Chen, M. Maddox, M. C. W. Coln, Y. Lu, and L. D. Fernando, "Precision passive-charge-sharing SAR ADC: Analysis, design, and measurement results," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1481–1492, May 2018.

[3] A. Wang and C.-J. R. Shi, "Analysis of passive charge sharing-based segmented SAR ADCs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 5, pp. 1195–1206, May 2020.

[4] Y.-H. Chung, C.-W. Yen, P.-K. Tsai, and B.-W. Chen, "A 12-bit 40-MS/s SAR ADC with a fast-binary-window DAC switching scheme," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 1989–1998, Oct. 2018.

[5] R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, and H. Zhu, "A 14b 80 MS/s SAR ADC with 73.6 dB SNDR in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3059–3066, Dec. 2013.

[6] M. Liu, A. H. M. van Roermund, and P. Harpe, "A 10-b 20-MS/s SAR ADC with DAC-compensated discrete-time reference driver," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 417–427, Feb. 2019.

[7] Y. Zhou, B. Xu, and Y. Chiu, "A 12-b 1-GS/s 31.5-mW time-interleaved SAR ADC with analog HPF-assisted skew calibration and randomly sampling reference ADC," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2207–2218, Aug. 2019.

[8] Y. Zeng, C.-H. Chan, Y. Zhu, and R. P. Martins, "An auxiliary-loop-enhanced fast-transient FVF LDO as reference buffer of a SAR ADC," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2022, pp. 2660–2664.

[9] Y. Shen, X. Tang, X. Xin, S. Liu, Z. Zhu, and N. Sun, "A 10-bit 100-MS/s SAR ADC with always-on reference ripple cancellation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 10, pp. 3965–3975, Oct. 2022.

[10] T. Ogawa, H. Kobayashi, M. Hotta, Y. Takahashi, H. San, and N. Takai, "SAR ADC algorithm with redundancy," in *Proc. APCCAS IEEE Asia Pacific Conf. Circuits Syst.*, Nov. 2008, pp. 268–271.

[11] W. Liu, P. Huang, and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2661–2672, Nov. 2011.

[12] J. Tsai et al., "A 0.003 mm^2 10b 240MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction and correlated-reversed switching," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1382–1398, Jun. 2015.

[13] A. Gines, A. Lopez-Angulo, E. Peralias, and A. Rueda, "Description of SAR ADCs with digital redundancy using a unified hardware-based approach," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[14] A. Lopez-Angulo, A. Gines, E. Peralias, and A. Rueda, "Redundant SAR ADCs with split-capacitor DAC," in *Proc. 25th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2018, pp. 801–804.

[15] Y. Shen, H. Li, E. Cantatore, and P. Harpe, "A SAR ADC with reconfigurable delay and redundancy to relax the reference driver," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2022, pp. 11–15.

[16] D. Osipov and Y. Bocharov, "Behavioral model of split capacitor array DAC for use in SAR ADC design," in *Proc. PRIME, 8th Conf. Ph.D. Res. Microelectron. Electron.*, Jun. 2012, pp. 1–4.

[17] J. Gao, G. Li, L. Huang, and Q. Li, "An amplifier-free pipeline-SAR ADC architecture with enhanced speed and energy efficiency," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 4, pp. 341–345, Apr. 2016.

[18] S. Brenna, A. Bonetti, A. L. Lacaita, and A. Bonfanti, "A modeling environment for the simulation and design of charge redistribution DACs used in SAR ADCs," in *Proc. UKSim-AMSS 16th Int. Conf. Comput. Modeling Simulation*, Mar. 2014, pp. 562–567.

[19] G. M. Salgado, A. Dicataldo, D. O'Hare, I. O'Connell, and J. M. de la Rosa, "Behavioral modeling of SAR ADCs in simulink," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[20] A. Gines, G. Leger, and E. Peralias, "Digital non-linearity calibration for ADCs with redundancy using a new LUT approach," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 8, pp. 3197–3210, Aug. 2021, doi: 10.1109/TCSI.2021.3066886.

[21] A. K. Chowdhary, S. Srimani, S. Das, K. Ghosh, and H. Rahaman, "Estimation of non-linear effects for capacitive DAC in SAR ADC: An analytical model," in *Proc. 2nd Int. Symp. Devices, Circuits Syst. (ISDCS)*, Mar. 2019, pp. 1–5.

[22] S. B. Mashhadi and S. I. Pishbin, "Efficient modeling and analysis of switch-induced error voltage in high resolution SAR ADCs," in *Proc. 18th IEEE Int. Conf. Electron., Circuits, Syst.*, Dec. 2011, pp. 208–211, doi: 10.1109/ICECS.2011.6122250.

[23] C. Li, C.-H. Chan, Y. Zhu, and R. P. Martins, "Analysis of reference error in high-speed SAR ADCs with capacitive DAC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 82–93, Jan. 2019.

[24] J. A. Serrano, A. J. Gines, and E. Peralías, "Fast simulation of non-linear circuits using semi-analytical solutions based on the matrix exponential," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Oct. 2020, pp. 1–5.

[25] A. H. T. Chang, "Low-power high-performance SAR ADC with redundancy and digital background calibration," Ph.D. thesis, Dept. Elect. Eng. Comput. Sci., Massachusetts Inst. Technol., Cambridge, MA, USA, Jun. 2013. [Online]. Available: http://dspace.mit.edu/handle/1721.1/82177

[26] M. Nasrollahpour and S. Hamedi-Hagh, "High speed, low offset, low power differential comparator with constant common mode voltage," in *Proc. IEEE 12th Int. Conf. ASIC (ASICON)*, Oct. 2017, pp. 871–874.

[27] S.-H. Wang and C.-C. Hung, "A 0.3 V 10b 3MS/s SAR ADC with comparator calibration and kickback noise reduction for biomedical applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 3, pp. 558–569, Jun. 2020.

[28] J. Shen et al., "A 16-bit 16-MS/s SAR ADC with on-chip calibration in 55-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1149–1160, Apr. 2018.

[29] H. Zhuang, W. Cao, X. Peng, and H. Tang, "A three-stage comparator and its modified version with fast speed and low kickback," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 29, no. 7, pp. 1485–1489, Jul. 2021.

Carlos Dominguez-Matas received the M.Sc. degree in physics from the University of Seville (US), Seville, Spain, in 2001, and the Ph.D. degree in microelectronics from US in 2008.

He joined IMSE-CNM. Since 2016, he has been an Associate Professor with US. He is currently a predoctoral student at the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Seville. His current research interests include the design, modeling, and testing of CMOS analog mixed-signal circuits, high-speed high-resolution data converters with digital foreground/background calibration, and RF front ends for wireless communications.

Antonio Gines received the Ph.D. degree in microelectronics from the Universidad de Sevilla (US), Seville, Spain, in 2008.

He joined the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Seville. Since 2016, he has been an Associate Professor with US. His current research interests include the design, modeling, and testing of CMOS analog mixed-signal circuits; high-speed high-resolution data converters with digital foreground/background calibration; and RF front ends for wireless communications.

Aranzazu Otin (Member, IEEE) received the M.Sc. degree in physics and the Ph.D. degree in electronics engineering from the University of Zaragoza, Zaragoza, Spain, in 2001 and 2007, respectively.

She is currently an Associate Professor with the Department of Electronic Engineering and Communications, University of Zaragoza. Her research interests include high-performance microelectronics design, especially low-power analog and mixed-signal application-specific integrated circuit (ASIC) design, and control strategies of inverters for induction-heating applications.

Dr. Otin is a member of the Aragon Institute for Engineering Research (I3A) and the Group of Power Electronics and Microelectronics.

Valentín Gutiérrez graduated in electronic engineering, robotics and mechatronics specialized in electronic instrumentation and control from the University of Seville, Seville, Spain, in 2016, and the master's degree in microelectronics from the Instituto de Microelectrónica de Sevilla, Seville, in 2018.

He was a predoctoral student with the Instituto de Microelectrónica de Sevilla.

Gildas Leger received the Ph.D. degree from the University of Seville, Seville, Spain, in 2007.

Since 2008, he has been a Tenured Scientist at the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Seville. His research is mainly focused on two lines: the design of analog and mixed-signal circuits for harsh environments (in particular for space applications) and the development of novel test methodologies leveraging the power of machine learning tools.

Eduardo Peralias received the Ph.D. degree from the University of Seville, Seville, Spain, in 1999.

Since 2001, he has been with the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Seville, where he is currently a Tenured Scientist. His research interests are in the areas of mixed design with emphasis on ADCs, test, and design for testability of analog and mixed-signal circuits, and statistical behavioral modeling.