Class-D/DE Dual-Mode-Operation Resonant Converter for Improved-Efficiency Domestic Induction Heating System

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Abstract.

Induction heating (IH) technology is nowadays widely present in domestic appliances because of its cleanness, high efficiency, and faster heating process. All of these advantages are due to its heating process, where the pot is directly heated by the induced currents generated with a varying magnetic field. As a result, the glass where the pot is supported is not directly heated and, consequently, efficiency and heating times are improved.

Induction heating systems are based on dc-link inverters to generate the required alternating current to feed the inductor. Usually, resonant converters are used to achieve higher efficiencies and power densities. In such systems, the maximum output power and efficiency are achieved at the resonant frequency, and the switching frequency is increased to reduce the output power. As a consequence, in these converters the efficiency is also reduced in the low-medium output power range.

This paper proposes the use of the half-bridge inverter in two operating modes to achieve higher efficiency in a wide output power range. The power converter topology can be reconfigured by changing the resonant capacitors through electromechanical relays. As a consequence, the entire efficiency of the cooking process is improved with a cost-effective procedure.

I. INTRODUCTION

The main advantages of domestic induction heating technology are the reduced heating times, cleanness, higher efficiency, and the more versatile cooking surfaces [1]. Induction heaters directly heat up the vessel by means of a varying magnetic field in the range of 20 kHz to 100 kHz. This magnetic field is generated by an inductor-coil system supplied by a resonant power converter.

A cooking process can usually be divided into two parts. The first one it is known as pre-heating, and it is used to rapidly increase the vessel temperature to the desired level. Higher output power levels for a short time are used in this part. The second one consists of holding the temperature for a long time with low-medium output power levels. As a result, the efficiency of low-middle power levels has a significant impact on the efficiency of the whole cooking process.

The resonant converters used to supply the inductor-pot system can be classified as a function of the number of active devices, which is directly related with the final cost. For low-cost appliances and low output power levels, the one switch topology (1-SW) is the most used [2]. The half-bridge inverter is the most used topology [1], [3-6] for medium-high output power levels due to its high efficiency and low voltage stress across the switching devices. Finally, for higher output power levels, the full-bridge inverter is used [7-9].

Considering the aforementioned alternatives, most of the commercial solutions use the half-bridge ZVS series resonant inverter (class D operation mode) because of its robustness and control simplicity [10-15]. For this topology and operation mode, the maximum output power occurs at the resonant frequency, yielding to the maximum efficiency. However, lower efficiency is achieved at low-medium output power levels due to the higher switching frequency [7], [10], [16]. Usually, pulse density modulation (PDM) is applied to keep high efficiency in the low output power range [10], [17], [18]. However, it increases flicker emissions, which can compromise the appliance electromagnetic compatibility (EMC). For this reason, PDM is usually applied at high switching frequencies, i.e. low output power, increasing switching losses. To overcome this limitation, a dual-mode-operation resonant converter is proposed [19] which further improves efficiency in the low output power range due to the reduced switching losses. Class-D half-bridge converter is used in the high output power range, whereas class-DE half bridge converter [20], [21] is used in the low to medium output power range. The combination of these operation modes achieves high efficiency levels in a wider range of output power levels. In this paper, the proposed converter is analytically studied and additional implementation and experimental results are given to prove the feasibility of the proposed converter.

This paper is organized as follows. Section II describes the proposed dual-mode resonant converter. Section III performs an efficiency analysis, while Section IV introduces the modulation strategies for the proposed hybrid converter. Finally, the experimental results are shown in Section V and the main conclusions of this paper are outlined in Section VI.

II. DUAL MODE RESONANT CONVERTER

The series resonant half-bridge applied to induction heating operates at switching frequencies higher than the resonant frequency to achieve zero voltage switching (ZVS) conditions [3]. To reduce switch-off switching losses, a lossless snubber network (C_s) is added. Typically, class-D operation mode implies that the snubber capacitor C_s is much lower than the resonant capacitor C_r [22]. However, if the class E conditions are achieved, i.e. ZVS and zero voltage derivative switching (ZVDS) at the turn-off, the operation mode is known as class DE. This operation mode ensures zero switching losses, but the maximum output power is lower than in class D operation mode. Considering this, a dual-mode resonant converter implementation is proposed in order to improve the efficiency in the whole operating range. Fig. 1 shows the proposed implementation scheme, where electromechanical switches SPST 1 and 2 allow varying the snubber and resonant capacitance in order to change the operation mode. The following subsections details the design procedure for both operation modes, where the superscript D denotes the class-D operation mode and the superscript DE is used for the class-DE operation mode. The operation modes of the half-bridge inverter, including class-D and class-DE operation, are shown in Fig. 2.

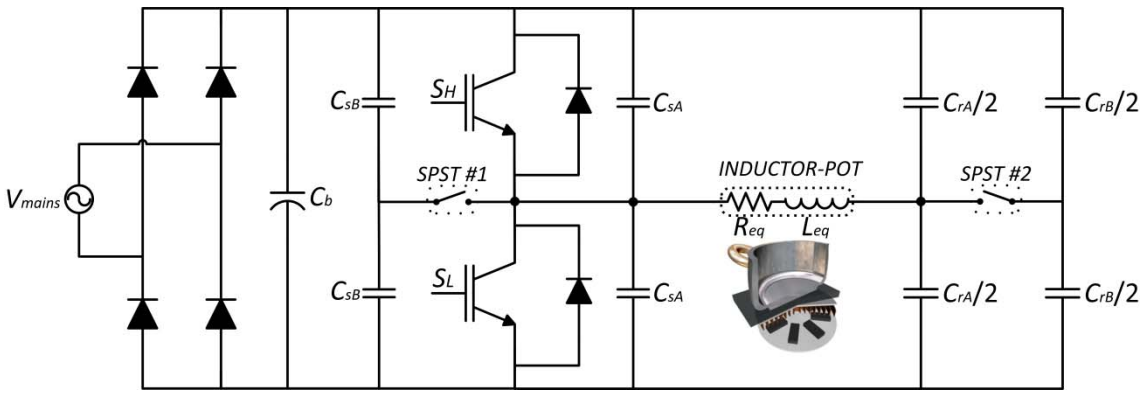


Fig. 1. Dual-mode series resonant half-bridge schematic

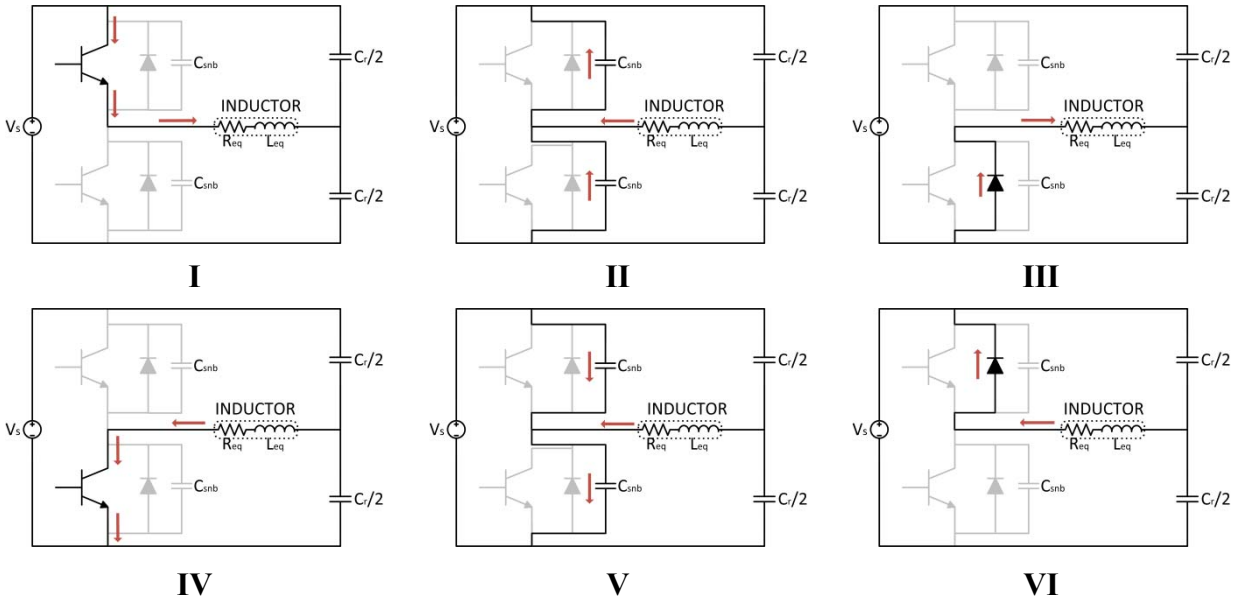


Fig. 2. Main circuit states of the half-bridge series resonant inverter.

During the first state (I), the load current is positive and it is supplied by the high-side transistor. When high-side transistor is deactivated, the switch-off current is used to charge/discharge the snubber capacitors (state II), i.e. the high-side snubber capacitor is charged to the supply voltage whereas the low-side snubber capacitor is discharged. In state III, the load current is also positive, and thus, it is supplied by the low-side diode. When the load current becomes negative (state IV), it is supplied by the low-side transistor. As soon as the low-side transistor is deactivated (state V), the load current charges the low-side snubber capacitor to the supply voltage whereas the high-side snubber capacitor is discharged. When both snubber capacitors are charged/discharged, the negative load current flows through the high-side diode (state VI). Finally, when the load current reaches zero, the load current is supplied by upper transistor (state I). Class-D operation mode uses configurations I to VI, whereas in class-DE operation mode the configurations II and V, i.e. snubber capacitors charge/discharge, are extended avoiding the use of configurations III and VI, diode conduction.

A. Class-D operation mode

The output power in the class-D inverter can be determined using Fourier-transform as expressed in the following expression [3].

$$P_o^D = \sum_{h=1}^{\infty} R_{eq} I_{o,\,rms}^2 = \sum_{h=1}^{\infty} R_{eq} \frac{V_{0,\,rms}^2}{R_{eq}^2 + (h2\pi f_{sw} L_{eq} - \frac{1}{h2\pi f_{sw} C_r^D})} = \\ = \sum_{h=1}^{\infty} \frac{2R_{eq} V_{mains}^2 / (h\pi)^2}{R_{eq}^2 + (h2\pi f_{sw} L_{eq} - \frac{1}{h2\pi f_{sw} C_r^D})}, \quad (1)$$

where R_{eq} and L_{eq} are the inductor-pot system electrical equivalent, f_{sw} is the switching frequency, and h is the harmonic number. The maximum output power ($P_{o,\max}^D$) occurs at resonant frequency. As a consequence, the first harmonic approximation can be assumed and the load resistance at this frequency must satisfy [3]

$$R_{eq} \le \frac{2V_{mains}^2}{\pi^2 P_{o,\max}^D}. \quad (2)$$

Besides, the resonant capacitor can be determined as

$$C_r^D = \frac{1}{L_{eq}(2\pi f_{sw})^2}. \quad (3)$$

The snubber capacitance $C_s^D = C_{sA}$ is used to decrease turn-off switching losses. This capacitance must be charged/discharged during dead time between transistor activation with the output current. As a consequence, a small value of capacitance must be used to ensure the charge/discharge to achieve ZVS in a wide range of operating conditions [3].

B. Class DE operation mode

The resonant inverter under class-DE operation mode must be designed to supply the required low-medium output power for the same inductor, i.e. same R_{eq}, L_{eq}. Resonant and snubber capacitors are therefore modified, being $C_r^{DE} = C_{rA} + C_{rB}$ and $C_s^{DE} = C_{sA} + C_{sB}$. The load resistance is determined by the maximum output power required in the class-D operation mode. As a consequence, the maximum output power when operating in class-DE operation mode is strongly dependent of the duty cycle *D*.

$$P_{o,\max}^{DE} = \frac{V_{mains}^2}{2\pi^2 R_{eq}}\left(1-\cos\left(2\pi D\right)\right). \tag{4}$$

Besides, the snubber capacitance can now be calculated as follows

$$C_{snb}^{DE} = \frac{1+\cos(2\pi D)}{\left(2\pi\right)^2 R_{eq} f_{sw}}. \tag{5}$$

The resonant frequency in the class DE operation mode, f_r^{DE}, determined by the inductor and the resonant capacitors, can now be calculated as

$$f_r^{DE} = \frac{f_{sw}}{2}\left(\sqrt{\left(\frac{\tan(\alpha)}{Q_{eq}}\right)^2 + 4} - \frac{\tan(\alpha)}{Q_{eq}}\right), \tag{6}$$

where $Q_{eq} = 2\pi f_{sw} L_{eq} / R_{eq}$ is the inductor power quality factor at the switching frequency, and α is the phase lag between current and voltage, calculated as

$$\tan\left(\alpha\right) = \frac{\pi\left(1-2D\right)+\sin\left(2\pi D\right)\cos\left(2\pi D\right)}{\sin^2\left(2\pi D\right)}. \tag{7}$$

Consequently, the resonant capacitor for the class-DE operation mode is given by

$$C_r^{DE} = \frac{1}{(2\pi f_r^{DE})^2 L_{eq}}. \tag{8}$$

As the Class DE operation mode is used to achieve the lower output power levels, both resonant and snubber capacitor use higher values than in the Class D operation mode. Therefore, the electromechanical relays SPST 1 and 2 are used to increase this capacitance for the Class DE operation mode.

III. EFFICIENCY ANALYSIS

Power losses in the converter can be divided into two terms: conduction and switching losses. Both of them are caused by the non-idealities in the switching devices: non-zero switching times and non-zero on resistance. As a result, switching waveforms in the converter have a direct impact in the entire converter losses.

As small snubber capacitors are used in the Class D operation mode, the output current can be considered constant during the charge intervals. As a result, the voltage across the device during the switching becomes linear:

$$v_{CE}^{D}(t) = \frac{I_{C,off}}{2C_{snb}^{D}} t, \ \left(0 \le t \le T_{snb}^{D}\right), \tag{9}$$

where I_C denotes the switch-off current in the switching devices. Moreover, the required time to charge/discharge the snubber capacitance can be calculated as

$$T_{snb}^{D} = V_S \frac{2C_{snb}^{D}}{I_{C,off}}. \tag{10}$$

In the case of the class-DE operation mode, the load current is modeled as a linear function that starts in $I_{C,off}$ and ends at zero

$$i_o(t) = I_{C,off}\left(1 - \frac{t}{T_{snb}^{DE}}\right), \ \left(0 \le t \le T_{snb}^{DE}\right), \tag{11}$$

as a result, the switch voltage is

$$v_{CE}^{DE}(t) = \frac{1}{2C_{snb}^{DE}} \int i_o(t)dt = \frac{I_{C,off}}{2C_{snb}^{DE}}\left(t - \frac{t^2}{2T_{snb}^{DE}}\right), \ \left(0 \le t \le T_{snb}^{DE}\right). \tag{12}$$

Where the class-E switching conditions, i.e. ZVS and ZVDS are achieved in the proposed voltage equation (12). The time required to charge/discharge the snubber capacitors T_{snb}^{DE} can be directly obtained from (12), yielding

$$T_{snb}^{DE} = V_S \frac{4C_{snb}^{DE}}{I_{C,off}}. \tag{13}$$

The proposed analytical model for the switching intervals have been validated with simulation results using SPICE simulation tool. The main simulation results are shown in Fig. 3, showing a good agreement with the proposed model.

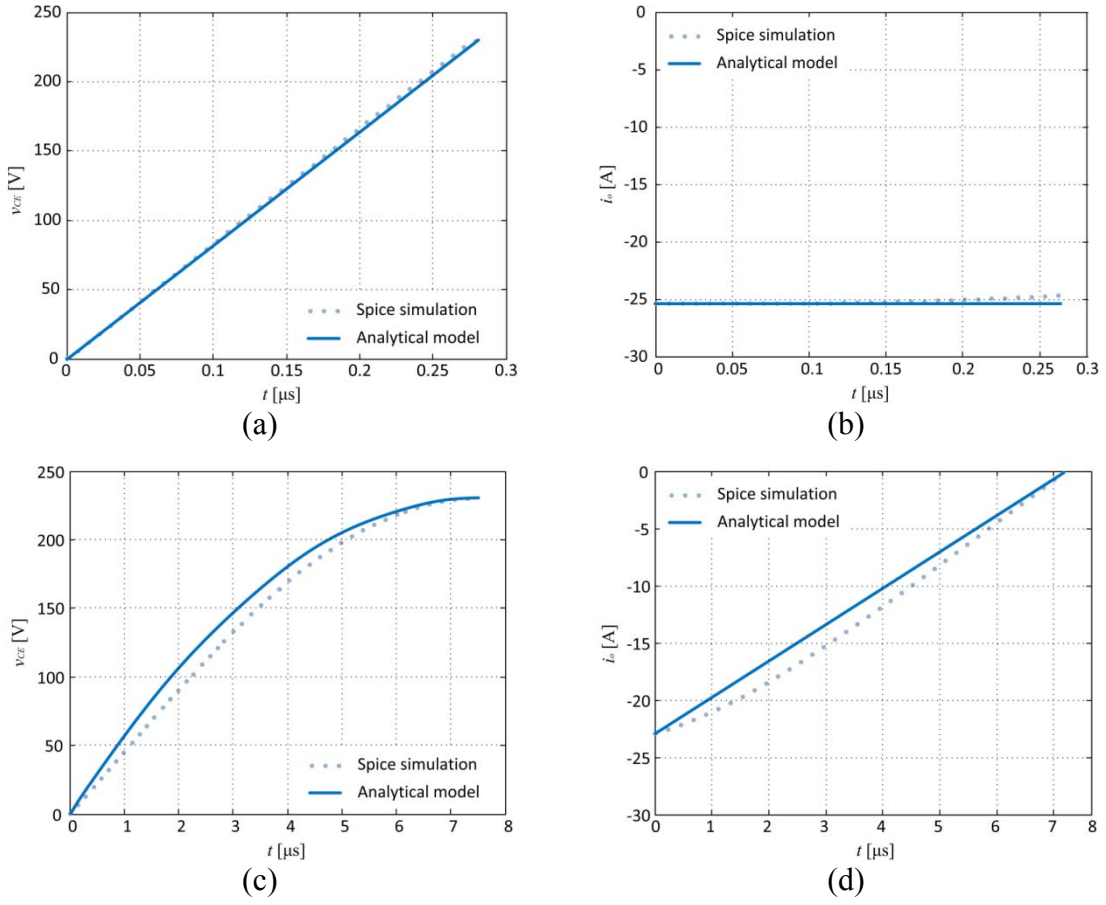


Fig. 3. Simulation and proposed analytical results. Voltage (a) and current (b) results for class-D operation mode using 15-nF snubber capacitor at 32 kHz. Voltage (c) and current (d) for class-DE operation mode using 464-nF snubber capacitor at 20 kHz..

Main differences between the SPICE and the analytical model are due to the linear current assumption. These errors have a reduced impact in the output power and conduction losses computation and provide a useful method to predict the required dead-time to ensure the correct snubber charge/discharge with reduced computation effort.

A. Conduction losses

Conduction losses can be calculated using the average and rms values of current through the devices. Since a bidirectional switch is used, there are two components in each switch to compute conduction losses, the IGBT ($P_{ON,IGBT}$) and the antiparallel diode ($P_{ON,DIODE}$). The total conduction losses, P_{ON}, therefore results

$$P_{ON} = 2\left(P_{ON,IGBT} + P_{ON,DIODE}\right), \tag{14}$$

Where each conduction term is

$$P_{ON} = r_{ON} I_{rms}^2 + v_{ON} I_{avg}, \tag{15}$$

were the on-resistance and collector-to-emitter saturation voltage are r_{ON} and v_{ON}, respectively. The block composed of the switching device, the antiparallel diode, and the snubber capacitance must provide the entire load current (Fig. 4). As a result, positive current values are supplied by the main transistor, whereas negative current values are supplied by the snubber capacitor and the antiparallel diode. Consequently, higher snubber capacitance implies lower antiparallel diode conduction and, as a result, lower diode conduction losses. Moreover, in the case of class-DE operation mode, the entire negative current is provided by the snubber capacitance, and antiparallel diode does not conduct.

In order to compute the average and rms value of current, it is required to obtain the conduction time in each device. Total conduction time in each switching device is (Fig. 5)

$$T_{on} = T\left(1 - 2T_{snb}\right), \tag{16}$$

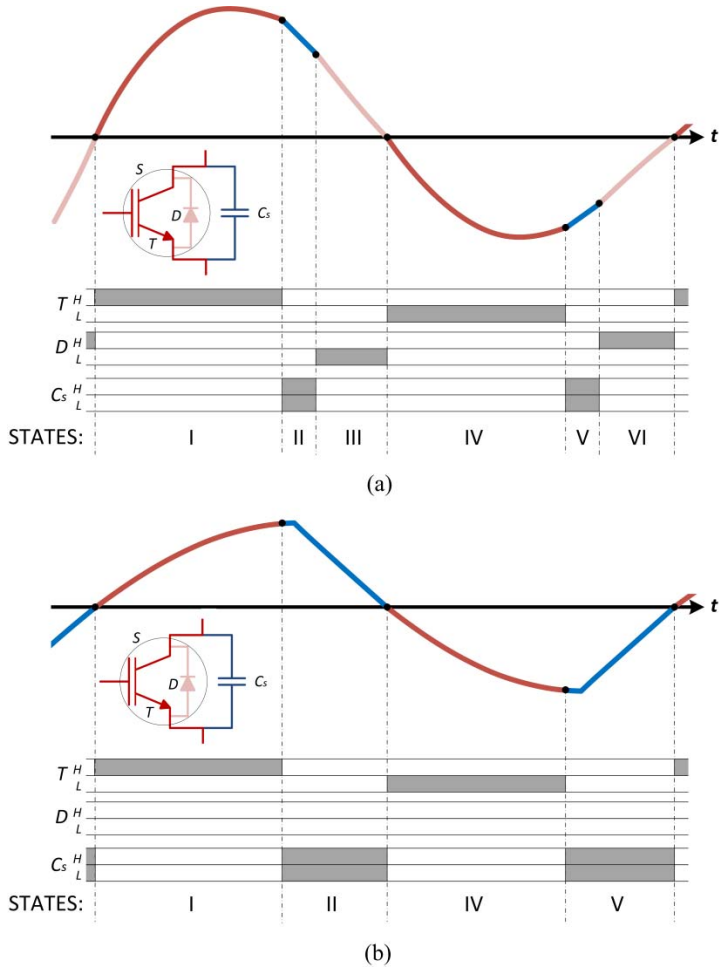


Fig. 4. Waveforms of the hybrid converter: output current and device activation. Class D operation mode (a) and class DE (b)

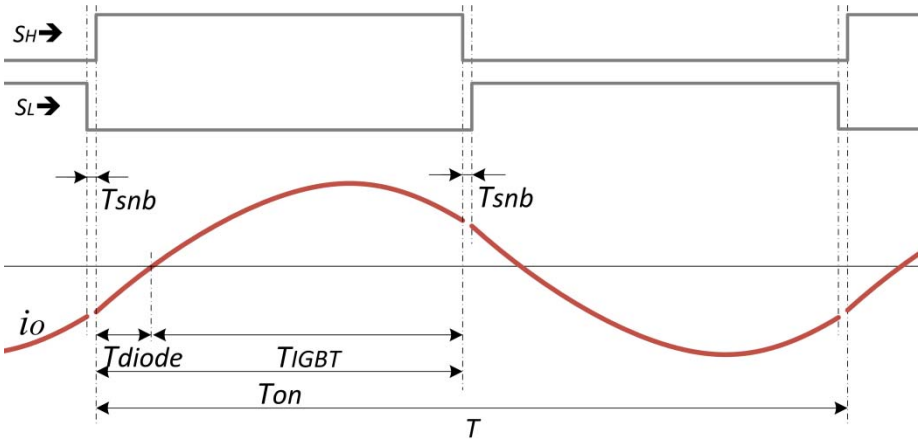


Fig. 5. Main current waveform and timing in the class-D operation mode.

In the case of class-D operation mode, the snubber current can be considered constant and as a result, switch-on and switch-off currents have the same opposite value, yielding that load current is [23]

$$i_o^D(t) = e^{-\xi t}\left(M_1^D \sin(\omega_n^D t) + M_2^D \cos(\omega_n^D t)\right), \tag{17}$$

where

$$\xi = R/2L_{eq},\ \omega_o^D = 1/\sqrt{L_{eq}C_r^D},\ \omega_n^D = \sqrt{\left(\omega_o^D\right)^2 - \left(\xi\right)^2}. \tag{18}$$

By applying boundary conditions, load current results

$$\begin{cases} i_o^D(t=0) = -I_{C,off} \Rightarrow M_2^D = -I_{C,off} \\ i_o^D(t=T_{on}) = I_{C,off} \Rightarrow M_1^D = I_{C,off}\left(\dfrac{e^{\xi T_{on}}}{\sin(\omega_n^D T_{on})} + \dfrac{1}{\tan(\omega_n^D T_{on})}\right), \end{cases} \tag{19}$$

As a result, the diode on time is

$$i_o^D(t=T_{diode})=0 \Rightarrow T_{diode}=\frac{1}{\omega_n^D}a\tan\left(\frac{-M_2^D}{M_1^D}\right)$$
$$\Leftrightarrow T_{diode}=\frac{1}{\omega_n^D}a\tan\left(\left(\frac{e^{\xi T_{on}}}{\sin(\omega_n^D T_{on})}+\frac{1}{\tan(\omega_n^D T_{on})}\right)^{-1}\right). \quad (20)$$

The transistor on time is $T_{IGBT}=T_{on}-T_{diode}$. Consequently, average currents result

$$I_{avg,diode}^D=\frac{I_{C,off}}{T\left(\omega_o^D\right)^2}\left[\omega_n^D\left(\frac{e^{-\xi T_{diode}}}{\sin(\omega_n^D T_{diode})}-\frac{1}{\tan(\omega_n^D T_{diode})}\right)+\xi\right], \quad (21)$$

$$I_{avg,IGBT}^D=\frac{I_{C,off}}{T\left(\omega_o^D\right)^2}\left[\omega_n^D\left(\frac{e^{\xi T_{IGBT}}}{\sin(\omega_n^D T_{IGBT})}-\frac{1}{\tan(\omega_n^D T_{IGBT})}\right)-\xi\right]. \quad (22)$$

and the rms currents are

$$I_{rms,diode}^D=\sqrt{\frac{I_{C,off}^2}{4\xi T\left(\omega_o^D\right)^2\sin(\omega_n^D T_{diode})}\left[\frac{\left(\omega_o^D\right)^2-\left(\omega_o^D\right)^2 e^{-2\xi T_{diode}}}{\sin(\omega_n^D T_{diode})}+\xi\left(\frac{\xi}{tg(2\omega_n^D T_{diode})}-\omega_n^D\right)\right]}, \quad (23)$$

$$I_{rms,IGBT}^D=\sqrt{\frac{I_{C,off}^2}{4\xi T\left(\omega_o^D\right)^2\sin(\omega_n^D T_{IGBT})}\left[\frac{\left(\omega_o^D\right)^2-\left(\omega_o^D\right)^2 e^{2\xi T_{IGBT}}}{\sin(\omega_n^D T_{IGBT})}+\xi\left(\frac{\xi}{tg(2\omega_n^D T_{IGBT})}-\omega_n^D\right)\right]}. \quad (24)$$

The proposed analytical model has been verified and compared using Spice simulator. The results are shown in Fig. 6 for the complete output power range in the class-D operation mode, obtaining a good agreement between analytical and simulation results.

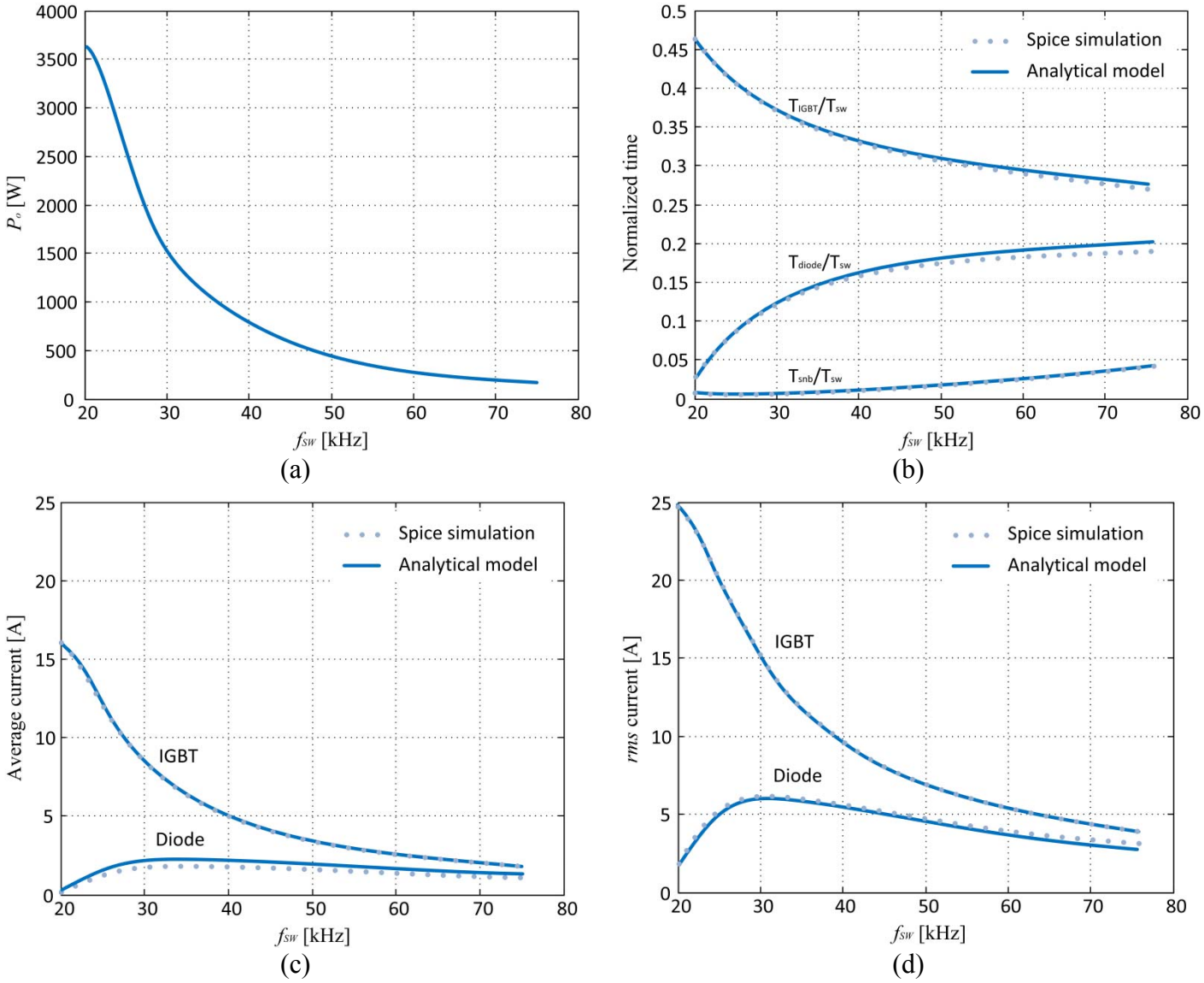


Fig. 6. Simulation versus Spice results: (a) output power; (b) normalized IGBT, diode and snubber times; (c) average currents in the IGBT and diode; (c) rms current in the IGBT and diode. Results for R_{eq}=2.89 Ω, L_{eq}=29.6 µH, resonant and snubber capacitor 2.04 µF and 15 nF, respectively.

In the case of the class-DE operation mode, the diode does not conduct and, therefore, $T_{diode}=0,\ T_{IGBT}=T_{on}$. By applying the same procedure, the average and rms values of current results

$$I_{avg,IGBT}^{DE}=\frac{I_{C,off}}{T\left(\omega_o^{DE}\right)^2}\left[\omega_n^{DE}\left(\frac{e^{\xi T_{on}}}{\sin(\omega_n^{DE}T_{on})}-\frac{1}{\tan(\omega_n^{DE}T_{on})}\right)-\xi\right], \tag{25}$$

$$I_{rms,IGBT}^{DE} = \sqrt{\frac{I_{C,off}^2}{4\xi T\left(\omega_o^{DE}\right)^2 \sin(\omega_n^{DE} T_{on})}\left[\frac{\left(\omega_o^{DE}\right)^2 - \left(\omega_o^{DE}\right)^2 e^{2\xi T_{on}}}{\sin(\omega_n^{DE} T_{on})} + \xi\left(\frac{\xi}{tg(2\omega_n^{DE} T_{on})} - \omega_n^{DE}\right)\right]}, \quad (26)$$

where $\omega_o^{DE} = 1/\sqrt{L_{eq} C_r^{DE}}$, $\omega_n^{DE} = \sqrt{\left(\omega_o^{DE}\right)^2 - (\xi)^2}$.

Consequently, the current distribution in the class-DE operation mode is partly derived to the snubber capacitor, reducing conduction losses (Fig. 7).

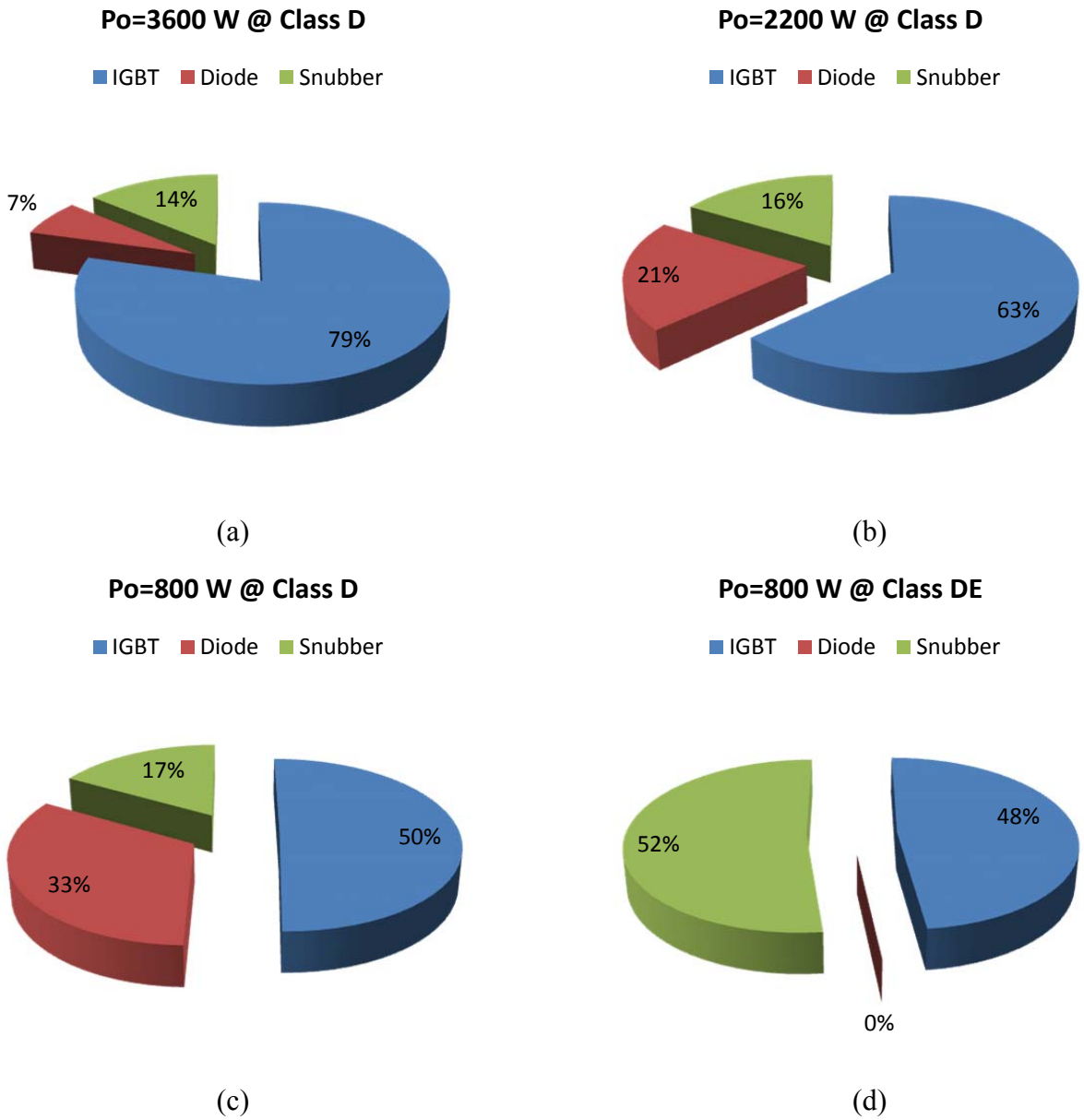


Fig. 7. Rms current dirstribution for class-D operation mode: (a) maximum output power, 3.6 kW, (b) nominal power (2.2 kW); minimum power (800 W) (c). Current distribution for class-DE at 800 W (d).

B. Switching losses

As the devices voltage waveforms in the switching transitions have been obtained (9), (12), switching losses can be directly calculated by means of using a piecewise switch-off current model [24], where the switch-off current is defined for IGBT devices by means of the tail factor β, and *fall* and *tail* intervals, t_f, t_t, respectively

$$i_{C,off}(t)=\begin{cases} I_{C,off}\left(1-\dfrac{\beta}{t_f}t\right), & \left(0\le t<t_f\right) \\ I_{C,off}(1-\beta)\left(1-\dfrac{t-t_f}{t_t}\right), & \left(t_f\le t\le t_f+t_t\right) \end{cases}. \tag{27}$$

Thus, the instantaneous switching losses can be obtained. Fig. 8 shows results for both operation modes delivering 800-W output power

$$p_{SW}^{D}(t)=\begin{cases} \dfrac{I_{C,off}^2}{2C_{snb}^{D}}\left(1-\dfrac{\beta}{t_f}t\right), & \left(0\le t\le t_f\right) \\ \dfrac{I_{C,off}^2(1-\beta)}{2C_{snb}^{D}}\left(1-\dfrac{t-t_f}{t_t}\right), & \left(t_f<t\le t_f+t_t\right) \end{cases}, \tag{28}$$

$$p_{SW}^{DE}(t)=\begin{cases} \dfrac{I_{C,off}^2}{2C_{snb}^{DE}}\left(1-\dfrac{\beta}{t_f}t\right)\left(t-\dfrac{t^2}{2T_{snb}^{DE}}\right), & \left(0\le t\le t_f\right) \\ \dfrac{I_{C,off}^2(1-\beta)}{2C_{snb}^{DE}}\left(1-\dfrac{t-t_f}{t_t}\right)\left(t-\dfrac{t^2}{2T_{snb}^{DE}}\right), & \left(t_f<t\le t_f+t_t\right) \end{cases}. \tag{29}$$

Therefore, the switching losses energy in each operation mode results

$$E_{SW}^{D}=\frac{I_{C,off}^2}{2C_{snb}^{D}}\left[t_f\left(1-\frac{\beta}{2}\right)+\frac{t_t}{2}(1-\beta)\right] \tag{30}$$

$$E_{SW}^{DE}=\frac{I_{C,off}^2}{48C_{snb}^{DE}T_{snb}^{DE}}\left[\begin{array}{l} 4t_f^2\left(T_{snb}^{DE}(3-2\beta)-t_f\left(1-\dfrac{3}{4}\beta\right)\right)+ \\ t_t(1-\beta)\left(6t_f^2+t_t^2+4t_ft_t-4T_{snb}^{DE}\left(3t_f+t_t\right)\right) \end{array}\right] \tag{31}$$

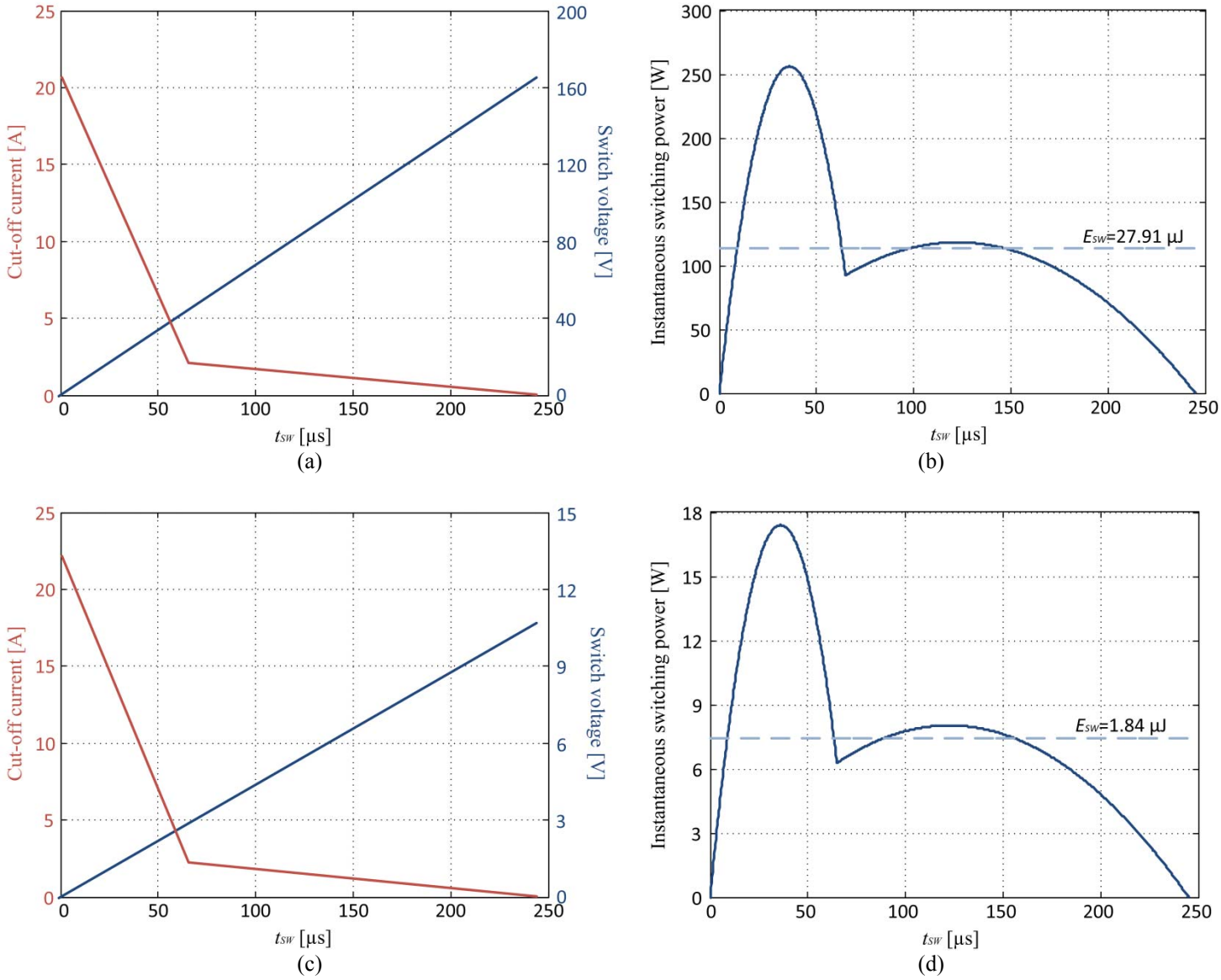


Fig. 8. Switching losses simulation for Class D (a, b) using 15 nF snubber capacitor and a cut-off current of 20.63 A at 800 W output power, yielding 328-ns snubber time. Results for Class DE (c, d) using 265 nF capacitor, a cut-off current of 22.7 A at 500 w output power, yielding 10.72-µs snubber time. Simulation results for β=0.9, t_f=65 ns, t_t= 180 ns.

Finally, switching losses result

$$P_{SW} = 2 f_{SW} E_{SW}. \tag{32}$$

IV. MODULATION STRATEGIES AND DIGITAL IMPLEMENTATION

A. Modulation strategies

According to the selected operation mode, the hybrid converter uses two modulation strategies. On the one hand, the class-D operation mode supplies the high output power range and, therefore, the square wave modulation (SW) is used [10]. Consequently, the maximum output power is achieved at the resonant frequency, and lower power levels can be obtained by increasing the switching frequency. As a result, the ZVS switching-on condition is achieved in the entire power range for this operation mode. The output power variation as a function of the switching frequency is described in (1).

On the other hand, when lower output powers are required, the system changes resonant and snubber capacitors to operate in the class-DE operation mode. For a given load, that is, for a given inductor-pot system, the class-DE optimal switching conditions are only achieved for a single operation point, i.e. a switching frequency, a duty cycle, and a phase lag. Thus, lower power levels are achieved using a pulse density modulation [7], [17], PDM, in the output power. By denoting T_{DPM} as the total pulse density period, the on-time duty cycle for the PDM is defined as D_{PDM} (Fig. 9). Consequently, the output power varies linearly with the PDM duty cycle

$$P_o^{DE} = D_{PDM} P_{o,\max}^{DE}, \; 0 \le D_{PDM} \le 1, \tag{33}$$

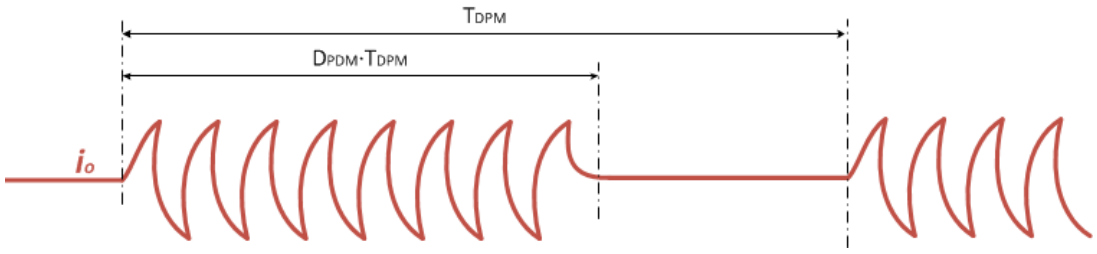


Fig. 9. Pulse density modulation (PDM): output current and control parameters.

The total PDM time, T_{PDM}, is chosen according to flicker requirements to ensure that EMC requirements are fulfill [10]. Fig. 10 shows both the modulation scheme and the output power variation for both of them. The maximum output power, 3.3 kW, is achieved close to resonance in the class-D operation mode and the output power threshold to switch to the class-DE operation mode is 800 W. The switching frequency for the class-DE operation mode is reduced to 20 kHz, reducing therefore the switching losses.

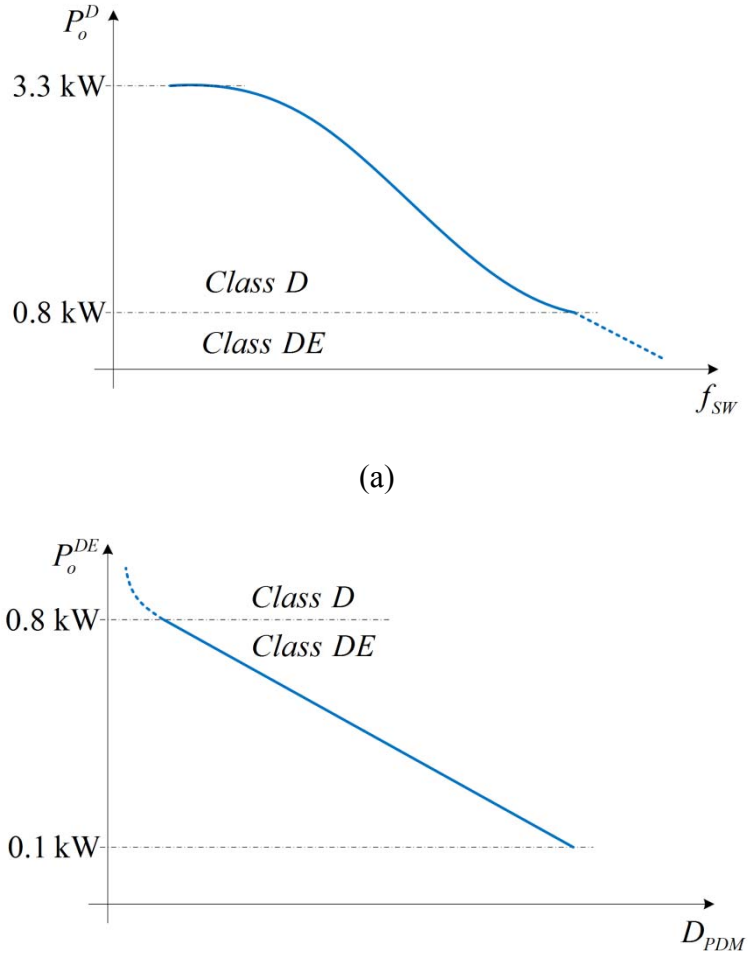


Fig. 10. Output power variation for class-D (a) and class-DE (b) operation modes. Power curve as a function of switching frequency in the class-D operation mode (a). Power curve as a function of the PDM duty cycle for the class-DE operation mode (b).

B. Digital control implementation

The proposed system is digitally controlled by a microcontroller and an application-specific integrated circuit (ASIC) [25]. The control algorithm as well as the modulation parameters is computed in the microcontroller, while some high computation tasks, such us the digital modulator, the current measurement circuits, and output power computations are included in the ASIC. Main logic level schematic diagram is shown in Fig. 11.

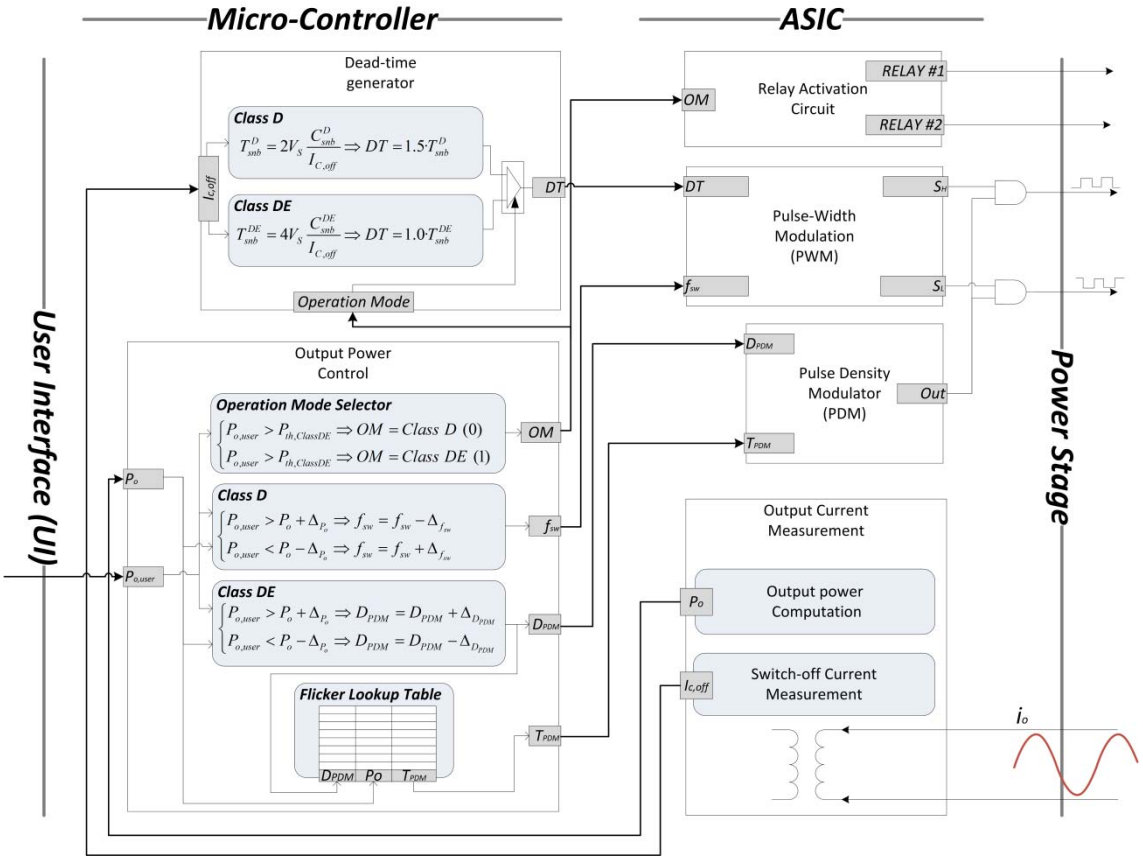


Fig. 11. Logic implementation in the proposed hybrid converter.

The output power set-point is defined by the user through a user interface (UI), which is controlled by the microcontroller. The operation mode depends on the power level, i.e. power levels higher than 800 W are supplied using the class-D operation mode, whereas

the class-DE operation mode is used for lower power levels. For the class-D operation mode, the control algorithm increases or reduces a fixed switching frequency quantity, $\Delta_{f_{SW}}$, if the measured output power differs from the set-point output power. On the other hand, for the Class DE operation mode, D_{PDM} is increased or reduced based on the output power set-point and the measured output power. However, in order to fulfill the EMC requirements, the flicker time, $T_{PDM,}$ must be in consideration. A lookup table is integrated in the memory of the microcontroller to compute the required flicker time to accomplish the standards proposed by the International Electrotechnical Commission (IEC), considered by the IEEE workgroup p1453 [26]. In addition, the required dead-time to ensure the correct snubber calculation is also performed by the microcontroller, using equations (10), (13), for the Class D and Class DE operation mode, respectively.

On the one hand, the ASIC generates the gating signals, as well as measures output current to perform the required calculations. Depending on the operation mode, the ASIC activates or deactivates the snubber and resonant capacitor relays to change the operation mode. A pulse width modulator (PWM) is also implemented, and the transistor activation signals are generated as a function of the switching frequency and the duty cycle. Besides, a Pulse Density Modulator (PDM) is also included to control the output power in the Class DE operation mode. Finally, the load current is also measured to obtain the output power measurement and the switch-off current, used to compute the correct dead-time in the microcontroller.

V. EXPERIMENTAL RESULTS

A prototype based on a commercial electronic board has been built to verify the proposed converter. Power levels from 0.8 kW up to 3 kW are supplied using the class-D operation mode, whereas class-DE operation mode is used for power levels lower than 800 W.

The inductor must be designed to ensure the maximum power level up to 3 kW for 230-V power supply voltage. Using (2), the inductor resistance must be lower than 3.26 Ω. The lower switching frequency was set to 20 kHz to avoid acoustic noise. The equivalent inductor-pot system resistance and inductance are 2.89 Ω and 29.6 μH, respectively. The measurements have been performed by means of a precision LCR meter from Agilent (E4980A). Consequently, the maximum available output power is

$$P_o \leq \frac{2V_{mains}^2}{\pi^2 R_{eq}} = \frac{2 \cdot 230^2}{\pi^2 2.86} = 3.7\ kW \tag{34}$$

Using (3), the resonant capacitor for the Class D operation mode results 2139 nF. On the other hand, the snubber capacitance was set to 15 nF in order to reduce switching losses and to allow a wider output power range.

For the Class DE operation mode, the duty cycle results 24.09% at 20 kHz switching frequency. Consequently, the snubber capacitor (5) is 463.29 nF. The resonant frequency (6) is 10.79 kHz to achieve the desired output power level, and the phase lag between current and voltage is α=59.39º. Finally, the resonant capacitor (8) results 7350 nF. A small value DC-Link capacitor, C_b, is used to ensure an input power factor close to one. Table I summarizes the selected values according to the proposed design method and using standard values.

TABLE I
PROTOTYPE PARAMETERS

	COMPONENTS	Class D	Class DE
f_{SW}	Switching frequency	20 kHz to 40 kHz	20 kHz
D	Duty cycle	50 %	24%
C_r	Resonant capacitor	2.14 µF	7.35 µF
C_{snb}	Snubber Capacitor	15 nF	464 nF
C_b	DC-Link capacitor	2x3.3 µF	
R_{eq}	Inductor-pot equivalent resistance	2.89 Ω	
L_{eq}	Inductor-pot equivalent inductance	29.6 µH	

The proposed prototype implementation board is shown in Fig. 12

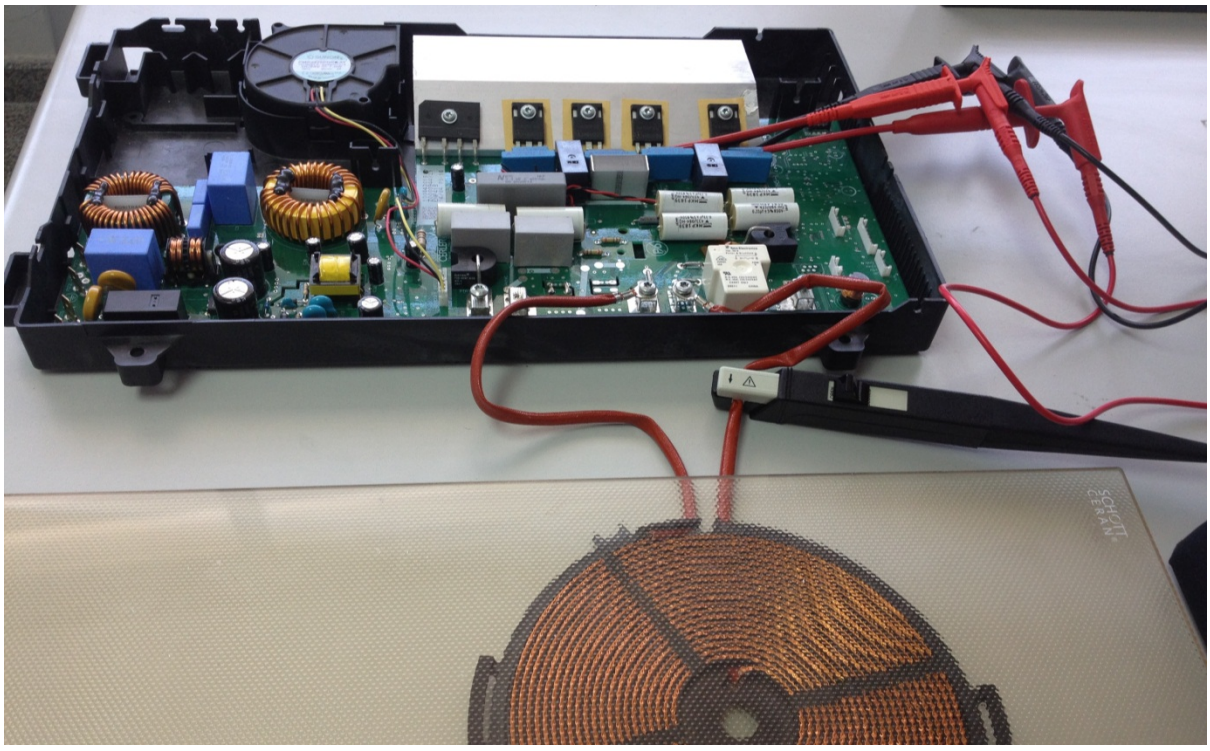
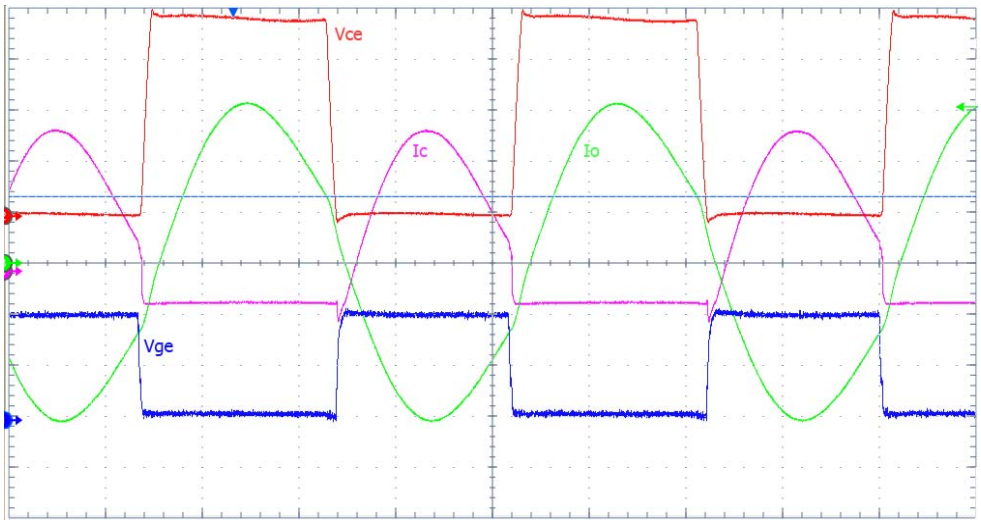
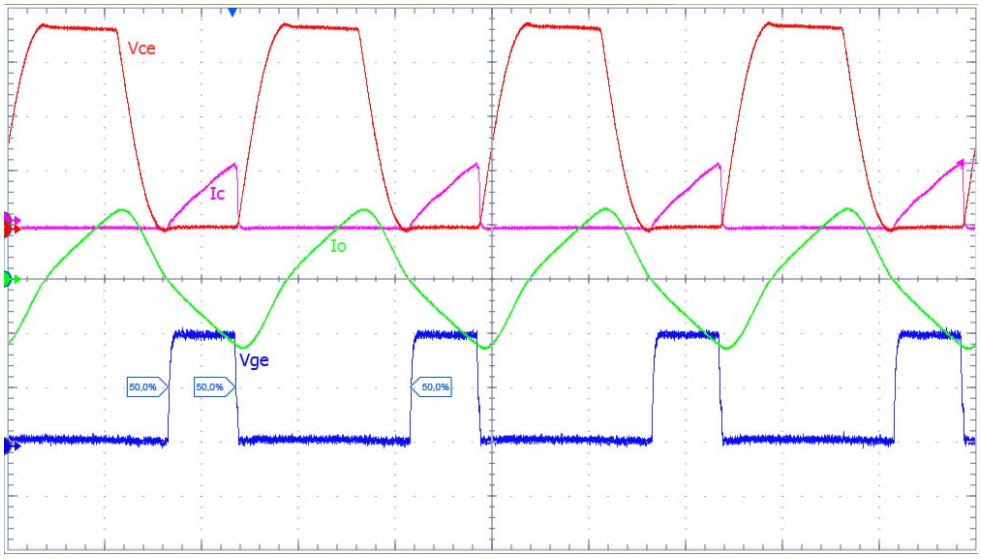


Fig. 12. Experimental setup for the proposed hybrid converter.

Fig. 13 shows the main waveforms for the class-D operation mode (a) and the class-DE operation mode (b). The converter shows a correct performance and the stray elements added by the electromechanical switches do not affect the converter operation. Therefore, the experimental results are in good agreement with the theoretical ones.



(a)



(b)

Fig. 13. Power converter main waveforms: collector-emitter voltage (*Vce*), 100 V/div; collector current (*Ic*), 10 A/div; output current (*Io*), 10 A/div; gate to-emitter voltage (*Vge*),10 V/div. Time: 1.25 µs/div. Class-D (a) and Class-DE (b) operation modes.

Efficiency in both operation modes have been measured using the power analyzer YOKOGAWA PZ-400 as the ratio between the input power and the power delivered to the load (Fig. 14). These results show that the class-D operation mode efficiency decreases as the switching frequency is increased when the square-wave control (SW) is applied i.e. lower output power range. The class-D operation mode operating with pulse density modulation (PDM) [7], [18] is usually applied when switching frequency increases to reduce switching losses (frequency limit, FL [10]), yielding a power losses reduction in the lower output range. However, the class-DE operation mode proposed in this paper obtains a significantly higher efficiency due to the switching and conduction losses reduction. The combination of both operation modes ensures high efficiency in the complete output power operation range.

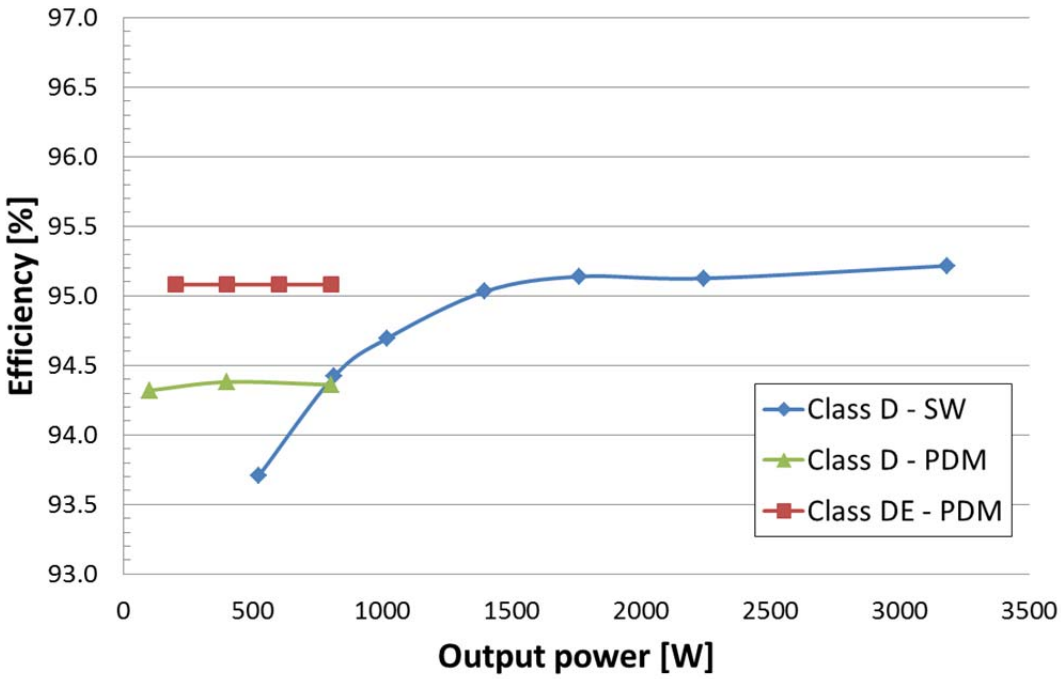


Fig. 14. Measured efficiency comparison for the proposed converter operating in class-D SW and class-DE PDM operation, and the current class D PDM operation.

VI. CONCLUSIONS

In this paper, a novel reconfigurable series resonant inverter topology is proposed in order to improve the efficiency in the whole operating range. It is based on a dual-mode resonant converter where the class-D and class-DE operation modes are combined to optimize the efficiency. The analytical results have been verified by means of an experimental prototype. As a result, the presented dual-mode topology is proposed as a cost-effective implementation to improve the overall converter efficiency.

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