High Efficiency Ac-Ac Power Electronic Converter Applied to Domestic Induction Heating

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Abstract.

This paper presents the analysis and design of a new ac-ac resonant converter applied to domestic induction heating. The proposed topology, based on the half-bridge series resonant inverter, uses only two diodes to rectify the mains voltage. The proposed converter can operate with zero voltage switching during both swith-on and switch-off transitions. Moreover, this topology doubles the output voltage and, therefore, the current in the load is reduced for the same output power. As a consequence, the converter efficiency is significantly improved.

The analytical and simulation results have been verified by means of a 3600-W induction heating prototype. An efficiency study has been carried out, obtaining values higher than 96%.

I. INTRODUCTION

Induction heating appliance market is increasing due to its fastest heating time and efficiency. Domestic induction hobs are now becoming a standard option, especially in Asia and Europe.

The principle of operation is based on the generation of a variable magnetic field by means of a planar inductor below a metallic vessel [1], [2]. The mains voltage is rectified and after that an inverter provides medium frequency current to feed the inductor. The usual operating frequency is higher than 20 kHz to avoid the audible range and lower than 100 kHz to reduce switching losses. The most used device is the IGBT because of the operating frequency range and the output power range, up to 3 kW. Nowadays, most designs use the half-bridge series resonant topology because of its control simplicity and high efficiency [3-6].

In the past, several ac-ac topologies have been proposed to simplify the converter and improve the efficiency [7-9]. Considering the induction heating application, several resonant matrix converters featuring MOSFETs [10], [11], IGBTs [12], or RB-IGBTs [13], [14] have been proposed. However, the final efficiency and cost are compromised due to the use of a higher number of switching devices. Other approaches, commonly used in electronic ballasts, simplify the rectifier stage in order to improve the converter performance [15-20]. This topology, known as half-bridge boost rectifier, reduces the switches count while keeping the same performance as more complex solutions.

The aim of this paper is to propose a new topology to improve the efficiency while reducing the power devices count for induction heating applications. The proposed topology is based on the series resonant half-bridge topology and requires only two

rectifier diodes. The effective output voltage is doubled, as in [21], [22], allowing a significant current reduction in the switching devices. Moreover, the proposed topology can operate with zero voltage switching conditions during both turn-on and turn-off transitions. As a consequence, the efficiency is improved while the devices count is reduced.

This paper is organized as follows. Section II describes the proposed topology. In Section III, a deeper analysis of the power converter is performed. Sections IV and V show the main simulation and experimental results, respectively. Finally, Section VI draws the main conclusions of this paper.

II. PROPOSED POWER CONVERTER

The proposed topology (Fig. 1) employs two bidirectional switches S_H and S_L composed of a transistor T_H or T_L, typically an IGBT, and an antiparallel diode D_H or D_L, respectively. Mains voltage v_{ac} is rectified by two diodes D_{rH}, D_{rL}, but only one of them is activated at the same time. This operation increases efficiency with regard to classical topologies based on a full-bridge diode rectifier plus a dc-link inverter.

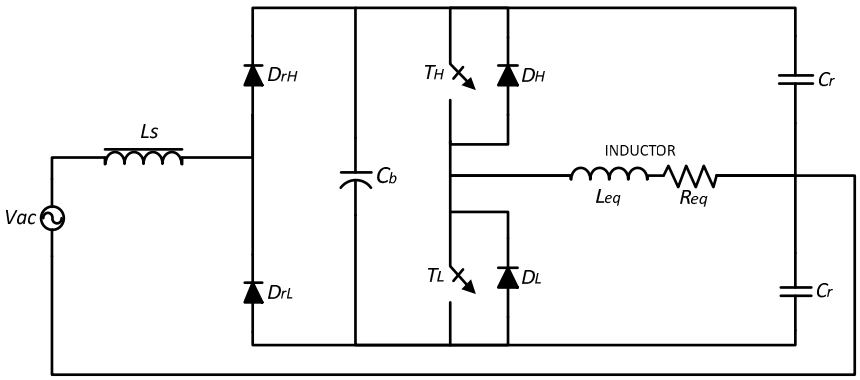


Fig. 1 Proposed ac-ac converter.

The proposed topology is a series-parallel resonant converter. The inductor-pot system is modeled as an equivalent series resistance (R_{eq}) and inductance (L_{eq}), as shown in Fig. 1 [23].

This topology implements resonant capacitors, C_r, and may use a bus capacitor C_b. Due to the symmetry between positive and negative mains voltage, both resonant capacitors have the same value. Input inductor L_s is used to reduce the harmonic content to fulfill the EMC regulations.

III. ANALYSIS

The topology presents symmetry between positive and negative ac voltage supply. Its symmetry simplifies analysis and makes possible to redraw the circuit as shown in Fig. 2.

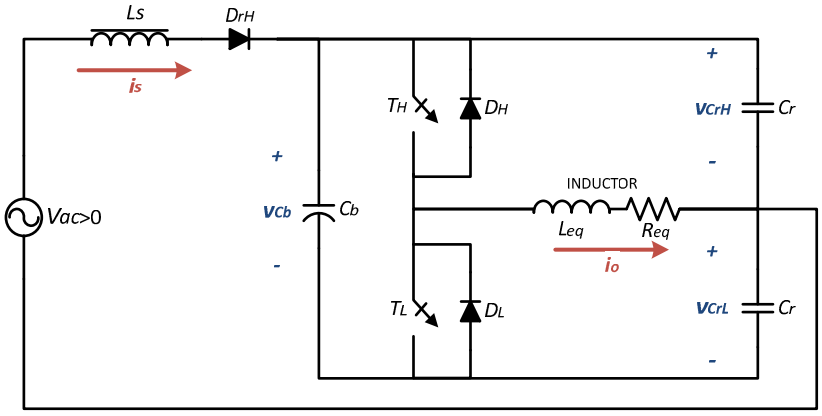


Fig. 2 Equivalent circuit during the positive mains voltage cycle.

Although this topology uses different resonant configurations, parallel and series, and different resonant tanks for each of them, it is possible to use a normalized nomenclature based on series resonance:

$$C_b = \alpha \cdot C_r, \quad \alpha \geq 0, \tag{1}$$

$$L_s = \beta \cdot L_{eq}, \quad \beta \geq 1, \tag{2}$$

$$\omega_0 = \frac{1}{\sqrt{L_{eq} \cdot C_r}}, \tag{3}$$

$$\omega_n = \frac{\omega_{sw}}{\omega_0}, \tag{4}$$

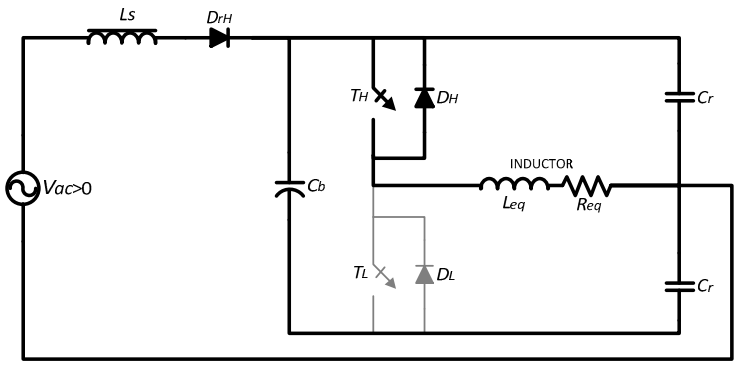
$$Z_0 = \sqrt{\frac{L_{eq}}{C_r}}, \tag{5}$$

$$R_{eq} = \frac{\omega_0 \cdot L_{eq}}{Q_{eq}} = \frac{Z_0}{Q_{eq}}, \tag{6}$$

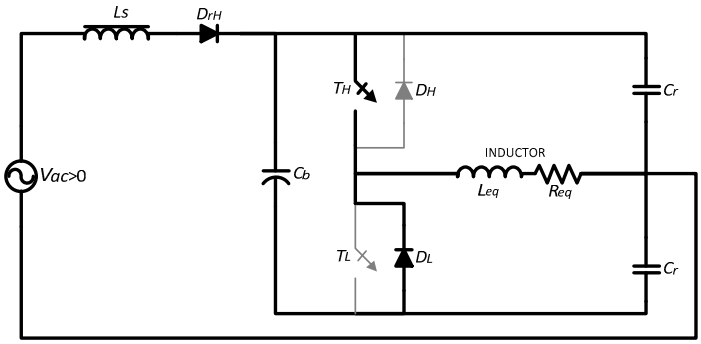
were α is the ratio between the dc-link and the resonant capacitors and β the ratio of the input choke and the equivalent inductance of the inductor-pot system. The parameters $\{\omega_0, \omega_{sw}, \omega_n\}$ are the angular resonant frequency, the angular switching frequency, and the normalized angular switching frequency, respectively. Z_0 defines the equivalent impedance of the resonant circuit, defined by L_{eq} and C_r. Finally, Q_{eq} is the equivalent inductor-pot system quality factor at the resonant frequency. The system will be analyzed using the state-space description. Each state is completely defined by a differential equation system and the lobal system response is the conduction angle, θ, average response of each state (I to III).

$$\dot{\mathbf{x}}(\theta) = \mathbf{A_k}\mathbf{x}(\theta) + \mathbf{B_k} \cdot v_{ac}, \quad k = \{1, 2, 3\}, \quad \theta = 0..2\pi, \tag{7}$$

where the state variables $\mathbf{x} = [i_s, v_{Cb}, v_{CrH}, v_{CrL}, i_0]^T$ are the input current, the voltage across the bus capacitor C_b, the voltage across both resonant capacitors, and the current through the load, respectively.



(a)



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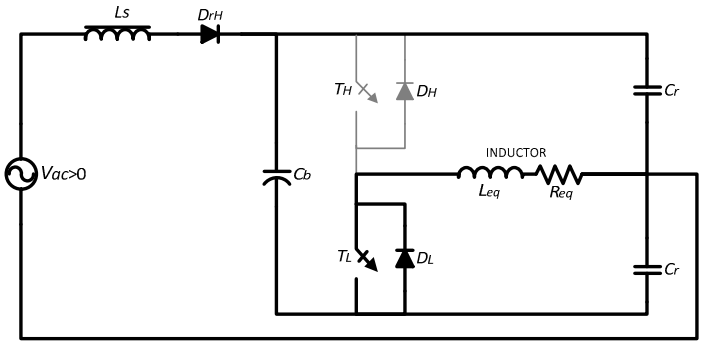


(c)

Fig. 3 Equivalent circuitrs. (a) State I, (b) state II, and (c) state III.

As it is shown in Fig. 3, working under ZVS conditions, there are three different states. Each on has its characteristic differential equation system. Fig. 4 shows the transition conditions for each state.

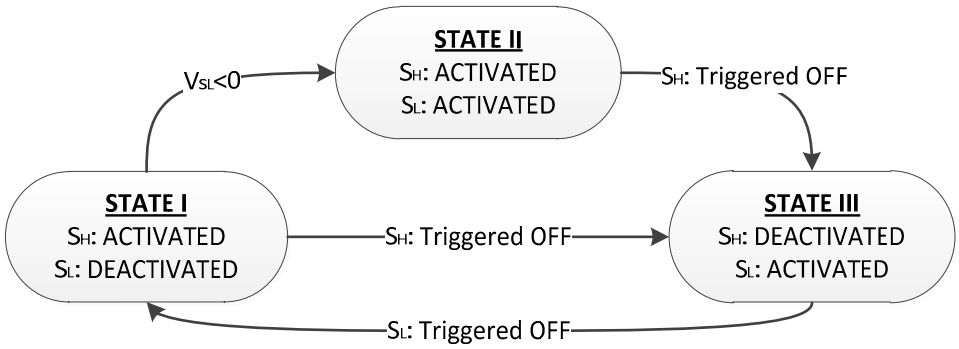


Fig. 4 States and transition conditions.

State I operates with the high-side switching device (S_H) triggered-on and activated and the low side switching device (S_L) triggered-off. The parallel resonant circuit is set by an equivalent capacitor C_{eq}, obtained from C_r and C_b and expressed in (8), and the inductor electrical parameters, R_{eq} and L_{eq}. The current flowing through S_H is the same as the one flowing through the load.

$$C_{eq} = C_r\left(1+\frac{C_b}{C_r+C_b}\right) = C_r\left(\frac{1+2\alpha}{1+\alpha}\right). \quad (8)$$

State I begins when S_L is triggered-off. In this moment, the antiparallel diode D_H conducts and S_H can be triggered-on ensuring ZVS switching-on conditions. Transitions from this state can lead either to state II or state III. If voltage across S_L reaches zero and D_L starts conducting, the transition condition to state II is fulfilled. On the other hand, if S_H is switched off when T_H conducts, next state is state III.

The normalized differential equations that defines the dynamics of the system in this state are:

$$\frac{di_0(\theta)}{d\theta} = \frac{1}{\omega_n Z_0}\left(v_{Ceq}(\theta) - \mathrm{R}_{eq}\cdot i_0(\theta)\right), \quad (9)$$

$$\frac{dv_{Ceq}(\theta)}{d\theta} = \frac{Z_0(1+\alpha)}{\omega_n(1+2\alpha)}\left(i_s(\theta) + i_0(\theta)\right), \quad (10)$$

$$\frac{di_s(\theta)}{d\theta} = \frac{1}{\beta\omega_n Z_0}\left(v_{ac} - v_{Ceq}(\theta)\right), \quad (11)$$

Therefore, the state space matrices for state I are:

$$\mathbf{A_1} = \begin{pmatrix} 0 & 0 & \frac{-1}{\beta\omega_n Z_0} & 0 & 0 \\ \frac{Z_0}{\omega_n(1+2\alpha)} & 0 & 0 & 0 & \frac{Z_0}{\omega_n(1+2\alpha)} \\ \frac{Z_0(1+\alpha)}{\omega_n(1+2\alpha)\alpha} & 0 & 0 & 0 & \frac{Z_0(1+\alpha)}{\omega_n(1+2\alpha)\alpha} \\ \frac{-\alpha Z_0}{\omega_n(1+2\alpha)} & 0 & 0 & 0 & \frac{-\alpha Z_0}{\omega_n(1+2\alpha)} \\ 0 & \frac{1}{\omega_n Z_0} & 0 & 0 & \frac{-\mathrm{R}_{eq}}{\omega_n Z_0} \end{pmatrix}, \quad \mathbf{B_1} = \begin{pmatrix} \frac{1}{\beta\omega_n Z_0} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}. \quad (12)$$

State II is characterized by the conduction of both switching devices, although only S_H is triggered-on. That is, T_H and D_L conducts at the same time. Current through load is supplied by both devices (T_H and D_L), and consequently, low conduction-stress for the devices is achieved. The equivalent parallel resonant circuit is set by the inductor electrical parameters in parallel with both resonant capacitors. C_b is short-circuited by both switching devices. This state starts when voltage across S_L reaches zero. In this moment, D_L start conducting at the same time as T_H is triggered-on. This state finishes when S_H is triggered-off and next state is state III. The main benefit results of the lower switch-off current achieved when S_H is triggered-off, due to the fact that the load current is supplied by both devices. In addition, S_H achieves ZVS conditions during both switch-on and switch-off transitions, reducing consequently the switching losses.

The normalized differential equations that defines the dynamics of the system in this state are:

$$\frac{di_s(\theta)}{d\theta} = \frac{1}{\beta\omega_n Z_0}\left(V_s - v_{CrH}(\theta)\right), \tag{13}$$

$$v_{Cb} = 0, \tag{14}$$

$$\frac{dv_{CrH}(\theta)}{d\theta} = \frac{Z_0}{2\omega_n}\left(i_s(\theta) + i_0(\theta)\right), \tag{15}$$

$$\frac{dv_{CrL}(\theta)}{d\theta} = \frac{-Z_0}{2\omega_n}\left(i_s(\theta) + i_0(\theta)\right), \tag{16}$$

$$\frac{di_0(\theta)}{d\theta} = \frac{1}{\omega_n Z_0}\left(v_{CrH}(\theta) - R_{eq}\cdot i_0(\theta)\right), \tag{17}$$

The state space matrix for this state can be shown in next equation.

$$\mathbf{A_2} = \begin{pmatrix} 0 & 0 & \frac{-1}{\beta\omega_n Z_0} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{Z_0}{2\omega_n} & 0 & 0 & 0 & \frac{Z_0}{2\omega_n} \\ \frac{-Z_0}{2\omega_n} & 0 & 0 & 0 & \frac{-Z_0}{2\omega_n} \\ 0 & 0 & \frac{1}{\omega_n Z_0} & 0 & \frac{-R_{eq}}{\omega_n Z_0} \end{pmatrix}, \quad \mathbf{B_2} = \begin{pmatrix} \frac{1}{\beta\omega_n Z_0} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}. \tag{18}$$

State III is defined by the conduction of S_L while S_H is deactivated. The equivalent resonant circuit is set by one resonant capacitor in parallel with the series connection of C_b capacitor and the parallel connection of the inductor and the other one resonant capacitance. Note that when C_b is zero (α=0), the equivalent resonant circuit is a series RLC circuit composed of the inductor-pot system and one resonant capacitor. This state starts when S_H is triggered-off. At this moment, D_L starts conducting and S_L can be triggered on achieving ZVS switch-on conditions. This state finishes when S_L is deactivated, and the next state is state I.

The normalized differential equations system that defines the dynamics is:

$$\frac{di_s(\theta)}{d\theta} = \frac{1}{\beta\omega_n Z_0}\left(V_s - v_{CrH}(\theta)\right), \tag{19}$$

$$\frac{dv_{Cb}(\theta)}{d\theta} = \frac{Z_0}{\omega_n}\left(i_s(\theta) - i_0(\theta)\frac{2+\alpha}{\alpha}\right), \tag{20}$$

$$\frac{dv_{CrH}(\theta)}{d\theta} = \frac{Z_0}{\omega_n}\left(i_s(\theta)(1+\alpha) - i_0(\theta)\alpha\right), \tag{21}$$

$$\frac{dv_{CrL}(\theta)}{d\theta} = \frac{-Z_0}{\omega_n}\left(i_s(\theta)\alpha - i_0(\theta)(1+\alpha)\right), \tag{22}$$

$$\frac{di_0(\theta)}{d\theta} = \frac{1}{\omega_n Z_0}\left(v_{CrH}(\theta) - v_{Cb}(\theta) - R_{eq}\cdot i_0(\theta)\right), \tag{23}$$

The space state matrix for this state is shown in the next equation.

$$\mathbf{A_3} = \begin{pmatrix} 0 & 0 & \frac{-1}{\beta\omega_n Z_0} & 0 & 0 \\ \frac{Z_0}{\omega_n} & 0 & 0 & 0 & \frac{-Z_0(2+\alpha)}{\alpha\omega_n} \\ \frac{Z_0(1+\alpha)}{\omega_n} & 0 & 0 & 0 & \frac{-\alpha Z_0}{\omega_n} \\ \frac{-\alpha Z_0}{\omega_n} & 0 & 0 & 0 & \frac{Z_0(1+\alpha)}{\omega_n} \\ 0 & \frac{-1}{\omega_n Z_0} & \frac{1}{\omega_n Z_0} & 0 & \frac{-R_{eq}}{\omega_n Z_0} \end{pmatrix}, \quad \mathbf{B_3} = \begin{pmatrix} \frac{1}{\beta\omega_n Z_0} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}. \tag{24}$$

IV. SIMULATION RESULTS

By using the space-state analysis presented in Section III, two operating modes can be described (Fig. 5). Both of them achieves ZVS switch-on conditions, however, only the first operation mode can also achieve ZVS switch-off conditions for S_H. The first operation mode uses the three states described before I, II and III. It makes possible to achieve ZVS conditions for the high-side switch in state II. The low-side switch has non-ZVS turn-off characteristic. However, turn-off current is always lower than in the high-side switch.

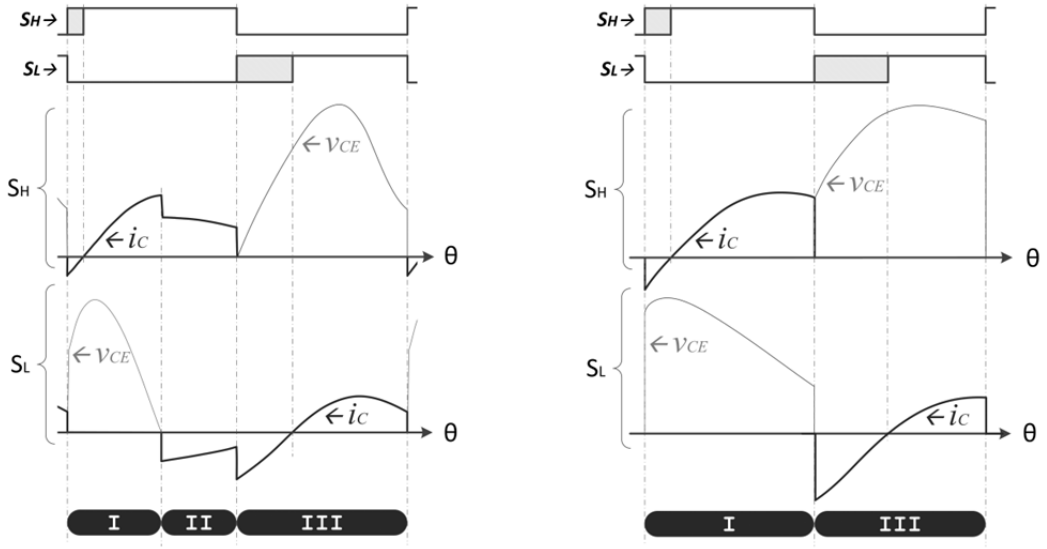


Fig. 5 Operation modes: (a) First operation mode. (b) Second operation mode.

The second operation mode only uses two states: I and III. This operation mode does not achieve ZVS conditions during switch-off, and the switching losses are therefore increased. This switching losses can be reduced by using snubber capacitors [24], [25].

Nowadays, the induction heating appliances power is limited by mains maximum current and voltage. The typical maximum output power is 3600 W, and the power converter prototype has been therefore designed to achieve 3600-W output power. Simulation parameters are C_r = 470 nF, and the inductor is modeled by L_{eq} = 65 uH and 6.5 Ω for the series equivalent resistor at switching frequency. The dc-link capacitor has been selected to be low enough to obtain a high power factor and a proper power control, as it is shown in this section, and it can be neglected in this analysis.

The control strategies considered to control the output power are the square wave control (SW), based on changing the switching frequency, and the asymmetrical duty cycle control [6], [24], [26], based on changing the duty cycle of the switching devices. Next subsections detail the main simulation results.

A. Square wave control

Square wave control modifies the output power by controlling the switching frequency. The switching frequency is higher than the resonant frequency to achieve switch-on ZVS, and the output power is reduced when the switching frequency is increased (Fig. 6).

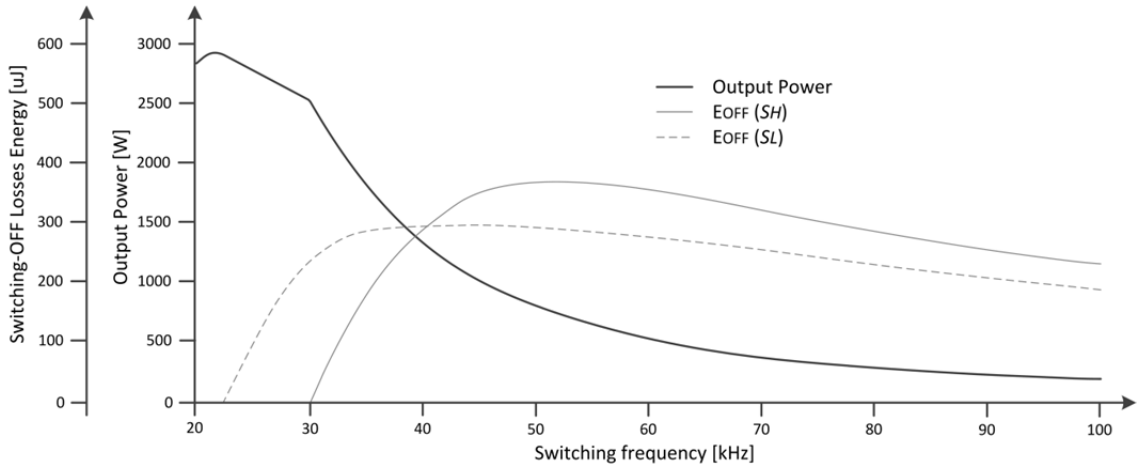


Fig. 6. Square wave control: Output power and switching losses.

As it is shown in Fig. 6, the frequency range starts in 22 kHz, which is the resonant frequency determined by L_{eq} and C_r, that ensures ZVS switching-on conditions, and can be increased to decrease output power. However, if the switching frequency reaches 30 kHz, switching-off losses increase because of ZVS switching-off conditions are not achieved. As a result, the suitable switching frequency range and, therefore, the output power range is reduced. To overcome this limitation, the Asymmetric Duty Cycle control strategy (ADC) is proposed.

B. Asymmetrical duty cycle control

ADC control varies the output power by changing the switching device duty cycle. As it is shown in Fig. 7, this control strategy delivers different output power by changing of the percent of conducting angle (θ) in which the high-side switch (S_H) is activated $D(S_H)$.

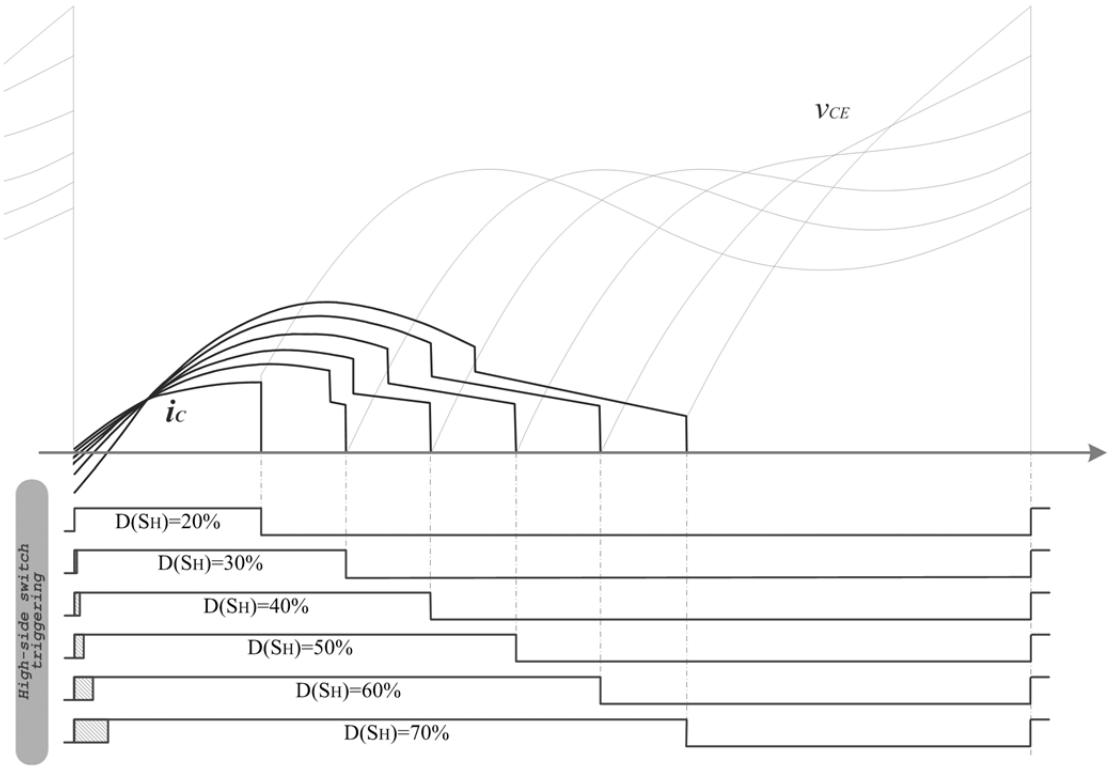


Fig. 7 ADC control strategy: main control signals and waveforms.

The low side switch (S_L) conducting angle can be calculated as follows:

$$D(S_L) = 2\pi - D(S_H) - \theta_{DT}, \quad (25)$$

where θ_{DT} is the dead-time conducting angle to avoid short-circuits. The variation of conducting angle is restricted by the achievement of soft-switching conditions for S_H, ZVS for switching-off, and by the achievement of ZVS in the switching-on commutation for both devices (antiparallel diode conduction at the beginning). In order to operate with switch-on ZVS conditions, the duty cycle must be higher than 30%. The upper boundary is kept to 60% to obtain a proper safety margin and balance the total amount of losses per switching device. Fig. 8 shows the power output variation achieved and the switching losses.

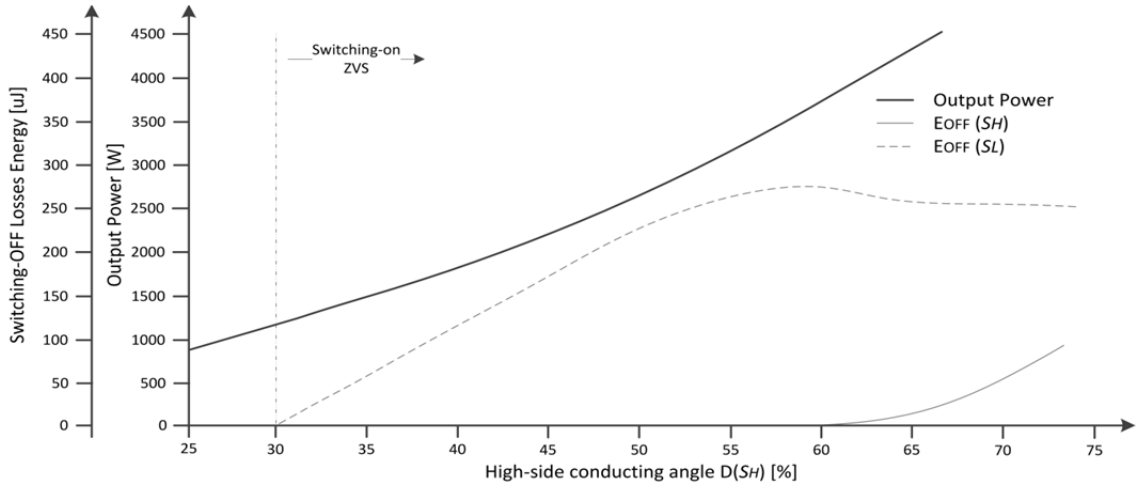
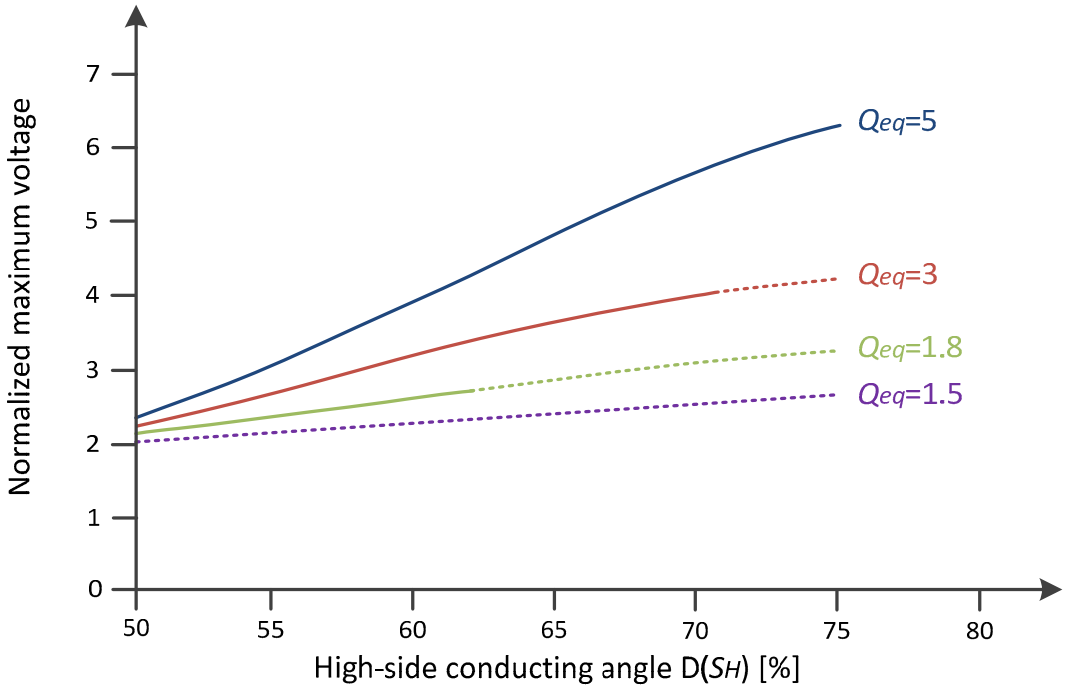


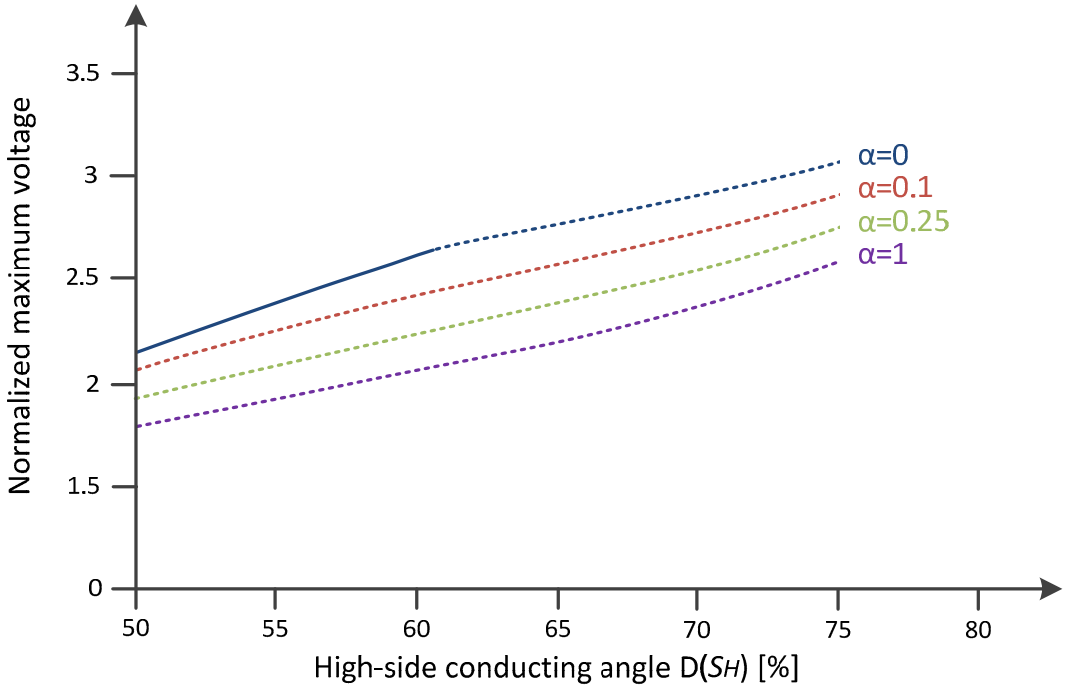
Fig. 8. Asymmetrical duty cycle control: Output power and switching losses.

One of the key design aspects when designing the proposed converter to operate with ADC control is the voltage that the switching devices must withstand. Fig. 9 shows the value of the voltage normalized to the input mains voltage as a function of the duty cycle for loads with different Q_{eq} (a) and different bus capacitors for the same Q_{eq} (b). In this figure, the optimum switching area is plotted with solid line.

As it is shown in Fig. 9 (a), the induction load must be carefully designed to avoid unfeasible high voltages. Besides, Fig. 9 (b) shows that the bus capacitor significantly reduces the duty cycle operating range, whereas the voltage in the switching device is reduced. As a conclusion, for this design the bus capacitor is removed to improve the duty cycle operating range, and consequently the output power control, and to reduce the number of components. However, other designs with lower output power control requirements may benefit of the voltage reduction.



(a)



(b)

Fig. 9 Normalized maximum voltage for different duty cycles: values for different load quality factors (a), and values for different bus capacitors and same Q_{eq} = 1.8 (b).

As a conclusion, the output power in the proposed converter can be effectively controlled by means of SW and ADC control strategies. The output power can be reduced from the maximum value at the resonant frequency, 3000 W, to 1000 W without degrading the converter efficiency. If further reduction is required, pulse density modulation (PDM) [27] can be used to keep a high efficiency. Next section shows the main experimental results to validate the analytical and simulation results.

V. EXPERIMENTAL RESULTS

To verify the proposed topology, a laboratory prototype was built. The desired maximum output power level is 3.6 kW, obtained at a switching frequency higher than 20 kHz to avoid the audible range. The inductor-pot system is characterized by $R_{eq} \approx 6.5\,\Omega$ and a measured equivalent inductance of 67 μH. The measurements have been performed by means of a precision LCR meter from Agilent (E4980A). Power supply is fixed to 230 V and the input inductance L_s in this paper was set to 1.4 mH to avoid high frequency ripple in the ac supply. The control signals are generated by means of an FPGA-based digital pulse width modulator [28], [29]. Table II shows the component values for the prototype:

TABLE II
PROTOTYPE PARAMETERS

COMPONENTS		Values
L_{eq}	Equivalent inductance	67 μH
R_{eq}	Equivalent resistance	6.5 Ω
$v_{ac,rms}$	Supply power source	230 V
C_r	Resonant capacitor	470 nF
C_h	DC-link capacitor	0 nF
L_s	Input inductance	1.4 mH
R_s	Equivalent series resistance	78 mΩ
S_H, S_L	Switching device with anti-parallel diode	IGBT FGH30RN120
D_{rH}, D_{rL}	Rectifier diodes	DESP 60-12AR

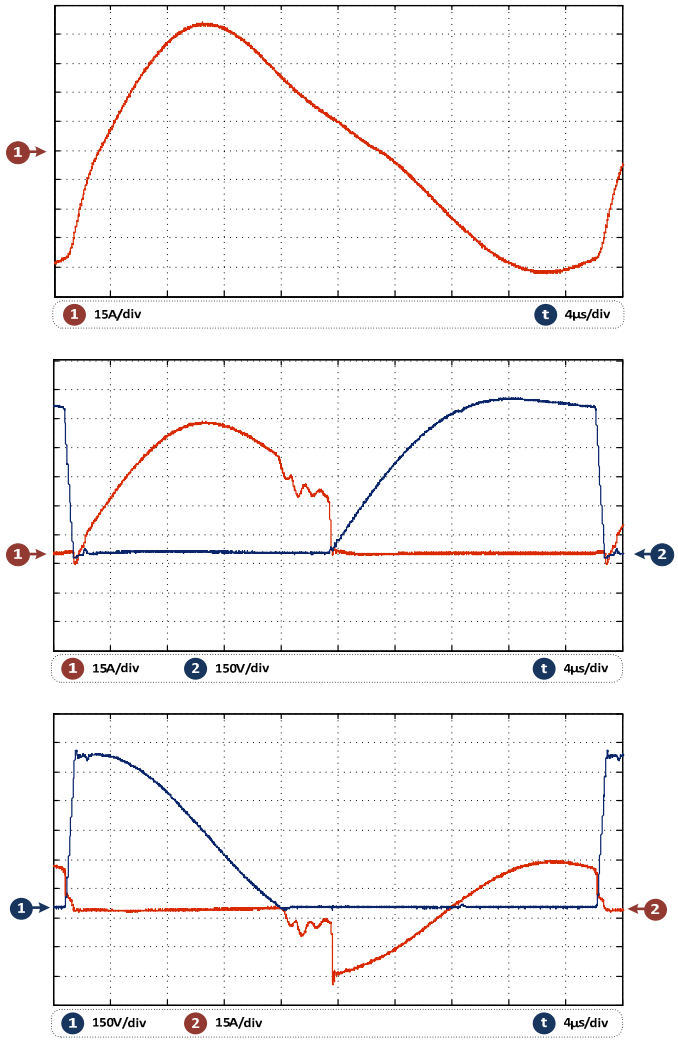
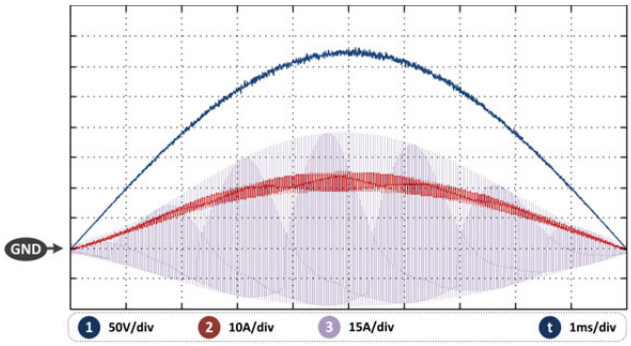
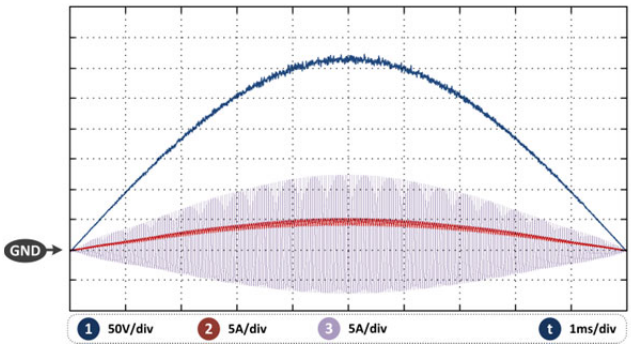


Fig. 10 Measured main waveforms. From top to bottom: inductor current (15 A/div), voltage (150 V/div) and current (15 A/div) in the high-side switch, and voltage (150 V/div) and current (15 A/div) in the low-side switch.



(a)



(b)

Fig. 11 Measured input waveforms for a mains half-cycle: (a) Maximum output power (3600 W; input voltage 50 V/div, input current 10 A/div, and load current 15 A/div) and (b) minimum output power (900 W; input voltage 50 V/div, input current and load current 5 A/div). Horizontal: 1 ms/div.

The main waveforms during a switching period for a 50% duty cycle are shown in Fig. 10, including the inductor current, and voltage and current through the switching devices. Besides, Fig. 11 shows the input voltage and current, and the load current during a mains half-cycle period. These measurements have been performed with an input inductor L_s = 1.4 mH. If further input current ripple reduction is required, either the power converter switching frequency or the input inductance can be increased. As a conclusion, these waveforms match up with the theoretical expected ones, and verify the proper operation of the converter.

The efficiency of the power converter has been measured using the power analyzer YOKOGAWA PZ-4000. The efficiency experimental results for both SW and ADC

control strategies are shown in Fig. 12, where a comparison with the classical half-bridge topology [3-5] has been included. The classical topology has a reduced overvoltage and it is therefore implemented with 600-V HGTG20N60 IGBTs, whereas the proposed topology is implemented with 1200-V IGBTs. In spite of this, Fig. 11 shows that the proposed topology achieves a significant efficiency improvement in the whole operating range.

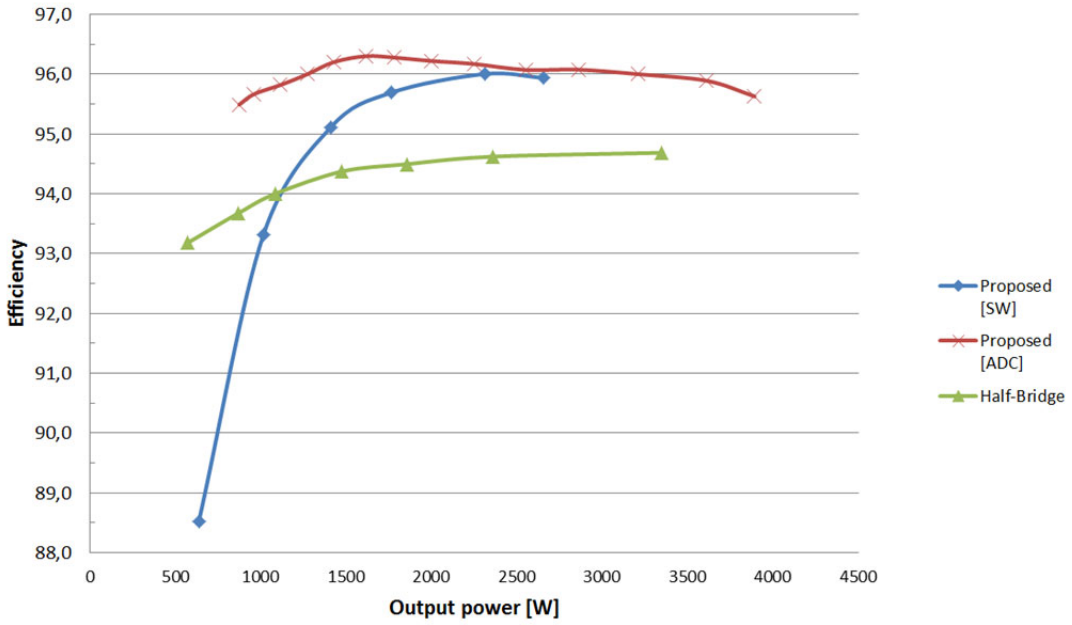


Fig. 12 Measured efficiency.

On one hand, SW control strategy achieves a higher efficiency in the high output power range. However, the efficiency significantly decreases in the low output power range due to the switching losses. On the other hand, the ADC control achieves the same high efficiency in the high output power range, but it keeps constant due to the soft-switching conditions. It is important to note that the proposed topology with ADC control achieves a significant efficiency improvement compared with the classical half-bridge topology due to the power devices and current reduction and the soft-switching conditions.

VI. CONCLUSIONS

This paper presents a new ac-ac converter applied to domestic induction heating. An analytical analysis has been performed in order to obtain the equations and operation modes that describe the proposed converter. The converter can operate with zero voltage switching during both turn on and turn off commutations. Besides, the output voltage is doubled compared to the classical half-bridge, reducing the current through the switching devices. As a consequence, the power converter efficiency is improved in the whole operating range.

A 3.6-kW prototype has been designed and implemented in order to validate the analytical and simulation results. The experimental measurements show a significant efficiency improvement compared to the classical half-bridge topology and validates the feasibility of the proposed converter.

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