Eur. Phys. J. C (2025) 85:1334
https://doi.org/10.1140/epjc/s10052-025-14940-1

THE EUROPEAN PHYSICAL JOURNAL C

Regular Article - Experimental Physics

Production, quality assurance and quality control of the SiPM Tiles for the DarkSide-20k Time Projection Chamber

DarkSide-20k Collaboration[⋆]

Received: 9 July 2025 / Accepted: 13 October 2025

Abstract The DarkSide-20k dark matter direct detection experiment will employ a 21 m^2 silicon photomultiplier (SiPM) array, instrumenting a dual-phase 50 tonnes liquid argon Time Projection Chamber (TPC). SiPMs are arranged into modular photosensors called *Tiles*, each integrating 24 SiPMs onto a printed circuit board (PCB) that provides signal amplification, power distribution, and a single-ended output for simplified readout. 16 Tiles are further grouped into *Photo-Detector Units* (PDUs). This paper details the production of the Tiles and the Quality Assurance and Quality Control (QA-QC) protocol established to ensure their performance and uniformity. The production and QA-QC of the Tiles are carried out at Nuova Officina Assergi (NOA), an ISO-6 clean room facility at LNGS. This process includes wafer-level cryogenic characterisation, precision die attaching, wire bonding, and extensive electrical and optical validation of each Tile. The overall production yield exceeds 83.5%, matching the requirements of the DarkSide-20k production plan. These results validate the robustness of the Tile design and its suitability for operation in a cryogenic environment.

1 Introduction

DarkSide-20k (DS-20k) is a Time Projection Chamber (TPC) for dark matter particle searches featuring an active mass of 50 tonnes of liquid argon from underground sources (UAr) currently under construction at Laboratori Nazionali del Gran Sasso (LNGS) in Italy. The collaboration opted to develop with Fondazione Bruno Kessler (FBK) a new generation of silicon photomultiplier (SiPM) especially optimised for operation at cryogenic temperature (80 K) with reduced noise, and to develop an in-house integration process to produce photo-detectors. These components equip the two large optical planes at the bottom and top of the TPC for a total surface of 21 m^2.

Among the benefits of utilising SiPMs over Photo Multiplier Tubes (PMTs) are their low voltage operation, insensitivity to magnetic fields, mechanical robustness, longevity, and compactness that facilitates covering large areas, while minimising empty spots. Additionally, SiPMs exhibit minimal residual natural radioactivity, which makes them ideal for low-background experiments like DS-20k [1].

At the heart of the DS-20k detector is a dual-phase TPC designed with a vertical electron drift configuration. The TPC is designed as an octagonal prism standing 348 cm tall with an inner diameter of 350 cm. The TPC is filled with low-radioactivity UAr, which serves as the target for Weakly Interacting Massive Particles (WIMPs) [2–4]. Above the liquid argon phase, a gas layer approximately 7 mm thick is maintained.

The TPC is enclosed in a stainless steel vessel filled with an extra 36 t of UAr, which serves as the neutron Inner Veto. The stainless steel vessel, the TPC and the Inner Veto are immersed in atmospheric liquid argon housed in a DUNE-like membrane cryostat functioning as the cosmogenic Outer Veto [5].

In the liquid argon TPC, light is produced by two processes: the primary liquid argon scintillation (S1) and gas proportional electroluminescence (S2) from ionisation electrons extracted into the gas layer. In DS-20k, both S1 and S2 signals will be detected by arrays of SiPMs mounted on two Optical Planes (OP) positioned on the top and bottom of the TPC's octagonal barrel. Each OP sits behind an optical window coated with Tetraphenyl butadiene (TPB) and covers an area of approximately 10.5 m^2. These OPs are equipped with 11.8 mm × 7.9 mm near-UV sensitive, high-density Cryo NUV-HD SiPMs developed by FBK, further optimised jointly with the DarkSide Collaboration and manufactured by LFoundry S.r.l. [1,6–8].

The SiPMs are arranged into *Tiles*. Every Tile functions as a module containing 24 SiPMs bonded to the front side of a printed circuit board (PCB). The PCB provides common power distribution to all the 24 SiPMs and includes cryogenic low-noise readout electronics, which deliver the total current

⋆ e-mail: ds-ed@lists.infn.it

Published online: 20 November 2025

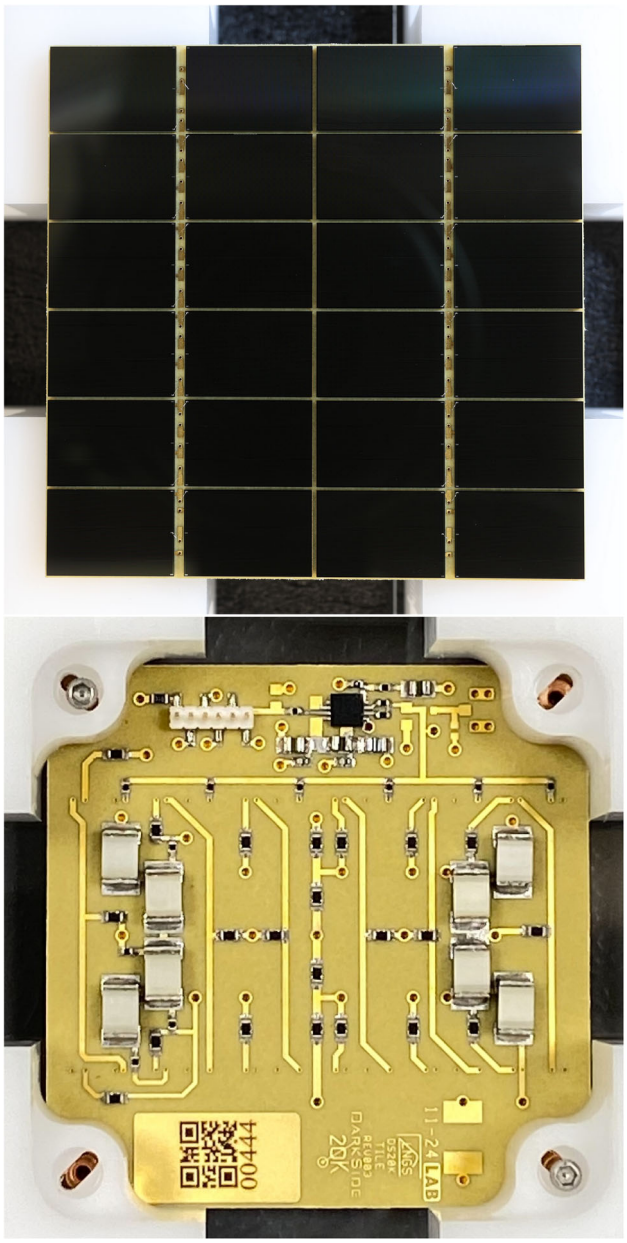

Fig. 1 Picture of a Tile showing the 24 SiPMs, mounted on the top side (Top), and the electronic components, mounted on the bottom side (Bottom). The Tile is mounted on the plastic holder used during the testing phase

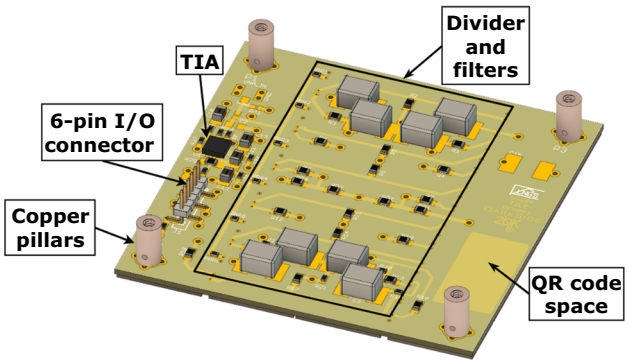

Fig. 2 PCB 3D rendering showing the electronic components on the bottom side of the Tile

from the SiPMs as a single-ended output signal. Therefore, the Tile is a compact, functional photodetector module. A picture of a Tile is shown in Fig. 1. Each SiPM is equipped with three aluminium anode pads, of which one is used for the cryogenic SiPM assessment and the remaining two are used for the wire bonding. The golden PCB cathode pad is also visible. The Inner Veto and the Outer Veto of DS-20k are also instrumented with SiPM-based photosensors integrated into Tiles.

In DS-20k, Tiles are assembled into *Photo-Detector Units* (PDUs) to further simplify the process of assembling and reading out the OP. A PDU consists of 16 Tiles mounted on a custom motherboard, where they are aggregated in groups of four to give four readout channels per PDU. All Tiles within a single PDU receive a common bias voltage. Each PDU generates four signal outputs, with each output representing the summed signals of each quadrant. The PDU will be the subject of a future paper.

Tiles are manufactured within the Nuova Officina Assergi (NOA) facility, located at INFN-LNGS, an ISO-6 clean room packaging space spanning 353 m^2 [9]. This facility is equipped with state-of-the-art production machinery for evaluating wafer quality and assembling SiPMs into Tiles. A batch of 260,000 SiPMs derived from 1400 LFoundry S.r.l. wafers underwent tests at NOA between 2023 and 2025 [10]. The SiPMs that successfully meet quality control standards are assembled into Tiles. 8448 Tiles among the ones that exhibit good quality are intended for use within the 528 PDUs of the DS-20k TPC.

This paper describes the production of the DS-20k TPC Tiles in NOA and the Quality Assurance and Quality Control (QA-QC) procedures accompanying the production. The paper is organised as follows: Sect. 2 details the Tile's design; Sect. 3 describes the Tile production process flow in NOA; Sect. 4 explains the QA-QC protocols; Sect. 5 highlights the most relevant results.

2 The Tile: a compact SiPM-based photodetector

Silicon photomultipliers (SiPMs) are single-photon detectors composed of arrays of closely arranged Single Photon Avalanche Diodes, which operate above the breakdown voltage, V_{bd}, to initiate self-sustaining charge avalanches upon photon absorption [11].

The distinct challenge of extracting signals from large areas of SiPMs arises primarily from their capacitance, which

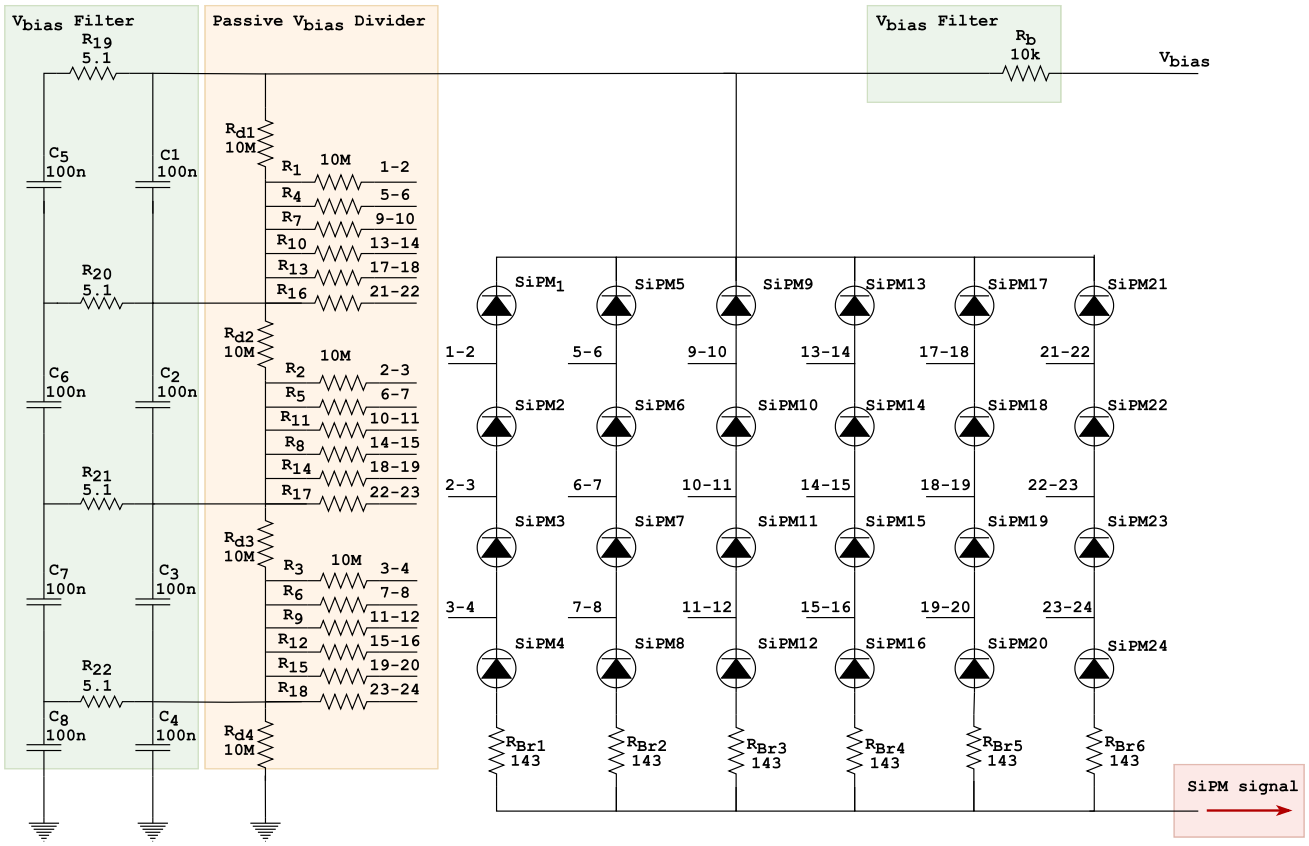

Fig. 3 Schematic of the Tile electronics: it consists of 24 1 cm^2-SiPMs arranged in a *4s6p* configuration, with 6 parallel branches of 4 SiPMs in series. This arrangement reduces capacitance for improved bandwidth while simplifying the readout with a single output signal (SiPM signal in the red shade). A precision voltage divider provides 1/4 of the input bias (V_{bias}) to all the SiPMs. The divider is composed of a network of 10 MΩ resistors (R_{d1} to R_{d4}, and R_1 to R_{18}, Passive V_{bias} Divider in the orange shade), coupled with 100 nF parallel capacitors (C_1 to C_8, V_{bias} Filter in the green shade) acting as a low-pass filter and charge storage. A 10 kΩ filter resistor is added in series to the divider, resulting in an overall 40.01 MΩ impedance. An additional 143 Ω series resistance (R_{Br1} to R_{Br6}) provides the necessary frequency compensation for the readout amplifier

is on the order of 50 pF/mm^2. A single SiPM covering a 1 cm^2 area exceeds the nanofarad range. In the DS-20k detector, the TPC's optical planes have a surface area around 10.5 m^2. Such a large surface requires a careful design of the readout electronics and the connection configuration of SiPMs.

The solution implemented in DS-20k involves arranging the 24 SiPMs within a Tile composed of 6 parallel branches, each containing 4 SiPMs connected in series [12]. This arrangement, hereafter known as *4s6p* (where *s* stands for series and *p* stands for parallel), helps decrease the total capacitance of each series branch, thus improving the bandwidth, at the cost of reducing the output current by a factor of 4. The surface of Tile is 24 cm^2 and within it, 22.2 cm^2 is the total sensitive area.

The *4s6p* SiPM matrix is read out by a single transimpedance amplifier (TIA). The Tile outputs a single-ended signal that represents the cumulative photo-currents of all SiPMs. A 3D illustration of the Tile is depicted in Fig. 2. The schematics of the Tile electronics are illustrated in Figs. 3 and 4.

In the Tiles, the SiPM matrix is attached to the front surface of a PCB with dimensions 49.5 × 49.5 mm^2. Each PCB comes equipped with a custom 6-pin input–output connector with a 1.27 mm pitch. Of these (refer to Fig. 4), one pin supplies the SiPM bias voltage input (V_{bias}), one pin manages the Tile power down (PD), two pins supply the low voltage (LV− and LV+), one pin transmits the output signal, and the final pin serves as the ground. The low voltage inputs undergo filtering in a LC network before being delivered to the TIA inputs. The PCB's back side accommodates the connector, the low-noise cryogenic readout electronics, and delivers the input voltages to the various components.

A precision voltage divider ensures an even distribution of bias voltage by providing 1/4 of the input bias to all the SiPMs. This passive voltage divider is based on 10 MΩ resistors (R_{d1} to R_{d4} in Fig. 3). The divider is also coupled with 100 nF Polyethylene Naphthalate (PEN) parallel capacitors

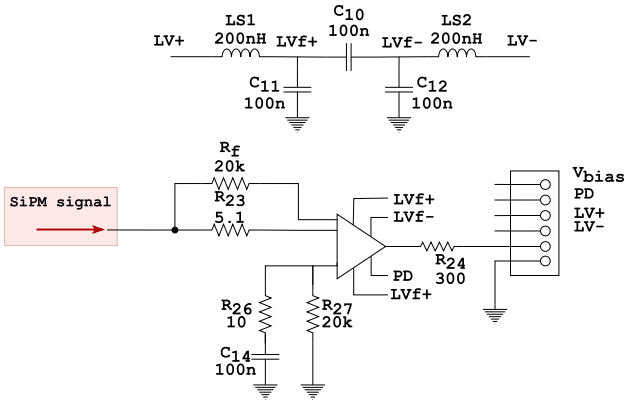

Fig. 4 Schematic of the TIA stage with a 20 kΩ feedback resistor (R_f) setting its gain and the 6-pin input–output connector. Of these (from top to bottom), one pin supplies the SiPM bias voltage input (V_{bias}), one pin manages the Tile power down (PD), two pins supply the low voltage (LV− and LV+), one pin transmits the output signal, and the final pin serves as the ground. The low voltage inputs undergo filtering in the LC network (in the top of the figure) before being delivered to the TIA inputs

(C_1 to C_8 in Fig. 3) to behave as a low-pass filter of cut-off frequency about 300 Hz. The decoupling capacitors act as a charge storage device, providing energy when required by the SiPM and making it less susceptible to short-term changes in the working point. The materials are chosen for low-radioactivity reasons, voltage tolerance, and behaviour in cryogenic environment.

High-precision electronics components (0.5% resistors, 5% capacitors) ensure the balance of the bias circuit through the series of SiPMs, as detailed in [13]. The 10 MΩ divider resistors result in an equivalent 40 MΩ divider resistance. A 10 kΩ filter resistor (R_b in Fig. 3) is added in series to the voltage divider, resulting in a 40.01 MΩ overall impedance. In the *4s6p* network, an additional 143 Ω series resistance (R_{Br1} to R_{Br6} in Fig. 3) provides the necessary frequency compensation for the readout amplifier. The resistor introduces a low-pass filter effect, which reduces the gain of the amplifier at higher frequencies and adds a pole in the frequency response of the amplifier, dampening the peak in the noise gain [12].

The Tile configuration provides a single positive current signal to the amplification stage. Early developments in Tile readout indicated that charge pre-amplifiers are not suitable for such a large input capacitance, suggesting that a TIA could be a viable alternative [1]. For this reason, the DarkSide Collaboration has selected available commercial SiGe operational amplifiers whose performance peaks at 77 K [12,13].[1]

[1] An alternative technology is implemented for the Tiles of the Inner and Outer Vetoes, where the amplification stage is achieved through a custom ASIC [14].

Reading out the whole Tile surface with a single amplifier significantly reduces the readout complexity [13].

The TIA stage is based on a high-speed, ultra-low noise LMH6629 amplifier, made with SiGe technology by Texas Instruments [15], that converts the photocurrent from the SiPMs to a voltage output with a gain set by the 20 kΩ feedback resistor. The TIA is supplied by 5 V (± 2.5 V with respect to the local middle ground point, refer to Fig. 4). The TIA stage drains an idle current of 15 mA at room temperature and 11 mA at cryogenic temperature, which means that each Tile has a total power consumption of 55 mW in liquid argon. Power dissipation in a cryogenic environment is critical since it can cause bubbling when immersed in liquid argon [4]. The single-ended output of the TIA is a negative voltage pulse due to the amplifier's inverting configuration. It is possible to power the TIA on and off using the PD input.

The DS-20k detector needs to meet stringent radiopurity requirements to maximise its sensitivity to very rare particle dark matter signals [16,17]. Therefore, significant effort was dedicated to selecting materials that minimise the radioactivity of the Tile while preserving its functionality. The primary background contributions originate from the PCB itself and the PEN capacitors mounted on its backside.

The PCB is made with Arlon 55NT by Arlon Electronic material [18], an epoxy laminate and pre-preg system, reinforced with nonwoven aramid, meeting the requirements of IPC-4101/55. The main PCB stack-up structure is based on two 0.48 mm Arlon laminate sheets between two 17 µm metal layers of copper and separated by two 75 µm pre-preg sheets.

This choice of material efficiently incorporates compatibility with lead-free processing to prevent unintended radioactive contamination from lead isotopes, such as ^{214}Pb, utilising a high-temperature multifunctional epoxy resin. The resin features a Thermal Expansion Coefficient ranging from 6 ppm/K to 9 ppm/K compatible with that of silicon to avoid mechanical stress and offers excellent dimensional stability owing to the nonwoven aramid reinforcement. Moreover, PCBs with polymeric reinforcement are intrinsically cleaner compared to traditional glass-reinforced laminates.

The bare PCBs and the individual electronic components were characterised using high-purity broad-energy germanium (BEGe) detectors to quantify radioactive contamination from the uranium and thorium decay chains, as well as gamma-emitting isotopes such as ^{40}K, ^{60}Co, and ^{137}Cs [19,20]. The measured activity is below the requirements set for DS-20k.

3 Tiles production workflow

The production workflow of the DS-20k TPC photoelectronics in NOA follows the block diagram illustrated in Fig. 5. Blue boxes refer to manufacturing processes, yellow boxes

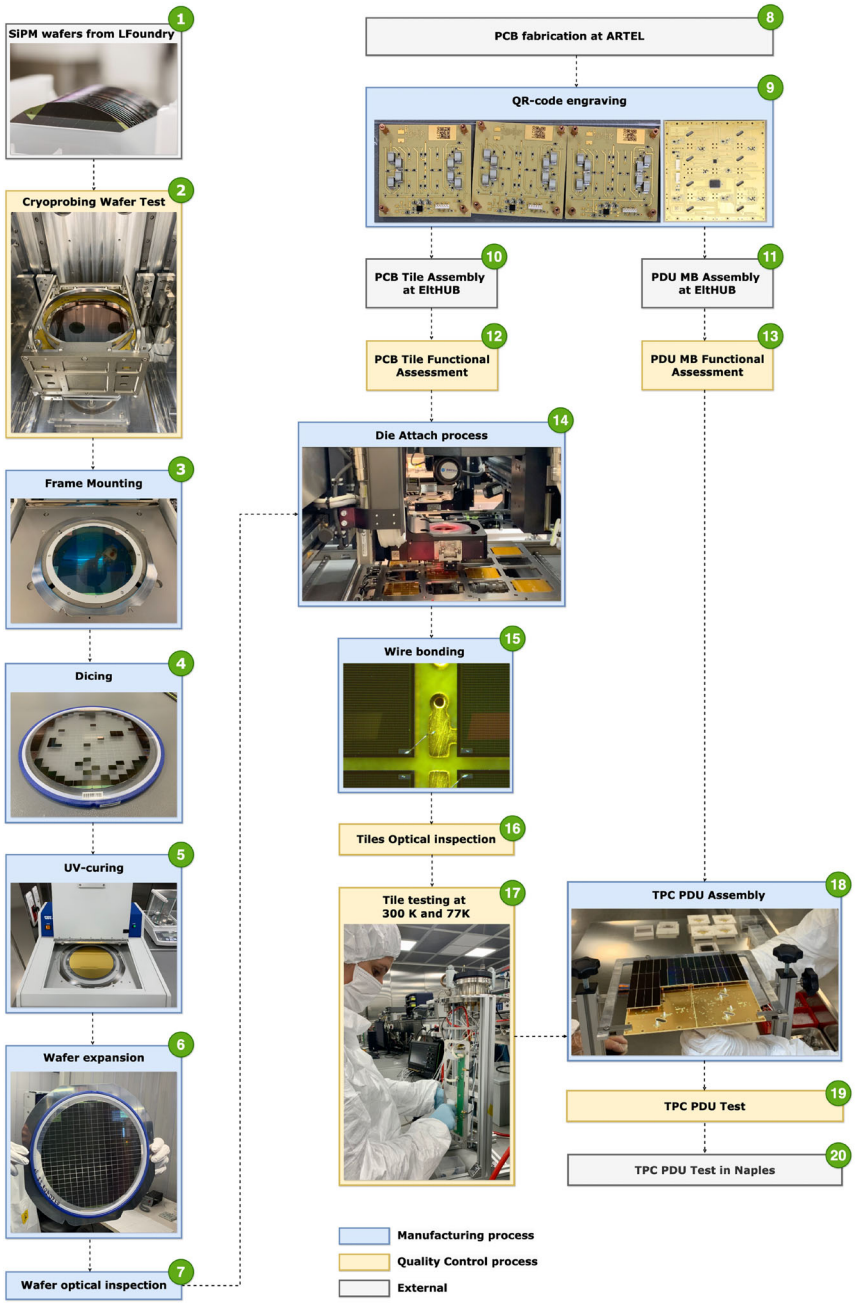

Fig. 5 Tile Production process flow in NOA. Blue boxes refer to manufacturing processes, yellow boxes to Quality Control processes and grey boxes to processes performed by external companies. Wafers from LFoundry S.r.l. (1) are characterised at cryogenic temperatures using a high-precision, semi-automated probe system (cryoprobing, 3). Faulty SiPMs are discarded. Next, wafers are mounted on a metal frame with Blue tape (4) and diced into 268 dice (5). The tape is UV-cured (6) to reduce its adhesiveness and expanded (7) for SiPM pick up. After wafer optical inspection (8), SiPMs are bonded on a PCB substrate via thermal compression (14). PDU Motherboards (MBs) and Tile PCBs from ARTEL S.r.l. (2) are engraved with a QR code (9), assembled with electrical components (10 and 11), and tested before bonding (12 and 13). SiPMs are wire bonded to PCB to connect anode and cathode terminals of two consecutive SiPMs within the same Tile branch (15). Fully mounted Tiles are inspected (16) and tested at room temperature and in liquid nitrogen with the Tile Testing Setup (17). Finally, Tiles that pass the quality criteria are used to assemble PDUs (18), which are tested at room temperature (19) before being shipped to Naples for a long-term test in liquid nitrogen (20)

to Quality Control processes and grey boxes to processes performed by external companies. This paper focuses on processes 3 to 7, 12, and 14 to 17. Processes 1 and 2 are detailed in the technical paper [10], while processes 13, 18, 19, and 20 will be described in other publications of the collaboration.

All wafers for probing are supplied by LFoundry S.r.l. (Avezzano, AQ, Italy) [21] in lots and stored in the NOA clean room (process 1 in Fig. 5).

The wafer characterisation is detailed in the DS-20k technical paper [10]. Here we only report the most relevant aspects. The wafer characterisation is carried out using a high-precision, semi-automated cryogenic probe system, the Cascade FormFactor PAC200 [22], which performs automatic electrical testing at the wafer level at a temperature of 77 K (process 2 "cryoprobing wafer test" in Fig. 5). The cryogenic characterisation of each SiPM includes measurements of the breakdown voltage, the quenching resistance, and the leakage current as a function of the bias voltage. The results of these tests are compiled into a wafer map, which is used to asses the performance of individual SiPMs. Devices that meet the specified requirements are identified as validated SiPMs, while those failing to comply with the performance criteria are excluded from deployment in the Tiles. The acceptance criteria for the SiPMs are detailed in the technical DS-20k paper [10].

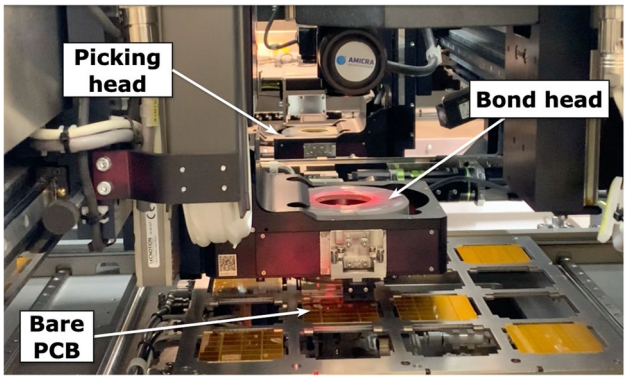

Fig. 6 SiPM assembly on the PCBs performed using an AMICRA NOVA PLUS die attacher. The custom PCB frame holder, developed to accommodate up to 16 PCBs simultaneously, is visible at the bottom

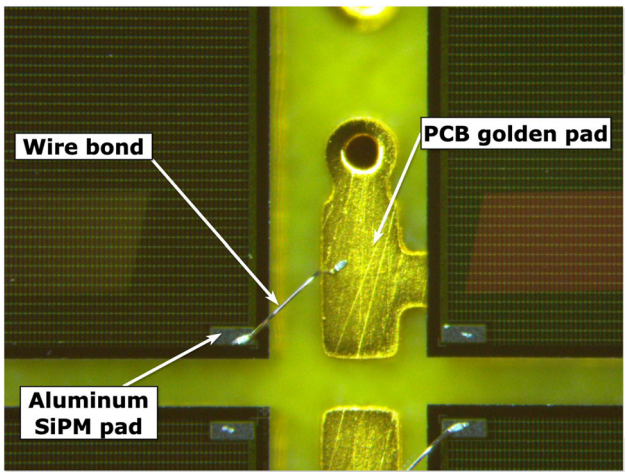

Fig. 7 Wire bonding: a low-resistance electrical contact is built between the SiPM anode and the PCB. The contact is made using a 25 µm thick aluminium conductive wire, through a wedge bonding

The throughput of the wafer characterization is 4 wafers per day, with the machine in use for (10–11) h per day, including the wafer loading, cooling, measurement, warm up, and unloading time [10].

After the characterization, each wafer is mounted on a metal frame and secured with Blue tape [23], needed to hold the wafer during the dicing process and to retain the dice after they are cut (process 3 "frame mounting" in Fig. 5). The wafer is then diced into 268 11.8 mm × 7.9 mm dice (4 "dicing" in Fig. 5) using a dicing blade with diamond particles and cooled with deionised water. After dicing, the Blue tape undergoes UV curing to reduce its adhesiveness. It is mechanically expanded to increase the spacing between the SiPMs, facilitating their pick-up during the die bonding process (processes 5 "UV curing" and process 6 "Wafer expansion" in Fig. 5).

An optical inspection using a microscope is performed to identify surface damages that occurred during wafer handling and dicing, as well as manufacturing defects that were not detected during the cryoprobe test (process 7 "Wafer Optical Inspection" in Fig. 5). Production wafers have proven to be devoid of large-scale defects; only a small number exhibited issues before the cryoprobe test. Wafer defects include surface scratches caused by the fabrication process, discoloured metal lines, black pads impacting wire bonding connectivity, and missing metallisation among the SiPM SPADs. Occasionally, surface features such as edge chipping of the SiPM are observed following the wafer dicing.

The operator has access to a list of wafer damages accompanied by pictures to facilitate the identification of defects. This additional down-selection process reduces the failure rate due to Tiles that exhibit anomalous current versus voltage (I-V) characteristic curves. The SiPMs that do not pass the optical inspection are excluded from the subsequent die attaching process. The percentage of discarded SiPMs in the optical inspection is around 3%.

The PCB substrates were manufactured by ARTEL S.r.l. [24] (Pieve al Toppo, AR, Italy) and stored in the NOA clean room (process 8 "PCB fabrication at ARTEL" in Fig. 5). Each PCB substrate then undergoes a QR code engraving process through a laser engraver LUXFIBER30-E JOKE [25] (process 9 "QR Code Engraving" in Fig. 5). With the QR code, each PCB can be uniquely identified and tracked during all the stages of the production. The time needed to engrave a packet of PCBs (20 pieces) is about half an hour, including the unpacking and repacking of the boards. An engraving rate of about 1000 PCBs per week is achieved by a full-time operator.

The bare PCBs are then sent to EltHUB S.r.l. [26] (Carsoli, AQ, Italy) for the electronic component population (process 10 "PCB Tile assembly at EltHUB" in Fig. 5). The PCBs with assembled electronics components are cleaned with demineralised water and sent back to NOA to be electrically assessed, as described in Sect. 4.1 (process 12 "PCB Tile Electrical Assessment" in Fig. 5). After cleaning, the PCBs are only handled in clean room environment.

The SiPMs are integrated on the PCBs by using an AMICRA NOVA PLUS die attacher (shown in Fig. 6). This machine is modular, tailored for micro-assembly applications, and features a placement accuracy of a few µm [27], using a thermocompression bonding technique (process 14 "Die Attach process" in Fig. 5). This packaging solution incorporates indium solder bump bondings, offering exceptionally robust bonds. The bonding tools of the machine have been customised to attach the large size SiPM dice using an indium NC-SMQ80 solder paste (18 mg to 21 mg per, where the range balances insufficient solder paste that causes die detachment and excess paste which may overflow from the SiPMs). A custom PCB frame holder has been developed to accommodate up to 16 PCBs simultaneously, optimising the assembly throughput [9].

At the start of the process, the silicon wafer is mounted on a custom metal frame and loaded into the machine. Meanwhile, the indium paste is dispensed onto the top surface of each of the PCBs following a predefined dot pattern. Only SiPMs that have been validated by both the cryoprobing (process 2) and optical inspection (process 7) are selected for integration.

SiPMs from the same wafer are bonded individually onto the tile PCBs, as shown in [10]. Each PCB is first heated to 80 °C on a chuck holder. Two bond heads, maintained at 135 °C, then execute the pick-and-place operation, precisely positioning and bonding the SiPMs with an accuracy of few µm. This process ensures a low-resistance electrical contact between the SiPM backside (cathode) and the PCB. In NOA, the die attaching machine is able to assemble up to 32 complete Tiles in 8 h of operation.

Subsequently, a wire bonding process is performed using the HESSE Bondjet BJ855 machine [28] (process 15 "Wire Bonding" in Fig. 5). This process builds an electrical contact with negligible resistance between the SiPM anode and PCB. The contact is made using a 25 µm thick aluminium conductive wire, through a wedge bonding, that joins the anode pad of the SiPM with the contact pad of the tile PCB, as displayed in Fig. 7.

The wire bonding process must establish a reliable electrical connection, resilient to temperature variations due to cryogenic operations of the devices, between the anode and cathode terminals of two consecutive SiPMs within the same branch of a Tile. Although all the SiPMs have three anode pads, the DS-20k Tile design only uses one wire between one of these pads and the corresponding cathode terminal. The time needed to wire bond a batch of 16 Tiles is about 1 h.

Fully equipped Tiles undergo an optical inspection (process 16 "Tile Optical Inspection" in Fig. 5) to verify the correct placement and the quality of the wire bonds, as well as the lack of defects. Defects in the Tile primarily arise during the die attaching stage.

The Tiles that pass the optical inspection are subsequently mounted on the Tile test setup where they undergo the quality control procedure detailed in Sect. 4.2 (process 17 "Tile Testing at room temperature and in liquid nitrogen" in Fig. 5).

The Tiles that pass the quality control procedure are used to assemble PDUs (process 18 "TPC PDU Assembly" in Fig. 5). These PDUs then undergo a room temperature test in NOA (process 19 "TPC PDU Functional Assessment", before being shipped to the Naples Photosensor Test Facility PTF, at Università di Napoli Federico II and INFN, NA, Italy) [29]. There, the PDUs undergo an electrical assessment at room temperature, followed by a long-term test in liquid nitrogen (process 20 "TPC PDU test in Napoli" in Fig. 5).

A production database maintains a record of all components employed in assembling Tiles, their progression through each stage, and measurements taken at every assembly phase. It tracks the location and shipment of each part. The database is a PostgreSQL [30], hosted at the INFN-CNAF (Italy) infrastructure and having multiple levels of backup and replication [31]. The database is accessible from the outside world only by using a password-protected API to retrieve and insert data [32]. In the production phase, various users are granted distinct access levels, depending on their particular roles in assembly or testing. A web interface provides simplified access to the database contents.

4 Tile quality assurance and quality control in NOA

The Tile performance is crucial for ensuring the reliability of light collection in the DS-20k TPC and the uniformity of the optical response across the OP. Spatial uniformity enhances energy, position, and particle-type reconstruction accuracy, particularly for pulse shape discrimination [2,33]. Moreover, the Tiles must sustain operation in a cryogenic environment without performance degradation.

Furthermore, maintaining a uniform response across the Tiles is essential when grouping Tiles in PDUs. The Tiles within a PDU are operated at a common bias voltage. Therefore, all of the Tiles must be able to operate at the maximum overvoltage to avoid the need for reducing the bias voltage or disabling individual Tiles.

The Quality Assurance and Quality Control (QA-QC) process is designed to ensure high-quality Tiles with uniform response, suitable for installation on the PDUs. The QA is the whole set of controls, procedures, and methods that we implement to ensure the quality of the product. The QC is the set of tests we put in place to detect failures. In literature, QA is often referred to as process-oriented; QC is referred to as product-oriented. Specifically, our QA-QC ensures uniformity and reliability of the Tiles by identifying defects early in production, optimising the manufacturing process, and verifying the operation in liquid nitrogen.

The quality assurance protocol guarantees that SiPMs within Tiles are sourced from the same wafer. Assembling a Tile with SiPMs from the same wafer significantly reduces SiPM-to-SiPM variability. Cryoprobing wafer tests (process "Cryoprobing wafer test", 2 in Fig. 5) have indeed shown that most variations of key performance parameters occur between different wafer lots [10]. Specifically, SiPMs within the same wafer exhibit breakdown voltages with a variance of $0.011\,\mathrm{V}^2$ and quenching resistors with a variance of $0.019\,\mathrm{M}\Omega^2$ [10]. The variability present within a wafer is due to imperfections in the manufacturing processes across the wafer's surface.

Selecting SiPMs that meet the acceptance criteria, from the same wafer, guarantees a narrow range of breakdown voltages (with nominal value 27 V at 77 K) and quenching

resistors. This helps prevent gain discrepancies when operating the SiPMs at a common bias within a Tile [10].

As part of the QA protocol, several machine parameters are measured and logged during the die bonding (process 14 in Fig. 5) and wire bonding (process 15 in Fig. 5). The continuous monitoring of the process stability and regular maintenance of the die bonding tools mitigates the risk of superficial defects on the SiPMs induced by the operation.

The constant monitoring of the wire bonding parameters (such as energy and deformation) allows us to evaluate the reliability of the wire bonding process. In addition, the quality and long-term stability of the process under various temperature conditions are evaluated through regular destructive tests of a set of wires that are bonded individually onto the golden metalisation of a PCB and the aluminium pads on two opposite SiPMs.

The quality assurance protocol also includes an initial electrical assessment of the PCB before mounting the SiPMs, as detailed in Sect. 4.1 (process 12 in Fig. 5). Fully mounted Tiles undergo an optical inspection (process 13 in Fig. 5). Subsequently, the quality of each Tile is assessed both at room temperature and in liquid nitrogen (process 13 in Fig. 5). The Tile test evaluates both the electrical conformity and the response to pulsed light, as detailed in Sect. 4.2.

Two custom LabVIEW applications were developed for the PCB electrical assessment and for the Tile quality control. The applications manage instrument interfaces, assist users through the test setup, automate the data acquisition and quality control, and archive the data in the production database.

4.1 Electrical quality control of Tile PCB

A PCB testing station (Fig. 8) was developed to execute electrical tests and to characterise the PCBs from EltHUB after the electrical components assembly (process 12 "PCB Tile functional assessment" in Fig. 5). The setup includes three structures: the "base board", the "pogo pin board" and a mechanical support.

The "base board" accommodates up to 4 PCBs alongside a microcontroller. The latter is used to drive the PD inputs of the PCBs in order to switch on and off their TIAs. The PCBs are manually connected to SMD 6-pin connectors by the user. The single-ended output of the PCBs is connected to an oscilloscope (Tektronix MSO64) via 50 Ω SMA coaxial cables to measure the TIA DC offset and to acquire the noise power spectrum. A DB25 connector connects the board to a Keithley 2450 Source Meter Unit (SMU).

The "pogo pin board" is equipped with 24 spring-loaded contacts (pogo pins) per PCB and 24 multi-pin connectors for the external Switching Multimeter (Keithley DAQ6510 equipped with a Keithley SM7702). It is used to apply the

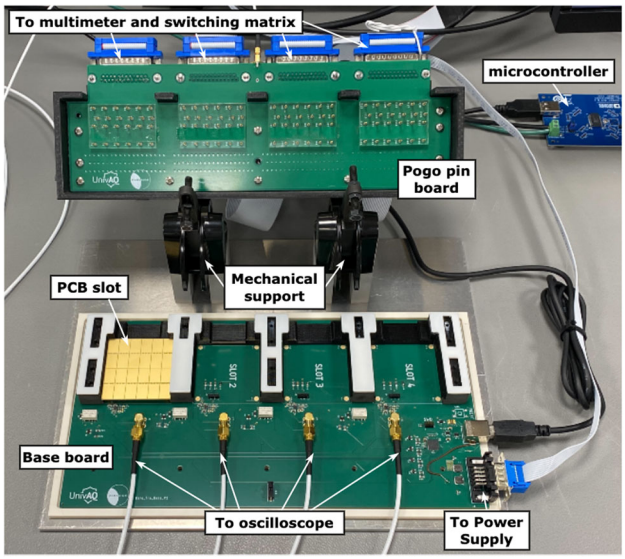

Fig. 8 Tile PCB electrical assessment setup. The testing setup is composed of a base with 4 connectors hosting 4 PCBs. A lid with a pogo pin board is placed on the PCBs to measure the passive components of the voltage divider

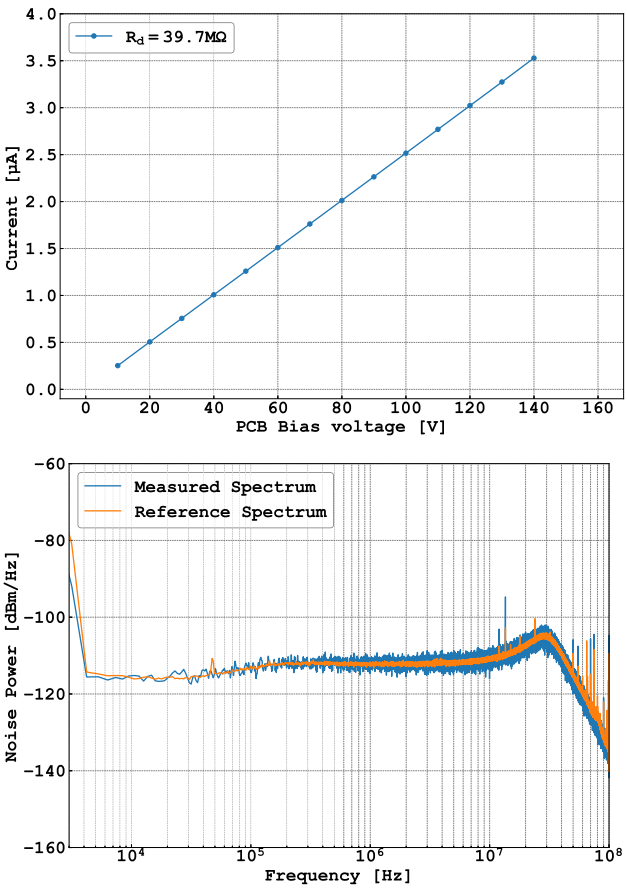

Fig. 9 PCB quality assessment. (Top) I-V curve, measured to check the linearity of the bias network within its working range and to extract its equivalent resistance. The divider resistance R_d is the reciprocal of the slope of the I-V curve. (Bottom) PCB noise spectrum compared to the reference spectrum

Table 1 Quality parameters for the PCB test. Min and Max are the boundaries of the specification range. R_d (I-V) is the equivalent divider resistance computed as the reciprocal of the slope of the I-Vcurve. R_d (SMU) is the divider equivalent resistance directly measured with the SMU at 40 V bias. The DC offset and the noise RMS are measured with the oscilloscope in the time domain. Spectrum integral is the integral of the Fast Fourier Transform (FFT) expressed in nW, and GoF represents the Goodness of Fit in a least squares comparison of the FFT with a reference shape. R_{g1}, R_{g2}, and R_{g3} are the equivalent resistances of multiple combinations of the divider components, detailed in the text. R^*_{Br} is the value of the combinations of the resistances R_{Br1} to R_{Br6} in each SiPM branch. Refer to Sect. 4.1 for more information

Parameter	Min.	Max.
R_d (I-V)	39.4 MΩ	40.1 MΩ
R_d (SMU)	39.6 MΩ	40.1 MΩ
DC offset	−150 mV	150 mV
Noise RMS	–	6.2 mV
Spectrum integral	–	900 nW
GoF	–	5
R_{g1}	14 MΩ	14.4 MΩ
R_{g2}	23.7 MΩ	24.2 MΩ
R_{g3}	33 MΩ	33.5 MΩ
R^*_{Br}	286.3 Ω	287.5 Ω

appropriate voltage to the PCBs divider resistances, thereby preventing them from remaining in a floating state.

A mechanical support is needed to apply the appropriate force on the pogo pin board (60 g for each pin) and to hold and stabilise the "base board" and the pogo "pin board".

The duration of a full electrical test is about 15 min for 4 PCBs. At the start of each test, the current consumption of the PCB is measured under nominal LV conditions of ± 2.5 V, all while applying no bias voltage. The first part of the test consists of measuring the characteristic current–voltage curve with the SMU. The measurement of the I-V curve of the PCB is performed to check the linearity of the bias network within its working range and to extract its equivalent bias resistance through a linear regression. The divider resistance R_d is computed as the reciprocal of the slope of the I-V curve. An example of an I-V curve is shown in Fig. 9 (top).

The second part of the test is the assessment of the noise characteristics using the oscilloscope. The noise characterisation is performed at 40 V of bias voltage. For each PCB under test, the oscilloscope returns the measure of the DC offset, the noise RMS, and the noise Fast Fourier Transform (FFT). The typical shape of a noise spectrum is shown in Fig. 9 (bottom). For each of the spectra, an assessment is carried out in the frequency range between 100 kHz and 9.6 MHz. In this range, we compute the integral of the spectrum and a least square comparison with respect to a reference noise curve, hereby called Goodness of Fit (GoF). A detailed description of the GoF computation is given in Sect. 4.2.4.

The quality checks on the noise features (refer to Table 1) ensure that the PCB has DC offset and noise levels within specifications and that the spectrum is compatible with that of a PCB in which all components have their assigned values within the expected tolerance and are assembled correctly.

In the third part of the PCB test, the discrete components mounted on the PCB are evaluated by measuring the current draw at specific points of the circuit when the bias network is supplied with 40 V, and by measuring a set of equivalent resistances in the PCB voltage divider using the custom pogo pin board.

The 10 MΩ network of the voltage divider ("Passive V_{bias} Divider" in the orange shaded area of Fig. 3) is assessed by measuring some equivalent resistances using the Switching Multimeter and the SMU. The equivalent resistances R_{g1}, R_{g2}, and R_{g3} under test are defined as

$$R_{g1} = R_{d1} + \left(R_{(1,7,13)} // R_{(4,10,16)} // \left(R_{d2} + R_{d3} + R_{d4}\right)\right), \quad (1)$$

$$R_{g2} = R_{d1} + R_{d2} + \left(R_{(2,8,14)} // R_{(5,11,17)} // \left(R_{d3} + R_{d4}\right)\right), \quad (2)$$

$$R_{g3} = R_{d1} + R_{d2} + R_{d3} + \left(R_{(3,9,15)} // R_{(6,12,28)} // R_{d4}\right), \quad (3)$$

where the "+" and "//" symbols indicate series and parallel combinations, respectively, and the subscripts with parenthesis denote which resistor is used in each specific measure (for instance, R_{g1} is measured three times, once with the parallel of R_1 and R_4, then R_7 and R_{10} and finally R_{13} and R_{16}). The nominal values of R_{g1}, R_{g2} and R_{g3} are 14.3 MΩ, 24 MΩ, and 33.3 MΩ, respectively, with a tolerance of about 0.5 MΩ.

The Switching Multimeter is then used to asses the resistors R_{Br1} to R_{Br6} in each parallel branch of the *4s6p* network (refer to Fig. 3). Since a direct measurement of these resistors is not possible, an indirect measure of five equivalent resistors is performed. This process involves fixing one resistor in the positive pole and measuring its series resistance with combinations of the remaining five resistors. These resistors are sequentially grounded using the internal generator of the Keithley DAQ6510, configured in multimeter mode. The combinations of the five resistors are:

$$R^{(1+2)}_{Br} = R_{Br1} + R_{Br2} \quad (4)$$

$$R^{(1+3)}_{Br} = R_{Br1} + R_{Br3} \quad (5)$$

$$R^{(1+4)}_{Br} = R_{Br1} + R_{Br4} \quad (6)$$

$$R^{(1+5)}_{Br} = R_{Br1} + R_{Br5} \quad (7)$$

$$R^{(1+6)}_{Br} = R_{Br1} + R_{Br6} \quad (8)$$

The nominal value of each of the R^*_{Br} is twice 143 Ω with a tolerance of about 1 Ω.

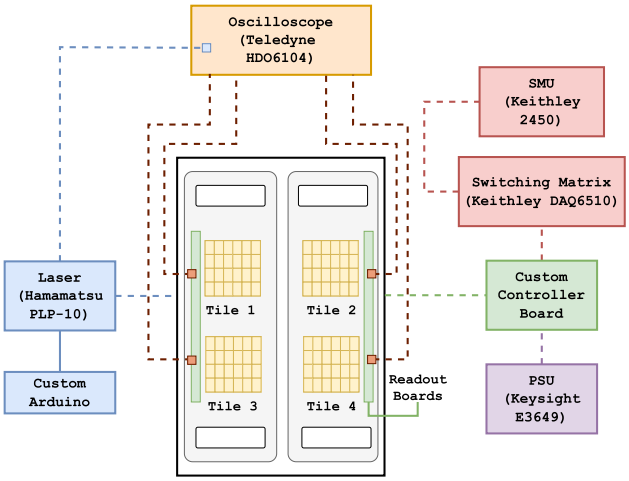

Fig. 10 Schematic representation of the Tile Testing Setup. The black box represents the dewar, where up to four Tiles can be mounted in pairs on two mechanical holders. Signals from the Tiles are acquired through a Teledyne HDO6104A oscilloscope. Tiles are illuminated by an optical fibre connected to an external laser source (Hamamatsu PLP-10), which is triggered by a custom Arduino. A custom controller board housing an onboard microcontroller drives the power down of the Tiles and triggers temperature checks. A Power Supply Unit (PSU, Keysight E3649) provides the Low Voltage (LV) to the electrical part of the Tiles. The Source Meter Unit (SMU, Keithley 2450) generates the bias voltage, and a Switching Matrix (Keithley DAQ6510) provides it to the Tile under test. All the instruments are connected to a local computer through USB connections, except the PSU which uses GPIB. The Custom Controller Board and Arduino are connected via Ethernet

Finally, the equivalent divider resistance R_d is measured by employing the pogo pin alongside the SMU resistance measurement mode, at an input bias voltage of 40 V. This approach might yield a result that deviates slightly from the slope of the I-V curve, as it is sensitive to the 10 MΩ resistors R_1 to R_{16} in Fig. 3.

The PCB quality control relies on the parameters listed in Table 1. The ranges were initially set according to the tolerances, then fine-tuned to exclude the outliers in the measured distributions. A PCB is considered accepted when all the quality parameters are within the specifications. The divider resistance R_d is evaluated with two different methods because of its substantial influence on Tile's performance.

4.2 Tile quality control

The quality control on the Tiles happens during process 17 ("Tile testing at 300 K and 77 K" in Fig. 5). The test is divided into two stages: an initial assessment at room temperature to identify potential electronic failures, followed by a second test in liquid nitrogen (77 K) to evaluate the Tile performance. The electrical behaviour of a Tile is expected to remain consistent when immersed in liquid argon, which has a boiling point of approximately 87 K.

The test starts with an initial assessment of the current drawn at zero bias voltage to check the electrical connections (Sect. 4.2.2). The test proceeds with a measure of the I-V curve in reverse bias, detailed in Sect. 4.2.3, which allows

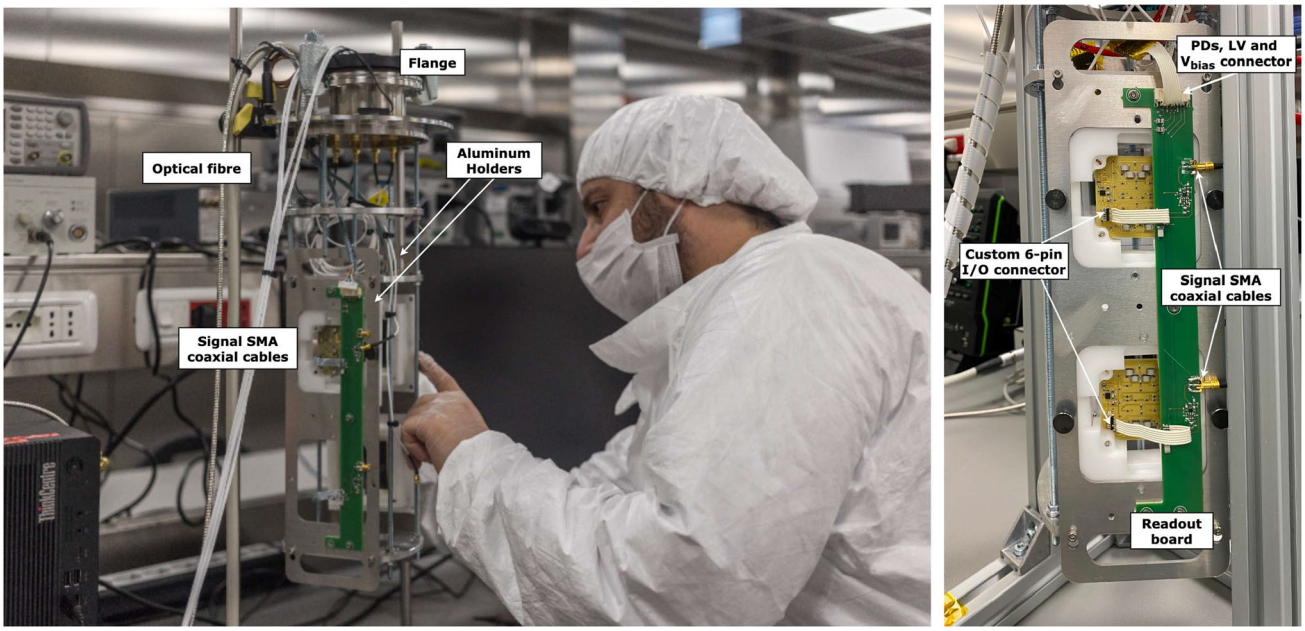

Fig. 11 Mechanical structure of the Tile Testing Setup. Four Tiles are mounted in pairs on two aluminium holders secured to the main frame. The Tiles' output signals are amplified by custom readout boards and connected to an oscilloscope via SMA coaxial cables exiting from the flange. The latter is also equipped with an optical fibre connected to a laser and illuminating the four Tiles

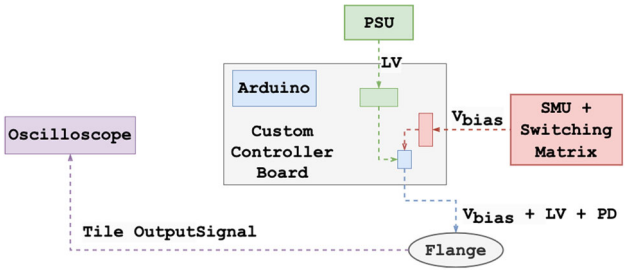

Fig. 12 Schematic representation of the bias voltage V_{bias} and Low Voltage (LV) paths through the custom controller board

Table 2 Quality assurance requirements for the low voltage (LV) current drawn with the Tile powered down (I_{LV}^{off}) and turned on (I_{LV}^{on}). The criteria have been tuned to identify a poor connection of the Tile with the measurement setup

Parameter	Temperature	Min.	Max.
I_{LV}^{off}	300 K	60 mA	71 mA
	77 K	35 mA	52 mA
I_{LV}^{on}	300 K	74 mA	87 mA
	77 K	44 mA	62 mA

the extraction of the breakdown voltage and measurement of the Tile voltage divider resistance. Subsequently, the noise RMS and the noise power spectrum are acquired with an oscilloscope, as detailed in Sect. 4.2.4. The test in liquid nitrogen includes a pulse counting measurement with a laser source. This process entails collecting pulse waveforms to evaluate their adherence to our quality criteria, as detailed in Sect. 4.2.5.

The total time needed to complete one full test, hence four Tiles, is about 1 h, including the time needed to warm up the Tiles after the test in liquid nitrogen.

4.2.1 Hardware setup

The Tiles are tested using a custom setup which can carry up to four units. A schematic representation of the Tile testing setup is shown in Fig. 10. Two identical Tile test setups are available in NOA, to increase the Tiles production throughput.

Before each measurement, the four Tiles under test are first tightly screwed on a plastic support and protected by an acrylic cover and then mounted in pairs on two aluminium holders, which are secured to the main frame (Fig. 11).

The mechanical structure is positioned inside a dewar, equipped with a sealed flange featuring a venting copper tube and electrical and optical feedthroughs. Four coaxial SMA connections are employed for the output signal transmission and connected to the Tiles via custom readout boards. The two readout boards serve as an impedance adapter between the output of the Tiles and the oscilloscope, also providing a tenfold amplification of the signals via an onboard operational amplifier. The Tile output signals are then acquired with an oscilloscope (Teledyne HDO6104A).

Additionally, a hermetically-sealed optical fibre feedthrough is integrated to allow the Tiles to be illuminated by an external laser source (Hamamatsu PLP-10), triggered by a custom Arduino [34]. The fibre is terminated with a cylindrical plastic diffuser and placed between the four Tiles to improve the uniformity of the illumination. The setup also includes a custom controller board housing an onboard microcontroller (Adafruit Feather M0, SAMD21 [35]), which triggers temperature checks and drives the power down of the TIA (refer to Fig. 4), which is needed to turn on and off each Tile individually. The custom controller board is also responsible for distributing the utilities to the Tiles. The board is connected to a local computer via Ethernet. A Power Supply Unit (PSU, Keysight E3649) provides the Low Voltage (LV) to the PCB (Fig. 4), while the SMU (Keithley 2450) generates the bias voltage (V_{bias}, refer to Fig. 3) needed to bias the SiPMs. A Keithley DAQ7702 Switching Matrix is used to deliver V_{bias} to the Tile under test. Figure 12 shows a schematic representation of the V_{bias} and LV paths through the controller board. To perform the test in liquid nitrogen, the mechanical structure is slowly inserted into the dewar to avoid abrupt temperature changes. After the test in liquid nitrogen, the Tiles are moved inside a cylinder, where they are thermalised using a flow of heated gaseous nitrogen to prevent condensation.

4.2.2 LV current assessment

At the beginning of each test, the current consumption of the Tile is measured under nominal LV conditions ($\pm$ 2.5 V) without any bias voltage. When the Tile is not biased, the current (I_{LV}^{off}) is mostly absorbed by the amplifying readout boards (refer to Sect. 4.2.1); when the Tile is powered, the current (I_{LV}^{on}) is also drawn by the TIA. Typical average values include 66 mA for the readout boards and 15 mA for the TIA at room temperature, whereas in liquid nitrogen, these values drop to 39 mA and 11 mA, respectively. Table 2 details the current consumption criteria. If these specifications are not satisfied, it is usually due to a poor connection of the Tile within the measurement setup.

4.2.3 I-V curve quality control

The I-V of each Tile in reverse-bias mode is obtained using a SMU Keithley 2450. The measure is acquired both at room temperature, in a separate dewar, and in liquid nitrogen. During the liquid nitrogen measurement, a laser source at 16 MHz and maximum intensity is illuminating the Tiles. Such a high

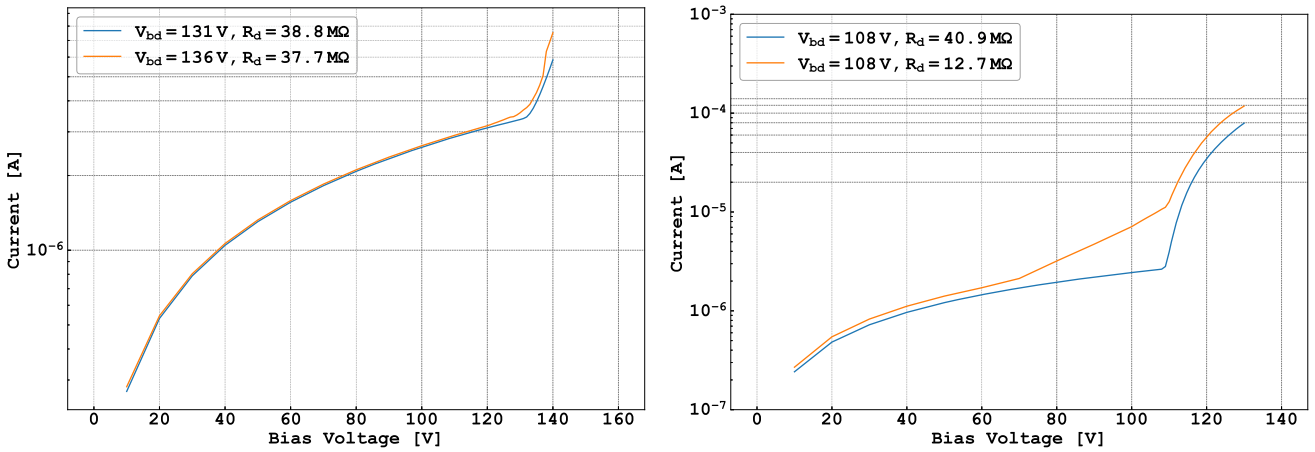

Fig. 13 I-V curves examples at room temperature (Left) and in liquid nitrogen (Right). The blue curves belong to Tiles that passed the quality control, indicating that the tile breakdown voltage V_{bd} and the divider resistance R_d are within the acceptance ranges. Conversely, the orange curves belong to a Tile with quality parameters that deviate from the requirements

Table 3 Quality parameters for the I-V curves and requirements at room temperature (300 K) and in liquid nitrogen (77 K). The parameter V_{bd} is the breakdown voltage, and R_d is the equivalent resistance of the voltage divider

Parameter	Temperature	Min.	Max.
V_{bd}	300 K	130.9 V	133 V
	77 K	107 V	110.1 V
R_d	300 K	38 MΩ	39.5 MΩ
	77 K	40.2 MΩ	41.5 MΩ

light flux is needed to induce a current of the order of tens of μA to overcome the divider current.

The voltage sweep is performed with a 10 V step where the linear region of the I-V curve is expected. Here, the current flows through the Tile voltage divider. On the other hand, a step of 1 V is used for the region where the breakdown is foreseen. At room temperature, the former is 10 V to 120 V and the latter is 121 V to 140 V, while in liquid nitrogen the ranges are respectively 10 V to 100 V and 100 V to 120 V (the nominal breakdown voltage of a SiPM at 77 K is 27 V, corresponding to 108 V for a Tile). A one-second delay is introduced between the voltage being applied and the current measurement. The current is measured five times for each voltage, with the median value recorded to mitigate the impact of fluctuations and outliers when adjusting the bias.

The parameters estimated from the I-V curve to asses the electrical functioning of the Tile are the Tile breakdown voltage V_{bd} and the equivalent resistance of the bias voltage divider, R_d.

The Tile breakdown voltage V_{bd} is the turning point of the I-V curve in the reverse bias region. The nominal value of V_{bd} for each Tile is 131 V at room temperature and 108 V in liquid nitrogen. We define the "turning point" of the I-V curve as the voltage corresponding to the maximum of the second derivative of the logarithm of the current,

$$\left.\frac{d^2\,(\ln I)}{d\,V^2}\right|_{V=V_{bd}} = \max\,. \tag{9}$$

The derivatives are computed via finite difference methods. The first derivative at point n is obtained by subtracting the value at point n from that at point $n+1$. Similarly, the second derivative follows the same calculation process. Subsequently, the algorithm identifies the maximum value in the second derivatives array, represented by the index n. Consequently, V_{bd} is estimated as the voltage corresponding to index $n+1$.

This second derivative method is distinct from the first derivative approach previously employed in the wafer quality assurance procedure for estimating the breakdown voltage of the SiPMs [10]. For the individual SiPMs, V_{bd} is determined as the voltage at which the first derivative of the current reached its peak. Because the Tiles incorporate a resistor divider, the post-breakdown curve does not rise as sharply as it does in the SiPMs. As a result, using the first derivative becomes less reliable for identifying the transition point due to the less pronounced peak in its curve. Conversely, the second derivative offers a more accurate indication of the transition point.

The current flowing prior to breakdown is the one that passes through the Tile voltage divider. The nominal value of its equivalent resistance R_d is about 40 MΩ, corresponding to the series combination of the four 10 MΩ resistors that make up the Tile voltage divider (refer to Fig. 3). At room temperature, the measured value is slightly lower due to the leakage currents of the SiPMs. The parameter R_d is estimated

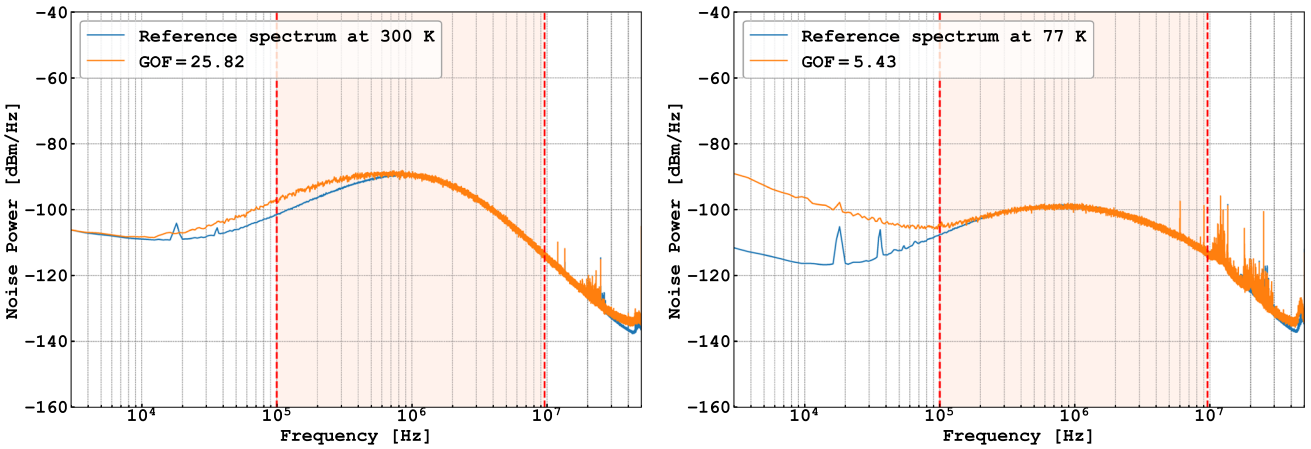

Fig. 14 Noise spectra examples at room temperature (left) and in liquid nitrogen (right). The blue curves represent the reference noise spectra. Conversely, the orange curves represent Tiles with at least one quality parameter deviating from these requirements. The shaded area indicates the region where the Goodness of Fit parameter is evaluated (100 kHz to 9.6 MHz). In this case, the Goodness of Fit parameter (GoF) of the orange curve does not meet the specifications

from the I-V curve as the reciprocal of the slope determined by a linear regression conducted in the nominal linear region.

This parameter is primarily employed to detect suboptimal I-V curves, such as those exhibiting another, albeit milder, deviation from linearity significantly below V_{bd} (for instance, approximately 70 V in Fig. 13). This phenomenon, known as *double slope* or *double breakdown*, leads to an estimate of the equivalent R_d that is significantly lower than our acceptance range.

Table 3 lists the quality requirements for the parameters V_{bd} and R_d. The requirement on V_{bd} is established to accept Tiles populated with working SiPM with nominal breakdown voltage. The acceptance range on R_d has been fine-tuned to exclude Tiles which exhibit the double slope feature.

Figure 13 shows some examples of I-V curves measured at room temperature and in liquid nitrogen. Each plot includes the results of the quality test. In both figures, the blue curves belong to a Tile that passed the quality control on the I-V curve, indicating that both V_{bd} and R_d are within the specifications of Table 3. Conversely, the orange curves belong to Tiles that deviate from the quality specifications.

4.2.4 Noise quality control

The noise root mean square (RMS) and the noise power spectrum for each Tile under test are measured using a Teledyne HDO6104A oscilloscope. These measures occur both at room temperature and in liquid nitrogen, at 40 V bias voltage, significantly below the Tile breakdown voltage, so that the avalanche generation in the SiPMs is suppressed.

In *Spectrum* mode, the oscilloscope directly measures the power spectrum. We collect the average power spectrum across 100 waveform triggers, each having a duration

Table 4 Quality parameters on the Tile noise at room temperature (300 K) and in liquid nitrogen (77 K). The absolute value of the DC offset and the noise RMS measured by the oscilloscope in the time domain, Spectrum integral is integral of the power spectrum expressed in μW, and GoF is the Goodness of Fit

Parameter	Temperature	Requirement
DC offset	300 K	< 180 mV
	77 K	< 150 mV
Noise RMS	300 K	< 9 mV
	77 K	< 4.1 mV
Spectrum integral	300 K	$\in (2.0\,\mu\text{W}, 2.5\,\mu\text{W})$
	77 K	$\in (0.32\,\mu\text{W}, 0.5\,\mu\text{W})$
Spectrum GoF	300 K	< 3
	77 K	< 4

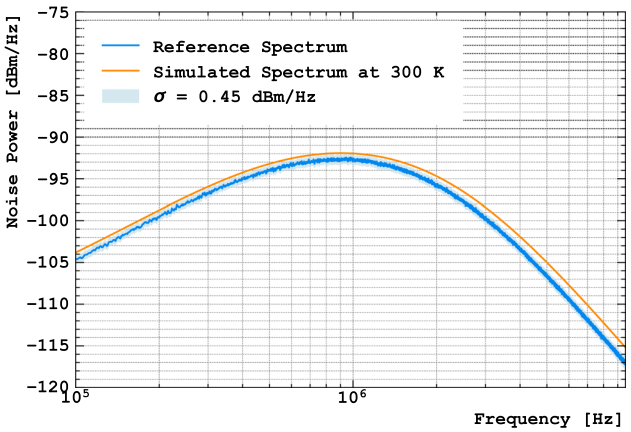

Fig. 15 Noise spectrum of the Tile simulated with the TINA-TI software (orange) compared to the noise spectrum of a reference Tile at room temperature (blue). The shaded region displays the error band including the statistical uncertainty

of 0.2 ms, sampled at 250 MSample/s and constrained by a bandwidth limit of 200 MHz. The oscilloscope returns the power spectrum in dBm, with a resolution bandwidth of about 2 kHz. Examples of noise spectra are shown in Fig. 14. For the same set of data, the oscilloscope also returns the noise RMS and the DC offset.

The analysis of the noise spectrum is conducted within the frequency range spanning from 100 kHz to 9.6 MHz, as this is the range of interest for the Tile's output signals. Above this range, high-frequency spikes due to electromagnetic pick-up from the signal cables pollute the analysis outcome. Below this range, the rising spectrum at low frequency observed in some Tiles is attributed to burst noise linked to production defects in the TIA and can be solved by replacing the chip.

The spectra are then normalised by converting the output spectrum of the oscilloscope from dBm to mW. The integral of the spectrum (in units of Watt) is computed in the frequency range 100 kHz to 9.6 MHz. A low value of the spectrum integral is typically due to detached branches in the SiPM bias network.

A GoF parameter is introduced to quantify the similarity to a noise spectrum of a Tile, where each component is assembled correctly and meets its designated value within the acceptable tolerance. The GoF is defined as:

$$\mathrm{GoF} = \frac{1}{N-1} \sum_{i=1}^{N} \frac{(y_i - k\bar{Y}_i)^2}{\sigma^2}, \tag{10}$$

Here, y is the value of the spectrum under evaluation, $\bar{Y}$ is the value of the reference spectrum, the subscript i refers to the i-th of the N points in the set, σ is the statistical uncertainty on the reference, and k is a global scale factor to parametrise small deviations to the reference. The GoF is minimised with respect to k.

The GoF is computed for a set of $N = 7$ frequencies chosen to have a flat distribution in logarithmic space (i.e. 100 kHz, 200 kHz, 400 kHz, ..., 6.4 MHz). This choice guarantees that deviations in the frequency range between 100 kHz and 1 MHz count as much as deviations in the frequency range between 1 MHz and 10 MHz.

The reference spectrum shape is computed as an average among 16 Tiles of good quality in the early stages of production. The scale factor k is introduced to account for small differences in environment noise levels between measurements. Typically, k differs from unity by less than one per cent. The statistical uncertainty σ was evaluated as the standard deviation of a flat sub-range of the spectrum values around the peak and corresponds to 0.45 dBm/Hz.

The experimental GoF distribution is close to a reduced χ^2 distribution with $N-1$ degrees of freedom, with a distinct peak around 1. A higher value of this parameter is often a hint of defects in the Tile electronics, such as the detachment of one or more of the branches in the SiPM bias network, typically resulting from faulty or missing wire bonds.

As a cross-check on the reference shape at room temperature, the Tile noise spectrum was simulated with the TINA-TI software [36] by reproducing the Tile circuitry. The simulated output spectrum is compared to the acquired data. The input parameters of the simulation are the Tile circuit elements discussed in Sect. 2 and the parameters included in the SiPM equivalent electrical model, namely a collection of microcells, each of them modelled as an avalanche photodiode operated in Geiger mode and passively quenched through a series resistor. The model used here is derived from [37,38].

The simulation reproduces the shape of the measured spectrum within 2%, as shown in Fig. 15 in the range of interest for the noise spectrum quality assurance.

The simulation cannot be performed at cryogenic temperature, as the software does not include the cryogenic characterisation of the TIA down to 77 K. However, a simplified calculation can be performed to obtain the expected maximum of the spectrum in liquid nitrogen at 1 MHz, as detailed in [12]. This can be achieved by summing the following contributions: (i) the voltage noise, which is the sum of the intrinsic voltage noise of the TIA and the Johnson-Nyquist voltage noise of the resistive components of the circuit (~ -171 dBm), (ii) the asymptotic noise gain (~ 50 dBm) and (iii) the amplification factor given by the readout boards (~ 20 dBm). Thus, the expected maximum in liquid nitrogen is -101 dBm/Hz, in excellent agreement with the measurements, as shown in Fig. 14.

The quality parameters related to the noise measurements are the DC offset, the noise RMS, the integral of the power spectrum and the GoF. Table 4 lists the quality requirements on these parameters. We confirmed that a Tile with an intentionally removed branch in the SiPM bias network did not pass the test.

4.2.5 *Pulse quality control*

The characterisation of the Tile pulse output signals is performed to asses the quality of the Tiles when exposed to a pulsed light source. In this procedure, the Tile is submerged in liquid nitrogen and illuminated by a Hamamatsu PLP-10 picosecond laser of 400 nm wavelength, operating at 500 Hz. The laser's intensity is attenuated to ensure that the Tile works within the few-photon range.

The Tile output signal is acquired using the oscilloscope, which is triggered by the sync signal from the Hamamatsu laser module. The oscilloscope is configured to acquire waveforms that are 5 µs in duration, sampled at 250 MSample/s. The signal starts approximately 1 µs after the waveform begins. The vertical range of the oscilloscope is adjusted to 0.8 V to account for potential DC offset shifts and large signal pulses.

Table 5 Quality parameters for the pulse assessment. The overvoltage refers to a nominal SiPM with 27 V breakdown voltage. Single Photo-Electron (SPE) mean, resolution, and Single-to-Zero Ratio (SZR) are estimated from the corresponding finger plot. Refer to Sect. 4.2.5 for the detailed definition and computation

Parameter	Tile Bias Voltage (V)	SiPM Overvoltage (VoV)	Minimum	Maximum
SPE mean (amplitude)	136	7	41 mV	50 mV
SPE mean (amplitude)	144	9	53 mV	65 mV
SPE mean (charge)	136	7	16 nV s	28 nV s
SPE mean (charge)	144	9	20 nV s	34 nV s
SPE resolution (amplitude)	136	7	–	0.11
SPE resolution (amplitude)	144	9	–	0.09
SZR (amplitude)	136	7	13.5	–
SZR (amplitude)	144	9	18.5	–
τ_{rise}	136	7	70 ns	100 ns
τ_{rise}	144	9	70 ns	100 ns
τ_{fall}	136	7	250 ns	390 ns
τ_{fall}	144	9	270 ns	390 ns

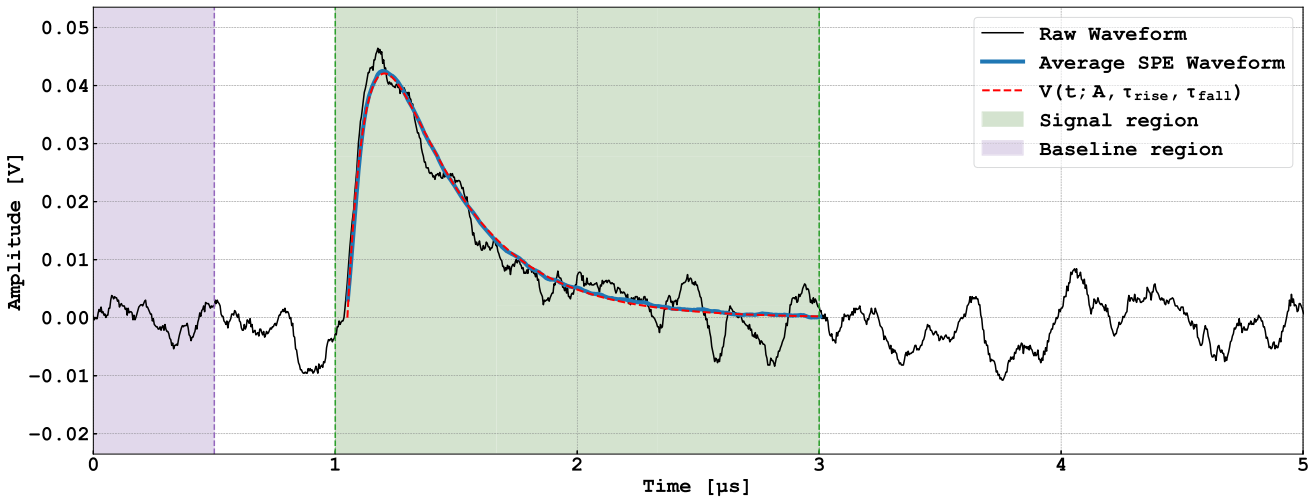

Fig. 16 Example of a raw pulse waveform in the Single PhotoElectron (SPE) regime, acquired at 7 VoV. The amplitude and charge (integral) of the pulse are evaluated in the *Signal region* (shaded in green). The region where the baseline is computed (shaded in violet) is in the first 0.5 µs. The blue line is the average SPE waveform. The red dashed line is the best fit to the average SPE waveform with the model in Equation 12. More details are given in the text

The acquisition is repeated with the Tile supplied at 4 different bias voltages: 132 V, 136 V, 140 V, and 144 V, which correspond to about 6, 7, 8, and 9 Volt over voltage (VoV) for SiPMs with nominal breakdown voltage of 27 V. For each bias voltage, 10,000 oscilloscope triggers are acquired (the number of triggers was 2500 before the fifth month of production). An example of a raw SPE waveform collected at 7 VoV is displayed in Fig. 16. The collected raw waveforms are saved in binary format and securely stored on a DS-20k server at LNGS. This method facilitates reanalysis of all the Tile pulse data, should there be any modification in the analysis procedure.

Before acquiring all triggers over the 4 different bias voltages, the LabVIEW application conducts an initial data acquisition at the highest overvoltage and displays a histogram of the amplitude distribution to the user. These histograms, commonly referred to as *finger plots*, typically display 4–5 peaks resembling fingers. It is mandatory for the user to ensure the initial two peaks are discernible and that the laser intensity is set so that the peak with the most entries falls in either the first or second position. The user can continue to adjust the laser intensity and view additional preliminary acquisitions until this condition is satisfied.

The data analysis starts by estimating the baseline, signal amplitude, and signal charge for each waveform gathered. The baseline is determined by averaging the waveform values from its start to 0.5 µs. This calculated baseline is then subtracted from the waveform. The signal amplitude is iden-

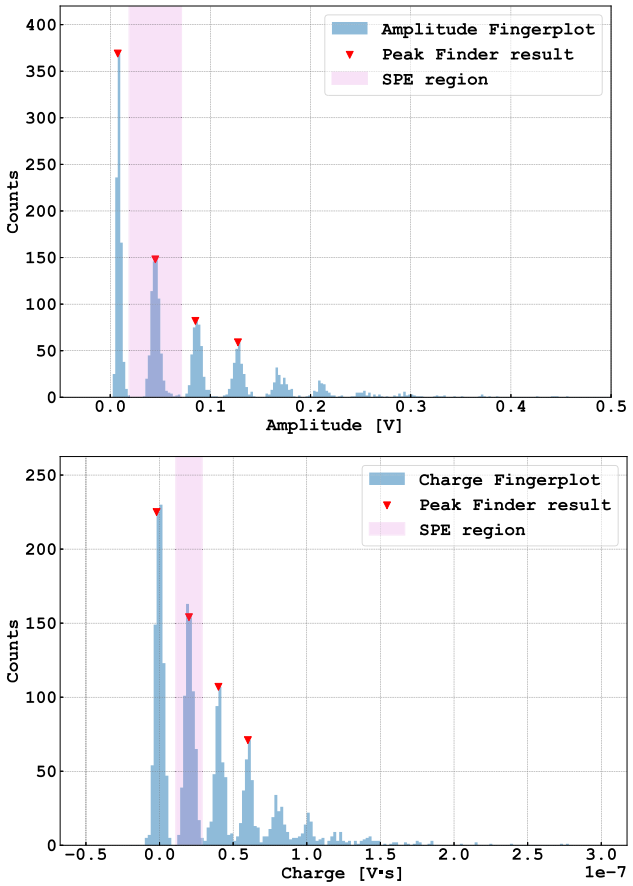

Fig. 17 Example of an amplitude and charge fingerplot acquired at 7 VoV. The peak finder algorithm correctly determines the abscissa of the peaks. The Single PhotoElectron (SPE) region is shaded in pink

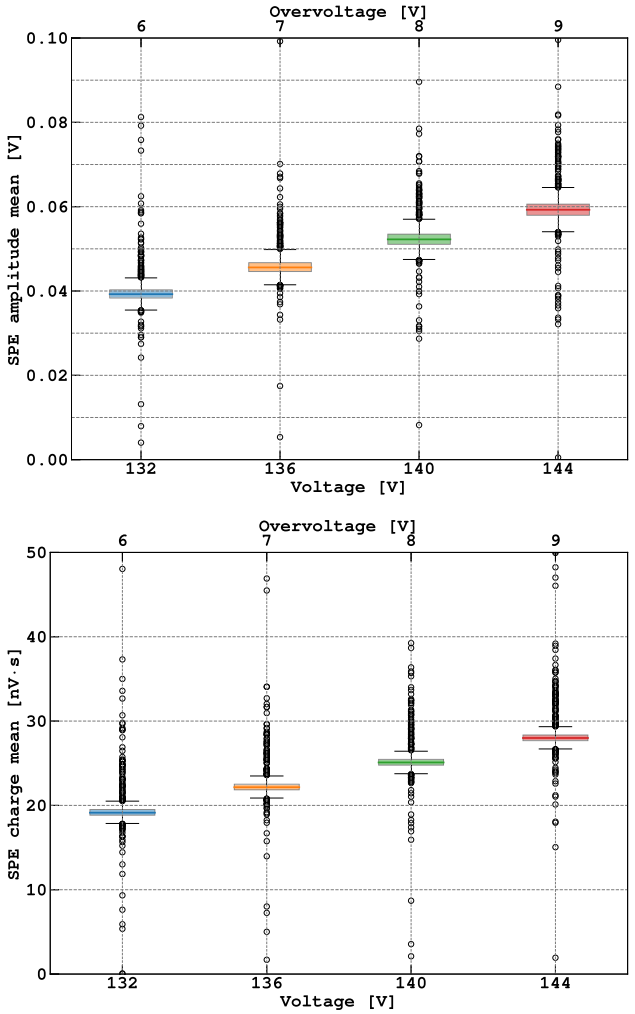

Fig. 18 Single PhotoElectron (SPE) amplitude boxplot (top) and charge (bottom) as a function of the bias voltage and overvoltage. Boxes represent data between the first and third quartiles. Dots represent outliers more than 1.5 InterQuartile Range (IQR) away from the top or bottom of each box

tified as the highest value of the waveform after baseline subtraction within the 1 to 3 µs interval. The signal charge is obtained by integrating the baseline-subtracted waveform over this same interval, employing the trapezoidal method for integration.

Upon processing each of the 10,000 waveforms per bias voltage, we populate two histograms: one for the amplitude distribution and another for the charge distribution. An example of these distributions is provided in Fig. 17. The amplitude histograms are divided into 200 bins ranging from 0 V to 0.5 V, while the charge histograms consist of 150 bins spanning from −20 nV s to 280 nV s.

Once the finger plots are complete, a peak detection algorithm identifies the peak positions in the histograms. Two types of peak detection algorithms were compared and adjusted to yield reliable results. The first is the Peak Detector from LabVIEW's Signal Processing library, utilising an algorithm that fits a quadratic polynomial to sequential groups of data points. The second employs the TSpectrum module from the ROOT library, which instead fits normal distributions. Post-tuning, both algorithms pinpoint the abscissa of the peaks with discrepancies under a few per cent, provided there is sufficient data (several hundred events per peak).

Peak positions are solely employed to delineate the zero PhotoElectron (0-PE) and Single PhotoElectron (SPE) regions within the finger plots. The boundary between the 0-PE and SPE regions is established by calculating the midpoint between the abscissae of the first and second peaks. The 0-PE region extends from the beginning of the histogram to this demarcation point. The SPE region, equal in width, begins at the end of the 0-PE region and encompasses the SPE peak.

After pinpointing the SPE region in the finger plot, its entire content undergoes fitting with a Gaussian distribution. The term *SPE amplitude* refers to the mean obtained from fitting the SPE region in the amplitude finger plot. Similarly, in the charge finger plot, the *SPE charge* is determined using the same method. Figure 18 illustrates the median of the distribution of SPE means as a function of bias voltage and overvolt-

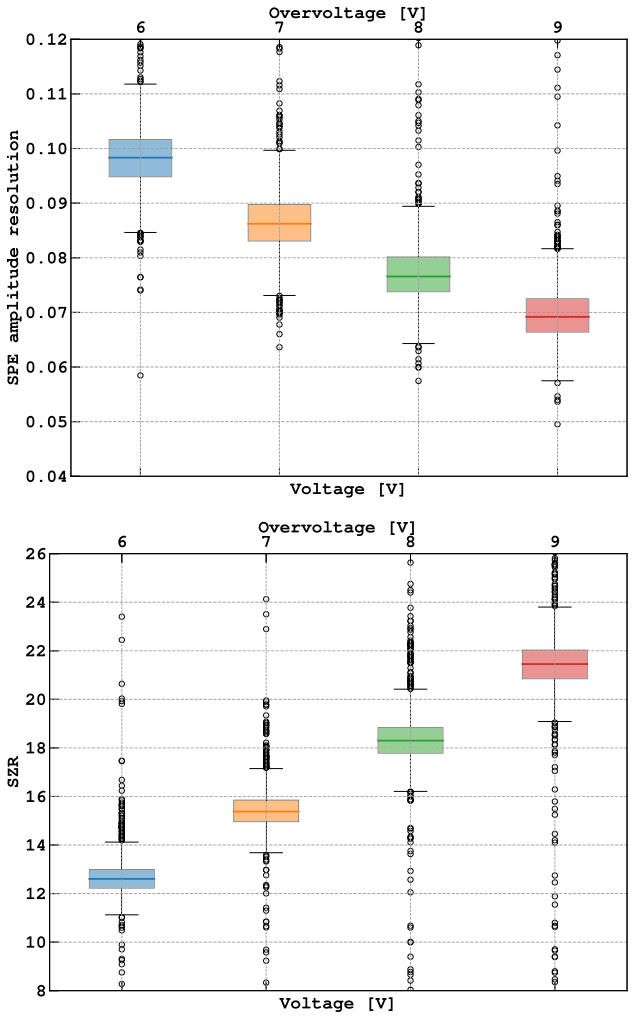

Fig. 19 Single PhotoElectron (SPE) resolution boxplot (Top) and Single-to-Zero Ratio (SZR) (Bottom) as a function of the bias voltage and overvoltage. Boxes represent data between the first and third quartiles. Dots represent outliers more than 1.5 InterQuartile Range (IQR) away from the top or bottom of each box

age, highlighting the range of the distribution (boxes) and its outliers. Dots represent outliers more than 1.5 InterQuartile Range (IQR) away from the top or bottom of each box. The median of the distribution indicates an approximately linear upward trend.

The *SPE resolution* is defined as the ratio of the fitted σ to the mean within the SPE region. By fitting across the entire SPE region, we can include both longer tails and false peaks as increases in the Gaussian's σ. This allows us to identify Tiles with less-than-ideal peaks. Figure 19 (top) presents how the SPE resolution (derived from the amplitude finger plot) varies with bias voltage and overvoltage, by displaying the median of the SPE resolution distribution, its range (boxes) and its outliers. The resolution tends to improve as the overvoltage is raised.

A Gaussian fit is also used to model the content of the whole 0-PE region. The mean and the σ of the Gaussian in

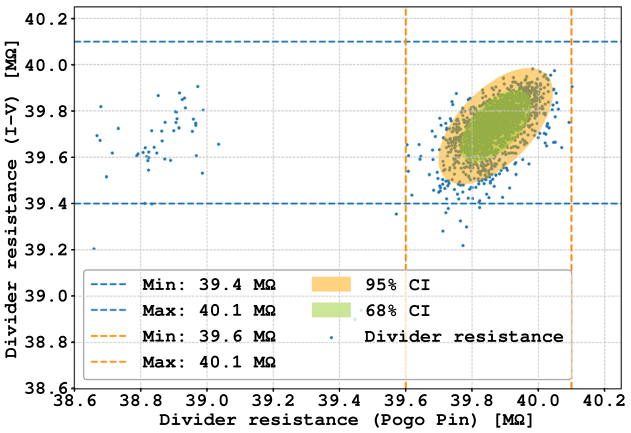

Fig. 20 Measurements of the Tile PCB's divider resistance R_d with the PCB test setup. The vertical axis refers to measurements derived from the I–V curve. The horizontal axis refers to the measurement performed with the pogo pin at 40 V bias voltage. The quality requirements are shown as dashed lines. The elliptical contours are derived from the data that passed the quality requirements, assuming Gaussian confidence intervals (CI). The origin of the set of points in the left part of the plot is currently under investigation

this region are used to define the *Single-to-Zero ratio* (SZR):

$$\mathrm{SZR} = \frac{\mu_1 - \mu_0}{\sigma_0}\,, \tag{11}$$

where μ_1 (μ_0) is the mean of the SPE (0-PE) peak and σ_0 is the 0-PE standard deviation. The SZR parameter quantifies the single photon detectability over baseline fluctuations, an extremely important feature for the performance of the DS-20k experiment.[2] Figure 19 (bottom) illustrates the SZR distribution in the form of a boxplot (from the amplitude finger plot) as a function of the bias voltage and overvoltage. Dots represent outliers more than 1.5 IQR away from the top or bottom of each box. As expected, the SZR increases with the overvoltage.

A final quality check assesses the conformity of the pulse shape of the SPE average waveform. The latter is computed by averaging all waveforms whose charge is in the interval $\pm 2\,\sigma$ centred on the SPE charge mean. The SPE average waveform is modelled with the function

$$V(t;\, A,\, \tau_{\mathrm{rise}},\, \tau_{\mathrm{fall}}) = A\left(e^{-t/\tau_{\mathrm{fall}}} - e^{-t/\tau_{\mathrm{rise}}}\right)\,. \tag{12}$$

The values A, τ_{rise}, and τ_{fall} are obtained through a χ^2 fit, where the uncertainties are set to the standard deviation of the average waveform in the baseline region. The parameters are initialised at their nominal values (τ_{rise} at 80 ns, τ_{fall} at

[2] The SZR is akin to a Signal-to-Noise ratio (SNR) that is tuned for reliability and automation during the quality assessment in NOA. However, since slightly different versions of SNRs have been used in DS-20k publications [1,39], we have chosen to give a specific name to the one used in this context.

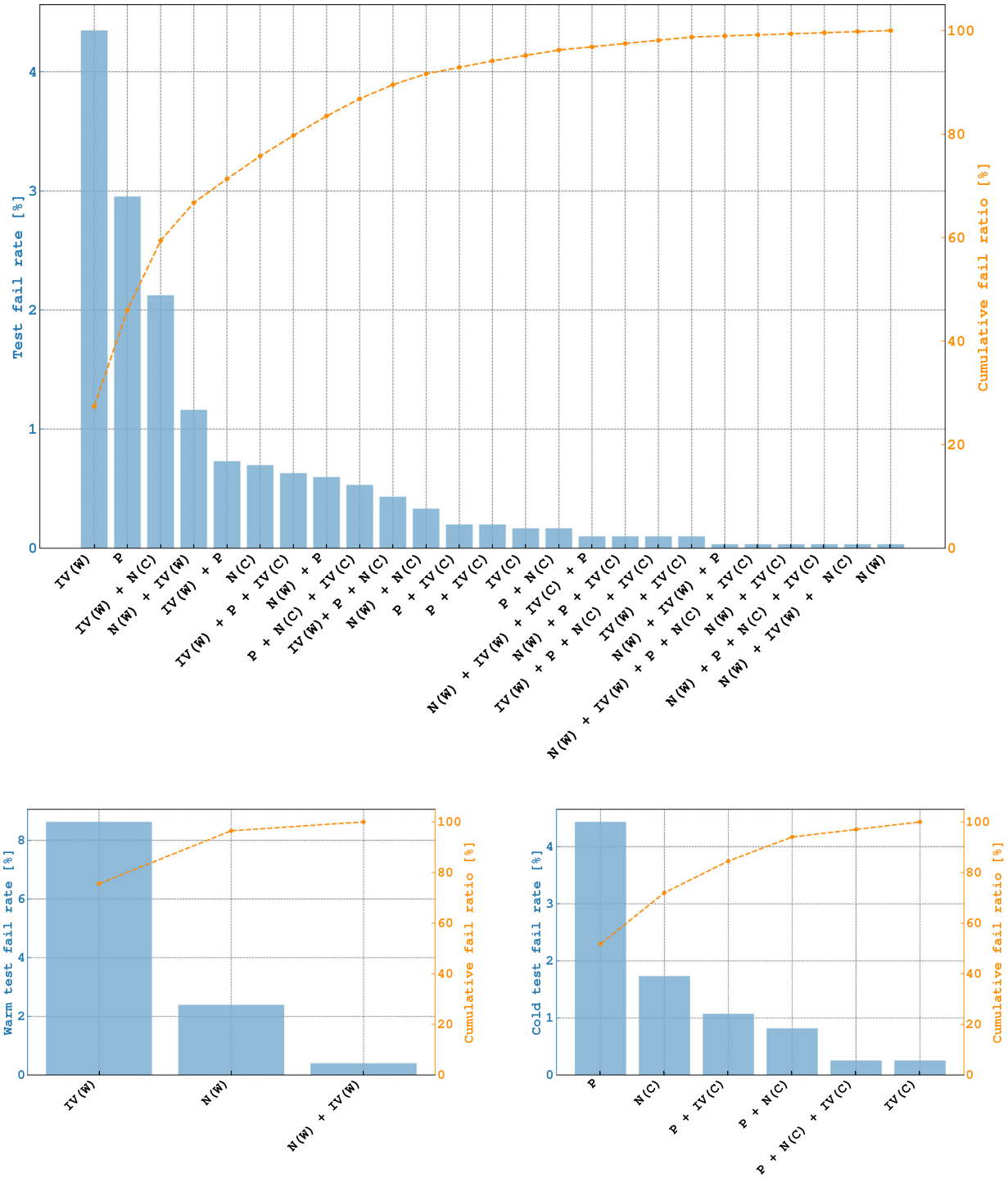

Fig. 21 Pareto charts illustrating the failure modes in the Tile quality assessment process. The top figure presents the overall failure distribution. The bottom row differentiates between tests conducted at room temperature (left) and in liquid nitrogen (right). On the horizontal axes, **IV** indicates failures associated with the I-V curve, **N** denotes noise-related failures, and **P** pertains to issues within the pulse quality assessment. The suffixes **W** and **C** inside parentheses distinguish between tests conducted at room temperature (warm) and those conducted in liquid nitrogen (cold). The most common failure is associated with the I-V curve at room temperature, accounting for 4.3% of the overall tests, followed by pulse quality assessment in liquid nitrogen at 2.9%, and the simultaneous failure of the I-V test at room temperature and the noise test in liquid nitrogen at 2.1%. Together, these three failure modes constitute approximately 60% of the cumulative fail ratio. In the warm test, the most common failure involves the I-V curve, accounting for 74% of the total failures at room temperature. In the cold test, the most frequent failure is the pulse quality, which represents 53% of failures in defective Tiles in liquid nitrogen

350 ns). The fit is performed in an interval of 2 µs, with the start time (corresponding to $t = 0$ in the model in Equation 12) assigned through a constant fraction discriminator set at 5% of the average SPE waveform peak. Figure 16 shows an example of an average SPE waveform along with the fitting function $V(t)$.

Table 5 lists the quality parameters for the pulse assessment. The quality control allows us to discard Tiles with SPE means at unexpected values, poor resolution, or low SZR. Very problematic Tiles with unusual finger plots, strictly not usable in DS-20k, typically fail all of the pulse checks. The requirements have been fine-tuned to exclude the outliers in the distributions and have shown to provide PDUs with good performance.[3] We perform the quality control for the measurements taken at two of the four bias voltages used, corresponding to 7 V and 9 V over voltage, as the other two have been shown to be redundant.

Starting in the fifth month of production (April 2025), the quality control pipeline was updated with an estimation of the Pulse Count Rate (PCR) using the waveforms acquired during the pulse counting assessment. The PCR is defined as the number of triggers with at least a PE pulse in the pre-trigger region over the total acquisition time. Tails of large pulses from the preceding time window are excluded from the computation. The acquisition time is defined as the number of triggers multiplied by the width of the pre-trigger region. Tiles with a PCR greater than about 1 Hz/mm^2 are transferred to an additional setup with dark Tile holders, dedicated to the measurement of the Dark Count Rate (DCR), for further investigation before PDU mounting. The DCR testing setup will be described in a future paper, as well as the impact of the DCR for DS-20k.

5 Results

The QA-QC procedures implemented at NOA have enabled a systematic evaluation of the Tile performance, ensuring compliance with the requirements for integration into the PDUs of the DS-20k TPC.

A pre-production phase was successfully conducted from January to October 2024 to asses process capability, throughput, and failure rates. During this phase, Tiles were assembled using a first batch of wafers meant to confirm the quality of the SiPM, allowing for the refinement of quality assurance procedures until they reached the standards described in this paper.

Based on the production yield achieved to date, we expect that the complete production of the Tiles for the TPC of DS-20k will be finalised in less than 30 months, with a throughput of 32 Tiles per day. This production process encompasses the cryogenic characterisation of the total 1400 silicon wafers (equivalent to 369.600 individual dice), testing of 10250 PCBs, the packaging and qualification of 10138 Tiles (including spares), and the assembly of 528 functional TPC PDUs.

[3] A paper containing details of the PDU performance in liquid nitrogen is in preparation.

Table 6 Results of the warm and cold Tile test with percentages associated with the nature of the failed test. More details on the failure modes are given in the text. A Tile must pass both the test at room temperature and in liquid nitrogen to be assembled in a PDU

Warm test	Cold test	Tiles percentage
Passed	Passed	83.5%
Passed	Failed	4.8%
Failed	Passed	5.2%
Failed	Failed	6.5%

The rest of this section highlights some of the results of the PCB and Tile production and quality control, focusing on uniformity, and production yield achieved during mass testing.

5.1 PCB assessment performance and yield

The PCB assessment demonstrated percent-level uniformity in the discrete components of the tested sample, confirming the stability of the component population process at EltHUB.

1730 Tile PCBs were tested in (2024–2025) including 131 from the pre-production batch and 1599 from the production phase. About % failed the test, primarily due to poor soldering of a resistor or surface contamination.

PCBs that failed the test due to improper mounting of electronic components were reworked and retested, with only 4 units failing the second test, resulting in a final yield of 99.8% after rework.

Figure 20 compares the two independent estimates of the Tile PCB divider resistance: the measurement using the pogo pin at 40 V bias voltage (horizontal axis) and the value retrieved from the slope of the I-V curve (vertical axis). The quality requirements are also shown. Elliptical contours are derived from the data that passed the quality requirements, assuming Gaussian confidence intervals (CI). The strong correlation between these methods highlights the reliability of the quality assurance. The PCB quality assurance significantly improves the Tile test yield, as it restricts the Tile test failures mainly to SiPM-related issues.

5.2 Tile performance and yield

The Tile test demonstrated good uniformity across the 1507 tested devices, including 261 pre-production and 1246 production Tiles. Overall, the distributions confirm the high uniformity of the Tiles, with 83.5% meeting all of the quality

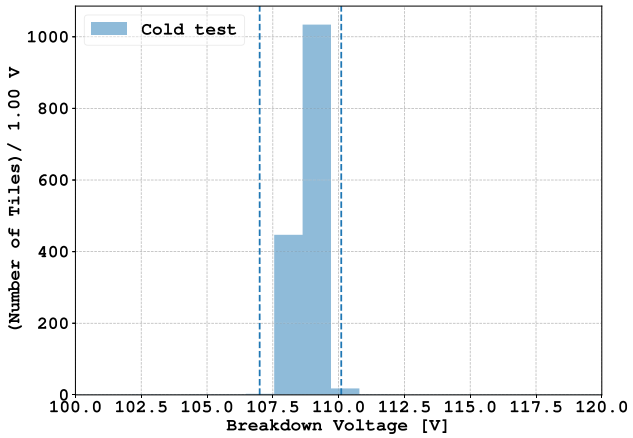

Fig. 22 Distribution of the measured breakdown voltage, V_{bd}, in liquid nitrogen. The QC requirements are shown as dashed lines

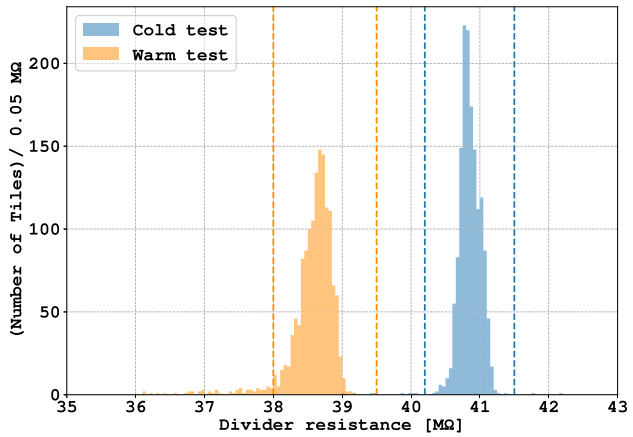

Fig. 23 Distribution of the measured Tile equivalent divider resistance, R_d, at room temperature (orange) and in liquid nitrogen (blue). The quality requirements are shown as dashed lines

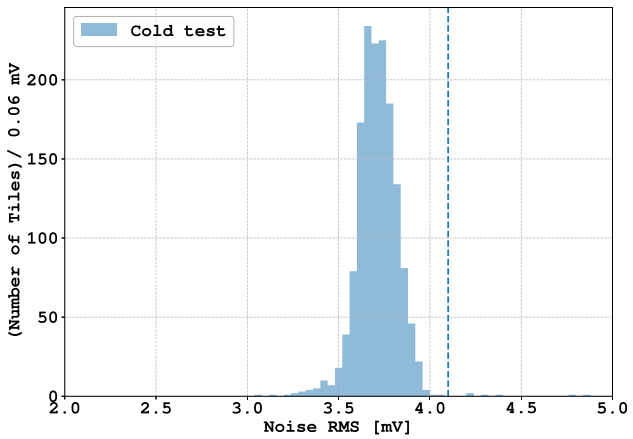

Fig. 24 Distribution of the Noise RMS, as measured by the oscilloscope in liquid nitrogen with a 40 V bias voltage (Blue). The quality requirement is shown as a dashed line

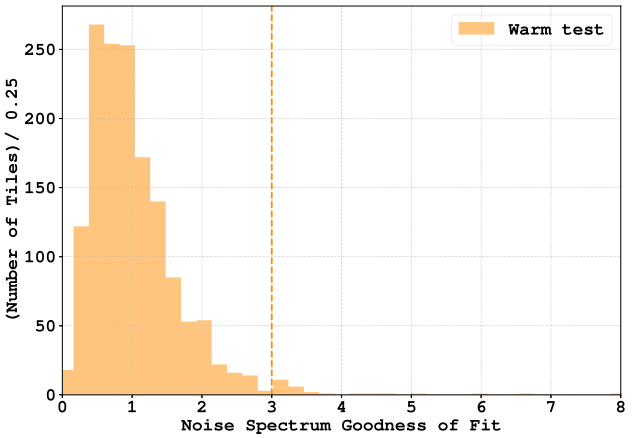

Fig. 25 Distribution of the measured Goodness of Fit parameter (GoF) at room temperature. The quality requirement is shown as a dashed line

requirements. Table 6 summarises the Tile percentage that failed both the warm and cold tests, only one of them or none of them.

The overall performance of the Tile test, categorised by failure type, is illustrated in the Pareto charts in Fig. 21. The most common failure is associated with the I-V curve at room temperature, accounting for 4.3%, followed by pulse quality assessment in liquid nitrogen at 2.9%, and the simultaneous failure of the I-V test at room temperature and the noise test in liquid nitrogen at 2.1%. Together, these three failure modes constitute 60% of the total failure rate. An I-V failure at room temperature is a symptom of misbehaviour of the Tile. Tiles may still pass the quality tests in liquid nitrogen but fail at room temperature. When retested in liquid nitrogen after some time, these Tiles often exhibit a worsened performance.[4]

The majority of the room temperature test failures (refer to Fig. 21 left) is due to I-V curves falling outside specifications, accounting for 74% of failed Tiles at room temperature, (approximately 8.7% of the total sample).

The most common failure mode in the test in liquid nitrogen (refer to Fig. 21 right) is related to the pulse quality control, representing 53% of failed Tiles in liquid nitrogen (around 5.9% of the full sample). The pulse counting test remains the most frequent failure mode even for Tiles that pass the test at room temperature.

Regarding the I-V curve assessment, Figs. 22 and 23 show the distribution of the breakdown voltage, V_{bd}, and the equivalent divider resistance, R_d, respectively, over all the Tiles tested in NOA at room temperature and in liquid nitrogen. Quality specifications are displayed as dashed lines.

[4] A long-term test in liquid nitrogen of PDUs built out of Tiles is carried out in the DS-20k Naples Photosensor Test Facility (PTF). The performance of the PDUs is the main topic of a paper in preparation.

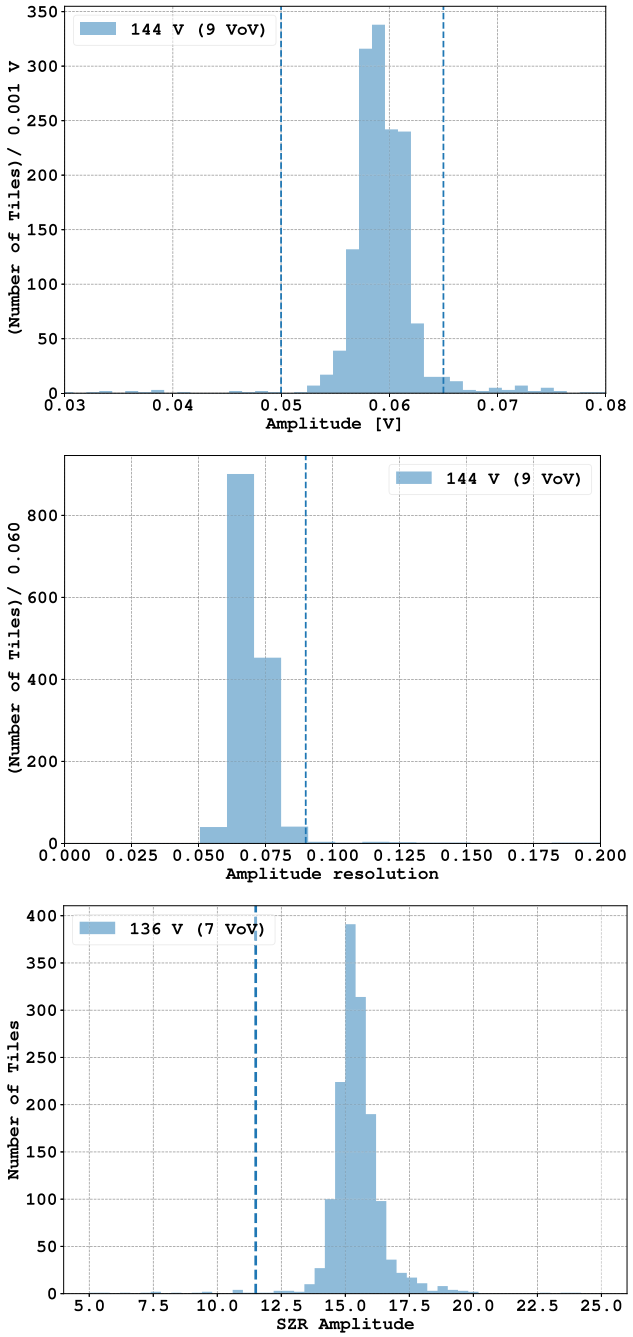

Fig. 26 Distributions of the mean of the Single PhotoElectron (SPE) amplitude (first from the top) and its resolution (second from the top) at 144 V (9 VoV) along with the Single to Zero Ratio (SZR, third from the top). The quality requirements are shown as dashed lines

The breakdown voltage distribution in liquid nitrogen peaks at 108 V, consistent with the expected value for a configuration of four SiPMs in series, each having a V_{bd} of 27 V [10]. Maintaining a narrow distribution of the breakdown voltage is essential when grouping Tiles in PDUs, since the Tiles within a PDU are operated at a common bias voltage. Significant variations in the breakdown voltage of the Tiles would cause gain mismatches, degrading the SPE resolution. Therefore, PDUs are constructed using Tiles that have a breakdown voltage consistency within a margin of 1 V.

The divider resistance distributions at room temperature and in liquid nitrogen exhibit the expected trend, with R_d increasing as temperature decreases. There is a small tail of Tiles with R_d out of specification despite the corresponding PCB meeting the specification of the quality control. The tail is mostly due to the double slope phenomenon introduced in Sect. 4.2.3, where the I-V curves show an additional, though less pronounced, departure from linearity below V_{bd}.

The primary reasons for failures in noise assessment are broken TIAs or the detachment of one or more SiPM branches. In either situation, the noise quality parameters fall outside the acceptance range, especially the Goodness of Fit (GoF), which is highly sensitive to these types of defects. Some examples of quality parameters distributions are shown in Figs. 24 and 25 showing respectively the RMS noise in liquid nitrogen (at 40 V bias voltage), measured with the oscilloscope, and the GoF parameter at room temperature. The mean GoF is consistent with one, meaning that the measured spectra are in excellent agreement with the reference spectrum. The tail of the distribution extends up to 40, with 3% of the Tiles exceeding the requirements.

The results of the pulse counting test in liquid nitrogen are exemplified in Fig. 26 by the distributions of the SPE mean, resolution, and SZR in amplitude with bias voltage 144 V (9 VoV). All of the distributions are sharply peaked, with only a small fraction of entries deviating significantly from the bulk of the distribution, 10% for the SPE amplitude mean, 6% for its resolution, and 2% for the SZR. The Tiles exhibiting SPE values that fall outside the expected range often have this issue because of secondary peaks located between the 0-PE and the SPE peak. This occurrence is typical in Tiles displaying an I-V characteristic with a double slope. Abnormal SPE resolution values arise from a broadening of the SPE peak. In finger plots with significant peak overlap, the SPE resolution surpasses the upper range of the histogram shown in Fig. 26 (second from the top).

As in [10], process capability indices are used to measure the ability of the Tile manufacturing process to produce Tiles within the specification limits. Three process Capability (Cp) indices are monitored on a monthly basis: CpL, CpU and CpK. CpU/CpL is a measurement of the Tile manufacturing process based on its Lower (Upper) Specification Limit LSL (USL). They are defined in Eqs. 13 and 14. They represent the ratio of the difference between the mean of the measured quantity X and the lower (upper) specification limit, LSL (USL), to the process's standard deviation, specifically the $3\sigma_X$ variation.

$$\mathrm{CpL} = \frac{\overline{X} - \mathrm{LSL}}{3\sigma_X} \tag{13}$$

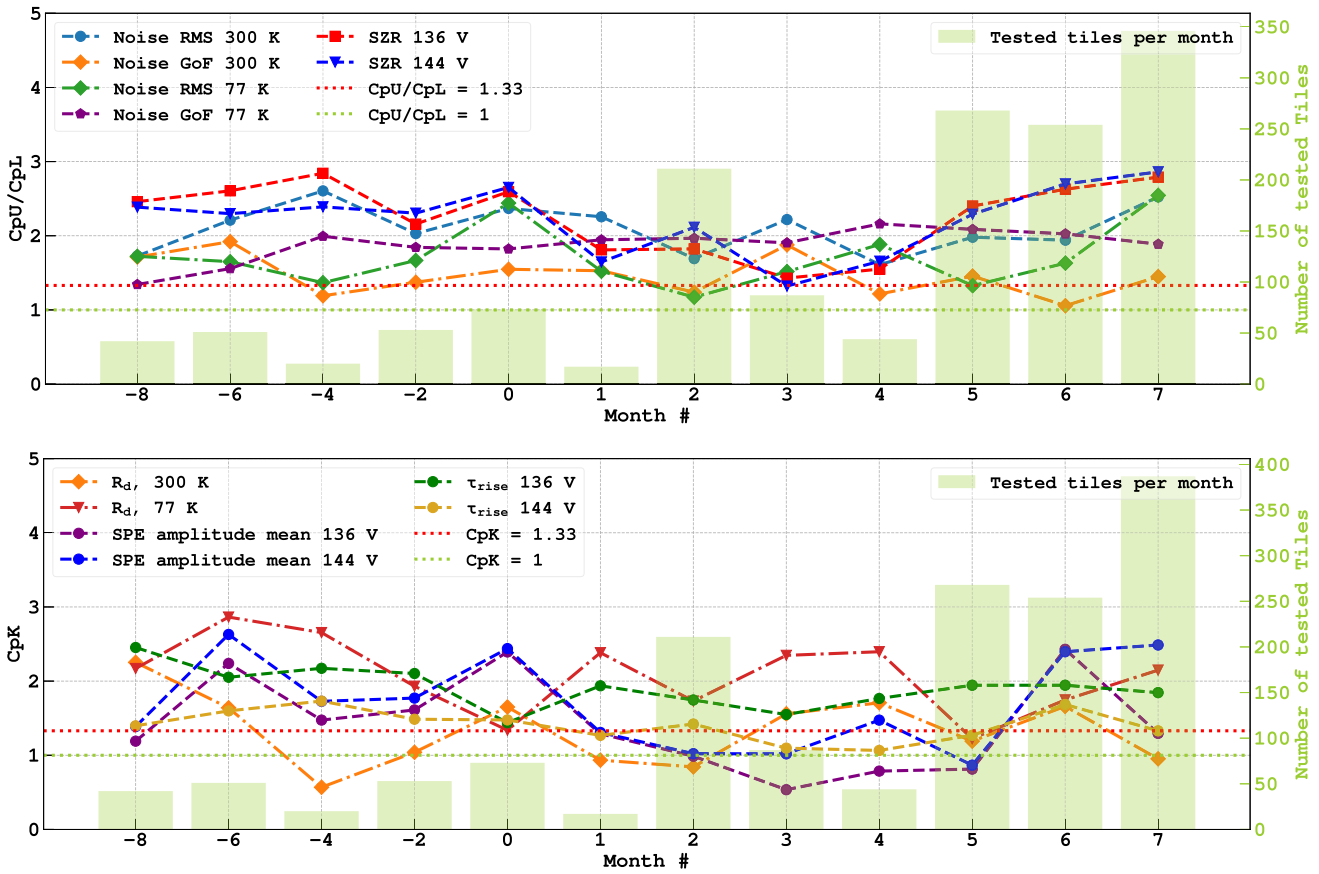

Fig. 27 The top figure shows the monthly CpU/CpL of the Tiles with respect to noise RMS, Goodness of Fit, and SZR at room temperature and 77 K, while the bottom figure displays the monthly CpK of the Tiles breakdown voltage V_{bd}, divider resistance R_d at room temperature and 77 K the Single PhotoElectron (SPE) mean in amplitude and τ_{rise} at 136 V and 144 V. Pre-production data is labelled with negative numbers from the beginning of the production and grouped in pairs. The red horizontal dashed line at 1.33 is the conventional industry standard, indicating a $4\sigma_X$ difference between the mean of the measured quantity and its upper specification limit, while the green horizontal dashed line at 1 indicates the conventional acceptance limit. The number of Tiles tested per month is displayed as well. Fluctuations of this quantity result from interruptions due to process adjustments, which decrease the monthly Tiles throughput

$$\mathrm{CpU} = \frac{\mathrm{USL} - \overline{X}}{3\sigma_X} \tag{14}$$

The CpK metric is essential for assessing process compliance when both upper and lower specification limits are required. It is defined as the ratio of the difference between the average of the measured quantity X and the nearest specification limit (either USL or LSL) to the standard deviation of the process ($3\sigma_X$ variation), as shown in Eq. 15.

$$\mathrm{CpK} = \min[\mathrm{CpU}, \mathrm{CpL}] \tag{15}$$

In both cases, the mean and standard deviation are computed by removing the outliers, defined as Tiles with more than 1.5 InterQuartile Range (IQR) above the upper (lower) quartile.

As an example, Fig. 27 (top) shows the monthly CpU/CpL of the Tiles' noise parameters (RMS, GoF, and SZR) at room temperature and in liquid nitrogen and the monthly CpK of the Tiles' R_d, SPE mean in amplitude, and τ_{rise} at 136 V and 144 V bias voltage (Bottom). Pre-production data is labelled with negative numbers from the beginning of the production and grouped in pairs. The red horizontal dashed line at 1.33 is the conventional industry standard [40], indicating a $4\sigma_X$ difference between the mean of the measured quantity and its upper specification limit, while the green horizontal dashed line at 1 indicates the conventional acceptance limit. The number of Tiles tested per month is displayed as well. Fluctuations of this quantity result from interruptions due to process adjustments, which decrease the monthly Tiles throughput.

Decreasing trends in process capability indices can be attributed to either insufficient data, which may occur due to process interruptions, or production-related issues. The decline seen in Fig. 27 around month-4 was caused by alterations in the die attaching process, resulting in some SiPMs with scratches that produced irregular I–V curves in Tiles. The slight decline observed around month 3 was due to the

use of wafers exhibiting a marginally higher SiPM breakdown voltage. Besides these identified issues, the process capability reflects a consistently stable production campaign.

6 Conclusions

The DS-20k experiment aims to achieve unprecedented sensitivity in WIMP dark matter direct detection using a double phase UAr-TPC instrumented with a novel SiPM-based photodetection system. The underlying photodetector module, the Tile, has been developed and demonstrated readiness for mass production at the Nuova Officina Assergi (NOA) facility at LNGS. This paper reported the quality assurance and quality control procedures implemented to ensure the performance, reliability, and uniformity of the Tiles throughout the production process.

A comprehensive QA-QC protocol was developed to asses the electrical and optical properties of each Tile at both room temperature and in liquid nitrogen. The characterisation included I-V curve measurements, noise spectrum analysis, and photon response testing. The results demonstrate a high level of uniformity across the 1507 tested Tiles. Key performance parameters, such as breakdown voltage, divider resistance, and single-photon response, have shown consistent and reproducible behaviour over the production time.

A well-optimised testing workflow enabled an efficient validation process, significantly improving production yield. The PCB and Tile test assessments at room temperature successfully identify major electronic faults early in the process. The quality check in liquid nitrogen ensures that the Tiles work as expected. The overall production yield exceeded 83.5%, with failures primarily attributed to I-V curve deviations and inconsistencies in Single PhotoElectron measurements. These results validate the robustness of the Tile design and its suitability for operation in a cryogenic environment.

The full production of 10138 Tiles, corresponding to an overall instrumented area of 21 m^2, is expected to end in less than 30 months with the completion of the cryogenic characterisation of the overall amount of 1400 silicon wafers (equivalent to 369.600 single dice), the test of 10250 bare PCBs, the packaging and qualification of 10138 Tiles and the building of 528 functional TPC PDUs.

Continuous refinements in the assembly and testing processes will further enhance production efficiency and ensure that only high-quality photodetectors are integrated into the experiment. The success of this effort establishes a strong foundation for deploying large-area SiPM-based photodetection systems in future low-background physics experiments.

Acknowledgements This paper is based upon work supported by the U.S. National Science Foundation (NSF) (Grants no. PHY-0919363, no. PHY-1004054, no. PHY-1004072, no. PHY-1242585, no. PHY-1314483, no. PHY-1314507, no. PHY-1622337, no. PHY-1812482, no. PHY-1812547, no. PHY-2310091, no. PHY-2310046, associated collaborative Grants, no. PHY-1211308, no. PHY-1314501, no. PHY1455351 and no. PHY-1606912, as well as Major Research Instrumentation Grant no. MRI-1429544), the Italian Istituto Nazionale di Fisica Nucleare (Grants from Italian Ministero dell'Istruzione, Università, e Ricerca Progetto Premiale 2013 and Commissione Scientific Nazionale II), the Natural Sciences and Engineering Research Council of Canada, SNOLAB, and the Arthur B. McDonald Canadian Astroparticle Physics Research Institute. This work received support from the French government under the France 2030 investment plan, as part of the Excellence Initiative of Aix-Marseille University – A*MIDEX (AMX-19-IET-008 – IPhU). We also acknowledge the financial support by LabEx UnivEarthS (ANR-10-LABX-0023 and ANR18-IDEX-0001), Chinese Academy of Sciences (113111KYSB20210030) and National Natural Science Foundation of China (12020101004). This work has been supported by the São Paulo Research Foundation (FAPESP) Grant 2021/11489-7 and by the National Council for Scientific and Technological Development (CNPq). Support is acknowledged by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under Germany's Excellence Strategy – EXC 2121: Quantum Universe – 390833306. The authors were also supported by the Spanish Ministry of Science and Innovation (MICINN) through the Grant PID2022-138357NB-C22, the "Atraccion de Talento" Grant 2018-T2/TIC-10494, the Polish NCN (Grants no. UMO-2022/47/B/ST2/02015 and UMO-2023/51/B/ST2/02099), the Polish Ministry of Science and Higher Education (MNiSW, Grant number 6811/IA/SP/2018), the International Research Agenda Programme AstroCeNT (Grant no. MAB/2018/7) funded by the Foundation for Polish Science from the European Regional Development Fund, the European Union's Horizon 2020 research and innovation program under Grant agreement no. 952480 (DarkWave), the Science and Technology Facilities Council, part of the United Kingdom Research and Innovation, and The Royal Society (United Kingdom), and IN2P3-COPIN consortium (Grant no. 20-152). We also wish to acknowledge the support from Pacific Northwest National Laboratory, which is operated by Battelle for the U. S. Department of Energy under Contract no. DE-AC05-76RL01830. This research was supported by the Fermi National Accelerator Laboratory (Fermilab), a U. S. Department of Energy, Office of Science, HEP User Facility. At the time of this work, Fermilab was managed by Fermi Research Alliance, LLC (FRA), acting under contract no. DE-AC02-07CH11359. This work was supported (in part) by the PRIN2020 project of the Italian Ministry of Research (MUR) (Grant no. PRIN 20208XN9TZ).

Data Availability Statement This manuscript has no associated data. [Author's' comment: Data sharing not applicable to this article as no datasets were generated or analysed during the current study.]

Code Availability Statement This manuscript has no associated code/software. [Author's comment: Code/Software sharing not applicable to this article as no code/software was generated or analysed during the current study.]

Funded by SCOAP[3].

References

1. C.E. Aalseth et al., DarkSide-20k: a 20 tonne two-phase LAr TPC for direct dark matter detection at LNGS. Eur. Phys. J. Plus **133**(3), 131 (2018). https://doi.org/10.1140/epjp/i2018-11973-4. (**ISSN:2190-5444**)
2. P. Agnes et al., DarkSide-50 532-day dark matter search with low-radioactivity argon. Phys. Rev. D **98**(10), 102 006 (2018). https://doi.org/10.1103/PhysRevD.98.102006
3. P. Agnes et al., Separating ^{39}Ar from ^{40}Ar by cryogenic distillation with aria for dark-matter searches. Eur. Phys. J. C **81**(4), (2021). https://doi.org/10.1140/epjc/s10052-021-09121-9. **(ISSN: 1434-6052)**
4. F. Acerbi et al., Benchmarking the design of the cryogenics system for the underground argon in DarkSide-20k. JINST **20**(02), P02016 (2025). https://doi.org/10.1088/1748-0221/20/02/P02016
5. D. Montanari et al., Development of membrane cryostats for large liquid argon neutrino detectors. IOP Conf. Ser. Mater. Sci. Eng. **101**(1), 012049 (2015). https://doi.org/10.1088/1757-899X/101/1/012049 **(P. Kittel and M. Sumption, Eds.)**
6. F. Acerbi et al., Cryogenic characterization of FBK HD near-UV sensitive SiPMs. IEEE Trans. Electron. Devices **64**(2), 521–526 (2017). https://doi.org/10.1109/ted.2016.2641586. (**ISSN:1557-9646**)
7. C. Piemonte et al., Performance of NUV-HD silicon photomultiplier technology. IEEE Trans. Electron. Devices **63**, 1–6 (2016). https://doi.org/10.1109/TED.2016.2516641
8. A. Gola et al., NUV-sensitive silicon photomultiplier technologies developed at Fondazione Bruno Kessler. Sensors **19**(2), 308 (2019). https://doi.org/10.3390/s19020308. (**ISSN: 1424-8220**)
9. L. Consiglio et al., Nuova Officina Assergi: a novel infrastructure for the production of cryogenic and radiopure Si-based photodetectors. Front. Phys. **12**, 1433347 (2024). https://doi.org/10.3389/fphy.2024.1433347. (**ISSN:2296-424X**)
10. F. Acerbi, DarkSide-20k Collaboration, Quality assurance and quality control of the 26 m^2 sipm production for the darkside-20k dark matter experiment. Eur. Phys. J. C **85**(5), 534 (2025). https://doi.org/10.1140/epjc/s10052-025-14196-9
11. G. Gallina et al., Characterization of SiPM avalanche triggering probabilities. IEEE Trans. Electron. Devices **66**(10), 4228–4234 (2019). https://doi.org/10.1109/TED.2019.2935690
12. M. D'Incecco et al., Development of a novel single-channel, 24 cm^2, SiPM-based, cryogenic photodetector. IEEE Trans. Nucl. Sci. **65**(1), 591–596 (2018). https://doi.org/10.1109/TNS.2017.2774779. (**ISSN:0018-9499**)
13. A. Razeto et al., Very large SiPM arrays with aggregated output. JINST **17**(05), P05038 (2022). https://doi.org/10.1088/1748-0221/17/05/P05038
14. R. Kugathasan, A low-power mixed-signal ASIC for readout of SiPM at cryogenic temperature. PoS **TWEPP2019**, 011 (2020). https://doi.org/10.22323/1.370.0011
15. TIA, LMH6629. https://www.ti.com/product/LMH6629. Accessed 3 Nov 2025
16. F. Acerbi et al., DarkSide-20k sensitivity to light dark matter particles. Commun. Phys. **7**(1), 422 (2024). https://doi.org/10.1038/s42005-024-01896-z. (**ISSN:2399-3650**)
17. V. Pesudo et al., Material assay campaign of the DarkSide-20k Experiment. AIP Conf. Proc. **2908**(1), 080 001 (2023). https://doi.org/10.1063/5.0161981. (**ISSN:0094-243X**)
18. Arlon Electronic Materials. https://www.arlonemd.com. Accessed 3 Nov 2025
19. P. Franchini et al., *DarkSide-20k Veto Photon-Detector Units: Construction and Characterization, 05,* vol. 19 (IOP Publishing, 2024), p. C05013. https://doi.org/10.1088/1748-0221/19/05/C05013
20. D. Santone, The DarkSide-20k Veto Readout System: PDUs Construction and Characterization (2024), p. 027. https://doi.org/10.22323/1.441.0027
21. P. Organtini, A. Gola, G. Paternoster, F. Acerbi, G. Margutti, R. Bez, Industrial Exploitation of SiPM Technology Developed for Basic Research. Nucl. Instrum. Methods Phys. Res. A **978**, 164 410 (2020). https://doi.org/10.1016/j.nima.2020.164410. (**ISSN:0168-9002**)
22. FormFactor, Pac-200 wafer-multi-chip-cryogenic-systems. https://www.formfactor.com/product/probe-systems/wafer-multi-chip-cryogenic-systems/pac200/. Accessed 3 Nov 2025
23. Blue Tape. https://www.sps-international.com/product/1027r-uv-adhesive-film-polyolefin/7447/. Accessed 3 Nov 2025
24. Artel PCB engineering. https://artel-srl.com. Accessed 3 Nov 2025
25. FiberLUX EL. https://www.elettrolaser.com. Accessed 3 Nov 2025
26. ELTGroup. https://www.eltgroup.net. Accessed 3 Nov 2025
27. AMICRA NOVA PLUS. https://amicra.semi.asmpt.com. Accessed 3 Nov 2025
28. HESSE Bondjet BJ855. https://www.hesse-mechatronics.com/en/bondjet-bj855-bj885/. Accessed 3 Nov 2025
29. Z. Balmforth et al., A large facility for photosensors test at cryogenic temperature. JINST **18**(03), C03024 (2023). https://doi.org/10.1088/1748-0221/18/03/C03024
30. PostgreSQL. https://www.postgresql.org. Accessed 3 Nov 2025
31. P. Franchini, DarkSide-20k production database for the SiPM detectors construction and characterisation. PoS **ICHEP2024**, 770 (2025). https://doi.org/10.22323/1.476.0770
32. A. Taylor, P. Franchini, S. Koulosousas, A cross-platform python interface to the darkside-20k production database (2024). https://doi.org/10.5281/zenodo.10817039
33. P. Agnes et al., Results from the first use of low radioactivity argon in a dark matter search. Phys. Rev. D **93**(8), 081101 (2016). https://doi.org/10.1103/physrevd.93.081101. (**ISSN:2470-0029**)
34. Arduino. https://www.arduino.cc. Accessed 3 Nov 2025
35. Adafruit Feather M0, SAMD21. https://learn.adafruit.com. Accessed 3 Nov 2025
36. TINA-TI. https://www.ti.com. Accessed 3 Nov 2025
37. Electrical characterization of silicon photo-multiplier detectors for optimal front-end design, in *2006 IEEE Nuclear Science Symposium Conference Record*, vol. 2, pp. 1276–1280 (2006). https://doi.org/10.1109/NSSMIC.2006.356076 **(ISSN:1095-7863)**
38. Modelling a silicon photomultiplier (SiPM) as a signal source for optimum front-end design. Nucl. Instrum. Methods Phys. Res. A **572**(1), 416–418 (2007). https://doi.org/10.1016/j.nima.2006.10.219, **(ISSN:0168-9002)**
39. The Global Argon Dark Matter Collaboration, DarkSide-20k Technical Design Report. INFN, Technical Report DARKSIDE-CSN2-TDR-2112 v3.0, Submitted to INFN (2021)
40. N. Heckert et al., *Handbook 151: NIST/SEMATECH e-Handbook of Statistical Methods*. NIST Interagency/Internal Report (NISTIR), National Institute of Standards and Technology, Gaithersburg, MD. https://www.nist.gov/publications/handbook-151-nistsematech-e-handbook-statistical-methods (2002)

DarkSide-20k Collaboration[★]

F. Acerbi[1], P. Adhikari[2], P. Agnes[3,4], I. Ahmad[5], S. Albergo[6,7], I. F. Albuquerque[8], T. Alexander[9], A. K. Alton[10], P. Amaudruz[11], M. Angiolilli[3,4], E. Aprile[12], M. Atzori Corona[13,14], D. J. Auty[15], M. Ave[3], I. C. Avetisov[16], O. Azzolini[17], H. O. Back[9], Z. Balmforth[75], A. Barrado Olmedo[20], P. Barrillon[21], G. Batignani[22,23], P. Bhowmick[24], M. Bloem[88], S. Blua[25,26], V. Bocci[27], W. Bonivento[13], B. Bottino[28,29], M. G. Boulay[2], T. Braun[24], A. Buchowicz[32], S. Bussino[33,89], J. Busto[21], M. Cadeddu[13], M. Cadoni[13,14], R. Calabrese[34,50], V. Camillo[35], A. Caminata[29], N. Canci[34], M. Caravati[3,4], M. Cárdenas-Montes[20], N. Cargioli[13,14], M. Carlini[4], A. Castellani[30,31], P. Cavalcante[4], S. Cebrian[37], S. Chashin[38], A. Chepurnov[38], S. Choudhary[5], L. Cifarelli[39,40], B. Cleveland[41,42], Y. Coadou[21], V. Cocco[13], D. Colaiuda[4,43], E. Conde Vilda[20], L. Consiglio[4], A. F. V. Cortez[5], B. S. Costa[8], M. Czubak[44], M. D'Aniello[34,45], S. D'Auria[31,46], M. D. Da Rocha Rolo[25], A. Dainty[86], G. Darbo[29], S. Davini[29], R. de Asmundis[34], S. De Cecco[27,47], G. Dellacasa[25], A. V. Derbin[49], A. Devoto[13,14], L. Di Noto[28,29], P. Di Stefano[51], L. K. Dias[8], D. Díaz Mairena[20], C. Dionisi[27,47], G. Dolganov[53,73], F. Dordei[13], V. Dronik[54], F. Dylon[55], A. Elersich[55], E. Ellingwood[51], T. Erjavec[55], N. Fearon[24], M. Fernandez Diaz[20], L. Ferro[13,14], A. Ficorella[1], G. Fiorillo[34,50], D. Fleming[55], P. Franchini[24], D. Franco[57], H. Frandini Gatti[58], E. Frolov[59], F. Gabriele[13], D. Gahan[13,14], C. Galbiati[52], G. Galiński[32], G. Gallina[52], M. Garbini[39,60], P. Garcia Abia[20], A. Gawdzik[61], A. Gendotti[62], G. K. Giovanetti[63], V. Goicoechea Casanueva[64], A. Gola[1], L. Grandi[65], G. Grauso[34], G. Grilli di Cortona[4], A. Grobov[53], M. Gromov[38], M. Gulino[66,87], B. R. Hackett[9], A. L. Hallin[15], A. Hamer[68], M. Haranczyk[44], B. Harrop[52], T. Hessel[57], C. Hidalgo[3], J. Hollingham[86], S. Horikawa[4,43], J. Hu[15], F. Hubaut[21], D. Huff[69], T. Hugues[51], E. V. Hungerford[69], A. Ianni[52], A. Ianni[4], V. Ippolito[27], A. Jamil[52], C. Jillings[41,42], R. Keloth[35], N. Kemmerich[8], A. Kemp[88], M. Kimura[5], A. Klenin[54], K. Kondo[4,43], G. Korga[19], L. Kotsiopoulou[68], S. Koulosousas[19], A. Kubankin[54], P. Kunzé[3,4], M. Kuss[22], M. Kuźniak[5], M. Kuzwa[5], M. La Commara[34,70], M. Lai[71], E. Le Guirriec[21], E. Leason[24], A. Leoni[4,43], L. Lidey[9], J. Lipp[86], M. Lissia[13], L. Luzzi[55], O. Lychagina[72], O. Macfadyen[19], I. Machts[57], I. N. Machulin[53,73], S. Manecki[41,42], I. Manthos[75], L. Mapelli[52], A. Marasciulli[4], S. M. Mari[33,89], C. Mariani[35], J. Maricic[64], M. Martinez[37], C. J. Martoff[9,76], G. Matteucci[34,50], K. Mavrokoridis[58], A. B. McDonald[51], S. Merzi[1], A. Messina[27,47], R. Milincic[64], S. Minutoli[29], A. Mitra[77], J. Monroe[24], E. Moretti[1], M. Morrocchi[22,23], A. Morsy[79], T. Mroz[44], V. N. Muratova[49], M. Murra[12], P. Musico[29], R. Nania[39], M. Nessi[78], G. Nieradka[5], K. Nikolopoulos[75], E. Nikoloudaki[57], I. Nikulin[54], J. Nowak[56], K. Olchanski[11], A. Oleinik[54], V. Oleynikov[59], P. Organtini[4,52], A. Ortiz de Solórzano[37], A. Padmanabhan[51], M. Pallavicini[28,29], L. Pandola[66], E. Pantic[55], E. Paoloni[22,23], D. Papi[15], B. Park[15], G. Pastuszak[32], G. Paternoster[1], R. Pavarani[13,14], A. Peck[71], K. Pelczar[44], R. Perez[8], V. Pesudo[20], S. Piacentini[3,4], N. Pino[66], G. Plante[12], A. Pocar[79], S. Pordes[35], P. Pralavorio[21], E. Preosti[52], D. Price[61], M. Pronesti[21], S. Puglia[6,7], M. Queiroga Bazetto[58], F. Raffaelli[22], F. Ragusa[31,46], Y. Ramachers[77], A. Ramirez[69], S. Ravinthiran[58], M. Razeti[13], A. L. Renshaw[69], A. Repond[71], M. Rescigno[27], S. Resconi[31], F. Retiere[11], L. P. Rignanese[39], A. Ritchie-Yates[61], A. Rivetti[25], A. Roberts[58], C. Roberts[61], G. Rogers[74], L. Romero[20], M. Rossi[29], A. Rubbia[62], D. Rudik[34,50,73], J. Runge[79], M. A. Sabia[5,27,47], P. Salomone[4,5], O. Samoylov[72], S. Sanfilippo[66], D. Santone[24], R. Santorelli[20], E. M. Santos[8], I. Sargeant[88], C. Savarese[90], E. Scapparone[39], F. G. Schuckman[51], G. Scioli[39,40], D. A. Semenov[49], M. Sestu[13,14], V. Shalamova[71], S. Sharma Poudel[69], A. Sheshukov[72], M. Simeone[34,80], P. Skensved[51], M. D. Skorokhvatov[53,73], O. Smirnov[72], T. Smirnova[71], B. Smith[11], F. Spadoni[9], M. Spangenberg[77], A. Steri[13,81], V. Stornelli[4,43], S. Stracka[22], A. Sung[52], C. Sunny[5], Y. Suvorov[34,50,53], A. M. Szelc[68], O. Taborda[3,4], R. Tartaglia[4], A. Taylor[58], J. Taylor[58], G. Testera[29], K. Thieme[64], A. Thompson[19], S. Torres-Lara[69], A. Tricomi[6,7], S. Tullio[13,14], E. V. Unzhakov[49], M. Van Uffelen[24], P. Ventura[8], T. Viant[62], S. Viel[2], A. Vishneva[72], R. B. Vogelaar[35], J. Vossebeld[58], B. Vyas[2], M. Wada[5], M. Walczak[3,4], Y. Wang[67,82], S. Westerdale[71], L. Williams[84], M. M. Wojcik[44], M. Wojcik[85], C. Yang[67,82], J. Yin[67,82], A. Zabihi[5], P. Zakhary[6,7], A. Zani[31], Y. Zhang[67], T. Zhu[55], A. Zichichi[39,40], G. Zuzel[44], M. P. Zykova[16]

[1] Fondazione Bruno Kessler, 38123 Povo, Italy
[2] Department of Physics, Carleton University, Ottawa, ON K1S 5B6, Canada
[3] Gran Sasso Science Institute, 67100 L'Aquila, Italy
[4] INFN Laboratori Nazionali del Gran Sasso, 67100 Assergi, AQ, Italy
[5] AstroCeNT, Nicolaus Copernicus Astronomical Center of the Polish Academy of Sciences, 00-614 Warsaw, Poland
[6] INFN Catania, 95121 Catania, Italy
[7] Università of Catania, 95124 Catania, Italy
[8] Instituto de Física, Universidade de São Paulo, São Paulo 05508-090, Brazil
[9] Pacific Northwest National Laboratory, Richland, WA 99352, USA
[10] Physics Department, Augustana University, Sioux Falls, SD 57197, USA

[11] TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3, Canada
[12] Physics Department, Columbia University, New York, NY 10027, USA
[13] INFN Cagliari, 09042 Cagliari, Italy
[14] Physics Department, Università degli Studi di Cagliari, 09042 Cagliari, Italy
[15] Department of Physics, University of Alberta, Edmonton, AB T6G 2R3, Canada
[16] Mendeleev University of Chemical Technology, Moscow 125047, Russia
[17] INFN Laboratori Nazionali di Legnaro, 35020 Legnaro, Padova, Italy
[18] Savannah River National Laboratory, Jackson, SC 29831, USA
[19] Department of Physics, Royal Holloway University of London, Egham TW20 0EX, UK
[20] CIEMAT, Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas, 28040 Madrid, Spain
[21] Centre de Physique des Particules de Marseille, Aix Marseille Univ, CNRS/IN2P3, CPPM, Marseille, France
[22] INFN Pisa, 56127 Pisa, Italy
[23] Physics Department, Università degli Studi di Pisa, 56127 Pisa, Italy
[24] University of Oxford, Oxford OX1 2JD, UK
[25] INFN Torino, 10125 Turin, Italy
[26] Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Turin, Italy
[27] INFN Sezione di Roma, 00185 Rome, Italy
[28] Physics Department, Università degli Studi di Genova, 16146 Genoa, Italy
[29] INFN Genova, 16146 Genoa, Italy
[30] Civil and Environmental Engineering Department, Politecnico di Milano, 20133 Milan, Italy
[31] INFN Milano, 20133 Milan, Italy
[32] Institute of Radioelectronics and Multimedia Technology, Faculty of Electronics and Information Technology, Warsaw University of Technology, 00-661 Warsaw, Poland
[33] INFN Roma Tre, 00146 Rome, Italy
[34] INFN Napoli, 80126 Naples, Italy
[35] Virginia Tech, Blacksburg, VA 24061, USA
[36] Department of Electrical and Electronic Engineering, Università degli Studi di Cagliari, 09123 Cagliari, Italy
[37] Centro de Astropartículas y Física de Altas Energías, Universidad de Zaragoza, 50009 Zaragoza, Spain
[38] Skobeltsyn Institute of Nuclear Physics, Lomonosov Moscow State University, Moscow 119234, Russia
[39] INFN Bologna, 40126 Bologna, Italy
[40] Department of Physics and Astronomy, Università degli Studi di Bologna, 40126 Bologna, Italy
[41] Department of Physics and Astronomy, Laurentian University, Sudbury, ON P3E 2C6, Canada
[42] SNOLAB, Lively, ON P3Y 1N2, Canada
[43] Department of Industrial and Information Engineering and Economics, Università degli Studi dell'Aquila, 67100 L'Aquila, Italy
[44] M. Smoluchowski Institute of Physics, Jagiellonian University, 30-348 Krakow, Poland
[45] Department of Structures for Engineering and Architecture, Università degli Studi "Federico II" di Napoli, 80126 Naples, Italy
[46] Physics Department, Università degli Studi di Milano, 20133 Milan, Italy
[47] Physics Department, Sapienza Università di Roma, 00185 Rome, Italy
[48] Chemistry, Materials and Chemical Engineering Department "G. Natta", Politecnico di Milano, 20133 Milan, Italy
[49] Saint Petersburg Nuclear Physics Institute, Gatchina 188350, Russia
[50] Physics Department, Università degli Studi "Federico II" di Napoli, 80126 Naples, Italy
[51] Department of Physics, Engineering Physics and Astronomy, Queen's University, Kingston, ON K7L 3N6, Canada
[52] Physics Department, Princeton University, Princeton, NJ 08544, USA
[53] National Research Centre Kurchatov Institute, Moscow 123182, Russia
[54] Radiation Physics Laboratory, Belgorod National Research University, Belgorod 308007, Russia
[55] Department of Physics, University of California, Davis, CA 95616, USA
[56] Physics Department, Lancaster University, Lancaster LA1 4YB, UK
[57] APC, Université de Paris, CNRS, Astroparticule et Cosmologie, 75013 Paris, France
[58] Department of Physics, University of Liverpool, The Oliver Lodge Laboratory, Liverpool L69 7ZE, UK
[59] Budker Institute of Nuclear Physics, Novosibirsk 630090, Russia
[60] Museo Storico della Fisica e Centro Studi e Ricerche Enrico Fermi, 00184 Rome, Italy

[61] Department of Physics and Astronomy, The University of Manchester, Manchester M13 9PL, UK
[62] Institute for Particle Physics and Astrophysics, ETH Zurich, 8093 Zurich, Switzerland
[63] Department of Physics and Astronomy, Williams College, Williamstown, MA 01267, USA
[64] Department of Physics and Astronomy, University of Hawai'i, Honolulu, HI 96822, USA
[65] Department of Physics and Kavli Institute for Cosmological Physics, University of Chicago, Chicago, IL 60637, USA
[66] INFN Laboratori Nazionali del Sud, 95123 Catania, Italy
[67] Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China
[68] School of Physics and Astronomy, University of Edinburgh, Edinburgh EH9 3FD, UK
[69] Department of Physics, University of Houston, Houston, TX 77204, USA
[70] Pharmacy Department, Università degli Studi "Federico II" di Napoli, 80131 Naples, Italy
[71] Department of Physics and Astronomy, University of California, Riverside, CA 92507, USA
[72] Joint Institute for Nuclear Research, Dubna 141980, Russia
[73] National Research Nuclear University MEPhI, Moscow 115409, Russia
[74] School of Physics and Astronomy, University of Birmingham, Edgbaston, Birmingham B15 2TT, UK
[75] Institute of Experimental Physics, University of Hamburg, Luruper Chaussee 149, 22761 Hamburg, Germany
[76] Physics Department, Temple University, Philadelphia, PA 19122, USA
[77] Department of Physics, University of Warwick, Coventry CV47AL, UK
[78] Istituto Nazionale di Fisica Nucleare, 00186 Rome, Italy
[79] Amherst Center for Fundamental Interactions and Physics Department, University of Massachusetts, Amherst, MA 01003, USA
[80] Chemical, Materials, and Industrial Production Engineering Department, Università degli Studi "Federico II" di Napoli, 80126 Naples, Italy
[81] Department of Mechanical, Chemical, and Materials Engineering, Università degli Studi, 09042 Cagliari, Italy
[82] University of Chinese Academy of Sciences, Beijing 100049, China
[83] Physics and Astronomy Department, University of California, Los Angeles, CA 90095, USA
[84] Department of Physics and Engineering, Fort Lewis College, Durango, CO 81301, USA
[85] Institute of Applied Radiation Chemistry, Lodz University of Technology, 93-590 Lodz, Poland
[86] Science and Technology Facilities Council (STFC), Rutherford Appleton Laboratory, Technology, Harwell Oxford, Didcot OX11 0QX, UK
[87] Engineering and Architecture Department, Università di Enna Kore, 94100 Enna, Italy
[88] Science and Technology Facilities Council (STFC), Rutherford Appleton Laboratory, Particle Physics Department, Harwell Oxford, Didcot OX11 0QX, UK
[89] Department of Mathematics and Physics, Roma Tre University, 00146 Rome, Italy
[90] Center for Experimental Nuclear Physics and Astrophysics, and Department of Physics, University of Washington, Seattle, WA 98195, USA