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Exploiting nonlinear oscillator dynamics for on-chip thermal sensing

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ABSTRACT

Real-time monitoring of temperature in FPGAs is crucial to ensure system reliability, as local temperature variations can affect their performance. For these purposes, virtual temperature sensors such as Ring Oscillator (RO)-based sensors are widely used. However, efficiently implementing them with a minimal number of Look-Up Tables (LUTs) remains a significant challenge. In this paper, we propose a novel temperature sensor architecture based on nonlinear oscillators, implemented on a 28 nm Artix-7 FPGA. The proposed approach minimizes the usage of FPGA resources while maintaining accurate thermal sensing. As a result, several nonlinear oscillators are analyzed, achieving better sensitivity (0.020%/°C) over a 25 % wider temperature range compared to other RO-based temperature sensors reported in the literature for the 28 nm technology node. These results highlight the potential of these oscillators as efficient, low-resource alternatives for real-time thermal monitoring in FPGA.

1. Introduction

Field-Programmable Gate Arrays (FPGAs) offer great flexibility for implementing embedded systems. However, their performance can be significantly affected by temperature and voltage variations. For this reason, real-time sensing in FPGAs becomes essential to detect thermal changes and apply mitigation strategies to prevent overheating, thus preserving reliability and durability. In this regard, several temperature [1,2] and voltage [3] sensors in FPGAs have already been proposed in the literature.

In particular, temperature sensors can be calibrated to measure either ambient temperature or the internal temperature of the chip. In addition, they can be externally connected to the FPGA or integrated within it. However, it should be noted that external sensors can only measure temperature at a specific point, limiting their performance for detecting thermal gradients within the device. However, integrated FPGA sensors offer several advantages [4]. Firstly, they can be implemented post-fabrication as they leverage the internal resources of the FPGA. Secondly, they can be placed at specific locations on the chip. This approach enables the implementation of sensor arrays, allowing for precise monitoring of the temperature gradient across the FPGA and the detection of hotspots [5].

It is widely known that the frequencies of Ring Oscillators (ROs) implemented in FPGA exhibit a dependence on temperature. For this reason, several studies have focused on the implementation of RO-based temperature sensors in FPGAs [6,7]. However, some works have highlighted the difficulty of implementing low-stage oscillators using only Look-Up Tables (LUTs), as their implementation can in some cases lead to nonmonotonic frequency–temperature behavior [8], limiting their suitability as temperature sensors. This behavior can be explained by the opposing effects that temperature has on carrier mobility and the transistor threshold voltage. In the initial stages, the impact of the threshold voltage predominates, particularly due to the extensive use of pass-transistor stages in the FPGA architecture [8]. As the temperature rises, both effects tend to counterbalance each other. However, at higher temperatures, the reduction in carrier mobility becomes the dominant factor. For this reason, only oscillators with a large number of inverter stages exhibit stable and predictable behavior that can be effectively exploited for temperature measurement applications [9,10].

In this work, a novel temperature sensor for FPGAs implemented using LUTs, based on the bias of nonlinear oscillators, is proposed. Traditionally, these oscillator architectures, such as the Galois Ring Oscillator (GARO) [11], have been used as True Random Number Generators (TRNGs) [12,13]. More recently, it has been observed that they can also be used to construct Physically Unclonable Functions (PUFs) [14]. This study reveals that the bias of certain nonlinear oscillator architectures exhibits a clear dependence on both the external and internal temperature of the FPGA, highlighting their suitability for temperature sensing applications in FPGA.

This paper is organized as follows: Section 2 presents the proposed temperature sensor as well as the implementation in FPGA; Section 3 evaluates its performance; and finally, conclusions are shown in Section 4.

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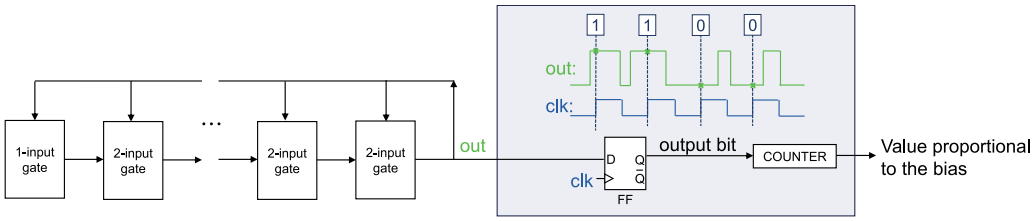


Fig. 1. Schematic of the bias measurement process.

2. Proposed sensor

2.1. Nonlinear oscillator design

The architecture of the proposed nonlinear oscillators consists of a combination of logic gates in a cascade. Each logic gate has two inputs: one is the output of the previous gate and the other is the feedback signal. The combination of various types of logic gates leads to different oscillator configurations, each referred to as a "configuration" in this study.

In this case, instead of measuring the frequency of the oscillators, the statistical bias is used. The statistical bias is a dimensionless parameter proportional to the number of logic ones of the signal when sampled with a reference clock over a certain time interval. In this case, a reference clock with a frequency of 1 MHz was used. A Flip-Flop (FF) is used to fix the measured bit value and a counter is implemented to store the number of ones. This value is proportional to the bias of the oscillator, which is calculated by dividing the number stored in the counter by the total number of samples. Fig. 1 summarizes this process.

2.2. Physical basis

The temperature-dependent bias observed at the output of the LUT-based nonlinear oscillator originates from the fact that temperature affects the propagation delays of rising and falling signal transitions differently. In the presence of nonlinear feedback, these delay asymmetries are amplified and translated into measurable changes in the output bit statistics. In an FPGA, a LUT is internally implemented as a complex CMOS network. Fundamentally, however, the effective propagation delay depends on the load capacitance (C_L) and on the drive current of the NMOS/PMOS networks ((I_N, I_P)). It is well known that the propagation times for a transition exhibit the following dependence:

$$t_{pHL} \propto C_L \cdot \frac{V_{DD}}{I_N(T)}, \quad t_{pLH} \propto C_L \cdot \frac{V_{DD}}{I_P(T)} \tag{1}$$

where t_{pHL} (high → low) is dominated by NMOS devices (discharge) and t_{pLH} (low → high) by PMOS devices (charge). Temperature affects I_N and I_P through two main mechanisms:

- Carrier mobility μ, which decreases with T (phonon scattering), reducing the current and increasing the delay.
- Threshold voltage V_{TH}, which typically decreases with T, increasing the current and reducing the delay.

The net result over typical operating ranges (e.g., −20 to 80 °C) and for standard CMOS technologies is usually an increase in delay with T (mobility-dominated behavior). However, what is relevant for our sensor is that NMOS and PMOS devices do not vary identically (due to differences in mobility, effective threshold voltage, internal LUT topology, and load/routing), which leads to:

$$t_{pHL}(T) \neq t_{pLH}(T) \quad \text{and} \quad \frac{d}{dT}\left(t_{pHL} - t_{pLH}\right) \neq 0 \tag{2}$$

This difference is the physical origin of a duty cycle different from 50 % and of its drift with temperature. If the oscillating signal does not exhibit a perfectly symmetric cycle (different times spent at '1' and '0'), $T_H(T)$ and $T_L(T)$, respectively, the duty cycle can be written as:

$$D(T) = \frac{T_H(T)}{T_H(T) + T_L(T)} \tag{3}$$

If, for simplicity, we particularize to a simple N-stage ring oscillator with odd N, we obtain:

$$T_H(T) \approx \frac{1}{2}(N+1)t_{pHL}(T) + \frac{1}{2}(N-1)t_{pLH}(T) \tag{4}$$

$$T_L(T) \approx \frac{1}{2}(N+1)t_{pLH}(T) + \frac{1}{2}(N-1)t_{pHL}(T) \tag{5}$$

Therefore:

$$D(T) \approx \frac{1}{2} + \frac{t_{pHL}(T) - t_{pLH}(T)}{2N[t_{pHL}(T) + t_{pLH}(T)]} \tag{6}$$

It follows that the duty cycle deviates from 0.5 when there is asymmetry between rising and falling delays, and that any differential variation with T will be reflected in $D(T)$. When the output is sampled uniformly (or sufficiently "incoherently") with respect to the oscillator phase, the probability of reading a '1', $P(1)$, is closely related to the fraction of time the signal remains high:

$$P(1) \approx D(T) \Rightarrow B(T) = P(1) - 0.5 \approx D(T) - 0.5 \tag{7}$$

This equality is approximate due to jitter, metastability, and sampling nonidealities, but it remains a monotonic and calibratable relationship under controlled experimental conditions (fixed sampling point, stable V_{DD}, constant sampling window).

In nonlinear architectures with multiple feedback paths, the system does not behave like a "linear" ring oscillator in which delay accumulates uniformly. Nonlinear feedback introduces competition among multiple logic and routing paths (with different NMOS/PMOS weights and different loads), as well as a strong dependence on the relative switching instants: small temperature-induced delay changes can alter the temporal ordering of events and, consequently, the dynamic pattern of the oscillator. As a result, small thermal variations that differentially affect t_{pHL} and t_{pLH} not only smoothly shift the frequency, but also produce significant changes in the temporal asymmetry of the cycle, which translate into changes in the output statistics (bias). In terms of sensitivity, nonlinearity acts as a "gain" mechanism for temperature variations, explaining why the bias may exhibit a stronger dependence on temperature than the frequency in conventional oscillators.

It should be noted that nonlinear oscillators with feedback constitute inherently complex architectures, whose dynamic behavior results from the interaction of multiple logic paths, temperature-dependent delays, nonlinearities, and statistical effects. At present, there is no analytical theoretical model that allows one to predict the bias sensitivity from the oscillator topology or to establish a systematic criterion for architecture selection. For this reason, in this work the oscillator choice has been made empirically, by evaluating different topologies and selecting those that exhibit a stable, monotonic, and reproducible dependence of the bias on temperature.

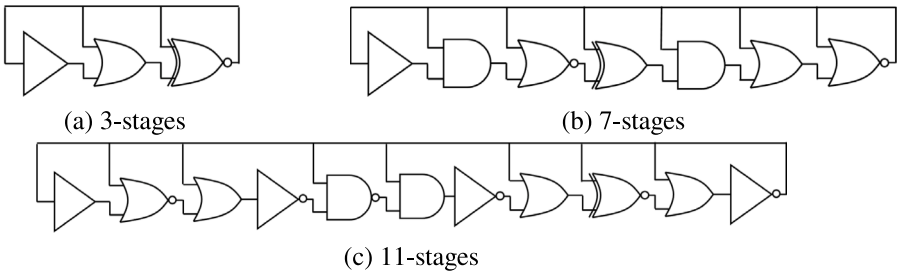
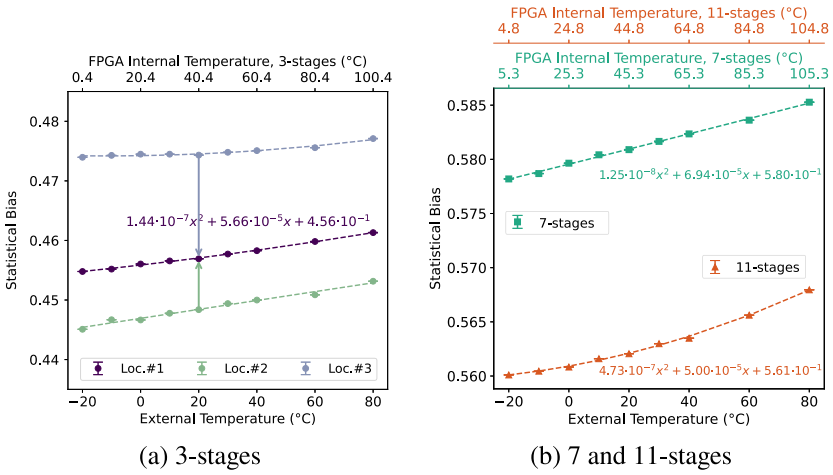


Fig. 2. (a) 3, (b) 7, (c) and 11 stages DNOs. The number of stages refers to the minimum number of LUTs required to implement these oscillators.



(a) 3-stages (b) 7 and 11-stages

Fig. 3. Calibration for (a) 3, (b) 7, and 11-stages DNO.

2.3. Implementation

Three oscillators of 3, 7, and 11 stages have been analyzed. The number of stages refers to the minimum number of LUTs required to implement these oscillators, so that each logical operation is implemented in a single LUT. Subsequently, several configurations have been generated randomly, considering the recommendations mentioned in [15] to ensure high reproducibility. Among the configurations that produced an oscillating output, one configuration has been selected for each number of stages (Fig. 2a, b and c). These temperature sensors have been implemented on a PYNQ-Z2 board, which contains a 28 nm Artix-7 FPGA. Additionally, the routing of the DNOs has been fixed so that the same sensor can be implemented in different locations, ensuring that the routing does not affect their performance.

The dependence of statistical bias on temperature in the previously explained DNOs, from the perspective of FPGA implementation, is due to changes in the propagation delays of the Look-Up Tables (LUTs). These FPGA elements are active components, and their electrical behavior varies with environmental factors such as temperature, since the characteristics of the internal transistors — carrier mobility, leakage currents, and switching times — are directly and systematically affected by it. This variation induces predictable modifications in the delays of logical paths, enabling DNOs to exhibit high thermal sensitivity. Thanks to this property, DNOs can exploit delay-competition statistics between equivalent logical paths, overcoming the limitations of frequency-based sensors.

2.4. Calibration

The starting hypothesis is that, just as temperature affects the oscillation frequency of a conventional ring oscillator, it also influences the bias of nonlinear oscillators —potentially— in a more pronounced way. For this reason, the bias of the three nonlinear oscillators have been measured 100 times at different temperatures during one second. This time allows proper oscillator analysis but could be reduced with similar error. A possible source of measurement inaccuracy is self-heating of the circuit induced by switching activity. To minimize this effect, the measurement cycle is usually kept short, and oscillation is disabled when no measurement is required. The temperature has been varied using the Aralab Fitoterm 22E thermal chamber, ranging from −20 °C to 80 °C, i.e., within the extended commercial temperature range. The average bias and its standard deviation have been obtained for each temperature. In Fig. 3a and b, the bias-temperature dependence for the three oscillators is shown. These temperature sensors could be calibrated either to measure the external temperature or to monitor the internal temperature of the FPGA, measured using the *on-chip Xilinx-Analog-to-Digital-Converter (XADC)*. For this reason, the figure shows their dependence on both measurements. As it can be seen, although the dependence of the bias within the temperature can vary depending on the selected configuration, in all three cases the bias tends to increase as the temperature rises.

As explained in [4], the frequency–temperature dependence of conventional ring oscillators in modern FPGAs typically follows a nonlinear function. In this case, for some configurations, the bias-temperature relationship $B(T)$ appears to be more linear. However, as this dependence can vary depending on the configuration, data have been fitted to a second-order polynomial: $B(T) = a_2 \cdot T^2 + a_1 \cdot T + a_0$. Once the calibration of the sensor is performed, the temperature can be derived given the bias using the inverse function $B^{-1}(T)$, which can be easily calculated since the function is monotonically increasing in the temperature range. In this case, 15 bits have been used to perform the bias-temperature calibration.

2.5. Oscillator location

Although the bias-temperature relationship tends to be approximately constant across different locations for a given configuration,

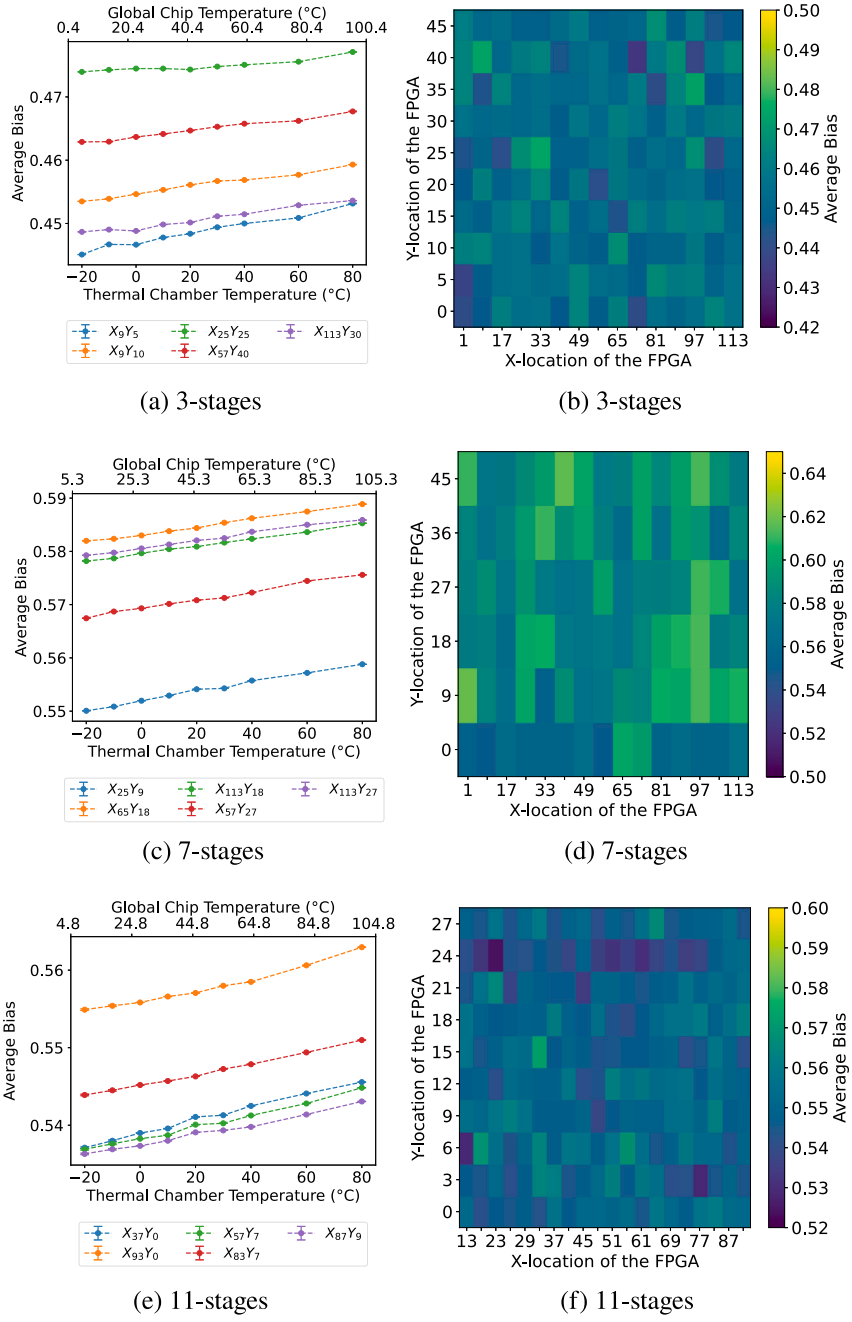
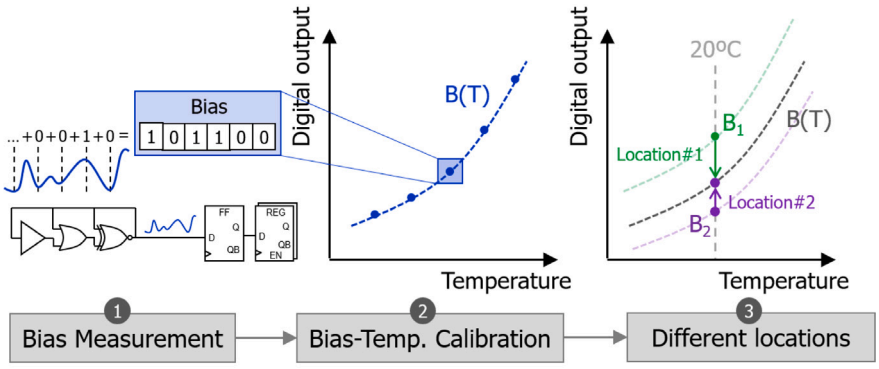


Fig. 4. Bias-temperature dependence at different locations for (a) 3-stages, (c) 7-stages and (e) 11-stages DNOs. Distribution of the average bias (b) 3-stages, (d) 7-stages and (f) 11-stages DNOs within their FPGA location.

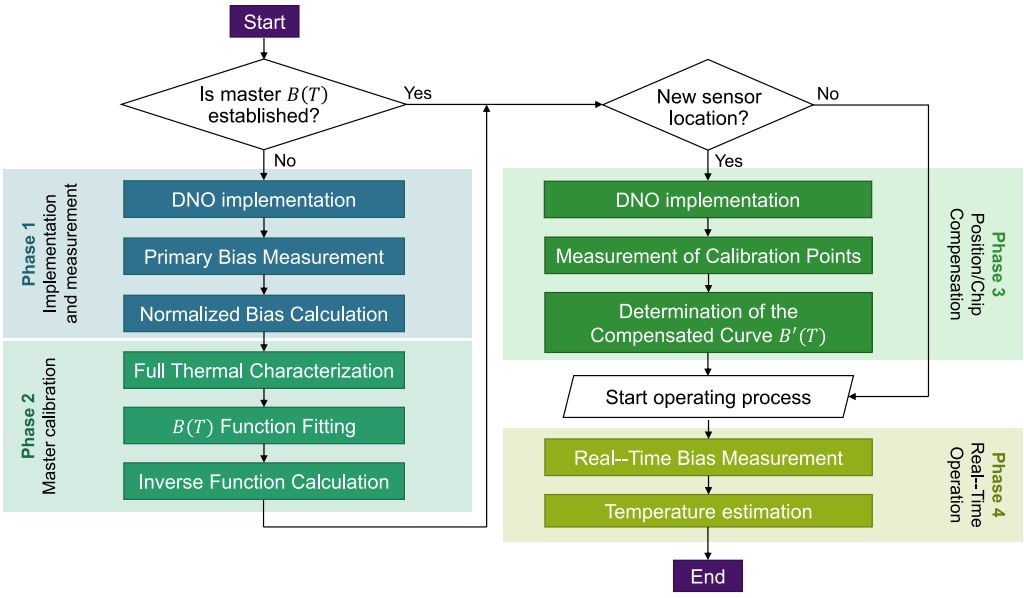
this dependence can vary slightly depending on the specific oscillator configuration used and its location. The curve may also be shifted vertically depending on the placement of the oscillator in the FPGA as it can be seen in Locations 1 and 2 of the 3-stages oscillator of Fig. 3a. While the rate at which the bias grows with temperature (the slope) remains nearly constant for many locations (such as Loc. 1 and Loc. 2), other locations (like Loc. 3) may exhibit a slightly different slope. In Fig. 4a, c, and e; the bias trend of several of these oscillators at different FPGA locations is shown as a function of temperature. Similarly, in Fig. 4b, d, and f; the distribution of the average bias for oscillators with three different stage counts is shown.

This way, to calibrate a second oscillator and obtain its curve $B'(T)$ given another oscillator and its curve $B(T)$, in most cases it is sufficient to perform a one-point calibration at a reference temperature. This process is summarized in Fig. 5a. However, from a practical standpoint, and specifically to account for the slight variations in the slope across different placements, relying only on a single-point calibration might not be sufficient to maintain high accuracy. Fig. 5b shows the summarized process in a flowchart.

As explained, although the curve increases monotonically, the rate at which the bias grows with temperature remains approximately constant across different locations for each configuration. This means that the differences between biases remain nearly unchanged with temperature. As a result, this architecture is particularly useful to construct PUFs where the output bit is determined by comparing pairs of oscillators at different locations, making a PUF built with this configuration robust to temperature variations.



(a) Temperature sensor operation principle.



(b) Temperature sensor operation principle flowchart.

Fig. 5. Temperature sensor operation principle and corresponding flowchart.

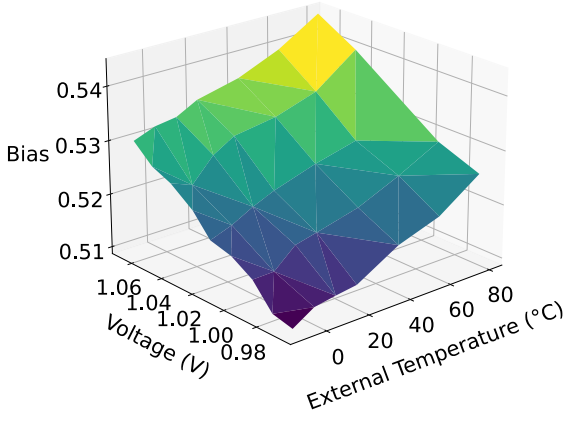


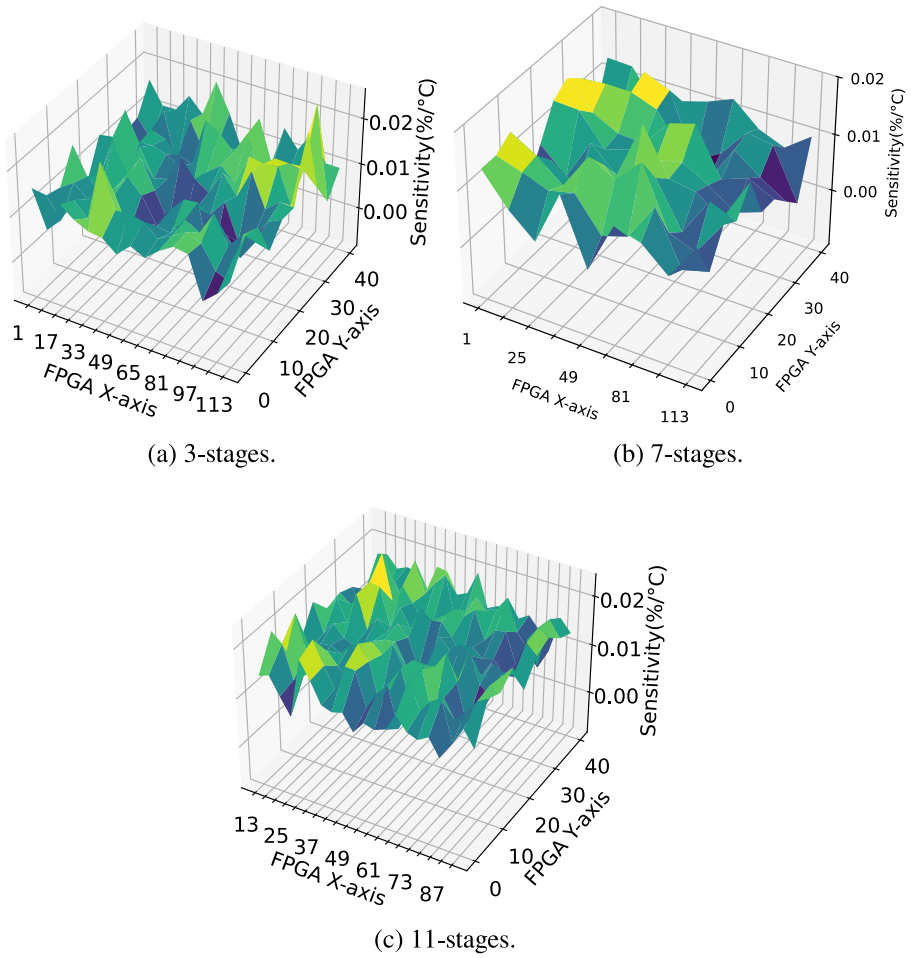
Fig. 6. Voltage-temperature-bias dependence of 11-stages DNO.

2.6. Voltage and aging variations

Finally, the temperature sensor could be made robust against variations in the supply voltage if there exists a well-defined voltage-temperature-bias surface. In Fig. 6, the bias surface obtained for a nonlinear 11-stage oscillator configuration is shown, where a well-defined surface can be seen such that a sensor based on this oscillator configuration would also be stable against FPGA voltage variations of up to ~5 % in the analyzed temperature range. Similar results are obtained for the 3- and 7-stage oscillators.

It is important to emphasize that the proposed sensor does not rely on an absolute measurement of delay or frequency, but on a statistical property (bias) associated with the dynamic behavior of the nonlinear oscillator. Aging due to NBTI/PBTI primarily manifests as a slow, quasi-monotonic shift of the threshold voltages, leading to a gradual increase in delays. In any case, aging-induced variation occurs over the long term, making it necessary in practice to compensate for aging through periodic recalibrations.

However, in 28 nm FPGAs, PBTI-induced aging in NMOS devices typically exhibits a very weak temperature dependence, with NBTI in PMOS devices being the dominant mechanism and only at very



(a) 3-stages. (b) 7-stages.

(c) 11-stages.

Fig. 7. Sensitivity within FPGA location for cases with worst and best average sensitivity: (a) 3-stages, (b) 7-stages and (c) 11-stages nonlinear oscillators.

high temperatures (>125 °C), which are well above our measurement range. Since the sensor operates at nominal voltage and with controlled activity cycles (oscillation enabled only during measurement windows), the electrical stress remains within recommended operating conditions, mitigating the severity of aging.

3. Sensor performance evaluation

3.1. Temperature sensor evaluation

The suitability of nonlinear oscillators as temperature sensors has been analyzed in terms of FPGA resource utilization, temperature range, and sensitivity. The obtained results are presented in Table 1, along with a comparison with other oscillator-based sensors implemented on FPGA on the same technology (28 nm) and other technologies. As it is later explained, the smaller the technology node, the more challenging it becomes to implement an efficient temperature sensor.

3.1.1. Resource utilization

The implementation of this temperature sensor requires both an oscillator and a counter. In this case, a simple counter consisting of an array of registers which can store up to two bytes has been implemented. A FF is also required to sample the signal. Regarding the oscillator, implementing the 3, 7, and 11-stage versions requires 3, 7, and 11 LUTs, respectively. As shown in Table 1, the proposed nonlinear oscillators allow implementing a temperature sensor exclusively with LUTs, while requiring only a minimal amount of them. This addresses one of the issues mentioned in [8] regarding the need to use oscillators with a high number of LUTs (35-LUTs) to start observing a trend between the parameter extracted from the oscillator (traditionally the frequency, in our case the bias) and temperature. Fast Carry Chains (FCC) are used in modern FPGAs to enhance the efficiency of arithmetic operations. In [8], FCCs are used to implement oscillators. Each stage of the oscillator consists of 2 LUT-pass (plus 1 LUT-nand in the first stage) and the FCC, which is formed by 4 MUX and 4 XOR, two of each used in one stage.

3.1.2. Temperature range

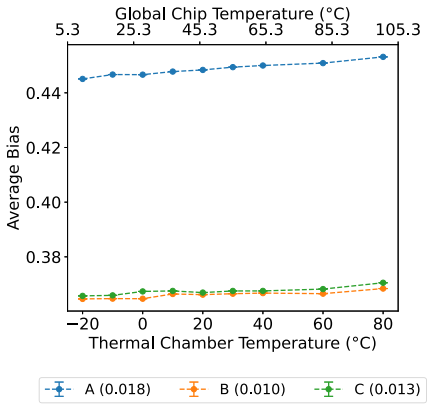
The temperature sensor designs based on the three proposed nonlinear oscillators have been tested over the extended commercial temperature range, from −20 °C to 80 °C, demonstrating their effective usability within this range. As shown in Table 1, this means that the proposed temperature sensor offers a wider operating range compared to other designs implemented in the same technology node.

3.1.3. Sensitivity

To evaluate the sensitivity of a temperature sensor based on a conventional ring oscillator, it is defined as:

$$S = \frac{\Delta f}{\Delta T} = \frac{f(T_{\max}) - f(T_{\min})}{T_{\max} - T_{\min}} \quad \left[\text{Hz}/^{\circ}\text{C}\right], \tag{8}$$

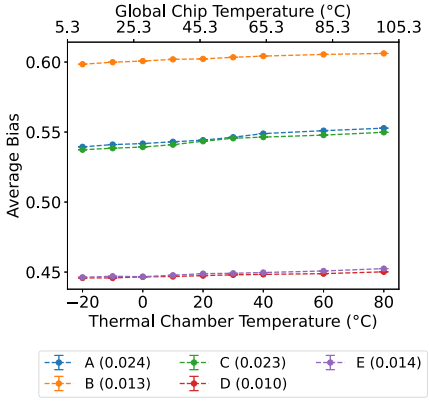
where $T_{\max}$ and $T_{\min}$ are the maximum and minimum temperatures within the operation range of the sensor, while $f(T_{\max})$ and $f(T_{\min})$ are the measured frequencies at these temperatures, respectively. Typically, sensitivity is expressed in units of %/°C, removing the dependence on Hz. This is particularly relevant in this case, since in the



(a) 3-stages average bias

Index	Configuration
A	DEL-NAND-NAND
B	NOT-AND-NAND
C	NOT-DEL-NAND

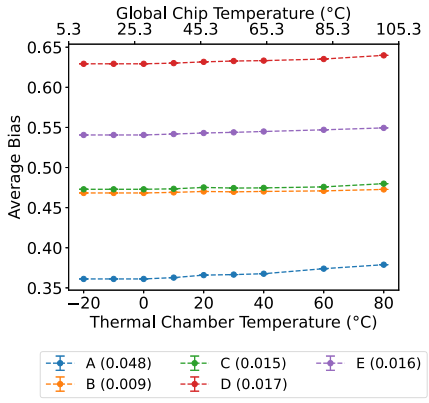
(b) 3-stages configurations



(c) 7-stages average bias

Index	Configuration
A	DEL-XNOR-OR-AND-AND-XOR-NOR
B	DEL-AND-NOR-XOR-AND-OR-NOR
C	NOT-NOR-NOR-NAND-AND-DEL-NOR
D	DEL-AND-XOR-NOR-XNOR-OR-NOT
E	DEL-NOR-OR-NOT-OR-OR-NOT

(d) 7-stages configurations



(e) 11-stages average bias

Index	Configuration
A	NOT-NAND-AND-XNOR-NOT-XNOR-XOR-NOT-NAND-DEL-NAND
B	NOT-OR-DEL-XOR-XNOR-OR-NOR-AND-NOT-XOR-DEL
C	DEL-XNOR-XOR-NOT-AND-NOR-XOR-NOT-NOR-OR-XOR
D	DEL-XNOR-NAND-XNOR-NOT-NOR-NAND-XNOR-DEL-OR-NOR
E	DEL-NOR-OR-NOT-NAND-AND-NOT-OR-XNOR-OR-NOT

(f) 11-stages configurations

Fig. 8. Bias-temperature dependence for other configurations of oscillators with (a) 3, (c) 7 and (e) 11 stages; and corresponding configurations with (b) 3, (d) 7 and (f) 11 stages.

proposed nonlinear oscillators, the frequency is not an output variable. This way, the normalized sensibility is defined as:

$$S_n = \frac{S}{f_{\text{ref}}} \cdot 100 \qquad [\%/°\text{C}], \tag{9}$$

where f_{ref} is the frequency at room temperature. In this case, it should be noted that we are not measuring frequencies, and f in (8) and f_{ref} in (9) correspond to the bias B and B_{ref} respectively. Thus, based on (9) and the values of the bias obtained in Fig. 3a and b, the sensitivity of the oscillators of 3, 7, and 11-stages has been calculated. The results are shown in Table 1 and compared with other state-of-the-art approaches.

Firstly, previous studies have shown that as the technology node decreases, the oscillator frequency is no longer significantly affected by temperature, as the influence of carrier mobility ceases to be dominant [18]. This directly impacts sensitivity, which is why higher sensitivity is observed in designs implemented on FPGAs with a larger technology node [4,16]. At the 28 nm node, some works such as [8,17], have proposed alternative oscillator architectures to improve sensitivity compared to conventional ring oscillators. Compared to these approaches, the 7-stage and 11-stage oscillators achieve better sensitivity: 0.016%/°C and 0.020%/°C, respectively. Meanwhile, the 3-stage design achieves a similar sensitivity (0.013%/°C) while requiring only

Table 1
FPGA resources, temperature range, sensitivity, power, and comparison with other oscillator-based proposals.

Work	Tech.	Resources	Range (°C)	S_n (%/°C)	Power[a]
[16]	90 nm	48 LUT	34–79	0.110	–
[4]	65 nm	5 LUT	5–90	0.098	$\hat{P}_{OH}$ in [0.69, 1.07][b]
[8]	28 nm	35 LUT	0–80	0.008	0.96 pJ/transition (single)
		3 FCC	0–80	0.014	
		5 FCC	0–80	0.010	
		9 FCC	0–80	0.011	
[17]	28 nm	7 LUT + 7 Latch	45–70	0.010	~5 W total system consumption (single)
This	28 nm	3 LUT	−20–80	0.013	0.116 W[c]
		7 LUT	−20–80	0.016	0.119 W[c]
		11 LUT	−20–80	0.020	0.122 W[c]

[a] Power metrics vary widely across the papers. Some report only the consumption of a single oscillator, others report a single oscillator but include the entire measurement system, and others present data for an oscillator array.
[b] In this work, they define the "differential average power consumption" (P_{OH}) as the difference between the system's power consumption with the oscillator array and its consumption without it. The value $\hat{P}_{OH}$ given corresponds to the normalized power overhead.
[c] Estimations of the power consumption of a matrix of with the same number of oscillators (200) of 3-stages, 7-stages and 11-stages respectively. Static consumption remains constant across the three cases. More details are shown in Section 3.2

3 LUTs to implement the oscillator. It must be noticed that this sensitivity may vary depending on the location on the FPGA, especially in the case of the 3-stage oscillator (Fig. 7), and that these values correspond to average sensitivities.

3.1.4. Oscillator configuration

In Section 2.2, the basic principles supporting the proposed approach were explained. However, it should be noted that the performance of the temperature sensor can vary significantly depending on the logic gate configuration. In this work, three configurations exhibiting good reliability were selected and used to implement the sensor. For completeness and with the aim of enabling future optimizations of DNO structures, Fig. 8 shows the bias–temperature curves for different DNO configurations with 3, 7, and 11 stages. To enable a fair comparison, all sensors were evaluated at the same physical location, using the same LUTs and the same FPGA, under identical operating conditions.

First, it can be observed that several configurations exhibit similar curves, such as configurations A/C and E/D for the 7-stage oscillators. It has been observed that the gates located in the last positions of the oscillator are critical for implementing a DNO with high reproducibility. Therefore, these similarities may be due to the fact that these sets of oscillators have the same logic gates in their final positions. For the 7-stage DNOs: configurations A and C have a NOR gate in the last position, while E and D have an OR-NOT combination in the last two positions. In the 3-stage DNOs, fewer different configurations are observed because, with a smaller number of stages, there are also fewer possible combinations of logic gates.

Second, it is observed that, for each number of stages, all configurations tend to exhibit very similar slopes and are, in general, shifted with respect to one another. As a result, these DNO configurations yield very similar sensitivities of the same order of magnitude. A notable exception is configuration A of the 11-stage oscillators, which exhibits a stronger temperature dependence, particularly at higher temperatures.

3.1.5. Error budget and resolution

Finally, the error sources have been examined. Firstly, there is an error associated with the reproducibility of the bias measurement. A hundred repetitions of the bias have been performed for each temperature and configuration, and the standard deviation has been calculated (Fig. 9). As observed, the bias reproducibility error is $\sim 10^{-5}$ (10^{-9} °C in the worst-case scenario), which is negligible. Secondly, there is the error due to the fitting of the bias to the calibration curve. In this case, a root mean square error (RMSE) of 1.23 °C using 11-stages has been observed by using the second-order polynomial calibration curve. Among the state-of-the-art proposals analyzed, [4] reports a RMSE of

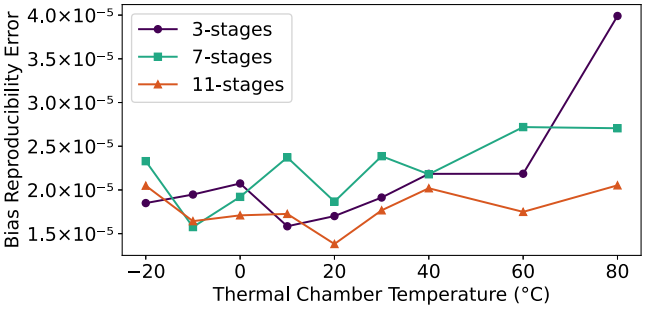


Fig. 9. Bias reproducibility error.

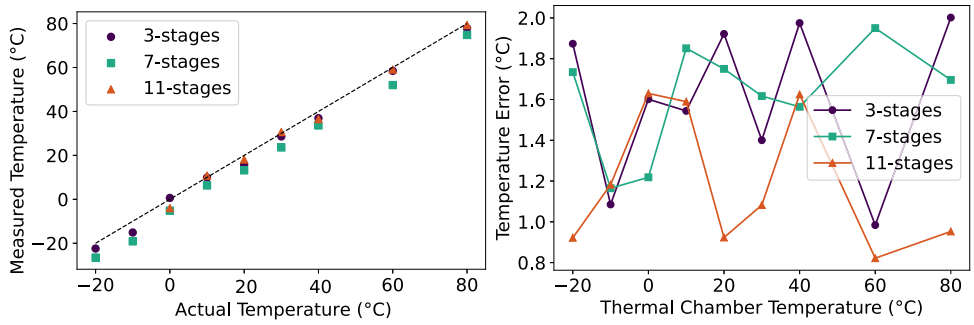
1.33 °C using a second-order polynomial in a larger technology node (65 nm). The rest of the references do not provide this information. This error depends on the configuration, and the purpose of this work is to demonstrate the feasibility of DNOs as sensors using arbitrary configurations. Considering the errors and temperature range, an equivalent resolution of 6 bits is obtained. Therefore, to perform the $B(T)$ calibration a smaller counter (less than 15 bits) could be used.

To provide a clearer insight into the error affecting the estimated temperature, Fig. 10 shows the estimated temperature for the three oscillator configurations with 3, 7, and 11 stages plotted against the actual temperature measured with the thermal camera. A diagonal dotted line is also included, representing the ideal case where both temperatures would be equal. As observed, this error varies depending on the configuration and the temperature. In particular, the 7-stage oscillator tends to exhibit slightly larger errors compared to the other configurations.

For a clearer analysis of the uniformity of the observed errors, Fig. 10 shows the errors obtained for each oscillator and temperature. Although the error is not uniform, no clear trend of increasing or decreasing with temperature is evident. However, it is noticeable that the error also varies according to the number of stages in the oscillator. Similarly, another thing that can be observed is that there is a correlation between this error and the reproducibility error shown in Fig. 9.

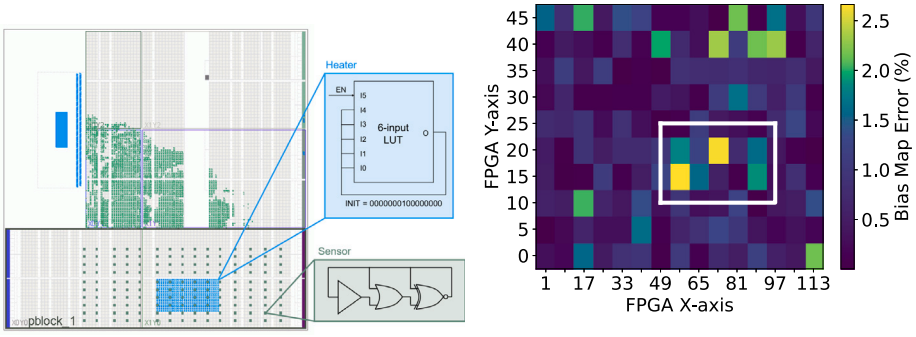
3.2. Temperature sensor network evaluation

One of the advantages of oscillator-based sensors is their ability to measure the temperature of the FPGA in real time, as well as their ability to detect hotspots. In some designs, this is crucial because temperature variations can affect certain architectures. To do

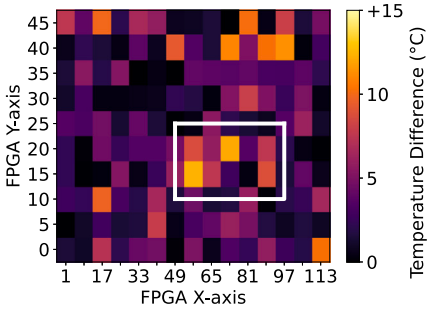


(a) Temperature transfer characteristic. (b) Detail of temperature errors.

Fig. 10. (a) Temperature transfer characteristic and (b) detail of temperature errors.



(a) FPGA implementation. (b) Bias map differences.



(c) Network temperature.

Fig. 11. (a) FPGA sensor matrix implementation of 3-stage nonlinear oscillators with heaters, (b) measured bias map differences and (c) network temperature.

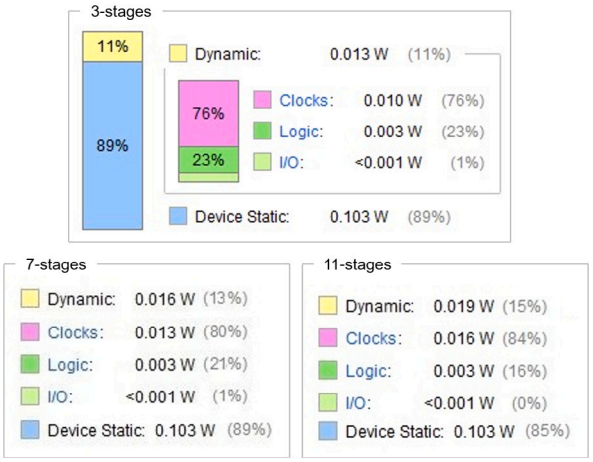
this a reference matrix of oscillator biases, $\mathbf{A}_{\text{ref}}$, measured at known temperature is compared with another matrix, $\mathbf{A}(\mathbf{t})$, measured at a different time t. To evaluate the suitability of the proposed oscillators for hotspot detection, a matrix of 3-, 7-, and 11-stage oscillators has been implemented in the lower region of the FPGA (Fig. 11a).

Furthermore, a *pblock* has been placed around the array to prevent Vivado from assigning other design elements to that area. Similarly to the previous case, the routing and placement of the oscillators have been fixed to ensure that they are as identical as possible. Furthermore, within the oscillator matrix, another matrix of heaters has been implemented, designed to increase the temperature in a specific region of the FPGA. Each of these heaters has been implemented using a single LUT. Finally, multiple bias measurements were taken with the heaters activated and deactivated. With the heaters turned off, the reference matrix $\mathbf{A}_{\text{ref}}$ is obtained, which can be compared to the matrix measured with the heaters $\mathbf{A}(\mathbf{t})$.

One of the observations is that 3-stage DNOs are more sensitive to detecting these hotspots compared to oscillators with a higher number of stages. In Fig. 11b, the absolute difference in the bias matrix measured when the heaters are enabled and the bias matrix measured when the heaters are disabled is shown. The x and y axes represent the LUT coordinates on the FPGA. What is therefore represented is $\boldsymbol{\sigma}_{\mathbf{B(t)}} = |\mathbf{A}_{\text{ref}} - \mathbf{A}(\mathbf{t})|$ for the 3-stage DNO, a parameter referred to in the figure as "Bias Map Error (%)". From this plot, two aspects can be observed:

- First, as can be seen, there is a more significant difference in the oscillator biases in the area where the heaters were implemented, which is the area outlined with a white rectangle in the figure.
- Second, a slightly greater difference is observed in the upper part of the FPGA, which could be attributed to these sensors being closer to the edge of the *pblock* and, therefore, closer to other heat-generating elements.

In addition, based on the calibration previously performed with the selected 3-, 7-, and 9-stage DNOs, a thermal field estimation model has been developed to transform the map of percentage bias increase detected from the hotspot map into a map of temperature increment



(a) Power estimation.

Resource		Utilization
LUT	3-stages	1166 (2.19%)
	7-stages	1978 (3.71%)
	11-stages	2793 (5.25%)
LUTRAM		-
FF		4200 (3.95%)
IO		1 (0.80%)
BUFG		1 (3.13%)

(b) FPGA resources.

Fig. 12. (a) Power estimation by Vivado and (b) used resources of the FPGA for the matrix of generalized nonlinear oscillators.

distribution at each of the analyzed points. A first approximation has been carried out based on the correlation between the measured biases and the estimated thermal response, using the sensitivity curves obtained from the prior calibration. Results are shown in Fig. 11c.

Finally, Fig. 12 shows the estimated power consumption of the proposed design, as reported by Vivado for the Artix-7 FPGA. The figure also presents the corresponding resource utilization. The higher static power consumption is mainly due to the clock signal. Regarding logic power consumption, the largest contribution arises from the registers used to store the oscillator bias values. Comparing the 3-, 7-, and 11-stage proposals, all of them use the same number of flip-flops, while the difference lies in the number of LUTs, which depends on the oscillator length. This aspect also impacts power consumption, together with other factors related to oscillator placement and the implementation process performed by Vivado.

4. Conclusions

In this work, the potential of nonlinear oscillators for real-time temperature monitoring in FPGA is analyzed. Our proposal reduces the number of LUTs required to implement the oscillators compared to conventional RO-based sensors, while providing a larger temperature range, from −20 °C to 80 °C. Unlike RO-based sensors, which require multiple stages to obtain a useful frequency-temperature response, this proposal achieves this using only 3 stages. Furthermore, some oscillators can detect FPGA hotspots and remain robust against minor supply voltage variations. As a result, the proposed sensor presents a sensitivity of 0.013%/°C with 3 LUTs, 0.016%/°C with 7 LUTs, and 0.020%/°C with 11 LUTs. Future work will address the impact of supply voltage variations.

CRediT authorship contribution statement

Raúl Aparicio-Téllez: Writing – review & editing, Writing – original draft, Visualization, Software, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Miguel Garcia-Bosque:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Investigation, Funding acquisition, Conceptualization. **Guillermo Diez-Señorans:** Writing – review & editing, Validation, Supervision, Methodology, Investigation, Conceptualization. **Santiago Celma:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Investigation, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: All authors reports financial support was provided by Agencia Estatal de Investigacion (PDC2023-145838-I00, PID2023-150244OB-I00, PID2020-114110RA-I00). Raul Aparicio-Tellez reports was provided by Diputaciòn General de Aragòn (DGA) fellowship. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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