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Research paper

A modular soft core-based system for affordable acquisition and processing of electrophysiological recordings

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ABSTRACT

Flexible low-cost platforms for high-fidelity recording of biological signals are essential to advance health monitoring applications, yet they often rely on proprietary hardware that is resource-intensive and expensive. This study introduces a cost-effective FPGA platform that embeds an ARM Cortex M1 soft core processor with custom logic for signal acquisition, signal conditioning, artifact suppression, and data management, which is built around an Intan RHD2000 headstage. On-chip routines perform automatic offset calibration and gain calibration to ensure measurement fidelity. A graphical user interface, co-developed with biomedical end users, ensures compliance with data rate and timing constraints, enables live visualization, and streamlines parameter configuration. Bench validation using a multichannel test generator reproducing cardiac field potentials up to ±2 mV and bandwidths up to 5 kHz demonstrated stable timing, low crosstalk, and accurate amplitude reconstruction. Platform performance matches that of commercial multielectrode array systems, with minor deviations attributed to interconnection effects. Together, these results provide an accessible and extensible platform that preserves measurement fidelity while lowering the barrier to adoption in resource constrained laboratories.

1. Introduction

Advances in personalized medicine and mobile health have driven the development of novel sensing and measurement technologies for medical applications. Wearable sensors now allow for the continuous monitoring of physiological signals [1], while digital twin frameworks are emerging to simulate organ-level function *in silico* [2]. At the same time, organ-on-chip platforms that reproduce the behavior of cells [3] and tissues [4] in artificially generated microenvironments are gaining popularity [5–8]. Referring to the recording and analysis of electrical activity in different parts of the body, there is a wide range of electrophysiological signals of interest, such as electrocardiogram (ECG) [9], electroencephalogram (EEG) [10], and electromyogram (EMG) [11]. These signals cover amplitudes from microvolts to millivolts and bandwidths from a few hertz to several kilohertz. They are also prone to motion artifacts, electromagnetic interference (EMI), and stimulation transients. Building an acquisition platform for such a range demands configurable analog front-ends, precise timing control, robust artifact suppression, and quantitative uncertainty analysis to ensure metrological traceability and adaptability in experimental and clinical scenarios [12].

Another key feature of next-generation measurement platforms is true closed-loop control, in which the system reacts in real time to the signals it records. Applications such as pacemakers, brain stimulators, and robotic assistants require response times of the order of a few microseconds to a few hundred microseconds, with very low jitter and strictly enforced timing accuracy to ensure both safety and effectiveness [13,14]. Providing this level of performance in a single device requires not only precise signal capture and real-time filtering but also tightly integrated control logic and built-in routines that verify both timing and amplitude accuracy at every acquisition step [15]. FPGA architectures that incorporate a soft core processor have demonstrated embedded self-calibration and metrological validation without compromising real-time performance [16,17], underscoring their suitability for advanced measurement platforms.

Currently, within the scope of health monitoring, a variety of commercial systems for electrophysiological signal acquisition are available,

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Fig. 1. Overview of the complete system block diagram.

such as Multi Channel Systems (MCS), MED64, Axion, and MaxWell. These solutions incorporate advanced hardware that simplifies the experimental setup; however, their proprietary designs severely limit user modifications. As a result, flexibility is low, and any custom adaptations can only be shared with other users possessing identical systems, which hampers reproducibility. To address these issues, open-source toolkits like Open Ephys, RTXI, Piphys, Willow, and Intsy have emerged [18–22], offering free software frameworks for real-time acquisition and control. Nevertheless, most of these alternatives still depend on expensive headstages and external hardware and focus on high-throughput neuroscience applications with channel counts and sampling rates that exceed the needs of many other biomedical studies. In particular, reliance on powerful FPGA boards or expensive data acquisition (DAQ) cards can create barriers to adoption in more modest research settings. Consequently, there is still a need for compact and configurable solutions that combine real-time acquisition, automatic calibration, and open interfaces without relying on costly or proprietary hardware.

This study presents an alternative FPGA-based platform built around a soft core processor and custom peripherals to address these challenges with minimal hardware overhead. The main aim is therefore to provide a flexible and accessible system architecture that addresses current limitations in configurability, openness, and real time operation. Our system handles communication with Intan RHD2000 headstages, supports configurable digital filtering and intelligent artifact blanking, and can execute closed-loop control algorithms, all on a single board. Before each acquisition session, an automatic calibration routine adjusts sensor offsets and gains to ensure measurement fidelity and to avoid reported conversion artifacts that can distort the time series and spectral content [23]. During operation, simple calibration checks maintain accuracy over time, and a graphical interface alerts the user if the chosen settings risk data loss or violate timing constraints. In addition, its modular design allows for rapid integration of other sensors, such as those used to measure temperature, humidity, or pH probes, making it adaptable to a wide variety of biomedical monitoring applications. Ultimately, this platform provides a versatile resource for exploring a wide range of biomedical research scenarios.

This paper is structured as follows. Section 2 describes the proposed system, detailing the FPGA-based hardware design, signal management, and communication modules, including the user interface. Section 3 presents the experimental setup used for validation, including the test bench configuration and the custom interconnection board. Section 4 presents and discusses the experimental results in both the time and frequency domains. Finally, Section 5 summarizes the conclusions and outlines ongoing work involving biological recordings.

2. System structure

2.1. System overview

This paper describes an electrophysiological signal acquisition system implemented on an FPGA, with an embedded ARM Cortex-M1 soft core processor as the main controller. Embedding the soft core in the FPGA enables on-chip intelligent sensing, including automatic offset and gain calibration, as well as artifact detection, while preserving the deterministic timing required for medical-grade measurements. This architecture is easily configurable to meet the specific requirements of each application. In practice, the design supports neural or cardiac recordings by adjusting sampling parameters and digital filter settings, without requiring any modification to the underlying hardware. Fig. 1 shows the main functional blocks of the implemented platform.

The “Signal acquisition” block includes specific devices for recording electrophysiological signals, such as electrodes for recording ECGs or multielectrode arrays (MEA) for recording local field potentials (LFPs) [24,25]. Depending on the specific signal, the most suitable recording device needs to be selected.

Next, the “Signal conditioning” block encapsulates a set of filters and amplifiers designed to improve and enhance the quality of the recorded signals. This conditioning process is essential to mitigate any potential interference, ensure that the signals obtained are adequate for the subsequent stages of the system, and maximize the useful information derived from them. An analog-to-digital converter is also included. All the actions performed in this block condition the signal for further processing in the FPGA. The RHD2000 integrated circuit family [26] was selected as an optimal option for this purpose, as it incorporates low-noise amplifiers with programmable bandwidths and a multiplexed analog-to-digital converter (ADC) among all input channels, which makes it suitable for a wide range of biopotential monitoring applications [27]. Configurable filter settings facilitate intelligent artifact blanking in hardware while preserving real-time performance. The headstage RHD2132 from Intan Technologies, which incorporates the chip mentioned, was used in the proposed system.

The “Processing unit” block is fully implemented in the FPGA and plays an important role in the processing of acquired electrophysiological signals. In the FPGA, a Cortex-M1 soft core processor-based design is configured to handle communication with the different peripherals implemented on the board itself, acting as a link to the input/output ports. The most relevant IP block of the system was developed from scratch and is responsible for managing the communication with the previously mentioned headstage. This peripheral is designed to reduce the computational load on the processor, allowing it to allocate resources to other tasks of interest. The inclusion of additional peripherals in the proposed platform can expand the final platform for a variety of purposes, such as managing system clocks, enabling General Purpose Input/Output (GPIO) ports to connect signals of interest, such as a synchronization trigger, and facilitating different types of communication protocols with the computer or memory.

An FPGA-based solution was selected to integrate a dedicated peripheral for the direct management of the RHD2000 family headstages. This peripheral offloads computationally intensive tasks from the processor, resulting in time savings. Specifically: (i) it establishes a modified Serial Peripheral Interface (SPI) protocol, which is mandatory for communicating with this family of Intan devices; (ii) it initializes the headstage device registers; (iii) it automates data management by using a FIFO buffer to store data throughout each user-defined cycle and a serial interface to communicate with an external system, sending data at the end of each cycle; and (iv) it includes intelligent blanking process management to reduce stimulation-related artifacts commonly found in such systems.

For data storage and user interaction, the system offers two operating modes. In streaming mode, digitized packets are transmitted over USB with embedded headers for integrity verification. In buffering mode, samples are temporarily stored in on-board DDR3L memory for later retrieval. A graphical user interface (GUI) enables users to select the sampling frequency (F_s), channel count, and storage mode; it automatically verifies these settings against data-rate and buffer capacity limits and alerts the user to potential overflows. During acquisition, built-in calibration routines adjust offset and gain to maintain signal fidelity. The interface also provides real-time data visualization, supports the adjustment of filter settings, and allows for the extraction of metrics such as peak amplitude. All user

actions are validated against the system parameters to prevent invalid configurations.

2.2. "Processing Unit": design and implementation

Electrophysiological recording of weak signals increasingly relies on high-throughput headstage chips, such as the RHD2000 chip family. Communicating with these devices requires long, ordered command sequences that can overload a general-purpose microprocessor, especially at high channel counts and sample rates. To address this, we created a custom FPGA peripheral that handles all RHD2000 interactions directly in hardware. It implements the modified SPI protocol, automatically initializes the device registers, buffers data in a FIFO, and applies intelligent blanking to suppress stimulation artifacts. By moving these time-critical tasks into the FPGA logic, the soft core is free to run higher-level routines (closed-loop control, calibration checks, and the user interface) without compromising real-time performance or overall system flexibility.

2.2.1. FPGA: soft core architecture

A key design decision concerns the processor used to manage peripherals. Two options exist: hard cores (fixed in silicon) typically achieve higher clock speeds but cannot be modified once fabricated [28], and soft cores (synthesized from the programmable logic) that can be adapted to the specific requirements of each project by extending instructions or bus interfaces as the design evolves [29]. This flexibility is valuable in electrophysiology, where bandwidth and control differ across applications; for example, in neural and cardiac recordings.

In this work, a Cortex-M1 soft core processor is instantiated on an Artix-7 FPGA (Xilinx) to handle peripheral communication and control. This configuration allows the use of the soft core processing capabilities while preserving the reconfigurability of the FPGA to implement additional functions as needed. This architecture efficiently allocates FPGA resources, including memories, logic blocks, and interfaces, according to the requirements of the project, thereby maximizing processor performance. The compact footprint of the Cortex-M1 enables efficient utilization of FPGA area and power resources. In addition, the ARM development ecosystem streamlines the development and integration of the processor, accelerating the design process.

The soft core manages the configuration and control of all on-board peripherals and coordinates the buses required to interface with the signal acquisition front end and the storage memory. In the implementation presented here, the system runs at 96 MHz, derived from the 100 MHz internal oscillator through the mixed-mode clock manager (MMCM). This frequency aligns the SPI data rate with the maximum speed supported by the RHD2132 headstage, ensuring stable data transmission and compliance with timing requirements during the acquisition process.

2.2.2. RHD peripheral: design and implementation details

The headstage device is responsible for amplifying and conditioning the bioelectrical signals prior to digitization and processing. Therefore, developing an effective peripheral to manage the communication and control functions of the headstage is essential for the overall system performance. This section presents the key aspects of the peripheral's design and functionality, as well as the specific challenges in its implementation. An overview of the modules that make up the peripheral can be seen in Fig. 2.

The IP manager of Vivado (Xilinx) was used to implement the peripheral that controls the headstage. Using this tool, an IP block with the AXI4-Lite interface and a bank of 64 registers was generated. This configuration provides an efficient and easy-to-use interface to communicate with and control the headstage from the microprocessor.

The AXI4-Lite interface was used for communication with the microprocessor, enabling register access and configuration of the peripheral from the control software. In addition, AXI4-Stream interfaces were used to facilitate communication between the internal blocks of the peripheral. These interfaces ensure synchronized and continuous data flow across the peripheral, minimizing latency and improving overall communication efficiency.

Once the base peripheral was generated, the SPI block was designed and integrated within it. The timing constraints specified by the manufacturer in the headstage datasheet were defined in the protocol to guarantee proper synchronization and reliable data exchange (Fig. 3).

The overview of the peripheral block diagram (Fig. 2) can be divided into several functional parts:

- The central section corresponds to the 64 internal registers of the peripheral, which are detailed below.
- On both sides, input/output interface blocks for AXI and SPI communication are incorporated. The buses for data transfer are highlighted in orange.
- The "processes" block controls the execution of the different routines and communicates directly with the register bank. In this section, a dashed frame indicates where additional functionalities could be incorporated.
- The "control" block implements a finite state machine (FSM) that manages the execution flow and interacts directly with the "status" block, which enables external monitoring of the peripheral state.
- "Tx Data" block incorporates a Universal Asynchronous Receiver-Transmitter (UART) transmitter interface and a FIFO of 65,536 16-bit words. An interrupt is generated in the case of a transmission overrun.
- Finally, several output ports connect the peripheral to external components: in blue, two interrupt lines to indicate the end of a conversion (I_PERI) or a full FIFO condition (I_TX_OVERRUN); in green, the UART data output line; and in purple, the OUT_BLNK output signal that manages the blanking operation during the CH Reader process.

Internal registers. The peripheral operates through a bank of 64 internal registers, grouped by functionality to manage configuration, process control, and data transmission. The description below follows the same top to bottom order shown in Fig. 2. The configuration registers define the parameters of the headstage, including initialization and communication settings. Additional registers handle direct commands, status monitoring, and channel selection, while dedicated registers store the results of the channel conversion process.

Control registers specify timing and blanking intervals, as well as parameters for UART data transmission. The register layout mirrors the memory structure of the RHD2000 device, ensuring seamless interoperability between the FPGA peripheral and the headstage. Read-only copies of the main RHD registers are maintained within the peripheral to preserve data consistency and simplify synchronization between hardware and software layers.

Input/Output interfaces. The peripheral has two main interfaces: one for communication with the microcontroller (AXI-4 Lite) and another for communication with the headstage device (SPI). As mentioned above, both are highlighted in orange in Fig. 2.

The "AXI Interface" block implements an AXI4-Lite slave interface for register access. The internal registers of the peripheral are designed to match the layout of the RHD2000 memory map and store a copy of their contents, facilitating interoperability and integration with other system components. This configuration allows one to easily control and know the status of the chip from the microcontroller simply by reading the register of interest.

The "SPI interface" block acts as the SPI master for communication with the RHD integrated circuit. Before its integration into the peripheral, independent testing of the SPI interface was carried out to adjust timing parameters and ensure proper operation. This interface enables high-speed and reliable data transmission between the peripheral and the RHD, ensuring a robust and stable connection during electrophysiological signal acquisition.

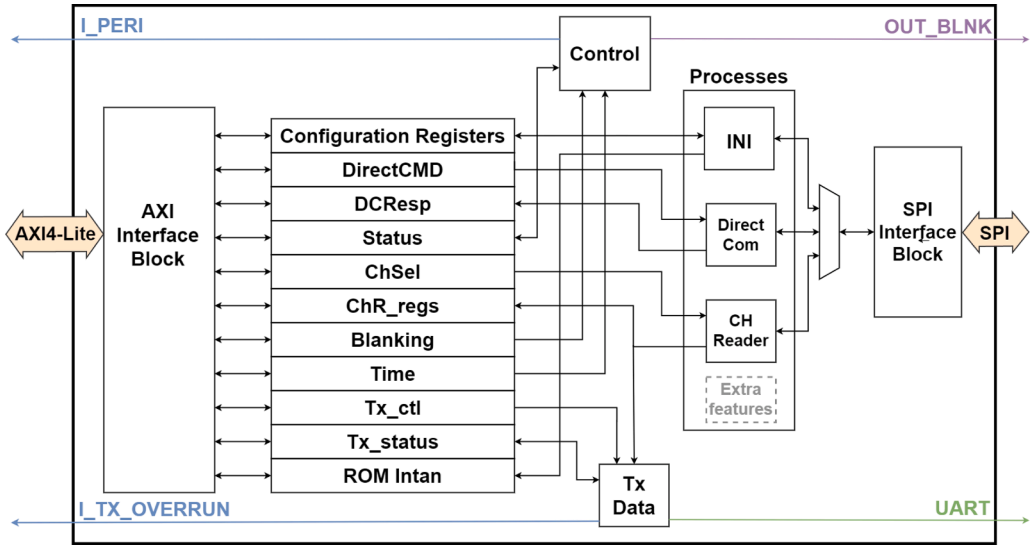

Fig. 2. Peripheral block diagram, showing its main blocks designed for the different subprocesses.

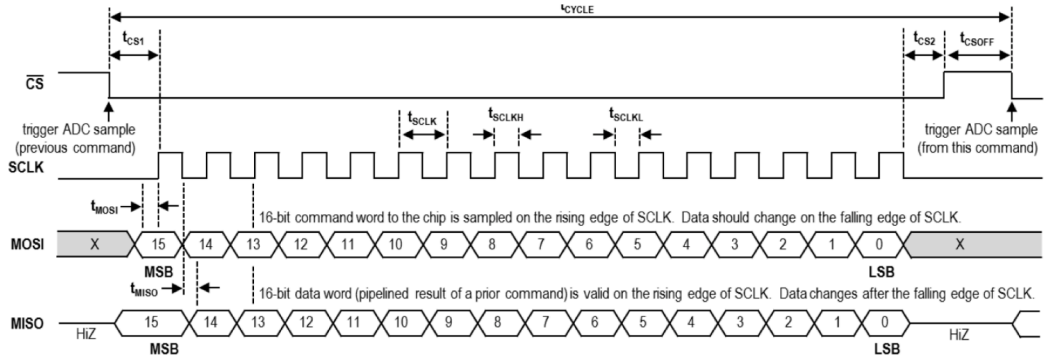

Fig. 3. Timing diagram for the SPI interface used by the RHD family chips (extracted from [26]).

Control module. The "Control" block is responsible for managing the peripheral and is activated by setting specific control bits in the status register. This block coordinates interrupt generation, process control, and the channel conversion loop, ensuring synchronized and efficient peripheral operation throughout the acquisition process.

Processes module. This block is one of the most important elements of the peripheral, containing the different processes executed to perform its functions. It is composed of three sub-blocks with different tasks: (i) **INI**, responsible for the initialization process of the headstage, ensuring it is properly configured for operation by reading the information stored in the configuration registers, following the initialization process specified in the datasheet [26] ; (ii) **Direct Com** handles the transmission of the commands stored in the DirectCMD register through the SPI interface, stores the responses in the DCResp, and generates an interrupt associated with the end of execution; and (iii) **CH Reader**, which is responsible for the conversion process of the selected channels.

The latter process, CH Reader, implements the main function of the peripheral: the electrophysiological signal acquisition loop. In this operating mode, the peripheral performs periodic captures of a set of channels selected by the user via the ChSel register, at a sampling frequency also defined by the user. The data from these acquisitions are stored in the respective registers, which can be read by the microprocessor.

Summary of main functionalities. The main functionalities of the peripheral can be summarized as follows: (i) the initialization process can be performed independently of the configuration stored in the registers via the AXI4-Lite interface. In addition, a calibration and a register copy operation are carried out; (ii) it features a configurable selected channel conversion process, with the ability to perform it periodically with an adjustable period; (iii) it generates two interrupts to notify the reception of responses and the end of the conversion loop; (iv) the register layout mirrors the memory structure of the RHD; (v) it is preconfigured to operate with a clock frequency of 96 MHz, which results in a 24 MHz serial interface and a maximum period channel conversion of 681.6 μs.

2.3. Data management: storage and transmission protocols

During the acquisition period, a large amount of data is converted and stored, which must then be sent to the computer for storage and visualization. Communication with the computer is implemented using two separate UART interfaces, distinguishing between command control and data transmission. Both interfaces use FTDI controllers to carry out data transfer via USB 2.0.

The data transmission interface, located within the Tx Data block, supports unidirectional transmission from the FPGA to the computer. The transmission rate is configurable, set by default to 1 Mbit/s, and can reach up to 12 Mbit/s, limited by the FTDI chip. This interface is managed by the peripheral's Tx_ctl and Tx_status registers. Its implementation includes two control registers and a 16-bit FIFO buffer with storage for 65,536 words, where the data to be transmitted is queued.

Data transmission interface. During the acquisition loop, the data captured during the Tsave periods are stored in the peripheral registers and, when enabled, are simultaneously sent to this interface for transmission. Data is transmitted in packets, with the samples from all the

Table 1
Summary of the commands protocol implemented for communication with the platform.

Name	Command	Modifier	Arguments
Test	test	.	.
Initialization	ini	.	.
		conf	-Rxx < reg value>
Direct command	cmd	read	<addr>
		write	<addr> <data>
		convert	< channel no.>
		calibrate	.
		clear	.
Capture loop	loop	config	-ch <channel sel. (hex)> -blnk <blanking time> -fs <sample freq> -nest <stim no.> -Tc <stim. save period>
		start	.

channels corresponding to the same instant. Each packet is preceded by a header that simplifies data handling once received by the computer, allowing for the detection of byte or whole packet losses. Given the 16-bit resolution of the headstage, each sample is transmitted as two 8-bit words in big-endian format.

The number of samples that the system can generate is limited by the transmission rate of the interface (R_{Tx}), which represents the main bottleneck for the system. The user must balance the capture time (T_{save}), stimulation frequency (F_{est}), and the number of channels to capture (N_{Ch}). This relationship is expressed by the inequality in Eq. (1), which compares the number of samples transmitted during stimulation with the number of samples generated per stimulation:

$$\frac{R_{Tx}}{20 \cdot F_{est}} \geq F_s \cdot (N_{ch} + 1) \cdot T_{save} \tag{1}$$

Properly sizing the communication parameters prevents residual samples in the FIFO at the end of the stimulation, thereby avoiding memory overflow and data loss.

Control interface. The control interface is directly managed by the microprocessor using the Xilinx UART-Lite IP. This interface transmits the commands and their responses at a standard rate of 115,200 bit/s, as it does not require a high data throughput. A set of commands sent from the computer has been defined to simplify configuration and provide access to all the platform functionalities.

2.4. MEA-CTL: user interface

A simple command protocol was defined to control the platform from an external device. Four main commands (Table 1) cover testing, headstage initialization, direct register access, and the capture loop, each with simple modifiers that keep the syntax compact. Sessions with biologists who routinely perform MEA recordings showed a clear preference for a graphical interface instead of a command line. Consequently, a dedicated GUI was developed in collaboration with these end users to encapsulate every command and automatically verify all configurable parameters.

The *test* command verifies the communication by using a known text string that the platform returns to this command, validating proper operation. All other commands interact directly with the headstage, either by reconfiguring its registers (through the *ini* command) or by sending direct orders. The acquisition loop is managed by two commands: *config*, which sets capture parameters, and *start*, which initiates the process. When configuring the parameters for the *config* command, it is crucial to consider the inequality in Eq. (1) to prevent data overflow.

This command-line interface enables direct verification and low-level interaction with the system; however, it requires knowledge of command syntax and argument formatting. Commands are transmitted as character strings terminated by a carriage return, and platform responses end with a newline character. To simplify usage and reduce the barrier for users unfamiliar with command-line operations, a graphical user interface (GUI) was developed to configure and execute commands interactively (Fig. 4).

The GUI is divided into three panels: (i) the connections panel manages communication with the two platform interfaces, both for the control connection and for the one that transmits data; (ii) the command control panel displays terminal activity and allows for manual command entry; and (iii) the command panel, which provides access to all configuration options. Commands can be configured intuitively, with real-time visualization of acquired signals and data export capabilities.

The DirectCMD and Ini windows enable the configuration of the corresponding platform commands. The GUI restricts user input to valid parameter ranges and automatically applies default values when fields are left empty, ensuring safer operation than direct command-line use.

The first two windows (DirectCMD, Ini) enable the configuration of the corresponding platform commands. The GUI restricts user input to valid parameter ranges and automatically applies default values when fields are left empty, ensuring safer operation than direct command line use.

The first configures the acquisition loop, allowing for parameter adjustments and automated verification against transmission constraints. The application prevents loop initiation until all configuration checks are satisfied. While the loop is active, messages are displayed for each new stimulus, and an indicator signals the ongoing data acquisition. The Loop Plot window provides a real-time preview of the recorded data.

The main functions of the platform are controlled in the following two windows: Ch Loop and Loop Plot. The first configures the acquisition loop, allowing parameter adjustment and automated verification against transmission constraints. The application prevents the loop from starting until all configuration checks are satisfied. While the loop is active, messages are displayed for each new stimulus, and an indicator is activated during ongoing data acquisition. The Loop Plot window provides a preview of the recorded data as it is stored.

Given that the data is transmitted in blocks preceded by a header, and each sample is composed of two 8-bit words, the GUI interprets and organizes the incoming stream accordingly. Packets are read in groups containing the number of channels plus the header. When the header is detected at the expected position, the samples are correctly assigned to each channel. Otherwise, transmission errors are detected, and the remaining samples are padded.

The acquired data are stored in a Matlab struct variable saved as binary *.mat* files. As shown in Fig. 5, the top level contains a field with general information about the capture, such as the converter resolution and the program information. It also stores a field for each capture performed in the same execution of the application, called “Records”. The general information field is common to all the captures in the file.

Each “Record” contains metadata about the acquisition, including channel identifiers and the parameters used, which are stored in a structure. Finally, the main data fields are: RawData, which contains the acquired samples; ChannelsTimestamp, which stores the time axis; and Triggers, which stores the temporal value and position of the trigger events.

3. Experimental validation

3.1. Experimental setup

Validating an acquisition platform with living tissue often faces practical constraints, such as short sample viability, limited availability, and

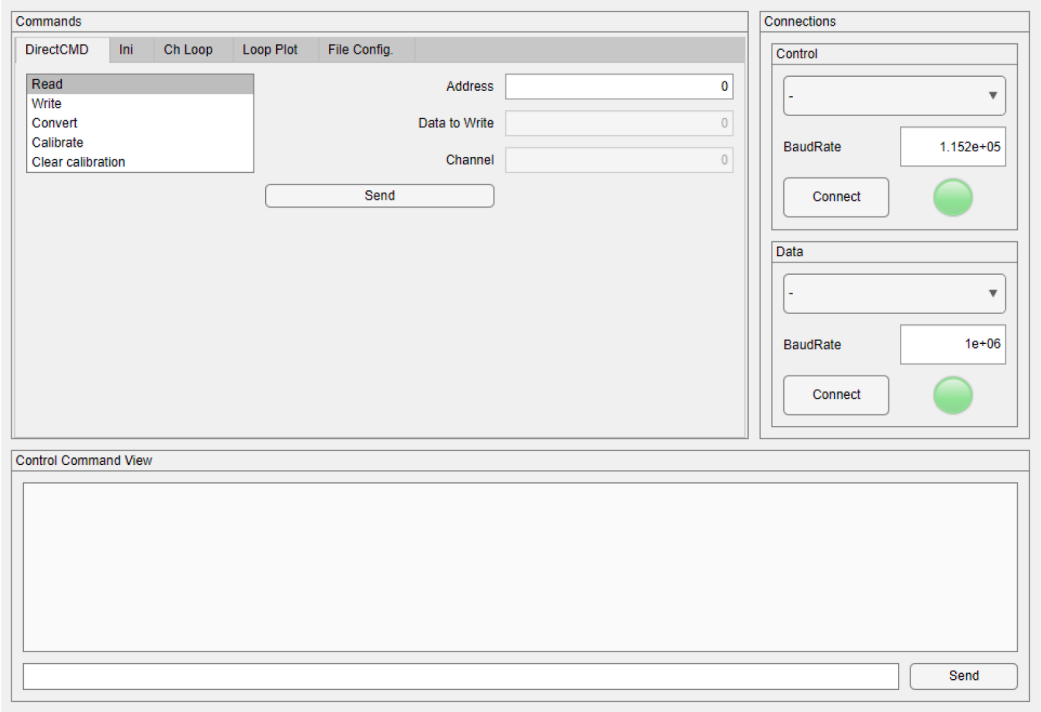

Fig. 4. Home screen of the control application. The interface is split into three panels: top left, commands window; top right, connections window; bottom, command control window.

variability between preparations. To establish baseline performance under controlled and repeatable conditions, the system was first evaluated using a synthetic testbench capable of reproducing the amplitude and frequency ranges typical of electrophysiological recordings, including action potentials and field potentials.

Fig. 6 shows the complete experimental setup, which consists of a low-amplitude signal generator, a custom PCB interface, and the FPGA board. Commercial MEA systems are routinely verified with the same generator prior to biological experiments; in fact, the Multi Channel Systems documentation recommends the 60MEA-SG to verify proper system operation. Its output levels cover the ranges reported in the literature for ventricular field potentials and other cellular signals [25,30].

3.1.1. Low amplitude stimulator - signal generation

A low-voltage signal generator was used to validate the acquisition platform across the full range of its intended applications. The 60MEA-SG unit provides 60 independent channels and can replay predefined waveforms, such as ECG, action potentials, and field potentials, at two selectable amplitude levels.

Among the different test patterns available, signals with cardiac morphology were selected to test the system, as they represent a primary application of the platform. The generator produced ventricular LFPs traces with peak values of approximately ± 3.1 mV on the highest amplitude channels and approximately ± 1.7 mV on the others, repeating at 1 Hz. Additional tests used ECG and single cell action potential patterns to verify correct operation with lower-amplitude and wider-bandwidth signals. A trigger output from the generator was connected to a general-purpose input on the FPGA, enabling precise time-stamping and alignment of each stimulus with the recorded data.

3.1.2. Interface system-stimulator

Working with low-amplitude signals presents major challenges related to noise, which may arise from poor connections, long cables, or other sources, potentially hiding the signal and rendering it unrecoverable. To minimize this, a custom printed circuit board (PCB) was designed to connect the signal generator to the headstage, where signal conversion occurs (Fig. 7).

Thirty-two pads from the generator were selected to link to the 32 inputs of the RHD2000 headstage, following a modified checkerboard pattern to maximize the coverage of the MEA surface. The PCB is a four-layer design, with the outer layers acting as ground planes and the inner layers used for signal routing. This structure reduces the impact of external noise and crosstalk between channels. Traces were routed to maximize the distance between adjacent lines, with the remaining inner areas filled with ground copper planes.

Spring-loaded pins ensure a stable connection with the generator pads, while a 3D-printed support (shown in black in Fig. 6) provides additional mechanical stability and vibration isolation.

3.2. Validation tests

The validation of the acquisition platform was performed using the synthetic testbench described in the previous section, with signals representative of cardiac field potential activity. The performance of the system was benchmarked against a commercial MEA acquisition unit from MCS, which is widely used as a reference in electrophysiological measurements.

The tests were designed to evaluate the signal acquisition performance of the platform under controlled conditions, focusing on its frequency response and its ability to accurately capture signals. The minimum sampling frequency required to faithfully record the LFPs was determined according to the methodology reported by Halbach et al. [31].

For this purpose, signals were acquired at 1, 5, and 10 kHz per channel using 16 active channels. Each acquisition included recordings from the FPGA-based platform and the MCS reference system, allowing for the comparison of the captured waveforms under the same experimental conditions.

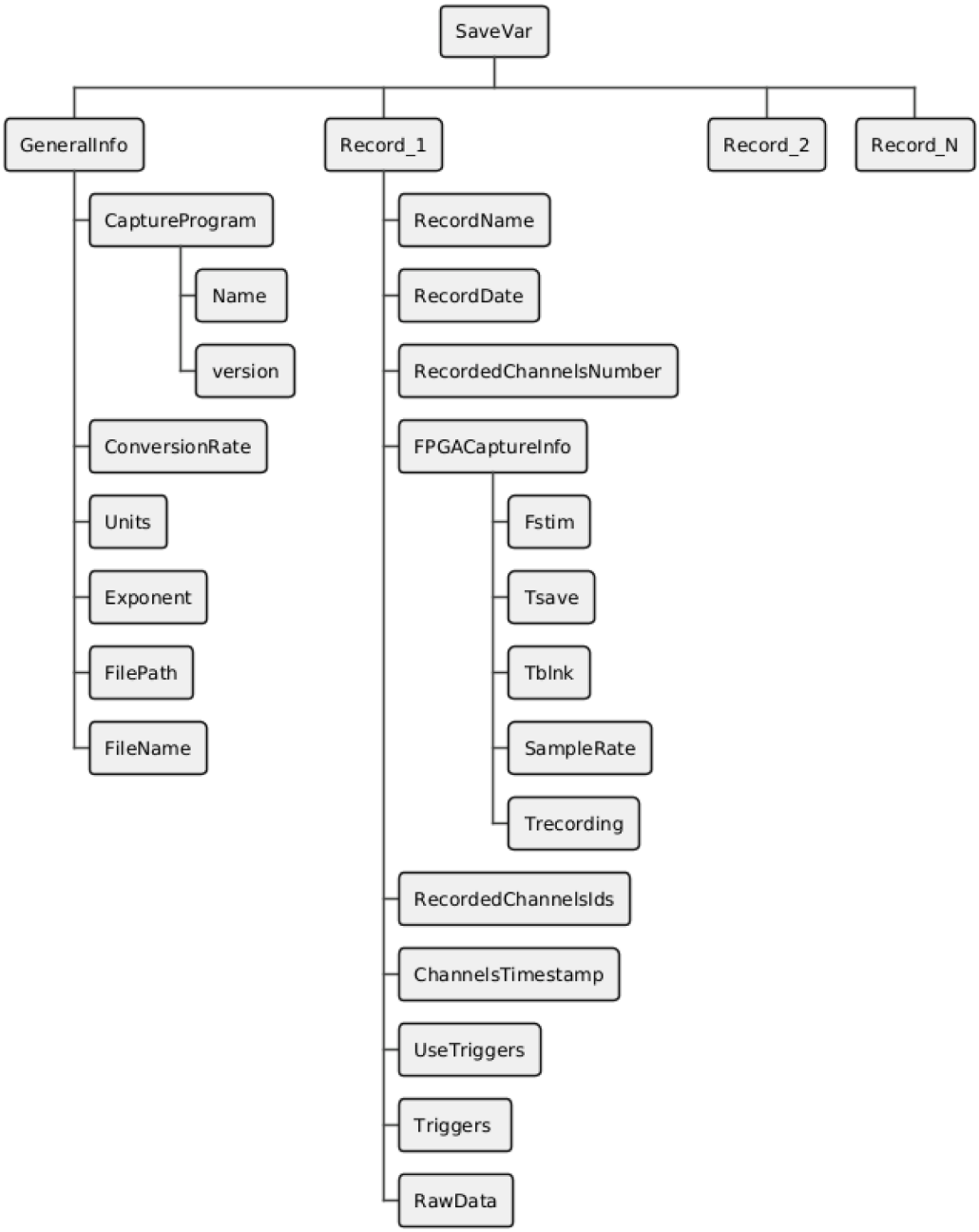

Fig. 5. Control application home screen. Split into three blocks: top left, commands window; top right, connections window; bottom, command control window.

4. Results and discussion

This section presents the results obtained from the validation tests described above. The signals captured by the FPGA-based platform were compared with those recorded using the MCS reference system.

Fig. 8 shows representative traces of ventricular field potential recordings acquired at different sampling frequencies. At 1 kHz per channel, the recorded signal exhibits clear distortion and insufficient temporal resolution to reconstruct the waveform, whereas acquisitions at 5 and 10 kHz reproduce the reference signal precisely, preserving both amplitude and morphology.

To shed light on the observed limitation, a frequency study was carried out (Fig. 9). The signal spectrum shows relevant content up to approximately 1.4 kHz, which implies that sampling frequencies above 2.8 kHz are required to meet the Nyquist criteria: $F_s > 2 \cdot f_{\max}$, with $f_{\max}$ defined as the highest frequency component of the signal to be acquired.

This confirms that the system can accurately acquire the signals of interest when an appropriate sampling rate is selected. These results also highlight a practical tradeoff between waveform fidelity and data throughput. For the signals evaluated here, sampling frequencies of 5 to 10 kHz provide a robust margin to preserve both morphology and amplitude, based on the results obtained from different sampling frequencies.

A comparison between the signals captured with the platform and those recorded with the MCS equipment reveals a constant DC offset in the platform data, which is present across all channels but varies in magnitude. The representation of a randomly selected channel at $F_s = 10$ kHz is shown in Fig. 10. In the presented system, the removal of the DC component was implemented in the control interface by subtracting the mean value of each channel. This approach was preferred for its simplicity compared to alternative high-pass filtering methods with cutoff frequencies around 0.5 Hz.

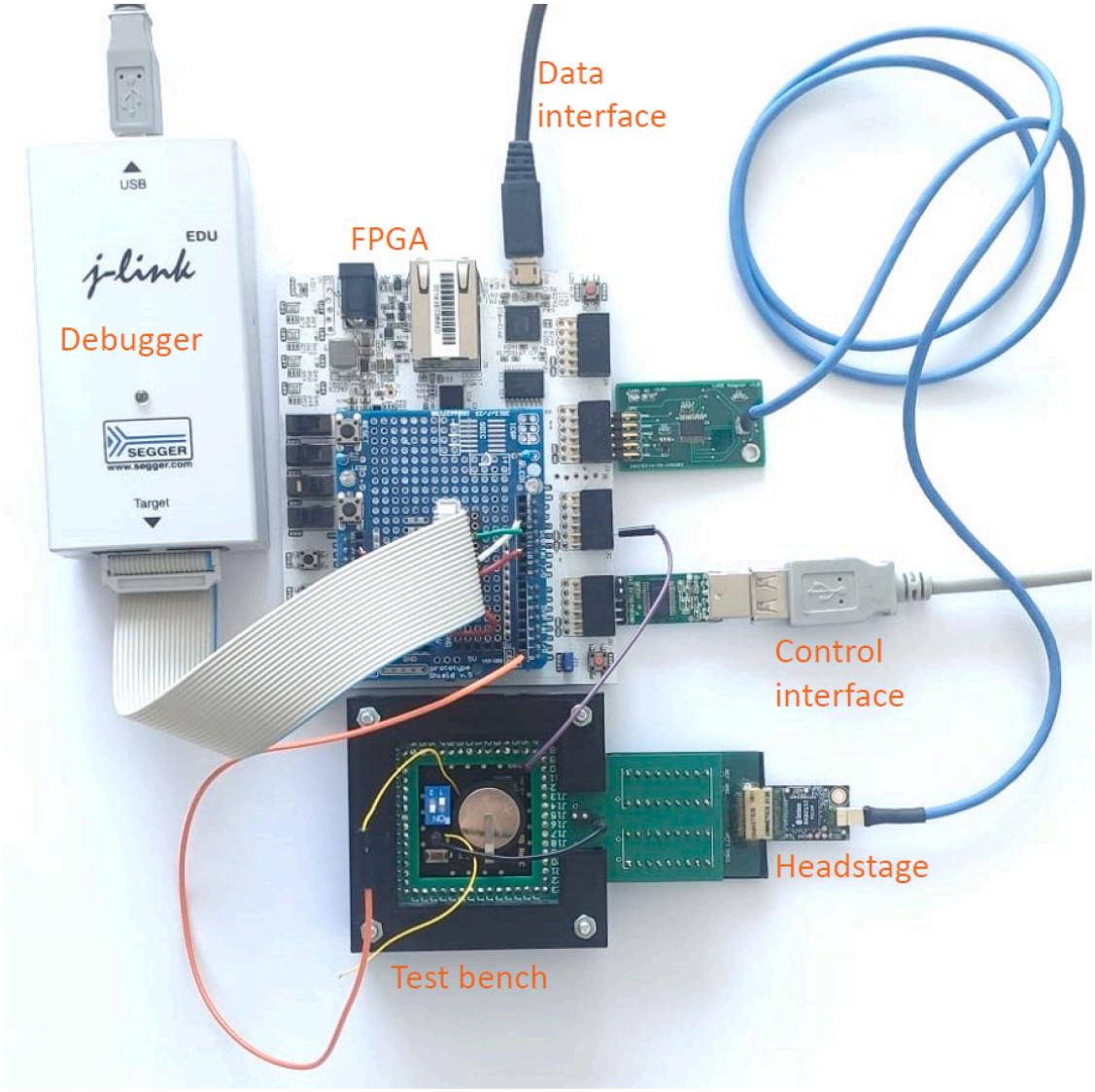

Fig. 6. Experimental setup used for system validation. The different components are labeled. The two communication interfaces that the system uses (control and the data) are shown.

This approach is appropriate for the comparative validation performed here, where relative morphology and amplitude are the main observables. Applications that require baseline accurate measurements can incorporate alternative offset handling strategies within the same architecture.

After offset correction, the platform and MCS signals were re-evaluated. Differences were observed during the depolarization phase, where the signal recorded by the FPGA-based system shows a slightly reduced amplitude compared to the reference. However, during the re-polarization phase, only minor variations were observed. The discrepancies in the rapidly changing depolarization phase may be attributed to parasitic effects in the PCB connecting the generator and the headstage. This observation emphasizes that part of the discrepancy can arise from the interconnection path rather than the acquisition core itself, particularly during fast transitions. It also motivates careful interconnection design when maximum fidelity of steep waveform components is required.

Validation using a multichannel signal generator across amplitudes ranging up to ± 2 mV and bandwidths up to 5 kHz demonstrated stable timing, low interchannel crosstalk, and accurate amplitude reconstruction, matching the behavior of a commercial MEA system while using significantly fewer hardware resources.

From an architectural perspective, the results support the partitioning of time critical acquisition tasks into dedicated FPGA logic, while higher level configuration and supervisory routines remain on the embedded soft core. This approach preserves deterministic timing during acquisition and keeps the platform adaptable for future processing and control extensions.

These results confirm that the proposed architecture is suitable for electrophysiological recordings under the signal conditions typically encountered in biological experiments. Furthermore, the modular structure of the FPGA and its soft core processor enables straightforward integration of additional functions, such as onboard filtering, closed loop stimulation, or auxiliary sensors, with minor hardware modifications.

Overall, the platform provides a cost-effective and flexible acquisition solution that maintains measurement precision comparable to commercial systems, while remaining accessible to laboratories with limited technical or financial resources.

While the validation presented in this work is based on a synthetic testbench, this approach was selected to ensure repeatable and

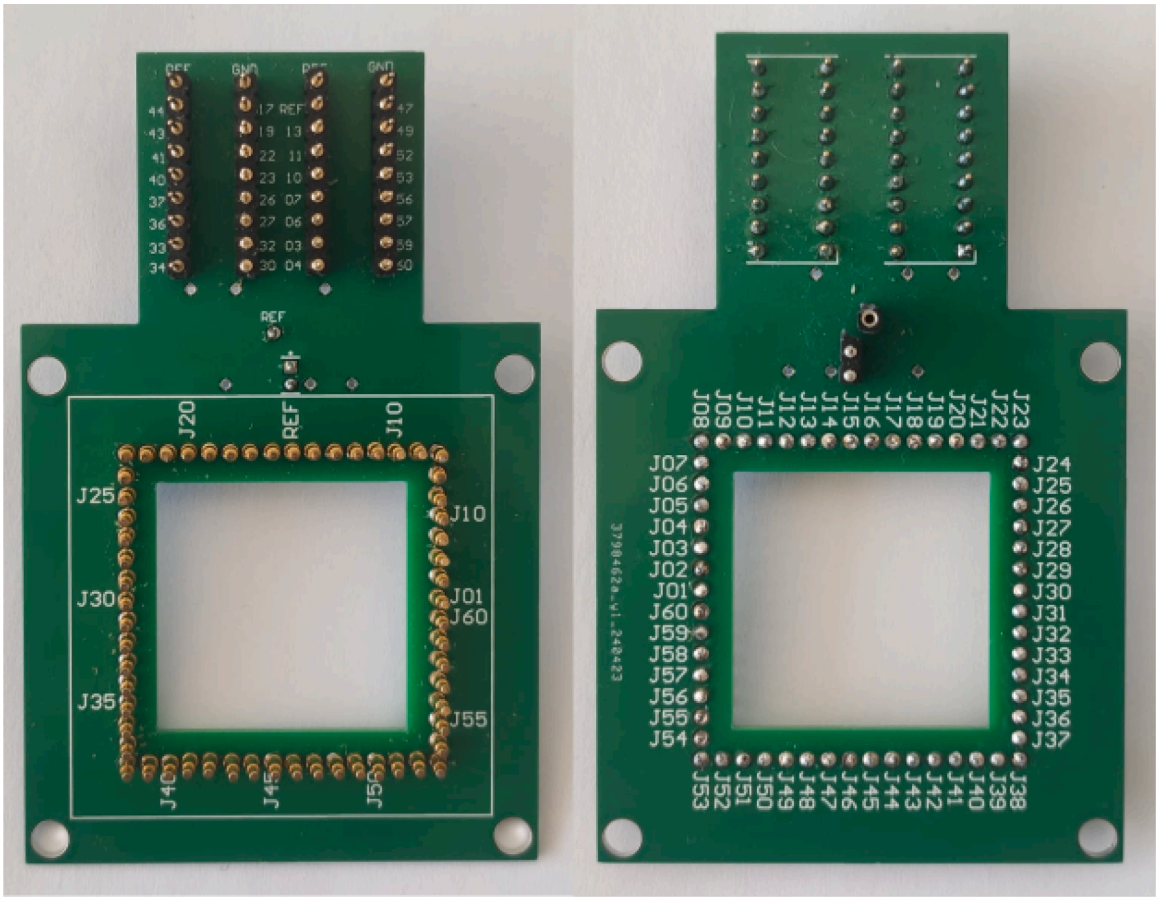

Fig. 7. Custom PCB designed for the interconnection between the generator and the headstage. At the top, four rows of standard male connectors are placed to establish the connection with the headstage, while at the bottom, spring pins are incorporated to ensure optimal contact with the pads available on the generator board.

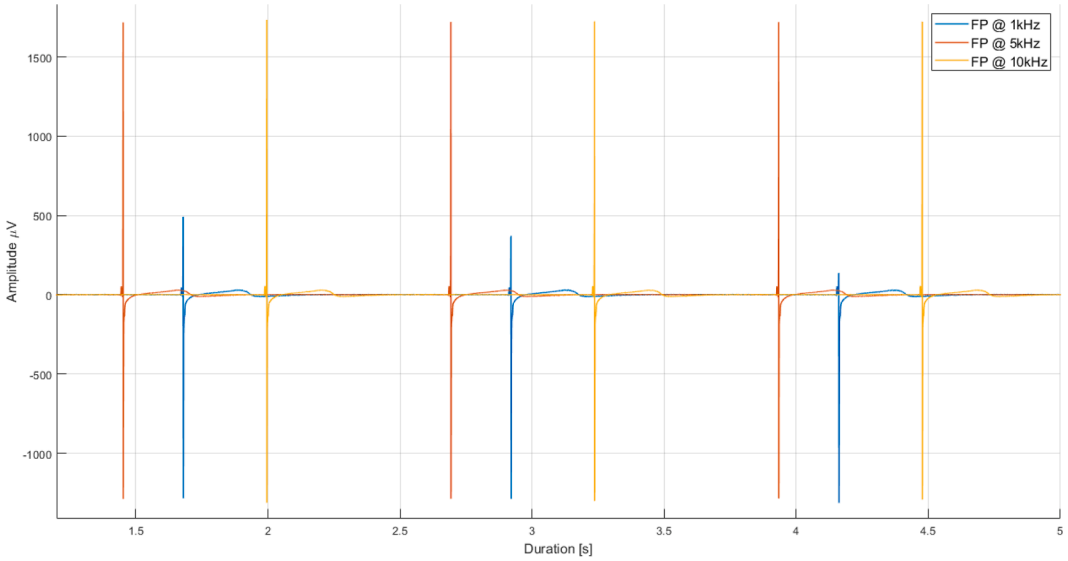

Fig. 8. Time representation of the FP signal for different sampling frequencies: 1, 5, and 10 kHz.

controlled conditions. Ongoing work is focused on extending the validation of the proposed platform to real biological preparations, where its modular architecture is expected to be particularly beneficial.

Regarding affordability, the cost discussion focuses on the core acquisition hardware (FPGA board, headstage, and interface electronics), excluding consumables such as electrode arrays, whose cost depends on the specific application and is common to both systems. Under these assumptions, the core hardware cost of the proposed platform is estimated to be approximately a factor of five lower than that of commercial MEA systems, whose pricing is quotation based and varies with configuration.

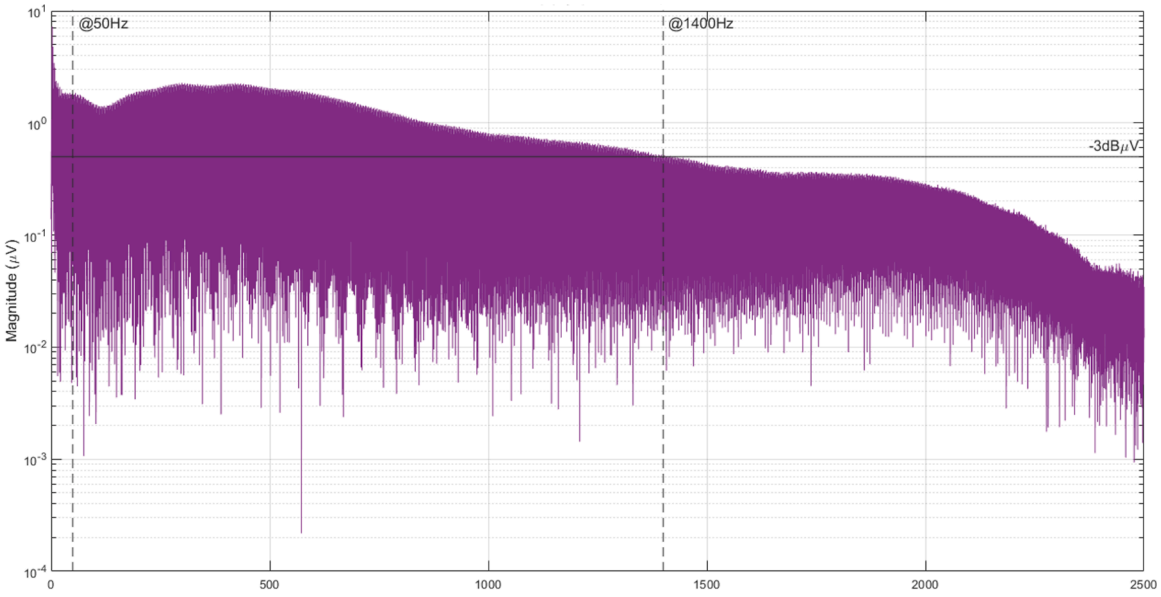

Fig. 9. Frequency representation of an FP signal acquired with the proposed platform.

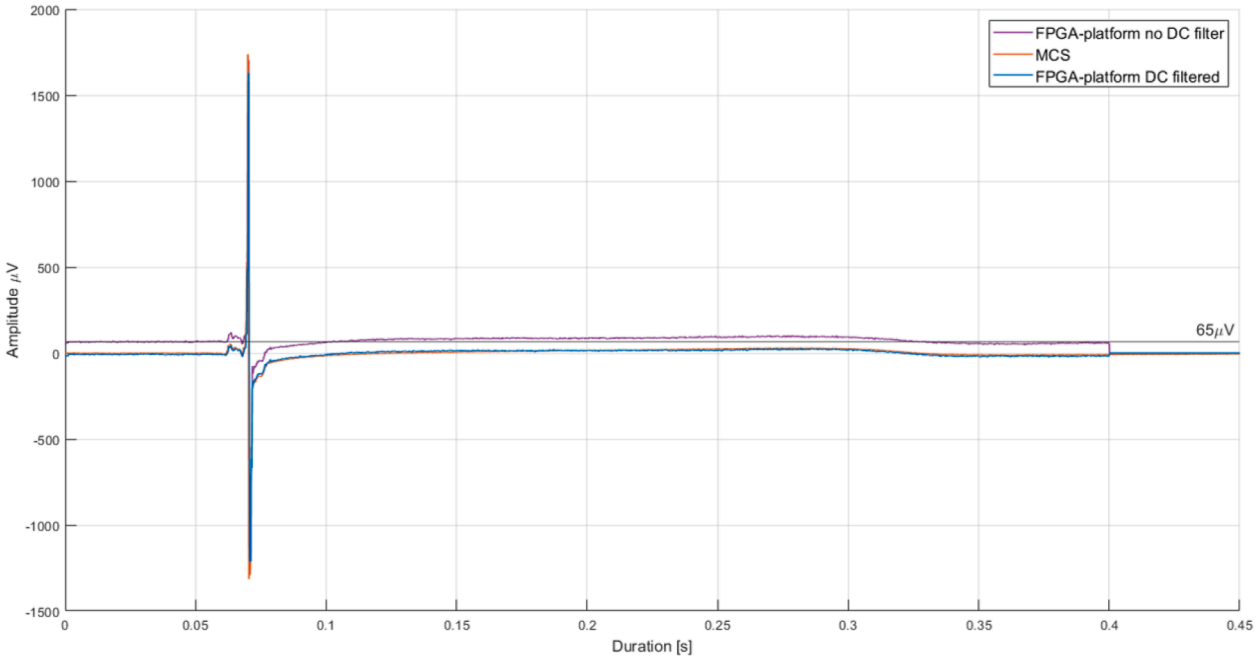

Fig. 10. Temporal comparison of an event captured by the MCS equipment and the same event captured (F_s = 10 kHz) by the platform before and after removing the continuous component.

5. Conclusions

A reconfigurable FPGA platform for electrophysiological measurements has been presented, combining a soft core Cortex M1 processor with dedicated logic for acquisition, conditioning, and data management around an Intan RHD2000 headstage. The resulting system provides a compact and affordable alternative to commercial multielectrode array acquisition units while preserving configurability and openness.

Blanking functionality was verified under laboratory conditions by injecting calibrated stimulation artifacts. The hardware module adjusted its suppression window and effectively removed the perturbations, confirming correct operation in a controlled environment. The system also integrates automatic initialization routines and real-time identification of key signal parameters to streamline calibration and maintain measurement fidelity.

Experimental validation with a multichannel test generator delivering cardiac-like field potentials up to ±2 mV and 5 kHz bandwidth showed that, for appropriately chosen sampling frequencies, the platform reproduces waveform morphology and amplitude in close agreement with a commercial MCS system, while maintaining stable timing, low interchannel crosstalk, and consistent DC offset compensation.

The soft core architecture enables the rapid integration of additional peripherals or control algorithms, opening a path toward onboard closed-loop stimulation, adaptive filtering, and the integration of auxiliary sensors such as temperature and pH probes for multimodal monitoring and organ-on-chip applications.

Declaration of generative AI and AI-assisted technologies in the writing process

During the preparation of this work, the authors used ChatGPT to check and improve spelling and grammar. After using this tool/service, the authors reviewed and edited the content as needed and take full responsibility for the content of the publication.

CRediT authorship contribution statement

Antonio Velarte: Writing – review & editing, Writing – original draft, Methodology, Investigation, Conceptualization; **Antonio Castel:** Writing – original draft, Methodology, Investigation, Conceptualization; **Aranzazu Otin:** Writing – review & editing, Supervision; **Aida Olivan-Viguera:** Writing – review & editing, Methodology, Investigation; **Esther Pueyo:** Writing – review & editing, Supervision, Funding acquisition.

Data availability

Data will be made available on request.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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