UNIVERSIDAD DE ZARAGOZA

Centro Politécnico Superior

PROYECTO FIN DE CARRERA

Ingeniería de Telecomunicaciones

DISEÑO E IMPLEMENTACIÓN DE AMPLIFICADOR DE TRANSIMPEDANCIA Y ECUALIZADOR PARA COMUNICACIONES DE BANDA ANCHA CON FIBRA ÓPTICA DE PLÁSTICO

(ANEXOS 2/2)

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Anexo I

Técnicas de Ecualización Adaptativa

En este anexo se introducen los conceptos más importantes de la ecualización adaptativa y, posteriormente, se analizan las diferentes posibilidades.

I.1 Introducción

Al analizar cualquier sistema de transmisión, se observa que las características del canal no se mantienen constantes a lo largo del tiempo. Esto, que se puede producir por múltiples motivos - cambios de temperatura, características del material, diversas curvaturas, longitud variable del canal, etc. - , conlleva que tanto la dispersión como la atenuación cambien sustancialmente; lo que supone cambios en el ancho de banda que, a su vez, hacen deseable el diseño de un ecualizador que se adapte a los cambios en la respuesta del canal. Es decir, que las características frecuenciales del filtro pasa-alta deben adaptarse a la respuesta del enlace, ya que, en caso contrario, se produciría una sobrecompensación o una subcompensación que provocaría que el bit a transmitir se distorsione y, en consecuencia, el BER aumente.

A grandes rasgos, la estructura de un ecualizador adaptativo consta de dos bloques: el ecualizador (EQ) y el bloque que se encarga de modificar la respuesta del ecualizador en función de un análisis de la transmisión (UPDATE). Formando de esta manera un bucle de realimentación. El diagrama de bloques de dicha estructura se representa en la Fig. I.1.

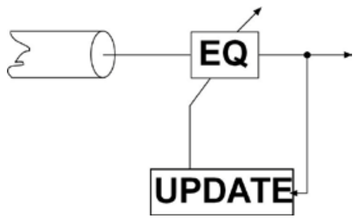


Fig. I.1 Diagrama de bloques de un ecualizador adaptativo.

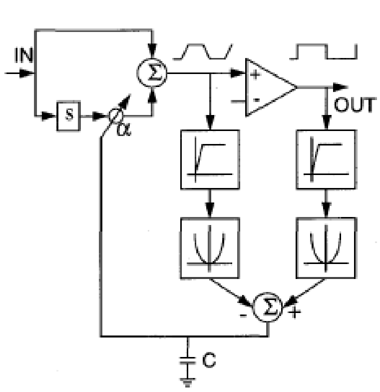
I.2 Clasificación

La primera consideración a tener en cuenta es dónde se realiza la adaptación: en el transmisor o en el receptor. Como en el transmisor no se tiene información del canal, la ecualización adaptativa se aplica normalmente en el receptor.

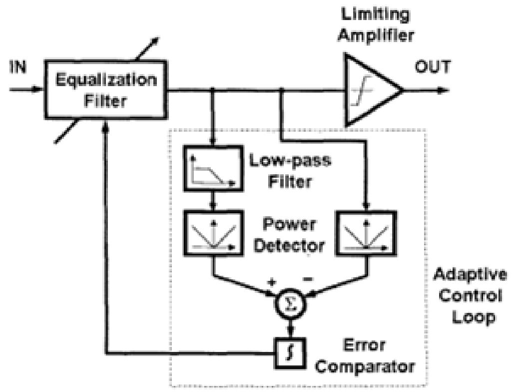
Para ecualizadores digitales, se utilizan diversos algoritmos, en los que el criterio más ampliamente aceptado es el de minimizar el error cuadrático (MSE) entre la secuencia recibida y la secuencia de entrenamiento conocida. Típicas estructuras que utilizan este criterio son: las *feed-forward transversal equalizers* (FFE) y las *decisión-feedback equalizer* (DFE). En ambas, se usa el algoritmo de mínimos cuadrados (LMS) o sus variaciones [HAR06].

Por otro lado, para los ecualizadores analógicos - ecualizadores pasivos (EQ-P) y de tiempo continuo (EQ-CT)-, el método de adaptación consiste en analizar la forma de onda de salida o su espectro. Y en función de la información obtenida modificar el comportamiento del EQ según convenga. Existen dos métodos para obtener dicha información: 1) muestrear y analizar las características de la transmisión en el dominio del tiempo o 2) la información se obtiene tratando de manera analógica el espectro de frecuencia. Este último es el más ampliamente implementado en los ecualizadores analógicos de alta velocidad [LIU04].

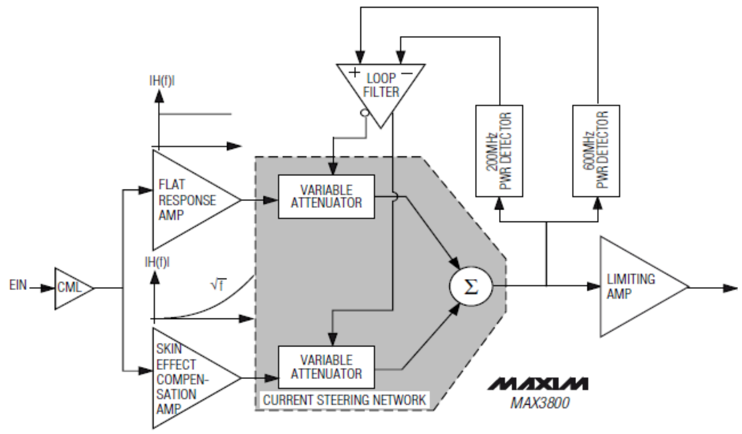
En la Fig. I.2., se representan los diagramas de bloques y las implementaciones típicas empleadas en ecualizadores analógicos de alta velocidad. Se observa que la diferencia radica en obtener la señal de error que proporciona la información de la respuesta del canal y es la que modifica al EQ.



(a)



(b)



(c)

Fig. I.2 Diagrama de bloques de ecualizadores analógicos adaptativos de alta velocidad: (a) Obtiene la diferencia de la componente en DC antes y después de un *slicer* [BAB98](b) compara la componente en DC con la potencia total recibida [SUN05] y (c) analiza la señal a 200 MHz y a 600 MHz para una aplicación de transmisión por cable coaxial a 3.2 Gbps [MAX01].

Anexo II Descripción de la instrumentación

En este anexo se realiza una breve descripción de la instrumentación empleada a lo largo de este PFC.

II.1. DCA 86100C, Agilent

El Analizador de Comunicaciones Digitales (DCA 86100C, Agilent), Fig. II.1, permite analizar y visualizar señales periódicas –como las PRBS- de alta velocidad. Proporciona toda la información intrínseca de un diagrama de ojo, así como análisis específicos de ruido y de *jitter*.

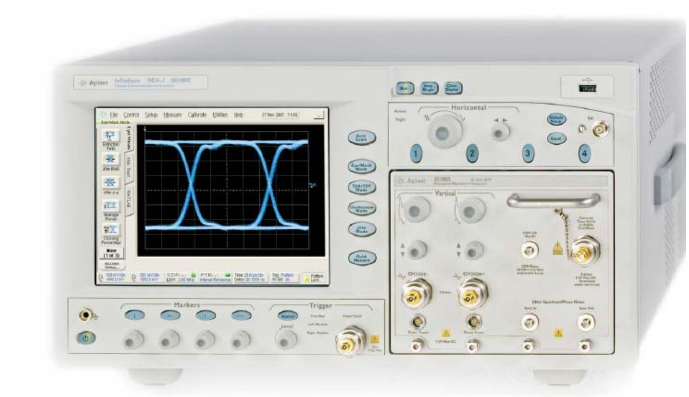
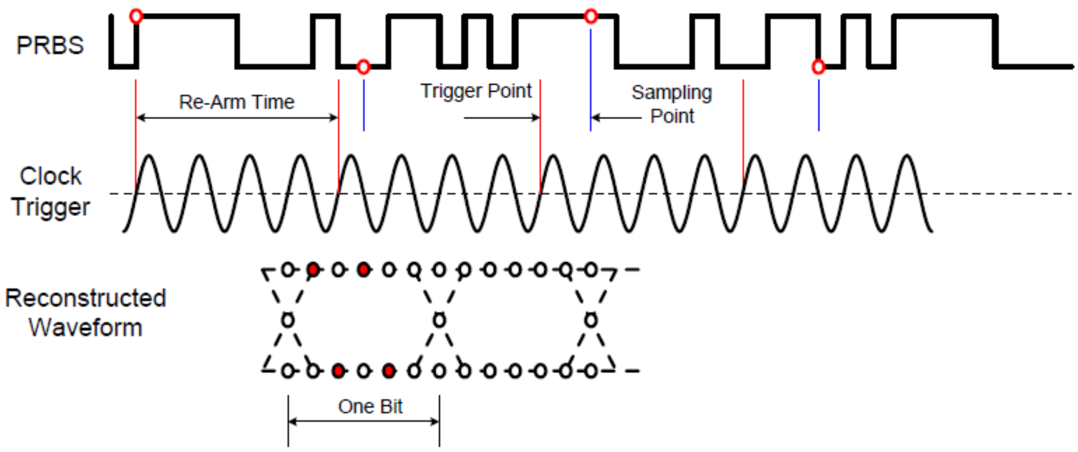
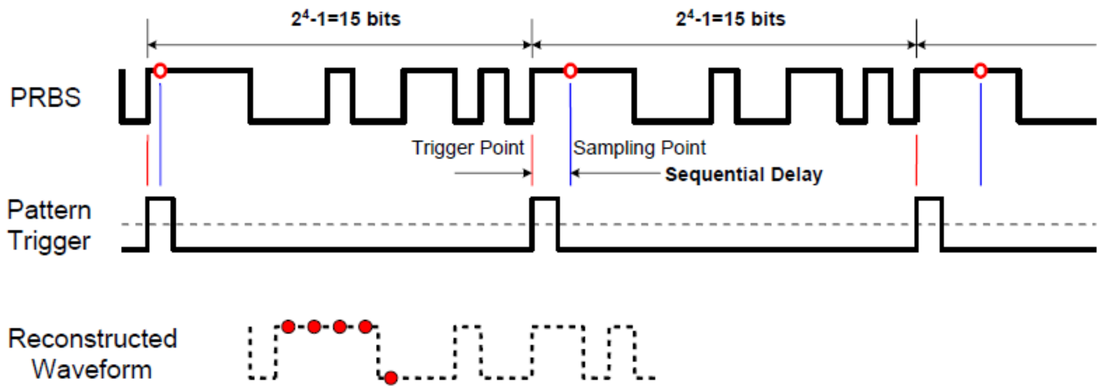


Fig. II.1 Analizador de redes. DCA 86100 C, Agilent [AGI05].

El DCA 86100C es un osciloscopio de tiempo equivalente que permite representar señales periódicas que uno de tiempo real no podría. La diferencia entre ambos tipos de osciloscopios radica en el método de muestreo empleado. El muestreo del segundo consiste en tomar muestras adyacentes, por lo que su límite de precisión vendrá impuesto por la capacidad de muestreo; mientras que el de tiempo equivalente toma muestras en diferentes barridos. Cada barrido viene marcado por una señal de disparo (*trigger*) que permite tomar de manera sincronizada, secuencial y ordenada una muestra de cada período de la señal. Cada una de éstas se toma con un retardo diferente respecto al *trigger*; este retardo se denomina retardo incremental y es el que marca la precisión del osciloscopio. Posteriormente se restaura la señal a un eje de tiempos común, situando cada muestra en función de su retardo. En la Fig. II.2.a se observa el método de muestreo y reconstrucción para representar un diagrama de ojo y en la Fig. II.2.b el de la señal PRBS propiamente dicha, para lo cual es necesario que se detecte el inicio del patrón de datos (*pattern jitter*).



II.2.(a)



II.2.(b)

Fig. II.2 Método de muestreo y reconstrucción en un osciloscopio de tiempo equivalente: (a) Diagrama de ojo y (b) Modo osciloscopio normal [AGI05].

II.2. BERT N4906A, Agilent

El medidor de tasa de error (BERT N4906, Agilent), Fig. II.3, permite medir el BER de un circuito, así como generar las señales necesarias para visualizar y analizar completamente un sistema a través de un DCA.

La salida que genera el BERT son secuencias de bits pseudoaleatorios (PRBS) que simulan una transmisión de datos real al contener un amplio rango de posibles transiciones de bits. Esto sirve para caracterizar el comportamiento de un sistema de comunicaciones.

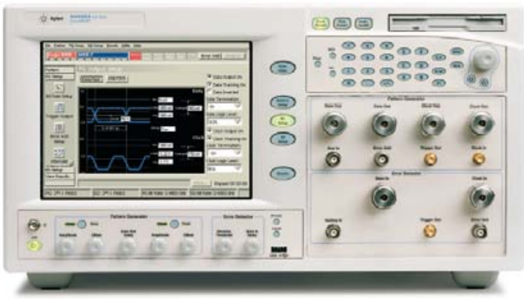


Fig. II.3 Medidor Tasa de Error. BERT N4906A, Agilent [AGI08].

II.3. ZVL 9KHz/6GHz, R&S

El analizador de redes vectorial (ZVL 9KHz/6GHz, R&S), Fig. II.4, nos proporciona la respuesta frecuencial del circuito bajo test (DUT). Para ello, es necesaria la correcta calibración que elimine de la medida tanto los elementos parásitos como los componentes necesarios en el *setup*. De esta forma, se asegura que la respuesta obtenida sea la del DUT.

Fig. II.4 Analizador de Redes Vectorial. ZVL 9KHz/6GHz, R&S [R&S09].

II.4. *Multimeter 3458A, Agilent*

El multímetro de precisión (*Multimeter* 3458A, Agilent), Fig. II.5, proporciona una medida exacta de las diferentes componentes en DC, tanto corriente como voltaje, con una sensibilidad máxima de 10 nV y 1 pA respectivamente.

Fig. II.5 Multímetro de Precisión. *Multimeter* 3458A, Agilent [AGI01].

II.5. *FM300 Fotec m*

El medidor de potencia óptica para fibra FM300, Fotec m, Fig. II.6, tiene un detector de silicio que permite medir la potencia recibida para una $\lambda \approx 665$ nm, en un rango de +10 a -70 dBm.

Fig. II.6 Medidor de Potencia Óptica para Fibra. FM300, Fotec m [FOT00].

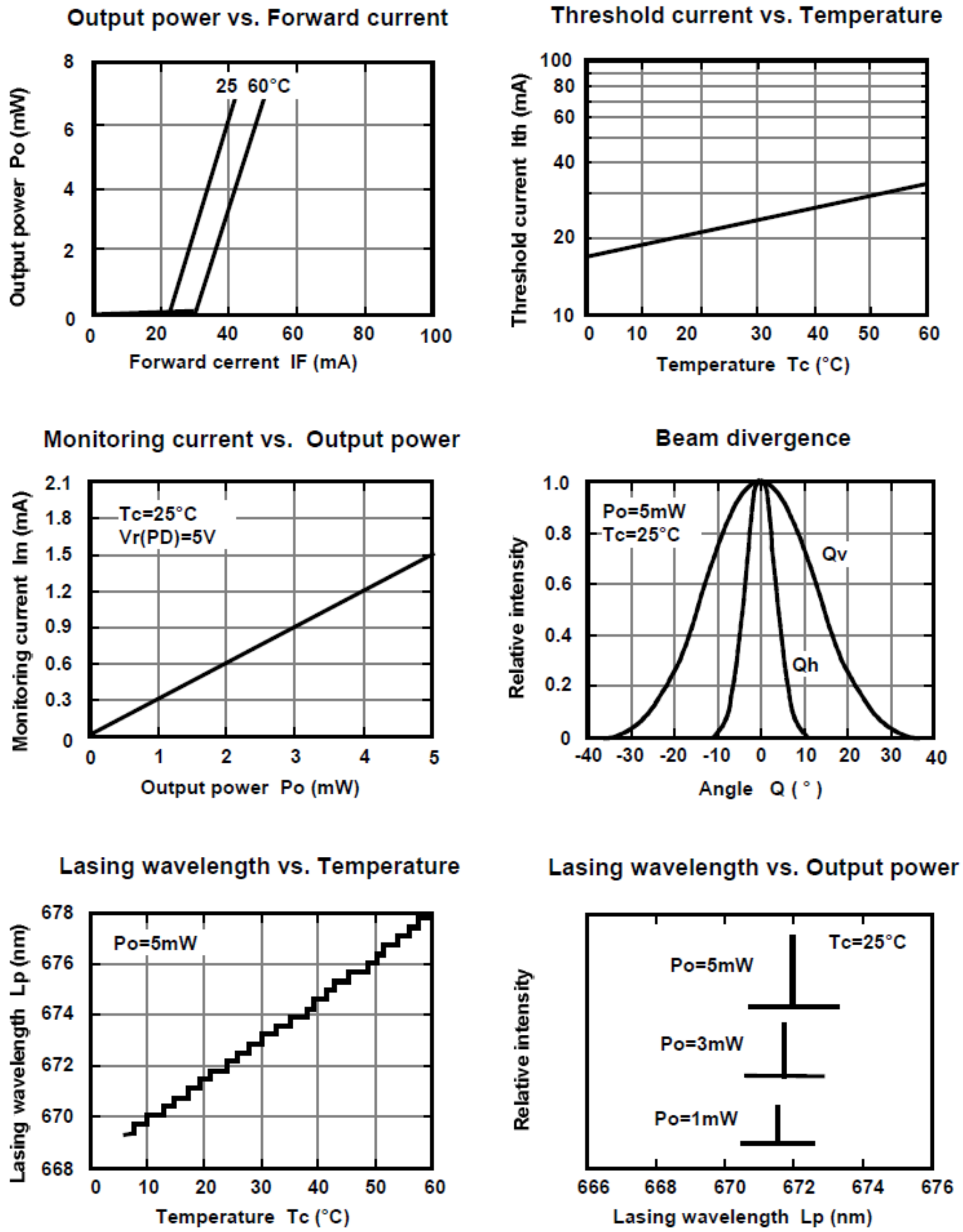
Anexo III Hojas de características

En este anexo se exponen las hojas de características de los componentes comerciales que se han utilizado en este PFC.

III.1. Red laser diode. DL 3149-057, Sanyo

DL-3149-057

Characteristics



This is typical data and it may not represent all products.

III.2. SI-POF. ESKA Premier GH 4002 2.2 mm, Mitsubishi

ESKA™ Premier Polyethylene-jacketed Optical Fiber Cord: GH-4002

Manufactured by Mitsubishi Rayon Co., Ltd.

Marketed and sold by Mitsubishi International Corporation July 2001

Structure		
Core Material	Polymethyl Methacrylate Resin (PMMA)	
Cladding Material	Fluorinated Polymer	
Core Refractive Index	1.49	
Numerical Aperture	0.5	
Refractive Index Profile	(Step Index)	
	Unit	*Typical*
Core Diameter	µm	980
Cladding Diameter	µm	1,000
Jacket Diameter (zip-cord)	mm	2.2 X 4.4
Fiber Diameter (mm) X # of fibers	1.0 mm X 2	
Approximate Weight (g/m)	8.0	

Packaging	
Spool Length (m)	500
Net weight on spool (kg)	4.9
Spool Weight (kg)	0.68
Carton Size (mm)	365 X 365 X 160
Carton Weight (kg)	5.5
Master Carton	5 spools
Jacket	
Color and Material	Black PE
Indication on Jacket	ESKA Premier; Pink color

Performance		Criteria for Acceptance and/or Test Conditions	Unit	Values
Temperature Range		No deterioration in optical properties *	°C	-55 ~ 85
Operating Temperature under Conditions of High Humidity		No deterioration in optical properties [95% RH] **	°C	=<75
Optical Properties	Transmission Loss	650nm collimated light (standard conditions) [10m – 1m cutback]	dB/km	=<170
	Loss under 95% RH			=<190
Mechanical Character-istics	Minimum Bend Radius	Loss increment =< 0.5dB [Quarter bend]	mm	=>25
	Repeated Bending Endurance	Loss increment =< 1 dB [conforms to JIS C 6861]	Times	=>10,000
	Tensile Strength	Tensile force at yield point [JIS C 6861]	N	=>140
	Twisting Endurance	Loss increment =< 1 dB [sample length = 1 m, tensile force = 4.9N]	Times	=>5
	Impact Endurance	Loss increment =< 1 dB [conforms to JIS C 6861]	N.m	=>0.4

Notes: Performance tested in conditions under 25°C unless otherwise indicated
* Attenuation increase is <10% after 1000 hours
** Attenuation increase is <10% after 1000 hours.

Applications

The GH-Series of single-jacket cables are typically used as data transfer media.

The information contained herein is presented as a guide to product selection. It is subject to change without notice, and should not be regarded as a representation, warranty or guarantee with regard to the quality, characteristics or use of this product

655 Third Avenue New York, NY 10017

Please visit www.fiberoptic-plastic.com to locate a sales representative near you

III.3. Si PIN S5972, Hamamatsu

PHOTODIODE

Si PIN photodiode
S5971, S5972, S5973 series

High-speed photodiodes (S5973 series: 1.5 GHz)

S5971, S5972 and S5973 series are high-speed Si PIN photodiodes designed for visible to near infrared light detection. These photodiodes provide wideband characteristics at a low bias, making them suitable for optical communications and other high-speed photometry. S5973 series includes a mini-lens type (S5973-01) that can be efficiently coupled to an optical fiber and a violet sensitivity enhanced type (S5973-02) ideal for violet laser detection.

Features

- High-speed response
  S5971 : 100 MHz (VR=10 V)
  S5972 : 500 MHz (VR=10 V)
  S5973 series: 1 GHz (VR=3.3 V)
- Low price
- High sensitivity
  S5973-02: 0.3 A/W, QE=91 % (λ=410 nm)
- High reliability

Applications

- Optical fiber communications
- High-speed photometry
- Violet laser detection (S5973-02)

■ General ratings / Absolute maximum ratings

Type No.	Dimensional outline/ Window material *1	Package (mm)	Active area size (mm)	Effective active area (mm²)	Absolute maximum ratings: Reverse voltage VR Max. (V)	Power dissipation P (mW)	Operating temperature Topr (°C)	Storage temperature Tstg (°C)
S5971	①/K	TO-18	ϕ1.2	1.1	20	50	-40 to +100	-55 to +125
S5972			ϕ0.8	0.5				
S5973			ϕ0.4	0.12				
S5973-01	②/L							
S5973-02	③/K							

■ Electrical and optical characteristics

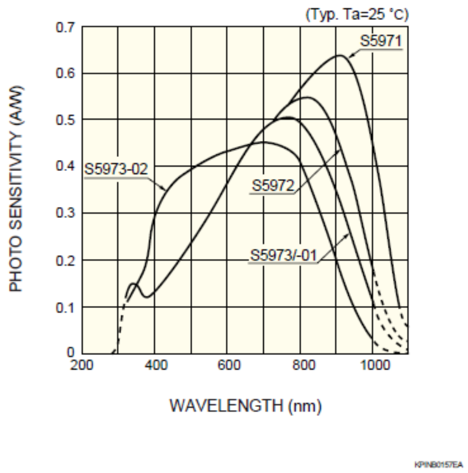
Type No.	Spectral response range λ (nm)	Peak sensitivity wavelength λp (nm)	Photo sensitivity S (A/W) λp	660 nm	780 nm	830 nm	Short circuit current Isc 100 lx (μA)	Dark current ID Typ. (nA)	Dark current ID Max. (nA)	Temp. coefficient of ID TCID (times/°C)	Cut-off frequency fc (GHz)	Terminal capacitance Ct f=1 MHz (pF)	NEP VR=10 V λ=λp (W/Hz$^{1/2}$)
S5971	320 to 1060	900	0.64	0.44	0.55	0.6	1.0	0.07 *3	1 *3	1.15	0.1 *3	3 *3	7.4×10^{-15}
S5972	320 to 1000	800	0.57			0.55	0.42	0.01 *3	0.5 *3		0.5 *3		3.1×10^{-15}
S5973		760	0.52		0.51	0.47	0.09	0.001 *4	0.1 *4		1.5 *4	1.6 *4	1.1×10^{-15} *4
S5973-01							0.42						
S5973-02			0.45	0.3 *2	0.42	0.37	0.09						1.9×10^{-15} *2, *4

*1: Window material K: borosilicate glass, L: lens type borosilicate glass
*2: λ=410 nm
*3: VR=10 V
*4: VR=3.3 V

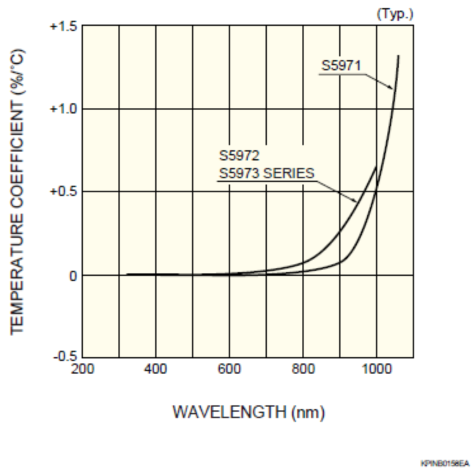
SOLID STATE DIVISION

HAMAMATSU

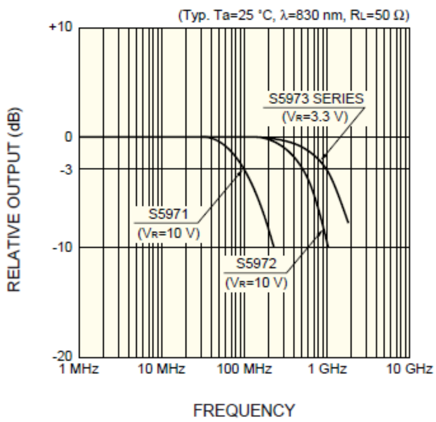
■ Spectral response



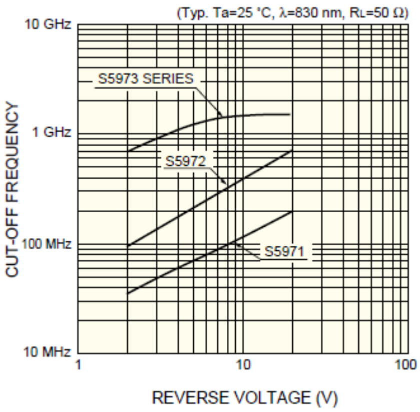
■ Photo sensitivity temperature characteristics



■ Frequency response

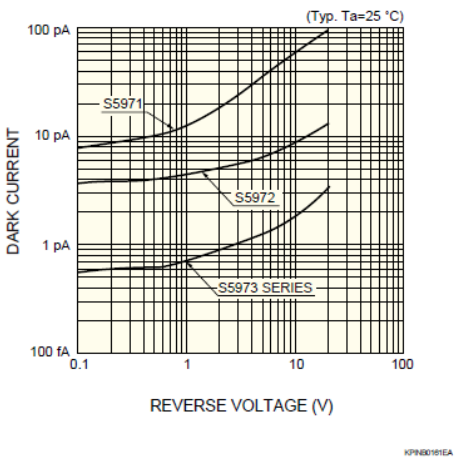


■ Cut-off frequency vs. reverse voltage

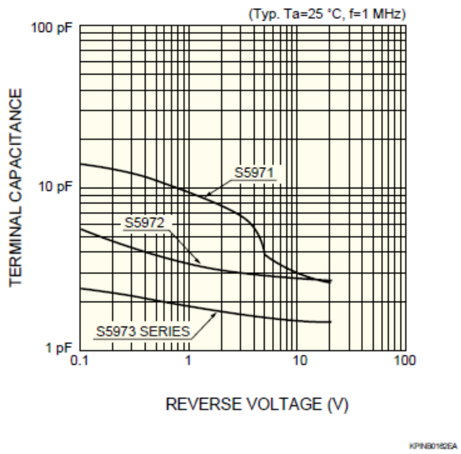


Si PIN photodiode S5971, S5972, S5973 series

■ Dark current vs. reverse voltage

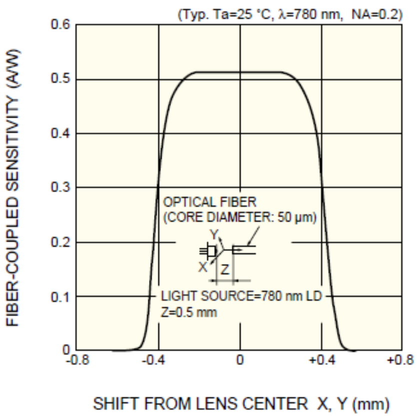


■ Terminal capacitance vs. reverse voltage

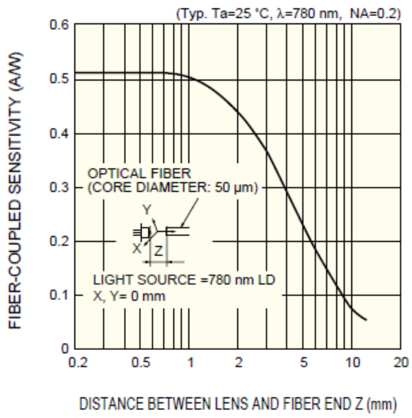


■ Fiber coupling characteristics (S5973-01)

X, Y direction



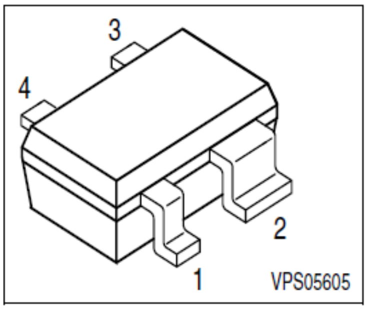
Z direction



III.4. Transistor. BFP640, Infineon

BFP640

NPN Silicon Germanium RF Transistor



BFP640E/L6327 and E/L7764

- High gain low noise RF transistor
- Provides outstanding performance for a wide range of wireless applications
- Ideal for CDMA and WLAN applications
- Outstanding noise figure F = 0.65 dB at 1.8 GHz
  Outstanding noise figure F = 1.3 dB at 6 GHz
- High maximum stable gain
  G_{ms} = 24 dB at 1.8 GHz
- Gold metallization for extra high reliability
- 70 GHz f_T-Silicon Germanium technology
- L6327 and L7764 are early Pb-free

ESD: **E**lectrostatic **d**ischarge sensitive device, observe handling precaution!

Type	Marking	Pin Configuration						Package
BFP640	R4s	1=B	2=E	3=C	4=E	-	-	SOT343

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	4	V
Collector-emitter voltage	V_{CES}	13	
Collector-base voltage	V_{CBO}	13	
Emitter-base voltage	V_{EBO}	1.2	
Collector current	I_C	50	mA
Base current	I_B	3	
Total power dissipation[1)] $T_S \leq 90°C$	P_{tot}	200	mW
Junction temperature	T_j	150	°C
Ambient temperature	T_A	-65 ... 150	
Storage temperature	T_{stg}	-65 ... 150	

[1] T_S is measured on the collector lead at the soldering point to the pcb

Infineon technologies **BFP640**

Thermal Resistance

Parameter	**Symbol**	**Value**	**Unit**
Junction - soldering point[1)]	R_{thJS}	≤ 300	K/W

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
DC Characteristics					
Collector-emitter breakdown voltage I_C = 1 mA, I_B = 0	$V_{(BR)CEO}$	4	4.5	-	V
Collector-emitter cutoff current V_{CE} = 13 V, V_{BE} = 0	I_{CES}	-	-	30	µA
Collector-base cutoff current V_{CB} = 5 V, I_E = 0	I_{CBO}	-	-	100	nA
Emitter-base cutoff current V_{EB} = 0.5 V, I_C = 0	I_{EBO}	-	-	3	µA
DC current gain I_C = 30 mA, V_{CE} = 3 V	h_{FE}	100	180	320	-

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Infineon technologies **BFP640**

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics (verified by random sampling)					
Transition frequency I_C = 30 mA, V_{CE} = 3 V, f = 1 GHz	f_T	30	40	-	GHz
Collector-base capacitance V_{CB} = 3 V, f = 1 MHz	C_{cb}	-	0.09	0.2	pF
Collector emitter capacitance V_{CE} = 3 V, f = 1 MHz	C_{ce}	-	0.23	-	
Emitter-base capacitance V_{EB} = 0.5 V, f = 1 MHz	C_{eb}	-	0.5	-	
Noise figure I_C = 5 mA, V_{CE} = 3 V, f = 1.8 GHz, $Z_S = Z_{Sopt}$ I_C = 5 mA, V_{CE} = 3 V, f = 6 GHz, $Z_S = Z_{Sopt}$	F	 - -	 0.65 1.3	 - -	dB
Power gain, maximum stable[1)] I_C = 30 mA, V_{CE} = 3 V, $Z_S = Z_{Sopt}$, $Z_L = Z_{Lopt}$, f = 1.8 GHz	G_{ms}	-	24	-	dB
Power gain, maximum available[1)] I_C = 30 mA, V_{CE} = 3 V, $Z_S = Z_{Sopt}$, $Z_L = Z_{Lopt}$, f = 6 GHz	G_{ma}	-	12.5	-	dB
Transducer gain I_C = 30 mA, V_{CE} = 3 V, $Z_S = Z_L$ = 50 Ω, f = 1.8 GHz I_C = 30 mA, V_{CE} = 3 V, $Z_S = Z_L$ = 50 Ω, f = 6 GHz	$\|S_{21e}\|^2$	 - -	 21 10.5	 - -	dB
Third order intercept point at output[2)] V_{CE} = 3 V, I_C = 30 mA, f = 1.8 GHz, $Z_S = Z_L$ = 50 Ω	IP_3	-	26.5	-	dBm
1dB Compression point at output I_C = 30 mA, V_{CE} = 3 V, $Z_S = Z_L$ = 50 Ω, f = 1.8 GHz	P_{-1dB}	-	13	-	

[1] $G_{ma} = |S_{21e} / S_{12e}| (k-(k^2-1)^{1/2})$, $G_{ms} = |S_{21e} / S_{12e}|$

[2] IP3 value depends on termination of all intermodulation frequency components.
Termination used for this measurement is 50Ω from 0.1 MHz to 6 GHz

BFP640

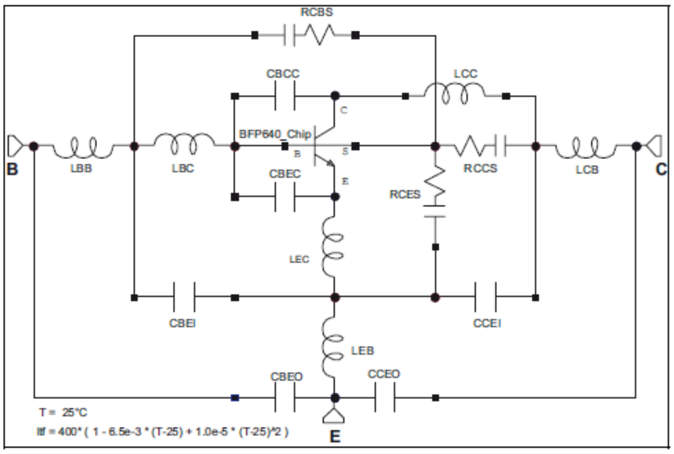
SPICE Parameter (Gummel-Poon Model, Berkley-SPICE 2G.6 Syntax):

Transitor Chip Data:

IS =	0.22	fA	BF =	450	-	NF =	1.025	-
VAF =	1000	V	IKF =	0.15	A	ISE =	21	fA
NE =	2	-	BR =	55	-	NR =	1	-
VAR =	2	V	IKR =	3.8	mA	ISC =	400	fA
NC =	1.8	-	RB =	3.129	Ω	IRB =	1.522	mA
RBM =	2.707	Ω	RE =	0.6	-	RC =	3.061	Ω
CJE =	227.6	fF	VJE =	0.8	V	MJE =	0.3	-
TF =	1.8	ps	XTF =	10	-	VTF =	1.5	V
ITF =	0.4	A	PTF =	0	deg	CJC =	67.43	fF
VJC =	0.6	V	MJC =	0.5	-	XCJC =	1	-
TR =	0.2	ns	CJS =	93.4	fF	VJS =	0.6	V
MJS =	0.27	-	XTB =	-1.42	-	EG =	1.078	eV
XTI =	3	-	FC =	0.8		TNOM	298	K
AF =	2	-	KF =	7.291E-11				
TITF1	-0.0065	-	TITF2	1.0E-5				

All parameters are ready to use, no scalling is necessary. Extracted on behalf of Infineon Technologies AG by: Institut für Mobil- und Satellitentechnik (IMST)

Package Equivalent Circuit:



LBC =	120	pH
LCC =	120	pH
LEC =	20	pH
LBB =	696.2	pH
LCB =	682.4	pH
LEB =	230.6	pH
CBEC =	98.4	fF
CBCC =	55.9	fF
CES =	180	fF
CBS =	79	fF
CCS =	75	fF
CCEO =	131.2	fF
CBEO =	102.5	fF
CCEI =	112.6	fF
CBEI =	180.4	fF
RBS =	1200	Ω
RCS =	1200	Ω
RES =	300	Ω

Valid up to 6GHz

For examples and ready to use parameters please contact your local Infineon Technologies distributor or sales office to obtain a Infineon Technologies CD-ROM or see Internet: http//www.infineon.com/silicondiscretes

III.5. Array de Transistores. HFA3127, Intersil

intersil

HFA3046, HFA3096, HFA3127, HFA3128

Data Sheet December 21, 2005 FN3076.13

Ultra High Frequency Transistor Arrays

The HFA3046, HFA3096, HFA3127 and the HFA3128 are Ultra High Frequency Transistor Arrays that are fabricated from Intersil Corporation's complementary bipolar UHF-1 process. Each array consists of five dielectrically isolated transistors on a common monolithic substrate. The NPN transistors exhibit a f_T of 8GHz while the PNP transistors provide a f_T of 5.5GHz. Both types exhibit low noise (3.5dB), making them ideal for high frequency amplifier and mixer applications.

The HFA3046 and HFA3127 are all NPN arrays while the HFA3128 has all PNP transistors. The HFA3096 is an NPN-PNP combination. Access is provided to each of the terminals for the individual transistors for maximum application flexibility. Monolithic construction of these transistor arrays provides close electrical and thermal matching of the five transistors.

Intersil provides an Application Note illustrating the use of these devices as RF amplifiers. For more information, visit our website at www.intersil.com.

Features

- NPN Transistor (f_T) 8GHz
- NPN Current Gain (h_{FE}). 130
- NPN Early Voltage (V_A) 50V
- PNP Transistor (f_T). 5.5GHz
- PNP Current Gain (h_{FE}). 60
- PNP Early Voltage (V_A) 20V
- Noise Figure (50Ω) at 1.0GHz 3.5dB
- Collector to Collector Leakage. . . . . <1pA
- Complete Isolation Between Transistors
- Pin Compatible with Industry Standard 3XXX Series Arrays
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- VHF/UHF Amplifiers
- VHF/UHF Mixers
- IF Converters
- Synchronous Detectors

Ordering Information

PART NUMBER*	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HFA3046B	HFA3046B	-55 to 125	14 Ld SOIC	M14.15
HFA3046BZ (Note)	HFA3046BZ	-55 to 125	14 Ld SOIC (Pb-free)	M14.15
HFA3096B	HFA3096B	-55 to 125	16 Ld SOIC	M16.15
HFA3096BZ (Note)	HFA3096BZ	-55 to 125	16 Ld SOIC (Pb-free)	M16.15
HFA3127B	HFA3127B	-55 to 125	16 Ld SOIC	M16.15
HFA3127BZ (Note)	HFA3127BZ	-55 to 125	16 Ld SOIC (Pb-free)	M16.15
HFA3127R	127	-55 to 125	16 Ld 3x3 QFN	L16.3x3
HFA3127RZ (Note)	127Z	-55 to 125	16 Ld 3x3 QFN (Pb-free)	L16.3x3
HFA3128B	HFA3128B	-55 to 125	16 Ld SOIC	M16.15
HFA3128BZ (Note)	HFA3128BZ	-55 to 125	16 Ld SOIC (Pb-free)	M16.15
HFA3128R	128	-55 to 125	16 Ld 3x3 QFN	L16.3x3
HFA3128RZ (Note)	128Z	-55 to 125	16 Ld 3x3 QFN (Pb-free)	L16.3x3

*Add "96" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Application Note MM3046

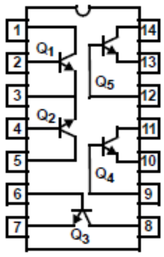
PSpice Listing

```
*
*COPYRIGHT © 1994 INTERSIL CORPORATION
*ALL RIGHTS RESERVED
*
*HFA3046/3096/3127/3128 PSpice MODEL
*REV: 1-3-94
*
***** UHFN - LE = 3 WE = 50  *****
*
*     ----- BJT MODELS -----
*
.model NUHFARRY NPN
+      (IS =  1.840E - 16     XTI=  3.000E + 00     EG =  1.110E + 00     VAF =  7.200E + 01
+      VAR =  4.500E + 00      BF =  1.036E + 02    ISE =  1.686E - 19      NE =  1.400E + 00
+      IKF =  5.400E - 02     XTB =  0.000E + 00     BR =  1.000E + 01     ISC =  1.605E - 14
+       NC =  1.800E + 00     IKR =  5.400E - 02     RC =  1.140E + 01     CJC =  3.980E - 13
+      MJC =  2.400E - 01     VJC =  9.700E - 01     FC =  5.000E - 01     CJE =  2.400E - 13
+      MJE =  5.100E- 01      VJE =  8.690E - 01     TR =  4.000E - 09      TF =  10.51E - 12
+      ITF =  3.500E - 02     XTF =  2.300E + 00    VTF =  3.500E + 00     PTF =  0.000E + 00
+     XCJC =  9.000E - 01     CJS =  1.150E - 13    VJS =  7.500E - 01     MJS =  0.000E + 00
+       RE =  1.848E + 00      RB =  5.007E + 01    RBM =  1.974E + 00      KF =  0.000E + 00
+       AF =  1.000E + 00)
*
*
***** UHFP - LE = 3 WE = 50 ****
*
.model PUHFARRY PNP
+      (IS =  1.027E - 16     XTI =  3.000E + 00    EG =  1.110E + 00     VAF =  3.000E + 01
+      VAR =  4.500E + 00      BF =  5.228E + 01    ISE =  9.398E - 20      NE =  1.400E + 00
+      IKF =  5.412E - 02     XTB =  0.000E + 00     BR =  7.000E + 00     ISC =  1.027E - 14
+       NC =  1.800E + 00     IKR =  5.412E - 02     RC =  3.420E + 01     CJC =  4.951E - 13
+      MJC =  3.000E - 01     VJC =  1.230E + 00     FC =  5.000E - 01     CJE =  2.927E - 13
+      MJE =  5.700E - 01     VJE =  8.800E - 01     TR =  4.000E - 09      TF =  20.05E - 12
+      ITF =  2.001E - 02     XTF =  1.534E + 00    VTF =  1.800E + 00     PTF =  0.000E + 00
+     XCJC =  9.000E - 01     CJS =  1.150E - 13    VJS =  7.500E - 01     MJS =  0.000E + 00
+       RE =  1.848E + 00      RB=  3.271E + 01     RBM =  9.902E - 01      KF =  0.000E + 00
+       AF =  1.000E + 00)
```

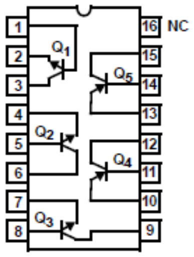
HFA3046, HFA3096, HFA3127, HFA3128

Pinouts

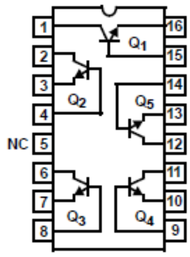
HFA3046
TOP VIEW



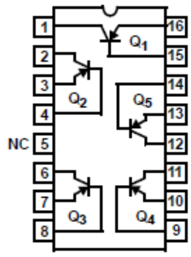
HFA3096
TOP VIEW



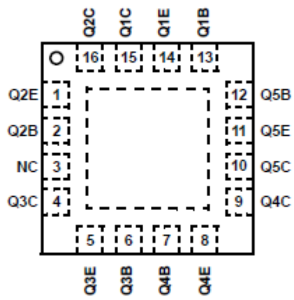
HFA3127
TOP VIEW



HFA3128
TOP VIEW



HFA3127, HFA3128
TOP VIEW



Absolute Maximum Ratings

Collector to Emitter Voltage (Open Base) 8V
Collector to Base Voltage (Open Emitter) 12V
Emitter to Base Voltage (Reverse Bias). 5.5V
Collector Current (100% Duty Cycle) . . . . . . 18.5mA at T_J = 150°C
34mA at T_J = 125°C
37mA at T_J = 110°C
Peak Collector Current (Any Condition). 65mA

Operating Information

Temperature Range . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld SOIC Package (Note 1)	120	N/A
16 Ld SOIC Package (Note 1)	115	N/A
QFN Package (Notes 2, 3)	57	10

Maximum Power Dissipation (Any One Transistor) 0.15W
Maximum Junction Temperature (Die) . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	DIE			SOIC, QFN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC NPN CHARACTERISTICS								
Collector to Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = 100µA, I_E = 0	12	18	-	12	18	-	V
Collector to Emitter Breakdown Voltage, $V_{(BR)CEO}$	I_C = 100µA, I_B = 0	8	12	-	8	12	-	V
Collector to Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = 100µA, Base Shorted to Emitter	10	20	-	10	20	-	V
Emitter to Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = 10µA, I_C = 0	5.5	6	-	5.5	6	-	V
Collector-Cutoff-Current, I_{CEO}	V_{CE} = 6V, I_B = 0	-	2	100	-	2	100	nA
Collector-Cutoff-Current, I_{CBO}	V_{CB} = 8V, I_E = 0	-	0.1	10	-	0.1	10	nA
Collector to Emitter Saturation Voltage, $V_{CE(SAT)}$	I_C = 10mA, I_B = 1mA	-	0.3	0.5	-	0.3	0.5	V
Base to Emitter Voltage, V_{BE}	I_C = 10mA	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	I_C = 10mA, V_{CE} = 2V	40	130	-	40	130	-	
Early Voltage, V_A	I_C = 1mA, V_{CE} = 3.5V	20	50	-	20	50	-	V
Base to Emitter Voltage Drift	I_C = 10mA	-	-1.5	-	-	-1.5	-	mV/°C
Collector to Collector Leakage		-	1	-	-	1	-	pA

Electrical Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	DIE			SOIC, QFN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC NPN CHARACTERISTICS								
Noise Figure	f = 1.0GHz, V_{CE} = 5V, I_C = 5mA, Z_S = 50Ω	-	3.5	-	-	3.5	-	dB
f_T Current Gain-Bandwidth Product	I_C = 1mA, V_{CE} = 5V	-	5.5	-	-	5.5	-	GHz
	I_C = 10mA, V_{CE} = 5V	-	8	-	-	8	-	GHz

HFA3046, HFA3096, HFA3127, HFA3128

Electrical Specifications $T_A = 25°C$ **(Continued)**

PARAMETER	TEST CONDITIONS	DIE MIN	DIE TYP	DIE MAX	SOIC, QFN MIN	SOIC, QFN TYP	SOIC, QFN MAX	UNITS
Power Gain-Bandwidth Product, f_{MAX}	I_C = 10mA, V_{CE} = 5V	-	6	-	-	2.5	-	GHz
Base to Emitter Capacitance	V_{BE} = -3V	-	200	-	-	500	-	fF
Collector to Base Capacitance	V_{CB} = 3V	-	200	-	-	500	-	fF

Electrical Specifications $T_A = 25°C$

PARAMETER	TEST CONDITIONS	DIE MIN	DIE TYP	DIE MAX	SOIC, QFN MIN	SOIC, QFN TYP	SOIC, QFN MAX	UNITS
DC PNP CHARACTERISTICS								
Collector to Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = -100µA, I_E = 0	10	15	-	10	15	-	V
Collector to Emitter Breakdown Voltage, $V_{(BR)CEO}$	I_C = -100µA, I_B = 0	8	15	-	8	15	-	V
Collector to Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = -100µA, Base Shorted to Emitter	10	15	-	10	15	-	V
Emitter to Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = -10µA, I_C = 0	4.5	5	-	4.5	5	-	V
Collector Cutoff Current, I_{CEO}	V_{CE} = -6V, I_B = 0	-	2	100	-	2	100	nA
Collector Cutoff Current, I_{CBO}	V_{CB} = -8V, I_E = 0	-	0.1	10	-	0.1	10	nA
Collector to Emitter Saturation Voltage, $V_{CE(SAT)}$	I_C = -10mA, I_B = -1mA	-	0.3	0.5	-	0.3	0.5	V
Base to Emitter Voltage, V_{BE}	I_C = -10mA	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	I_C = -10mA, V_{CE} = -2V	20	60	-	20	60	-	
Early Voltage, V_A	I_C = -1mA, V_{CE} = -3.5V	10	20	-	10	20	-	V
Base to Emitter Voltage Drift	I_C = -10mA	-	-1.5	-	-	-1.5	-	mV/°C
Collector to Collector Leakage		-	1	-	-	1	-	pA

Electrical Specifications $T_A = 25°C$

PARAMETER	TEST CONDITIONS	DIE MIN	DIE TYP	DIE MAX	SOIC, QFN MIN	SOIC, QFN TYP	SOIC, QFN MAX	UNITS
DYNAMIC PNP CHARACTERISTICS								
Noise Figure	f = 1.0GHz, V_{CE} = -5V, I_C = -5mA, Z_S = 50Ω	-	3.5	-	-	3.5	-	dB
f_T Current Gain-Bandwidth Product	I_C = -1mA, V_{CE} = -5V	-	2	-	-	2	-	GHz
	I_C = -10mA, V_{CE} = -5V	-	5.5	-	-	5.5	-	GHz
Power Gain-Bandwidth Product	I_C = -10mA, V_{CE} = -5V	-	3	-	-	2	-	GHz
Base to Emitter Capacitance	V_{BE} = 3V	-	200	-	-	500	-	fF
Collector to Base Capacitance	V_{CB} = -3V	-	300	-	-	600	-	fF

Electrical Specifications T_A = 25°C (Continued)

PARAMETER	TEST CONDITIONS	DIE			SOIC, QFN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL PAIR MATCHING CHARACTERISTICS FOR THE HFA3046								
Input Offset Voltage	I_C = 10mA, V_{CE} = 5V	-	1.5	5.0	-	1.5	5.0	mV
Input Offset Current	I_C = 10mA, V_{CE} = 5V	-	5	25	-	5	25	µA
Input Offset Voltage TC	I_C = 10mA, V_{CE} = 5V	-	0.5	-	-	0.5	-	µV/°C

S-Parameter and PSPICE model data is available from Intersil Sales Offices, and Intersil Corporation's web site.

Typical Performance Curves

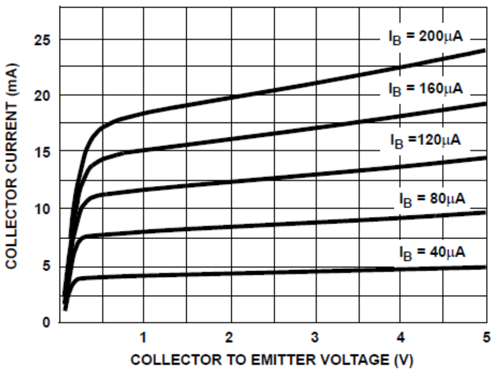


FIGURE 1. NPN COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

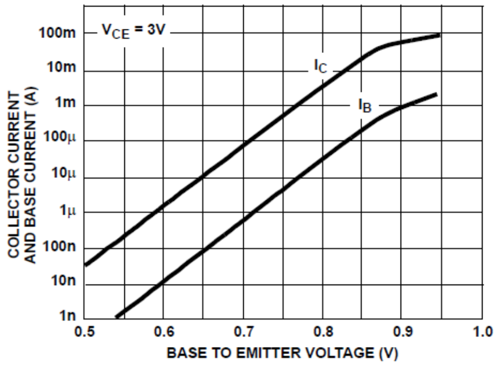


FIGURE 2. NPN COLLECTOR CURRENT AND BASE CURRENT vs BASE TO EMITTER VOLTAGE

Typical Performance Curves (Continued)

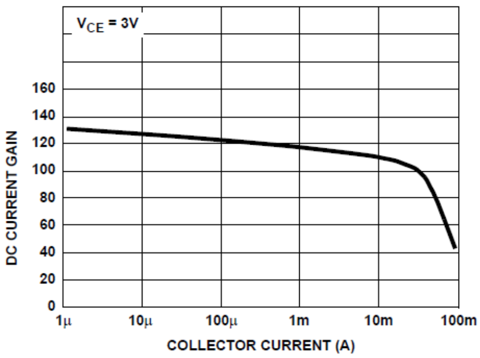


FIGURE 3. NPN DC CURRENT GAIN vs COLLECTOR CURRENT

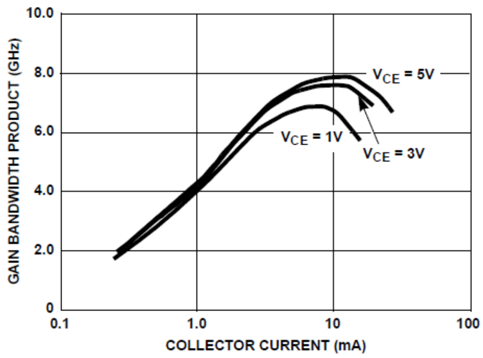


FIGURE 4. NPN GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

III.6. Bias-T. ZFBT-4R2G+, Minicircuits

Coaxial

Bias-Tee

50Ω Wideband 10 to 4200 MHz

ZFBT-4R2G+

CASE STYLE: K18

Connectors	Model	Price	Qty.
SMA	ZFBT-4R2G+	$59.95	(1-9)
BRACKET (OPTION "B")		$2.50	(1+)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-55°C to 100°C
Storage Temperature	-55°C to 100°C
RF Power	30 dBm max.
Voltage at DC port	30 V max.
Input Current	500 mA
DC resistance from DC to RF&DC port	4.5 ohm typ.

Permanent damage may occur if any of these limits are exceeded.

Coaxial Connections

RF	1 (SMA female)
RF&DC	2 (SMA male)
DC	3 (SMA female)

Features

- wideband, 10 to 4200 MHz
- low insertion loss, 0.6 dB typ.
- good isolation, 40 dB typ.

Applications

- biasing amplifiers
- biasing of laser diodes
- biasing of active antennas
- DC return
- DC blocking
- test accessory

Bias-Tee Electrical Specifications

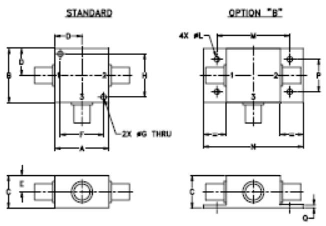
FREQUENCY (MHz)		INSERTION LOSS* (dB)						ISOLATION* (dB) (RF port to DC port) (RF&DC port to DC port)						VSWR** (:1)					
		L		M		U		L		M		U		L		M		U	
f_L	f_U	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.	Max.	Typ.	Max.	Typ.	Max.
10	4200	0.15	0.6	0.6	1.2	0.6	1.6	32	20	40	20	50	20	1.06	1.2	1.13	1.3	1.13	1.3

L= low range (f_L to 10 f_L) M= mid range (10 f_L to f_U/2) U= upper range (f_U/2 to f_U)

* Insertion Loss and Isolation are guaranteed up to 20 dBm-RF power and 200mA DC current.

**VSWR measured with open and short at DC port.

Outline Drawing



Outline Dimensions (inch / mm)

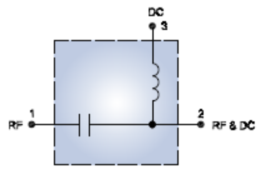
A	B	C	D	E	F	G	H
1.25	1.25	.75	.63	.38	1.00	.125	1.000
31.75	31.75	19.05	16.00	9.65	25.40	3.18	25.40

J	K	L	M	N	P	Q	wt
--	--	.125	1.688	2.18	.75	.07	grams
--	--	3.18	42.88	55.37	19.05	1.78	70.0

Typical Performance Data

Freq. (MHz)	Pin (dBm)	INSERTION LOSS (dB) with Current						ISOLATION (dB) (Pin= -10dBm) with current						VSWR (:1)
		0mA	20mA	50mA	100mA	150mA	200mA	10mA	20mA	50mA	100mA	150mA	200mA	
0.10	19.80	0.17	0.17	0.16	0.17	0.20	0.24	19.46	19.04	17.83	14.58	12.66	11.75	1.16
0.27	19.80	0.13	0.13	0.13	0.14	0.14	0.15	25.86	25.53	24.52	21.43	19.31	18.16	1.07
0.53	19.80	0.12	0.12	0.12	0.11	0.11	0.11	29.17	28.98	28.36	26.18	24.40	23.37	1.04
1.06	19.80	0.13	0.13	0.12	0.11	0.12	0.12	30.81	30.74	30.56	29.62	28.62	27.92	1.02
10.00	18.50	0.16	0.17	0.17	0.16	0.16	0.16	30.06	30.07	30.07	30.20	30.38	30.56	1.04
114.75	19.50	0.22	0.25	0.24	0.22	0.22	0.22	34.45	34.49	34.27	33.99	33.83	33.59	1.07
324.25	19.70	0.50	0.55	0.53	0.52	0.53	0.56	44.65	44.61	44.25	43.90	43.91	43.34	1.06
743.25	18.70	0.28	0.31	0.30	0.29	0.29	0.29	51.19	50.50	50.16	50.65	51.69	52.47	1.06
952.75	18.20	0.31	0.33	0.33	0.31	0.32	0.33	40.75	40.80	40.97	40.97	40.93	40.95	1.11
1581.25	18.00	0.46	0.48	0.47	0.46	0.48	0.49	42.58	42.59	43.94	43.77	44.36	44.17	1.13
2000.25	17.10	0.46	0.48	0.47	0.46	0.46	0.47	45.46	45.57	45.73	45.48	46.14	45.28	1.12
2524.00	14.40	0.40	0.42	0.41	0.42	0.43	0.44	53.15	53.72	52.19	53.17	52.67	53.67	1.12
3047.75	14.20	0.45	0.48	0.47	0.46	0.46	0.49	52.46	52.25	51.55	51.33	51.46	50.99	1.09
3676.25	15.10	0.73	0.74	0.75	0.75	0.75	0.75	46.32	47.19	46.36	45.53	46.19	45.65	1.07
4200.00	17.90	1.04	1.07	1.07	1.06	1.05	1.06	28.42	28.36	28.24	28.14	28.01	27.92	1.09
4502.50	-0.60	1.17	1.19	1.18	1.19	1.17	1.16	28.15	28.10	28.05	27.96	27.84	27.87	1.14
4802.00	-0.70	1.26	1.26	1.27	1.25	1.22	1.20	37.95	38.01	38.19	37.93	37.58	37.51	1.12
5251.75	-1.10	1.19	1.17	1.16	1.13	1.11	1.09	49.68	51.04	49.12	49.37	49.13	48.19	1.11
5550.75	-2.00	1.65	1.63	1.60	1.56	1.54	1.51	38.44	38.56	38.36	38.07	37.85	38.19	1.10
6000.00	-2.40	1.70	1.71	1.65	1.59	1.54	1.50	34.37	34.36	34.23	34.40	34.49	34.48	1.12

Electrical Schematic



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IF/RF MICROWAVE COMPONENTS

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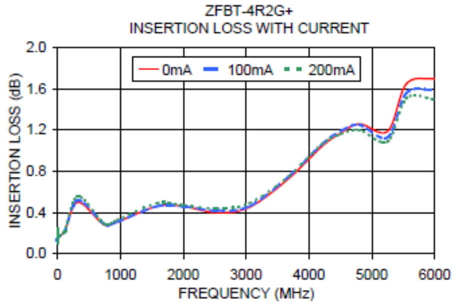
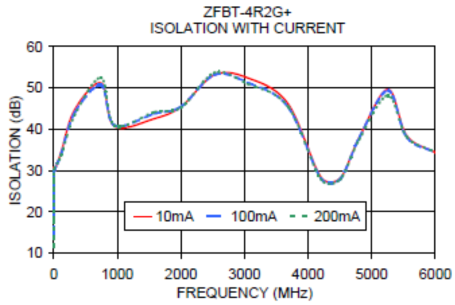
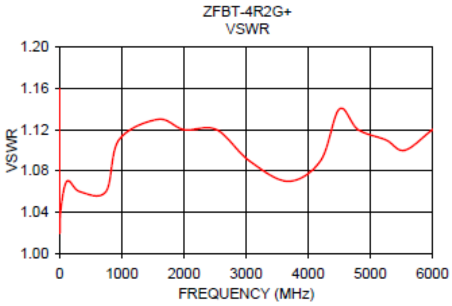
Page 1 of 2

Performance Charts

ZFBT-4R2G+







III.7. Balun. *Model BIB-100G, Prodyn*

DATA SHEET

PRODYN BALUNS

PRODYN baluns are bilateral, high performance, balanced to unbalanced passive converters. All three ports exhibit an excellent TDR (low VSWR) and the two differential ports are well isolated each from the other. These two features are of importance when using the unit with unmatched sources such as D-Dot (open circuit source) or B-Dot (short circuit source) when maximum clear time is desired. Also, the PRODYN baluns can be ordered with optional lead x-ray shielding.

ELECTRICAL SPECIFICATIONS:

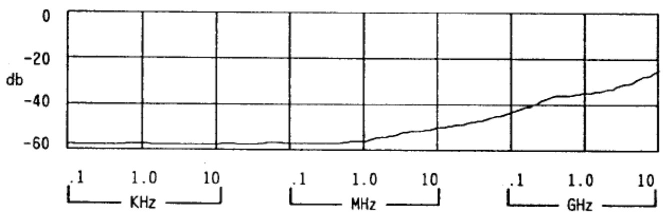
TYPE

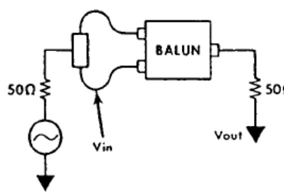
	A	B	C	D	E	F	G	HV*
Bandwidth (3db)	10 KHz - 250 MHz	15 KHz - 400 MHz	20 KHz - 600 MHz	22 KHz - 1.4 GHz	50 Hz - 150 MHz	200 KHz - 3.5 GHz	250 KHz - 10 GHz	200 KHz - 3 GHz
Risetime (10-90%)		Pulse risetime approximates specified CW bandwidth						
Insertion Loss (Nominal)	6 db	6 db	6 db	6 db	6 db	8 db	8 db	8 db
Propagation Delay ns (Nominal)	3.2	2.2	1.9	1.4	5.3	.6	.6	.6
Max Input Voltage (50 ns Duration)	1000 V	1000 V	1000 V	1000 V	1000 V	1000 V	1000 V	5000 V
Common Mode Rejection Ratio(db) See Graph Below	≥ 32	≥ 32	≥ 30	≥ 30	≥ 36	≥ 28	≥ 20	≥ 28
Port Impedance (3 Ports)	50	50	50	50	50	50	50	50

** This balun is equipped with type 'HN' connectors only, to accommodate high voltage.*

COMMON MODE MEASUREMENT (Typical)

$$CMRR = 20 \text{ Log } \frac{V \text{ out}}{V \text{ in}}$$





CONNECTOR OPTIONS

CONNECTOR TYPES

MODEL No.	INPUT	OUTPUT
BIB-100	SMA (Female)	SMA (Female)
BIB-101	SMA (Male)	SMA (Male)
BIB-110	GR (Twinax, TCC type)	GR (Locking)
BIB-120	Type 'N' (Female)	Type 'N' (Female)
BIB-125	Type 'N' (Female)	SMA (Female)
BIB-130	Twinax (Amphenol - 22950)	Type 'N' (Female)
BIB-135	GR (Twinax, TCC type)	Type 'N' (Female)
BIB-140	Type 'N' (Female)	Type 'N' (Male)
BIB-150	GR (Twinax, TCC type)	GR (Locking)
BIB-160	GR (Twinax, TCC type)	SMA (Female)
BIB-170	SMA (Female)	Type 'N' (Female)
BIB-180	BNC (Female)	BNC (Female)
BIB-190	TNC (Female)	Type 'N' (Female)
BIB-200	HN (Female)	HN (Female)

HOW TO ORDER: Example: A 20 KHz to 600 MHz Balun with Type 'N' Female connectors on input and output will have the following model Number: BIB-120C

Connector — Bandwidth Option

NOTE: Housing size may vary on bandwidth and connector option.

Special Bandwidth and/or connector options can be manufactured for a small additional charge. Please consult current price list and factory for details.

Anexo IV

Publicaciones del autor

IV.1. Introducción

IV.2. *"Low-Cost TIA and Equalizer For SI-POF"*. 19th International Conference on Plastic Optical Fibers

IV.3. "*1.8V - 3GHz CMOS Limiting Amplifier with Feedforward Frequency Compensation*". Microelectronics Reliability

IV.4. *"A 0.18 µm CMOS Integrated Transimpedance Amplifier-Equalizer for 2.5 Gb/s*". IEEE International Midwest Symposium on Circuits and Systems

En este anexo se presentan las publicaciones en las que ha colaborado el autor y relacionadas con el proceso de elaboración de este PFC.

IV.1. Introducción

Autores: I. Lope, J. Mateo, J. M. García del Pozo, J. Urdangarín and S. Celma.
Título: *Low-Cost TIA and Equalizer For SI-POF.*
Congreso: 19th International Conference on Plastic Optical Fibers. Yokohama, Japan, 2010.
Referencia: [LOP10].

Autores: J. M. García del Pozo, S. Celma, A.Otín, I. Lope and J. Urdangarín.
Título: *1.8V - 3GHz CMOS Limiting Amplifier with Feedforward Frequency Compensation*
Revista: Microelectronics Reliability, 2010.
Referencia: [GAR10].

Autores: F. Aznar, S. Celma, B. Calvo and I. Lope.
Título: *A 0.18 µm CMOS Integrated Transimpedance Amplifier-Equalizer for 2.5 Gb/s*.
Congreso: IEEE International Midwest Symposium on Circuits and Systems. Seattle, 2010.
Referencia: [AZN10].

Low-Cost TIA and Equalizer for SI-POF

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Abstract: This paper presents an analog front-end suitable for low-cost POF systems compatible with the standard IEEE 1394b. The proposed front-end includes a Si PIN photodiode, a transimpedance amplifier and a differential equalizer.

1. Introduction

A great interest has emerged in the use of plastic optical fibers (POFs) for data transmission systems. The low cost of manufacture and maintenance of such systems makes them very attractive for the consumers. For this reason, recently the standard IEEE 1394b includes the requirements of a POF system in local area networks [1].

The analog receiver front-end appears as one of the most important blocks because it sets the network performance. Given this consideration, in the last years several alternatives of analog front-ends have been reported, [2-4]. In all these proposed designs the conventional architecture includes a low cost silicon photodiode (PD), a transimpedance amplifier (TIA) and a continuous-time equalizer (EQ).

Precisely in this work, a complete analog front-end is presented. In section 2, the design of the front-end is introduced. In section 3, the results will be shown, and at the end, the main conclusions will be drawn.

2. Design of the front-end

2.1 Fiber and photodiode

In order to implement a suitable analog front-end, the designer needs to know the signal transmission and detection characteristics of the fiber and the photodiode, respectively.

Taking into account the strong dependence of the fiber bandwidth on the length, the first step was to measure the bandwidth of the POF (ESKA Premier GH 4002 2.2 mm) with lengths of 10, 20 and 30 m. It was tested following the approach reported in [5]. The results are shown in Fig. 1.

The choice of the photodiode represents the second critical design criterion. Nevertheless, if the aim is a low cost system, silicon photodiodes is the best option. In our case, a S5972 Si PIN Photodiode (Hammamatsu) has been selected.

To get a good characterization of the photodiode, an analysis was made of its depletion capacitance, C_{PD}, versus the reverse bias voltage, V_{REV}. This analysis is shown in Fig. 2. These results show that for $V_{REV} \geq 1.5$ V, the value of C_{PD} remains almost unchanged in 3 pF.

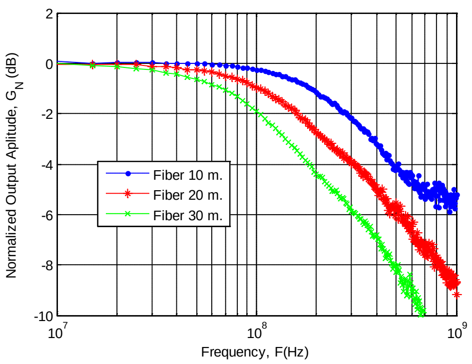

Fig.1. Frequency response of the POF GH 4002 with different lengths.

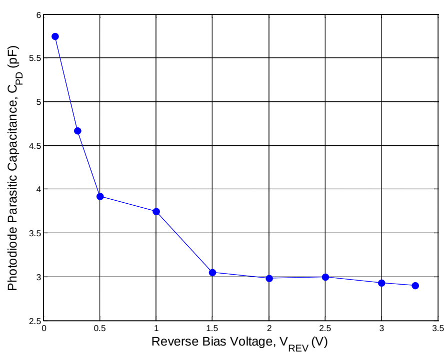

Fig. 2. Photodiode capacitance as a function of the reverse voltage.

2.2 Transimpedance amplifier

In this work, a shunt-feedback TIA designed with a passively loaded bipolar transistor is proposed. The structure is depicted in Fig. 3.

As shown in this figure, an input matching network is also included. This is based on a bias resistor, R_{PD} = 2 kΩ, and a decoupling capacitor, C_D= 22 nF. The resistor value is calculated for reduced impact in the frequency response and the capacitor avoids the pernicious DC offset input current. One important design condition is $R_{PD} >> Z_{in}$ where Z_{in} represents the input impedance and whose value is around 100 Ω.

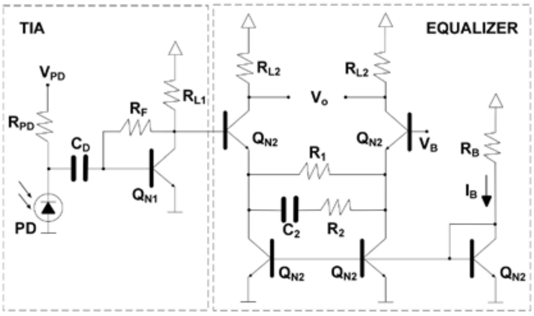

Fig. 3. Schematic of the proposed front-end.

The transistor Q_{N1} is the key device in this input block. The transresistance, the bandwidth and the noise, fundamental specs in a TIA, depend strongly on it. The optimization of this transistor is done in two different ways: First, choosing proper commercial devices and then maximizing the channel capability in the Shannon sense.

In this work, a BFP640 NPN Silicon Germanium RF Transistor, with packaging SOT343 (Infineon), is selected for the implementation of Q_{N1}. This transistor has a transition frequency of 40 GHz. This transition frequency guarantees as main frequency limitation the photodiode depletion capacitance, which has been well characterized in the previous section.

Shannon´s equation in [6] allows obtaining the expression of the TIA capability, C, given by:

$$C = BW \cdot \log_2\left(\frac{i_{in} + \left(\bar{i}^2_{n,TIA}\right)^{\frac{1}{2}}}{\left(\bar{i}^2_{n,TIA}\right)^{\frac{1}{2}}}\right) \tag{1}$$

where BW, i_{in} and $i_{n,TIA}$ represent the bandwidth, the input signal amplitude and the input-referred noise, respectively. Applying small-signal models for each device of the TIA, analytical are obtained:

$$T_R \approx (\beta \cdot R_{L1}) \| R_F \tag{2}$$

$$BW \approx \frac{1}{2\pi \cdot \left(\frac{C_{in}}{\beta} + C_{bc}\right) \cdot T_R} \tag{3}$$

$$\bar{i}^2_{n,TIA} \approx \left(\frac{4kT}{R_F} + \frac{2qI_C}{\beta}\right) BW_n \tag{4}$$

In these equations T_R represents de transresistance of the TIA, β is the current gain of the bipolar transistor Q_{N1}, C_{in} is the input parasitic capacitance of the TIA and C_{bc} is the base-collector capacitance. C_{in} includes the PD depletion capacitance, C_{PD}, the base-emitter capacitance, C_{be}, and the parasitic capacitance of the track, C_{TRACK}. Similarly, I_C is the collector current and $BW_n = 1.1 \cdot BW$ is the effective white noise bandwidth. The rest of the magnitudes have the conventional meaning, [7-8].

All the previous intrinsic magnitudes have dependence on the bias current. These dependences are quite complicated in some cases, and for this reason the value of each magnitude is directly extracted from the simulator. Keeping in mind this fact, the theoretical results of the normalized capability of the proposed TIA are those shown in Fig. 4.

In these results, the biasing was defined in each point for optimum output dynamic range and for optimum bias point of the next stage (the equalizer). For this reason, given a specific bias current, resistors R_F and R_{L1} in Fig. 3 were calculated to set V_{CE} to 1.75 V. Similarly, another factor which must be taken into account is that the input current is around 1 µA.

Although the optimum capability is obtained within I_C = 40 mA, our definitive choice was I_C = 30 mA, R_F = 4 kΩ and R_{L1} = 50 Ω. These values are chosen for two reasons: 1) the proper output matching impedance is obtained and 2) the C improvement between the two previous currents does not justify the increase in the power consumption. Final calculated specs are: $T_R \approx$ 70 dBΩ, BW≈ 251 MHz and $i_{n,TIA} \approx$ 125 nA_{rms}.

2.3 Equalizer

The proposed equalizer is shown in Fig. 3. It is based on a bipolar degenerated pair with a RC compensation network. All bipolar transistors are implemented by using a commercial HFA3127 NPN bipolar array with package SOIC (Intersil). In this way, a good tracking between paired transistors is obtained achieving a better differential response. The transition frequency is 8 GHz.

The optimization of the equalizer capability mainly implies the optimization of the frequency response. However, given the signal levels required by the limiting amplifier (next block in the receiver), certain gain factors must be guaranteed. The simulated results of the equalizer capability as a function of the bias current are shown in Fig. 5.

Again, the biasing was defined in each point to obtain the optimum output dynamic range. For this reason, given a specific bias current, the optimum R_{L2} was calculated to set the DC output level to 1.75 V.

Although the optimum capability is obtained within I_C = 50 mA, to reduce the power consumption and to get an output matching impedance (R_{L2} = 50 Ω) I_C = 30 mA was chosen. These values provide a gain G ≈ 17 dB and a minimum BW ≈ 600 MHz (without equalization network).

Once the pair is optimized, the RC compensation network must be designed. Equation (5) presents the equalizer transfer function where the dependence on the intrinsic parameters is shown. The parameter r_{be} represents the base-emitter resistance. The transfer function has in first order approximation a zero and a pole.

$$H(s) \approx \frac{\beta R_L}{r_{be} + (\beta+1)R_1} \cdot \frac{1 + sC_1(R_1 + R_2)}{1 + s\dfrac{C_1\left(r_{be}(R_1+R_2) + (\beta+1)R_1R_2\right)}{r_{be} + (\beta+1)R_1}} \tag{5}$$

In order to get a well designed equalizer an iterative process based on comparison between theoretical and experimental results is employed. In this work, the network is changed manually by simple manipulation of the PCB. In the definitive version the change of the compensation network will be done electronically by means of an ADG904 digital RF switch array (Analog Devices). The final network values will be shown in the next section.

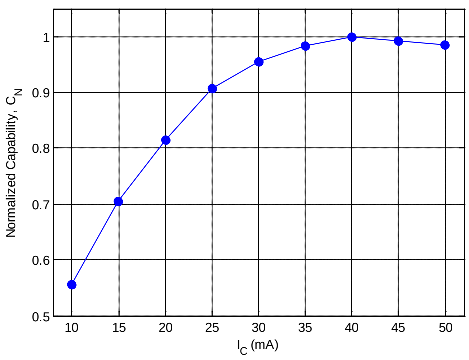

Fig. 4. Normalized TIA capability as a function of the bias current.

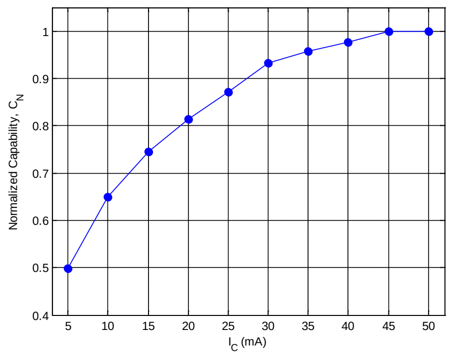

Fig. 5. Normalized equalizer capability as a function of the bias current.

3. Experimental results

The proposed design was mounted in a double-sided PCB, see Fig. 6. One of these sides is a uniform ground plane where the PD is soldered (bottom). The other is used for signal and supply routing (top). The whole system power consumption is 396 mW with a single 3.3 V supply voltage.

Our test circuit includes another PCB where a DL3149-057 red laser diode (Sanyo) with a 50Ω matching network is employed. This test laser is routed by using a bias-T ZFBT-4R2G+ (Minicircuits).

The results in Fig. 7 correspond to the frequency response of the whole circuit measured with a ZVL 6 GHz network analyzer (R&S). This analysis considers different fiber lengths with the adequate compensation network. These results are compared with those obtained when no equalization is made. This comparison shows a bandwidth enlargement between 3.7 and 4.6 times, depending on the fiber. It is quite interesting to note that the output cut-off frequency is almost constant despite of the variable input cut-off frequency. This confirms the proper system operation.

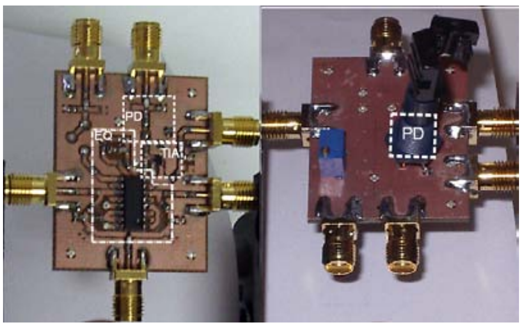

Fig. 6. Whole proposed analog front-end.

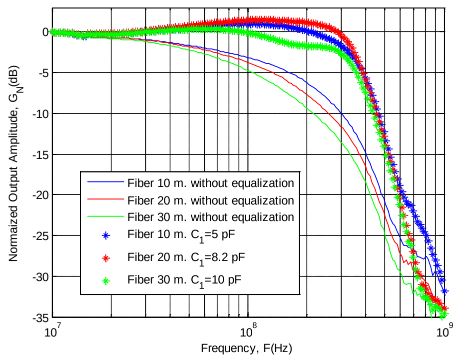

Fig. 7. Frequency response of the analog front-end.

Fig. 8, 9 and 10 show the experimental eye diagrams of the whole circuit measured with an Infiniium DCA-J 86100C digital communications analyzer (Agilent) and a N4906A bit error rate tester (Agilent). All results consider a 2^{31}-1 non-return to zero pseudorandom bit sequence (NRZ PRBS) at 800 Mb/s and the same transmitted optical power. Eye diagrams show a variation in the eye opening from 3 mV to 24 mV, obtaining the smallest result with the fiber of 30 m. Nevertheless, all cases achieve a BER lower than 10^{-12}. The worst jitter is 170 ps_{rms} for the fiber of 30 m.

Fig. 11 presents the output noise distribution as a function of the 1/0 logical state. The maximum experimental noise contribution is detected when the state is 1 achieving 614 μV_{rms} while our theoretical models predict 410 μV_{rms}.

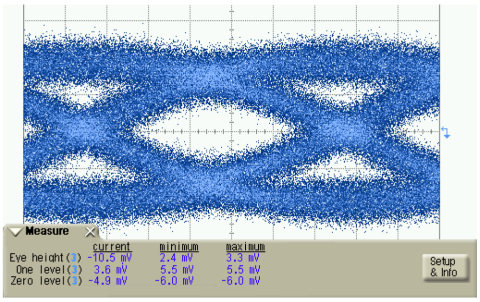

Fig. 10. Eye diagram at 2^{31}-1 NRZ PRBS. R_1=220 Ω, R_2 = 5Ω, C_2 = 10 pF, 30 m fiber length and 800 Mb/s.

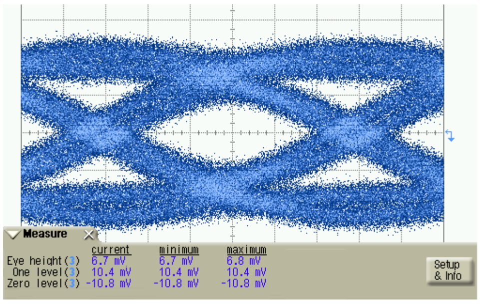

Fig. 10. Eye diagram at 2^{31}-1 NRZ PRBS. R_1=220 Ω, R_2 = 5Ω, C_2 = 8.2 pF, 30 m fiber length and 800 Mb/s.

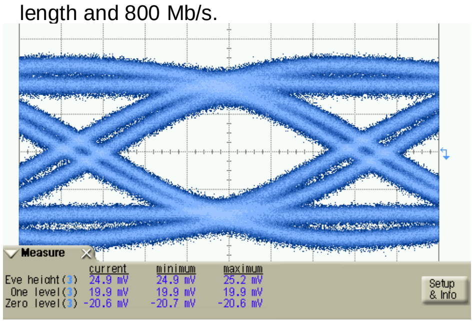

Fig. 10. Eye diagram at 2^{31}-1 NRZ PRBS. R_1=220 Ω, R_2 = 5Ω, C_2 = 5 pF, 10 m fiber length and 800 Mb/s.

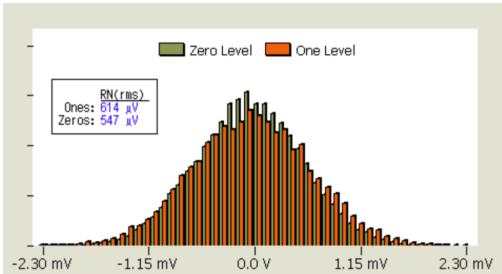

Fig. 11. Output rms noise distributions.

4. Conclusions

This paper has presented an analog front-end suitable for low-cost POF systems in the standard IEEE 1394. The proposed front-end includes a Si PIN photodiode, a transimpedance amplifier and a differential equalizer. The analog front-end has been designed in bipolar technology with supply voltage of 3.3 V. The whole system consumes 396 mW, achieves a total gain of 70 dBΩ and operates up to 800 Mb/s. At this bit rate and with fiber lengths up to 30 m, the circuit has a BER $\leq 10^{12}$ and a maximum jitter of 170 ps_{rms}.

Acknowledgements

This work has been supported by MICINN (TEC2008-05455/TEC, TEC2009-14718-C03-02) and DGA (PI127/08).

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1.8 V–3 GHz CMOS limiting amplifier with efficient frequency compensation

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ABSTRACT

A compact robust CMOS limiting amplifier (LA) for high data traffic optical links is presented in this work. The core considers two different blocks. First, four common-source inverter amplifiers are included, which optimize the gain-bandwidth product of the structure. And second, two additional compensation stages are placed strategically between the gain stages alleviating the pernicious load effect. These stages develop two different compensation techniques simultaneously thus increasing the bandwidth. The proposed design consumes 113 mW with a single 1.8 V supply. It achieves a cut-off frequency up to 3 GHz and provides a gain of 21 dB. The circuit is packaged in a QFN24 and mounted on a commercial FR4 PCB.

1. Introduction

The receiver front-end is one of the key building blocks in an optical network. This module faces the signal conversion from optical to electrical and the signal conditioning. This is usually achieved in the analog domain while the digital circuitry is kept for data recovery and processing. As Fig. 1 shows, an analog front-end includes three sub-blocks: the photodiode, the preamplifier (Pre) and the postamplifier (Pos) [1].

The postamplifier exhibits large gain and high bandwidth as the strongest design criteria. The postamplifier noise can be discarded and this is because the most relevant noise contribution in an optical receiver is associated to the photodiode and the preamplifier [2].

Two common postamplifier topologies are the variable gain amplifier and the limiting amplifier. However, the use of limiting amplifiers offers several advantages, such as higher operating speeds, lower voltage supply and power consumption, easier design in terms of stability and complexity, smaller area and simpler monolithic implementation [3,4]. For this reason we have chosen this postamplifier topology.

Limiting amplifiers (LAs) are open-loop non-linear systems which provide voltage gain, thereby increasing the signal amplitude between two logical states [5]. They normally consist of two basic building blocks: the core and the DC offset compensation circuit (DCCC). The block diagram of the whole limiting amplifier is shown in Fig. 1. The core employs a cascade of N amplifiers which are fully optimized for gain and bandwidth. The DCCC works as a DC feedback loop detecting the offset at the output and correcting it at the input. This second block increases reliability by avoiding mismatch and temperature errors [6].

The optimal value of N depends on the topology of each amplifier. The basic implementation of a core was well described in [7]. In that case, each amplifier was designed as a differential pair optimizing the gain-bandwidth product. Nevertheless, this simple implementation has a serious drawback: a strong bandwidth dependence on the technology. This phenomenon has its origin in the load effect between stages. A possible solution is to select a more advanced and more expensive CMOS process.

Other solutions without resorting to more sophisticated technologies have been reported to alleviate this setback. The first one is based on the downscaling technique [8]. The structure also consists of N amplifiers but in this case each amplifier is scaled with respect to its predecessor. This technique slightly reduces the load effect, but the problem remains.

Another compensation technique is the well-known passive shunt-peaking [9]. This technique increases the bandwidth by generating a peak in the frequency response. The main drawback with this alternative is precisely the use of N passive inductors. These devices present low levels of reliability and accuracy, low quality factors and require a lot of area.

Other authors use the so-called multi-feedback technique. In this case, N amplifiers are employed which include feedback loops either in the same stage or between different stages. For example, [10] reports a feedback loop which uses capacitors that implement a negative capacitance in each stage. In another case, feedback loops between different stages are proposed [11]. This aims for a peak effect like that obtained in the previous technique. However, the multi-feedback technique suppresses several of the most important advantages of limiting amplifiers, i.e., stability and simplicity.

In the present work, the effort is concentrated on the design of a limiting amplifier with a new compensation technique which

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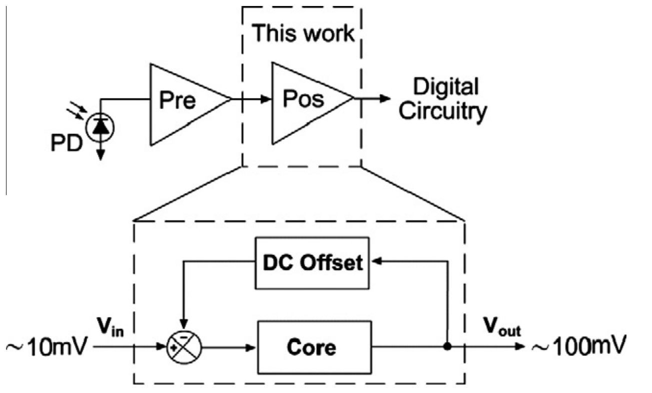


Fig. 1. Optical receiver architecture and the implementation of the postamplifier as a limiting amplifier.

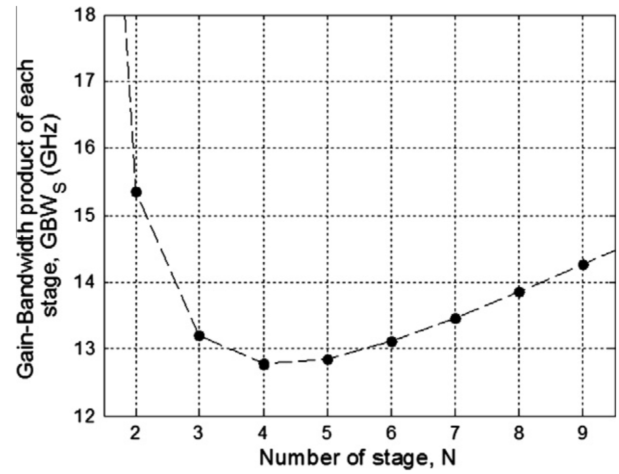


Fig. 2. Gain-bandwidth product as a function of the number of stages.

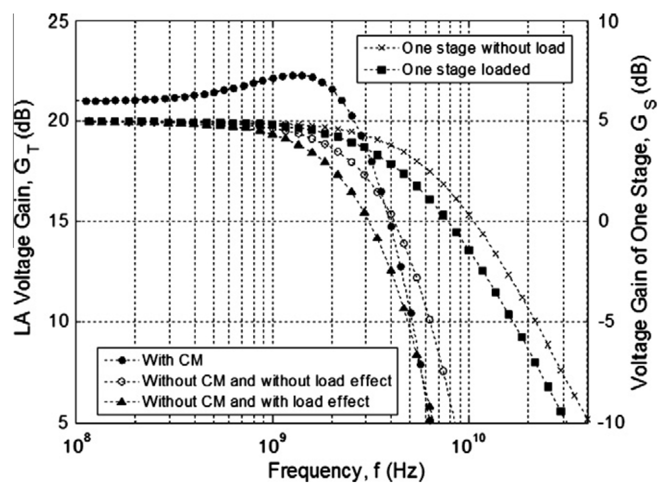


Fig. 3. Postlayout frequency response in different steps of the design process.

avoids all the previous reported drawbacks. Section 2 presents the proposed limiting amplifier describing in detail the whole design process. In Section 3, the results are analyzed. And finally, conclusions are drawn in Section 4.

2. Proposed limiting amplifier

The design process begins by considering common-source (CS) inverter cells implementing each amplifier. The main advantages of these simple topologies are the low-voltage operation and the large bandwidth. Other important benefits are two requirements for reliability: stability and predictable behavior for any operating condition. If N identical inverter amplifiers with no load effect between stages are placed in cascade, the gain-bandwidth product of each amplifier stage (GBW_s) can be expressed as a function of the cut-off frequency, f_c, and the voltage gain, G_T, of the whole limiting amplifier:

$$GBW_s = (G_T)^{\frac{1}{N}} \frac{f_C}{\sqrt{2^{\frac{1}{N}} - 1}} \tag{1}$$

In such a configuration, an approximated expression of N which optimizes GBW_s, N_{opt}, is reported in [12] which is valid when $G_T \gg \sqrt{2}$:

$$N_{\text{opt}} \approx 2\ln(G_T) \tag{2}$$

The voltage amplitude at the output of the preamplifier is around 10 mV and the amplitude at the output of the LA should be around 100 mV. Obviously, this means a total gain G_T of 10 (20 dB). Considering this fact and the Eq. (2), the optimum value of the number of stages is $N_{\text{opt}} = 4.61$. However, N must be an integer number. Thus, a choice between 4 and 5 stages must be made. The final choice of four stages is based on the proposed compensation technique which is explained later.

Given a standard with a specific bit rate, the bandwidth of the LA must be equal to or higher than the fundamental frequency of the data stream [13]. So, if the bit rate is 3 Gb/s, the bandwidth must be set at $f_c = 3$ GHz. If this criterion and the expression (1) are taken into account, the optimal gain-bandwidth product of each actively loaded inverter cell should be $GBW_{s,\text{opt}} \approx 12$ GHz. Using four stages, the gain (G_s) and the bandwidth (BW_s) per stage should equal 1.8 and 6.7 GHz, respectively. All these previous considerations are also deduced from the theoretical results of Fig. 2.

Common-source stages can be implemented in two different ways, actively or passively loaded. Actively loaded CS amplifiers usually present higher gains, larger output swings and more compact designs. For these reasons, actively loaded stages have been chosen. In the proposed CS stages the active loads are implemented with PMOS transistors working solely as DC bias current sources. This means that the signal is processed only by NMOS transistors which achieve transition frequencies higher than PMOS transistors making the circuit faster.

However, the load effect between stages has been neglected in our approach. This assumption must be checked. The results in Fig. 3 shows the impact of this effect on one stage and on the whole structure when the core is implemented with transistors. The curves with higher bandwidth incorporate an ideal voltage buffer with unity gain between stages providing isolation. Nevertheless, the responses with lower cut-off frequency do not incorporate this ideal buffer and therefore suffer the load effect. A bandwidth reduction of up to 16% can be observed and, obviously, the required frequency performance is not reached.

In this work, an efficient way of frequency compensation is suggested, which alleviates this load effect, retaining all the original advantages of the simpler core based only on N CS stages. Let us now show the proposed core of the LA which is depicted in Fig. 4.

This topology is unconventional due to the inclusion of another two identical compensation stages (CM). One is placed between the first two amplifiers. Similarly, another CM stage is placed between the other two amplifiers. These compensation stages are based on two NMOS transistors. The upper transistor is biased by a resistor connected between the supply and gate terminals, R_i. This resistor is basically idle in the DC operating point because

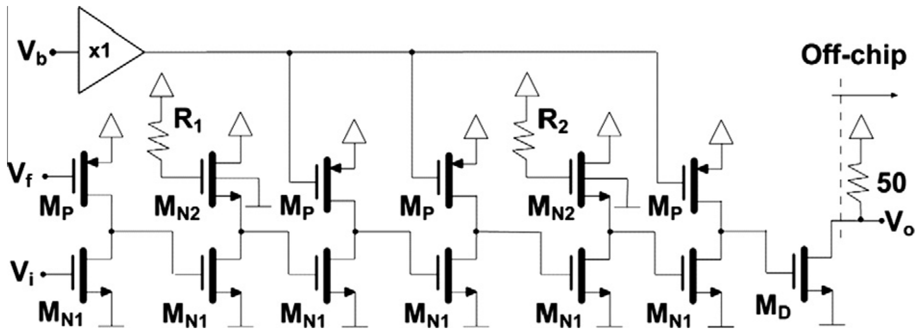


Fig. 4. Proposed core of the LA.

there is no current flow across, so the gate voltage of the upper transistor equals V_{DD}. However, it plays a very important rule in the proposed frequency compensation. This can be understood by analyzing the simplified models of each stage of the core.

Actively loaded CS stages, which provide the main gain contribution, can be modelled by a first order transfer function [14]:

$$H_{CS,i}(s) \approx \frac{-g_{N1} r_{oN1}}{sC_O r_{oN1} + 1} \tag{3}$$

where g_{N1} is the M_{N1} transconductance, r_{oN1} is the M_{N1} output resistance and C_O is the output load capacitance of the stage. Similarly, taking into account the load effect it can be demonstrated how the CM stages can be modelled by a second order transfer function which has one zero and two poles [15]:

$$H_{CM,i}(s) \approx \frac{\frac{-g_{N1} r_o}{g_{N2} r_o + 1}(1 + sC_{gsN2} R_i)}{s^2 \frac{C_O C_{gsN2} r_o R_i}{g_{N2} r_o + 1} + s \frac{C_O r_o + C_{gsN2}(r_o + R_i)}{g_{N2} r_o + 1} + 1} \tag{4}$$

where the variable r_o denotes the parallel equivalent resistance between of r_{oN1} and r_{oN2}, and C_{gsN2} is the gate-source parasitic capacitance of M_{N2}.

In these two expressions, the contributions of the bias PMOS transistors are neglected. This approximation may seem tough. However, it is justified because the most important frequency contribution is made by the parasitic C_{gs} of the NMOS transistors. Now, consider two groups of amplifiers formed each of them by two CS stages and a CM stage. The resulting transfer function of the LA core is given by:

$$H_C(s) = \prod_{i=1}^{2} H_{CS_i}(s) \cdot H_{CM_i}(s) \cdot H_{CS_i}(s) \tag{5}$$

Taking Eqs. (3)–(5) into account, an understanding can be obtained of how the proposed structure works. By using the correct sizes of NMOS transistors (M_{Ni}) and polysilicon resistors (R_i), two different frequency compensations are achieved simultaneously. Initially, the zero of the CM stage cancels the pole of the first CS stage. And finally, the second order transfer function provides a shunt-peaking effect. This effect compensates the drop in the frequency response due to the second CS stage. This approach is reproduced in the three last stages.

Note that no extra passive devices such as inductors are used. This makes the design more compact and robust than other previous structures based on passive inductors [9]. The topology maintains the minimum voltage supply condition. The use of only two CM stages barely increases the power consumption. And finally, the structure presents no physical feedback loop, thus ensuring stability.

In the proposed LA, the bias voltage V_f fixes the quiescent current of the input stage. This voltage is the error signal provided by the DC feedback loop. The bias voltage V_b fixes the rest of the bias currents. In this prototype V_b is externally adjustable for test purposes. The voltages V_f and V_b are identical in the absence of DC drifts. Another design criterion is imposed. A bias point where $V_{GS,MN} = V_{DS,MN} \approx 1$ V must be set to simplify the biasing circuitry, achieve a large output swing and obtain a better matching between NMOS transistors.

DC compensation circuits are usually designed using RC networks and error amplifiers. A MOS transistor operating in the triode region works as high value resistor. A MOS capacitor operating in strong inversion implements the other network device. Together, they make it possible to achieve lower cut-off frequencies with no external devices, obtaining a fully integrated implementation [6]. In Fig. 5, M_R and M_C form the MOS RC network. The passively loaded CS stage works as an error amplifier fixing the DC loop gain (~20 dB) and also operating as a DC level shifter. The bias voltage V_{ref} is set manually for testing purposes. The entire LA including the DCCC has a low cut-off frequency of around 300 kHz.

The results reported in Fig. 6 shows the output DC level dependence on temperature in two cases, with and without the DC com-

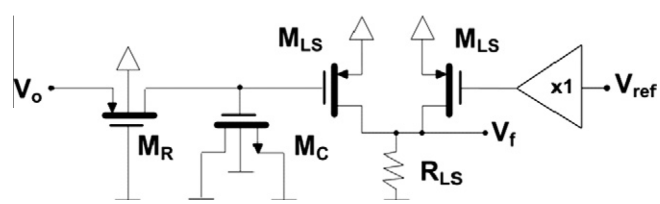


Fig. 5. Proposed DCCC of the LA.

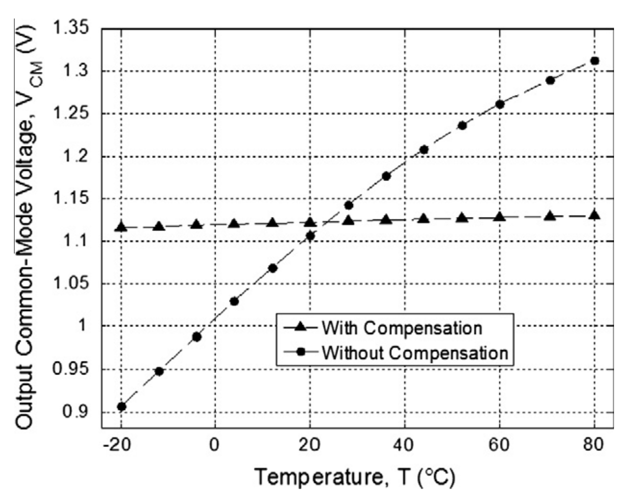


Fig. 6. DC output level as a function of temperature.

pensation circuit. The range of simulated temperatures is from −20 °C to 80 °C. The obtained results show an obvious improvement setting the thermal sensitivity at 0.2 mV/°C. This reduces the original value by 95%.

3. Experimental results

The limiting amplifier was fabricated in a low-cost 180 nm CMOS process. The prototype includes ESD protection circuits and an open drain based driver. The total power consumption is 113 mW at 1.8 V single supply voltage (including LA and test blocks). Table 1 summarizes the values of the main circuit devices. The total active area is 140 × 80 μm^2. Fig. 7 shows the die photo.

The buffers included at the input of the DC bias voltages V_b and V_{ref} (see Figs. 4 and 5) isolate the off-chip and on-chip parts. Nevertheless, in a definitive analog front-end IC, the bias voltages will be generated by means an internal bandgap reference. The die was enclosed in a QFN24 package and mounted on a FR4 PCB, guaranteeing low cost and minimizing parasitic effects (Fig. 8). The bottom layer of the board includes the supply/bias voltage filtering networks based on a low-Q ferrite inductor (4.7 μH) and three different low ESR/ESL ceramic capacitors (1 μF, 10 nF and 1 nF). The SMD coupling capacitors of 22 nF are situated in the top layer. The same layer of the PCB also includes input and output impedances of 50 Ω realized by SMD resistors and microstrip lines. The second and third layers are uniform ground and supply planes, respectively. This configuration isolates the RF and DC planes minimizing crosstalk and avoiding instabilities [16]. The DC input level is set by using a bias-T ZFBT-4R2G+ (Minicircuits) with operation frequencies between 10 and 4200 MHz.

The supply inductor package size is SMD 1008, which supports the maximum DC current flow. On the other hand, the rest of the PCB devices are SMD 0603. This choice is for test purposes as it is small enough for parasitic effects and large enough for manipulation in the case of substitution.

All DC and RF signals are introduced by using planar SMA connectors with a flat response of up to 18 GHz. This configuration provides low EM interference, reduced insertion losses and minimum impact on the frequency response.

Table 1
Values of the main parameters of the circuit devices.

Device	Value
M_{N1}	W_{N1} = 25.0 μm L_{N1} = 0.18 μm
M_{N2}	W_{N2} = 80.0 μm L_{N2} = 0.18 μm
M_P	W_P = 45.0 μm L_P = 0.18 μm
M_D	W_D = 55.0 μm L_D = 0.18 μm
M_R	W_R = 0.24 μm L_R = 1.00 μm
M_C	W_C = 25.0 μm L_C = 25.0 μm
R_1	500 Ω
R_2	500 Ω

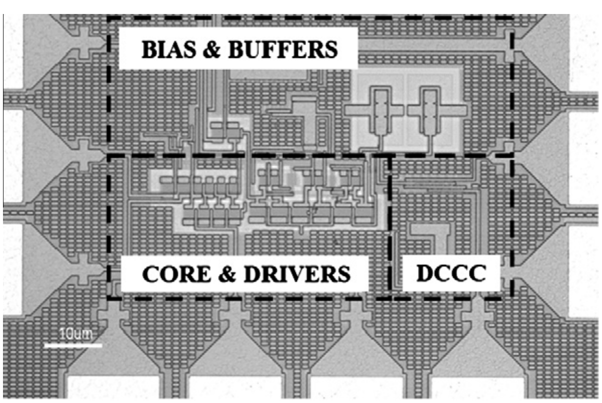


Fig. 7. Die photo of the limiting amplifier. Some circuit parts are situated beneath the passivation layer.

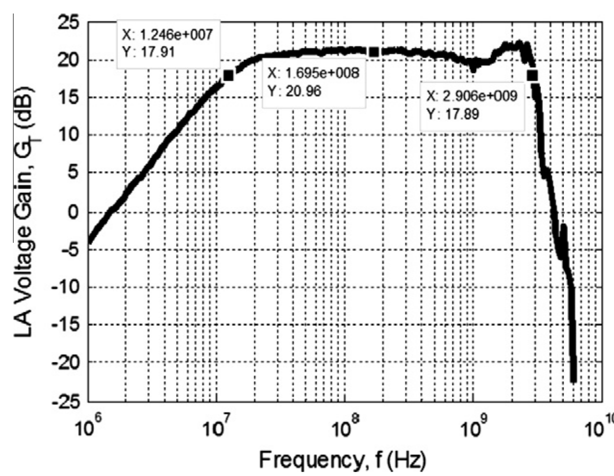
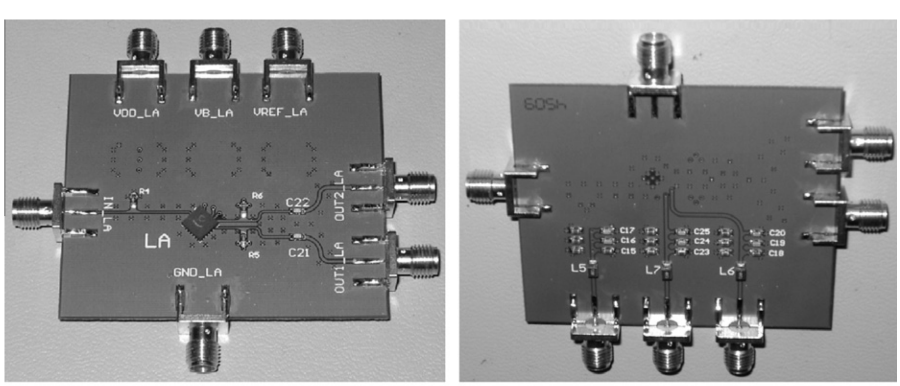
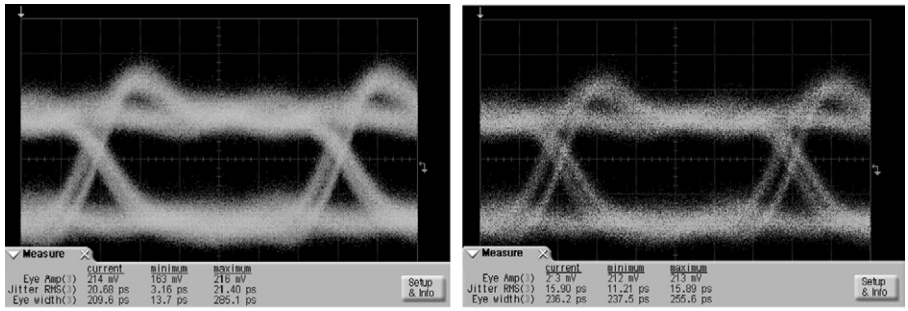


Fig. 9. Frequency response of the whole design.



(a) **(b)**

Fig. 8. Photo of the PCB with packaged LA: (a) top and (b) bottom.



(a) (b)

Fig. 10. Eye diagram of the proposed LA. Input signal, 3 Gb/s 2^{31}-1 NRZ PRBS with an amplitude of: (a) 15 mV and (b) 25 mV.

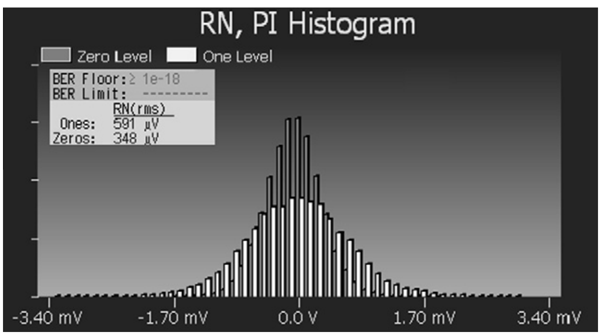


Fig. 11. Output noise as a function of the logical state. Input signal, 3 Gb/s 2^{31}-1 NRZ PRBS with an amplitude of 15 mV.

The results in Fig. 9 correspond to the frequency response of the whole PCB. This was obtained by using a ZVL 9 kHz/6 GHz (R&S) network analyzer and calculated with the expression reported in [17]. A gain of 21 dB is obtained with a bandwidth of 3.0 GHz. These experimental results differ from the simulation in the low cut-off frequency and the small drop at 1 GHz. While the cut-off frequency should be around 300 kHz, the use of the bias-T set this cut-off frequency at 10 MHz. The other difference is associated to the small fluctuations in the fabrication process of the compensation resistors.

The eye diagrams of the system with a 3 Gb/s 2^{31}-1 non-return to zero pseudorandom bit sequence (NRZ PRBS) are shown in Fig. 10. The response is evaluated with two different amplitudes, 15 mV and 25 mV. The available bit error rate tester (BERT) cannot provide lower output amplitudes than 250 mV, therefore two different attenuators of 5 dB and 20 dB have been used which operate up to 18 GHz, BW-S5W2+ and BW-S20W2+ (Minicircuits). While the eye amplitudes remain almost identical, equaling 213 mV, the total jitter is higher in the case of lower input amplitudes achieving 20 ps_{rms}.

Fig. 11 plots the output noise distribution as a function of the logical state. The worst measured values are 591 μV_{rms} and 348 μV_{rms} when the states are 1 and 0, respectively.

The analysis shown in Fig. 12 is the bit error rate, BER, as a function of the input voltage amplitude. These results show that the circuit achieves a BER $\leqslant 10^{-12}$ (error free) when $V_{in} \geqslant 14.2$ mV.

The eye diagram, noise distributions and BER curves have been measured by using the BERT N4906A (Agilent) and the digital communications analyzer (DCA) Infiniium DCA-J 86100C (Agilent).

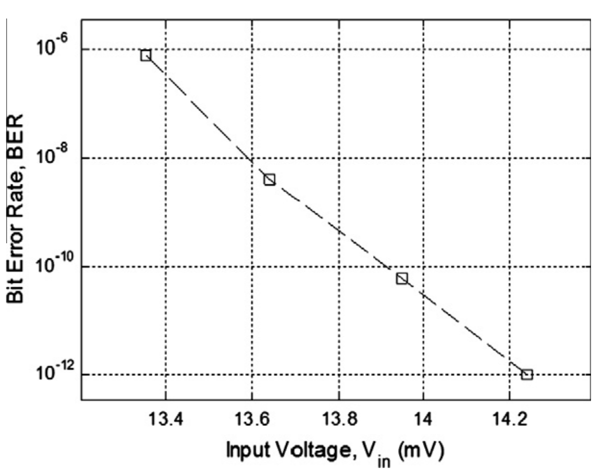


Fig. 12. BER response versus input voltage. Input signal, 3 Gb/s 2^{31}-1 NRZ PRBS.

4. Conclusions

A compact robust CMOS limiting amplifier (LA) for high data traffic optical links is presented. The core includes two different types of stages. Firstly, four common-source inverter amplifiers optimize the gain-bandwidth product providing the required gain. Secondly, two additional compensation stages are included. These stages develop two different frequency compensation techniques simultaneously: pole-zero cancellation and shunt-peaking. These alleviate the pernicious load effect thereby increasing speed with ensured stability. The LA also includes a DC compensation circuit based in a MOS RC network and an error amplifier. This DCCC which is monolithically implemented avoids mismatch and temperature problems.

The entire design was fabricated in a low-cost 1.8 V, 0.18 µm CMOS technology. It achieves an upper cut-off frequency of up to 3 GHz, and consumes 113 mW. The prototype was enclosed in a QFN24 plastic package and mounted on a FR4 PCB. It has been tested up to 3 Gb/s obtaining a BER $\leqslant 10^{-12}$ @ $V_{in} \geqslant 14.2$ mV. These results show the excellent performance of the proposed structure. They also highlight this design as a low-cost preferential consumer choice in standards 10 Gigabit Ethernet (10GE) and Synchronous Optical Network (SONET), such as 10GBase-LX4 and OC-48, respectively.

Acknowledgments

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A 0.18 μm CMOS Integrated Transimpedance Amplifier-Equalizer for 2.5 Gb/s

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***Abstract*—This paper presents a transimpedance amplifier (TIA)-equalizer combination optical receiver for 2.5 Gbit/s communications realized in a standard 180 nm CMOS process. The first stage, a transimpedance amplifier (TIA), is based on a conventional structure with an inverting voltage amplifier and a feedback resistor, but incorporates a technique to prevent the TIA saturation at high input currents. Simulation results show an optical sensitivity of 4 μA for a BER = 10^{-12} and a maximum input current of 1.5 mA_{pp}, what leads to an input dynamic range above 52 dB. The TIA is followed by an equalizer which compensate the typical frequency response of an integrated photodiode. The power consumption is 6.5 mW for the TIA and 4.1 mW for the equalizer with 1.8 V supply.**

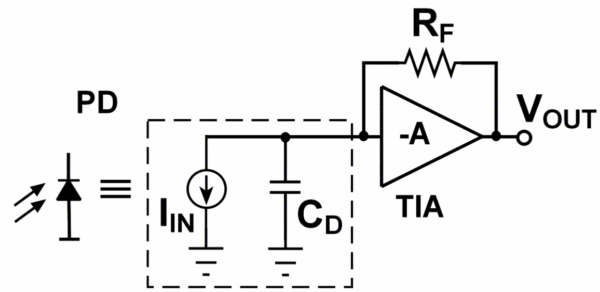

Fig. 1. Shunt-feedback TIA and photodiode model.

I. INTRODUCTION

In a typical optical receiver system, the most critical component affecting the whole system speed and noise-sensitivity is the front-end transimpedance amplifier (TIA). Therefore, many different TIA topologies have been proposed to date. The most popular is the shunt feedback amplifier, based on a voltage inverting amplifier with a feedback resistor R_F, as shown in Fig. 1. The feedback resistor directly affects the dynamic range (DR) of the TIA, defined as the ratio of maximum to minimum photocurrent that can be properly sensed. The DR can be extended by using a variable R_F to vary the transimpedance as a function of the input signal strength, taking care of introducing a method to improve control of stability and bandwidth, as both the quality factor and the bandwidth change with R_F [1]. Alternatively, to improve DR, compression of the input photocurrent can be implemented [2]. In addition, this latter technique has the advantage that prevents the TIA saturation at high input currents, which strongly degrades the pulse response of the complete optical receiver.

In addition to the photodiode response commonly modeled as shown in Fig. 1, which results in a dominant pole related to the photodiode capacitance and the input impedance of the TIA, the responsivity of an integrated photodiode also depends on the frequency: owing to slowly diffusing carriers [3], the frequency response is degraded by about 5 dB/dec from 1 MHz on. To compensate this undesirable effect, an equalizer, based on a source degenerated structure, is included after the TIA, attaining an approximately flat frequency response.

This paper presents a low-cost high speed optical receiver that includes a transimpedance amplifier, based on a previous work [4], and an equalizer to optimize the frequency response assuming an integrated photodiode. The whole design is implemented in a standard 180 nm CMOS process, achieving a data rate of 2.5 Gbit/s. The paper is organized as follows. Section II describes the proposed TIA and equalizer circuit implementations, which are the two first stages of a complete 2.5 Gb/s optical receiver. The main performances are summarized in Section III. Finally, conclusions are given in Section IV.

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II. CIRCUIT DESCRIPTION

A. Transimpedance Amplifier Architecture

To protect the TIA from saturation and improve the input current overdrive capability, the full input photocurrent range (3.6 μA – 1.5 mA) is divided into two regions: inactive and active. In the inactive region, the TIA responds linearly to the input current, while in the active region the transimpedance gain is reduced dependent on a control voltage, whereby the output voltage is still approximately linear to the input current signal.The proposed TIA, shown in Fig. 2, is formed by a three-stage inverting amplifier (N_1, P_1, N_2, P_2, N_3, R), a fixed shunt feedback resistor R_F = 5 kΩ, the transistor N_4 for carrying high photocurrents and one feedback transistor (N_5).

For the shunt-feedback TIA amplifier, a large feedback resistor is used in order to minimize its contribution (eq. 1) to the input referred noise current ($i_{noise,RF}$) achieving a good noise performance. Then, a high open-loop inverting amplifier gain A is required (eq. 2) to provide enough bandwidth (BW).

$$i_{noise,RF} = \frac{4k_B T}{R_F} \quad (1)$$

$$BW \propto \frac{A}{R_F C_D} \qquad with \qquad A >> 1 \quad (2)$$

where k_B is the Boltzmann's constant and T is the temperature. Thus, three stages are needed for the inverting amplifier to achieve enough gain A with simple common source stages, which are suitable for low voltage operation. In this design, an inverter (N_1, P_1) is used as first stage, because it shows the highest gain, hence optimizing the overall noise performance. The second (N_2, P_2) and third (N_3, R) stages are common source circuits biased with a diode connected PMOS and a resistor R, respectively. Minimal length is used in all MOS transistors to optimize frequency and noise response. The widths of the NMOS transistors are chosen for a good noise-power trade-off and the widths of the PMOS transistors and the value of the resistor are designed to keep a common-mode voltage of 0.9 V over the whole structure.

Transistor N_5 creates a current feedback path which avoids input current overload. N_4 forms a parallel current path for high photocurrents in order to be able to use a small bias current through N_1 and P_1. Both effects enhance the input dynamic range. The operation of these transistors depends on the value of their gate voltage V_C: when V_C = 900 mV, the transistors are OFF, in the denominated inactive region; when V_C > 900 mV, the transistors are ON, in the active region.

B. Transimpedance Gain

As just mentioned, the transimpedance amplifier can work in two different regions. For V_C = 900 mV, both transistors N_4 and N_5 are OFF and do not affect the TIA operation. Therefore, the input current I_{IN} flows through the feedback resistor R_F, resulting in an output voltage given by:

$$V_{OUT} = I_{IN} R_F \quad (3)$$

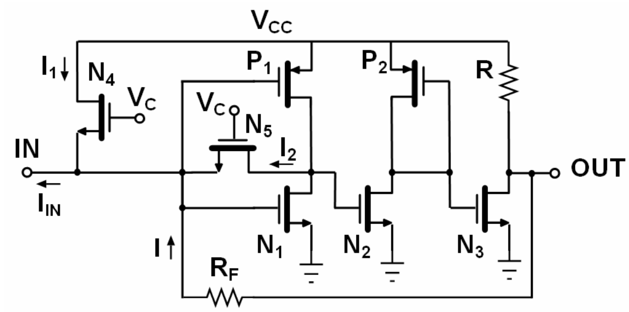

Fig. 2. Proposed transimpedance amplifier.

This linear relationship, with the selected R_F = 5 kΩ and due to the limit of output swing ($V_{CC} - V_{CM} \approx 0.9$ V), works properly for small input currents (I_{IN} < 150 μA). So, the noise and frequency performance of the inactive region determines the sensitivity of the transimpedance amplifier. When a higher input current is received from the photodiode, the TIA, to avoid overload, must work in the active region. This happens for V_C > 900 mV, when N_4 and N_5 are ON, creating two new current paths I_1 and I_2 (see Fig. 2), so that:

$$I_{IN} = I_1 + I_2 + I \quad (4)$$

Assuming some approximations [3], the output voltage can be expressed as:

$$V_{OUT} = IR_F = \left[1-\beta\left(V_C\right)\right]\left[I_{IN} - I_1\left(V_C\right)\right]R_F \quad (5)$$

where $0 \le \beta \le 1$ is a constant which depends on the control voltage. This expression shows a reduction factor $1-\beta(V_C)$ for the transimpedance and a voltage drop $-(1-\beta(V_C))\, R_F\, I_1(V_C)$. Both effects (denominated A and B, respectively) match with the simulation results as shown in Fig. 3.

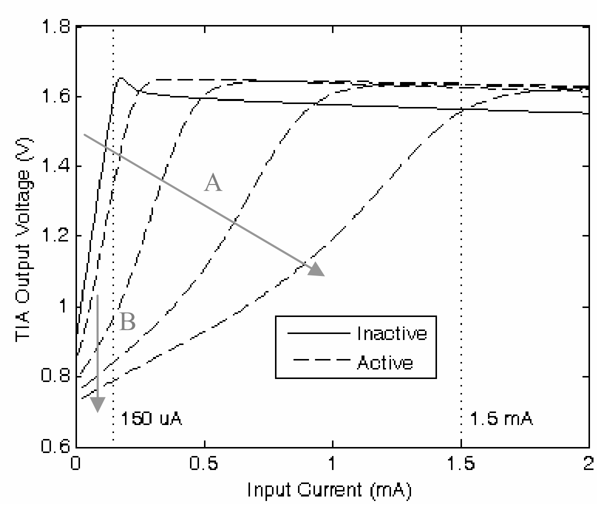

Fig. 3. DC response of the TIA over the whole control voltage swing (inactive: V_C = 900 mV, active: V_C = 1.5 V to 1.8 V, 100 mV step).

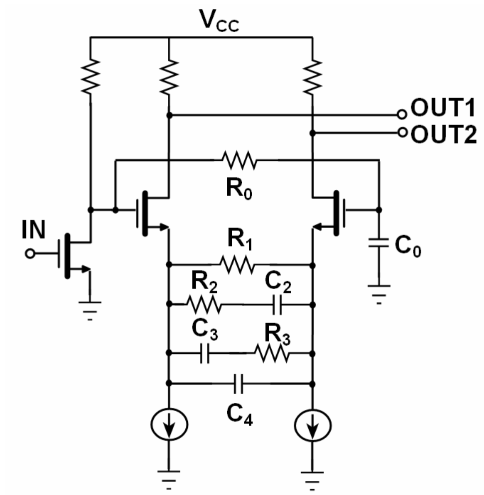

Fig 4. Proposed equalizer with differential output.

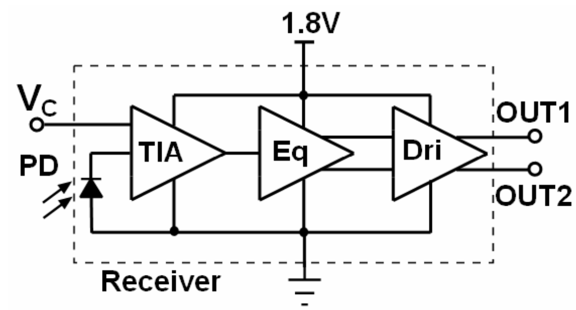

Fig. 5. Block diagram of the optical receiver.

C. Equalizer

The proposed equalizer, as shown in Fig. 4, consists of two stages: a common source and a differential amplifier. The first stage, in addition to increasing the gain, is used to provide a common-mode voltage of 1.2 V at the input of the differential amplifier.

In order to generate a differential output, a low-pass filter (R_0, C_0) is implemented between the inputs of the differential amplifier. It creates a low frequency cut-off below 100 kHz. Differential output is highly desirable to increase supply rejection.

The high pass characteristic of the equalizer is obtained by a source degenerated structure for the differential amplifier, as shown Fig. 4. The impedance is formed by a RC network ($R_{1\text{-}3}$, $C_{2\text{-}4}$) in order to attain a slope of 5 dB/dec from 1 MHz on, which is the complementary frequency response for a typical integrated photodiode. Notice that it is possible to choose the slope and the initial frequency modifying the values of the RC network for a specific photodiode.

D. Circuit implementation

The block diagram of the optical receiver is shown in Fig. 5. It includes the aforementioned TIA and equalizer with a differential 50 Ω output driver. The output driver is necessary to perform experimental measurements. Its main assignment is to drive 50 Ω loads with high output swing. Finally, the output driver shows a 5 dB gain, increasing the transimpedance, without equalizing, up to 97.4 dBΩ.

TABLE I
SUMMARY OF OPTICAL RECEIVER PERFORMANCE

Parameter	Value
Technology	180 nm CMOS
Supply Voltage	1.8 V
Bit Rate	2.5 Gb/s
Transimpedance	74.5 kΩ*
Photodiode Capacitance	C_D = 500 fF
Bandwidth	1.6 GHz
RMS Output Noise	18.97 mV*
Sensitivity @ BER = 10^{-12}	3.56 μA_{pp}
Input Dynamic Range (peak to peak)	3.56 µA to 1.5 mA 52.5 dB
DC Power Dissipation	6.5 mW (TIA) 4.1 mW (equalizer) 54 mW (Output Driver)

* Calculated from a simulation without equalizing

III. PERFORMANCES

The proposed transimpedance amplifier with equalizer has been integrated in a standard 180 nm CMOS technology with a supply voltage of 1.8 V. Its main performances are summarized in Table I. To calculate the sensitivity (S), defined as the lowest peak to peak input signal for a certain BER, if no ISI is supposed:

$$S(\mu A) = \frac{2Q \cdot n(mV)}{T_R(k\Omega)} \tag{6}$$

where n is the RMS output noise, T_R is the midband transimpedance and Q = 7 for BER = 10^{-12}.

The TIA alone consumes 6.5 mW, the equalizer 4.1 mW and the total power dissipation is 64.6 mW. The frequency response without equalizing and after equalizing over the whole control voltage swing is shown in Fig. 6 and Fig. 7, respectively, including the effect from slowly diffusion carriers. The lower cut-off frequency, as expected, is below 100 kHz, while the amplifier bandwidth is about 1.6 GHz for C_D = 500 fF. The overall transimpedance is 74.5 kΩ (97.4 dBΩ). The input spectral noise for the most critical state (inactive state determines sensitivity) for the TIA and for the complete circuit is shown in Fig. 8. It is calculated from the RMS output noise, without equalizing, at the output of the TIA and the driver divided by the squared of the midband transimpedance gain at the same point, respectively. The RMS output noise integrated over the full amplifier bandwidth for inactive state is below 19 mV, what leads to a RMS input referred noise below 0.26 μA_{pp}. For the TIA alone, the RMS input referred noise is higher (0.46 μA_{pp}). The improvement in the noise is achieved, in spite of more noise sources, thanks to a better behaviour at high frequency (see Fig. 8). The result for the noise response of the complete circuit corresponds to a sensitivity below 3.6 μA_{pp}. Therefore, considering a highest input current peak to peak of 1.5 mA (see Fig. 3), the input dynamic range is 52.5 dB. Finally, Figure 9 shows two eye diagrams at 2.5-Gb/s with PRBS 2^{31}-1 considering a rise and fall time of 20 ps for the photocurrent from the integrated photodiode, for the inactive case nearby sensitivity and the active case. The result of the simulation is noiseless, but RMS output noise, based on a normal distribution, has been added. As can be seen, in both cases duty cycle distortion is avoided thanks to the almost linear DC response of the transimpedance amplifier. In conclusion, this work shows competitive results compared with previously published designs [5-8].

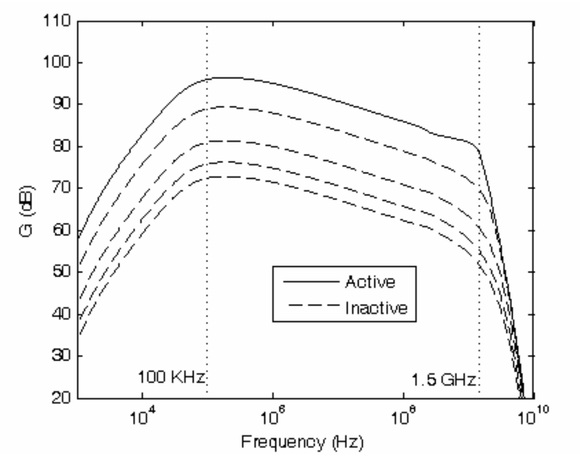

Fig. 6. Frequency response over the whole control voltage swing (inactive: V_C = 900 mV, active: V_C = 1.5 V to 1.8 V, 100 mV step).

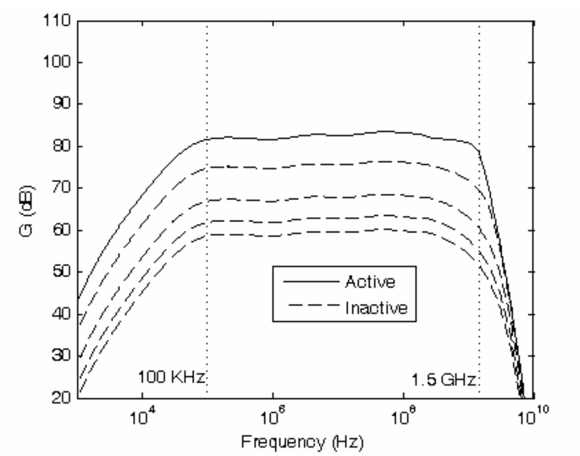

Fig. 7. Equalized frequency response over the whole control voltage swing (inactive: V_C = 900 mV, active: V_C = 1.5 V to 1.8 V, 100 mV step).

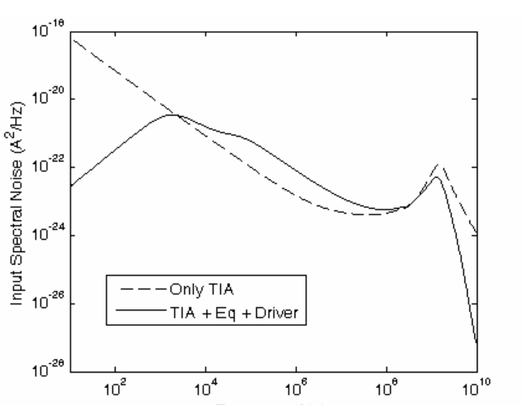

Fig. 8. Spectral input noise in inactive region for the TIA (dashed line) and for the complete circuit (solid line) without equalizing.

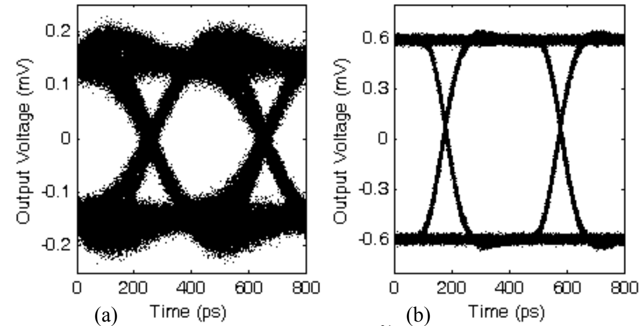

Fig. 9. Eye diagrams for 2.5-Gb/s PRBS 2^{31}-1 with a rise and fall time of 20 ps for an input current nearby sensitivity (4 μA_{pp}) in the inactive region (a) and in the active region (b) for 1.5 mA_{pp} (V_C = 1.8V).

IV. CONCLUSIONS

A 180 nm CMOS high performance transimpedance amplifier is presented in this work. It is designed for an integrated photodiode which is modeled with a capacitance of 500 fF. The TIA shows a sensitivity below 4 µA and an input dynamic range above 52 dB, thanks to a new technique to enhance the highest input current. This technique, modified from a logarithmical DC compression, keeps an approximately linear input-output response, avoiding duty cycle distortion over the whole input dynamic range. In addition, the receiver is able to compensate the frequency response of the integrated photodiode.

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