1N581x

LOW DROP POWER SCHOTTKY RECTIFIER

MAIN PRODUCTS CHARACTERISTICS

$I_{F(AV)}$	**1 A**
V_{RRM}	**40 V**
T_j	**150°C**
V_F **(max)**	**0.45 V**

DO41

FEATURES AND BENEFITS

- VERY SMALL CONDUCTION LOSSES
- NEGLIGIBLE SWITCHING LOSSES
- EXTREMELY FAST SWITCHING
- LOW FORWARD VOLTAGE DROP
- AVALANCHE CAPABILITY SPECIFIED

DESCRIPTION

Axial Power Schottky rectifier suited for Switch Mode Power Supplies and high frequency DC to DC converters. Packaged in DO41 these devices are intended for use in low voltage, high frequency inverters, free wheeling, polarity protection and small battery chargers.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value			Unit
			1N5817	1N5818	1N5819	
V_{RRM}	Repetitive peak reverse voltage		20	30	40	V
$I_{F(RMS)}$	RMS forward current		10			A
$I_{F(AV)}$	Average forward current	T_L = 125°C δ = 0.5	1			A
I_{FSM}	Surge non repetitive forward current	tp = 10 ms Sinusoidal	25			A
P_{ARM}	Repetitive peak avalanche power	tp = 1µs Tj = 25°C	1200	1200	900	W
T_{stg}	Storage temperature range		- 65 to + 150			°C
Tj	Maximum operating junction temperature *		150			°C
dV/dt	Critical rate of rise of reverse voltage		10000			V/µs

* : $\frac{dPtot}{dTj} < \frac{1}{Rth(j-a)}$ thermal runaway condition for a diode on its own heatsink

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction to ambient	Lead length = 10 mm	100	°C/W
$R_{th\ (j-l)}$	Junction to lead	Lead length = 10 mm	45	°C/W

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Tests Conditions		1N5817	1N5818	1N5819	Unit
I_R *	Reverse leakage current	Tj = 25°C	$V_R = V_{RRM}$	0.5	0.5	0.5	mA
		Tj = 100°C		10	10	10	mA
V_F *	Forward voltage drop	Tj = 25°C	I_F = 1 A	0.45	0.50	0.55	V
		Tj = 25°C	I_F = 3 A	0.75	0.80	0.85	V

Pulse test : * tp = 380 µs, δ < 2%

To evaluate the conduction losses use the following equations :
$P = 0.3 \times I_{F(AV)} + 0.090\ I_{F^2(RMS)}$ for 1N5817 / 1N5818
$P = 0.3 \times I_{F(AV)} + 0.150\ I_{F^2(RMS)}$ for 1N5819

Fig. 1: Average forward power dissipation versus average forward current (1N5817/1N5818).

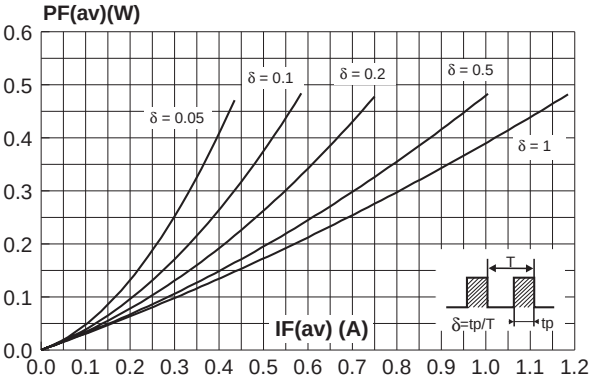


Fig. 2: Average forward power dissipation versus average forward current (1N5819).

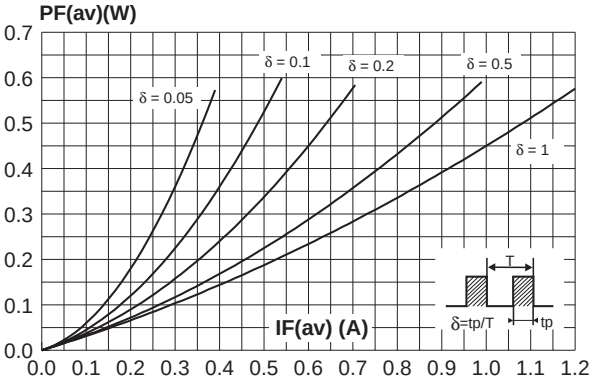


Fig. 2-1: Average forward current versus ambient temperature (δ=0.5) (1N5817/1N5818).

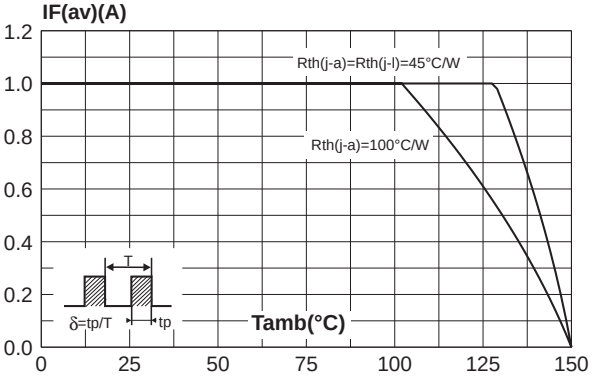
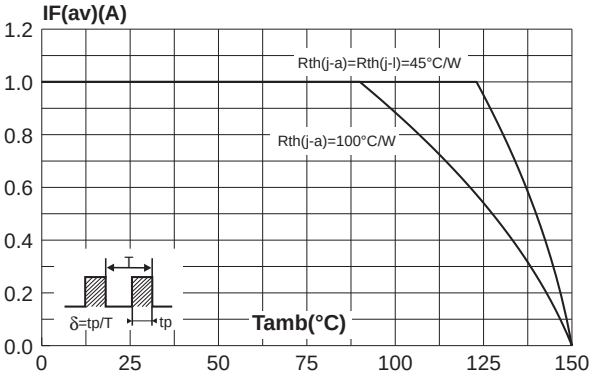


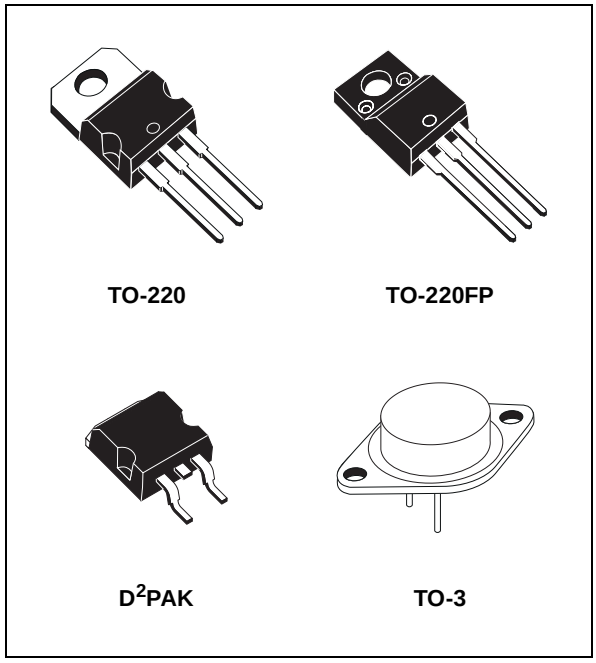
Fig. 2-2: Average forward current versus ambient temperature (δ=0.5) (1N5819).



L7800 SERIES

POSITIVE VOLTAGE REGULATORS

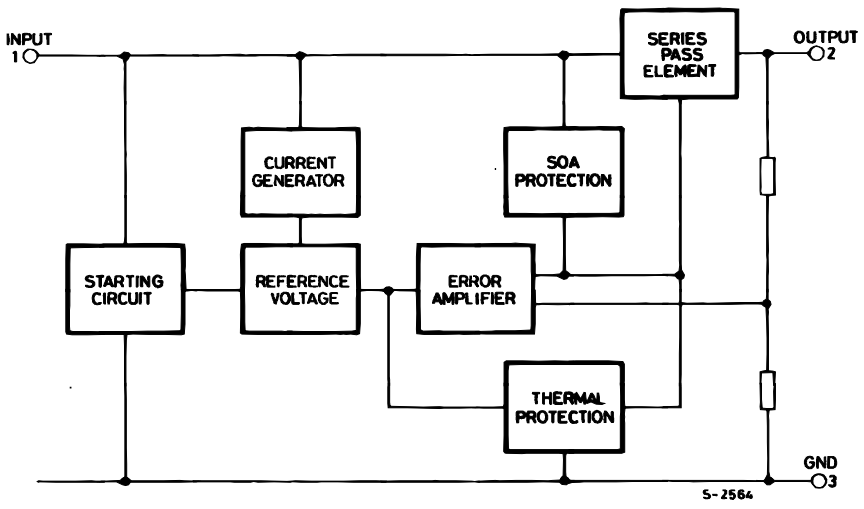
- OUTPUT CURRENT TO 1.5A
- OUTPUT VOLTAGES OF 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSITION SOA PROTECTION



DESCRIPTION

The L7800 series of three-terminal positive regulators is available in TO-220, TO-220FP, TO-3 and D^2PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltage and currents.

SCHEMATIC DIAGRAM



Copper Enamelled Wire

PRO-POWER
Quality Cables

Specifications:

Coating	: Polyurethane.
Primary Insulation Material	: Polyurethane.
Primary Insulation Colour	: Transparent.
Maximum Operating Temperature	: 120°C.
Melting Temperature	: 480°C.
Approval Bodies	: BS4520.

Specification Table

Wire Size (SWG)	Current Rating (A)	Conductor Area CSA (mm^2)	External Diameter	Conductor Make-up	Reel Length (m)	Weight (g)	Part Number
35	0.048	0.030	0.200	1/0.200	1850	500	ECW0.2
34	0.061	0.039	0.224	1/0.224	1430		ECW0.224
33	0.076	0.050	0.250	1/0.250	1120	440	ECW0.25
30	0.12	0.080	0.315	1/0.315	720	500	ECW0.315
27	0.194	0.140	0.400	1/0.400	450		ECW0.4
25	0.304	0.200	0.500	1/0.500	290	460	ECW0.5
24	0.381	0.250	0.560	1/0.560	230	500	ECW0.56
22	0.613	0.400	0.710	1/0.710	140		ECW0.71
21	0.779	0.520	0.800	1/0.800	125		ECW0.80
19	1.210	0.660	1.000	1/1.000	70		ECW1.0
18	1.910	0.820	1.250	1/1.250	47		ECW1.25
16	2.740	2.000	1.500	1/1.500	32		ECW1.5

Dimensions : Millimetres (Unless Specified)

Data Sheet No. PD60046-S

International
IOR Rectifier

IR2104(S)&(PbF)

HALF-BRIDGE DRIVER

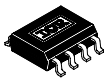
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Internally set deadtime
- High side output in phase with input
- Shut down input turns off both channels
- Matched propagation delay for both channels
- Also available LEAD-FREE

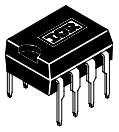
Product Summary

V_{OFFSET}	600V max.
I_O+/-	130 mA / 270 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	680 & 150 ns
Deadtime (typ.)	520 ns

Packages



8 Lead SOIC
IR2104S

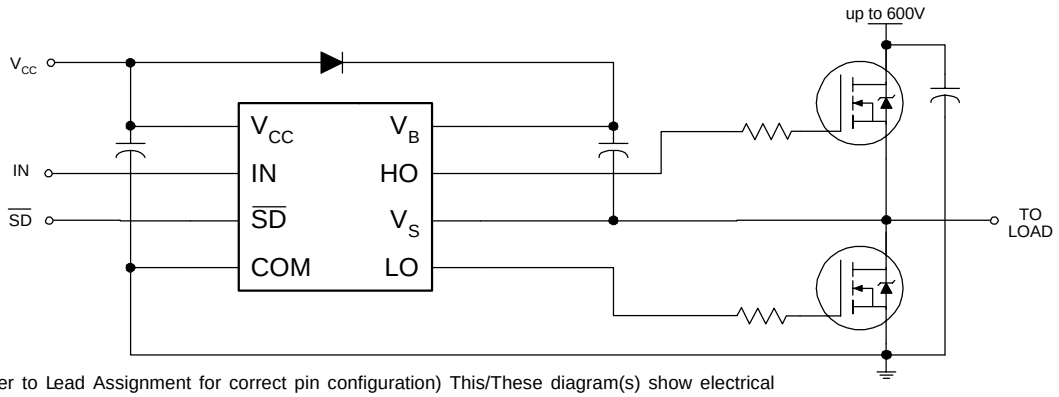


8 Lead PDIP
IR2104

Description

The IR2104(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

Typical Connection



(Refer to Lead Assignment for correct pin configuration) This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	820	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 600V
t_{sd}	Shutdown propagation delay	—	160	220		
t_r	Turn-on rise time	—	100	170		
t_f	Turn-off fall time	—	50	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” (HO) & Logic “0” (LO) input voltage	3	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” (HO) & Logic “1” (LO) input voltage	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	SD input positive going threshold	3	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	SD input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	3	10		V_{IN} = 5V
I_{IN-}	Logic “0” input bias current	—	—	1		V_{IN} = 0V
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	V_O = 0V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	360	—		V_O = 15V PW ≤ 10 µs

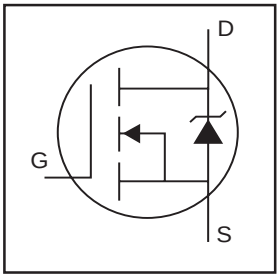
International
IOR Rectifier

PD - 94006A

IRF640N
IRF640NS
IRF640NL

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 200V

$R_{DS(on)}$ = 0.15Ω

I_D = 18A

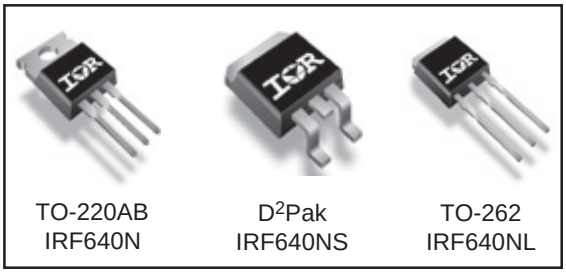
Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF640NL) is available for low-profile application.



TO-220AB	D^2Pak	TO-262
IRF640N	IRF640NS	IRF640NL

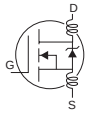
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	18	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	13	
I_{DM}	Pulsed Drain Current ①	72	
P_D @T_C = 25°C	Power Dissipation	150	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	247	mJ
I_{AR}	Avalanche Current①	18	A
E_{AR}	Repetitive Avalanche Energy①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ⑥	8.1	V/ns
T_J	Operating Junction and	-55 to +175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew④	10 lbf•in (1.1N•m)	

10/08/04

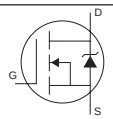
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.15	Ω	V_{GS} = 10V, I_D = 11A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	6.8	—	—	S	V_{DS} = 50V, I_D = 11A ③
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	67	nC	I_D = 11A
Q_{gs}	Gate-to-Source Charge	—	—	11		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	33		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	V_{DD} = 100V
t_r	Rise Time	—	19	—		I_D = 11A
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		R_G = 2.5Ω
t_f	Fall Time	—	5.5	—		R_D = 9.0Ω, See Fig. 10 ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1160	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	185	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	53	—		f = 1.0MHz, See Fig. 5



Source-Drain Ratings and Characteristics

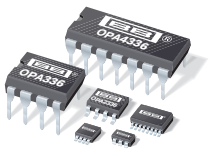
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	18	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	72		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 11A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	167	251	ns	T_J = 25°C, I_F = 11A
Q_{rr}	Reverse Recovery Charge	—	929	1394	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient④	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)⑤	—	40	

Burr-Brown Products
from Texas Instruments



OPA336
OPA2336
OPA4336

SBOS068C – JANUARY 1997 – REVISED JANUARY 2005

SINGLE-SUPPLY, *micro*Power CMOS OPERATIONAL AMPLIFIERS
*micro*Amplifier™ Series

FEATURES

- SINGLE-SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT (within 3mV)
- *micro*POWER: I_Q = 20μA/Amplifier
- *micro*SIZE PACKAGES
- LOW OFFSET VOLTAGE: 125μV max
- SPECIFIED FROM V_S = 2.3V to 5.5V
- SINGLE, DUAL, AND QUAD VERSIONS

APPLICATIONS

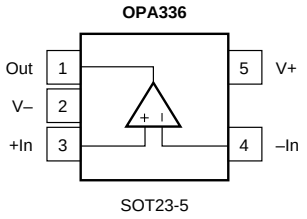
- BATTERY-POWERED INSTRUMENTS
- PORTABLE DEVICES
- HIGH-IMPEDANCE APPLICATIONS
- PHOTODIODE PRE-AMPS
- PRECISION INTEGRATORS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT

DESCRIPTION

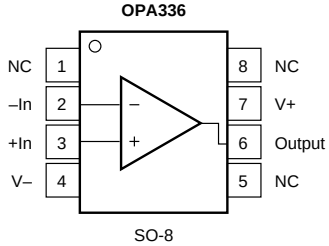
OPA336 series *micro*Power CMOS operational amplifiers are designed for battery-powered applications. They operate on a single supply with operation as low as 2.1V. The output is rail-to-rail and swings to within 3mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply—ideal for single-supply applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

In addition to small size and low quiescent current (20μA/amplifier), they feature low offset voltage (125μV max), low input bias current (1pA), and high open-loop gain (115dB). Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

OPA336 packages are the tiny SOT23-5 surface mount and SO-8 surface-mount. OPA2336 come in the miniature MSOP-8 surface-mount, SO-8 surface-mount, and DIP-8 packages. The OPA4336 package is the space-saving SSOP-16 surface-mount. All are specified from –40°C to +85°C and operate from –55°C to +125°C. A macromodel is available for download (at www.ti.com) for design analysis.

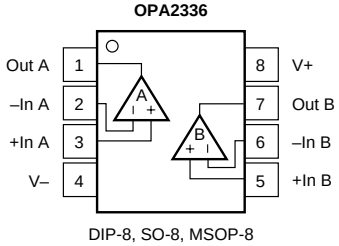


SOT23-5

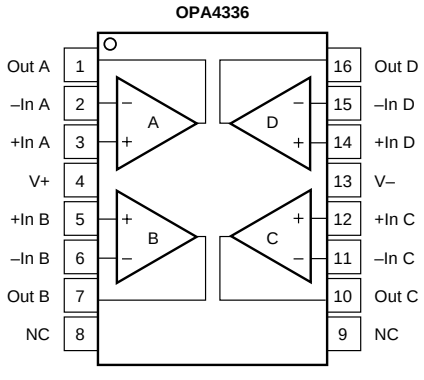


SO-8

NC = No Connection



DIP-8, SO-8, MSOP-8



SSOP-16

NC = No Connection

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DRAWING DESIGNATOR	PACKAGE MARKING
Single			
OPA336N	SOT23-5	DBV	A36[2]
OPA336NA	SOT23-5	DBV	A36[2]
OPA336NJ	SOT23-5	DBV	J36
OPA336U	SO-8 Surface-Mount	D	OPA336U
OPA336UA	SO-8 Surface-Mount	D	OPA336UA
OPA336UJ	SO-8 Surface-Mount	D	OPA336UJ
Dual			
OPA2336E	MSOP-8 Surface-Mount	DGK	B36[2]
OPA2336EA	MSOP-8 Surface-Mount	DGK	B36[2]
OPA2336P	DIP-8	P	OPA2336P
OPA2336PA	DIP-8	P	OPA2336PA
OPA2336U	SO-8 Surface-Mount	D	OPA2336U
OPA2336UA	SO-8 Surface-Mount	D	OPA2336UA
Quad			
OPA4336EA	SSOP-16 Surface-Mount	DBQ	OPA4336EA

NOTES: (1) For the most current package and ordering information, see the package option addendum at the end of this data sheet. (2) Grade will be marked on the Reel.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	7.5V
Signal Input Terminals, Voltage[2]	(V–) –0.3V to (V+) +0.3V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Rating:	
Charged Device Model, OPA336 NJ and UJ only (CDM)[4]	1000V
Human Body Model (HBM)[4]	500V
Machine Model (MM)[4]	100V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package. (4) OPA336 NJ and UJ have been tested to CDM of 1000V. All other previous package versions have been tested using HBM and MM. Results are shown.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: V_S = 2.3V to 5.5V

Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA336N, U OPA2336E, P, U			OPA336NA, UA OPA2336EA, PA, UA OPA4336EA			OPA336NJ, UJ			UNITS
			MIN	TYP[1]	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE												
Input Offset Voltage	V_{OS}			±60	±125		*	±500		±500	±2500	µV
vs Temperature	dV_{OS}/dT			**±1.5**			*			*		**µV/°C**
vs Power Supply	PSRR	V_S = 2.3V to 5.5V		25	100		*	*	*	*	*	µV/V
Over Temperature		V_S = 2.3V to 5.5V			**130**			*	*		*	**µV/V**
Channel Separation, dc				0.1			*			*		µV/V
INPUT BIAS CURRENT												
Input Bias Current	I_B			±1	±10		*	*		*	*	pA
Over Temperature					**±60**			*			*	**pA**
Input Offset Current	I_{OS}			±1	±10		*	*		*	*	pA
NOISE												
Input Voltage Noise, f = 0.1 to 10Hz				3			*			*		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			40			*			*		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			30			*			*		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE												
Common-Mode Voltage Range	V_{CM}		–0.2		(V+) –1	*		*	*		*	V
Common-Mode Rejection Ratio	CMRR	–0.2V < V_{CM} < (V+) –1V	80	90		76	86		76	86		dB
Over Temperature		–0.2V < V_{CM} < (V+) –1V	**76**			**74**			**74**			**dB**
INPUT IMPEDANCE												
Differential				10^{13} || 2			*			*		Ω || pF
Common-Mode				10^{13} || 4			*			*		Ω || pF
OPEN-LOOP GAIN												
Open-Loop Voltage Gain	A_{OL}	R_L = 25kΩ, 100mV < V_O < (V+) – 100mV	100	115		90	*		90	*		dB
Over Temperature		R_L = 25kΩ, 100mV < V_O < (V+) – 100mV	**100**			**90**			**90**			**dB**
		R_L = 5kΩ, 500mV < V_O < (V+) – 500mV	90	106		*	*		*	*		dB
Over Temperature		R_L = 5kΩ, 500mV < V_O < (V+) – 500mV	**90**			*			*			**dB**
FREQUENCY RESPONSE												
Gain-Bandwidth Product	GBW	V_S = 5V, G = 1		100			*			*		kHz
Slew Rate	SR	V_S = 5V, G = 1		0.03			*			*		V/µs
Overload Recovery Time		V_{IN} • G = V_S		100			*			*		µs
OUTPUT												
Voltage Output Swing from Rail[2]		R_L = 100kΩ, A_{OL} ≥ 70dB		3			*			*		mV
		R_L = 25kΩ, A_{OL} ≥ 90dB		20	100		*	*		*	*	mV
Over Temperature		R_L = 25kΩ, A_{OL} ≥ 90dB			**100**			*			*	**mV**
		R_L = 5kΩ, A_{OL} ≥ 90dB		70	500		*	*		*	*	mV
Over Temperature		R_L = 5kΩ, A_{OL} ≥ 90dB			**500**			*			*	**mV**
Short-Circuit Current	I_{SC}			±5			*			*		mA
Capacitive Load Drive	C_{LOAD}			See Text			*			*		pF
POWER SUPPLY												
Specified Voltage Range	V_S		2.3		5.5	*		*	*		*	V
Minimum Operating Voltage				2.1			*			*		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		20	32		*	*		23	38	µA
Over Temperature		I_O = 0			**36**			*			**42**	**µA**
TEMPERATURE RANGE												
Specified Range			–40		+85	*		*	*		*	°C
Operating Range			–55		+125	*		*	*		*	°C
Storage Range			–55		+125	*		*	*		*	°C
Thermal Resistance	θ_{JA}											
SOT-23-5 Surface-Mount				200			*			*		°C/W
MSOP-8 Surface-Mount				150			*					°C/W
SO-8 Surface-Mount				150			*			*		°C/W
DIP-8				100			*					°C/W
SSOP-16 Surface-Mount				100			*					°C/W
DIP-14				80			*					°C/W

*Specifications same as OPA2336E, P, U.

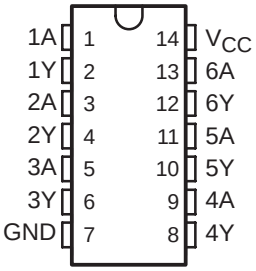
NOTES: (1) V_S = +5V. (2) Output voltage swings are measured between the output and positive and negative power-supply rails.

- **Dependable Texas Instruments Quality and Reliability**

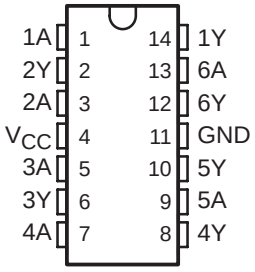
description/ordering information

These devices contain six independent inverters.

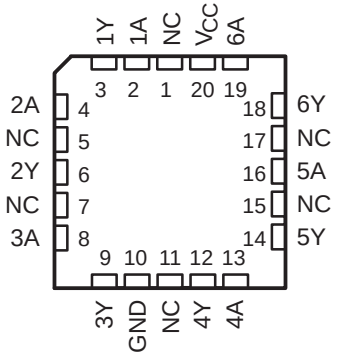
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

ORDERING INFORMATION

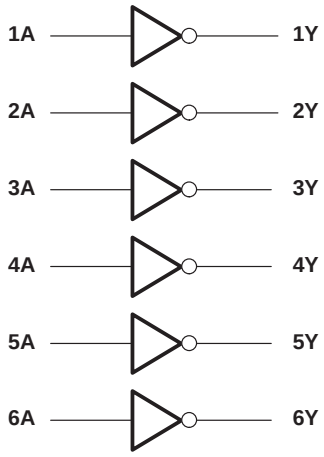
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube	SN7404N	SN7404N
		Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
	SOIC − D	Tube	SN7404D	7404
		Tape and reel	SN7404DR	
		Tube	SN74LS04D	LS04
		Tape and reel	SN74LS04DR	
		Tube	SN74S04D	S04
		Tape and reel	SN74S04DR	
	SOP − NS	Tape and reel	SN7404NSR	SN7404
		Tape and reel	SN74LS04NSR	74LS04
		Tape and reel	SN74S04NSR	74S04
	SSOP − DB	Tape and reel	SN74LS04DBR	LS04
−55°C to 125°C	CDIP − J	Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
		Tube	SN54LS04J	SN54LS04J
		Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
		Tube	SNJ54S04J	SNJ54S04J
	CFP − W	Tube	SNJ5404W	SNJ5404W
		Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC − FK	Tube	SNJ54LS04FK	SNJ54LS04FK
		Tube	SNJ54S04FK	SNJ54S04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

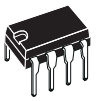


$Y = \overline{A}$

TS555

LOW POWER SINGLE CMOS TIMER

- VERY LOW POWER CONSUMPTION :
  110 µA typ at V_{CC} = 5V
  90 µA typ at V_{CC} = 3V
- HIGH MAXIMUM ASTABLE FREQUENCY 2.7MHz
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE555
- WIDE VOLTAGE RANGE : +2V to +16V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

P
TSSOP8
(Thin Shrink Small Outline Package)

DESCRIPTION

The TS555 is a single CMOS timer which offers very low consumption ($I_{cc(TYP)}$ TS555 = 110µA at V_{CC}=+5V versus $I_{cc(TYP)}$ NE555 = 3mA) and high frequency $f_{f(max.)}$ TS555 = 2.7MHz versus $f_{(max.)}$ NE555 = 0.1 MHz)

Thus, either in Monostable or Astable mode, timing remains very accurate.

The TS555 provides reduced supply current spikes during output transitions, which enables the use of lower decoupling capacitors compared to those required by bipolar NE555.

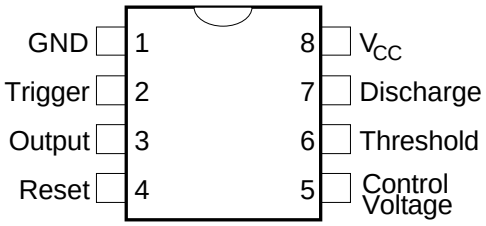
Timing capacitors can also be minimized due to high input impedance ($10^{12}\Omega$).

ORDER CODES

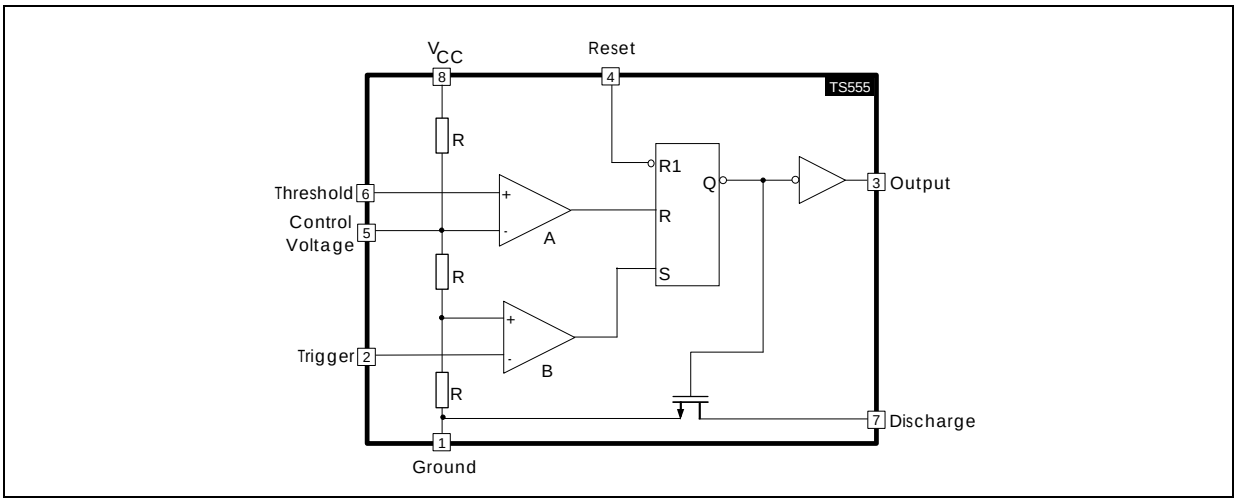
Part Number	Temperature Range	Package		
		N	D	P
TS555C	0°C, +70°C	•	•	•
TS555I	-40°C, +125°C	•	•	•
TS555M	-55°C, +125°C	•	•	•

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape & Reel (PT)

PIN CONNECTIONS (top view)



BLOCK DIAGRAM



FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW <-----> Level Voltage ≤ Min voltage specificed

HIGH <-----> Level Voltage ≥ Max voltage specificed

x <-----> Irrelevant

ABSOLUTE MAXIMUM RATINGS

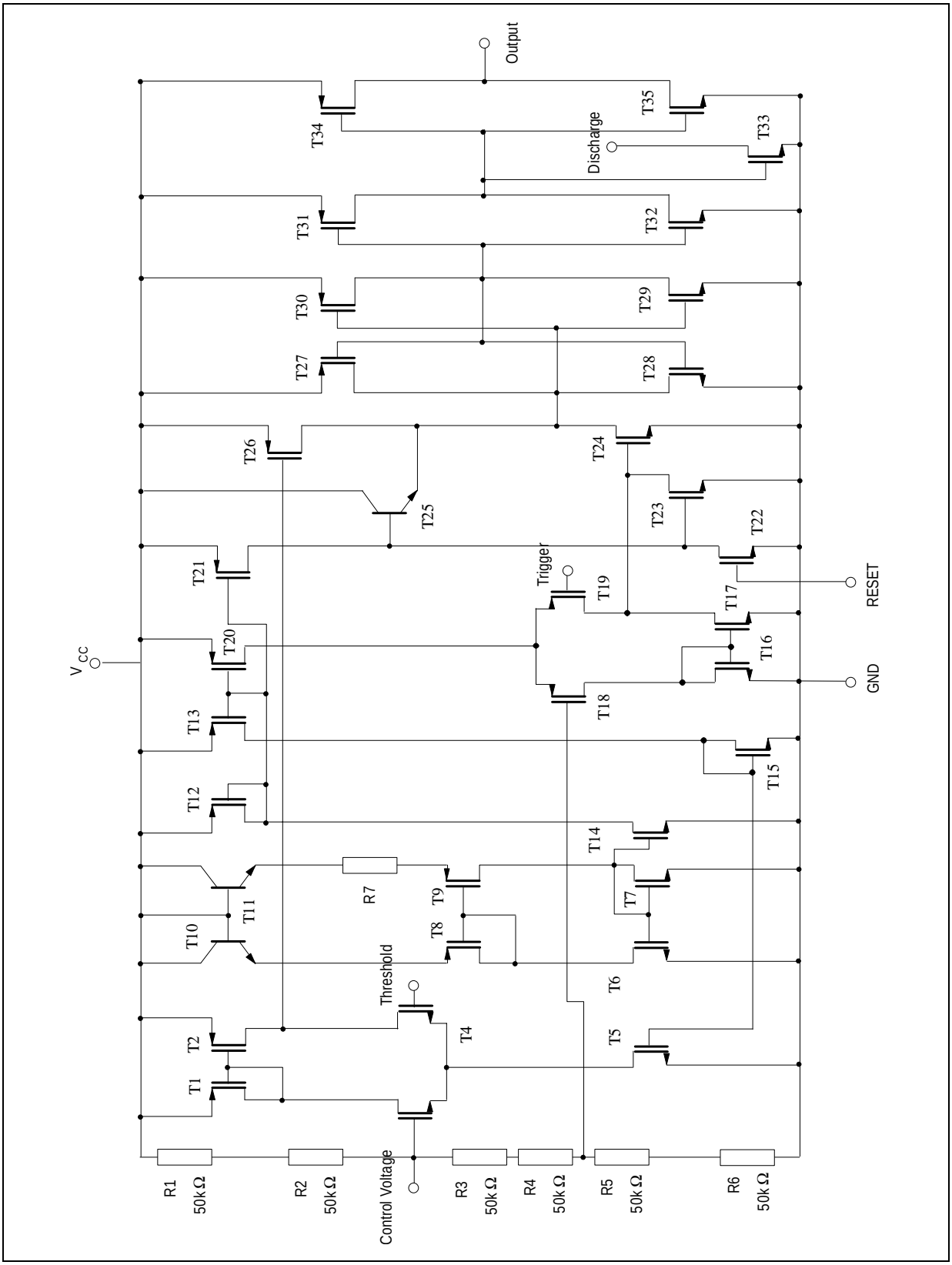
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		+18	V
T_j	Junction Temperature		+150	°C
T_{stg}	Storage Temperature Range		-65 to +150	°C
P_D	Power dissipation[1)]	DIP8 SO8 TSSOP8	1250 715 625	mW

1. T_j = 150°C, T_{amb} = 25°C with Rthja = 100°C/W for DIP8 package
Rthja = 175°C/W for SO8 package
Rthja = 200°C/W for TSSOP8 package

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+2 to +16	V
T_{oper}	Operating Free Air Temperature Range TS555C TS555I TS555M	 0 to +70 -40 to +125 -55 to +125	°C

SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = +2V, T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current (no load, High and Low States) $T_{min.} \le T_{amb} \le T_{max.}$		65	200 200	µA
V_{CL}	Control Voltage Level $T_{min.} \le T_{amb} \le T_{max.}$	1.2 1.1	1.3	1.4 1.5	V
V_{DIS}	Discharge Saturation Voltage (I_{dis} = 1mA) $T_{min.} \le T_{amb} \le T_{max.}$		0.05	0.2 0.25	V
I_{DIS}	Discharge Pin Leakage Current		1	100	nA
V_{OL}	Low Level Output Voltage (I_{sink} = 1mA) $T_{min.} \le T_{amb} \le T_{max.}$		0.1	0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{source} = -0.3mA) $T_{min.} \le T_{amb} \le T_{max.}$	1.5 1.5	1.9		V
V_{TRIG}	Trigger Voltage $T_{min.} \le T_{amb} \le T_{max.}$	0.4 0.3	0.67	0.95 1.05	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage $T_{min.} \le T_{amb} \le T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset Current		10		pA