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Voltage equalization of an ultracapacitor module by cell grouping using number partitioning algorithm

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Abstract: Ultracapacitors are low voltage devices and therefore, for practical applications, they need to be used in modules of series-connected cells. Because of the inherent manufacturing tolerance of the capacitance parameter of each cell, and as the maximum voltage value cannot be exceeded, the module requires inter-cell voltage equalization. If the intended application suffers repeated fast charging/discharging cycles, active equalization circuits must be rated to full power, and thus the module becomes expensive. Previous work shows that a series connection of several sets of paralleled ultracapacitors minimizes the dispersion of equivalent capacitance values, and also the voltage differences between capacitors. Thus the overall life expectancy is improved. This paper proposes a method to distribute ultracapacitors with a number partitioning-based strategy to reduce the dispersion between equivalent submodule capacitances. Thereafter, the total amount of stored energy and/or the life expectancy of the device can be considerably improved.

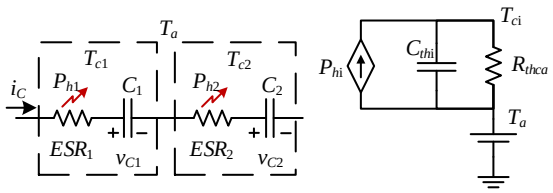
Keywords: Ultracapacitor module, Storage system, Voltage balancing, Partitioning algorithm, Parallel-series connection, Ageing

1. Introduction

Compared with batteries, ultracapacitor modules offer higher power densities and cycling capabilities, but lower energy densities, so they are preferred when high power discharge and/or charge is required [1-6]. Some examples of applications are energy recovery systems [1,2], buffering of energy source fluctuations [7,8], hybrid vehicles [4,9] and others.

Ageing of the ultracapacitor module, which depends mainly on the temperature and voltage level of each cell [10], is one of the main concerns of engineers. The ageing is manifested by an increment of the Equivalent Series Resistance (ESR) and a decrement of the capacitance of the cell. Ultracapacitors are low voltage devices, usually below 3V, and hence they must be serialized up to 50 to 200 elements, depending on the required nominal voltage [11]. Tolerance in capacitive value leads to different voltage levels in series-connected capacitors, which results in two main undesirable effects [12]. First, the overall voltage level is limited to a value below the theoretical maximum voltage. Thus, the practical stored energy, which depends on the square of the voltage, is smaller than the theoretically installed energy. Second, the ageing process is accelerated, as it is shown below.

Fig. 1.a shows an example of two ultracapacitors connected in series, with v_{Ci} the voltage across the cell, ESR_i the equivalent series resistance, P_{hi} the power losses at each ESR_i and T_{ci} the case temperature. Fig. 1.b depicts the equivalent thermal circuit of a cell, being C_{thi} the thermal capacitance and R_{thca} the case to ambient thermal resistance.



a) b)

Fig. 1. Equivalent models: a) equivalent electrical circuit of two ultracapacitors connected in series, b) thermal model of a cell

The ageing of the capacitance C of any ultracapacitor can be generally described by equation (1). It depends on the voltage of the cell and on its temperature, and it is always negative.

$$\frac{dC}{dt} = f_{aC}\left(v_C, T_c\right) < 0 \tag{1}$$

In the same way, the ageing of the ESR depends also on the voltage and the temperature of the cell but it is always positive, see equation (2).

$$\frac{dESR}{dt} = f_{aR}\left(v_C, T_c\right) > 0 \tag{2}$$

The temperature of any cell T_c depends on the heating power generated at the ESR by its own current i_C and on the ambient temperature T_a, as represented by equation (3).

$$T_c = f_T\left(T_a, ESR, i_C\right) \tag{3}$$

Fig. 2.a shows the ageing loops between parameters and variables. Sloping arrows describe the type of variation that the related variable undergoes during the ageing process. The capacitance parameter evolves towards smaller values and therefore, for a given current profile, the resulting voltage increases. Considering that the ageing process depends on the voltage value, capacitance reduction is accelerated. A similar behavior can be observed when

analyzing the evolution of the *ESR*. For any given current, a higher *ESR* value leads to a higher heating power, which generates higher temperatures at the cell, and therefore the *ESR* growth is accelerated.

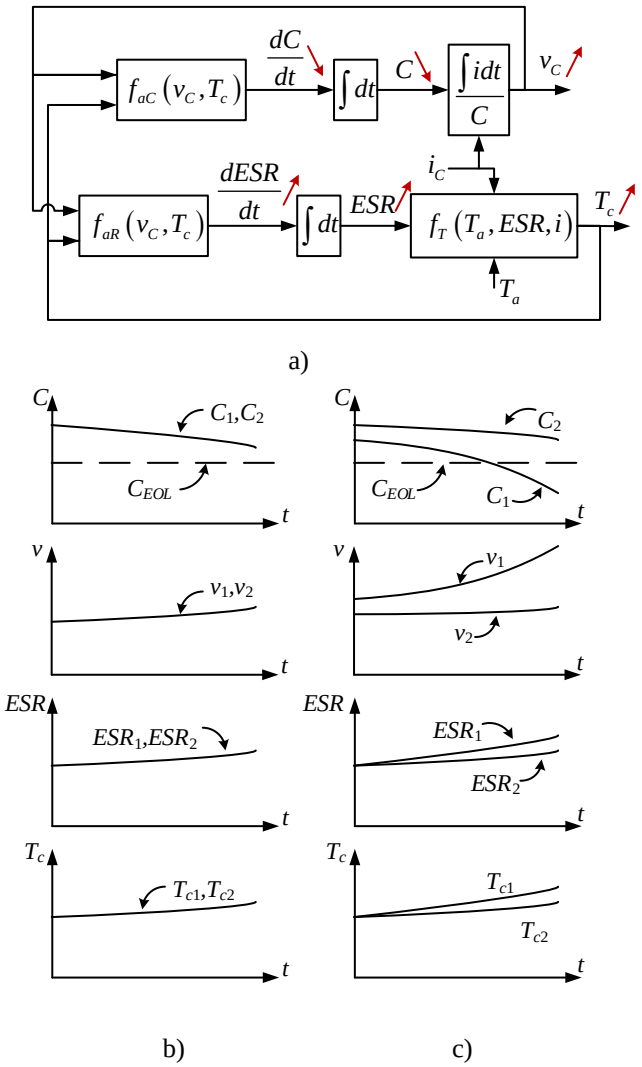


Fig. 2. Ageing process: a) closed-loop interrelations between ageing variables and parameters of a cell, b) ageing proces of two ultracapacitors in series with identical initial parameters and c) the same as b) but with different initial capacitances, $C_1(0)<C_2(0)$

Moreover, there is a cross coupling between the capacitance degradation and the *ESR* increment. A higher voltage due to a lower capacitance has a negative impact on *ESR* and a higher temperature due to a higher *ESR* leads to a lower capacitance. It can be concluded that the ageing process is inherent to any ultracapacitor device and that there is no way of avoiding it. The point is that, unless some basic precautions are adopted, the ageing process of serialized cells can get worse. Let's analyse the example of Fig. 1.a where two ultracapacitors are connected in series. Two cases can be studied. In the first case both ultracapacitors are identical, and therefore if they handle the same current and ambient temperature, their ageing processes are identical, see Fig. 2.b. In this figure capacitor voltage and temperature curves refer to the maximum voltage and temperature values when operating under identical charging-discharging cycles. C_{EOL} refers to the capacitance value that is considered to be the end-of-life of the ultracapacitor. Actually, in a practical case initial ESRs do not differ significantly from each other but dispersion in capacitance is quite large and falls in the range from 20% to 30%. Fig. 2.c depicts the case where initial capacitances are different, being $C_1(0)<C_2(0)$. As it can be observed, an initial lower capacitance C_1 leads to a higher initial voltage v_1, thus its ageing is boosted and C_1 and ESR_1 degenerate faster than C_2 and ESR_2. Therefore, initial parameter dispersion is amplified during the ageing process, and the initially worst suited ultracapacitor goes faster through a destructive feedback loop, thus reaching the end of life in a relatively short time span. The fast failure of a single cell belonging to an all-in-series configuration implies the premature end-of-life of the entire module. In order to avoid the premature failure of the module, engineers must take into account the initial dispersion of capacitances and formulate voltage equalization solutions.

Voltage equalization strategies belong broadly to two families: the passive ones and the active ones [11]. Passive equalization networks can be built by clamping diodes that draw current when the related cell voltage goes above its maximum safe value. The main drawback of this strategy is that if the module does not operate at its usual maximum voltage level, the imbalance in voltage cannot be avoided. Thus, this strategy has to be complemented with equalizing resistors, which lead to energy consumption and slow balancing strategy.

Active equalization strategies, on the other hand, are based on DC/DC converters that can achieve efficient energy exchange from most charged capacitors to those with lower voltage levels. They are complex and could be expensive too, depending on the required equalizing dynamics (i.e. power).

The imbalance problem must be carefully addressed during charging processes, although it has no significant impact during discharging process. Charging processes are of two types: high power processes and low power processes. In dealing with a low power charging case, a low-power, low-cost equalizing system will be the most effective solution. Typical applications are pulsed power discharge devices [6], ride through systems [13], wherein the energy can be slowly stored and where an abrupt high-power discharge is often needed.

On the other hand, in energy recovery applications, such as regenerative braking [1,2,4,9], or in pulsed load cycling applications [3,5], a high-power charge is required. Therefore, a fast voltage rise occurs and the maximum permissible level is easily reached. In such fast charging and discharging situations, high-power voltage equalizing systems, based on active DC/DC power converters, should be the solution. But in most cases the required equalizing power is equal to that of the installed power, so the device cost almost doubles, and the reliability is reduced.

This paper addresses this issue and proposes a method for ultracapacitor cell-grouping and placement in such a way that dispersion of equivalent capacitances is minimized and thus intrinsic voltage equalization is achieved avoiding the use of extra equalizing electronics

2. Optimal module topology

Any energy storage system must generally fulfill two requirements: (i) a given energy storage capability and (ii) the ability to exchange this energy at a given rate, i.e. its nominal power [11]. These two figures, together with the thermal cycling profile, determine the total number of ultracapacitors to be installed, say *N*. At this point, the designer must decide how the cells are distributed, i.e. the number of cells in series and/or in parallel and the overall voltage. The distribution so chosen directly impacts the module reliability, its fault tolerance behavior, the resulting voltage balance, and therefore, its ageing [14].

The total amount of energy W_n that an ultracapacitor can store at nominal voltage V_n is equal to

$$W_n = \frac{1}{2} C V_n^2 \tag{4}$$

For a given power exchange, the current/voltage relationship follows the well-known hyperbolic law (5), so the lower the module voltage level, the higher the current rating would be.

$$P_n = V_{\min} I_{\max} \tag{5}$$

Due to current limitations, nominal power exchange at very low voltages is not possible, and consequently, part of the energy storage capability cannot be exploited. The minimum voltage is typically limited to half the nominal value (V_n), resulting in "usable" energy W_u equal to:

$$W_u = \frac{1}{2} C \left(V_n^2 - \left(\frac{V_n}{2} \right)^2 \right) = 0.75 W_n \tag{6}$$

That is, 75% of the installed storage capability is theoretically available. Considering the typical low nominal voltage of ultracapacitor cells, most of the designers try to obtain voltage/current levels that are compatible with industrial standards by means of a single string of serialized ultracapacitors (see Fig. 3.a).

As the cells are in series, all of them are equally charged and therefore their voltage level will depend on their actual capacitor value,

$$v_i = \frac{Q}{C_i} \tag{7}$$

Supposing the "worst" case of only one capacitor with a 20% lower capacitance, the overall maximum voltage is

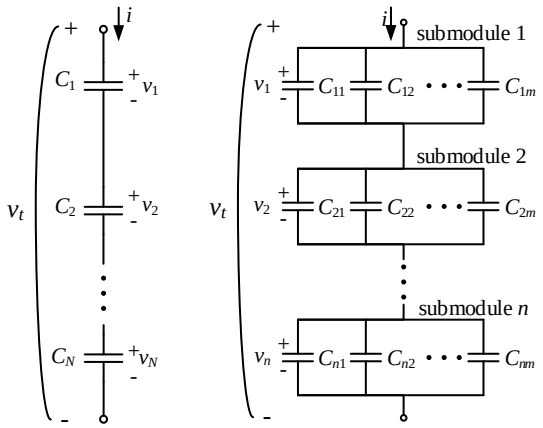
$$v_{\max} = \frac{Q_{\max}}{C_i} = \frac{v_n 0.8 C_n}{C_n} = 0.8 v_n \tag{8}$$

So, the maximum usable energy is

$$W_u' = \frac{1}{2} C \left(V_{\max}^2 - \left(\frac{V_n}{2} \right)^2 \right) = 0.39 W_n \tag{9}$$

and the actual usable energy, compared to the theoretical ideal case of (6), is

$$\frac{W_u'}{W_u} = 0.52 \tag{10}$$



a) b)

Fig. 3. Different module topologies: a) series connection of *N* cells and b) first parallel then series configuration

Thus, in the all-in-series configuration of Fig. 3.a, initial dispersion of capacitances limits the practical energy exchange capability to half the theoretically available one. To make things worse, the "bad" cell with a higher voltage suffers faster ageing, going through a destructive ageing loop. Another known issue of the all-in-series configuration is that, as all the cells have the same current, those with the higher ESR withstand higher temperatures, undergoing accelerated ageing in another destructive loop.

The work presented in [14] shows that the optimal distribution is a combination of *n* submodules, built by *m* parallel connected ultracapacitors, which are then connected in series (see Fig. 3.b). This configuration has several advantages in terms of ageing and reliability. Considering a capacitance tolerance of ΔC, the equivalent capacitance dispersion between the submodules is statistically reduced to

$$\Delta C_{eq} = \frac{\Delta C}{m} \tag{11}$$

This means that the voltage differences between different submodules are reduced equally, and the ageing dispersion is reduced too. In the same way, differences in

ESR lead to different currents through paralleled capacitors, in such a way that the capacitor with the lowest ESR gets higher current and vice versa, thus avoiding the above mentioned destructive ageing loop.

3. Optimal grouping of ultracapacitors by partitioning algorithm

Previous section identifies the drawbacks of the all-in-series topology, and recapitulates the optimal topology identified in [14]. The advantages of the first-parallel then-series connection strategy are statistics-dependent and can be obtained in whichever way this topology is used. But, there is still scope for improving the results, i.e. to minimize the dispersion between equivalent capacitance values of submodules. This improvement can be achieved by simply answering this question: "*Considering a module built by n submodules in series, being each submodule built by m cells in parallel, that is, a population of* $N = n \times m$ *ultracapacitors, and knowing the individual capacitance* C_i *of each cell, is there any grouping method that minimizes the dispersion between the equivalent capacitances of each submodule?*" The work presented herein answers this question and confirms that scope for improvement does exist. The improved grouping strategy is based on heuristic approach, followed by a recursive algorithm, which is inspired by number partitioning strategies [15].

3.1. Heuristic distribution algorithm

Considering that there are *N* capacitors to be grouped,

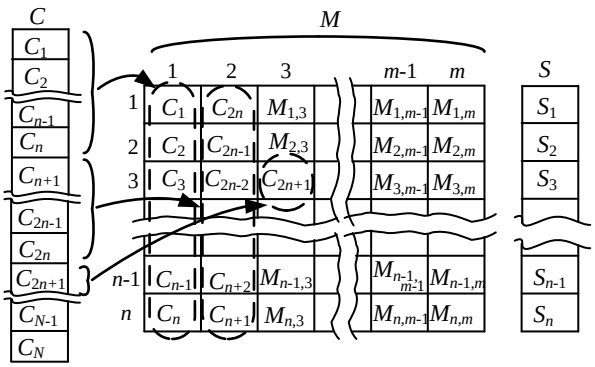
$$\overline{C} = \{C_1, C_2, \cdots, C_N\} \tag{12}$$

the capacitors are organized in their decreasing order of capacitance values, as follows:

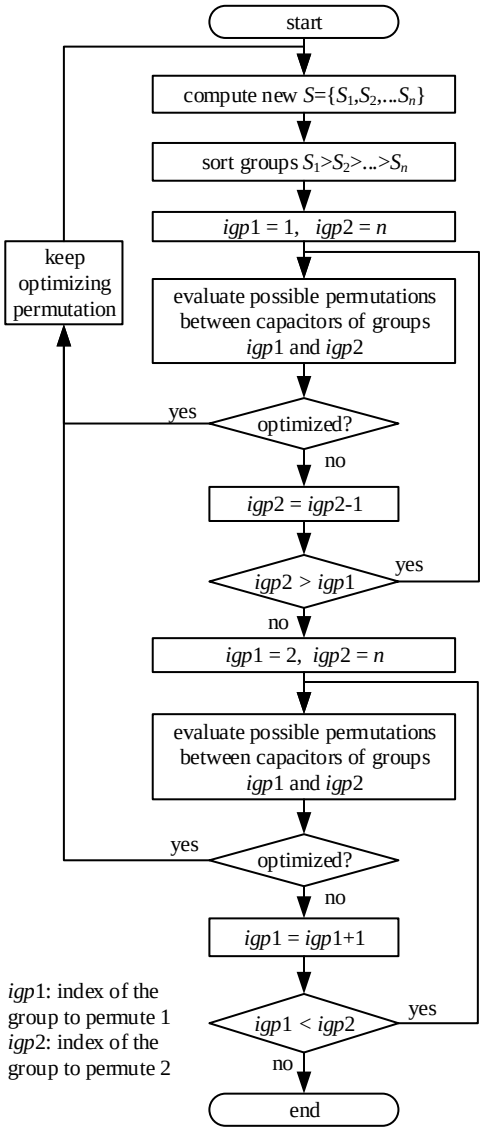
$$C_1 \geq C_2 \geq \cdots \geq C_N \tag{13}$$

This set of organized capacitors is on the left side of Fig. 4.a. The ultracapacitor module is symbolized by the matrix *M* and it is at the center of Fig. 4.a. It has *n* files corresponding to the *n* submodules, and *m* columns related to the *m* capacitors in parallel (see Fig. 3.b). On the right side of Fig. 4.a, the array *S* summarizes the sum of the capacitance values of each line (or group or submodule), see equation (14):

$$S_i = \sum_{j=1}^{m} M_{ij} \tag{14}$$



a)



b)

Fig. 4. Grouping process: a) initial heuristic distribution of capacitors and b) flow chart of the recursive distribution algorithm.

It is noteworthy that this value has been used during the distribution of the capacitors, i.e. even if the module is

partially occupied by capacitors, the sum of each group is computed and used as the key input during distribution steps.

The initial distribution algorithm starts with placing the largest n capacitors in the first column, that is $M_{1,1} = C_1$, $M_{2,1} = C_2$, ... $M_{n,1} = C_n$. If the dispersion between the sums is to be minimized, the next natural step is to place the next largest capacitor, i.e. C_{n+1}, in the group with the minimum sum, that is, in the n^{th} group (see Fig. 4.a). This way, the second column is filled by capacitors ranging from C_{2n} down to C_{n+1}. The next larger capacitor to be located is C_{2n+1}, and the strategy to be followed remains the same: the capacitor is placed in the group with the minimum sum, in this example, the 3rd group. The algorithm concludes with placing all the capacitors in the module.

3.2. Grouping improvement by number-partitioning based algorithm

The flow chart of Fig. 4.b shows the recursive algorithm employed to reduce the dispersion between the sums of the groups of capacitors. It is based on number-partitioning strategies [15]. First, all the groups are sorted in the descending order of sum values, i.e.:

$$S_1 > S_2 > ... > S_{n-1} > S_n \tag{15}$$

Hence, the maximum dispersion between equivalent capacitors is the difference between the first and the last sums. Therefore, the algorithm must find a capacitor permutation that decreases the sum of the first group S_1 or increases the sum of the last group, S_n. The first loop looks for improvement in the first sum. The *index of the group to permute* 1 (*igp*1) points permanently toward the first group, whereas the *index of the group to permute* 2 (*igp*2) goes through all the groups, from the last one up to the second one. Fig. 5.a shows an example of two groups whose capacitor-permutations are to be tested.

Each capacitors of group 1 can be permuted, one-by-one, with all the capacitors of group 2. Fig. 5.a shows the case where the third capacitor of group 1 is permuted by capacitors of group 2. The sum of all the capacitors distributed within the groups G_1 and G_2 remains constant:

$$S_1 + S_2 = \sum_{i=1}^{m} C_{1i} + \sum_{i=1}^{m} C_{2i} = \text{constant} \tag{16}$$

After each permutation, the resulting sums S_1 and S_2 are computed. Considering equation (16), if one of the sums increases, the other one must decrease. This way, after a permutation, if the sums of the first and second groups S_1 and S_2 become smaller than the maximum of the initial sums, then the new maximum equivalent capacitor will become smaller, and thus an improvement will be achieved.

Fig. 5.b shows an example with the sums and dispersion values of three different cases. First, the initial sums and dispersion values are shown. The maximum initial sum (S_{0max}) is computed. In the permutation case (*a*), the new sums are smaller than the initial maximum one, and hence smaller dispersion D is achieved. Therefore, the permutation must be retained. In the permutation case (*b*), one of the new sums is larger than the maximum initial sum, and hence larger dispersion D is obtained. Therefore, this permutation must be discarded.

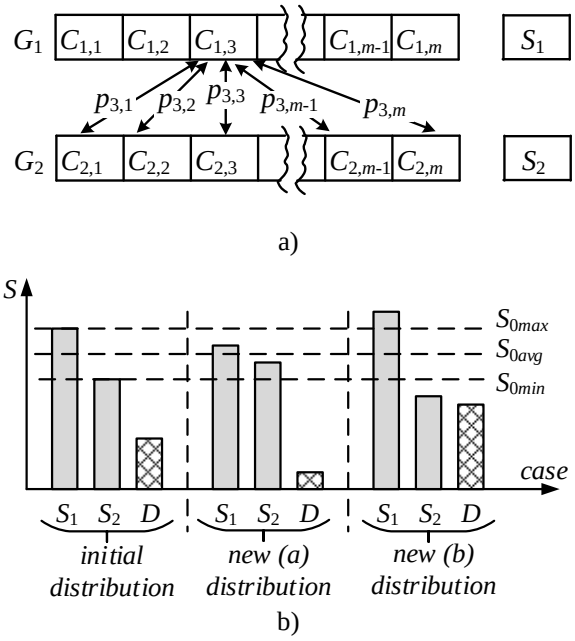


Fig. 5. Permuting test procedure: a) example of possible permutations between the third capacitor of group 1 and all the capacitors of group 2, b) sums (S_1, S_2) and dispersion (D) of the algorithm of Fig. 10 before permutation test (*initial distribution*), and after two permutation examples (better *new [a] distribution* and worse *new [b] distribution*)

After a successful permutation test, the algorithm stops permuting, keeps the new capacitor configuration and activates a flag signaling that an improved grouping has been identified.

When the high-level algorithm of Fig. 4.b receives a flag signaling improvement, it retains the new module configuration, computes the new sums, sorts all the groups in descending order of the resulting sums and goes through a new interaction process. If interactions with the first group (larger sum) do not lead to any improvement, interactions with the last group (smaller sum) are tested. In this case an improvement is achieved when the new sums are larger than the initial smaller sum of the last group. Once an improvement is identified, it is retained and, as the group composition is modified, the algorithm goes back to the starting point of (see Fig. 4.b) and re-evaluates again any possible improvement, repeating all the steps explained in this section.

The distribution obtained is considered final, when the partition is tested under all possible permutations and it is found that no further improvement is possible. It has to be pointed out that the proposed algorithm involves

unnecessary repetition of some tests; so, it does not offer the optimum execution time. But, it is very simple, reliable and can be used with any personal computer. Besides, it is fast enough for designing any practical ultracapacitor module.

4. Examples of partitioning

In this section, several examples are presented to show the advantages of the proposed algorithm. A module of 18 series-connected groups, each of 3 capacitors, is to be designed. There are 54 capacitors (3×18) to be distributed in 18 groups. The nominal value of each capacitor is C_n=350F with a manufacturing tolerance of +20%, that is, the actual capacitance will be always greater than the nominal one. Fig. 6.a shows the normally distributed capacitance values of the capacitors to be grouped. **¡Error! No se encuentra el origen de la referencia.**6.b depicts the relative deviation from the average value of the equivalent capacitance of each group under different grouping strategies.

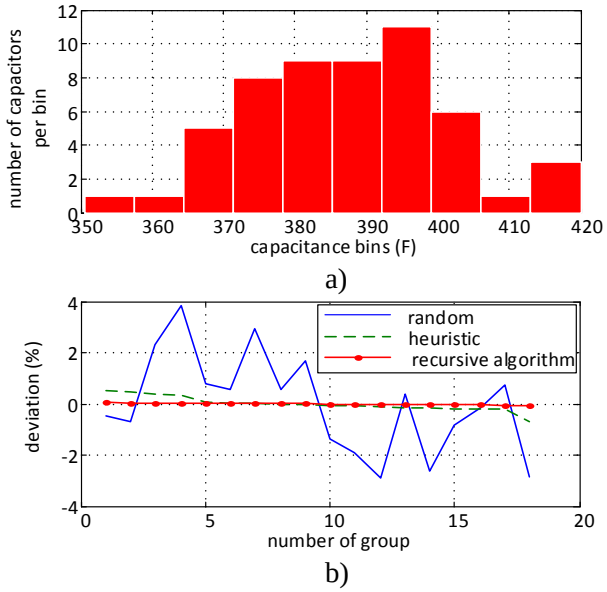


Fig. 6. Grouping example: a) normally distributed initial set of capacitor values, b) resulting equivalent capacitor values of each group under different distribution strategies, percentage deviation from the average value

As can be seen, the more elaborate the grouping strategy, the lower is the dispersion achieved between the equivalent capacitors of different groups. The randomly grouped case has a total dispersion of 6.8%, which is close to the statistically predicted 6.66% [see equation (11)]. The heuristic distribution strategy decreases the dispersion down to 1.36%, whereas, when recursive partitioning algorithm is used, it decreases to 0.137%, that is, ten times better than the previous case. It is obvious that the higher the number of capacitors in parallel, the lower the dispersion achieved. In this case, with only three capacitors in parallel, the proposed algorithm leads to a negligible dispersion of 0.137%, thus achieving a remarkable matching between serialized submodules. In this example, the execution of the distribution algorithm takes only 80msec (Intel Core 2 Duo CPU E7500 @2.93GHz).

In order to check whether the initial distribution of capacitances has any important impact or not in the results, 100 cases, with different normally distributed populations, are processed. Fig. 7.a summarizes the maximum dispersion percentages in all the studied cases. It can be seen that the random-type distribution leads to dispersion levels of a minimum of 4% and a maximum of 10%, average being 6.6%, as predicted. Fig. 7.b shows the vertical zoom of both heuristic-type and recursive-type results. Heuristically, a maximum dispersion of 2.2% is possible, against less than 0.3% by using the proposed recursive algorithm. Thanks to the partitioning-based algorithm, quasi-identical capacitances are assured among different submodules, and thus it is possible to build a module that minimizes the voltage equalizing problem.

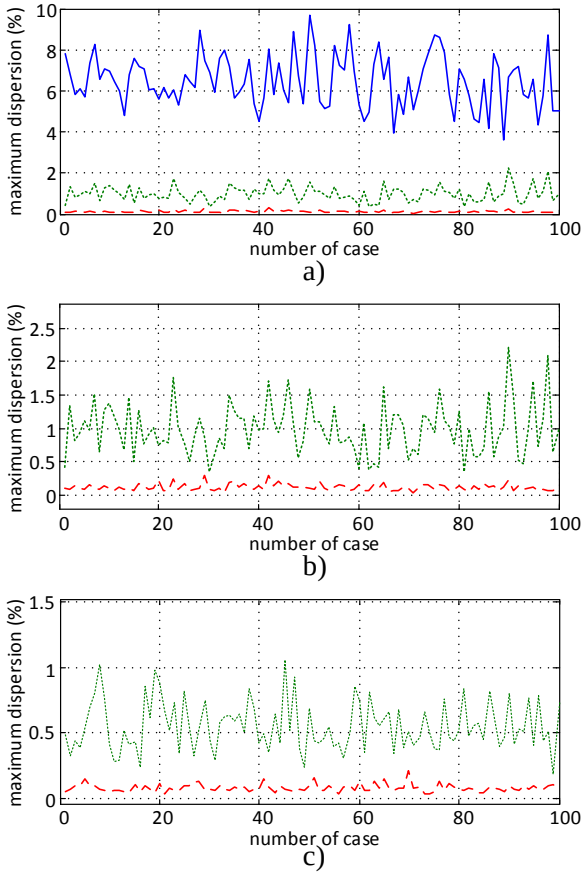


Fig. 7. Maximum dispersion percentage results from a broad set of different initial populations. In all cases the solid line refers to random grouping, dotted line corresponds to the heuristic distribution strategy and dashed line comes from the proposed algorithm: a) normally distributed 100 initial populations, b) zoom of Fig. 7.a, c) randomly distributed 100 initial populations

Though manufacturing processes lead to normally distributed parameters, it is also interesting to check the behavior of the proposed method with randomly distributed

capacitances. Because of that, 100 additional cases of randomly distributed populations of capacitances have been considered. Fig. 7.c shows the maximum dispersion percentage for both heuristic-type and recursive-type cases. Heuristically, a maximum dispersion of 1% is possible, whereas the number partitioning-based algorithm achieves a maximum dispersion below 0.2%. It can be concluded that the proposed algorithm, though simple, achieves practically negligible levels of dispersion.

5. Impact of partitioning-type distribution on expected life

As has been stated in the introduction, the minimizing of capacitance dispersion between series-connected submodules leads to intrinsic voltage equalization and thus to improvement of overall life expectancy of the module. This section shows the expected ageing of different types of modules.

5.1. Electrical and thermal models

Fig. 1.a shows the basic electrical model of the ultracapacitor cell. Considering the simulation step (17)

$$\Delta t(k) = t(k+1) - t(k) \tag{17}$$

The voltage at the cell at simulation step k+1 can be computed using equation (18)

$$V_C(k+1) = V_C(k) + \frac{i_C(k)\Delta t(k)}{C(k)} \tag{18}$$

When a given current $i_C(k)$ crosses the cell some power is lost due to joule effect at its ESR, thus heating the cell by a heating power $P_h(k)$ equal to:

$$P_h(k) = ESR(k)\left[i_C(k)\right]^2 \tag{19}$$

A simple thermal model of a cell is shown at Fig. 1.b, where T_a is the temperature of the air surrounding the cell, T_c represents the cell temperature, R_{thca} is the thermal resistance from the cell case to the air and C_{th} considers the thermal capacitance of the cell. Thus, the cell temperature at simulation step k+1 can be computed using equation (20)

$$T_c(k+1) = T_c(k) + \frac{\Delta t(k)}{C_{th}(k)}\left[P_h(k) - \frac{T_c(k) - T_a}{R_{thca}}\right] \tag{20}$$

The ambient temperature has been kept constant at 35ºC; so, temperature differences will be only due to differences in ESR parameters, which lead to different self-heating phenomena. Though thermal aspects have considerable impact on the ageing of ultracapacitor cells, no further discussion on thermal analysis is proposed here as it would be beyond the scope of this paper.

5.2. Ageing model

The ageing has been computed using the equivalent ageing time proposed in [16]. As it is already known from experiments and data provided by manufacturers, under constant voltage and temperature operating conditions both the capacitance C and the equivalent series resistance ESR exhibit a constant degradation rate. This effect can be modelled by equations (21) and (22),

$$C(k) = C(0)\left(1 + a_C t_{eq}(k)\right) \tag{21}$$

$$ESR(k) = ESR(0)\left(1 + a_R t_{eq}(k)\right) \tag{22}$$

where $C(k)$ and $ESR(k)$ stand for capacitance and ESR values at simulation step k, $C(0)$ and $ESR(0)$ are their initial values and a_C and a_R represent the ageing coefficients if the cell is operated under constant temperature and voltage levels, i.e. T=T_0 and V=V_0, which will be herein denoted as the *reference conditions*, see equations (23)-(24).

$$a_R = \frac{\Delta ESR}{\Delta t} \quad @T = T_0, V = V_0 \tag{23}$$

$$a_C = \frac{\Delta C}{\Delta t} \quad @T = T_0, V = V_0 \tag{24}$$

The variable $t_{eq}(k)$ represents the equivalent amount of life-time that has already been used up, that is, if the operation conditions are harder than the reference ones then $t_{eq}(k) > t(k)$, and reciprocally, if the operation conditions are better than the reference ones we get $t_{eq}(k) < t(k)$. Under constant operating conditions the rate of ageing depends, exponentially, on the temperature and on the voltage. The higher the voltage or the temperature, the higher the ageing, i.e. the larger the total amount of life-time that is being consumed. This phenomena can be modeled by equation (25),

$$t_{eq} = t\, c_T^{\frac{T-T_0}{\Delta T}} c_V^{\frac{V-V_0}{\Delta V}} \tag{25}$$

where c_T and c_V are coefficients that are empirically obtained through tests when the operation conditions differ a given ΔT and ΔV from the reference conditions T_0 and V_0 [16]. The reference conditions are arbitrarily chosen but it is a common practice to set them close to the nominal voltage and to the maximum operating temperature.

In practical cases the temperature and voltage of the cells are not kept constant so equation (17) cannot be directly applied. This problem can be overcome if the simulation step is small enough as to consider quasi-constant temperature $T(k)$ and voltage $V(k)$ values within the simulation step $\Delta T(k)$. From (25) it is straightforward to compute the total amount of life-time $\Delta t_{eq}(k)$ that is being consumed with the simulation step k as:

$$\Delta t_{eq}(k) = \Delta t(k) c_T^{\frac{T(k)-T_0}{\Delta T}} c_V^{\frac{V(k)-V_0}{\Delta V}} \quad (26)$$

Thus the equivalent time $t_{eq}(k+1)$ of any cell at the end of the simulation step k will be equal to the equivalent time at the beginning of the simulation step $t_{eq}(k)$ plus the equivalent time that has been consumed within the simulation step, $\Delta t_{eq}(k)$, see equation (27).

$$t_{eq}(k+1) = t_{eq}(k) + \Delta t_{eq}(k) \quad (27)$$

The work presented in this paper has been carried out using the BCAP350 ultracapacitor from Maxwell Technologies, with the ageing parameters of Table 1.

5.3. Ageing results

Simulations have been run under the MATLAB-SIMULINK environment. The simulation step is set to $\Delta t(k)=1sec$, which is small enough to take into account electrical and thermal dynamics but large enough to perform practical simulations. Anyway, it has to be pointed out that a personal computer (Intel Core 2 Duo CPU E7500 @2.93GHz) requires more than 8 hours if a period of 800 days has to be simulated.

This section shows the expected ageing of three modules, built by the same set of ultracapacitors, but with different topology or grouping strategy. A total of 54 ultracapacitors, with the capacitance distribution shown in Fig. 6.a, have been considered for this purpose. First, the behavior of the all-in-series 54×1 topology has been studied.

Tests conditions have been chosen in such a way that a fast ageing is assured. The 54x1 module is charged and discharged at a constant power of 2.5kW whit a cycling period of 60 seconds. The voltage level of each individual cell is monitored and the charging process stops when any of them reaches the nominal voltage level V_n=2.7V. The discharging process is completed when the voltage of any of the cells falls down to the 40% of the nominal voltage, i.e. down to 1.08V. The charging process lasts around 22 seconds, then the module stands during 8 seconds. Next, the discharging process takes 22 seconds and after a standby of 8 seconds, another cycle starts with a charging process. The resulting power profile is recorded and used as the power-requirement when simulating other modules.

Fig. 8.a shows the evolution of the capacitance parameter of each ultracapacitor. As it has been previously mentioned, the manufacturer provides a positive +20% tolerance range for the capacitance parameter, so initial capacitances at t = 0days are above the nominal C_n=350F value. Looking at Fig. 8.a it is possible to identify the destructive ageing loop: the capacitors with the lower capacitance present the fastest ageing processes. In the example of the figure the worst capacitor has an initial capacitance of C=355F and after 800 days it has fallen down to C=283F, a degradation of 72F. Looking at the best capacitor, it evolves from 410F down to 391F, losing only 19F during its ageing. Consequently, the initial dispersion of ΔC_0=410-355=55F grows up to ΔC=391-283=108F at the end of the test, which represents a 30% of the nominal value.

Fig. 8.b shows the percentage deviation of the capacitance of each ultracapacitor from its initial value. After 800 days of power cycling, one of the capacitors has suffered a deterioration of 20%, which is considered the end-of-life. This capacitor has suffered the destructive ageing loop mentioned earlier. Thus, the entire module must be discarded.

Next, the randomly distributed 18 series of 3 parallel ultracapacitors topology (18×3 topology) has been studied (see Fig. 8.c). As already reported in the literature [14], the statistical minimization of the dispersion between equivalent capacitances, plus the current equalization through different parallel paths, has been responsible for a more homogenous ageing. Thus, after 800 days of operation, the worst capacitance degradation is only 10.2% of the initial capacitance.

Finally, the ageing of an 18×3 module, with partitioning-based distribution of capacitors, has been analysed (see Fig. 8.d). Thanks to the improvement on the capacitance dispersion, the ageing is homogeneous, and therefore the module reaches an ageing of 8.5% after 800 days of operation. Note that even an ideal module built by a set of ideal capacitors with a 0% of manufacturing tolerance suffers an unavoidable ageing of around 8.5%.

From the point of view of module engineering, the proposed distribution strategy avoids ageing acceleration due to voltage imbalance and, as all the ultracapacitors share almost the same voltage, they can be operated at nominal voltages during fast charging processes. It is possible to compare the energy storage ability of different modules. The theoretical usable energy offered by an ideal module built by N cells of C_n capacitance each, evolving from V_{min} to V_n, is:

$$W_{Mu\_th} = N \frac{1}{2} C_n \left(V_n^2 - V_{\min}^2 \right) \quad (28)$$

The actual usable energy, W_{Mu} can be computed as

$$W_{Mu} = \frac{1}{2} \sum_{i=1}^{N} C_i \left(V_{i\max}^2 - V_{i\min}^2 \right) \quad (29)$$

Due to ageing phenomena, individual capacitance values C_i decrease and the dispersion between serialized capacitors or submodules increases. The increment of the capacitance dispersion implies lower maximum voltages $V_{i\,\max}$ and higher minimum voltages $V_{i\,\min}$. Therefore, due to ageing phenomena all the parameters involved in equation (29) evolves in such a way that the actual usable energy W_{Mu} decreases.

It is possible to define the so called “efficiency of use”, η_u , as the relationship between the actually usable energy W_{Mu} (29) and the total amount of energy $W_{M\,\max}$ (30) that theoretically can be stored in an ideal module built by ideal capacitors, see equation (31).

$$W_{M\max} = N\frac{1}{2}C_n V_n^{\,2} \quad (30)$$

$$\eta_u = 100 \times \frac{W_{Mu}}{W_{M\max}} \quad (31)$$

Fig. 8.e shows the evolution of the efficiency of use of the studied modules during the ageing process. The ideal module built by ideal capacitors of C_n=350F leads to a theoretical and constant efficiency of use of 84%. As actual initial values of capacitors are above the nominal one, initial efficiency of use of modules are higher than the theoretical one. The optimally distributed 18×3 module offers an initial 92% efficiency of use, the randomly distributed 18×3 module has an initial efficiency of use of 90% and the all-in-series 54×1 module exhibits the lowest initial efficiency of use of 85%. After 800 days of ageing the improved 18×3 module has the best figure with an efficiency of use of 84%. This means that, thanks to the initial positive tolerance (initial capacitances higher than the nominal one) and the adequate grouping strategy, the improved 18×3 module offers, after more than two years of ageing, the equivalent of the initial theoretical efficiency of use. The 54×1 module is below the nominal efficiency of use after only 80 days, and after 800 days the efficiency of use has fallen down to 68%.

5.4. Discussion

The module building method proposed herein offers several advantages and some drawbacks. The main advantages are obtained when applied to cases with high-power charging rates, where it is possible to increment the expected life-time of modules that do not include a full-power active balancing system. This advantage can be inversely exploited, that is, given a targeted life-time, a more economical version of the module can be built. Additionally, full-power voltage equalizing circuits can be downgraded or even completely removed. As it has been previously pointed out, full-power voltage equalizing methods are expensive but are usually required when a conventional ultracapacitor module needs to operate up to its maximum theoretical usable energy. Thanks to the intrinsic voltage equalization achieved, the proposed method improves the efficiency of use, maximizing the available usable energy.

If the thermal engineering assures a quasi-homogenous ambient temperature surrounding all the cells, the dispersion of parameters is negligible and, therefore, no voltage-equalizing device is required. If this is not the case and ultracapacitor cells withstand important temperature differences, parameter dispersion will increase and, consequently, an active voltage equalizing device would still be required.

It has to be noted that, in the presence of parameter dispersion, if a perfect voltage balance is required, the equalizing power must match the nominal charging power.

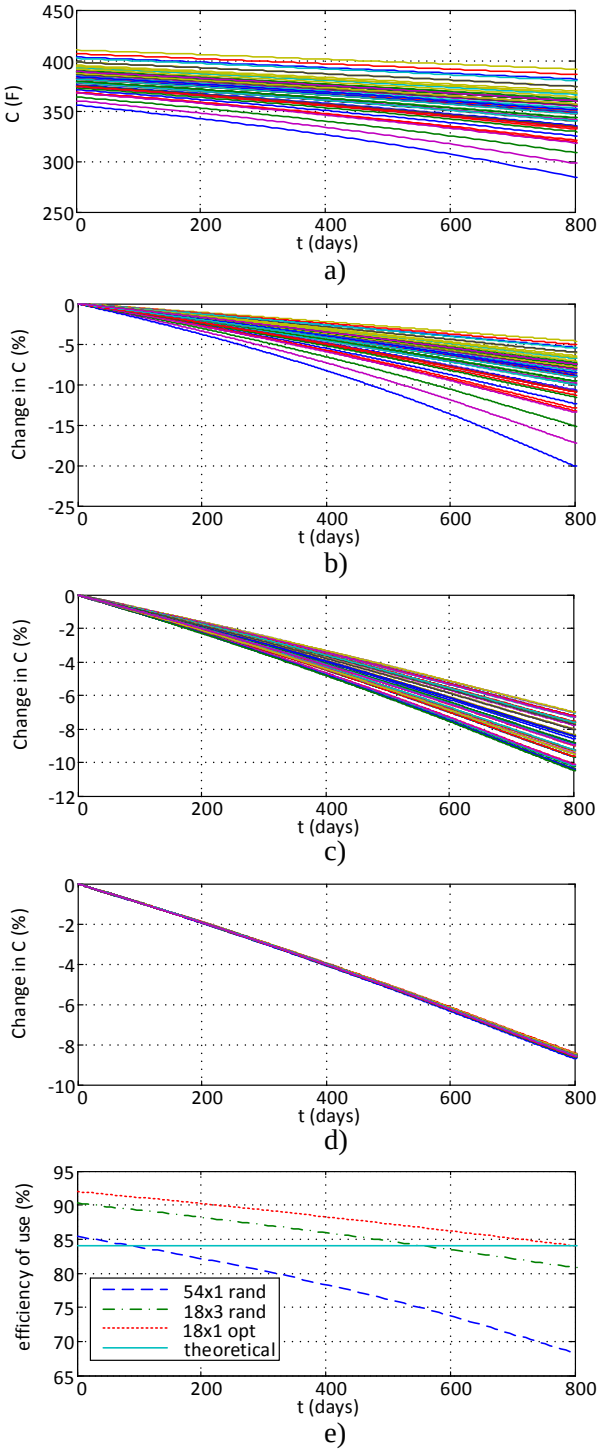


Fig. 8. Ageing results: a) capacitance evolution of the all-in-series 54×1 configuration, b) per-unit capacitance evolution of the all-in-series 54×1 module, c) per-unit capacitance evolution of the 18×3 randomly grouped topology, d) per-unit capacitance evolution of the 18×3 module with partitioning-based ultracapacitor distribution and e) evolution of the efficiency of use

A downgraded equalizing power leads to imperfect voltage equalization; the voltage dispersion level will depend on the part of the power that is not equalized and on

the capacitance dispersion level. Thus, even in the case that a thermal issue generates some parameter dispersion, thanks to the proposed method, the resulting efficiency of use could be inside the required specifications. If this is not the case, a downgraded equalizing system could be enough to achieve the desired efficiency of use.

One of the possible drawbacks of the proposed method is that, apparently, it should be more complex and expensive to place several cells in parallel instead of a single larger cell with an equivalent capacitance. E.g., considering the 18×3 module previously studied, built by capacitors of 350F, it should be possible to get an equivalent 18×1 module built by single 1050F capacitors. At first sight, the 18×1 equivalent topology should be simpler, cheaper and, as there are fewer elements, more reliable. But a thorough analysis shows that actually things are not this way:

- It is true that the manufacturing cost per farad decreases when the capacitance increases, but production volume must be also considered. The fact is that thanks to a larger production volume, ultracapacitors around 310-350F offers the same cost per farad than larger ultracapacitors of around 1500 or 3000F. Actually, 310-350F ultracapacitors lay in a low-cost niche within the ultracapacitors range.
- In the same way, it is apparently cheaper to connect only one large ultracapacitor instead of three or more small ones in parallel. But ultracapacitors around 310-350F can be still soldered to PCBs whereas larger cells require screw-bolt connections in complex mechanical set-ups, which are more expensive. Additionally, voltage monitoring electronics must be added, which is simpler and more reliable to achieve in the all-in-one PCB topology of small ultracapacitors than in the screw-bolt mechanical structure of larger ultracapcitors, where multiple signal connectors are required.
- Considering reliability, it has been already proven [14] than the topology adopted herein is more reliable and robust against faults than the single string of larger cells in series.

The proposed method has some drawbacks related to two additional manufacturing steps. First, each single cell must be labelled and its capacitance must be measured before the module is assembled. Second, cells must be inserted according to its optimal position. The individual measuring process is the only item that could add a significant cost to the overall manufacturing process. As a matter of fact, some manufacturers offer measured and labelled cells with a cost increment of only 10%, which is smaller than the savings achieved by the improvement of the efficiency of use and by downgrading or removing the active voltage equalizing device. Therefore, the advantages of the proposed method prevail.

6. Conclusions

When an ultracapacitor-based storage module is intended for high power-cycling applications, active voltage equalizing systems must be rated at full power, and thus the module becomes expensive. This paper has shown that an alternative method, based on a judicious grouping of the capacitors, can be used. Thanks to partitioning-based algorithms, it is possible to build an ultracapacitor module with several submodules in series, having almost the same equivalent capacitance value; in other words, intrinsic voltage equalization can be achieved. This improvement can be exploited in two ways: First, more energy can be stored in the same set of ultracapacitors; second, the overall ageing of the module can be improved. The proposed method does not add relevant costs but achieves important improvements.

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