

A rail-to-rail differential quasi-digital converter for low-power applications

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Abstract This paper presents an ultra low power differential voltage-to-frequency converter (dVFC) suitable to be used as a part of a multisensory interface in portable applications. The proposed dVFC has been designed in 1.2-V 0.18- μm CMOS technology, and it works properly over the whole differential input range (0.6 ± 0.6 V) providing an output frequency range of 0.0–0.9 MHz. The system has been tested for temperature variations from -40 to $+120$ °C and supply voltage variations of up to 30 %, being the maximum linearity error in the worse case of 0.017 %. Simulations against common mode voltage variations show a deviation in the output frequency of 0.4 %. This dVFC has power consumption below 60 μW , and it includes an enable terminal that sets the system in a sleep mode (180 nW) while no conversion is request. The dVFC occupies an active area of $250 \mu\text{m} \times 150 \mu\text{m}$.

Keywords CMOS mixed integrated circuits · Low-voltage low-power · Sensor interface · Voltage-to-frequency converter

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1 Introduction

At present, the use of wireless sensor networks (WSN) is continuously growing. Therefore, the development of smart sensors has increased due to the need for the sensor signal to be compatible with digital signal processors. A smart sensor includes, besides the sensing device, the interface so that the output is a digital signal related to the measured magnitude. Thus, due to the large amount of sensors involved in these networks, the use of low-cost analog sensors along with a programmable interface is the preferred choice if cost reduction becomes a priority. The interface has to be capable of adapting every sensor output to the input digital port requirements of the microcontroller (μC) embedded in each sensing node.

The simplest interface consists of an analog-to-digital converter (ADC) preceded by a programmable voltage adapter that adjusts the sensor output range to the ADC input range by means of gain and offset controls. However, in embedded microcontroller measurement systems, such as WSN, the use of voltage-to-frequency converters (VFC), also known as quasi-digital converters, have risen as a highly suitable alternative to the standard analog-to-digital conversion due to its advantages: the quasi-digital frequency signal offers high noise immunity and can straight interface the microcontroller, which next performs the final digitalization using its internal timers [1].

There are several types of VFCs, being the charge balance and the multivibrator the most common approaches. Although the charge balance VFC is more accurate than its multivibrator based counterpart, the former is also more complex and it demands more power than the latter [2], which provides sufficient accuracy to be used with low cost sensors used in WSNs. Therefore, recently reported low-voltage low-power CMOS VFCs are mainly based on an input voltage-to-

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62 current converter (VIC) followed by a multivibrator based
 63 current-to-frequency converter (IFC) and they operate in
 64 single-input mode [3, 4]. However, for certain sensor con-
 65 ditioning applications, such as the widely used Wheatstone
 66 bridge, or for noise rejection, differential signal processing
 67 would be desirable. Previous approaches to design CMOS
 68 differential VFCs also employ a VIC followed by an IFC
 69 approach, being the input differential VIC based on a dif-
 70 ferential amplifier with voltage controlled gain [5], an
 71 instrumentation amplifier [6] or a second generation current
 72 conveyor [7]. However, they present serious limitations in
 73 terms of input operating range, power consumption or
 74 important temperature dependence. Preliminary designs of
 75 the structure that is going to be introduced in this paper have
 76 been presented by the authors at two recent conferences [8, 9].
 77 In addition, the proposed dVFC is a simplified and revisited
 78 version of the VFC presented at another conference [10],
 79 advancing towards ultra low-power consumption. Thus, in
 80 this final design, the biasing circuit has been improved to
 81 show a temperature independent behavior and a global enable
 82 has been included to set the system into an extremely low-
 83 power state while no measure is done. Further, to reduce
 84 power, OTAs are the simplest ones and the power manage-
 85 ment made in the control circuit has been corrected.

86 Therefore, the goal of this paper is the design and
 87 complete verification of a novel CMOS differential VFC
 88 fulfilling the following major requirements to fit WSN
 89 applications: low-voltage, compatible with the single-cell
 90 batteries used in the WSN market; low-power, in order to
 91 optimize battery life; rail-to-rail operation, since taking
 92 advantage of the full V_{DD} range results in enhanced reso-
 93 lution in the subsequent digitalization; the output levels
 94 have to be compatible with the μC logic levels and the
 95 output range must fit typical low-power μC clock fre-
 96 quencies (4 MHz). Finally, it is desirable that the VFC has
 97 temperature compensation and supply regulation to main-
 98 tain constant sensitivity. Section 2 explains the proposed
 99 rail-to-rail temperature and supply independent differential
 100 VFC. Section 3 reports the main results obtained for a 1.2-
 101 V 0.18- μm CMOS implementation and conclusions are
 102 drawn in Sect. 4.

103 2 Differential voltage-to-frequency converter

104 2.1 Operation principle

105 The proposed differential voltage-to-frequency converter
 106 (Fig. 1) consists of a differential voltage-to-current converter
 107 (dVIC) followed by a bidirectional current integrator driven
 108 by a voltage window comparator (VWC) control circuit.

109 The input dVIC [Fig. 2(a)], as it will be explained
 110 thoroughly in Sect. 2.2, transforms the input signals

111 $V_{in+} = V_{CM} + V_d/2$ and $V_{in-} = V_{CM} - V_d/2$ into signals
 112 $V_A = V_{CM} + V_d/4$ and $V_B = V_{CM} - V_d/4$ at nodes A and
 113 B, respectively. Note that the differential input voltages
 114 $V_{in+} - V_{in-} = V_d$ must be positive. Therefore a sign cir-
 115 cuit (explained in Sect. 2.6) can be required. Voltages V_A
 116 and V_B generate across resistor R_S the current signal
 117 $I_d = V_d/2R_S$, which is next directly replicated through
 118 transistors T_3 and T_4 with a scaling factor given by $K:1$.

119 The scaled current I_d/K alternately charges and dis-
 120 charges a grounded capacitor C between the stable limits
 121 V_L and V_H of a VWC. The comparison results V_{CL} , V_{CH} are
 122 driven to a simple NAND-based RS flip-flop, which grants
 123 a stable output signal and provides the switching signals
 124 S_{DW} and S_{UP} that drive the gates of cascode transistors T_{3C}
 125 and T_{4C} , thus determining the direction of the current in the
 126 bidirectional current integrator. In this way, a repeated loop
 127 is built with a frequency of oscillation given by:

$$f_0 = \frac{I_d/K}{2C(V_H - V_L)} = \frac{1}{2C(V_H - V_L)} \frac{V_d}{2KR_S} \quad (1)$$

2.2 Differential voltage-to-current converter

131 The rail-to-rail dVIC is shown in Fig. 2(a). OTA_{VF1} and
 132 OTA_{VF2} are feedback voltage attenuation OTAs [11],
 133 which do not act as voltage followers but attenuate the
 134 input signal to keep transistors $T_1 - T_{1C}$ and $T_2 - T_{2C}$ in
 135 saturation region over the complete input range, so that the
 136 output current mirroring does not restrict the V-I operating
 137 range. To achieve this, let us focus on OTA_{VF1} , whose
 138 complete scheme is shown in Fig. 2(b). Between the main
 139 OTA_1 non-inverting input –at a voltage V_{in+} due to neg-
 140 ative feedback– and node A, an attenuator is introduced,
 141 implemented using a non-inverting amplifier stage formed
 142 by $\text{OTA}_{aux1} - T_{A1}$, an input resistor R_1 biased at V_1 and
 143 feedback resistor R_2 . By means of a straightforward anal-
 144 ysis, the voltage at node A is

$$V_A = \frac{R_2 V_1 + R_1 V_{in+}}{R_1 + R_2} \quad (2)$$

146 The voltage level V_1 is fixed to V_{CM} and resistors are set
 147 to $R_1 = R_2$, so that $V_A = V_{CM} + (V_d/4)$. Similarly, for
 148 OTA_{VF2} , again selecting the auxiliary voltage level
 149 $V_2 = V_{CM}$ and input and feedback resistors $R_3 = R_4$, the
 150 voltage at node B is

$$V_B = \frac{R_4 V_2 + R_3 V_{in-}}{R_3 + R_4} \quad (3)$$

152 This results in a fully symmetric structure, which
 153 maintains at nodes A and B the common mode voltage
 154 V_{CM} while the differential voltage V_d is halved. Therefore,
 155 the voltage across resistor R_S is $(V_A - V_B) = (V_d/2)$, and
 156 thus, a current $I_d = V_d/2R_S$ is generated.

Fig. 1 Block diagram of the proposed differential VFC

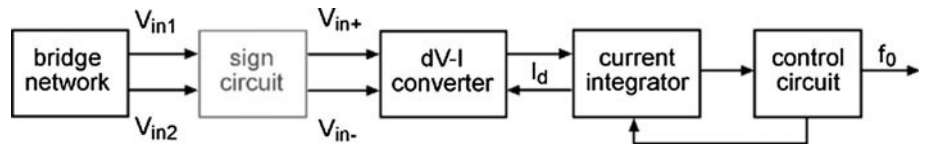
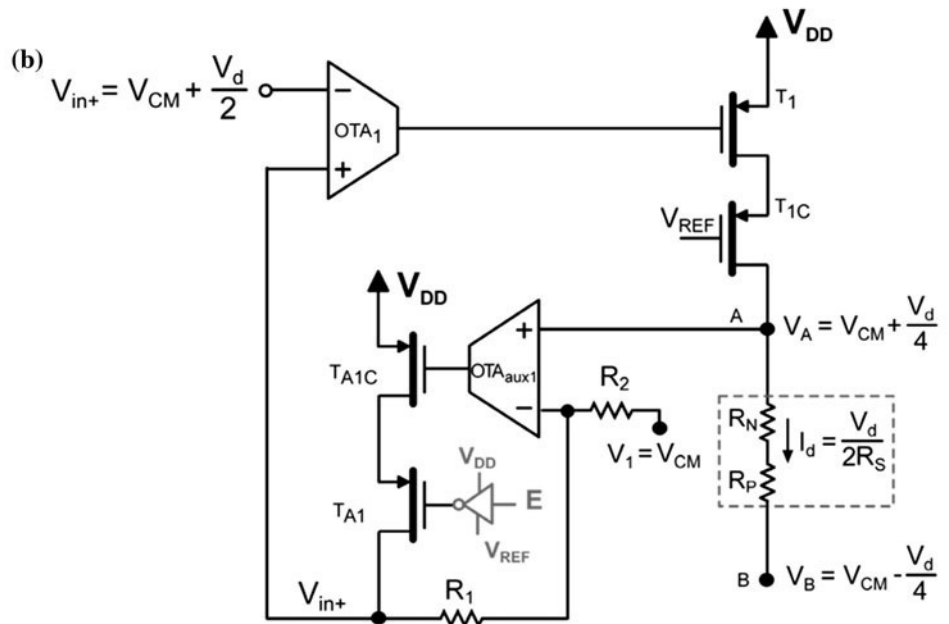
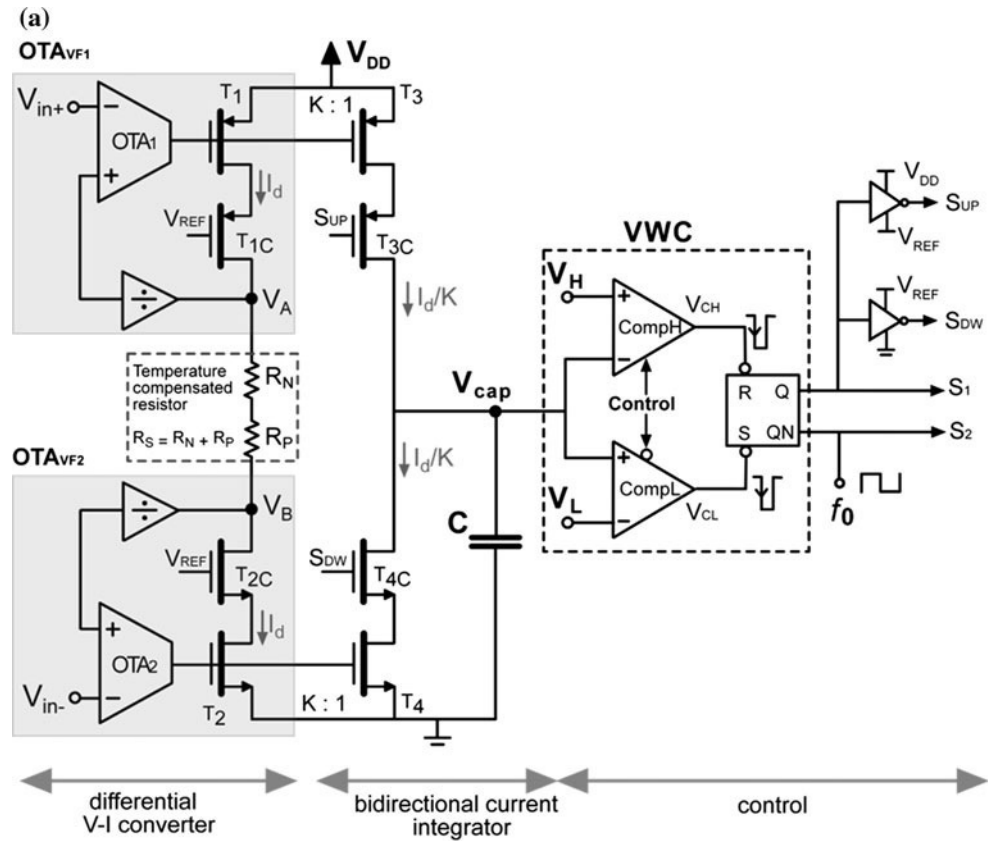


Fig. 2 Schematics of a proposed dVFC and b OTAVF1



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157 As the input of both OTAs in OTA_{VF1} swing between
 158 V_{CM} and V_{DD} , they are made up using the simple NMOS
 159 input stage OTA shown in Fig. 3, to reduce both, the area
 160 and the power consumption. In the same way, as the input of
 161 both OTAs in OTA_{VF2} swing between GND and V_{CM} , they
 162 are made up of a simple PMOS input stage OTA, formed by
 163 the counterpart of the structure shown in Fig. 3. The resistor
 164 that makes the voltage-to-current conversion, R_S , is set to
 165 $R_S = 40 \text{ k}\Omega$ and $R_1 = R_2 = R_3 = R_4 = 25 \text{ k}\Omega$, as a trade-
 166 off between power and area consumptions.

167 All OTAs work in the subthreshold region over all the
 168 input range to reduce power consumption, and they have a
 169 compensation network (a conventional $R_C - C_C$ network,
 170 not shown) to guarantee the system stability, while
 171 avoiding peaks in the closed-loop frequency response and
 172 underdamped oscillations [12].

173 2.3 Current integrator and control circuit

174 The generated current I_d is driven through transistors T_1
 175 and T_2 , and replicated through transistors T_3 and T_4 with a
 176 scaling factor $K:1$, being $K = 20/3$, in order to optimize the
 177 power consumption, while obtaining a suitable sensitivity
 178 in the dVFC. Cascode transistors are used to improve the
 179 current copy, but also because they work as the switching
 180 elements controlling the direction of the current: let us
 181 assume that the outputs of the VWC are $S_1 = '1'$ and $S_2 =$
 182 $'0'$, so that the switching signals that drive the gate of the
 183 cascode transistors T_{3C} and T_{4C} are $S_{UP} = V_{REF}$ and
 184 $S_{DW} = GND$ respectively. Thus, transistor T_{3C} is ON and
 185 T_{4C} is OFF, so that the current charges the capacitor C until
 186 the voltage V_{cap} reaches the comparison limit V_H . At that
 187 moment, the output of the upper comparator changes to $'0'$,
 188 what makes the VWC output signals change, being $S_1 =$
 189 $'0'$ and $S_2 = '1'$, and the switching signals $S_{UP} = V_{DD}$ and
 190 $S_{DW} = V_{REF}$, setting transistor T_{3C} in OFF and transistor

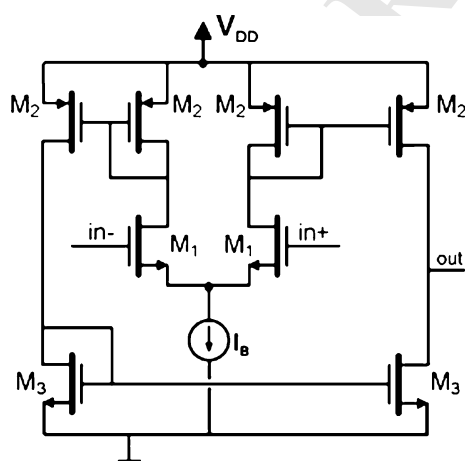


Fig. 3 Schematics of the NMOS OTA

T_{4C} in ON. Thus, the current discharges the capacitor until
 it reaches the lower limit V_L , starting again the charging
 phase. For both the NMOS and PMOS cascode transistors
 the gate voltage is set to $V_{REF} = 0.4 \text{ V}$ for simplicity. The
 integrating capacitor is set to $C = 3.125 \text{ pF}$.

The VWC is made up of two high-speed continuous-
 time simple differential pairs followed by inverters, shown
 in Fig. 4, and a NAND-based RS flip-flop. Transistors of
 the VWC employ minimal length to optimize speed.
 Comparison limits are set to $V_L = 0.4 \text{ V}$ and $V_H = 0.8 \text{ V}$
 to keep transistors T_3 and T_4 working in the saturation
 region.

Therefore, taking into account the chosen values, the
 output frequency in Eq. (1) is now given by

$$f_0(\text{MHz}) = 0.75V_d(V) \quad (4)$$

2.4 V_{DD} and temperature dependence

Insensitivity to power supply variations is always desired,
 but it is even more important in battery operated systems,
 where the supply voltage continuously decreases. Thus, a
 simple solution to generate the bias current that reduces the
 power supply sensitivity is a conventional beta-multiplier
 referenced self-biasing circuit, shown in Fig. 5, that is used
 to set $I_B = 0.5 \mu\text{A}$ [13]. Taking into account that all tran-
 sistors work in subthreshold region, the current I_B is given
 by

$$I_B = \frac{nV_T}{R} \ln \alpha \quad (5)$$

where n is the emission coefficient, V_T is the thermal
 voltage (26 mV at room temperature) and $\alpha = 6$ is the
 scaling factor between M_4 and M_5 .

Note that (5) is, in first order, power supply independent.
 With respect to temperature, I_B presents a positive variation
 due to the thermal coefficients of V_T and n . This variation
 can be compensated if the resistor $R = 115.6 \text{ k}\Omega$ is
 implemented featuring the same positive variation. The
 temperature variation of a resistor is given by

$$R(T) = R_0 \left(1 + TC_1(T - 25) + TC_2(T - 25)^2 \right) \quad (6)$$

where R_0 is the resistor value at room temperature and TC_1
 and TC_2 the first and second order temperature coefficients,
 respectively. Thus, R is made up with the serial connection
 of two resistors A and B with different thermal coefficients,
 being the composite resistor thermal coefficients given by

$$TC_i = TC_{i,A}(\beta/(1 + \beta)) + TC_{i,B}(1/(1 + \beta)) \quad (6)$$

where $\beta = R_{0,A}/R_{0,B}$ is the ratio of resistances at room
 temperature [14], being $i = 1, 2$ the order of the temper-
 ature coefficient. The composite resistor is made up with a
 NWELL
 $(TC_1 = 2.504 \times 10^{-3} \text{ } ^\circ\text{C}^{-1}$,

Fig. 4 Schematics of the comparators forming the VWC

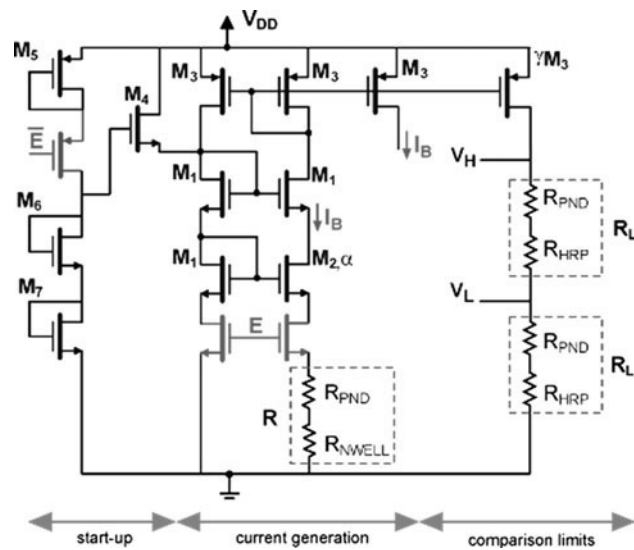
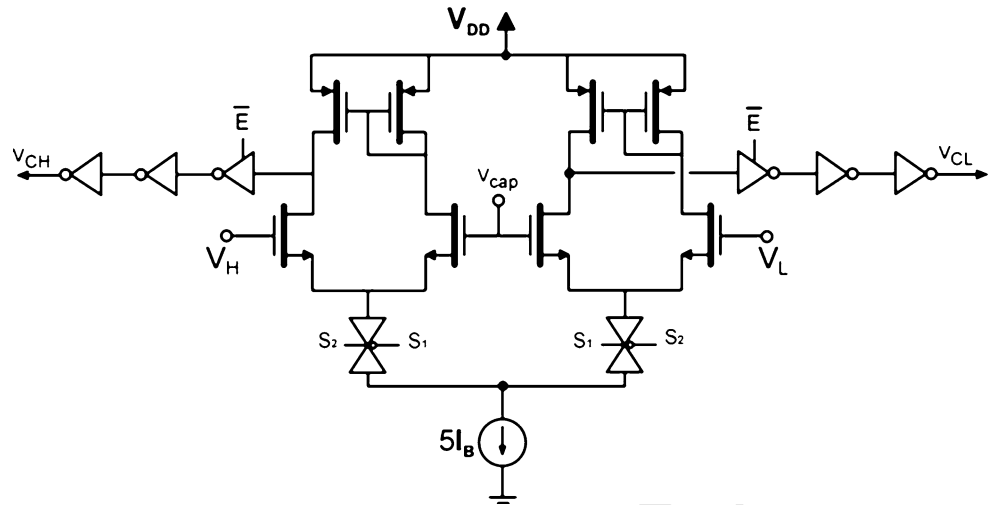


Fig. 5 Schematics of the β -multiplier reference circuit

238 $TC_2 = 8.566 \times 10^{-6} \text{ }^\circ\text{C}^{-2}$) and a P⁺ nonsalicide diffu-
 239 sion (PND) ($TC_1 = 1.184 \times 10^{-3} \text{ }^\circ\text{C}^{-1}$, $TC_2 = 7.310 \times$
 240 $10^{-7} \text{ }^\circ\text{C}^{-2}$) resistors, being their ratio $\beta = 20/17$, and
 241 $TC_1 = 1.791 \times 10^{-3} \text{ }^\circ\text{C}^{-1}$, $TC_2 = 4.355 \times 10^{-6} \text{ }^\circ\text{C}^{-2}$
 242 the composite thermal coefficients, that compensate the
 243 temperature variation of V_T and n .

244 The VWC comparison limits, V_H and V_L , can be
 245 obtained from the generated I_B as shown in Fig. 5, being
 246 $V_L = 8I_B R_L$ and $V_H = 8I_B 2R_L$. Therefore, to achieve V_{DD}
 247 and T independent comparison limits, the resistors R_L are
 248 implemented with the serial connection of two resistors, R_P
 249 and R_N with opposite temperature coefficients [9]. This is
 250 achieved by implementing R_N with a high resistive poly-
 251 silicon (HRP) layer ($TC_1 = -8.34 \times 10^{-4} \text{ }^\circ\text{C}^{-1}$, $TC_2 =$
 252 $1.30 \times 10^{-6} \text{ }^\circ\text{C}^{-2}$) and R_P with PND, being their ratio that
 253 immunizes the resistor against temperature variations $\beta =$
 254 1.5, and the final thermal coefficients $TC_1 = -2.68 \times$

255 $10^{-5} \text{ }^\circ\text{C}^{-1}$, $TC_2 = 9.08 \times 10^{-7} \text{ }^\circ\text{C}^{-2}$. To generate $V_H =$
 256 0.8 V and $V_L = 0.4$ V, the resistor $R = 100 \text{ k}\Omega$ as a
 257 compromise between area and power consumption, and it
 258 is implemented with $R_P = 60 \text{ k}\Omega$ and $R_N = 40 \text{ k}\Omega$.

259 With V_H and V_L supply and temperature independent,
 260 the remaining temperature dependence of the circuit is
 261 mainly due to resistor R_S . Therefore, it is implemented in
 262 the same way as R_L ($R_{PND} = 16 \text{ k}\Omega$, $R_{HRP} = 24 \text{ k}\Omega$).

263 This temperature compensation seems to be highly
 264 process dependent. However, the value of ten composite
 265 resistors ($R_{PND} + R_{HRP}$) have been measured by using a
 266 4-wires technique, obtaining a 0.13 % dispersion between
 267 measured resistors with a maximum deviation of 4.1 %
 268 with respect to its nominal value, which shows that there is
 269 a need of a gain calibration in a fabricated dVFC. The
 270 composite resistors were next tested against temperature
 271 variations, varying less than 1.6 % over all the temperature
 272 range ($-40, +120 \text{ }^\circ\text{C}$), which proves that the adopted
 273 temperature compensation technique is correct. If this
 274 technique is desired to be migrated to a different process/
 275 technology, the ratio β among two resistors with different
 276 temperature coefficients should be recalculated to obtain a
 277 composite resistor that exhibits final first and second order
 278 temperature coefficients that minimize the temperature
 279 dependence.

280 Note that R_1, R_2, R_3 and R_4 do not need to be temper-
 281 ature compensated neither have accurate specified values
 282 because as long as they are well matched their ratio will
 283 remain constant. Therefore they are implemented using a
 284 HRP layer to optimize area.

285 **2.5 Power consumption considerations**

286 Power consumption is a key parameter in battery operated
 287 systems. Therefore, a power reduction technique based on
 288 the alternate operation of the comparators is introduced by

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289 adding transmission gates (as shown in Fig. 4): in the
290 charging phase, the only comparator working is the high
291 comparator whereas in the discharging phase, the only one
292 that works is the low comparator.

293 In addition, an enable terminal has been included to set
294 the VFC into a low-power mode with 180 nW power dis-
295 sipation most of the time, waking up just to perform the
296 calibration, frequency measurements and digital conver-
297 sions, then returning to the sleep mode. The enable acts
298 mainly in the β -multiplier reference circuit to no generate
299 the biasing current and the comparison limits, but it also
300 acts in the first inverter of each of the comparators con-
301 forming the VWC, fixing the digital state of each of the
302 remaining inverters.

303 2.6 Sign circuit

304 In order to assure the proper operation of the circuit, a sign
305 circuit can be required. It is implemented by means of a rail-to-
306 rail comparator and transistors acting as switches, as shown in
307 Fig. 6. The comparator is made up with an open-loop OTA
308 equal to the one in Fig. 3 but with two complementary dif-
309 ferential input amplifier stages in parallel to achieve rail-to-
310 rail performance, followed by inverters. When $V_{in1} > V_{in2}$,
311 $V_C = V_{DD} \equiv '1'$ and $V_{CN} = GND \equiv '0'$, so that T_5 and T_7
312 are ON and T_6 and T_8 are OFF; therefore, $V_{in+} = V_{in1}$,
313 $V_{in-} = V_{in2}$. Conversely, when $V_{in1} < V_{in2}$, $V_{in+} = V_{in2}$ and
314 $V_{in-} = V_{in1}$.

315 3 Post-layout results

316 Figure 7 shows the layout of the proposed dVFC, designed
317 in a low-cost 0.18 μm CMOS technology from UMC with
318 a single supply of 1.2 V. Power consumption is below
319 60 μW (180 nW in power down) and the active area is
320 250 $\mu\text{m} \times 150 \mu\text{m}$, dominated by the β -multiplier circuit
321 and the capacitors.

322 Figure 8(a) shows the variation of the normalized I_B and
323 $V_H - V_L$ over the ($-40, +120$ $^\circ\text{C}$) temperature range: I_B
324 varies 52.5 pA/ $^\circ\text{C}$ while $V_H - V_L$ varies 29.4 $\mu\text{V}/^\circ\text{C}$.
325 Figure 8(b) shows the variation of the normalized I_B and
326 $V_H - V_L$ over a 1.0–1.4 V supply voltage range. In this case
327 I_B varies 4.5 nA/V and $V_H - V_L$ 11.3 mV/V.

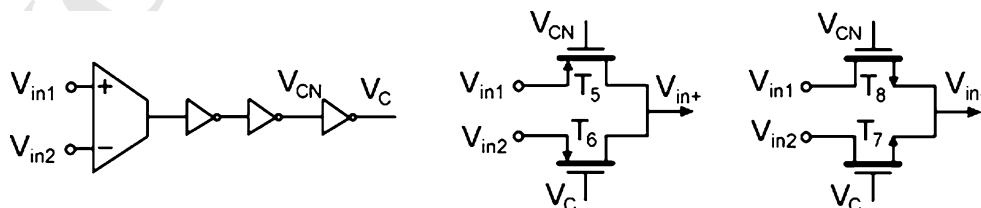


Fig. 6 Schematics of the sign circuit

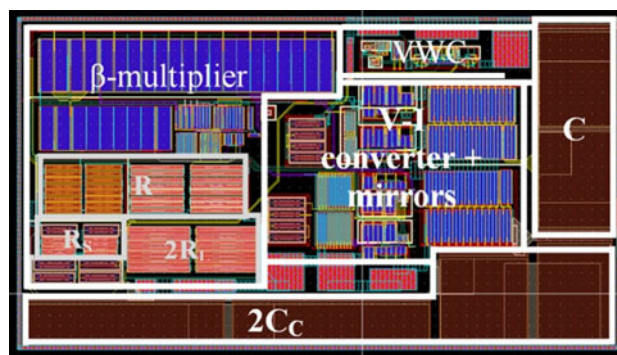


Fig. 7 Layout of the proposed dVFC

328 There are some errors that define the dVFC linearity: the
329 gain or sensitivity error is the deviation in slope of the
330 actual dVFC from the ideal one; the offset error, which is a
331 constant frequency added to the output frequency, com-
332 puted as $(f_{0,sim}(V_{in,min}) - f_{0,the}(V_{in,min}))$, expressed in Hz
333 where $f_{0,sim}$ is the simulated value and the theoretical value
334 $f_{0,the}$ is given from Eq. (4); the relative error, without offset
335 and gain calibration, computed as $(f_{0,sim} - f_{0,the})/f_{0,the}$; and
336 the main parameter, since it will define the maximum
337 achievable number of bits in the frequency-to-code con-
338 version, is the linearity error, which is calculated as the
339 deviation of a straight line passing through the experimental
340 VFC points. As with most precision circuitry, through
341 adequate calibration processes gain and offset errors can be
342 trimmed by the user in the microcontroller. However, this
343 does not happen with the linearity error, which is inherent to
344 each VFC topology. The linearity error can be thus con-
345 sidered a fundamental parameter, and the smaller the line-
346 arity error, the better the VFC. The offset errors are mainly
347 due to mismatching in the OTAs differential pairs as well as
348 to a non-ideal current copy across $T_1 - T_3, T_2 - T_4$. Gain
349 errors are mainly due to deviations in the charging capacitor
350 C , in the resistors R_S that converts the differential input
351 voltage into a current and in the resistors R_L that provides
352 the comparison limits V_H and V_L of the VWC, and it is also
353 due to mismatching in the differential pairs of the compar-
354 ators forming the VWC. Therefore, a calibration with
355 two points can be made in the microcontroller to obtain the
356 experimental gain and offset of the dVFC, thus being able to
357 establish the $V_{in} - f_0$ relationship accurately.

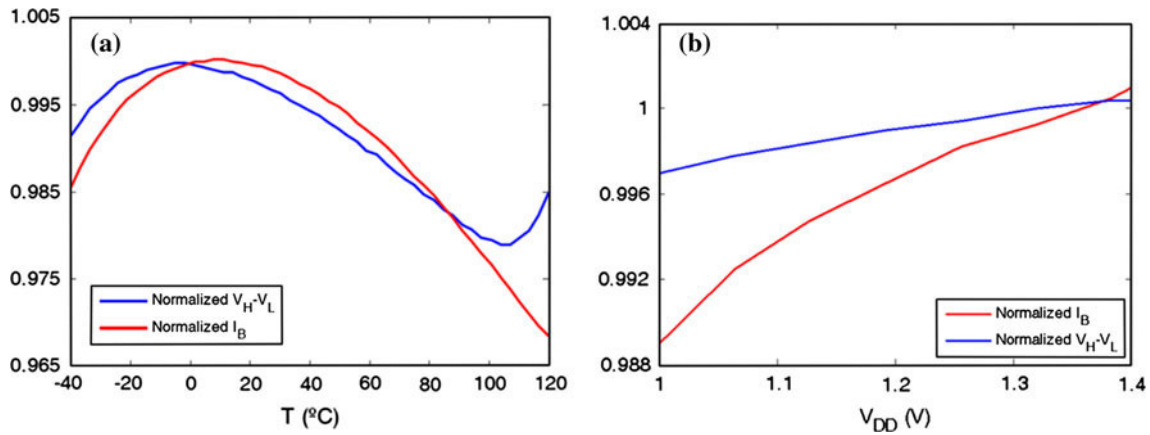


Fig. 8 Normalized I_B and V_H-V_L over a $(-40, +120\text{ }^\circ\text{C})$ temperature range and b $(1.0, 1.4\text{ V})$ supply range

358 At room temperature, with the nominal supply of 1.2 V
 359 and a common mode voltage of $V_{CM} = V_{DD}/2 = 0.6\text{ V}$ the
 360 output frequency varies linearly between 0.0 and 0.9 MHz
 361 with a gain error of 2.9 %, an offset error of 2.8 kHz, a
 362 maximum relative error of 4.1 %, and a linearity error of
 363 0.002 % for an input range of $(0.6 \pm 0.6\text{ V})$.

364 Figure 9(a) shows the output frequency f_0 over the input
 365 range at different temperatures, from -40 to $+120\text{ }^\circ\text{C}$, and
 366 Fig. 9(b) shows f_0 over the input range for different supply
 367 voltages, being $V_{CM} = V_{DD}/2$.

368 Over all the $(-40, +120\text{ }^\circ\text{C})$ temperature range, the
 369 maximum gain error is 4.5 %, the maximum offset error is
 370 3.1 kHz, the maximum relative error is 8.7 %, and the linearity
 371 error remains below 0.014 %. When the system is
 372 simulated for 30 % supply voltage variations $(1.2 \pm 0.2\text{ V})$,
 373 the input range varies accordingly; however, the errors
 374 remain bounded: the maximum gain error is 6.1 %, the
 375 maximum offset error is 3.8 kHz, the maximum relative
 376 error is 8.9 %, and the linearity error remains below
 377 0.005 %. In the worst case ($V_{DD} = 1\text{ V}$, $T = -40\text{ }^\circ\text{C}$) the
 378 linearity error remains below 0.017 %.

379 The system has also been tested against $V_{CM} = 0.6 \pm$
 380 0.3 V variations at the nominal $V_{DD} = 1.2\text{ V}$ supply vol-
 381 tage. The frequency remains nearly constant with a maxi-
 382 mum variation of 0.4 % with respect to the frequency at
 383 $V_{CM} = 0.6\text{ V}$.

384 A Monte Carlo analysis has been carried out varying in
 385 3σ the process and mismatch foundry models in order to
 386 see the effect of mismatching. For 20 iterations, and over
 387 different single and differential input voltages, the varia-
 388 tion on the output frequency is on average 3 %, mainly due
 389 to variations on the generated current across R_S .

390 The main performances of the proposed dVFC are
 391 compared in Table 1 with the few dVFCs encountered in
 392 the literature [5, 6]: exhibit a rather limited input range,
 393 larger errors, higher power consumption and they operate
 394 at higher supply voltages. The proposed dVFC is based on

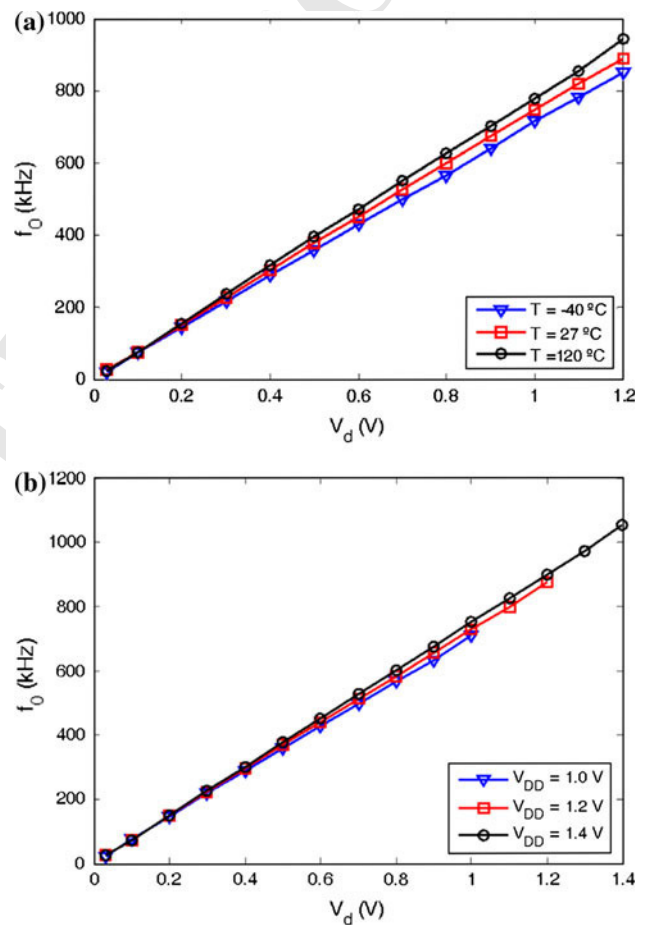


Fig. 9 Output frequency vs. differential input voltage for a $(-40, +120\text{ }^\circ\text{C})$ temperature range and b $(1.0, 1.4\text{ V})$ supply range

a preliminary design previously reported by the authors 395
 [10], however the newer and depurated version of dVFC 396
 exhibits a lower power consumption as well as a reduced 397
 area because: (i) it uses OTAs with single differential pairs 398
 instead of rail-to-rail OTAs, (ii) due to the common mode 399
 voltage at nodes V_1 and V_2 , the current across feedback 400

Author Proof

Table 1 Comparison of dVFCs

Parameter	[7], 2010	[6], 2011	This study
Technology	Commercial devices	0.18 μm CMOS	0.18 μm CMOS
Supply voltage (V)	± 5	1.8	1.2
Sensitivity (kHz/V)	75	861	750
Input range	0.2 V diff (0.0 ± 0.1 V)	1.2 V diff (1.2 ± 0.6 V)	Full range (0.6 ± 0.6 V)
Relative error (%)	$< 5^1$	–	10.4^2
Linearity error (%)	–	0.4^1	0.014^2
Power consumption (μW)	–	375	60

¹ Nominal² For 30 % V_{DD} variation and ($-40, +120$ °C) temperature range

resistors R_1 , R_2 , R_3 and R_4 is halved, (iii) the charging and discharging currents are obtained directly from the V–I converter without using current mirrors. In addition, this dVFC keeps the common mode voltage V_{CM} , therefore maintaining the same operating conditions for the OTAs. As a conclusion, the proposed dVFC offers high performance characteristics with a compact design.

4 Conclusions

A simple compact 1.2-V 0.18- μm CMOS differential voltage-to-frequency converter has been presented showing improved characteristics over the state-of-the-art converters for low-power sensor interface electronics. This rail-to-rail dVFC exhibits low temperature and supply sensitivity, featuring competitive performances with other low-voltage low-power counterparts. The sensitivity and start frequency can be easily tuned.

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