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DESIGN AND PROTYPING OF A SWITCH FOR HIGH CURRENTS

Bachelor's Thesis

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Graz, June 2016

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

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Abstract

This thesis deals with the design, prototyping and testing of a switch for high currents that will be deployed in a materials science application involving the DCPD technique. Taking a previous version of the project as a starting point, all the necessary steps will be comprehensively detailed with a strong emphasis on the required theoretical concepts.

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1. Introduction

1.1. Why I Chose This Project

Before coming to TU Graz for my Erasmus year, I was aware that I had to write my final thesis by the end of the exchange in order to complete my studies and finally become an engineer. But little did I know that I would end up taking a project like the one which is documented in these pages.

Being keen on topics such as analogue electronics, microcontrollers or programming it was a surprise that I decided to do my work on power electronics, a field I was completely unfamiliar with. That is the reason why I was slightly hesitant when, after asking Professor Söser for a thesis subject, he assigned me to this project. However, I had always been intrigued about the somewhat obscure world of power transistors, high currents and hot temperatures: after all, a component warmer than my finger was a bad omen in most of the work I had done before. And this thesis dealt with every single topic I intellectually feared and would not want to see on my paper: MOSFETs, huge amperages, temperature-dependent effects or total absence of code.

But I accepted. I knew that this may be my last chance of being on good terms with power electronics, so I said yes. In any case, it looked like quite a challenge.

1.2. What This Project Wants to Achieve

Once I joined the project, it was time to start with the work. And the first step, as is often the case, was to know exactly what I had to do. In short,

this thesis is about the design and prototyping of a system that is capable of handling large DC currents for a materials science experiment; its result is a piece of lab equipment (in the form of a PCB) that will be used in experiments involving a technique called DCPD (Direct Current Potential Drop).

This system that I had to design was to deliver a bidirectional high current to a load by the use of a H-Bridge. In fact, this work was an update of a similar device designed by Professor Söser some time ago; it was certainly helpful the fact that I could use the schematic of his project as a starting point.

Retrospectively, I think that this work is not a complex one for somebody who has the required knowledge and experience needed for dealing with power electronics, but for me (a novice at the field) it was a demanding exercise. In any case, as I see it, there are two different types of challenging thesis: the ones that deepen into one's expertise taking a solid background as a beginning, and those which create the foundations of a discipline completely new for the student; this work belongs to the latter kind.

1.3. Objectives

The goals of this project, both practical and theoretical, can be summarized as follows:

- Study of the DCPD technique and understanding of the role the final system will play in it.
- Deconstruction and reverse-engineering of the previous version of the circuit.
- Detailed comprehension of the Power MOSFET transistor.
- Thorough research of several power electronics topics required for the conception of the system.
- Design and simulation of the circuit.
- Fabrication of a PCB and prototyping of the system.
- Testing in order to evaluate performance.
- Writing of this report.

1.4. How This Project Was Developed

	March	April	May	June	July
Study of DCPD	X				
Reverse-Engineering	X	X			
Study of MOSFETs	X	X	X		
Study of Power Electronics		X	X		
Design & Simulation			X		
PCB Design			X	X	
Prototyping				X	
Testing				X	X
Writing				X	X

Table 1.1.: Chronology of the project.

Regarding the time frame of this thesis, it started in January 2016 but work was not begun until March. It was completed in July of that same year. There is a simple overview of how the tasks evolved through time in Table 1.1. Also it may be interesting to note how the workload was shared between different activities:

- Meetings with supervisor: 5h
- Reading literature: 125h
- Theoretical design: 100h
- Prototyping: 50h
- Testing: 15h
- Writing this document: 100h

Which makes a rough total of 395 hours.

1.5. Structure of This Document

Before finishing this chapter, the way this document is organised will be described pointing out which were the accomplishments achieved:

1. **Chapter 1:** this introduction. Overview of the project; temporal and academic boundaries.
2. **Chapter 2:** about the DCPD technique. Summary of selected literature on the topic.
3. **Chapter 3:** setting of the purpose and goals of the project, from a technical perspective. Clarification of the specifications of the required system.
4. **Chapter 4:** study of the previous board. This chapter deals with the reverse-engineering process that was performed on the received schematic, as well as with identifying the elements that should be updated.
5. **Chapter 5:** comprehensive review and explanation of the theoretical framework that was found to be necessary for this thesis. The whole learning process was autonomous.
6. **Chapter 6:** detailed design of the new system including thermal and electrical considerations, as well as simulations of the devised circuits.
7. **Chapter 7:** testing of the performance of the finished project.
8. **Chapter 8:** conclusion and further development.
9. **Appendix A:** compilation of different schematics used through the progress of this work.
10. **Appendix B:** very detailed analysis of the switching of the MOSFET.
11. **Appendix C:** some samples of screen captures taken with the oscilloscope during testing phase.

2. The DCPD Technique

2.1. Introduction to Fatigue Tests

The presence of a crack in a component or structure can significantly reduce its lifespan. That is why a huge effort has been put into the research of this field in the last 50-70 years. Cracks can appear due to fatigue, or as a consequence of manufacturing processes (deep machining marks, voids in welds, metallurgical discontinuities...).

One of the main ways of studying the formation and growth of cracks in a material is through fatigue tests (NDT, 2016; e-Fatigue, 2016). These are experiments in which a cyclic load is applied to a test piece (also known as *plate* or *specimen*) until it cracks and, ultimately, breaks. The standard output of this process is a curve (S-N curve, Figure 2.1, a) which compares the cyclic stress (S) against the number of cycles until failure (N).

However, another important relation that can be extracted from this kind of experiment is the one linking the crack length versus the number of cycles, for a fixed stress (Figure 2.1, b). Whereas for the first output graph (Fig. 2.1, a) it is enough to detect the break of the specimen, for the latter it is necessary to measure somehow the length of the flaw. Originally this was done through visual inspection and, as Burgers (Burgers and Kempen, 1994) points out, "[...] sometimes employing magnifying glasses or stereo microscopes with low magnifications. Specimens were provided with a scale for reading the length of the crack. An obvious disadvantage of visual observations is that it requires the attendance of an observer. Consequently such tests can be run during working hours only." These many requirements and disadvantages caused the automatic crack length measurements to be developed.

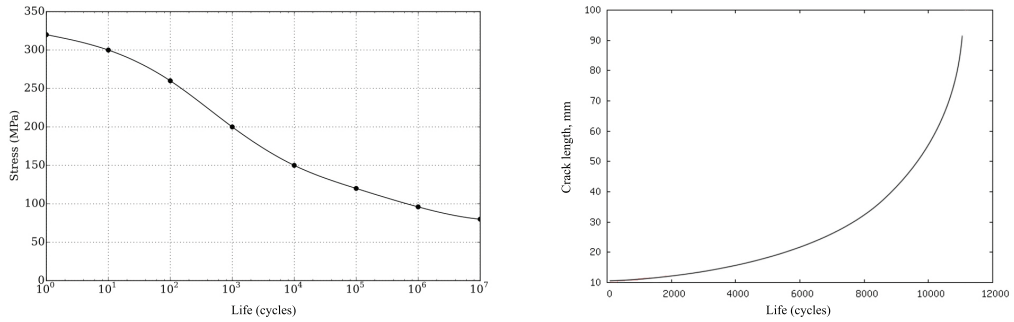

Figure 2.1.: a) S-N curve for brittle Aluminium with an UTS of 320MPa b) Example of crack length vs. number of cycles curve

2.2. The Direct Current Potencial Drop Method

DCPD stands for Direct Current Potential Drop, and is a technique for automatically measuring crack length. It was initially developed in the 1940s in Germany (Aronson, 1979), and refined during the following years until it came to be one of the current standard tests for fatigue analysis. The DCPD method has been accepted in fracture mechanics as one of the most accurate and efficient methods for monitoring crack growth. It also has been applied to monitor fatigue, stress corrosion and creep cracks. Moreover, it is useful for measuring velocities of fast running cleavage cracks and for evaluating the extent of crack closure in fatigue crack propagation studies (S. Nath and Lord, 1990).

In the DCPD method (Figure 2.2), a constant current (maintained by external means) is passed through an already-cracked specimen, and the electric potential drop, $V(a)$, is measured between two points symmetrically at both sides of the fatigue crack. The second potential drop, $V(a_0)$, is measured as a reference in an undisturbed part of the specimen. Since the distance between the attachment points is the same for $V(a)$ and $V(a_0)$, both potential drops should be equal if there is no crack ($a = 0$) and provided the electrical current is homogeneously distributed over the specimen width (something that can be achieved if the distance between leads is large enough). As the

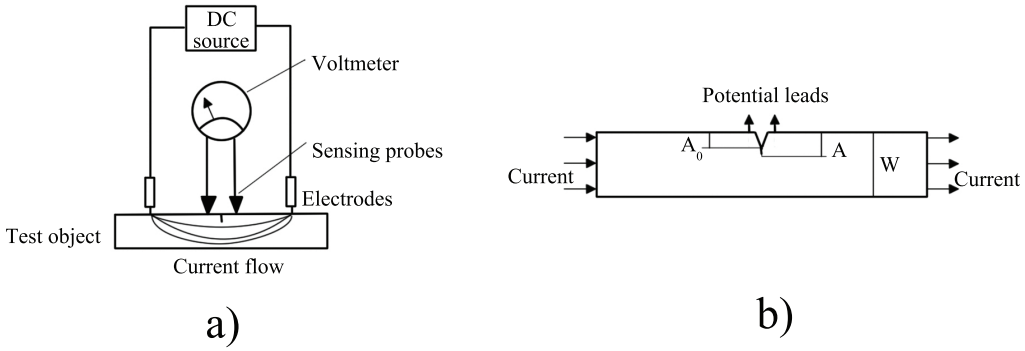

Figure 2.2.: Experiment set-up

crack increases, the uncracked cross-sectional area of the test piece decreases, the current path resistance increases and thus the potential drop between the leads becomes larger. In practice for a particular geometry, calibration curves are given in the form of $\frac{U}{U_0}$ versus $\frac{A}{W}$, where U_0 is the reference potential drop across the initial cracked specimen, U is the potential drop as the crack length increases, and $\frac{A}{W}$ is the crack length to width ratio. These calibration curves have been determined experimentally, analytically (Johnson's formula) and numerically; and they are accepted for use in fracture mechanics. Through the use of such non-dimensionalized ratios, calibration curves become independent of material properties, test piece thickness, and magnitude of input current (provided it remains constant) and are mainly a function of specimen and crack geometry and the locations of current input and potential measurement leads (S. Nath and Lord, 1990; Burgers and Kempen, 1994; Aronson, 1979). Hence, through appropriate calibration for the particular test piece geometry under test it is possible to estimate the length of the crack by just measuring the corresponding voltages:

$$a = f\left(\frac{V(a)}{V(a_0)}\right) \tag{2.1}$$

As it was found (Burgers and Kempen, 1994), there are two reasons for including a reference potential drop, $V(a_0)$:

1. Despite the current being kept constant, small variations can occur, either in one test or between different tests. Such variations will affect both V(a) and V(a_0) in the same way but there will be no effect on $\frac{V(a)}{V(a_0)}$, because they will cancel each other.
2. The electrical conductivity and the thermovoltages of the electrical connections are temperature-dependent. Variation of the temperature of the specimen under test will therefore affect $V(a)$ and $V(a_0)$. However, again the ratio $\frac{V(a)}{V(a_0)}$ will not be affected due to the symmetry of the electrical circuit, provided the whole specimen has the same temperature.

2.2.1. Highlights of the DCPD technique

Here there are, as a summary, some of the discussed characteristics and advantages of the Direct Current Potential Drop method:

1. The electrical potential drop method was adopted for automatic crack length measurements in fatigue crack propagation tests, which can be run without personnel attendance. The crack length is calculated from the ratio of the potential drop measured near the crack and a reference potential drop measured on the same specimen of some distance away from the crack.
2. The crack length calculations are carried out by the same computer that controls the load application of the fatigue machine. This is done instantaneously during a test, which offers interesting possibilities for automatic fatigue load adjustments dictated by the crack length.
3. The electrical potential drop method is also successfully applied to record and trace crack growth which cannot be observed visually.
4. The measured potential drop is in good agreement with the theoretical analysis of Johnson, and with finite-elements simulations. Required corrections are about 1 percent as a maximum.

3. Purpose and Goals of This Project

3.1. Required Equipment for DCPD Measurements

As it was explained in the previous chapter, the DC Potential Drop technique is based on the measurement of the voltage drop over a crack on a test piece. It was also said that the direct current is kept constant through external means. That means that for such an experiment, the measuring equipment is completely independent of the current management circuitry.

In some cases it is also useful to have the possibility of changing the direction of the current. This work deals with the design and development of such a device: one which will be used in a real application in the field of materials science at TU Graz. In the following sections we will briefly explain what was done in that institution prior to the start of this project, as well as its reasons to exist.

3.2. About the Former Switching Board

The seed of this thesis is a project developed by Professor Peter Söser at TU Graz in 2015. He designed and deployed a circuit capable of handling a certain direct current for a DCPD test set-up. The schematic of the project devised by him can be found on Figure A.1, Appendix A.

The final version of that project could provide a specimen (which we will usually refer to as *load*) a current of up to 10A (in both directions: +10A and -10A) taking as an input a fixed current and a control signal. In other words, the device could switch the direction of the current (externally fixed) through the load depending on the value of a certain control signal. After designing the circuit, it was built on a PCB. On Chapter 4 there is a detailed explanation of how this board worked.

3.3. Request of New Device. Specifications

Not long after the aforementioned project was finished, it was necessary to upgrade it. And that is the topic of this thesis: the design and prototyping of an updated current switching device taking as a starting point the former version. The most important requirement was that the system should be able to deliver up to 30 Amperes of DC current to the load, an amount significantly larger than before.

Some of the specifications to be fulfilled or relevant parameters are the following:

- Current through load: up to 30A, in both directions.
- The input current is set externally.
- Direction of the output current dependent on a digital input.
- Frequency of the switching between 0.1 and 1Hz (most of the analysis can be performed as DC).
- The load will be during most of the time lower than 1Ω, and can be considered as purely resistive.

4. Study of the Previous Board

The initial step for developing the new board was, obviously, understanding how the old one worked. That is what this chapter will be about: a comprehensive analysis of such circuit based on its corresponding schematic (Figure A.1). We will divide the system into building blocks which will be explained and the required changes for meeting the new specifications will be discussed.

4.1. Block Analysis

The original schematic consists of many devices, each of them playing a specific role. It is possible to group them into different blocks in order to make this "reverse engineering" problem easier.

First of all, it is important to identify the inputs and outputs of this design. On the schematic (Fig. A.1) they appear as standard connectors (`SCON`):

- **Supply Voltage:** this is the input voltage for powering the board. It should be around 18-20 Volts, and is referenced to ground.
- **Input current:** externally regulated, through this connector the circuit receives the current that will eventually be fed to the load. There is a corresponding ground-referenced terminal for sinking that current.
- **Load:** those two terminals are meant to provide the external load (specimen under test) the required current.
- **Logic input:** this is the digital input which controls the direction of the current through the load.

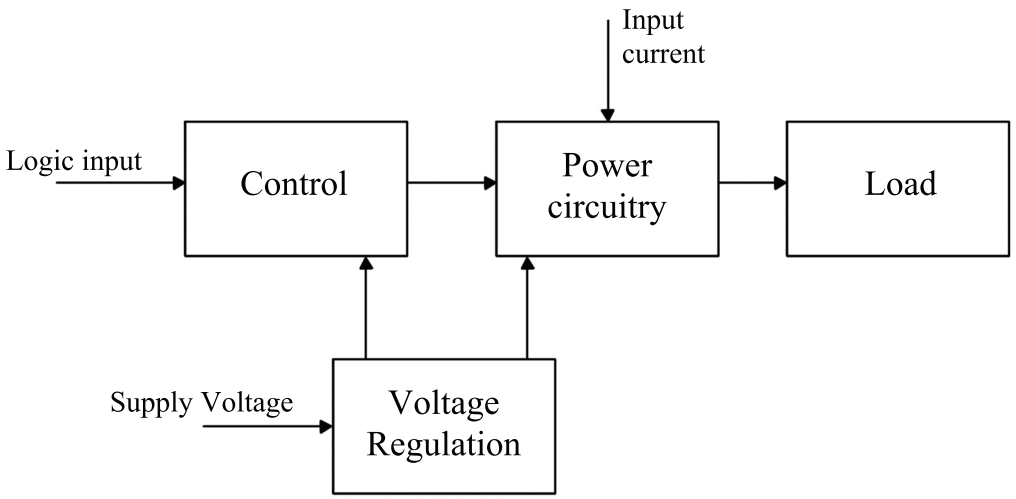

Figure 4.1.: Block diagram of the system

Those are the inputs and output of the whole system, and we can divide the circuit into smaller, easier to analyse blocks taking them as a guide. An approach to that can be seen on Figure 4.1: the complete schematic has been simplified to a few boxes (which represent specific parts of the board) and arrows (exchanges between sub-systems).

We came up with three distinct blocks: one which takes care of regulating different internal voltages, another that manages and improves the input logic signal, and the biggest of all: the power electronics circuitry, which deals with high currents. We will discuss them in the following sections.

4.1.1. Voltage supply circuitry

The corresponding schematic for this block is shown in Figure 4.4. We can clearly see it is a standard set-up consisting of a protection stage and two linear voltage regulators.

Regarding the protection devices, they are simply a varistor (R2, a kind of non-linear resistor that becomes a short-circuit under big voltages) and a

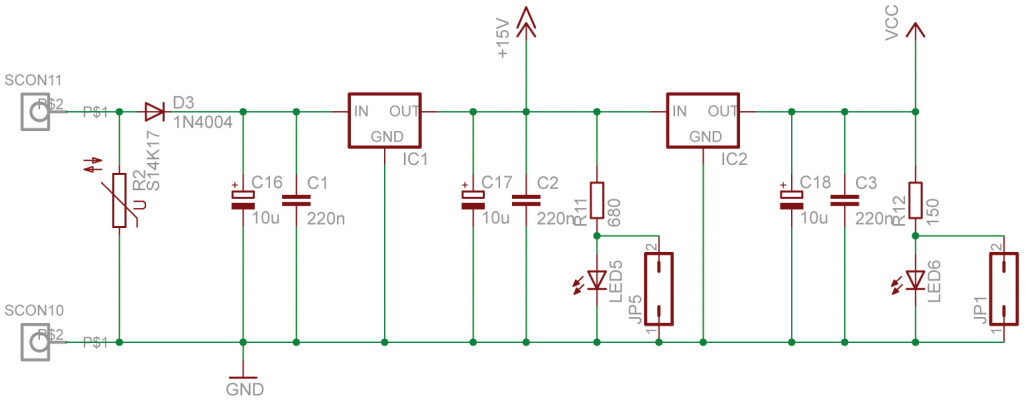

Figure 4.2.: Schematic of the voltage regulation sub-system

standard diode (D3) which blocks negative voltages in case the supply leads are reversed.

After that stage, we encounter the cascaded linear regulators: the first one, IC1, is a typical 7815 which offers a stable output voltage of 15V (labelled as +15V in the schematic). Next to it, being fed from the output of the previous one, there is a second regulator, IC2. In this case it is a 7805, rated for an output voltage of 5V (Vcc). Of course, there are also some filtering capacitors (both electrolytic and ceramic) which yield a good performance against noise and current peaks. There are also two LEDs which give visual feedback about the proper working of the circuit.

4.1.2. Control electronics

Another interesting block from the initial design is the one that generates the necessary signals for reversing the direction of the output current. We can see the relevant part of the schematic on Figure 4.3. In a nutshell, the purpose of this system is to produce two logic signals which encode the direction of the mentioned current from a potentially noisy input voltage. Both input and outputs are TTL-level signals.

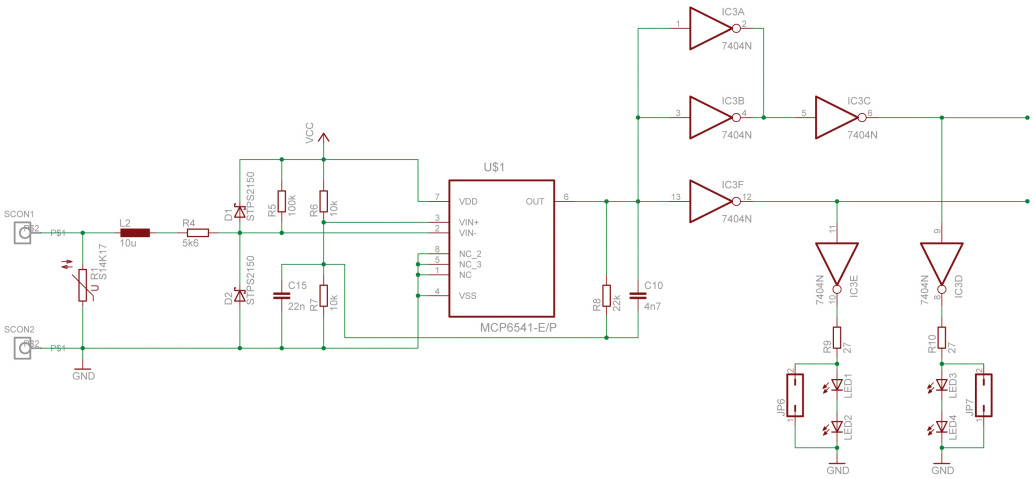

Figure 4.3.: Schematic of the logic sub-system

In the middle of the Figure we can find a comparator (MCP6541), which works as a hysteresis comparator. The pivoting levels for the hysteresis are 2 and 3V, and they are achieved through resistors R6, R7 and R8. Additionally there are two capacitors (C10, C15) which allow for noise immunity of the stage.

As for protection of the comparator, there exist several devices which enhance the reliability of the circuit. The first of all is the pull-up resistor R6: it prevents the inverting input to float if there is no external signal applied. Next to it we find two clamping Schottky diodes (D1,D2) that clamp the aforesaid input in the range (-0.2V, 5.2V), so no harmful voltage reaches the comparator (Cubed, 2012). Also it is important to mention current-limiting resistor R4 and inductor L2 (offers protection against current transients). Finally, as for the previous block, there is a varistor (R1) that short-circuits itself if the applied voltage is too big.

On the right-hand side of Figure 4.3 there are several inverters (7404) that buffer the output of the comparator, and generate a complementary pair of signals that will be used to change the direction of the output current.

4.1.3. Power management

The next block that will be analysed is the largest and most complex of the whole system, for it comprises many devices and deals with large currents. The concerning sub-schematic is that shown on Figure 4.4.

In short, it is a typical H-Bridge (transistors `Q1`, `Q2`, `Q3` and `Q4`) which receives the input current from connectors `SCON3-SCON9` and feeds it to the load, located after the terminals `SCON4-SCON5`. The transistors are driven by two IR2108PBF gate drivers (`U1`, `U2`). These devices work under the principle of bootstrap (see section 5.5.1), for which the capacitors `C13`, `C14` and diodes `D4`, `D5` are required.

These gate drivers are controlled by the two logic voltages generated by the control circuitry, and can be seen floating on the left side of Figure 4.4. Depending on their logic state (`HIGH-LOW` or `LOW-HIGH`) the current will go through one branch of the bridge (`Q1`, `Q2`) or through the other (`Q3`, `Q4`), resulting in the two different directions of the output current flowing through the load.

4.2. Required Modifications

Now that the original layout has been properly reverse-engineered, it is time to decide what will be kept, what will be changed and what has to be completely designed again. So, for each of the already mentioned blocks, the tasks to carry out are:

1. **Control electronics:** in principle, it can be reused. However, if the gate driver model is changed, it may be necessary to modify the interface.
2. **Voltage regulation:** depending on the requirements of the new design, we might have to update it so it can deliver more current.
3. **Power circuitry:** it will be necessary to check if the current set-up can handle the required 30A. If not, a new H-Bridge shall be designed. The gate drivers are dependent of the bridge, so they will have to be revised, too.

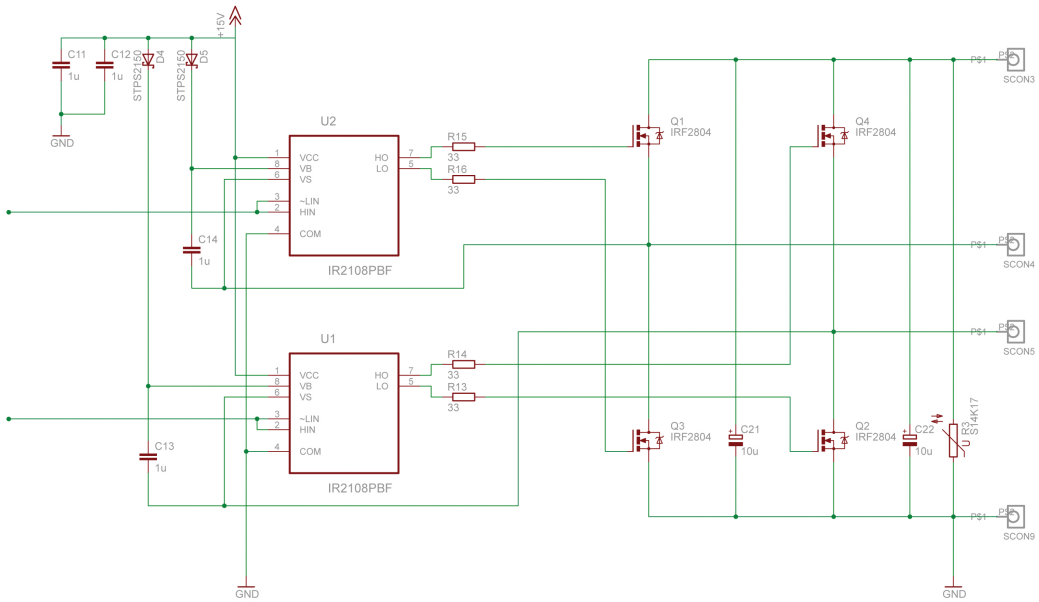

Figure 4.4.: Schematic of the power management circuitry

4. **PCB:** since the new design should be prototyped and eventually deployed, the fabrication of a new PCB will be required.

With this information in mind, the process of creating the new board could start. But, as usual (and even more having such potentially hazardous currents), theory goes before practice. And prior to designing anything, it was needed to acquire some knowledge concerning several topics. Chapter 5 will deal with that, comprising the main themes about which we had to research or get informed.

5. Things to Be Learnt

The goal of this thesis is, so far, clear: improving the previous version of the board so that it can handle more current. In order to achieve that, it was necessary to study and understand comprehensively several subjects related to power electronics and heat transfer, mainly. Some literature (Hart, 2011, Burdío, 2014) proved to be of great help. In this chapter the most important concepts about the topics will be listed.

5.1. Switching of MOSFETs

Lacking a background on MOSFET transistors, it was paramount to fully understand their operation, specially during switching (because the components in the H-Bridge work as switches: the active mode will be avoided). As a start some books dealing with basic concepts about FET technology (V. Fernández, 2015; Boylestad, 1972) were read, as well as specific application notes (*Understanding and Predicting Power MOSFET Switching Behavior* n.d.).

A great effort was made in order to completely understand which were the parameters that influenced transistor switching. As a result, a technique for estimating switching times was developed (it can be found on Appendix B).

Also *Power MOSFET Tutorial* 2006 was helpful to determine which factors could influence switching speeds.

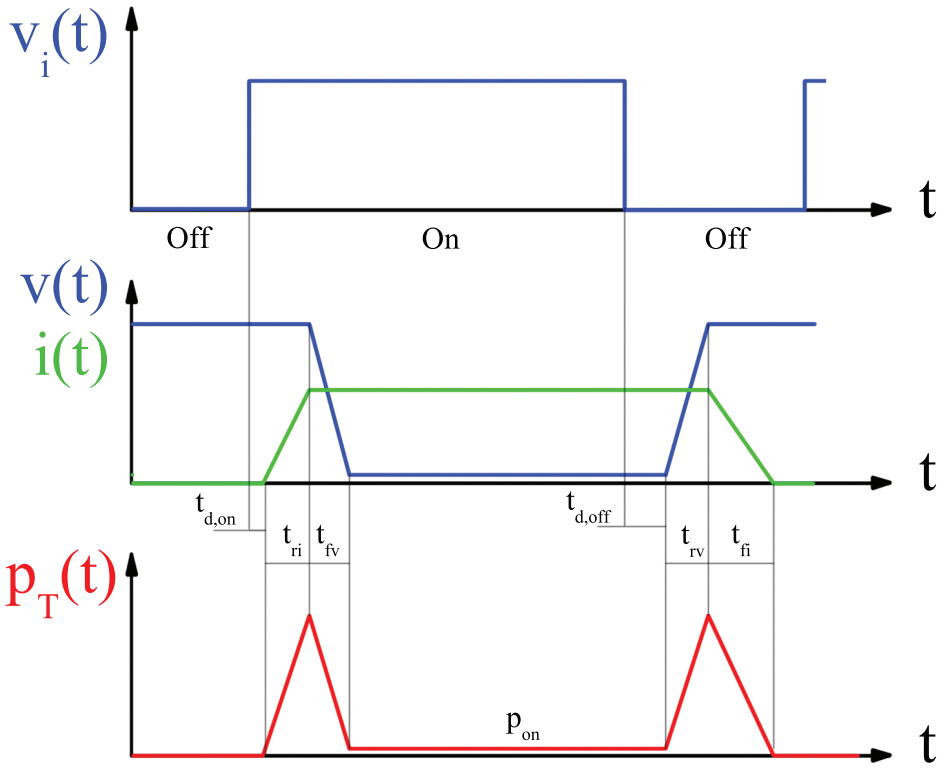

Figure 5.1.: Typical switch curves with inductive load

5.2. Operation With Inductive Load

Since the manufactured board may be at a certain distance of the specimen, there could be a stray inductance in the load (thus, becoming slightly inductive instead of purely resistive). Hence it might be necessary to analyse the evolution of voltage across the switch terminals and the current through it when handling an inductive load. A schematic version of the process can be seen on Figure 5.1. It is interesting to remark the different nature of the times shown on the graph. On the one hand, we have the $t_{d,on}$ and $t_{d,off}$ delays which are only attributable to the charge/discharge of the equivalent gate-to-source capacitance of the MOSFET. On the other, there

are the rise and fall times for voltage and current: these appear as a result of the inductive behaviour of the load (due to it opposing to changes in current).

5.3. Total Losses on Switches

Certainly it is essential to analyse the power losses on the bridge switches, since that will be the main limiting factor for the maximum current that the board will be able to handle. Attending to the three different modes a transistor is usually operated in (On, Off and active) we obtain the three different types of losses involved in switched-mode power electronics: on-, off- and switching-losses:

$$P_T = \frac{1}{T_s}\int_0^{T_s} v(t)i(t)dt = P_{on} + P_{off} + P_s \sim P_{on} + P_s$$

Being the impedance of the transistor typically huge in Off-state, it is common practice to neglect the off-losses (since they are minuscule compared to the others). Regarding the conduction losses, for the MOSFET they are expressed as a function of its $R_{DS,on}$ resistance:

$$P_{on} = \frac{1}{T_s}\int_0^{T_s} v_{on}(t)i_{on}(t)dt = R_{DS,on}I_{on,rms}^2\frac{t_{on}}{T_s} = R_{DS,on}I_{rms}^2$$

Finally, the switching losses depend on the switching time and on the nature of the load. The latter can be modelled with the constant a: typically $a = 2$ is used for inductive loads, and $a = 6$ for pure resistances:

$$P_s = P_{s,on} + P_{s,off} = \frac{1}{a}V_{s,on}I_{c,on}\frac{t_{s,on}}{T_s} + \frac{1}{a}V_{s,off}I_{c,off}\frac{t_{s,off}}{T_s}$$

5.4. MOSFET Body Diode. Losses

Due to their semiconductor structure, a parasitic diode is present in MOSFETs. It can be useful in some cases (as free-wheeling diode, for instance), but its presence makes necessary to analyse the potential associated losses. The power implications are most important during turn off, due to the negative current peak during the reverse recovery time, t_{rr}, associated with the device. These losses are calculated using the following formula:

$$P_{s,diode,off} = \frac{1}{T_s} \int_0^{t_{rr}} v(t)i(t)dt \sim V_{s,off} Q_{rr} f_s$$

The Q_{rr} value can be found on the datasheet of the device, commonly listed as "Reverse Recovery Charge".

5.5. MOSFET Gate Drivers

MOSFETs are voltage-controlled devices. And, as happens with other technologies, a driver circuit might be required in order to take it from On to Off state in an optimal way. Seen from the gate terminal, MOSFETs are basically a capacitor (more on that on Appendix B) which needs to be charged or discharged to be "closed" or "open", respectively. Since that process implies a current which in the initial instant can be high, proper methods of sourcing or sinking it are required.

Typically we distinguish between high-side and low-side drivers, depending on the location of the transistor in relation to the power rails. In any case, the standard gate driver is shown on Figure 5.2, Left: the voltage V_{GS} can be one of the two available levels (for instance, +15V and 0V), by applying to the gate terminal either V_{GG+} or V_{GG-}. In the case of a low-side device it is relatively straightforward to drive it: since the source terminal (for a N-MOSFET, as is often the case) is tied to ground, any positive voltage on the gate will achieve a positive V_{GS} and can potentially switch the transistor on. On the other hand, making $V_G = 0$ we make $V_{GS} = 0$, thus turning the device off.

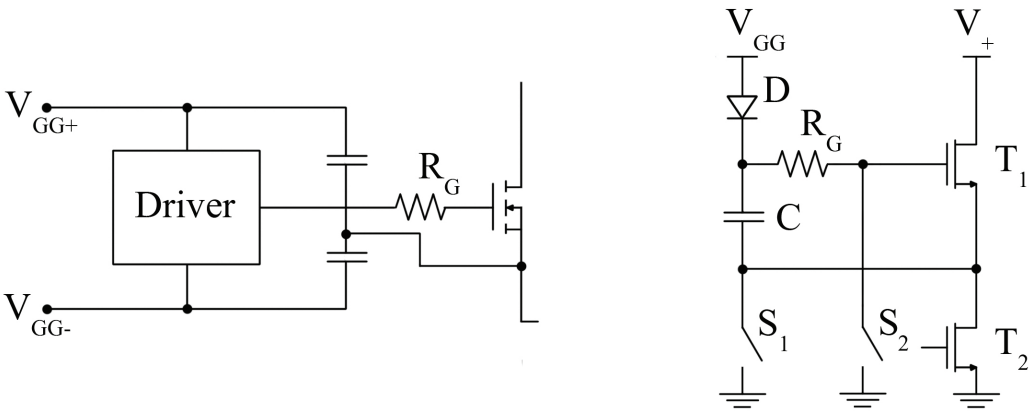

Figure 5.2.: Left: typical gate driver scheme. Right: bootstrap scheme.

However, high-side devices are tough cookies: they do not have their source terminal connected to ground, but the opposite: it is the drain pin the one which is tied to the positive supply rail. While the transistor is ON, it is desirable to have a very small voltage drop over it, which results in the source terminal being just a few millivolts below the positive rail. But because the switch is conducting, the V_{GS} voltage should be relatively large (15-20V are typical values). And that is a problem: the gate voltage will be then above the rail, which is usually the largest tension on the circuit.

5.5.1. Bootstrap Gate Drivers

One of the ways to overcome the obstacle met some lines above is with the help of a bootstrap driver. The standard scheme can be seen on Figure 5.2, Right. The principle under it works is the following: if switches S_1, S_2 are closed, the transistor T_1 is OFF (because $V_G < V_S$) and the diode D lets the current flow and charge the capacitor C to roughly V_{GG}. As soon as we want transistor T_1 to turn on, the switches S open so that $V_{GS,T1} = V_C = V_{GG}$. The capacitor does not charge or discharge thanks to the bootstrap diode: being the gate voltage greater than V_{GG}, the diode is reverse-biased and current cannot flow from V_{GG}.

In order to have a properly working circuit, it is necessary to dimension the driver components. As for the resistance R_G, there is a detailed guide on how to choose it on Appendix B. Regarding the bootstrap-specific components, it was learnt (*HV Floating MOS-Gate Driver ICs* n.d.) that the capacitor should be able to maintain the required V_{GS} voltage and be bigger than the equivalent C_{iss} gate capacitance. As for the diode, special attention has to be paid to its switching speed and current rating.

5.6. Concepts About Heat Transfer

As mentioned earlier, when a MOSFET is in ohmic mode it can be modelled with a simple resistor, $R_{DS,on}$, and its associated losses are proportional to it and to the square of the effective current (Equation 5.3). In the end, those losses P_{on} are nothing else than heat that dissipates into the environment. An undesirable effect of that process can be painfully experienced if a power MOSFET is touched with a finger: it may be extremely hot. Since silicon-based devices should not be at temperatures higher than 150-175°C and the current application involves large currents, it is convenient to conduct a thermal analysis of the device (the used methodology is explained in detail in F.P. Incropera, 2006).

5.6.1. MOSFET thermal circuit

The equivalent thermal circuit of a MOSFET without sink is shown on Figure 5.3, Left (Hart, 2011). As we can see, the junction temperature, T_j, increases with P_{on} and with the thermal resistances. Typical values for these impedances are provided by manufacturers in the datasheets. If required, the $R_{\theta,ca}$ resistance can be lowered by attaching a sink to the transistor.

5.6.2. Coupled thermal-electrical model

A remarkable characteristic of MOSFETs is that their drain-to-source resistance, R_{DS}, has a positive temperature coefficient. That is to say, it in-

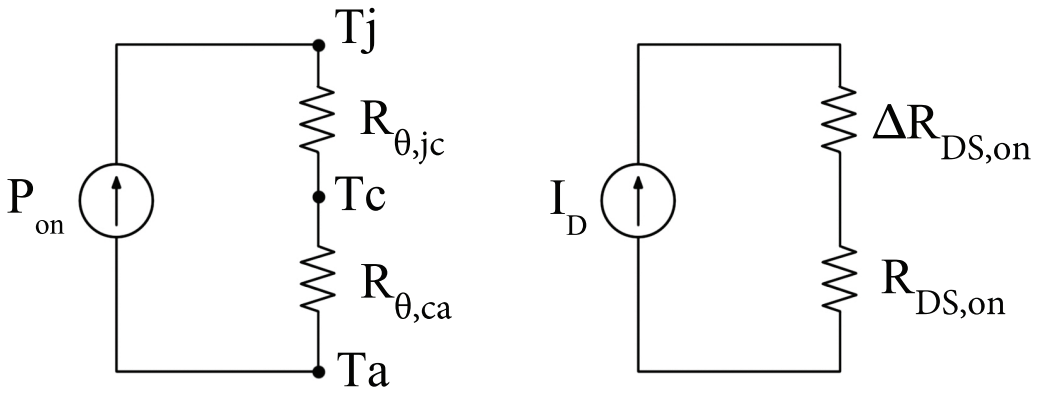

Figure 5.3.: Left: equivalent thermal circuit. Right: equivalent electric circuit.

creases with the temperature of the junction, T_j. In Figure 5.3, Right a dissected schematic is shown: it considers both the constant $R_{DS,on}$ (typically at $T_j = 25°C$) and its variation.

This poses a problem for electrical analysis since current I_D flows through the device, heating it up. As the temperature of the junction increases, so the equivalent $R_{DS,on}$ does, making the dissipated power even larger. This process keeps going on until the temperature stabilizes, and hence the On-resistance (*Power MOSFET Tutorial* 2006).

It is clear then than a purely electrical model cannot be used to represent a Power MOSFET: it has to be coupled to the thermal model. For a specific constant current I_D we have the following system of equations that describe the DC behaviour:

$$\begin{aligned} P_{on} &= I_D^2 R_{DS,on}(T_j) \\ T_j &= T_a + P_{on}(R_{\theta,ca} + R_{\theta,jc}) \end{aligned}$$

Solving them for the appropriate variable it is possible to calculate the maximum current that the device can handle at a certain junction temperature, or determine if a sink is required or not, for instance.

5.6.3. Improving the efficiency

If the current is fixed, it is advisable to lower the temperature of the junction; it will improve the overall efficiency of the system and extend the life of the device. There are several ways of achieving that:

- **Fins:** It is common practice to attach cooling fins to transistors in order to increase the heat exchange surface. Their downside is the size: they usually are quite bulky.
- **Deep saturation:** driving transistors further into the On-region makes them more conductive, thus lowering the losses. It is achieved by increasing the V_{GS} voltage for MOSFETs, or the I_B current for bipolar transistors. A disadvantage of doing this is that switching takes longer; it can be critical in high-speed applications.
- **Parallelization:** connecting transistors in parallel effectively reduces the equivalent On-resistance of the group, lowering significantly the junction temperatures. More on that on Section 5.7 .

5.7. Paralellization of MOSFETs.

As discussed earlier, a solution to the junction temperature problem is parallelizing transistors. For BJTs it is not an advisable solution: due to their negative temperature coefficient, the one with the lowest initial resistance will get more and more current, leading to its overheating and eventual failure.

However, a great advantage of MOSFETs comes from their positive temperature coefficient: as mentioned, the hotter they get the higher their $R_{DS,on}$ resistance becomes. When paralleled, if one of the group has an initial lower resistance than the others it will draw more current which will lead to an increase of its $R_{DS,on}$, thus stabilizing the set.

Of course, this negative feedback does not guarantee equal current sharing, but rather temperature stability: due to construction mismatches the ON-resistances will likely be slightly different. The worst case scenario should also be considered: that in which one of the transistors of the group has

the lowest possible resistance and the others the highest (*Paralleling Power MOSFETs* n.d.), after having reached thermal equilibrium.

5.8. Eagle

The final circuit will have to be designed and, eventually, mounted on a PCB. Lacking experience on the matter, it was required to learn how to draw schematics and compose an according layout. The program typically used by the *Institut für Elektronik* for this task is Eagle, so a tutorial was followed in order to get familiarised with it (*Eagle Tutorial* 2015).

6. Design and Prototyping

This chapter documents the process followed for designing the new version of the project, focusing on specific components and devices. The theoretical background for some of the assumptions made were explained on Chapter 5.

6.1. Overview of IRF2804 Characteristics

One of the requirements for this project was to use the IRF2804 HEXFET Power MOSFET. It is manufactured by International Rectifier, and offers some interesting features:

- Low On-resistance, of around 2.0mΩ at $T_j = 25°C$.
- Large maximum drain current: $I_{D,max} = 75A$.
- T_j can rise up to 175°C without compromising device safety.
- Fast switching: gate charge $Q_G \sim 200nC$.

The following sections will focus on making this specific device able to deliver safely 30 Amps of direct current.

6.2. Thermal Design

Here the dimensioning of the power MOSFETs will be developed, regarding some temperature-related requirements. The theoretical framework was previously set in Section 5.6.

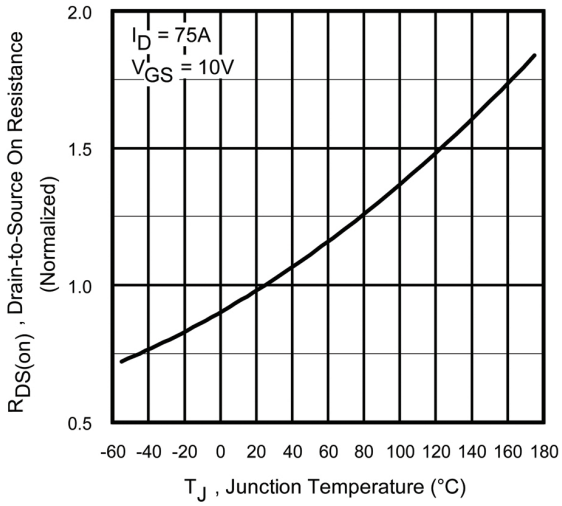

Figure 6.1.: IRF2804. Normalized On-resistance vs. Temperature

6.2.1. Overview of IRF2804 thermal characteristics

According to the IRF2804 datasheet, this device has the following thermal resistances:

- $R_{\theta,jc} = 0.45°C/W$, Junction-to-Case.
- $R_{\theta,cs} = 0.5°C/W$, Case-to-Sink, greased surface.
- $R_{\theta,ja} = 62°C/W$, Junction-to-Ambient, maximum.
- $R_{\theta,ja} = 40°C/W$, Junction-to-Ambient, PCB mount.

Another graph from the datasheet which is worth analysing is the one displayed on Figure 6.1. It shows how the $R_{DS,on}$ resistance increases with temperature. In order to obtain an analytical expression, the curve will be linearised taking two points: $R_{DS,on,norm}(T_j = 25°C) = 1$ and $R_{DS,on,norm}(T_j = 160°C) = 1.75$:

$$\begin{aligned} R_{DS,on}(T_j) &= R_{DS,on}(25°C) + \Delta R_{DS,on} \sim R_{DS,on}(25°C)\left(1 + (T_j - 25)\frac{0.75}{135}\right) \sim \\ &\sim 2m\Omega(0.8611 + 0.00556T_j) \sim (1.722 + 0.0111T_j)\text{m}\Omega \end{aligned}$$

With T_j in degrees Celsius.

6.2.2. Operating conditions of the switch

The working conditions for the switch are the following:

- Maximum current to handle: $I_t = 30\text{A}$ (DC).
- $T_{j,max} = 150°\text{C}$, below the limit in order to increase safety.
- No fins, so cost and size are kept at minimum.

6.2.3. Design with one transistor

First of all we will study whether or not the IRF2804 transistor can fulfil all the requirements mentioned above. The starting point will the set of equations 5.6.2 together with the obtained temperature linearisation (Formula 6.1). Coupling the equations,

$$\begin{aligned} \frac{T_j - T_a}{R_{\theta,ja}} &= I_t^2 R_{DS,on}(T_j) \Rightarrow \frac{T_j - T_a}{R_{\theta,ja}} \sim I_t^2 (1.722 + 0.0111 T_j) \cdot 10^{-3} \Rightarrow \\ \Rightarrow \cdots &\Rightarrow T_j \sim \frac{T_a + 1.7222 \cdot 10^{-3} R_{\theta,ja} I_t^2}{1 - 11.1 \cdot 10^{-6} R_{\theta,ja} I_t^2} \end{aligned}$$

In the worst case the junction-to-ambient thermal resistance is 62°C/W. And the subsequent junction temperature, T_j, would rise to 357°C: a value which results in the complete destruction of the device.

With the same set of equations it is also possible to calculate the necessary drain-to-source resistance which meets the specifications (with an ambient temperature of 40°C):

$$\begin{aligned} \tfrac{T_j - T_a}{R_{\theta,ja}} &= I_t^2 R_{DS,on} = P_{on} \\ T_j &\leq 150°\text{C} \Rightarrow P_{on} \leq \frac{150°\text{C} - T_a}{R_{\theta,ja}} \sim \frac{150°\text{C} - 40°\text{C}}{62°\text{C/W}} = 1.77\text{W} \end{aligned}$$

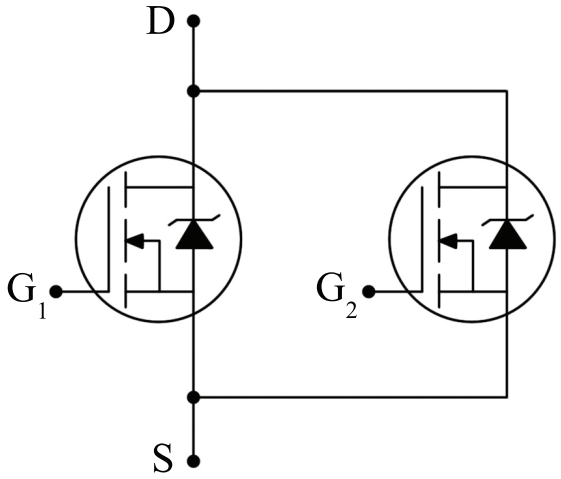

Figure 6.2.: Two MOSFETs in parallel.

That power dissipation requirement is directly connected to the On Resistance:

$$P_{on} = I_t^2 R_{DS,on} \leq 1.77\text{W} \Rightarrow R_{DS,on} \leq 1.97\text{m}\Omega$$

Since the $R_{DS,on}$ resistance is already 2mΩ at a junction temperature of 25°C, it is clear that in any case a single transistor will not be able to deliver the required current.

6.2.4. Design with two transistors

As explained in Section 5.7, a simple method for reducing the equivalent On-resistance of a switch is paralleling two or more transistors. Now we will check if a set of two paralleled MOSFETs (like the one on Figure 6.2) is enough for handling 30A on DC.

The whole calculation is based on the fact that two equal resistors in parallel show an overall resistance of half the one of a single resistor (R//R = $\frac{R}{2}$). Taking the linearised formula of drain-to-source resistance over junction

temperature and naming the one of the paralleled set as $R^*_{DS,on}$, it is evident that:

$$R^*_{DS,on} = \frac{1}{2}(1.722 + 0.0111T_j)\text{m}\Omega = 0.861 + 0.00556T_j\text{m}\Omega$$

Following the same methodology as before, now we solve the coupled thermal-electrical system with the obtained $R_{DS,on}(T_j)$:

$$T_j - T_a = R_{\theta,ja}I_t^2(861 + 5.56T_j)\cdot 10^{-6} \Rightarrow T_j \sim \frac{T_a + 861\cdot 10^{-6}R_{\theta,ja}I_t^2}{1 - 5.556\cdot 10^{-6}R_{\theta,ja}I_t^2}$$

Setting $R_{\theta,ja} = 62°\text{C/W}$ and T_a to 40°C, we just have to substitute values in order to find out the final junction temperature of the transistors:

$$T_j(I_t = 30\text{A}) = 127.59°\text{C}$$

Which is a value that meets all the requirements. As a result, a topology of two transistors in parallel will be used for each of the switches in the H-Bridge. Regarding the drain-to-source resistance at the working temperature, the formulas yield:

$$\begin{aligned} R^*_{DS,on} &= 1.57\text{m}\Omega \\ R_{DS,on} &= 3.14\text{m}\Omega \end{aligned}$$

6.2.5. Worst-case scenario for two transistors

It was discussed on Section 5.7 that construction mismatches on R_{DS} can lead to junction temperature inequalities. For the IRF2804 that value can oscillate between 1.3 and 2.3mΩ. Then, if we assume that one of the transistors of the set has a value $R_{DS,1} = R_{DS,on,min}(T_j) = R_{DS,on,min}\cdot(\text{a} + \text{b}T_j)$ and the other $R_{DS,2} = R_{DS,on,max}(T_j) = R_{DS,on,max}\cdot(\text{a} + \text{b}T_j)$ (with a = 0.8611 and b

= 0.00556, as found on section 6.2.1), it is straightforward to calculate the parallel resistance as a function of temperature:

$$R^*_{DS}(T_j) = R_{DS,1}(T_j) // R_{DS,2}(T_j) = \frac{R_{DS,1} \cdot R_{DS,2}}{R_{DS,1} + R_{DS,2}}(a + bT_j) = R^*_{DS}(a + bT_j)$$

Now, repeating the same process as before but with the worst-case resistance (at $I_t = 30A$, $T_a = 40°C$ and junction-to-ambient thermal resistance of 62°C/W we arrive at the junction temperature of the pair:

$$T_j \sim \frac{T_a + aR_{\theta,ja} I_t^2 R^*_{DS}}{1 - bR_{\theta,ja} I_t^2 R^*_{DS}} \sim 108.19°C$$

Which is well below the limit. For that junction temperature, the relevant parameters of the mismatched transistors are:

$$\begin{aligned} R_{DS,1}(108.19°C) &= 1.90m\Omega \rightarrow I_{D,1} = 19.17A \rightarrow P_1 = 0.698W \\ R_{DS,2}(108.19°C) &= 3.36m\Omega \rightarrow I_{D,2} = 10.83A \rightarrow P_2 = 0.395W \end{aligned}$$

Which are perfectly safe values for the MOSFET with the lowest resistance of the set.

6.3. Device Losses. Switching Time

Now we will proceed to calculate the power losses in the MOSFETs. It is important to remember that the switching frequency is extremely low (a square wave between 0.1 and 1Hz), and that will dampen significantly many of frequency-dependent losses. The formulas used are explained on section 5.3. Of course, this analysis will be done considering the switch as a matched pair of paralleled IRF2804 transistors.

6.3.1. Conduction losses

Assuming that the switching frequency is the highest possible ($f_s = 1\text{Hz}$) and that thermal equilibrium has been reached, the conduction losses for each transistor are:

$$P_{on} = R_{DS,on} I_{on,rms}^2 \frac{t_{on}}{T_s} = 1.57\text{m}\Omega(15\text{A})^2 \frac{0.5\text{s}}{1\text{s}} \sim 0.1766W$$

Due to the frequency being so low (specially when it is 0.1Hz), it may be better to assume DC operation (after all, for an electronic device a period of 5 seconds can be considered as such). In that case, the conduction losses P_{on} would be around 0.35W.

6.3.2. Diode losses

For the sake of completion we will calculate the turn-off losses caused by the body diode of the MOSFET. Assuming an Off-voltage $V_{s,off}$ of 10V (although in practice it will be of a few hundreds of millivolts), it is clear that these losses are totally negligible:

$$P_{Diode,off} \sim V_{s,off} Q_{rr} f_s = 10\text{V} \cdot 100\text{nC} \cdot 1\text{Hz} = 10^{-6}\text{W} \sim 0$$

6.3.3. Switching losses. Choice of t_s

The switching losses are caused by the transition of the operation point of the transistor through the active region, and are highly dependent on the duration of that process:

$$P_s = P_{s,on} + P_{s,off} = \frac{1}{6} V_{s,off} I_D f_s (t_{s,on} + t_{s,off})$$

Setting $V_{s,off}$ to the unreal value of $10V$, and a maximum dissipated power of 10mW (in order to disregard its contribution), it is easy to find which is the

maximum switching time (in Figure 5.1 they are appear as $t_{s,on} = t_{ri} + t_{fv}$ and $t_{s,off} = t_{rv} + t_{fi}$, although in our case we are considering a resistive load):

$$P_s = \frac{1}{6} \cdot 10\text{V} \cdot 15\text{A} \cdot 1\text{Hz}(t_{s,on} + t_{s,off}) \leq 0.01\text{W} \Rightarrow t_{s,on} + t_{s,off} \leq 400\mu\text{s}$$

Which is a ridiculously high period of time for a transistor like the IRF2804. It is clear then that, almost regardless of the chosen switching time t_s, the mean value of these losses shall be ignored with no afterthoughts. However that does not mean we should not consider them during turn-off or turn-on. It is always necessary to keep the device within the SOA (*Safe Operating Area*), and that is something that will be covered in section 6.9

6.4. Dimensioning of I_g and R_g

Taking into account the restriction enunciated in the previous paragraph, we will choose arbitrarily a turn-off time $t_{s,off}$ of 1.5μs, so the current through the gate terminal is not be excessively high during switching. Using this parameter as design rule instead of $t_{s,on}$ (which is smaller than its counterpart) proper operation is guaranteed.

Setting the final $V_{GS,f}$ to 15V, the Matlab script provided at the end of Appendix B was used in order to dimension the gate resistance. The chosen R_g was 33Ω. And the corresponding gate current in the initial moment of switching is, then, $V_{GS,f}/R_g = 0.45$A (per transistor).

6.5. Analysis of Gate Driver IRS2003

Another requirement for the project was to use the IRS2003 IC as MOSFET gate driver[1]. Each of these devices is actually a half-bridge driver: just

[1] A three-state fast driver was originally designed for this purpose, but the low-frequency requirements of this application rendered it unnecessary.

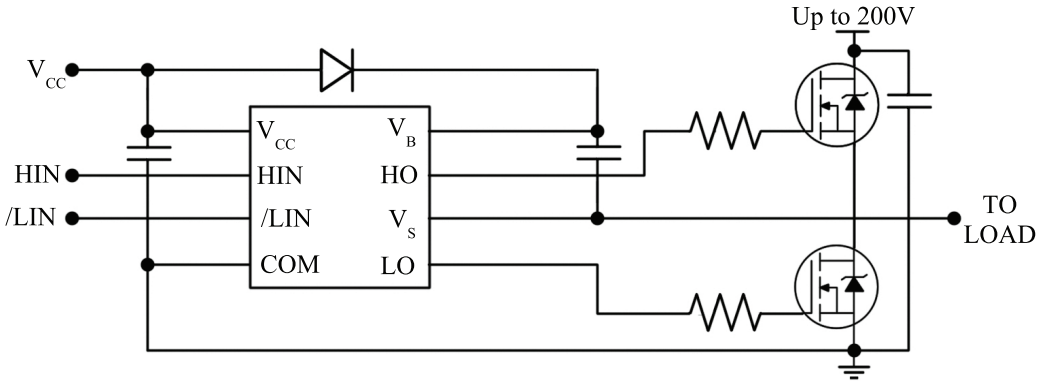

Figure 6.3.: Typical connection of IRS2003 Half-Bridge driver.

perfect for our needs. Its main features are, according to the datasheet provided by International Rectifier, the following:

- Floating channel designed for bootstrap operation.
- Gate drive supply range from 10 to 20V.
- 5V logic compatible.
- Matched propagation delay for both channels.
- Internally set dead-time of around 520ns.
- $I_{0\pm}$: 130/270mA.

As we can see, it comprises a bootstrap gate driver for the high-side device, as well as a standard low-side driver. As a result, with two of these ICs (one for each branch) it is possible to correctly operate a typical H-Bridge. It is also interesting to note the internal dead-time: it prevents the two transistors from conducting at the same time. That is specially desirable when powering inductive loads, but in our case it just makes the system more robust.

The only feature of this device that does not completely fulfil the specifications is the I_0 current: as we calculated before, the initial gate peak should be around 0.45A; and this IC does not support that. Another gate driver (IRS2184) with better output characteristics was proposed, but due to logistic reasons the IRS2003 was finally chosen.

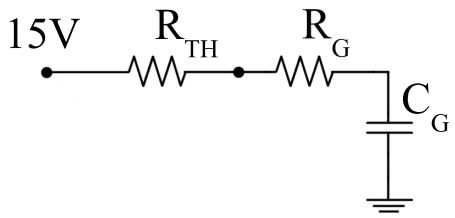

Figure 6.4.: Model of driver output connected to MOSFET gate

Making a *very* rough analysis, we could model those 130mA of maximum current with a Thévenin equivalent, as shown on Figure 6.4. Subsequently, the R_{TH} would have a value of $15\text{V}/130\text{mA} = 115\Omega$. Added to the already-present 33Ω of R_G, it makes an effective gate resistor of 148Ω. Inserting that value in the written Matlab script (Appendix B), we obtain a total switching time of 6μs, way lower than the restriction imposed on section 6.3.3. It could be argued that the external R_G resistance is no longer needed, but in any case it is advisable to connect a physical resistor in order to attenuate eventual oscillations caused by the rapid increase of the gate current in the first moments of switching.

6.6. Impact of I_g Peaks on Supply Voltages

The board receives two input supplies: a current supply which is managed by the H-Bridge, and a voltage supply ($\sim$18V) used for powering the devices that control the system (drivers, logic, regulators...). As it was briefly commented on section 4.1.1, that voltage is stepped down to 15 and 5 Volts with the help of two linear regulators. In addition there are some capacitors populating the board that keep the voltages constant over time.

Being the H-Bridge composed of eight synced power MOSFETs (that is to say, four switches with two transistors each), the current requirements may be high during switching. That is the reason why the filtering capacitors were chosen to have a value of 10μF: they ensure a clean, constant supply even at the initial moments of turn-on or turn-off. A voltage-regulating

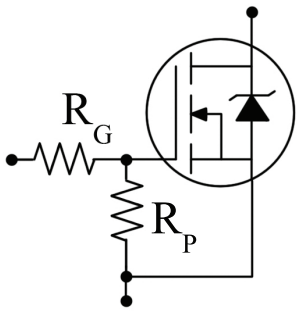

Figure 6.5.: MOSFET protected against driver IC failure

stage with higher output current was considered, but its benefits would be irrelevant.

6.7. Pull-Down Resistors

In the hypothetical situation that the gate driver stops working, the gate terminal could be left floating. Since the state of the MOSFET depends mainly on the V_{GS} voltage, an induced noise could be enough to turn the transistor on temporarily and potentially cause further damage. In order to prevent so, a simple yet effective protection has been deployed on the design (Figure 6.5). It just consists of an unappealing resistor, R_P.

Resistor R_P makes sure that, if the driver IC is not effectively connected, there is always a direct path from the gate terminal to the source of the MOSFET. That ensures that the gate-to-source voltage will not accidentally rise, keeping it zero. However, if there *is* a working gate driver connected, resistors R_G and R_G work as a voltage divider, thus lowering the gate-to-source level. That is the reason why the R_P resistance is high (a value of 50kΩ was chosen):

$$V_{DS} = \frac{1}{1 + \frac{R_G}{R_P}} V_{O,Driver} = \frac{1}{1 + \frac{33\Omega}{50k\Omega}} V_{O,Driver} \sim V_{O,Driver}$$

6.8. Stray Inductances

Stray inductances can be a nasty thing to manage in a power electronics design, specially when handling high currents. Special care has to be taken regarding induced voltages: a fast change in current causes a rise in voltage proportional to the magnitude of the parasitic inductances, and that could lead to failure of the switches. However, in our case that is a minor problem due to the very low voltages involved: even if the stray inductances were undesirably high (something tackled through a proper layout design), the voltages present in the board are so small that the devices would suffer no harm. Anyway, the bridge also comprises two capacitors (one for each branch) which mitigate their effect.

6.9. First H-Bridge Design

Now it is time to sketch and simulate the first design of the power management block: the H-Bridge. The schematic that was devised is the one shown on Figure 6.6, and the OrCAD implementation can be found on Appendix A.2 (although it features a capacitor in parallel with a switch, it was not simulated: its role will become clear in the next section). The circuit assumes ideal gate drivers, but uses the right MOSFET models provided by International Rectifier.

As final gate-to-source voltage we used 15V, and a load of 100mΩ. The simulation shows the curves of a single transistor (out of the two that form each switch) being shut off (instead of being turned on, which takes less time). The PSpice output is shown on Figure 6.7. Let us have a look at each of the variables:

- **Gate driver output (Top, Blue):** it falls from 15 to 0V, triggering the switching-off.
- **Gate-to-source voltage (Top, Red):** coherently with the capacitive behaviour of the gate terminal, it decreases slowly along the time axis. Also here it is possible to observe the reliability of the algorithm developed on Appendix B: the switching time is slightly higher than 1μs,

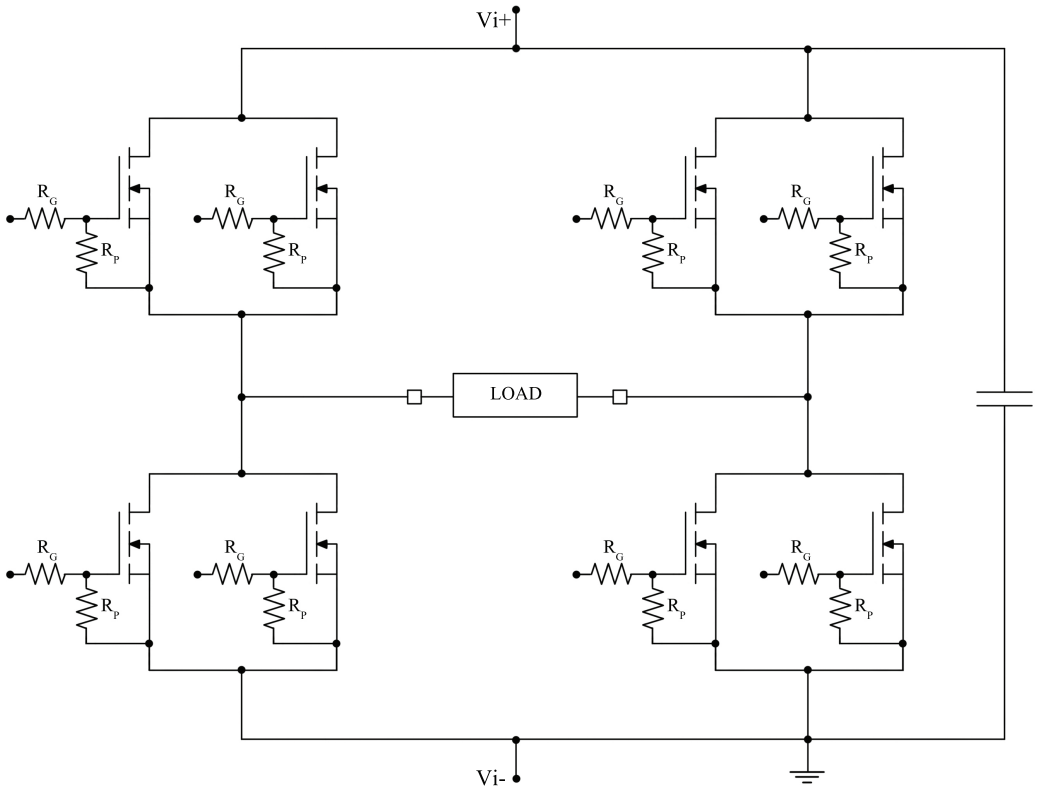

Figure 6.6.: First power stage design

as expected (although it can be considered finished after 600ns, when the current stops flowing rather than when the V_{GS} voltage becomes zero).

- **Gate current (Top, Green):** with a factor of 10:1 (so it can be visualized in the same graph), this is the current entering the gate terminal. It is negative, which means that the equivalent capacitor is discharging.
- **Dissipated power (Center):** measured in Watts, this shows the losses of the transistor. As we can see, they reach briefly a significant value of 7.6W.
- **Drain current (Bottom, Red):** in this curve it is very easy to spot the different phases through which the transistor goes during switching: first, a small delay time of 120ns, followed by a steep descent to 10A. After that, the MOSFET crosses the Miller plateau (500ns), and shortly

Figure 6.7.: Simulation without snubber. Top: gate current (Green, 10:1), input voltage (Blue), gate-to-source voltage (Red). Centre: power dissipated by a single MOSFET. Right: drain-to-source voltage (Green), drain current (Red)

after the switching can be regarded as finished.

- **Drain-to-source voltage (Botton, Green):** here we observe the transition from the $V_{DS,on}$ voltage (a few mV) to $V_{DS,off}$.

With the simulation seamlessly backing the theoretical calculations (which was a nice surprise), there was only left a small thing to consider: the switching losses in the transistor. Although they are not dangerous and only last for around 100ns, it may be wise to consider the inclusion of a snubber in order to make the design more efficient.

6.10. Final Schematic

After analysing the simulation results of the first H-Bridge design, we discovered that some details could be subject to changes. In the following

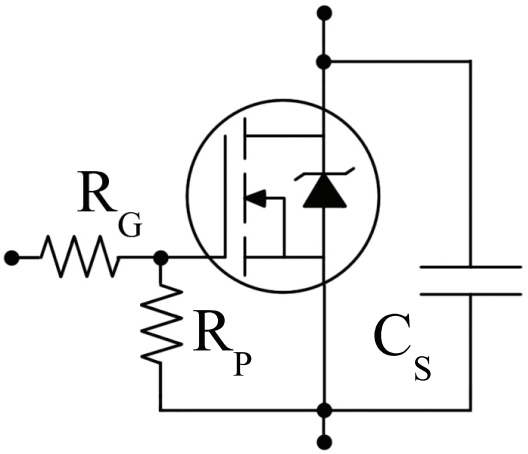

Figure 6.8.: MOSFET with snubber capacitor

paragraphs those variations will be listed and explained.

6.10.1. Inclusion of snubbers

As we have argued, the dissipated power peak during switching is quite large. In order to reduce this effect, it may be convenient to add a snubber to each of the switches. Some topologies were considered, but due to the very loose speed requirements of the stage a simple snubber capacitor was chosen (as displayed on Figure 6.8). Its value was arbitrarily decided through simulation, using the same OrCAD file as before (A.2) but including the new device.

A value of $C_s = 1\mu$F was chosen, and it was a complete success: with that snubber capacitor, the switching losses peak only reaches 2.2W. A 70% reduction of the dissipated energy is achieved, which could allow the stage to switch at higher frequencies without risking the devices. The corresponding simulation is the one on Figure 6.9.

Figure 6.9.: Simulation with snubber. Top: gate current (Green, 10:1), input voltage (Blue), gate-to-source voltage (Red). Centre: power dissipated by a single MOSFET. Right: drain-to-source voltage (Green), current through snubber (Blue), drain current (Red)

6.10.2. Switching speed. Number of drivers

We have discussed the topic of the maximum sink/source current that the gate drivers can handle, and its impact on switching speed. All those considerations were made assuming that each pair of transistors (high- and low-side) was being driven by one side of the driver. However, since we chose to parallel the MOSFETs, there are eight transistor to be taken care of.

The whole bridge can be seen as two branches (left and right) of two switches, composed each by two transistors. The question is, should each branch or diagonal be powered by a single gate driver or by two? Owing to the fact that switching speed was already compromised by the low output current capabilities of the chosen device (IRS2003), it may be wise to use four gate drivers: one for each pair of MOSFETs.

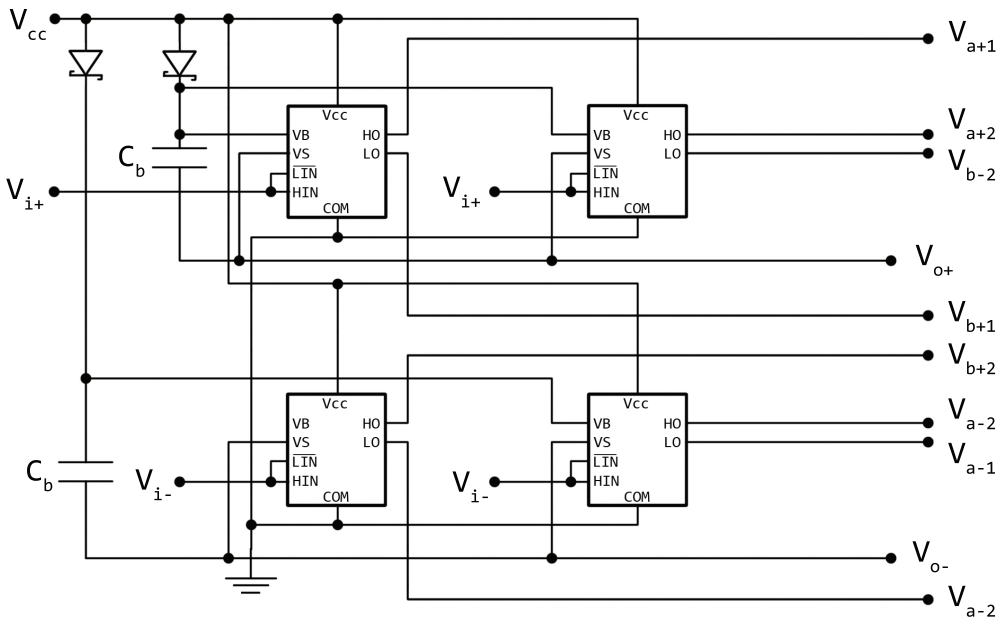

Figure 6.10.: Four-driver stage for 8 Power MOSFETs.

The devised design is shown on Figure 6.10. It has two inputs (V_{i+}, V_{i-}), two reference points (corresponding to the output of the H-Bridge) and eight terminals that should be connected to the gates of the transistors. The naming works as follows: **a/b** refers to the bridge diagonal, **+/-** to the side (either high or low), and **1/2** to the position of the transistor in the pair. Regarding the bootstrap capacitor, a 2.2μF electrolytic one was chosen so it could handle the current draw of two transistors without its voltage being significantly affected.

However, if the benefits of having four ICs instead of two are irrelevant, it could be not worth having them. The dead-time mismatches between transistors belonging to the same pair might bring unwanted power losses. That is why a method for choosing between the different set-ups (two or four driver ICs) was conceived. As pictured on Figure 6.11, it is nothing else than a jumper-based selecting interface. Consequently, the design will have four of these selectors, one for each pair of transistors.

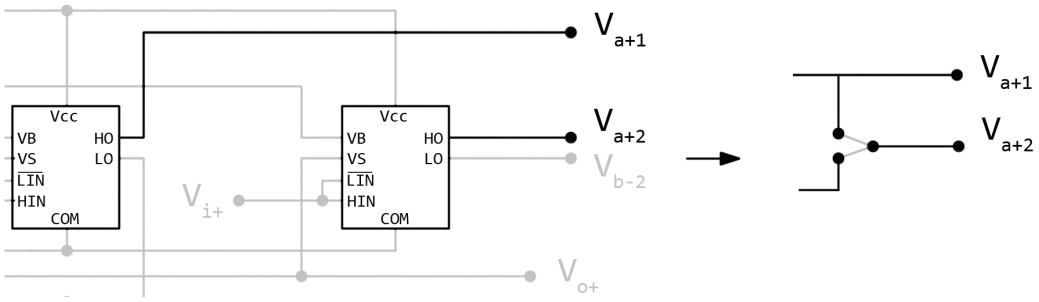

Figure 6.11.: Jumper bridge for selecting the gate driver configuration.

6.11. PCB Design

The PCB was designed using the software *Eagle* (5.8).The schematic comprised the features and blocks explained above, and is located at Appendix A (Schematics A.3 and A.4).

After juggling with the program for a while, a compact yet clean layout was devised. Despite the Auto-route feature being available, the high-current traces had to be drawn by hand to ensure that the path resistance would be as low as possible. Still, such traces (namely the ones flowing from and to transistors drains and sources) were designed so they could be reinforced with external wires.

Also attention was paid to corners: sudden changes in direction were avoided in order to reduce electromagnetic emissions. Furthermore, we did not draw current-carrying traces parallel to each other so crosstalk was reduced.

6.12. Manufacturing of PCB

When the layout was finished and approved (final design on Figure A.5), it was sent to fabrication. Shortly after the PCB was received we soldered all the components. It was tested with a small current through a 10kΩ resistor, in order check if the bridge worked as it should in low-power operation.

When it was clear that the board operated as expected, the testing phase began.

7. Testing

With the PCB ready, it was time to make some measurements to check if the project worked as it should. Several configurations were tested and reviewed in order to detect possible flaws or faults. The magnitudes of interest will be temporal (regarding switching), electrical (voltage drops, equivalent resistances) and thermal. The equipment that was used for this task was a four-channel oscilloscope and an infra-red thermometer.

The connections were made according to the wiring diagram displayed on Figure 7.1. Each oscilloscope probe is represented by a long arrow, together with its name. The fourth (V_1), not shown, measures the output of the gate drivers and is the one used by the trigger function. Although the board should be operated at a frequency of 0.1 to 1Hz, the tests were performed at 1kHz in order to visualize properly the signal on the oscilloscope. Since the switching behaviour is completely frequency-independent, the conclusions of these tests are perfectly valid for lower frequencies. Finally, the load was simulated with a wire that offered a resistance similar to that the of the specimens.

7.1. Test Set-Ups

7.1.1. Two gate drivers, no snubbers

The first tested set-up was the simplest of all: through appropriate wiring of the jumpers, the board was configured for operating with two gate drivers (one per branch). Also there were no snubber capacitors.

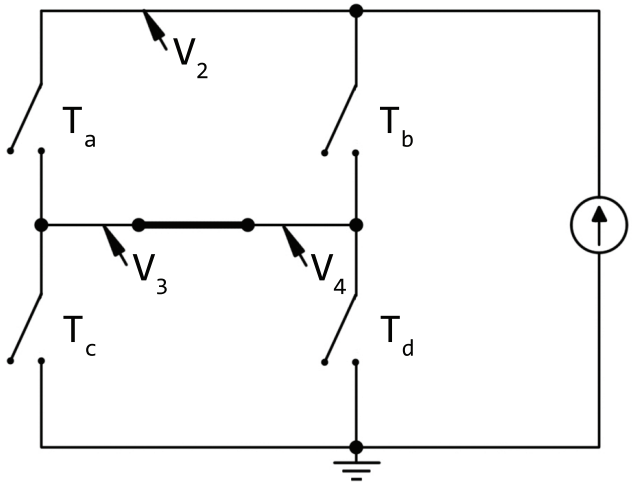

Figure 7.1.: Test setup. The long arrows represent oscilloscope probes.

Operation at 5 Amps

The acquired data is shown in Figure C.1. It displays both the turn-on and turn-off transitions. Among the relevant information that we can get through visual inspection, one thing stands out: the high overshooting and ringing during switching, as a result of the inductance of the load, and maybe to the stray inductances of the board. A filtering capacitor in parallel with each pair of transistors should be added in order to improve the signal.

Regarding the data, they are summarized in Table 7.1. They were extracted from the oscilloscope prints, and through their manipulation important values were obtained. This table is arranged as follows:

- Data columns: each one shows the measured values while one branch was conducting and the other was not.
- First three data rows: they are the acquired values, as extracted from the oscilloscope graph.
- Second block: these four rows show the voltage drops across the switches (named according to Figure 7.1). They are not the voltage-to-source voltages of the transistors: the values also include the voltage drop belonging to the copper traces.

- Last four rows: calculated using the voltages from the previous block and the total current, they are the equivalent On-resistances of the H-bridge.

I = 5 Amps	Pos. Diagonal ON	Neg. Diagonal ON
$V_+ = V_2$	90,2 mV	95,7 mV
V_3	73,1 mV	17,2 mV
V_4	17,5 mV	65,1 mV
$V_a = V_2$-V_3	17,1 mV	78,5 mV
$V_b = V_2$-V_4	72,7 mV	30,6 mV
$V_c = V_3$	73,1 mV	17,2 mV
$V_d = V_4$	17,5 mV	65,1 mV
$R_a = V_a/I$	3,42 mΩ	
$R_b = V_b/I$		6,12 mΩ
$R_c = V_c/I$		3,44 mΩ
$R_d = V_d/I$	3,5 mΩ	

Table 7.1.: Data gathered with two gate drivers and no snubber capacitors. The current was 5 Amps.

These data were acquired with an ambient temperature of 25.6°C. At this current the case was at $T_j = 27.8°C$, a ridiculous increase. Assuming that the drain-to-source resistance of one MOSFET is 3.14mΩ (the one it should have when the current is at its maximum; see section 6.2.4), the junction temperature can be estimated as follows:

$$\begin{aligned} P_{on} &= R_{DS,on} I_D^2 = 3.14\text{m}\Omega \cdot (2.5\text{A})^2 \sim 0.02\text{W} \\ P_{on} &= \frac{T_j - T_c}{R_{\theta,jc}} \Rightarrow T_j = T_c + P_{on} R_{\theta,jc} \sim 27.8°\text{C} \end{aligned}$$

Operation at 10 Amps

When it was clear that the board was properly working, the total current was increased to 10 Amps. The chosen switching frequency was the same as before: around 1kHz.

The concerning oscilloscope screenshot is shown in Figure C.2, and the interpreted data can be found in Table 7.2. The methodology that was followed is the same as in the previous case, when the current was 5A.

I = 10 Amps	Pos. Diagonal ON	Neg. Diagonal ON
$V_+ = V_2$	186,1 mV	200,6 mV
V_3	154,7 mV	38,4 mV
V_4	38,4 mV	139,7 mV
$V_a = V_2\text{-}V_3$	31,4 mV	162,2 mV
$V_b = V_2\text{-}V_4$	147,7 mV	60,9 mV
$V_c = V_3$	154,7 mV	38,4 mV
$V_d = V_4$	38,4 mV	139,7 mV
$R_a = V_a/I$	3,14 mΩ	
$R_b = V_b/I$		6,09 mΩ
$R_c = V_c/I$		3,84 mΩ
$R_d = V_d/I$	3,84 mΩ	

Table 7.2.: Data gathered with two gate drivers, no snubber capacitors and a total current of 10 Amps.

In this test the ambient temperature was 25.6°C too, and the one at the case of the transistor 33.6°C, a few degrees higher than before. Following the calculations performed some lines above, the junction temperature was found to be 33.7°C. In fact, being the junction-to-case thermal resistance of the MOSFET so small the temperature of the case will be roughly the same as the one of the junction.

Going back to the oscilloscope capture, there is a peculiarity (also present in the test at 5 Amps): the voltage at the upper part of the H-Bridge (measured with the probe 2, V_2) ought be constant, since the voltage drop on the whole setup should be the same regardless of the diagonal which is conducting. However, there is a difference: while the positive diagonal (transistors *a*, *d*) is ON we have $V_2 = 90.2$mV, and in the complementary case the drop is slightly higher (95.7mV). After calculating the equivalent resistances of each switch, it is easy to notice that there is something odd: the resistance R_b is much higher than the other three. There are two possible causes for this behaviour. The first one is that, due to the position of the probes,

this resistance includes a higher length of copper. The second option is worse: it could happen that one of the transistors of the pair is not properly working, and as a result the resistance of the switch would be doubled. Before carrying out the next tests this problem will be addressed.

7.1.2. Two gate drivers, 1μF snubbers

I = 6.5 Amps	Pos. Diagonal ON	Neg. Diagonal ON
$V_+ = V_2$	115,9 mV	119,6 mV
V_3	94,5 mV	19,1 mV
V_4	21,8 mV	83,3 mV
$V_a = V_2\text{-}V_3$	21,4 mV	100,5 mV
$V_b = V_2\text{-}V_4$	94,1 mV	36,3 mV
$V_c = V_3$	94,5 mV	19,1 mV
$V_d = V_4$	21,8 mV	83,3 mV
$R_a = V_a/I$	3,29 mΩ	
$R_b = V_b/I$		5,58 mΩ
$R_c = V_c/I$		2.93 mΩ
$R_d = V_d/I$	3,35 mΩ	

Table 7.3.: Data gathered with two gate drivers, snubber capacitors (1μF) and a total current of 6.5 Amps.

The next test that was carried out involved several improvements of the system. The first of all was the diagnostic and solution to the bridge resistance mismatch in one of the branches, as it was found in the previous section. Gladly, the root of the problem was not a non-working transistor: the anomaly was caused by an uneven length of the copper paths in each of the diagonals. It can clearly seen in Figure A.5: the positive input of the bridge, V_+, is located much closer to the upper-left pair of transistor than to the upper-right pair. This inequality was softened including additional air-wires connecting the spots labelled as `W2`.

The test was performed at a current of 6.5A and a frequency of 1kHz (as explained before, it is low enough for switching losses not being accountable) in order to get a proper visualization of both rising and falling edges. The

oscilloscope capture is displayed in Figure C.3, and the interpreted data in Table 7.3.

Concerning the branch resistances, there are two differences when compared to the previous set-up. The first one is the commented external wire: the R_b value is around 0.5mΩ lower than before. Although it is still higher than for other branches, its decrease proves that the diagnostic was right. The second one is also an improvement on R_c: it is purely based on the fact that probe 3 was located at another spot, making the value more faithful to reality.

There was also a temperature performance improvement due to the inclusion of the snubber capacitors: the case-to-ambient temperature difference was 2.2°C, the same value that was obtained without snubbers at a lower current.

7.1.3. Test with four gate drivers

I = 10 Amps	Pos. Diagonal ON	Neg. Diagonal ON
$V_+ = V_2$	179,4 mV	191,9 mV
V_3	145 mV	32,5 mV
V_4	32,5 mV	135,6 mV
$V_a = V_2\text{-}V_3$	34,4 mV	159,4 mV
$V_b = V_2\text{-}V_4$	146,9 mV	56,3 mV
$V_c = V_3$	145 mV	32,5 mV
$V_d = V_4$	32,5 mV	135,6 mV
$R_a = V_a/I$	3,44 mΩ	
$R_b = V_b/I$		5,63 mΩ
$R_c = V_c/I$		3,25 mΩ
$R_d = V_d/I$	3,25 mΩ	

Table 7.4.: Data gathered with four gate drivers, snubber capacitors (1μF) and a total current of 10 Amps.

The next test included the snubber capacitors that were added on the previous run, as well as two additional driver ICs so that each MOSFET was

driven by one stage. The configuration jumpers were accordingly changed for this purpose.

In this case the current with which the measurements were taken was 10A. The concerning oscilloscope picture is shown in C.4, and the resulting equivalent voltages and resistances appear in Table 7.4.

It is interesting to note that the ringing/overshooting present during switching is mostly due to the inductive nature of the load and to the inappropriate banana connectors that were feeding the board. The deployed system should address this problem by the use of proper twisted-pair cable for both high-current inputs and outputs.

Regarding the temperature characteristics of this set-up, it was not possible to obtain data for comparing it with the previous board configurations: the temperature of the case of the MOSFETs was similar to that which was obtained in section 7.1.1. This was due to the lack of adequate laboratory equipment that could provide the system with the required 30A. In any case, it is interesting to remark that the performance of the board was better at higher frequencies (1kHz) than in DC. The explanation to this phenomenon is that duty ratio was around 0.5, making the effective power lower. In addition, the applied frequency was low enough to not heat excessively the device through switching losses.

7.2. Extrapolation to Full Capacity

Had a 30A current source been available, it would have been possible to measure what was the case or junction temperature of the MOSFETs at the maximum rating for the board was designed. However, the results point out that the system had a proper thermal design, being the MOSFETs only 8-10°C warmer than the room temperature when the system was at one third of its capacity.

7.3. Maximum Ratings

Although the board was designed for delivering safely a current of 30A, it may seem that it could easily deliver higher currents if needed. However, this is not advisable without improved cooling: according to the equations developed in section 6.2.4, a current of 33A (just 3 more Amps than the maximum value) would increase the junction temperature in 20°. This happens due to the fact that power losses are not linear with current, but quadratic. Moreover, the relation is not even quadratic: due to the increase of drain-to-source resistance with temperature, the growth is higher. In big-Theta notation, we could argue that $T_j(I_t) = \Theta(I_t^3)$.

The conclusion in this regard is that, if it is needed to use this system with currents higher than 30A, enhanced cooling methods should be used in order to keep the MOSFETs at a safe temperature.

8. Conclusion and Future Work

Finally the project came to its end. Before closing this document, it may be relevant to evaluate the fulfilment of the goals that were set prior to the start of this work (section 1.3):

- **Study of the DCPD technique and understanding of the role the final system will play in it:** a working background was acquired about this materials science analysis method.
- **Deconstruction and reverse-engineering of the previous version of the system:** the former board was successfully analysed, gaining knowledge about several topics in the process, such as protective components or noise-free hysteresis comparators.
- **Detailed comprehension of the Power MOSFET transistor:** from almost ignorance about MOSFETs, a solid theoretical base was acquired through extensive study of relevant literature (mainly books and application notes). Moreover, original Appendix B was written to back that knowledge up.
- **Thorough research of several power electronics topics required for the conception of the system:** comprehensive understanding of subjects regarding the matter was gained, specially concerning MOSFET gate drivers and thermal analysis of power transistors. This was done in a pure autonomous way, reading extensively about the matter and deciding which areas were to be deepened.
- **Design and simulation of the circuit:** a careful sketch of the circuit was made, avoiding faults thanks to the relevant computer simulations. Some insight was gained concerning the CAD analysis of coupled thermal-electrical systems.
- **Fabrication of a PCB and prototyping of the system:** know-how regarding layout design was acquired, as well as about pertinent software (Eagle).

- **Testing in order to evaluate performance:** it was learnt how to carry out tests involving high currents by the correct use of the necessary laboratory equipment, as well as to identify and correct errors using the oscilloscope.
- **Writing of this report:** as a result of the accomplishment of the aforementioned goals, this detailed document arose showing all the knowledge that was gained during the development of the project.

8.1. Further Developments

Some of the directions in which the built system could be improved are the following:

- Include a limiter of maximum frequency, in order to make sure the current change rate does not exceed the (0.1-1Hz) range.
- Implement a temperature measuring device based on the drain-to-source resistance and on the total input current that is able to shut the board off if a certain temperature is exceeded.
- Improvement of the PCB layout in order to reduce as much as possible the stray inductances.
- Add new air-wires connecting the points marked as `W` on the PCB (A.5) in order to reduce path resistances.
- Estimate the path resistances of the H-bridge so that an equivalent model can be identified.
- Add a shunt resistor capable of measuring the total current entering the bridge, as well as stage that based on that shunt can detect if the maximum current is exceeded and accordingly switch the board off.
- If the gate driver ICs were updated to a pin-compatible model with higher output current, the board could be easily used in ACPD applications.

8.2. Personal Thoughts

As a closing for this thesis, I think it is a work that not only achieved the goals that were originally set, but also gave me a serious background on power electronics, a discipline that was totally new for me. Even if at some points I thought I would not make it, I always was able to find my way back.

Another challenging part was the writing of this document: it is said that something is not properly understood as long as one is not able to explain it, and that proved true while I was penning this thesis. There were many times in which I had to go back to the literature in order to get some more information and clearly make my point. Regarding the illustrations that enclose the text, it took some effort to design them but I thought it was worth having a homogeneous, visually appealing paper that could deliver the content more easily.

In conclusion, this project was worth the time spent on it: I learnt a lot, I enjoyed during its development and, eventually, was happy with the result.

Appendix

Appendix A.

Schematics and PCB Layouts

In this Appendix there are gathered several schematics and PCB Layouts regarding the project.

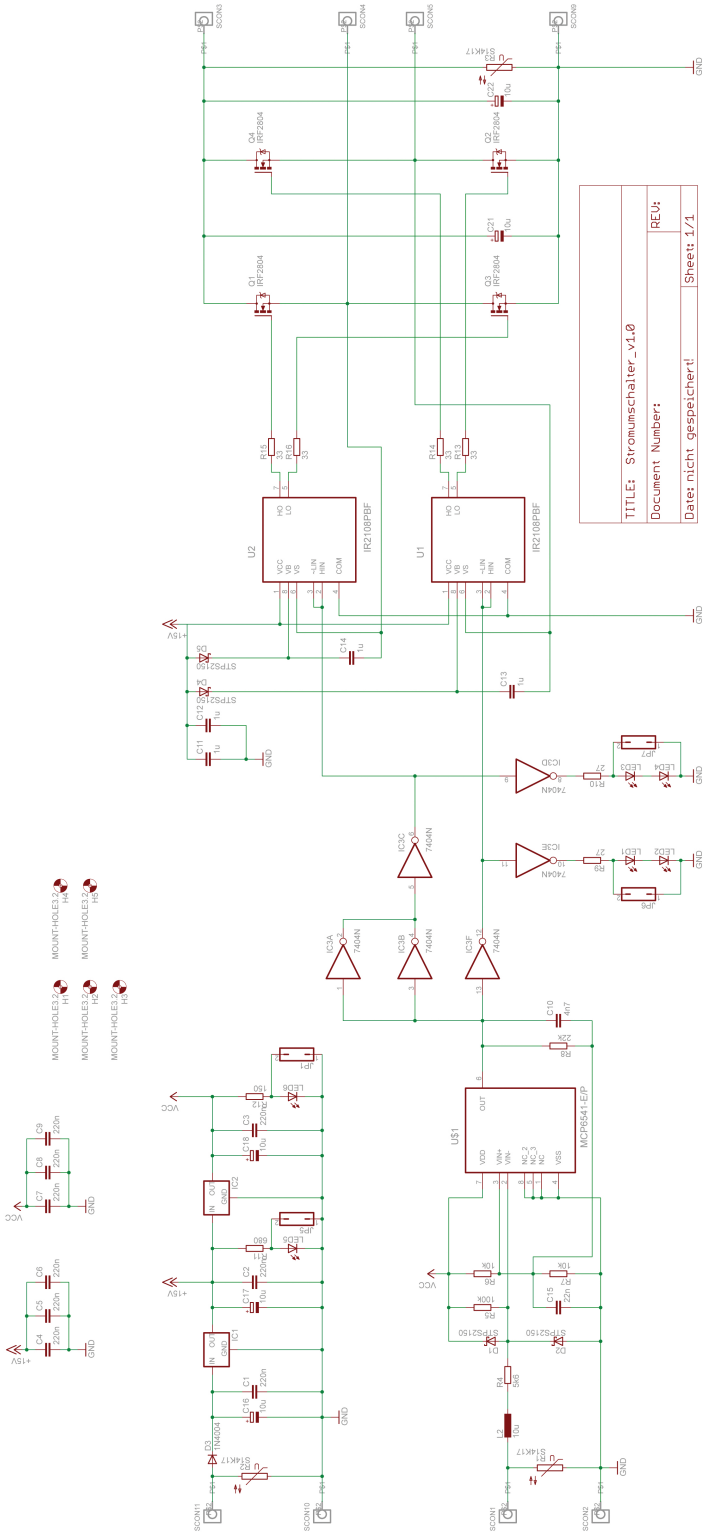

Figure A.1.: Previous version of the switching board

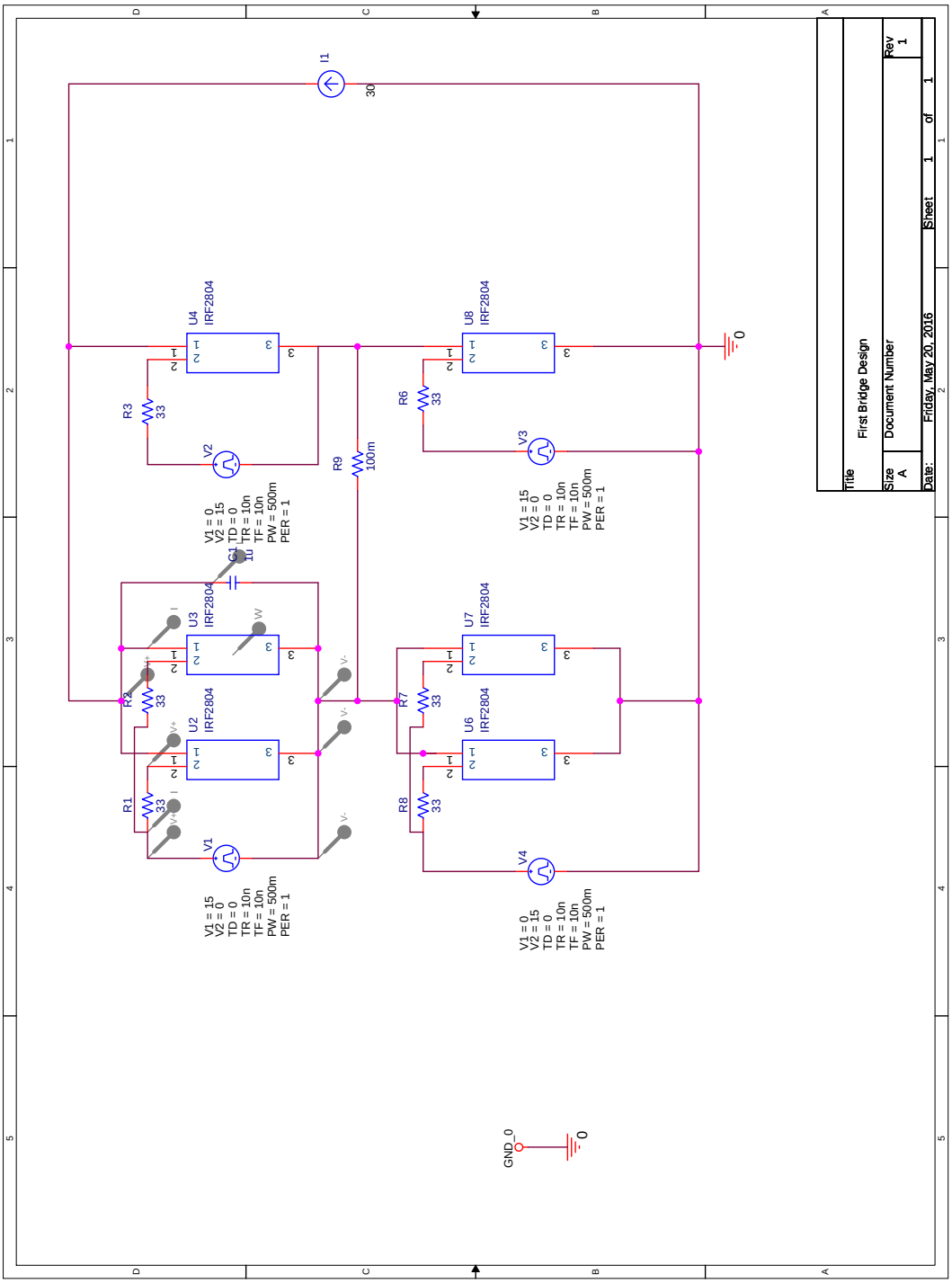

Figure A.2.: OrCAD schematic of the first simulated H-Bridge

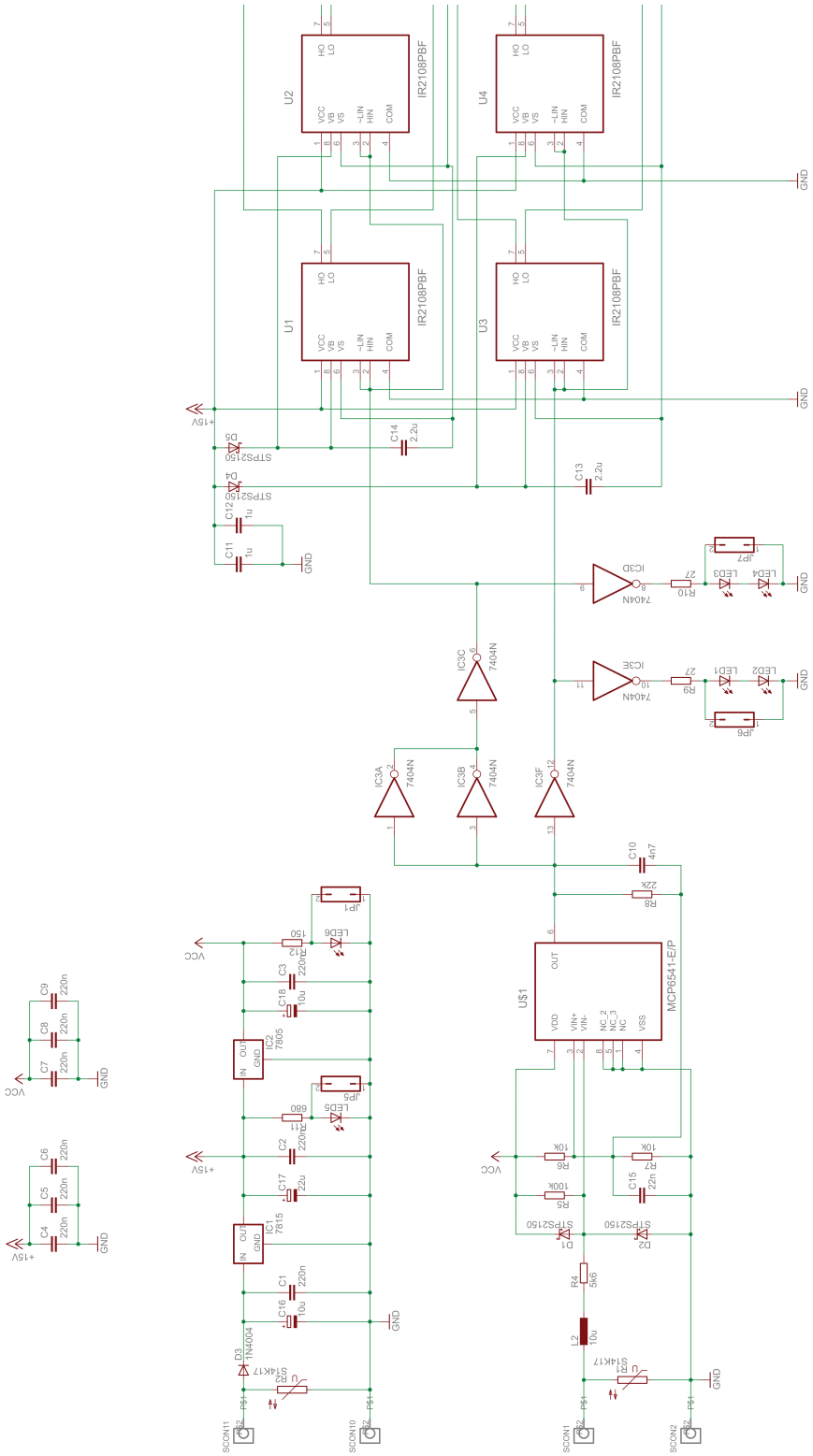

Figure A.3.: Schematic of the final design (left half).

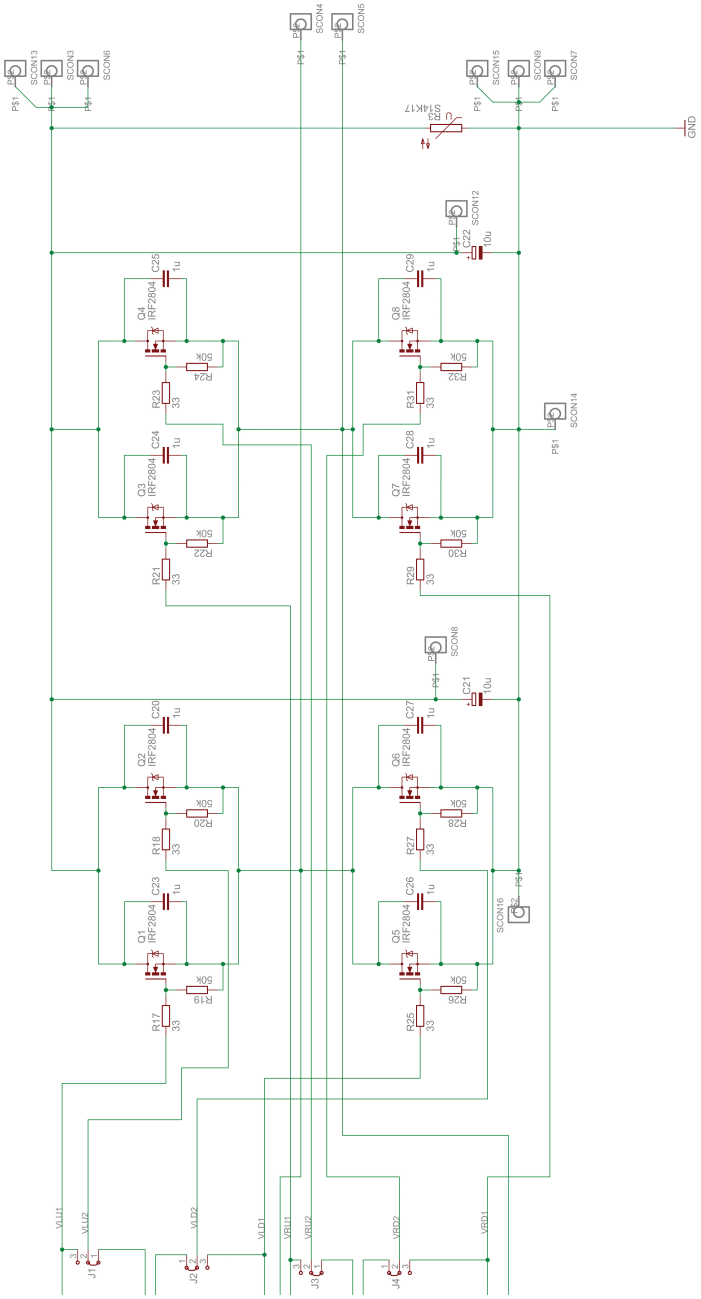

Figure A.4.: Schematic of the final design (right half).

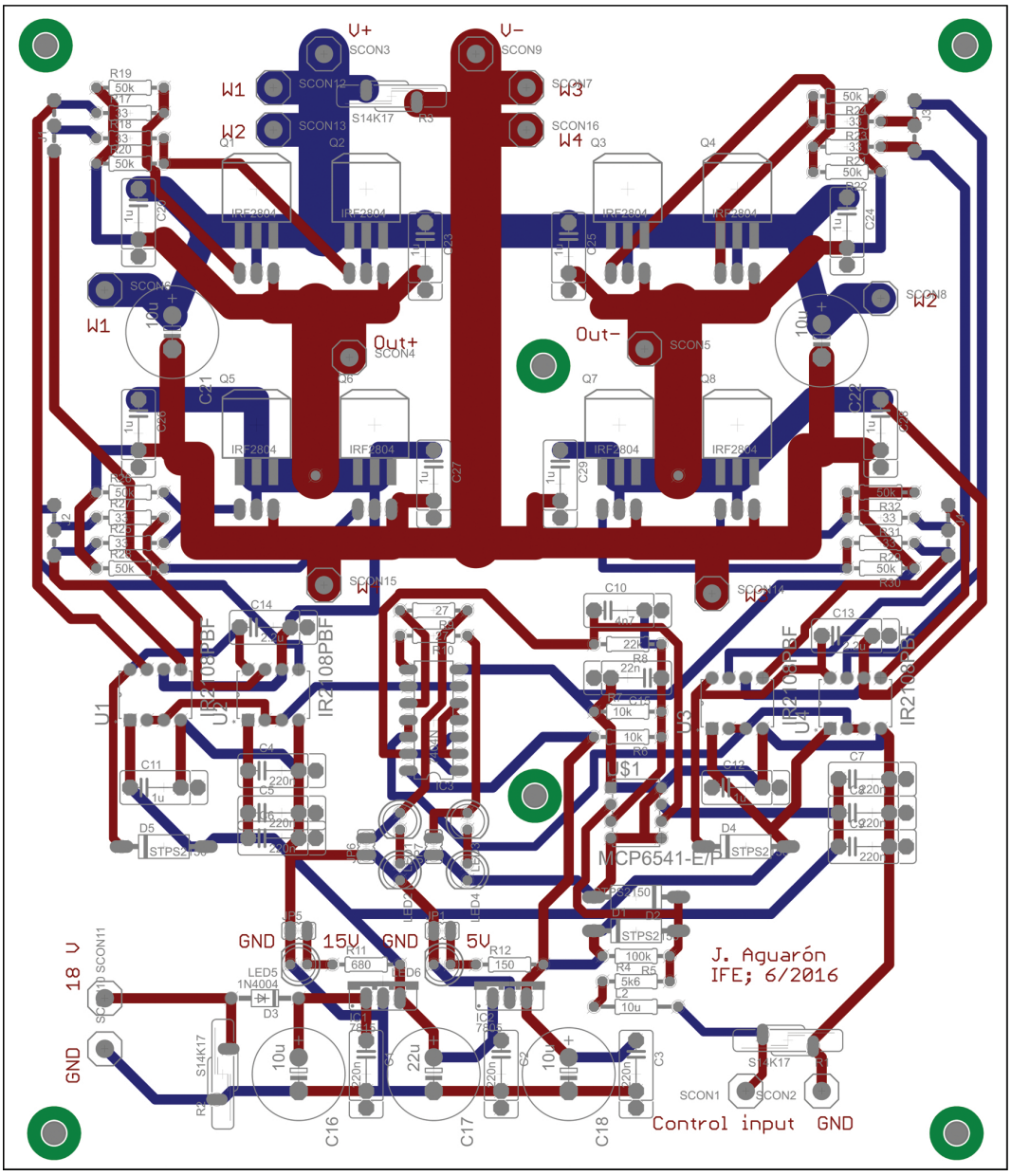

Figure A.5.: Layout of the PCB, as sent for manufacturing. Red traces: top layer. Blue traces: bottom layer.

Appendix B.

Estimating MOSFET Switching Behaviour Through (V_{GS}, Q_G) Curves

B.1. Purpose of This Study

After reading many application notes and papers (main works: *Gate Drive Characteristics and Requirements for HEXFET Power MOSFETs* n.d.; *Understanding and Predicting Power MOSFET Switching Behavior* n.d.) about the processes that take place during the turn-on or turn-off of a MOSFET, it was clear that there exist several approaches to the analysis of this phenomenon (through simulation, based on the Miller capacitance, relying solely on datasheet parameters...). This appendix is an attempt to tackle that problem eventually resulting in a consistent, well-defined algorithm that allows to estimate the switching times in order to properly dimension the gate drive.

B.2. Charge of a Capacitor

First we will start with the long-known RC series circuit (Figure B.1). Even if it is a very simple system, it is convenient to review it in order to extract some equations that will be useful later in the text.

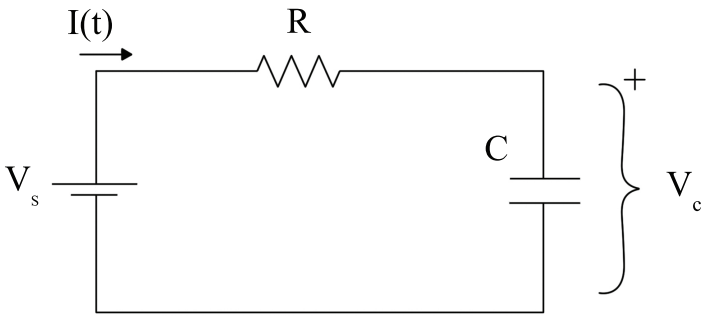

Figure B.1.: Basic RC circuit

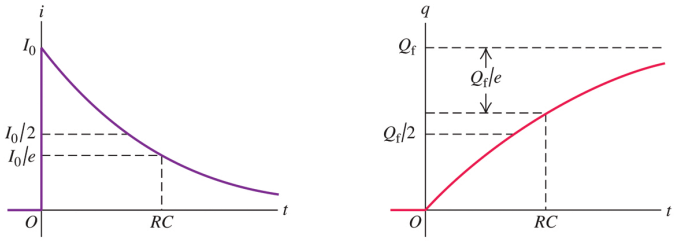

Figure B.2.: Current and charge of capacitor (Young and Freedman, 2008)

The initial conditions and assumptions are the following: the capacitor is discharged ($V_c(0) = 0, Q_c(0) = 0$), and the capacitance C, resistance R and voltage V_s are known and constant. In $t = 0$, then, the current through the loop is nothing else than $\frac{V_s}{R}$, as can be seen on Figure B.2. Since $i = \frac{dq}{dt}$, $V_c = \frac{q}{C}$ and $i = \frac{V_s - V_c}{R}$, we obtain:

$$\frac{dq}{dt} = \frac{V_s}{R} - \frac{q}{RC} = \frac{CV_s - q}{RC}$$

Rearranging terms and integrating, this yields:

$$\frac{dq}{q - CV_s} = -\frac{dt}{RC} \Rightarrow \int_0^q \frac{dq^*}{q^* - CV_s} = -\int_0^{t^*} \frac{dt^*}{RC} dt^* \Rightarrow \frac{q - CV_s}{-CV_s} = e^{-t/RC}$$
$$\xrightarrow{Q_f = CV_s} \frac{q - Q_f}{-Q_f} = e^{-t/RC} \Rightarrow q = Q_f(1 - e^{-t/RC})$$

Furthermore, considering that $V = Q/C$, we get to the classical expression of the voltage in the capacitor over time:

$$V_c(t) = V_s(1 - e^{-t/RC}) \tag{B.1}$$

However, if we take arbitrary integration limits t_1, t_2 and play with the equations, it is possible to express the time required by the capacitor to reach a specific voltage:

$$t_2 - t_1 = -RC \ln\left(1 - \frac{V_c(t_2) - V_c(t_1)}{V_s - V_c(t_1)}\right) \tag{B.2}$$

Naming V_R the voltage over the resistor R we reach the final equation, which will be used later in the text:

$$\Delta t = -RC \ln\left(1 - \frac{\Delta V_c}{V_R(t_1)}\right) \tag{B.3}$$

In short, this expression provides us with an easy way to calculate the time needed by the capacitor to be charged from a certain voltage up to another.

B.3. MOSFET Gate as a Capacitor

One of the main advantages of MOSFET transistors over other technologies, such as BJT, is that the former do not need a constant gate current to be kept in a certain state (whereas bipolar transistors are to be fed a base current).

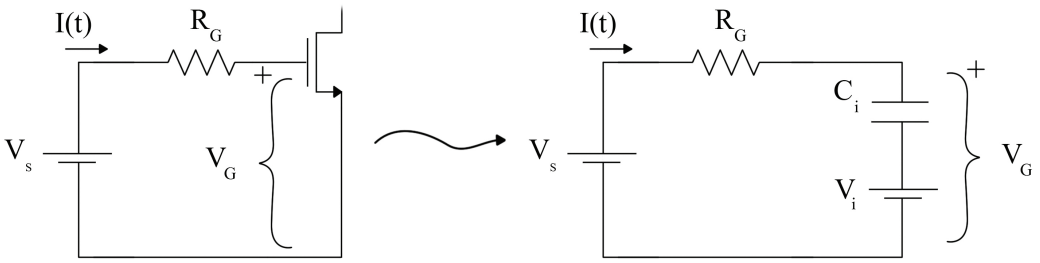

Figure B.3.: Equivalent circuit seen from the Gate terminal

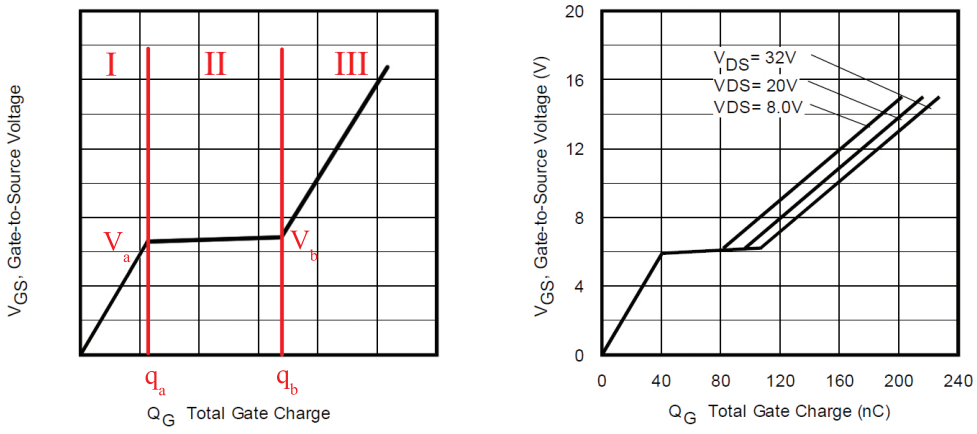

Figure B.4.: Left: a typical (V_{GS}, Q_G) curve. Right: the IRF2804-specific curve.

That advantage arises from the fact that, seen from the gate terminal, the MOSFET is a capacitor. In fact, the classical symbol of the MOSFET was designed to resemble one.

Usually MOSFET gate drivers are used because they offer a short-impedance path for sourcing or sinking the current peaks during switching. But, in the end, they can be modelled as a voltage source (V_s) and a gate resistor(R_G). So, when coupled to a MOSFET, the equivalent is nothing but the one shown in Figure B.3: a simple RC circuit.

Due to the capacitive features of the gate terminal, it is common to find in

the datasheets provided by manufacturers a graph linking gate voltage and stored charge. A prototype of such curve can be seen on Figure B.2, left. A real example taken from the IRF2804 datasheet is shown on Figure B.2, right.

This is a very interesting picture since it will let us estimate, after some transformations, the switching time of the MOSFET. But first we will have a look at the meaning of the different sections indicated on Figure B.2, left. As we already stated, the definition of capacitance is $C = Q/V$. Having on the graph the gate-to-source voltage as a function of gate charge, it is evident that the derivative in one point of the curve is $\frac{dV_{GS}}{dQ_G} = \frac{1}{c}$. That is, the inverse of the small-signal capacitance.

Luckily, each of the three sections (I, II, III) is a straight line: that allows us to state that, in every section, the slope is constant and hence the capacitance. That makes possible to identify the gate-source with an equivalent capacitor. For instance, in section I the corresponding circuit could be modelled by a capacitor with value $C_1 = (V_a/q_a)^{-1} = q_a/V_a$ (Figure B.5). For sections II and III the point in which they start has to be taken into account; in the case of the third part that shift is modelled with a voltage source of the same value as the initial point (as seen on Figure **??**). Section II is the same as III, but it is important to note the low value of the slope (thus a huge capacitance). In literature this part of the curve is known as *Miller plateau*, and can cause power-sharing inequalities in paralleled MOSFETs (*Using power MOSFETs in parallel* 2015). In any case, the equivalent capacitor is so large that can be omitted and modelled mathematically with different tools (more on B.4.2).

B.4. Prediction of Switching Behaviour

Now that the underlying theory and assumptions are explained, it is time to put them into practice. In this section we will reach a simple way of estimating specific switching times for the MOSFET, using the same type of analysis for each of the curve sections shown in Figure B.2.

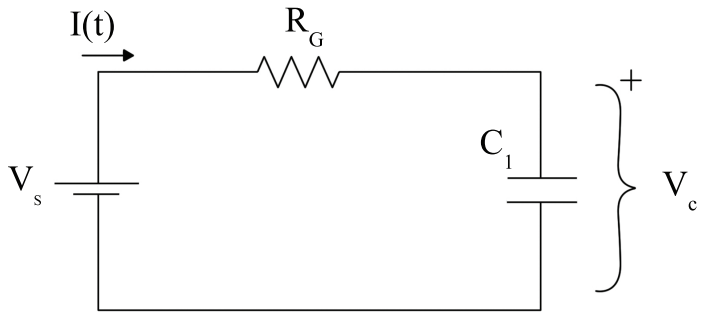

Figure B.5.: Model of the first section of the curve.

B.4.1. Section I

As mentioned before, the equivalent driver-transistor circuit of this section is the one displayed on Figure B.5. Again, the capacitance during the whole process is $C_1 = q_a/V_a$ (all voltages and charges named according to that graph, B.2). Initially the capacitor is discharged, will charge until its voltage (V_c) reaches V_a. From that moment on this model will no longer be valid, and we shall use the one specific for section II.

Using equation B.3, we discover that the time needed to reach V_a is:

$$\Delta t = -RC \ln\left(1 - \frac{\Delta V_c}{V_R(t_1)}\right) \Rightarrow t_1 = -R_G C_1 \ln\left(1 - \frac{V_a}{V_s}\right) \tag{B.4}$$

Another remarkable use of this equation in the present section is estimating the $t_{d,on}$ of the MOSFET. That is the time needed by the gate-to-source voltage to reach the threshold voltage, V_{TH}. Since that value is below the Miller voltage (V_a) we can safely use the same formula and values:

$$t_{d,on} = -R_G C_1 \ln\left(1 - \frac{V_{TH}}{V_s}\right) \tag{B.5}$$

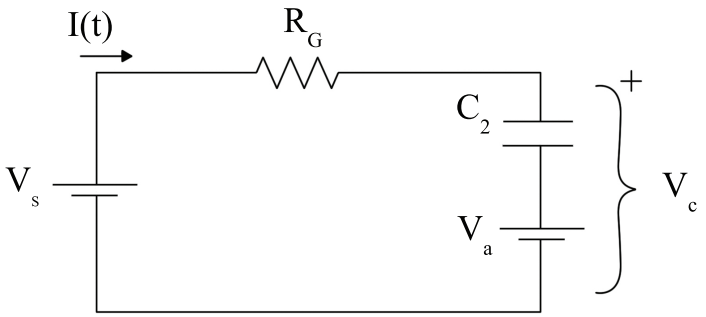

Figure B.6.: Model of the second section of the curve.

B.4.2. Section II

For this section the model that applies is that on Figure B.4.2. As mentioned before, the initial voltage with which the equivalent circuit works is V_a, and so is the value of the voltage source displayed. Using the same formula as before, we obtain the time needed to "cross" section II:

$$\Delta t = -RC \ln\left(1 - \frac{\Delta V_c}{V_R(t_1)}\right) \Rightarrow t_2 - t_1 = -R_G C_2 \ln\left(1 - \frac{V_b - V_a}{V_s - V_a}\right) \tag{B.6}$$

However, in many datasheets the values V_a and V_b are very close to each other (or simply the same) and that causes an equivalent infinite capacitance. A simple way of overcoming this difficulty is going back to the definition of current and latch on it until we see the light:

$$i = \frac{dq}{dt} \Rightarrow q = \int i \cdot dt \xrightarrow{i:constant} \Delta q = i\Delta t \tag{B.7}$$

The voltage V_{GS} along this section of the curve is clamped to V_a, and so the current will be. Now we are ready to calculate the required time:

$$i = \frac{V_s - V_a}{R_G} \Rightarrow \Delta t = \frac{\Delta q}{i} \Rightarrow t_2 - t_1 = \frac{(q_b - q_a)R_G}{V_s - V_a} \tag{B.8}$$

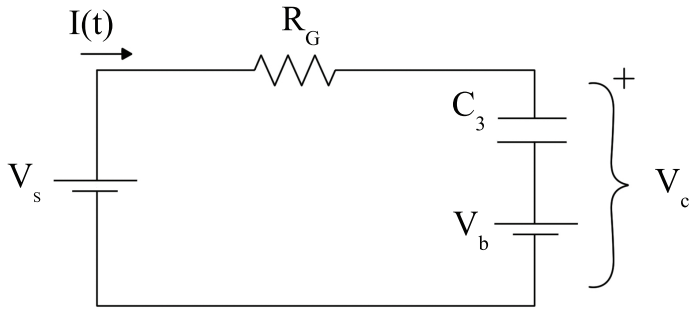

Figure B.7.: Model of the third section of the curve.

B.4.3. Section III

For calculating the parameter C_3 of this part of the curve we will take the q_c at which V_{GS} reaches V_s (that is, when the transistor is completely on). Then, the equivalent capacitance is $C_3 = (q_c - q_b)/(V_s - V_b)$. Since the time needed to fully charge a capacitor is theoretically infinite, in order to apply our equation we set an arbitrary final capacitor voltage, such as $V_f = 0.95V_s$:

$$\Delta t = -RC\ln(1 - \frac{\Delta V_c}{V_R(t_1)}) \Rightarrow t_3 - t_2 = -R_G C_3 \ln(1 - \frac{V_f - V_b}{V_s - V_b}) \qquad \text{(B.9)}$$

B.4.4. Review of some important times

There exist several relevant temporal parameters. We already calculated $t_{d,on}$, but here we will briefly enumerate them, along with the formula for estimation:

- Delay time (switch-on): $t_{d,on} = -R_G C_1 \ln(1 - \frac{V_{TH}}{V_s})$
- Rise time: $t_r = t_a$
- Total switching time: $t_{on} = t_3$

B.4.5. Extrapolation to switch-off

Although this analysis has been focused on the behaviour of the MOSFET during switch-on, usually the turn-off temporal parameters are more relevant because they are typically larger. In order to estimate them, the process that needs to be followed is the same, but starting with the capacitor discharge equations.

B.5. Matlab Code

A small script was written in Matlab in order to get a better grasp of how each parameter modifies the switching times of the MOSFET:

```
%% INPUT DATA
%Execute everything this section first
% Circuit-specific
Vs = 15;      %Volts
Rg = 33;      %Ohms
% MOSFET-specific (take from datasheet)
Va = 5.9;         %V
qa = 40e-9;       %C
Vb = 6.15;        %V
qb = 85e-9;       %C
Vc = 0.95*Vs + 0.05*Vb;

%% Take qc from datasheet
qc = 180e-9;

%% Calculate Capacitors
C1 = qa/Va;
C2 = (qb-qa)/(Vb-Va);
C3 = (qc-qb)/(Vc-Vb);

%% Calculate times
ta = -Rg*C1*log(1-(Va/Vs));
```

```
23 tb = ta - Rg*C2*log(1-(Vb-Va)/(Vs-Va));
24 tc = tb - Rg*C3*log(1-(Vc-Vb)/(Vs-Vb));
25
26 %% Output
27 T1 = sprintf('Time ta will be %0.5g', ta);
28 T2 = sprintf('Time tb-ta will be %0.5g', tb-ta);
29 T3 = sprintf('Time tb: %0.5g', tb);
30 T4 = sprintf('Total switching time: %0.5g', tc);
31 disp(T1); disp(T2); disp(T3); disp(T4);
```

Appendix C.

Oscilloscope Screen Captures

This Appendix contains the different oscilloscope prints that were acquired during the testing phase.

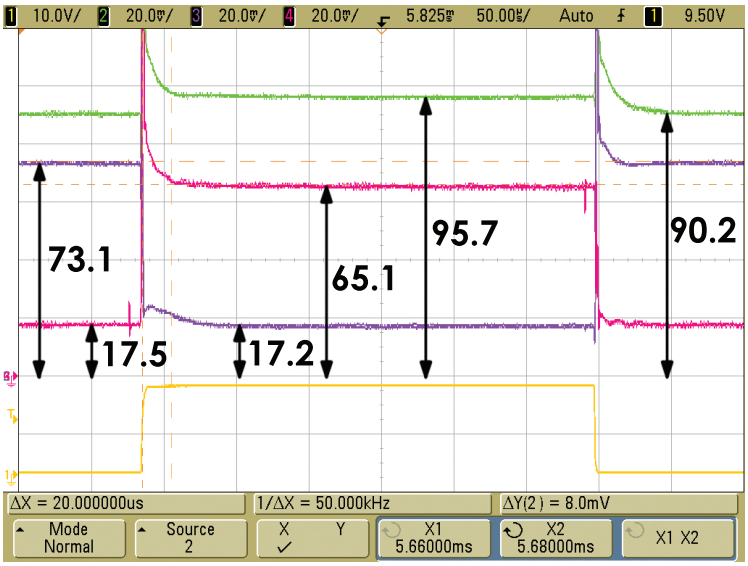

Figure C.1.: Oscilloscope capture: two drivers, no snubbers, 5 Amps. Values in mV.

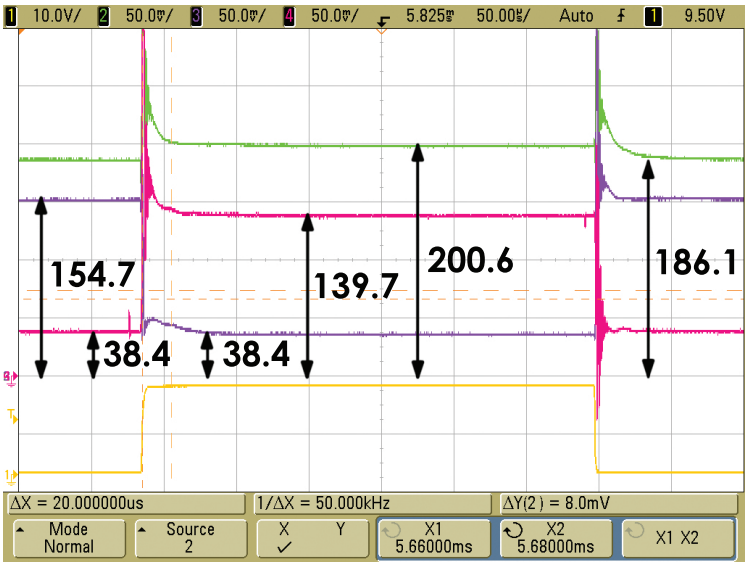

Figure C.2.: Oscilloscope capture: two drivers, no snubbers, 10 Amps. Values in mV.

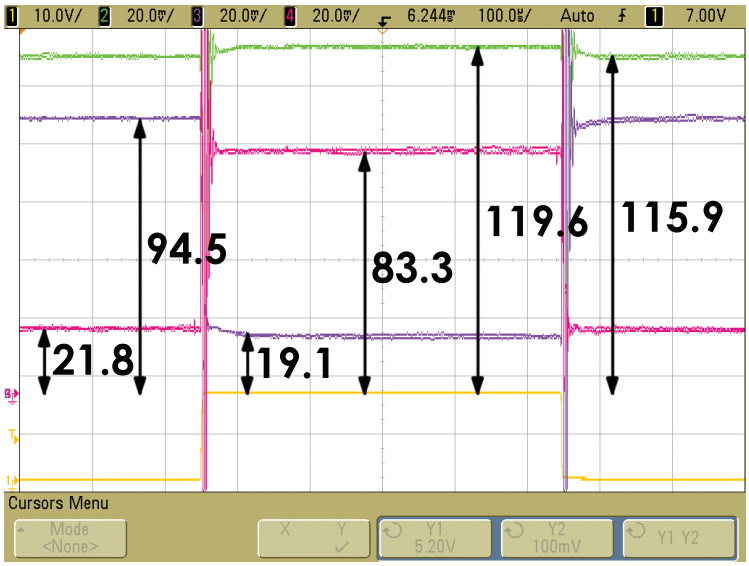

Figure C.3.: Oscilloscope capture: two drivers, 1μF snubbers, 6.5 Amps. Values in mV.

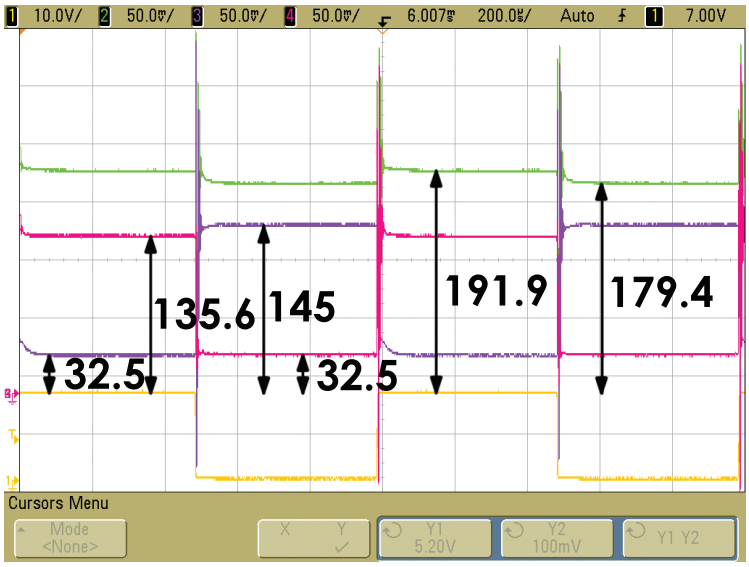

Figure C.4.: Oscilloscope capture: four drivers, 1μF snubbers, 10 Amps. Values in mV.

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