28820 - Electronic Technology II

Información del Plan Docente

Academic Year	2016/17
Academic center	175 - Escuela Universitaria Politécnica de La Almunia
Degree	424 - Bachelor's Degree in Mechatronic Engineering
ECTS	6.0
Course	3
Period	First semester
Subject Type	Compulsory
Module	---

1.Basic info

1.1.Recommendations to take this course

1.2.Activities and key dates for the course

2.Initiation

2.1.Learning outcomes that define the subject

2.2.Introduction

3.Context and competences

3.1.Goals

3.2.Context and meaning of the subject in the degree

3.3.Competences

3.4.Importance of learning outcomes

4.Evaluation

5.Activities and resources

5.1.General methodological presentation

The learning process designed for this subject is based on the following:

This Electronic Technology II course is conceived as a set of contents, but divided into four blocks. The first block, brings together concepts of operation of the power components and protective elements. The second and third blocks, form the core of the subject matter must contribute to the formation of the student: static switches, drives and regulators, rectifiers and power inverters. The final block contains some of the key applications of power electronics, without attempting to

cover all fields of application of this discipline.

The first three blocks will be dealt with under three fundamental and complementary ways, these are: the theoretical concepts of each teaching unit, solving problems or issues and laboratory practices, supported in turn by another series of activities such as tutorials and seminars and will be tested individually, independent for each of the blocks.

The fourth block will have a different treatment, as the students will work only in groups only in the issues that they were previously assigned, they will be allowed to express their preferences but all topics will be assigned to a group. They will prepare presentation materials and defend their work with a public exhibition, which will be valued by the other students and the teacher.

The teacher / student interaction becomes a reality through a division of work and responsibilities between students and teachers. However, it is taken into account to some extent the students can set the pace of learning according to their needs and availability, following the guidelines set by the teacher.

The organization of teaching involves the active participation of students, and conducted according to the following guidelines:

The organization of the actual teaching will be based on the following guidelines:

* **Lectures** : theoretical activities conducted by the teacher, so that the theoretical support of the subject is given, highlighting the major issues, structuring them on chapters and / or sections and connecting them to each other.

* **Practice Classes** : The teacher deals with problems or study cases to complement the theoretical classes with practical issues.

* **Seminars** : The total group of lectures or practical classes may or may not be divided into smaller groups, as appropriate. They will be used to analyze cases, solve problems, etc. Unlike what happens with the practical classes, the teacher is not the protagonist. He just listens, guides, clarifies, assesses, evaluates. We want to encourage the student participation and try to make continuous assessment easier and learn about the learning performance.

* **Lab Practice work** : The total group of master classes will be divided into several groups according to the number of students enrolled, but never more than 20 students, so that smaller groups are formed. The students will carry out assemblies, measurements, simulations, etc. The participation of the student is important and also the continuous assessment and the learning performance.

* **Group tutorials** : Scheduled tracking learning activities in which the teacher meets with a group of students to guide their autonomous learning work and consultancy of targeted work or tasks that require a very high degree of advice from the teacher.

* **Individual tutorials** : These are made on a one-to-one basis, at the department. They aim to help solving problems that are the students might have, particularly those which for several reasons cannot attend group tutorials or need a more personalized attention. These tutorials may be face-to-face or virtual.

5.2.Learning activities

The program that the student is offered to achieve the expected results includes the following activities...

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Face-to-face Generic Activities :

* **Theoretical classes** : the concepts and procedures of the subject will be developed and practical examples as support will be developed

- **Practical classes** : problems and case studies will be done to complement the theoretical concepts studied

* **Lab practice work:** Students will be divided into several groups not bigger than 20 students being monitored by the teacher.

● **Defense and presentation of topics** : on the particular contents assigned

to each group of students, belonging to Block 4

Non-class Generic Activities:

* Study and assimilation of the concepts and procedures outlined in the laboratory.

* Understanding and assimilation of the problems and practical cases solved in practical lessons.

* Organization of seminars, suggested problems solving, etc.

* Organization of laboratory practice work, development of scripts and reports.

* Production of written continuous assessment tests and final exams

Monitored autonomous activities : Although they will rather have a mixed nature between face-to-face and non-class tuition they have been considered separately and will be focused mainly to seminars and tutorials under the supervision of the teacher.

Reinforcement activities : With a remarkable non-class nature, through a virtual learning portal (Moodle, e-mail) several activities that reinforce the basic contents of the subject will be carried out. These activities can be customized or not, and will be monitored through the portal.

Scheduling of a teaching week: The course is designed in the Degree verification document with a low experimental load, so the 10 hours per week are distributed as follows:

* Theoretical and practical classes: 3 hours per week (blocks 1, 2 and 3)

5 hours per week (block 4)

* Labs: 1 hour per week

* Other activities: 6 hours per week (blocks 1, 2 and 3)

4 hours per week (block 4)

Global Schedule distribution: The subject consists of 6 ECTS credits, which represents 150 hours of the student work in the subject during the semester, 10 hours per week for 15 teaching weeks, distributed as follows:

* 48 hours in the classroom: 60% presentation of concepts and 40% of problem solving-type, at a rate of 3 hours per week, except for weeks with control tests when one hour will be reduced and in the last weeks when there will be a two hour increase.

* 15 hours of supervised laboratory practice: Weeks 1 to 15 in sessions of 1 hour.

* 15 hours of seminars and group tutorials: to complete the practical activities of each block and particularly for the preparation of block 4 (see table calendar in activities and resources)

* 66 hours of personal study: a rate of 4 hours in each 15-week semester, to develop work, exercising, studying theory, etc ... (in the table below the recommended distribution schedule is set)

* 6 hours of testing (3 tests in 2 hours), to be done in weeks: 3rd, 7th and 12th.

5.3.Program

Essential contents of the subjects for achieving the learning outcomes.

Theoretical contents.

The theoretical contents are based on four blocks (numbers 1-4) preceded by an introductory block 0 to Digital Electronic Technology. The choice of the contents of the blocks has been made seeking the clarification of the final goal, so that with the gathering of contents, the student achieves a structured knowledge, easily understandable by Mechatronics Engineers.

Each of the blocks consists of units, with a temporary assignment of one or two weeks of the course, these units gather the contents needed to the acquisition of preset learning outcomes, according to the following relationship

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Block 0: INTRODUCTION

- Overview of digital technology. Components, functions,
- Manufacturing techniques, levels of integration.
- Conceptual maps

Block 1: INTRODUCTION TO TECHNICAL DIGITAL

1. Basic elements of digital technology

* Numbering Systems

* Binary Codes

* Boolean algebra

* Logic gates

2. Digital Integrated Circuits

* Technical and manufacturing processes

* Digital Technologies and families. Interface

* Technical parameters. logic levels, delays, speed, etc.

3. Methods of combinational logic design

* Logic gates: Methods of Karnaugh.

* Integrated Circuits with function logic gate

* Integrated Circuits with exclusive-OR function

* Function O-Exclusive: Venn Boards

* Design and implementation of applications

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Block 2: ANALYSIS AND DESIGN OF LOGIC CIRCUITS COMBINATIONAL

4. Coders and Decoders

* Integrated Circuits CODEC functions

* Decoder: summations and logical positive-negative

* Design and implementation of applications

* Decoders BCD to 7 segments and ASCII

5. Multiplexers and demultiplexers

* Integrated Circuits multiplexer-demultiplexer functions

* Multiplexers: Allocation Tables states

* Design and implementation of applications

6. Other functions Combinational

* Comparators

* Arithmetic Circuits

* Parity Generators-Detectors

Block 3: ANALYSIS AND DESIGN OF SEQUENTIAL LOGIC CIRCUITS

7. Basic Bistables and synchronized

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* Flip-flop RS and other performances

* Maps and status symbols

* Design and schedules

* Synchronisation levels and flanks

* JK / Master-Slave

* D / Edge-Triggered

* Behaviors mode T

8. Digital counters and digital records

* Asynchronous and synchronous counters Counters

* Modes account. Design processes

* Counters sequencers. universal counter

* Records Storage and displacement

* serial / parallel inputs. Outputs series / parallel

* Scroll left / right.

* Universal Register. Accumulator register.

9. P.L.D matrix Architectures and A.S.I.C.

* Programmable Logic Devices (PLD)

* Evolution of PLD: PAL, PLA, GAL, Macro-cells, ...

* FPGA, LCA-RAM, EPLD, CPLD, ...

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* Development processes with PLD

* Hardware description languages (HDL)

* Application Specific Integrated Circuits (ASIC)

* Gate-Array, Standard-Cell, Full-Custom

Block 4 : DIGITAL DEVICES HIGHLY INTEGRATED

10. Semiconducting Memories

* Architecture: cells, addressing

* Volatile Memory: Static and Dynamic

* Nonvolatile Memory: ROM to Flash

11. Converters A / D and D / A

* Direct Digital Converters

* Digital Converters fed back

* Digital Analog Converters

12. Computer Systems

* Microcomputers

* Microprocessors

* Programmable logic controllers (PLC)

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Practical contents.

Each unit presented in the previous sections has associated practices, both/either through practical cases, interpretation and/or real or simulated assemblies leading to the achievement of results and their analysis and interpretation. As the units are covered, practice tasks will be suggested, preferably in the classroom and also through the Moodle Platform.

5.4.Planning and scheduling

5.5.Bibliography and recomended resources

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