29819 - Digital Electronics

Información del Plan Docente

Academic Year	2016/17
Academic center	110 - Escuela de Ingeniería y Arquitectura 326 - Escuela Universitaria Politécnica de Teruel
Degree	440 - Bachelor's Degree in Electronic and Automatic Engineering 444 - Bachelor's Degree in Electronic and Automatic Engineering
ECTS	6.0
Course	2
Period	Second semester
Subject Type	Compulsory
Module	---

1.Basic info

1.1.Recommendations to take this course

1.2.Activities and key dates for the course

2.Initiation

2.1.Learning outcomes that define the subject

2.2.Introduction

3.Context and competences

3.1.Goals

3.2.Context and meaning of the subject in the degree

3.3.Competences

3.4.Importance of learning outcomes

4.Evaluation

IN ZARAGOZA

Course grading

The course is evaluated according to the following items:

- Mid-term exam (CP)

29819 - Digital Electronics

- Final exam (CE)

- Laboratory classes (CL)

The final grade (CG) is obtained using the following equations:

CGaux=max{0.3xCP + 0.6xCE + 0.1xCL, 0.9xCE + 0.1xCL}

CG = CGaux if CL>4, otherwise CG=min{4, CGaux}

IN TERUEL

The course is graded followin g these rules:

COURSE PERIOD:

Laboratory sessions: (grade *CL* 0 to 10). It accounts for a 25% of the final grade. A minimum of 4 is required to pass the subject.

OFFICIAL CALL (EXAM PERIOD):

- **Written exam (theory and problems)** : grade *CT* 0 to 10 puntos. It accounts for the 75% of the final grade. A minimum of 4 is required to pass the subject.
- **Laboratory exam** : grade *CL* 0 to 10 puntos. It accounts for the 25% of the final grade. A minimum of 4 is required to pass the subject. This exam is compulsory only for those students who did not obtain a minimum of 4 in *CL* during the course period.

TOTAL GRADE: If the student has a grade of at least 4 in *CL* and *CT* , the final grade will be obtained from CL and CT with the weights indicated above. Otherwise, the student will fail and the grade will be obtained as the minimum of these two values: 4 and 0.75xCT+0.25xCL.

5.Activities and resources

5.1.General methodological presentation

The course includes lectures, exercises and laboratory sessions.

5.2.Learning activities

29819 - Digital Electronics

In EINA, Zaragoza:

Course structure : 2 hours of lectures and 1 hour of problems each week, plus six 2.5-hour laboratory sessions, one per week for selected weeks throughout the semester. Students will work in groups of two in the laboratory, and the lab reports will be prepared in groups too.

In EUP, Teruel:

Course structure : 2 hours of lectures and 1 hour of problems each week, plus several laboratory sessions (about 15 hours in total), acoording to the schedule of the EUPT. Students will work in groups of two in the laboratory, and the lab reports will be prepared in groups too.

5.3.Program

In EINA, Zaragoza:

Lecture outline :

* Fundamentals of Digital Electronics.

* Combinational Logic Circuits.

* Sequential Logic Circuits.

* Technologies of Digital Circuits.

Brief description of laboratory sessions

* P1: Fire-alarm circuit design.

* P2: BCD to Seven-segment decoder design.

* P3: Liquid level indicator circuit design.

* P4: 2-digit BCD counter design using an FPGA.

* P5: State-machine design using an FPGA.

* P6: PWM generation to control a servo motor using an FPGA.

In EUP Teruel:

Syllabus:

- Fundamentals of logic systems
- Characteristics of digital circuits
- Combinational logic
- Introduction to VHDL
- Codification and error detection
- Lacthes and registers
- Programmable Logic Devices
- Sequential logic
- Counters and its applications

Laboratory sessions:

- Properties of CMOS circuits
- Combinational circuits in VHDL
- Monostables and astables with the 555
- Sequential circuits in VHDL
- Counters in VHDL (I)
- Counters in VHDL (II)
- Design of complex systems

5.4.Planning and scheduling

Lectures, problem and laboratory sessions are held according to schedule set by the EINA (schedules available on their website) in Zaragoza or EUPT in Teruel.

5.5.Bibliography and recomended resources

All course materials are posted on Moodle.

Moodle will be also used to communicate announcements and is where students will submit laboratory reports.

Basic references:

- J.I. Artigas, L.A. Barragán, C. Orrite, I. Urriza, "Electrónica Digital. Aplicaciones y problemas con VHDL", Prentice-Hall, 2002.
- J. F. Wakerly, "Digital Design. Principles and Practices", 4ª Edición, Pearson Education Inc., 2006.

Other references:

- T. L. Floyd "Fundamentos de Sistemas Digitales", 9º Edición, Pearson Educación, 2006.
- J.I. Artigas, L.A. Barragán, C. Orrite, "Aplicaciones y Problemas de Electrónica Digital", Prensas Universitarias de Zaragoza. Colección Textos Docentes, 2007.

29819 - Digital Electronics

- T. Pollán, "Electrónica Digital", Prensas Universitarias de Zaragoza. Colección Textos Docentes, 3ª edición, 2007. Disponible en http://diec.cps.unizar.es/~tpollan/
- Pollán Santamaría, Tomás. Electrónica digital. I, Sistemas combinacionales / Tomás Pollán Santamaría. 3ª ed. Zaragoza : Prensas Universitarias de Zaragoza, 2007
- Pollán Santamaría, Tomás. Electrónica digital. II, Sistemas secuenciales / Tomás Pollán Santamaría. 3ª ed. Zaragoza : Prensas Universitarias de Zaragoza, 2007
- Pollán Santamaría, Tomás. Electrónica digital. III, Microelectrónica / Tomás Pollán Santamaría. 3ª ed. Zaragoza : Prensas Universitarias de Zaragoza, 2007
- Pollán Santamaría, Tomás. Electrónica digital. IV, Tecnología CMOS / Tomás Pollán Santamaría. 3ª ed. Zaragoza : Prensas Universitarias de Zaragoza, 2007
- Guía de usuario de la placa de FPGA "Spartan-3 Board" utilizada en el laboratorio.
- Catálogos de circuitos integrados de los diversos fabricantes (web de los fabricantes).