60924 - Advanced digital systems

Información del Plan Docente

Academic Year	2016/17
Academic center	110 - Escuela de Ingeniería y Arquitectura
Degree	533 - Master's Degree in Telecommunications Engineering
ECTS	5.0
Course	1
Period	First semester
Subject Type	Compulsory
Module	---

1.Basic info

1.1.Recommendations to take this course

1.2.Activities and key dates for the course

2.Initiation

2.1.Learning outcomes that define the subject

2.2.Introduction

3.Context and competences

3.1.Goals

3.2.Context and meaning of the subject in the degree

3.3.Competences

3.4.Importance of learning outcomes

4.Evaluation

5.Activities and resources

5.1.General methodological presentation

The candidate should after this course have an in-depth knowledge of digital integrated circuit hardware design.The emphasis is on FPGA technology, but most of the design techniques can also be applied to ASIC devices. The student should be familiar with the latest state-of-the-art system on chip (SoC) design methodologies, including high-level synthesis . Students should be able to learn the benefits and drawbacks of the various design methods for solving a problem. Through practical assignments, experience will be achieved from both using tools as well as designing their own system.

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5.2.Learning activities

This course includes a combination of lectures, laboratory assignments, and a final exam.

Lectures (25H) - Students are expected to attend all lectures, be attentive during lecture, and participate in class discussion.

Lab Assignments (25 H) - The course will include 12 lab sessions that allow students to incrementally design, implement, test, and evaluate several small communications blocks. Students are expected to work in a group of two students. It is suggested that students form a group early on and keep the same group throughout the semester.

5.3.Program

Course topics:

Advanced VHDL coding

High Level Synthesis

System on Chip design

ASIC design flow

5.4.Planning and scheduling

The schedule of the lectures and lab sessions is posted on the university website.

5.5.Bibliography and recomended resources

- Ashenden, Peter J.. VHDL-2008: just the new stuff / Peter J. Ashenden, Jim Lewis Morgan Kaufmann, 2008.
- Fingeroff, Michael. High-Level Synthesis Blue Book / Michael Fingeroff Xilibris Corporation, 2010.
- Golshan, Khosrow. Physical Design Essentials: An ASIC Design Implementation Perspective / Khosrow Golshan Springer, 2007.
- Chandrasetty, Vidram Arkalgud. VLSI Design: A Practical Guide for FPGA and ASIC Implementations / Vikram Arkalgud Chandrasetty, Springer, 2011.