Anexos

1. Hardware y Firmware

1.1. Electrodos

1.1.1. Electromiografía de superficie

La SEMG tiene la peculiaridad de que los registros obtenidos muestran actividad poblacional de las unidades motoras, esto es debido a que los electrodos, al estar en la superficie del musculo, no son capaces de captar la señal de una sola unidad motora, sino que por el contrario, captan la información de varias UMs [1]. Es por esta razón que esta técnica no es muy utilizada para diagnósticos médicos muy precisos. Por otro lado el uso de los electrodos superficiales es mucho más adecuado para el estudio del comportamiento promedio de la actividad eléctrica de un musculo o grupo de músculos, lo cual es muy utilizado para detectar fatiga muscular.

1.1.1.1. Electrodos superficiales

Estos electrodos son principalmente superficies de metal, sin embargo, debido al estar en contacto directo con la piel hay que tomar ciertas consideraciones: la piel es un tejido conductivo cuyo material intracelular y extracelular está compuesto de soluciones electrolíticas, en la cual la corriente es transportada por iones, mientras que el metal es un material altamente conductivo, en el cual la corriente es transportada por electrones, en consecuencia, la interfaz electrodo piel es en sí muy ruidosa [2].
Existen varios tipos de electrodos de superficie, estos se dividen principalmente en dos grandes grupos: electrodos secos y electrodos húmedos. Los electrodos húmedos son aquellos en los que entre la placa de metal y la piel se encuentra una substancia electrolítica o gel conductor, esto se hace con el fin de minimizar el ruido intrínseco que se genera entre el contacto de la piel y el metal, este gel conductor mejora la conductividad y el flujo de la corriente.

1.1.2. Electromiografía invasiva

Los músculos del cuerpo están conformados por varias motoneuronas, las cuales inervan una zona específica de las fibras musculares; la electromiografía invasiva se encarga de obtener el registro del potencial generado por una unidad motora en particular, es una técnica muy útil para diversas especialidades, sobretodo en rehabilitación, medicina interna o traumatología. Sirve para localizar el área lesionada, concretando si es un problema de una mano, brazo o pierna, o si es algo más difuso y definiendo si la lesión es de un musculo, nervio, tronco o raíz nerviosa, o más de uno.

1.1.2.1. Electrodos invasivos

Para medir los potenciales generados por las unidades motoras, la electromiografía invasiva hace uso de electrodos de aguja. Un electrodo de aguja consiste en una delgada aguja de metal la cual es insertada en el musculo directamente. La figura 71 muestra distintos tipos de electrodos de aguja [2].

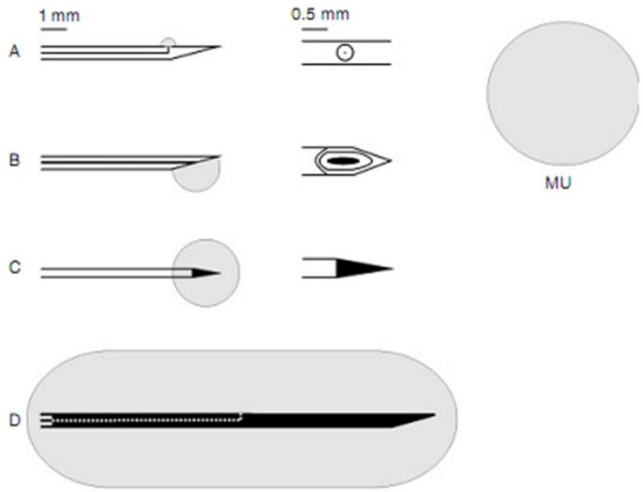


Figura 71. A) Electrodos de fibra simple, B) Electrodo de aguja concéntrico, C) Electrodo mono polar, D) Macro electrodo

La amplitud de la señal registrada por los electrodos de aguja depende del area de registro que ocupan, asi como tambien de la distancia del electrodo a la fuente de la señal (UM) [1]. Siendo la amplitud mas grande mientras el electrodo esta mas cerca de la unidad motora; la amplitud disminuye mientras mas lejano este el electrodo de la fuente.
Debido a que la inserción de los electrodos de aguja es bastante dolorosa y además requiere la supervisión médica, la electromiografía invasiva se limita a usos clínicos y de carácter medico, principalmente es usada para diagnosticar enfermedades motoras, esta caracteristica hace difícil su uso en investigaciones para el desarrollo de protesis ya que muchas personas consideran muy molesto el procedimiento de inserción.

1.1.3. Disposición de los electrodos, forma y tamaño

Uno de los puntos más importantes en el EMG de superficie es la localización de los electrodos. Debido a esto, se originó una iniciativa europea para tratar de estandarizar estos factores: localización, tamaño y forma de los electrodos. Es así que en 1996 surge el SENIAM (Surface Electromiography for Noninvasive Assessment of Muscles) [5] para tratar de dar ciertas recomendaciones en cuanto a estas variables.
La distancia inter-electrodo es definida como la distancia centro a centro del área conductiva de los electrodos.
La forma del electrodo es definida como el área conductora que entra en contacto con la piel, la mayoría de las referencias bibliográficas coincide en la forma circular como la más utilizada.
Las medidas preferidas del electrodo usado en muchas de las publicaciones suele ser de 10mm de diámetro.

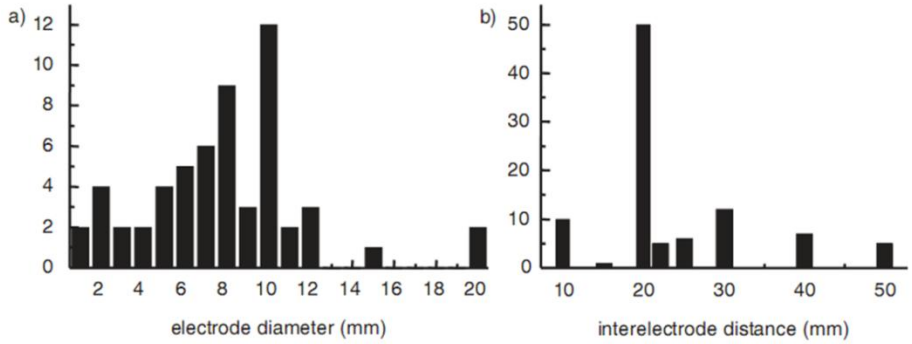


Figura 72. a) Histograma del diámetro del electrodo. b) Histograma de la distancia inter-electrodo

El SENIAM proporciona una serie de pasos antes de realizar las mediciones de SEMG:

1. Selección de los electrodos para SEMG.
2. Preparación de la piel, usando algún gel conductor o limpiando la zona con alcohol.
3. Posicionar al paciente en la postura inicial, dicha postura puede ir variando dependiendo del estudio a realizar.
4. Determinar la localización de los electrodos.
5. Fijar los electrodos.
6. Finalmente testear las conexiones.

Estas medidas son bien merecidas, ya que una medición de SEMG es bastante variable y es muy difícil repetir experimentos y obtener los mismos valores. Uno de los factores que interviene es que la amplitud de la señal de SEMG aumenta en relación al desplazamiento longitudinal del electrodo sobre el músculo.

1.2. Opciones en el diseño

1.2.1. Tensión Bipolar:

Debido a que la señal electromiográfica presenta amplitudes en el rango de 1mV, es necesario hacer una serie de amplificaciones. La cadena de ganancias se muestra en la Figura 73. Dicha cadena de ganancia deberá tener una amplificación de unos 1500 consiguiendo de esta forma una tensión de 1,5V. Para lograr las amplificaciones, se usan amplificadores operacionales en configuración no inversora.

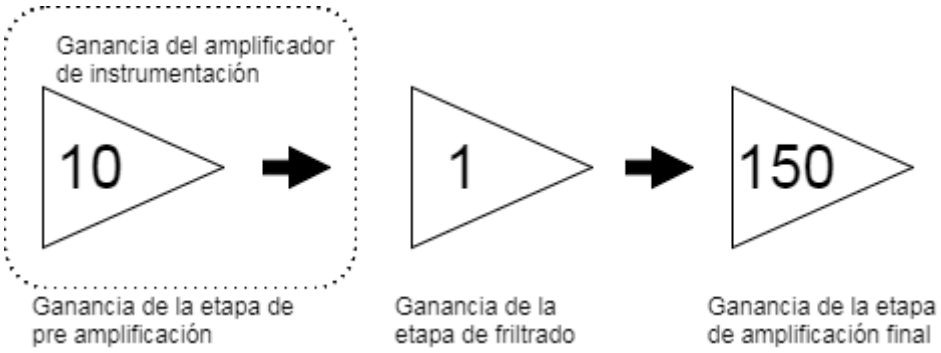


Figura 73. Diagrama del proceso de amplificación en cascada del sistema

Un punto importante en el diseño de un prototipo con tensión bipolar es el uso de dos fuentes de alimentación, de ahí el nombre de "fuente bipolar"; esta característica tiene ciertas desventajas, y la más evidente es el uso de dos baterías, esto se debe a las características de los circuitos integrados usados, ya que estos no fueron fabricados para trabajar a niveles de voltaje más bajos de 5V.

1.2.2. Tensión Unipolar

Uno de los cambios más significativos en el diseño de un prototipo LVTTL con tensión unipolar respecto al bipolar es el uso de una sola fuente de alimentación, la cual es de 3.3V, de ahí el nombre LVTTL (Low Voltage Transistor–Transistor Logic). Debido a que los potenciales de EMG presentan componentes positivos y negativos, es necesario manejar dos niveles de tensión, uno más positivo y otro menos positivo. Por este motivo se implementó una referencia o "tierra virtual". Opciones para la realización de dicha "tierra virtual":

1º.Mediante un divisor resistivo y un AO con una configuración como seguidor de tensión.

2º.Mediante un zener regulable.

Esta "tierra virtual" tendrá el valor de la mitad de la fuente de alimentación de 3.3V y es sobre esta referencia de voltaje que estará montada la señal de EMG.

Un problema que hay que considerar es el consumo y la vida útil de la fuente de alimentación que se usará para alimentar al sistema. Al trabajar con baterías se deben de tener en cuenta algunos aspectos, por ejemplo se debe de mantener un voltaje en la alimentación lo más invariante que se pueda, esto se debe a que el convertidor A/D tomará como referencia de la conversión los valores de la fuente de alimentación y si estos varían con el tiempo, se tendrá un dato erróneo al finalizar la conversión. Además se incorporará un circuito para la recarga de dicha batería mediante conexión USB tipo mini B.

1.3. Etapa analógica

1.3.1. Filtro paso bajo de segundo orden

Las características más relevantes de la estructura de Sallen-Key son [14]:

Simplicidad: al estar formada por un número mínimo de componentes pasivos.

Versatilidad: al poderse adaptar a todas las situaciones posibles, y con la posibilidad de amplificación. La red de realimentación negativa, constituida por R_3-R_4, propicia la estabilidad y la opción amplificadora, mientras que la red de realimentación positiva, integrada por R_1-C_1-R_2-C_2, realiza la función selectiva a la frecuencia característica del filtro, aunque debe garantizarse, en cualquier circunstancia, la ineludible condición de estabilidad.

Del análisis de la dependencia del parámetro δ, se deduce que, para facilitar el proceso de diseño sin perder versatilidad, pueden considerarse iguales las resistencias y con una relación c las capacidades, con lo cual:

$$R_1 = R_2 = R\,; \frac{C_2}{C_1} = c : C_1 = C\,, C_2 = cC \rightarrow\ \omega_n = \frac{1}{\sqrt{c}RC} = 2\pi f_n\,;\ \delta = \frac{(1-K)+2c}{2\sqrt{c}}$$

Se ha elegido que el filtro tendrá una ganancia unidad, por lo que:

$$K = 1 + \frac{R_3}{R_4} = 1 \rightarrow R_3 = 0\,; f_n = \frac{1}{2\pi\sqrt{c}RC}\,, siendo\ c = \delta^2$$

Para la elección del valor de δ se tiene en cuenta la sobreoscilación, la siguiente gráfica muestra la relación de este valor δ y la ganancia donde se puede apreciar si existe o no sobreoscilación.

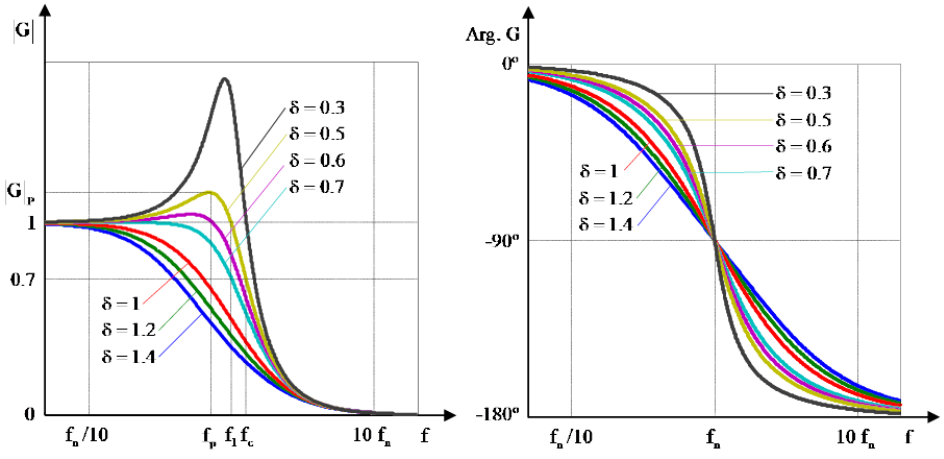


Figura 74. Efecto de δ en el filtro paso bajo

1.3.2. Filtro paso bajo de segundo orden

Del análisis de la dependencia del parámetro δ [14], se deduce que, para facilitar el proceso de diseño sin perder versatilidad, pueden considerarse iguales los condensadores y con una relación r las resistencias, con lo cual:

$$C_1 = C_2 = C\ ; \frac{R_2}{R_1} = r : R_1 = R\ , R_2 = rR \rightarrow\ f_n = \frac{1}{2\pi\sqrt{r}RC}$$
$$\delta = \frac{r(1-K)+2}{2\sqrt{r}}; para\ K = 1 \rightarrow\ \delta = \frac{1}{\sqrt{r}}$$

De forma análoga como se hizo con el filtro paso bajo de segundo orden, existe la relación de δ con la ganancia:

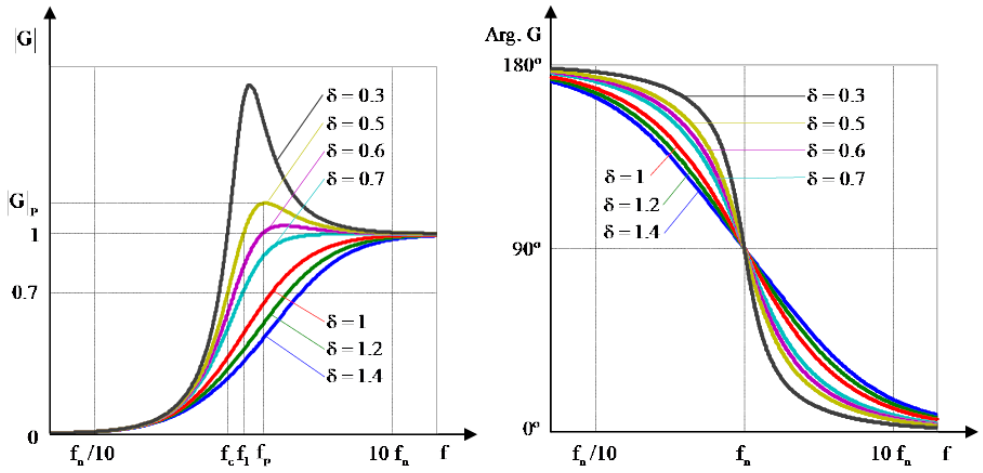


Figura 75. Efecto de δ en el filtro paso alto

1.3.3. Filtro Notch

Con la combinación de estas ecuaciones se obtiene la función de transferencia [6]:

$$G(s) = \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{(CR)^2} + s^2}{\frac{1}{(CR)^2} + \frac{2}{CR}s + s^2}$$

Donde:

$$\omega_o = \frac{1}{RC}$$

1.4. Simulaciones de las etapas analógicas

Para las simulaciones de los filtros utilizados en el prototipo se ha usado el programa OrCaD Capture CIS v16.3.

1.4.1. Filtro paso alto de segundo orden a 20Hz

Para el filtro paso alto de segundo orden se ha simulado el circuito electrónico del apartado 2.6 de la memoria.

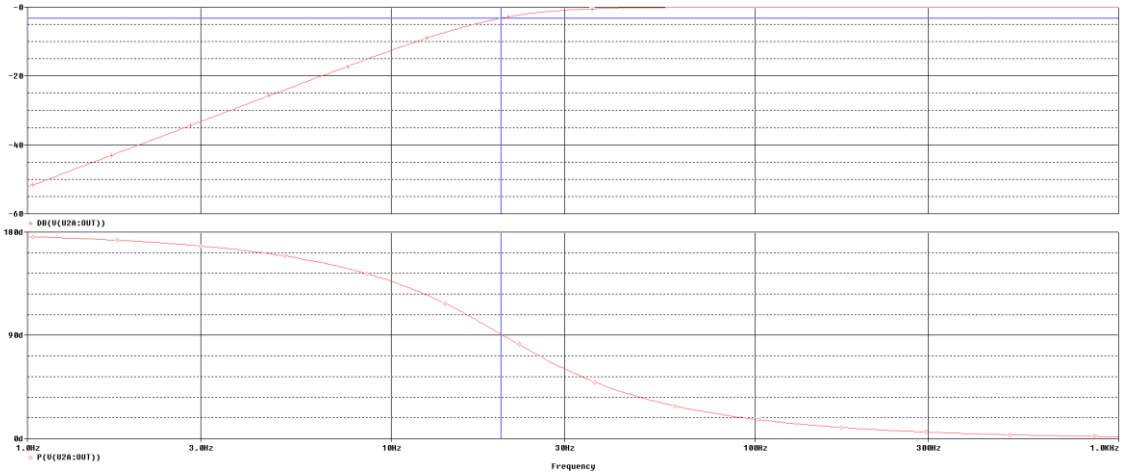


Figura 76. Filtro paso alto a 20Hz de segundo orden

Cursor en la frecuencia de corte:

Trace	Cursor1
X Value	20.015
P(V(U2A:OUT))	91.050
DB(V(U2A:OUT))	-3.2049

Figura 77. Datos en la frecuencia de corte del filtro paso alto de segundo orden

Se puede apreciar que para la frecuencia de corte de 20Hz se tienen los -3dB y un desfase de 90º.

Comprobación de la caída en dB en una década:

Trace	Cursor1	Cursor2
X Value	1.0000	10.000
P(V(U2A:OUT))	175.965	137.081
DB(V(U2A:OUT))	-52.282	-12.567

Figura 78. Caída en dB en una década del filtro paso alto de segundo orden

Se puede observar en la fila de los dB como existe una caída de 40db por década, característico de un filtro de segundo orden.

1.4.2. Filtro paso bajo de primer y segundo orden a 500Hz

1er orden:

Para el filtro paso bajo de primer orden se ha simulado el circuito electrónico del apartado 2.6 de la memoria.

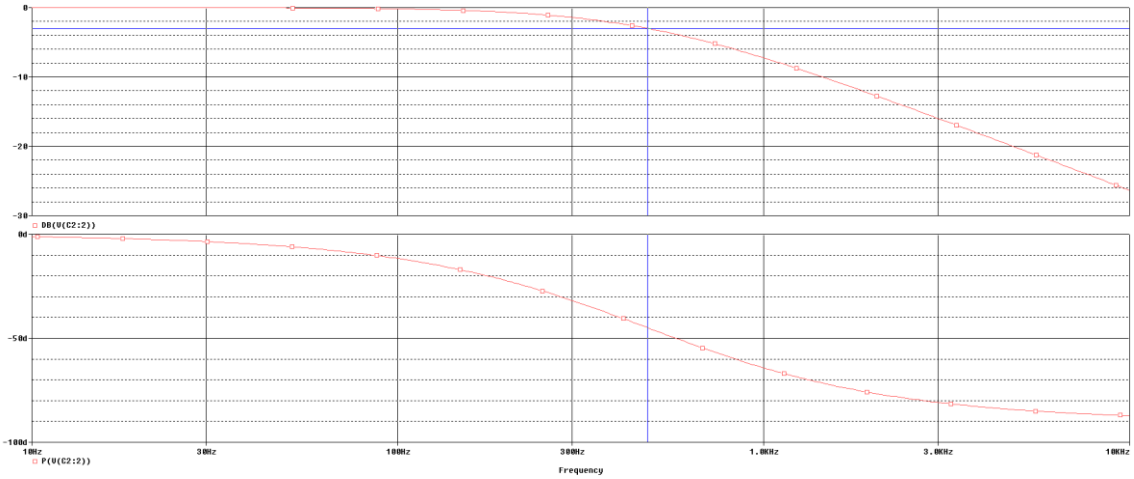


Figura 79. Filtro paso bajo a 500Hz de primer orden

Cursor en la frecuencia de corte:

Trace	Cursor1	Trace	Cursor1
X Value	500.408	X Value	481.318
P(V(C2:2))	-46.056	P(V(C2:2))	-44.942
DB(V(C2:2))	-3.1735	DB(V(C2:2))	-3.0018

Figura 80. Datos en la frecuencia de corte del filtro paso bajo de primer orden

Como se puede observar la frecuencia de corte realmente está en 480Hz que es la frecuencia donde existe una caída de -3dB, esto es debido a la diferencia del valor exacto en la resistencia usada, ya que estamos limitados con valores comerciales de dicho componente, además de un desfase de -45º.

Comprobación de la caída en dB en una década:

Trace	Cursor1	Cursor2
X Value	1.0000K	10.000K
P(V(C2:2))	-64.253	-87.239
DB(V(C2:2))	-7.2421	-26.344

Figura 81. Caída en dB en una década del filtro paso bajo de primer orden

Se puede contemplar en la fila de los dB como existe una caída de 20db por década, característico de un filtro de primer orden.

2º orden

Para el filtro paso bajo de segundo orden se ha simulado el circuito electrónico del apartado 2.6 de la memoria.

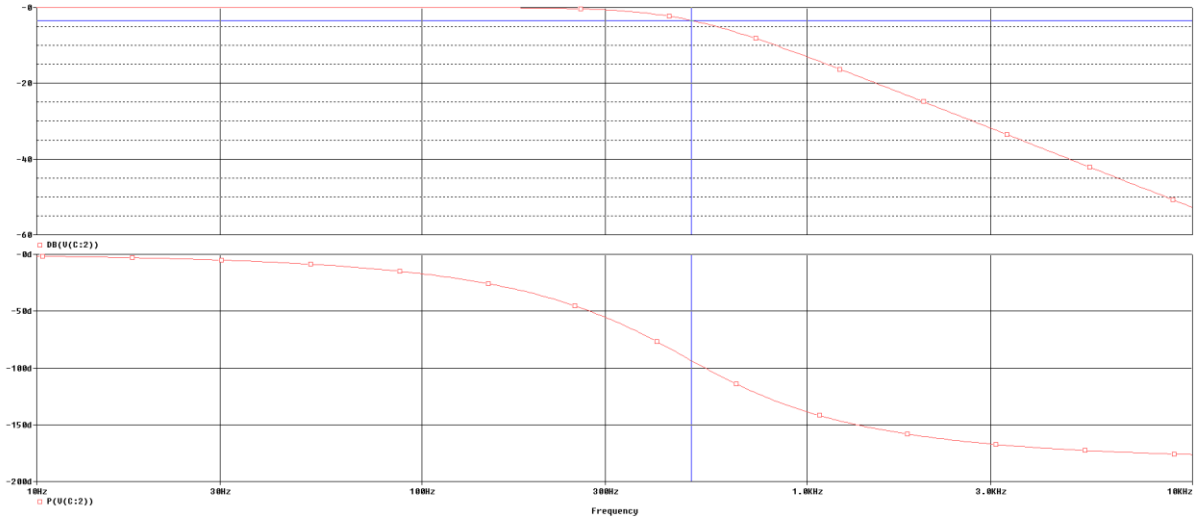


Figura 82. Filtro paso bajo a 500Hz de segundo orden

Cursor en la frecuencia de corte:

Trace	Cursor1	Trace	Cursor1
X Value	500.408	X Value	479.450
P(V(C:2))	-93.571	P(V(C:2))	-89.969
DB(V(C:2))	-3.4098	DB(V(C:2))	-3.0062

Figura 83. Datos en la frecuencia de corte del filtro paso bajo de segundo orden

En semejanza con lo que se ha mencionado en el apartado anterior, en éste caso también ocurre que la frecuencia de corte real está en los 480Hz y con un desfase en este caso de -90º.

Comprobación de la caída en dB en una década:

Trace	Cursor1	Cursor2
X Value	1.0000K	10.000K
P(V(C:2))	-138.710	-176.315
DB(V(C:2))	-13.015	-52.793

Figura 84. Caída en dB en una década del filtro paso bajo de segundo orden

Se puede contemplar en la fila de los dB como existe una caída de 40db por década, característico de un filtro de primer orden.

1.4.3. Comparación entre ambos órdenes del filtro paso bajo

En este caso se superponen ambos filtros, dando como resultado la figura 79.

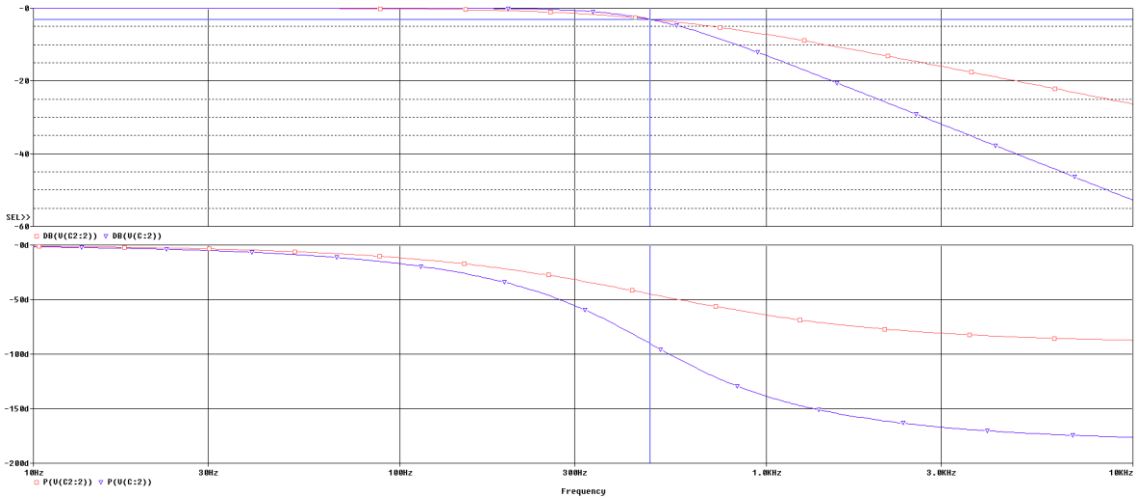


Figura 85. Comparación entre diferentes órdenes en el filtro paso bajo

Cursor en la frecuencia de corte:

Trace	Cursor1	Trace	Cursor1
X Value	500.408	X Value	481.318
P(V(C2:2))	-46.056	P(V(C2:2))	-44.942
P(V(C:2))	-93.571	P(V(C:2))	-90.422
DB(V(C2:2))	-3.1735	DB(V(C2:2))	-3.0018
DB(V(C:2))	-3.4098	DB(V(C:2))	-3.0560

Figura 86. Datos en la frecuencia de corte del filtro paso bajo

Comprobación de la caída en dB en una década:

Trace	Cursor1	Cursor2
X Value	1.0000K	10.000K
P(V(C2:2))	-64.253	-87.239
P(V(C:2))	-138.710	-176.315
DB(V(C2:2))	-7.2421	-26.344
DB(V(C:2))	-13.015	-52.793

Figura 87. Caída en dB en una década del filtro paso bajo de primer y segundo orden

Una elección de un filtro de mayor orden siempre será más beneficiosa, pero es más caro ya que se requiere de una mayor cantidad de componentes para su implementación. En el prototipo alfa se han incluido ambos para su comparación.
Para el prototipo beta se implementará el filtro paso bajo de primer orden, como se puede apreciar en la figura 6 la potencia de la señal EMG a éstas frecuencias es muy baja, por lo que no es crítico el uso de un filtro con un orden alto.

1.4.4. Filtro notch

Para el filtro notch se ha simulado el circuito electrónico del apartado 2.6 de la memoria.

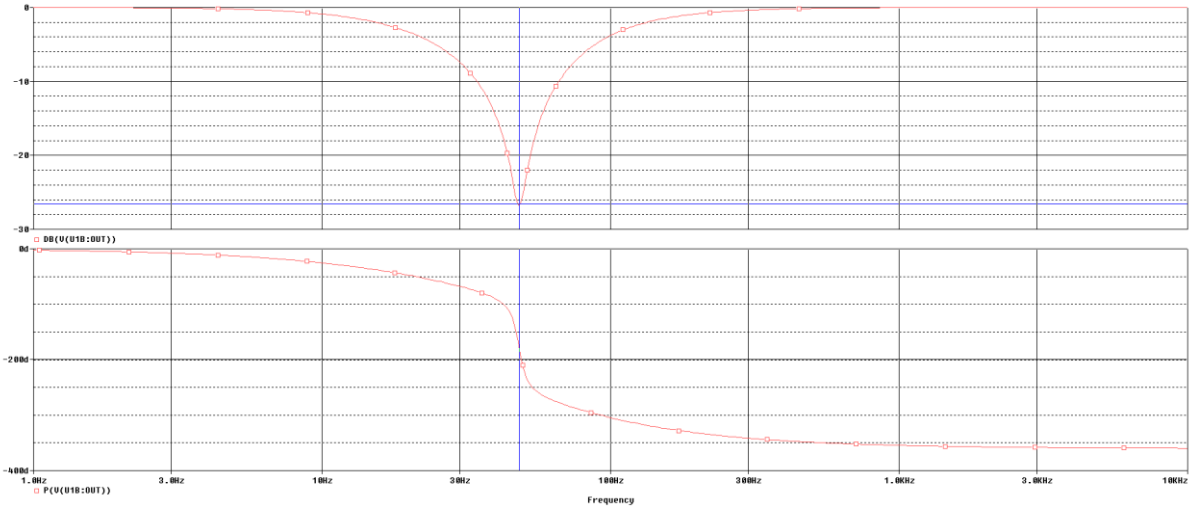


Figura 88. Frecuencia de aplicación del filtro Notch

Frecuencia de aplicación del filtro notch:

Trace	Cursor1
X Value	48.382
P(V(U1B:OUT))	-181.055
DB(V(U1B:OUT))	-26.612

Figura 89. Datos en la frecuencia de aplicación del filtro Notch

Frecuencias de corte de aplicación en el filtro notch:

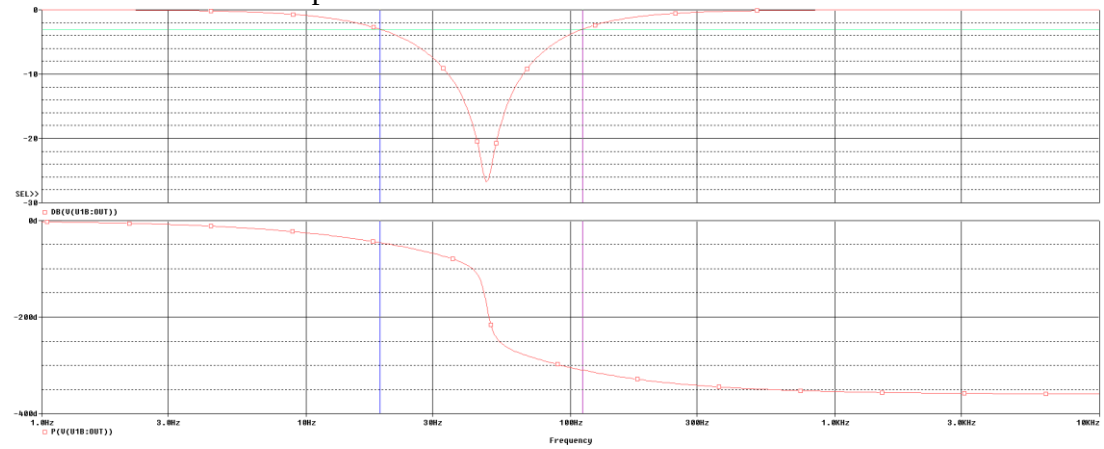


Figura 90. Frecuencias de corte del filtro Notch

Trace	Cursor1	Cursor2
X Value	19.023	110.929
P(V(U1B:OUT))	-45.739	-309.927
DB(V(U1B:OUT))	-3.0263	-3.0143

Figura 91. Datos en las frecuencias de corte del filtro Notch

La implementación o no del filtro notch depende del posible ruido electrónico ambiental que se tenga, ya que en la frecuencia de aplicación del filtro notch se tiene una potencia de la señal EMG muy alta. Por lo que para el prototipo se ha decidido poder puentear o no este filtro de forma manual.

1.4.5. Toda la etapa analógica con y sin filtro notch

Se ha simulado la etapa de acondicionamiento de la señal EMG con una ganancia de 760 y 2500 dando los siguientes resultados:

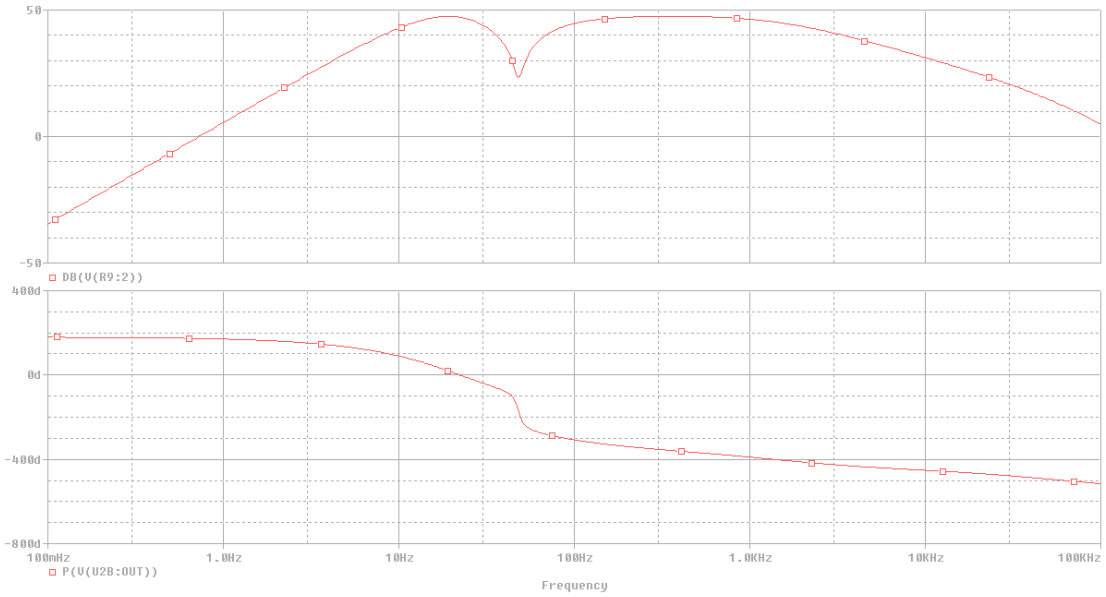


Figura 92. Etapa analógica con filtro Notch con ganancia de 760

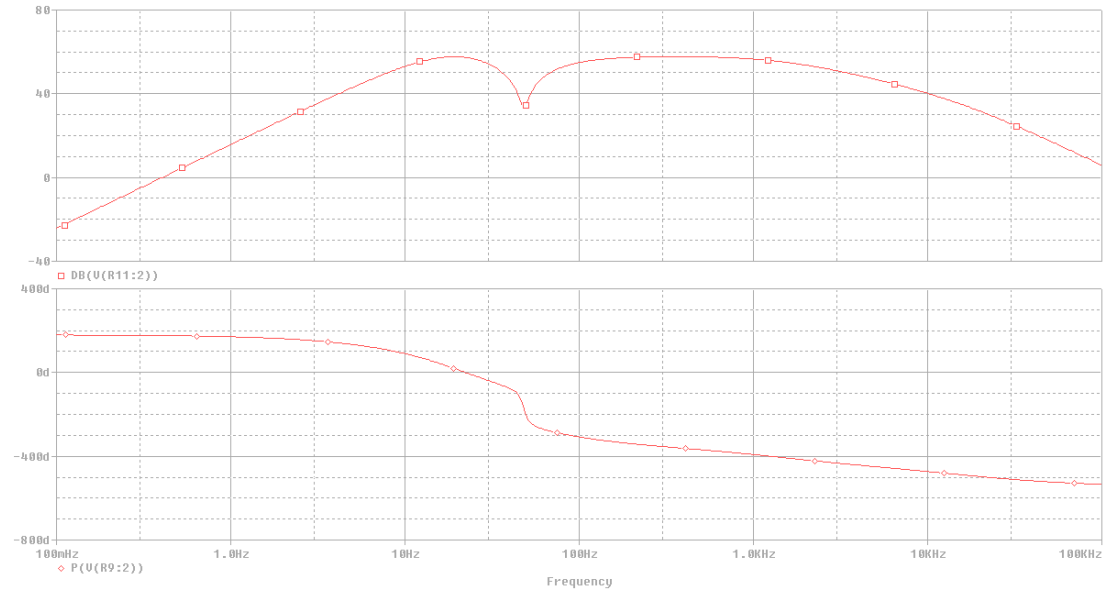


Figura 93. Etapa analógica con filtro Notch con ganancia de 2500

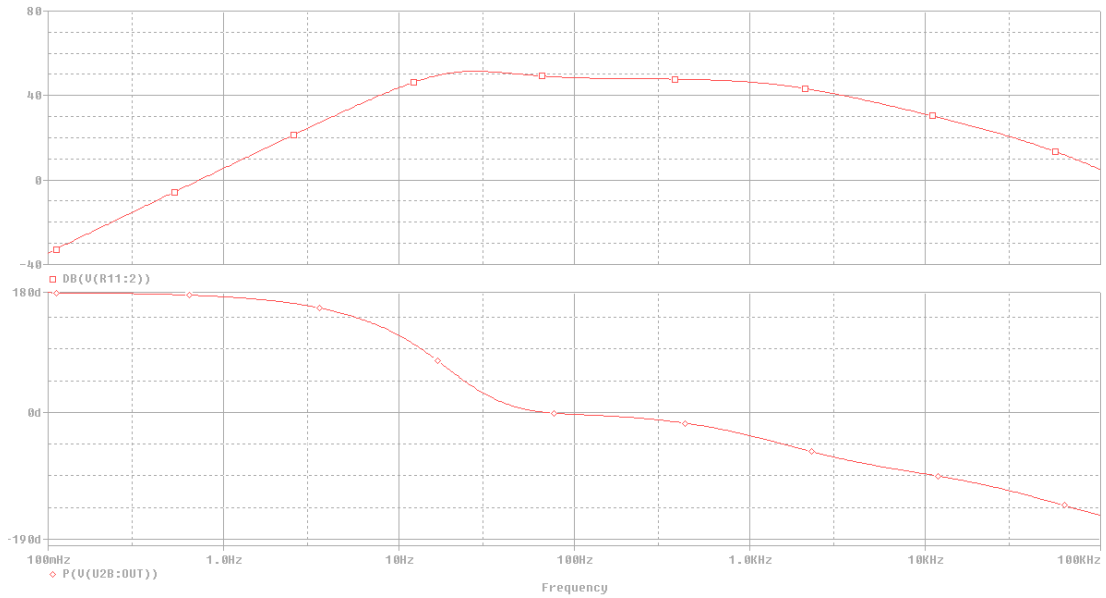


Figura 94. Etapa analógica sin filtro Notch con ganancia de 760

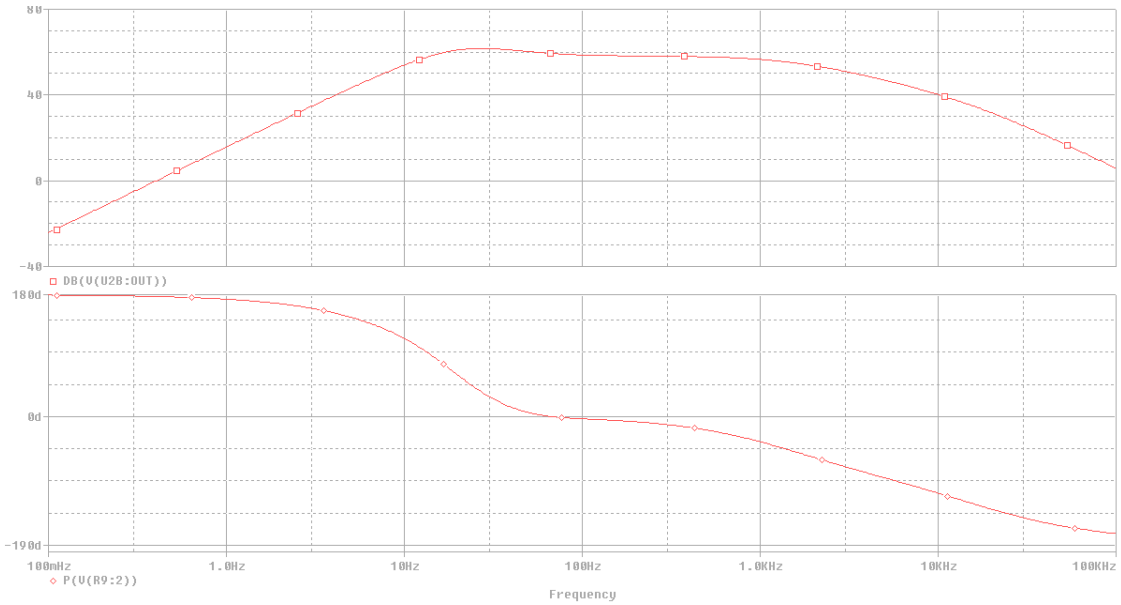
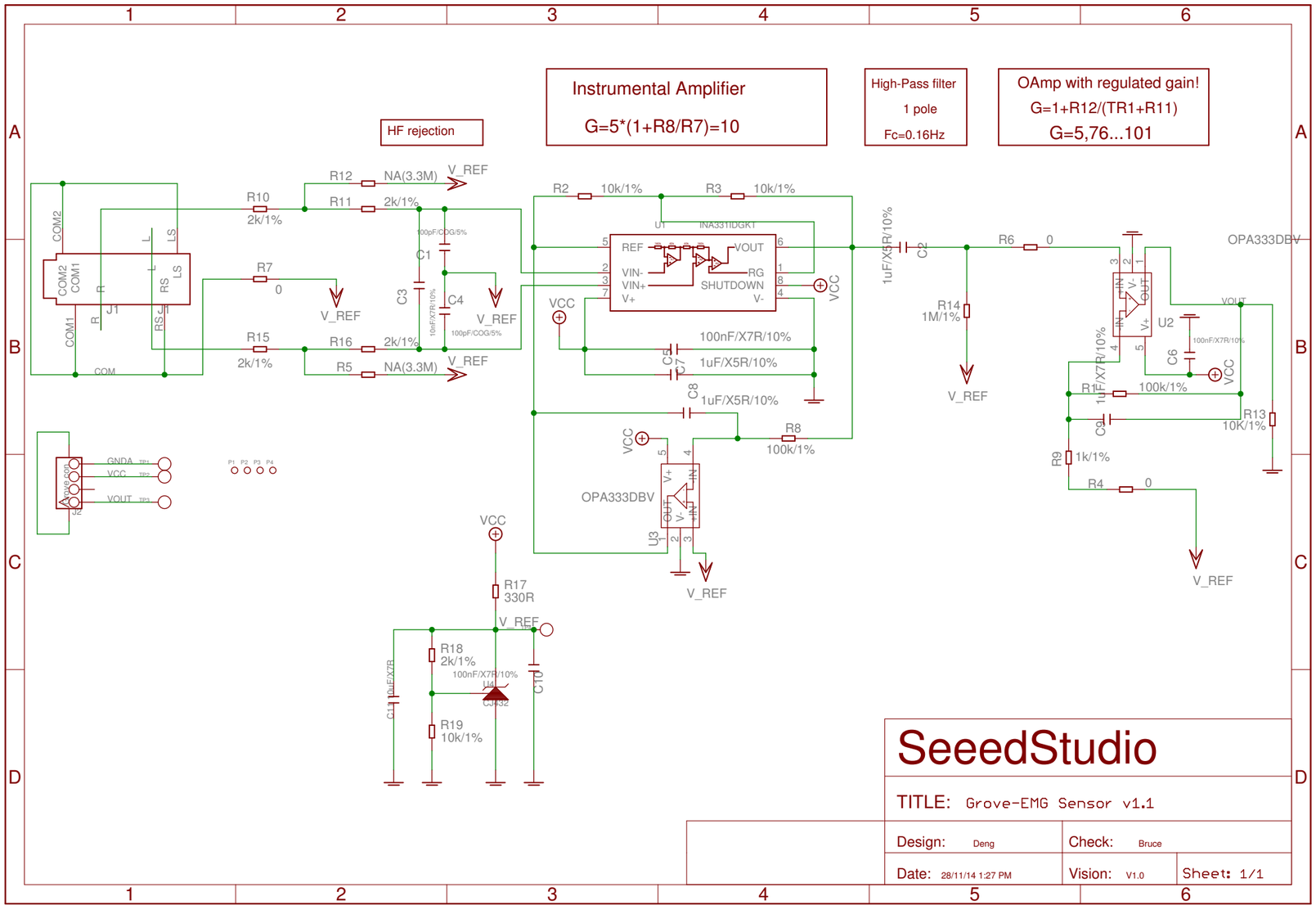


Figura 95. Etapa analógica sin filtro Notch con ganancia de 2500

2. Planos

2.3. Grove

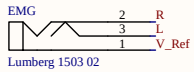
2.3.2. Esquemático


Instrumental Amplifier
G=5*(1+R8/R7)=10
HF rejection
High-Pass filter
1 pole
Fc=0.16Hz
OAmp with regulated gain!
G=1+R12/(TR1+R11)
G=5,76...101
R12 NA(3.3M)
R10 2k/1%
R11 2k/1%
R7 0
R15 2k/1%
R16 2k/1%
R5 NA(3.3M)
C1 100pF/COG/5%
C3 10nF/X7R/10%
C4 100pF/COG/5%
V_REF
R2 10k/1%
R3 10k/1%
U1 INA331IDGKT
REF
VIN-
VIN+
V+
VOUT
RG
SHUTDOWN
V-
VCC
C5 100nF/X7R/10%
C7 1uF/X5R/10%
C8 1uF/X5R/10%
R8 100k/1%
OPA333DBV
U3
C2 1uF/X5R/10%
R6 0
R14 1M/1%
U2
C6 100nF/X7R/10%
R1 100k/1%
C9 1uF/X7R/10%
R13 10K/1%
R9 1k/1%
R4 0
R17 330R
R18 2k/1%
R19 10k/1%
C11 1uF/X7R
C10 100nF/X7R/10%
U4
CJ432
J1
COM2
COM1
COM
L
LS
R
RS
GNDA TP1
VCC TP2
VOUT TP3
P1 P2 P3 P4
SeeedStudio
TITLE: Grove-EMG Sensor v1.1
Design: Deng
Check: Bruce
Date: 28/11/14 1:27 PM
Vision: V1.0
Sheet: 1/1

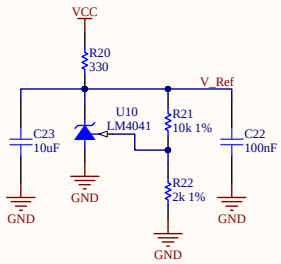
2.4. Prototipo alfa

2.4.1. Esquemático

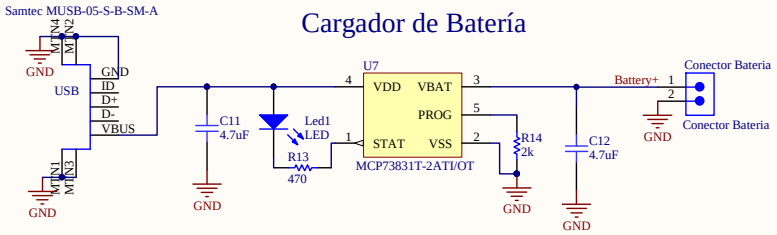
Entrada Señal EMG



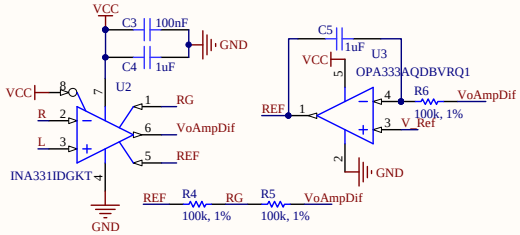
Tensión de Referencia



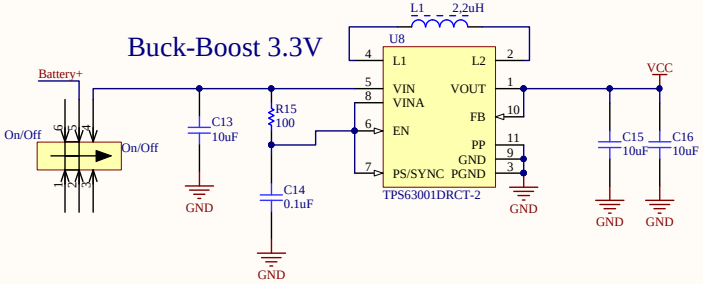
Cargador de Batería



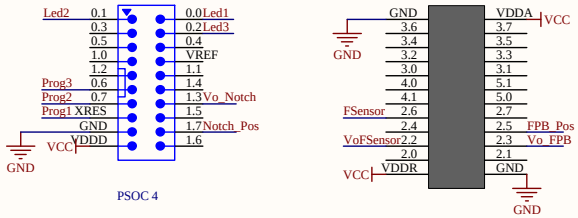
Amplificador Diferencial de Instrumentación G=5*(1+R5/R4)=10



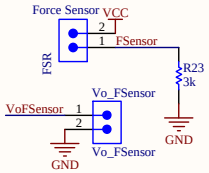
Buck-Boost 3.3V



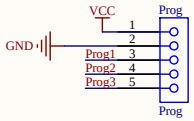
PSOC 4



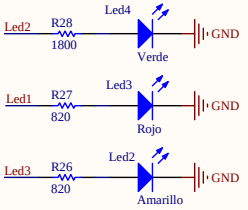
Sensor de Presión



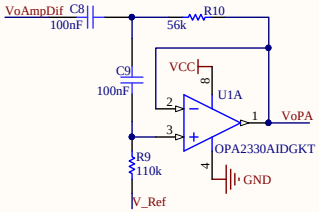
Programación



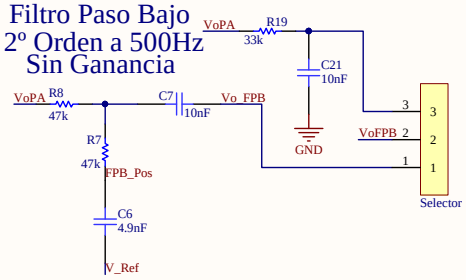
Leds Informativos



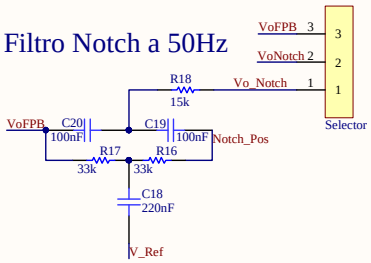
Filtro Paso Alto 2º Orden a 20Hz Sin Ganancia



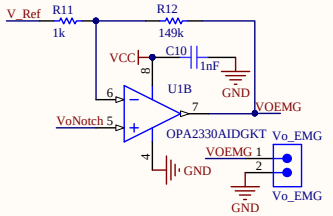
Filtro Paso Bajo 2º Orden a 500Hz Sin Ganancia



Filtro Notch a 50Hz

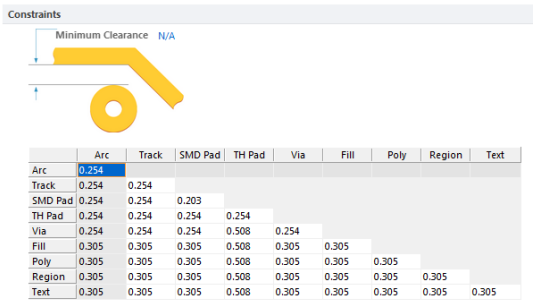


Amplificación Final Ganancia = 150



Title: Sensor EMG para biofeedback en fisioterapia		
Size: A3	Number: 1.0	Revision: 15/05/17
Date: 11/16/2017	Sheet of 1 to 1	
File: EMG.SchDoc	Drawn By: Rafael Fernández Gómez	

2.4.2. PCB



	Arc	Track	SMD Pad	TH Pad	Via	Fill	Poly	Region	Text
Arc	0.254								
Track	0.254	0.254							
SMD Pad	0.254	0.254	0.203						
TH Pad	0.254	0.254	0.254	0.254					
Via	0.254	0.254	0.254	0.508	0.254				
Fill	0.305	0.305	0.305	0.508	0.305	0.305			
Poly	0.305	0.305	0.305	0.508	0.305	0.305	0.305		
Region	0.305	0.305	0.305	0.508	0.305	0.305	0.305	0.305	
Text	0.305	0.305	0.305	0.508	0.305	0.305	0.305	0.305	0.305

Figura 96. PCB Rules

Las distancias están en mm.

2.4.2.1. Cara TOP

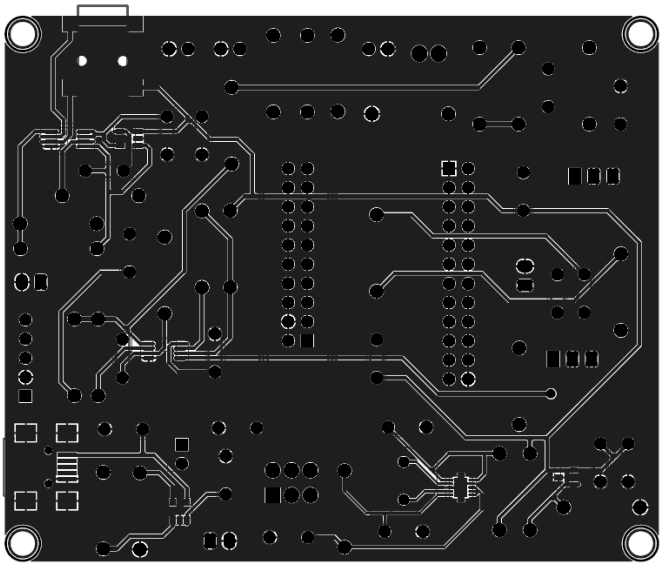


Figura 97. Cara TOP de la PCB del prototipo alfa

2.4.2.2. Cara BOTTOM

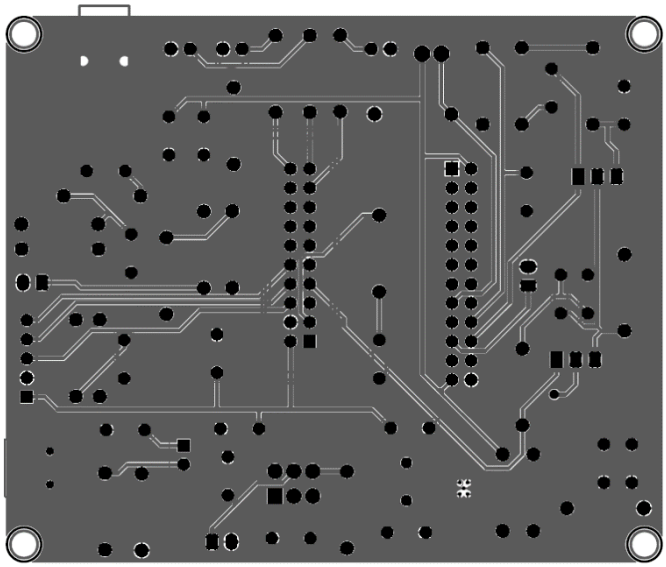
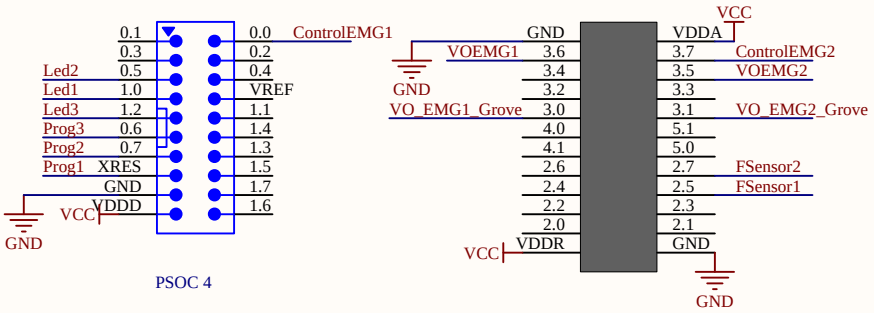


Figura 98. Cara BOTTOM de la PCB del prototipo alfa

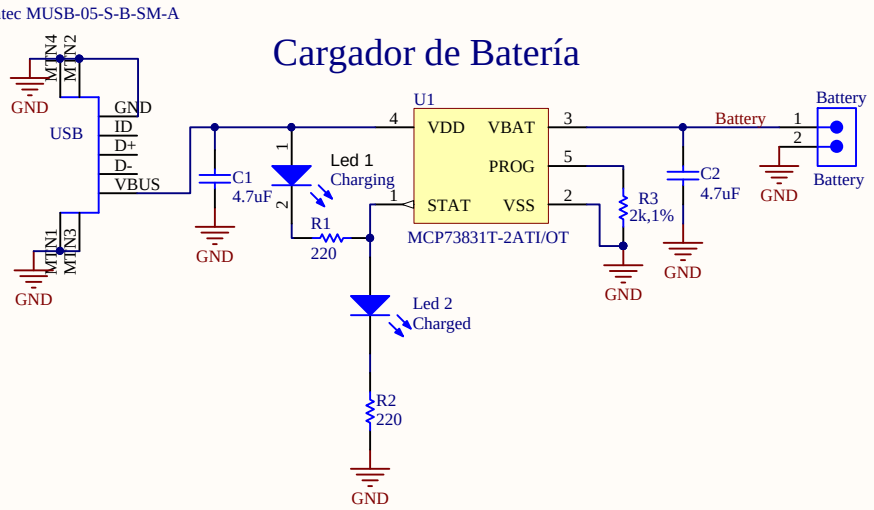
2.5. Prototipo Beta

2.5.1. Esquemático

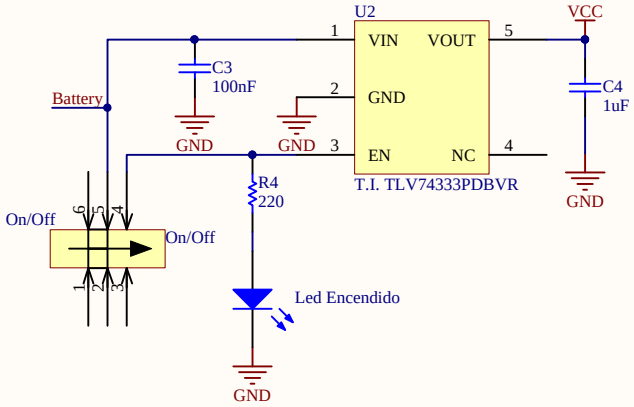
PSOC 4



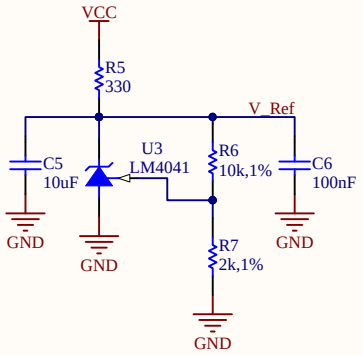
Cargador de Batería



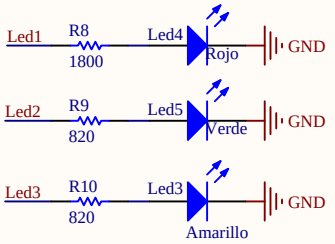
LDO Regulator 3.3V



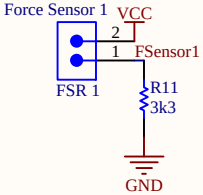
Tensión de Referencia



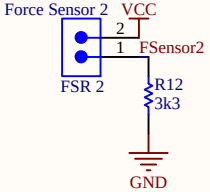
Leds Informativos



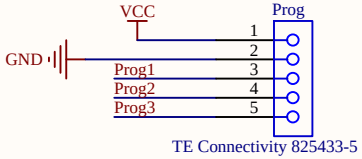
Sensor de Presión 1



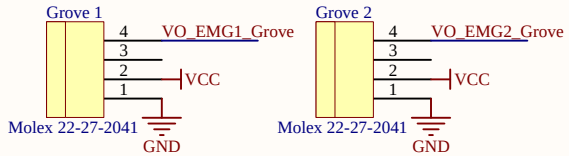
Sensor de Presión 2



Programación

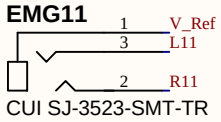


Grove

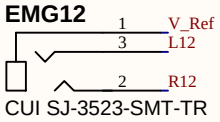


Title	Sensor EMG para biofeedback en fisioterapia	
Size: A4	Number: 2.0	Revision: 18/09/17
Date: 11/16/2017	Sheet of 1 to 3	
File: EMGyPressure.SchDoc	Drawn By: Rafael Fernández Gómez	

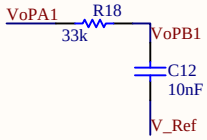
Señal EMG 1



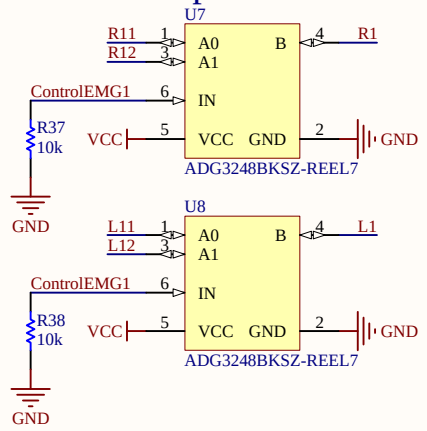
Señal EMG 2



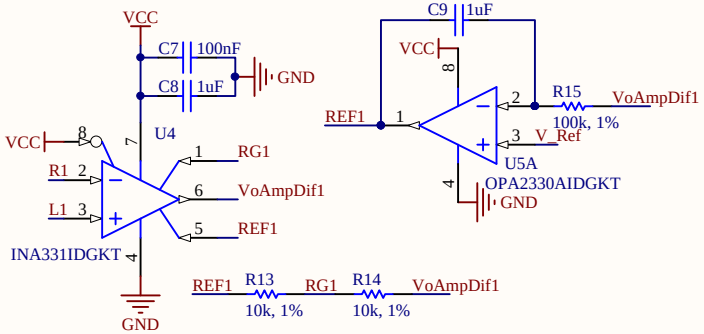
Filtro Paso Bajo 1er Orden a 500Hz



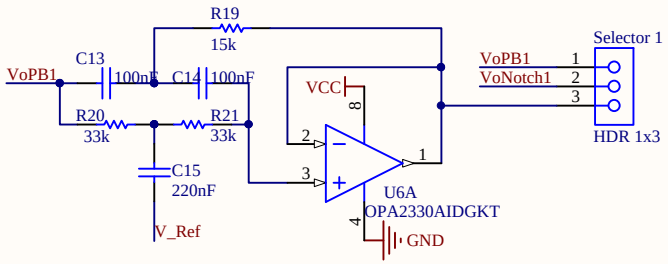
Multiplexores



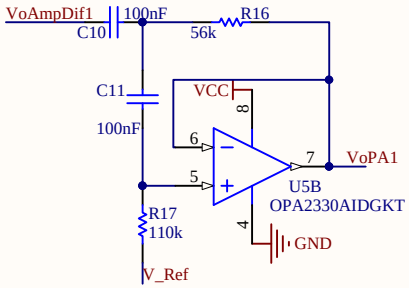
Amplificador Diferencial de Instrumentación G=5*(1+R5/R4)=10



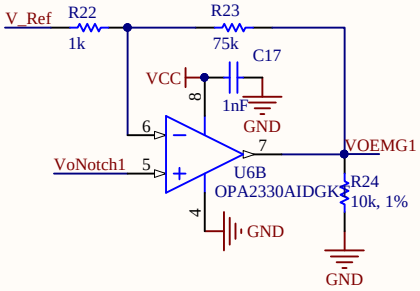
Filtro Notch 50Hz



Filtro Paso Alto 2º Orden a 20Hz Sin Ganancia



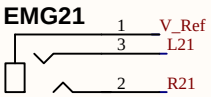
Amplificación Final Ganancia = 76



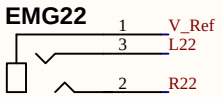
Ganancia Total = 760

Title: Sensor EMG para biofeedback en fisioterapia		
Size: A4	Number: 2.0	Revision: 18/09/17
Date: 11/16/2017	Sheet of 2 to 3	
File: EMGyPressure2.SchDoc	Drawn By: Rafael Fernández Gómez	

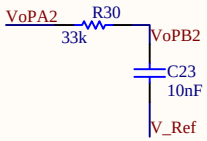
Señal EMG 1



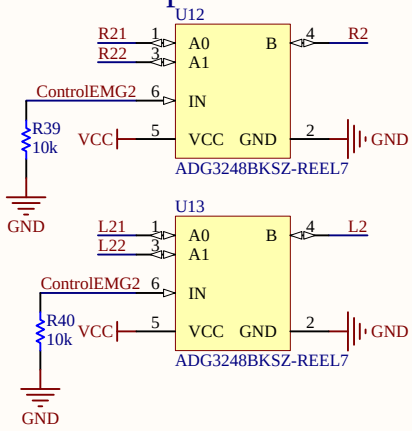
Señal EMG 2



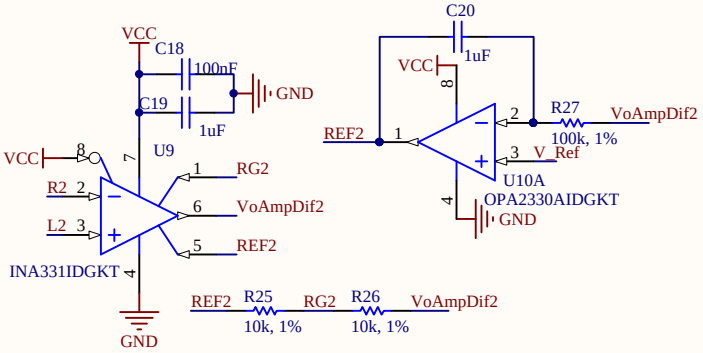
Filtro Paso Bajo 1er Orden a 500Hz



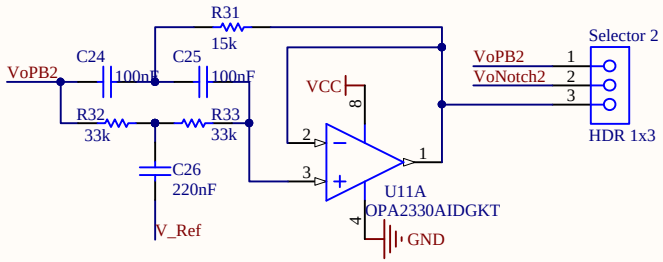
Multiplexores



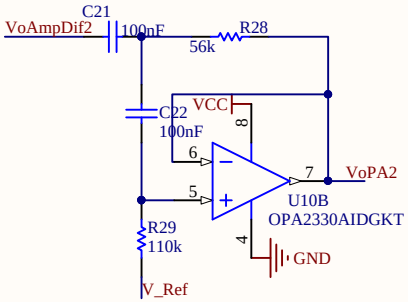
Amplificador Diferencial de Instrumentación G=5*(1+R5/R4)=10



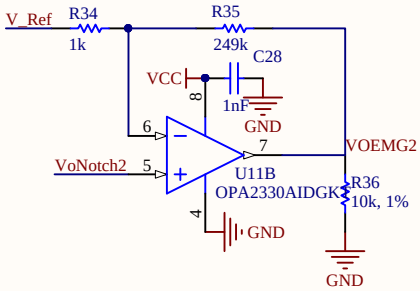
Filtro Notch 50Hz



Filtro Paso Alto 2º Orden a 20Hz Sin Ganancia



Amplificación Final Ganancia = 250



Ganancia Total = 2500

Title: Sensor EMG para biofeedback en fisioterapia		
Size: A4	Number: 2.0	Revision: 18/09/17
Date: 11/16/2017	Sheet of 3 to 3	
File: EMGyPressure3.SchDoc	Drawn By: Rafael Fernández Gómez	

2.5.2. PCB

2.5.2.1. Cara TOP

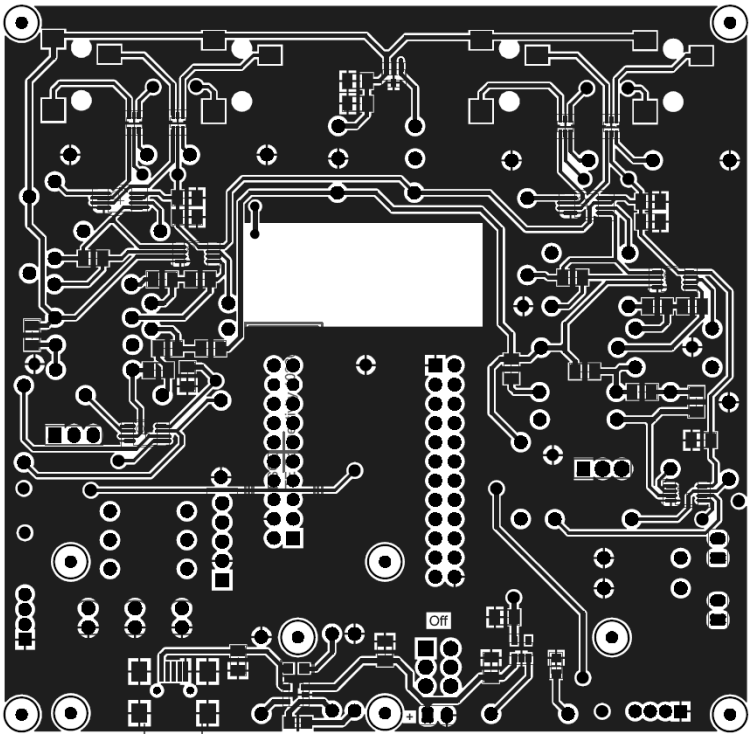


Figura 99. Cara TOP de la PCB del prototipo beta

2.5.2.2. Cara BOTTOM

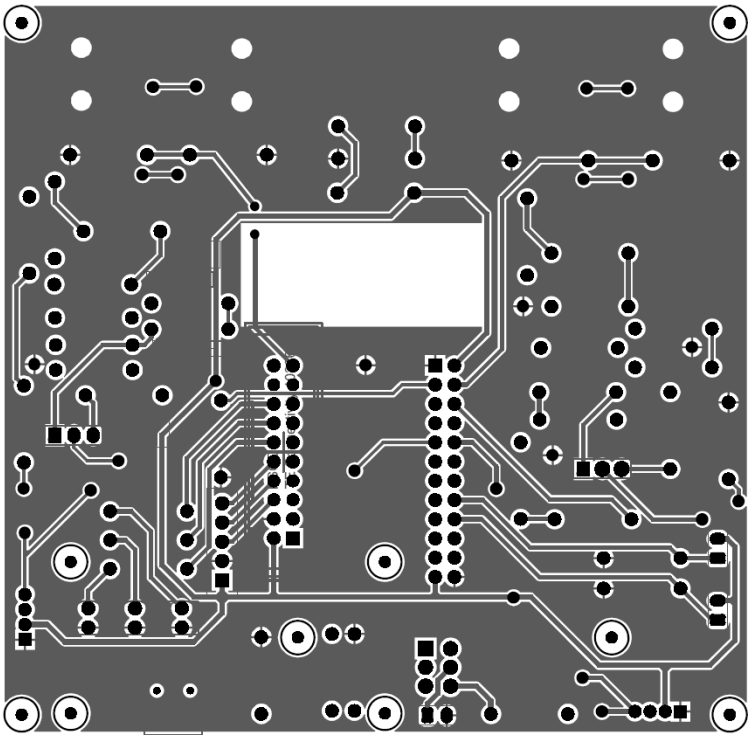


Figura 100. Cara BOTTOM de la PCB del prototipo beta

3. PSoC Creator 4.0

3.1. Esquemático

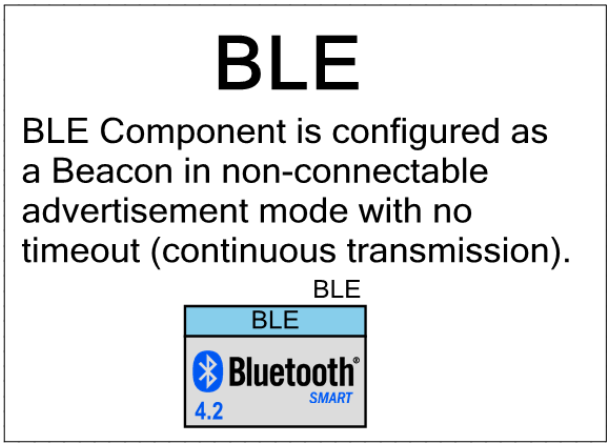


Figura 101. Bloque Bluetooth Low Energy en PSoC

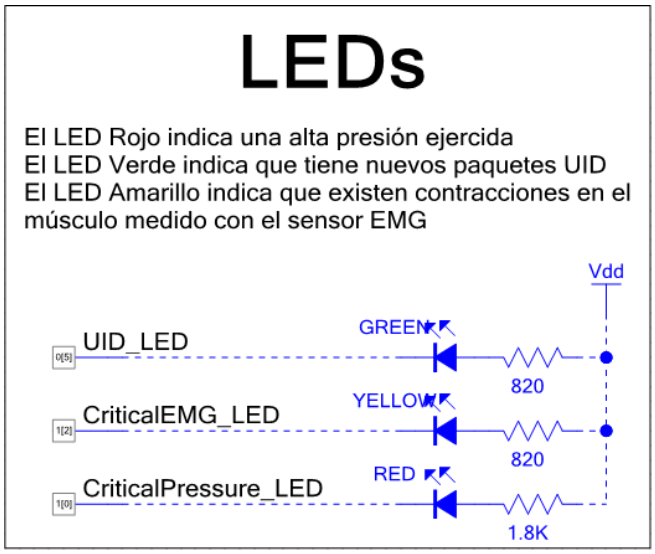


Figura 102. Bloque de interfaz Led en PSoC

Figura 103. Bloque del control de los Multiplexores en PSoC

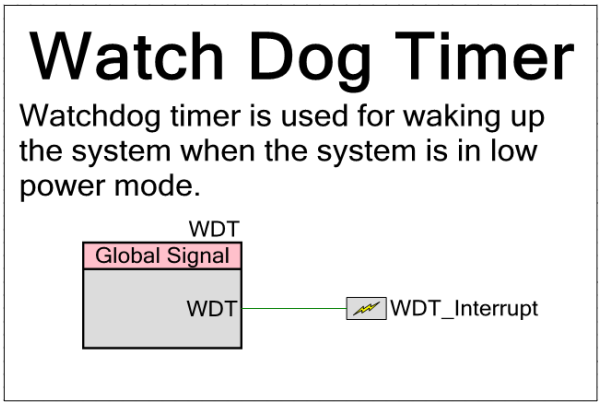


Figura 104. Bloque del Watch Dog Timer en PSoC

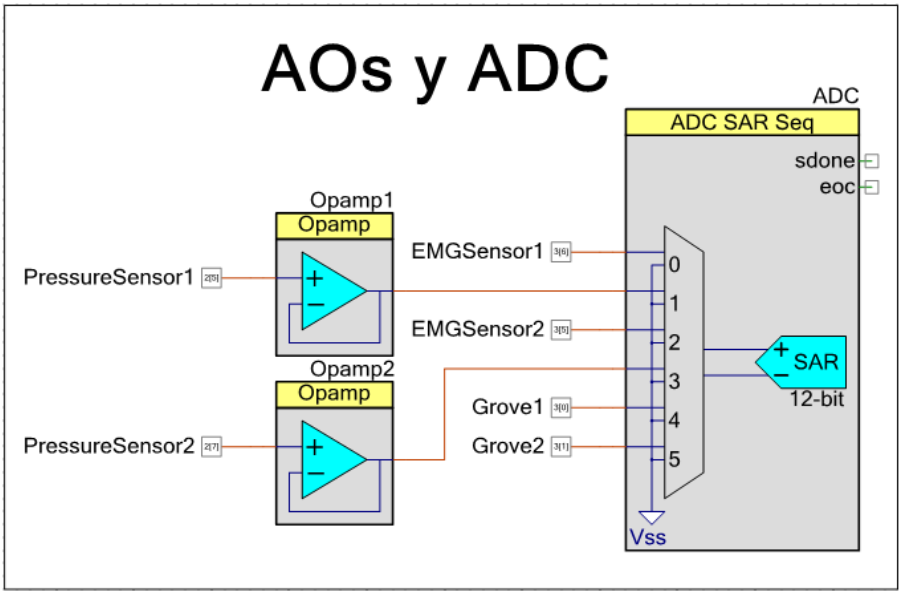


Figura 105. Bloque de los AOs y del CAD en PSoC

3.2. Configuración de pines y bloques de analógica

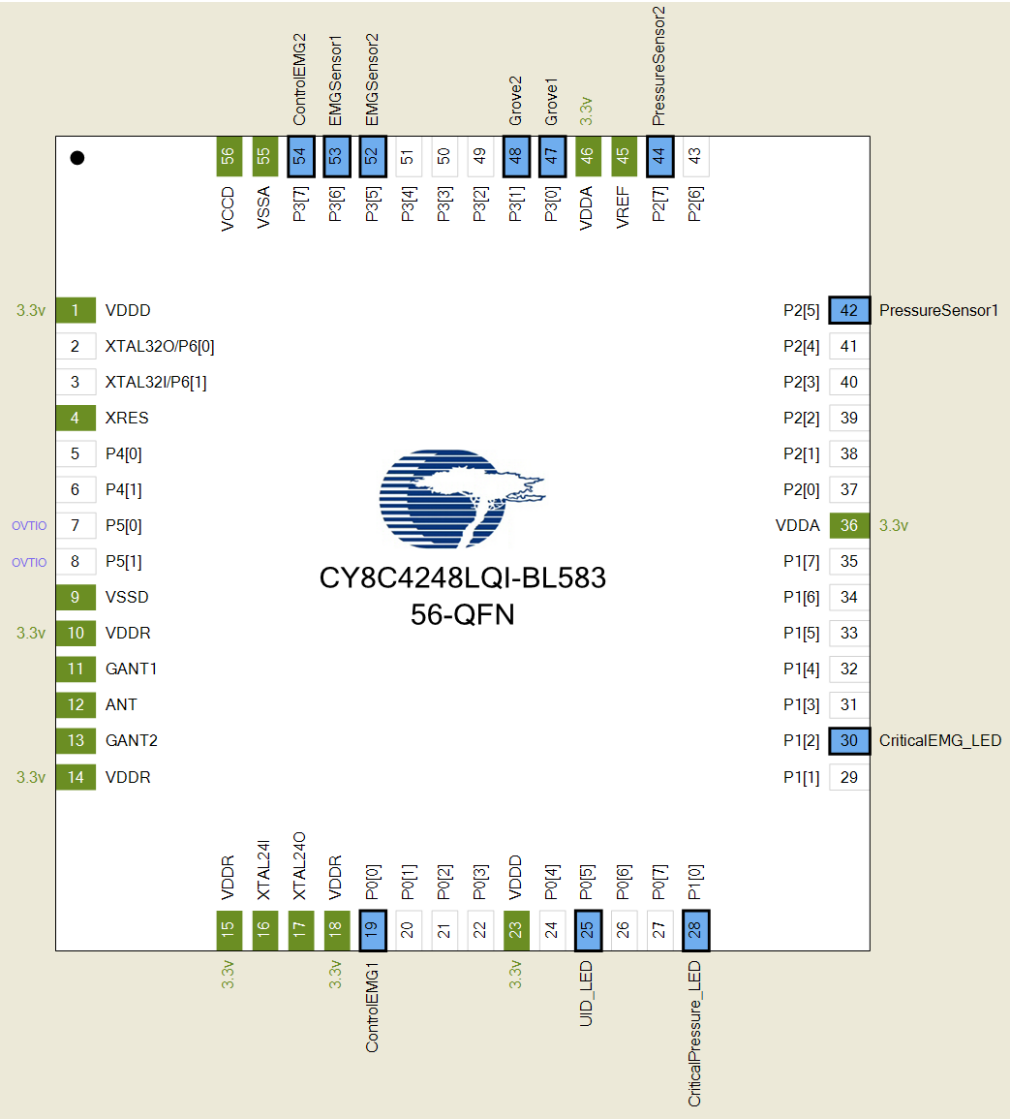


Figura 106. Configuración de pines en el microcontrolador

	Name	Port	Pin	Lock
	ControlEMG1	P0[0]	19	☑
	ControlEMG2	P3[7]	54	☑
	CriticalEMG_LED	P1[2]	30	☑
	CriticalPressure_LED	P1[0]:0	28	☑
	EMGSensor1	P3[6]	53	☑
	EMGSensor2	P3[5]	52	☑
	Grove1	P3[0]	47	☑
	Grove2	P3[1]	48	☑
	PressureSensor1	P2[5]	42	☑
	PressureSensor2	P2[7]	44	☑
	UID_LED	P0[5]	25	☑

Figura 107. Lista de los pines usados en el microcontrolador

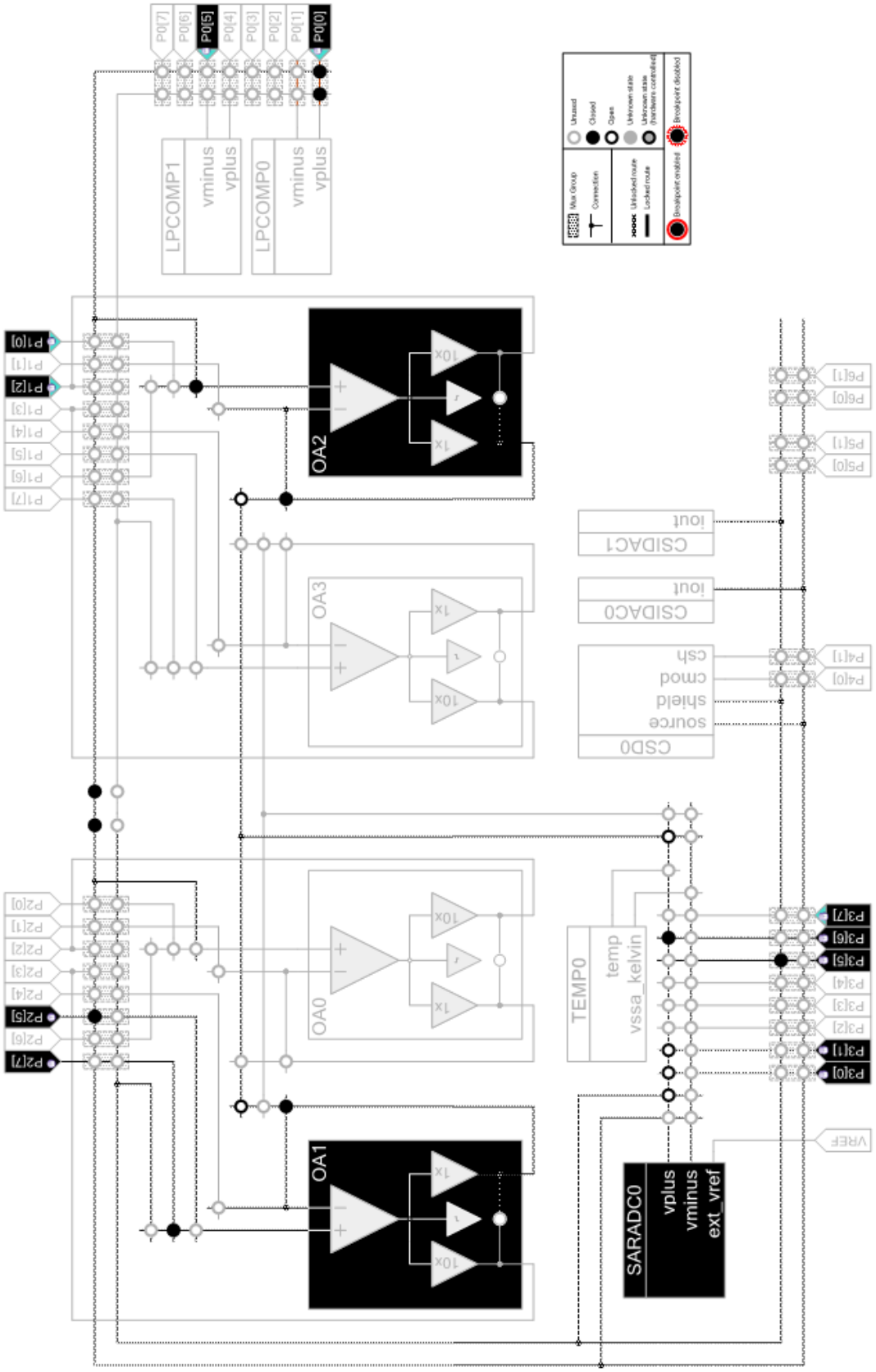


Figura 108. Configuración de la analógica interna del microcontrolador

3.3. Software

A continuación se adjunta toda la programación en C de los archivos que compone nuestro prototipo beta, partiendo del código de ejemplo: PSoC_4_BLE_Eddystone.

3.3.1. Main.c

```
/*******************************************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : main.c
* Version           : 1.0
* Device Used           : CY8C4248LQI-BL583
* Software Used         : PSoC Creator 3.3 CP2
* Compiler              : ARM GCC 4.9.3, ARM MDK Generic
* Related Hardware      : CY8CKIT-042-BLE-A Bluetooth Low Energy
Pioneer Kit
* Owner             : DEJO
*
********************************************************************
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Reserved.
*******************************************************************/

/*******************************************************************
*                            THEORY OF OPERATION
********************************************************************
* This project implements a BLE beacon based on Google's Eddystone
protocol.
* To view the beacon on an android device use Locate Beacon (or any
other beacon
* scanning app).
*******************************************************************/
#include <project.h>
#include <stdbool.h>
#include "WatchdogTimer.h"
#include "main.h"
#include "Eddystone.h"
#include "EMGyPressure.h"
#include "LiquidCrystal_I2C.h"
#include <stdio.h>

/*******************************************************************
* Global Variable Declaration
*******************************************************************/

/* This counter keeps track of total number of advertisement packets
*  transmitted. */
static uint32  advPacketCount = 0;

/* This flag when true stops BLE for advertising. */
static bool stopAdv = false;

/* To decide whether to have connectable or non-connectable adv */
static bool startConnAdv = false;
```

```
/*******************************************************************************
* Function Name: WCO_ECO_LowPowerStart
********************************************************************************
*
* Summary:
*   This function is used to handle the WCO and ECO clock during the
*   stabilization process.
*
* Parameters:
*   none
*
* Return:
*   none
*
*******************************************************************************/
void WCO_ECO_LowPowerStart(void)
{
    /* Setup counter0 for WCO startup */
    WDT_Initialize(CY_SYS_WDT_COUNTER0, WCO_STARTUP_PERIOD);

    /* Start the WCO clock */
    CySysClkWcoStart();

    /* WCO takes 500ms to stabilize. Enable counter 0 to trigger an
interrupt
    *  after 500ms. This helps to keep the device in low power mode
for 500ms.
    */
    WDT_EnableCounter(CY_SYS_WDT_COUNTER0_MASK);

    /* Put the system in deepsleep and Wait for the WDT counter 0
interrupt to
    *  wake up the device. On wakeup WCO is up & running */
    CySysPmDeepSleep();

    /*Unlock the WDT registes*/
    CySysWdtUnlock();

    /* Switch WCO to the low power mode after startup */
    CySysClkWcoSetPowerMode(CY_SYS_CLK_WCO_LPM);

    /* LFCLK is now driven by WCO */
    CySysClkSetLfclkSource(CY_SYS_CLK_LFCLK_SRC_WCO);

    /* WCO is running, shut down the ILO */
    CySysClkIloStop();

    /*Lock the WDT registes*/
    CySysWdtLock();

    /* Disable counter 0 */
    WDT_DisableCounter(CY_SYS_WDT_COUNTER0_MASK);

    /* Setup counter0 for ECO startup */
    WDT_Initialize(CY_SYS_WDT_COUNTER0, ECO_STARTUP_PERIOD);

    /* WCO is stabliized and It's time to start ECO */
    CySysClkEcoStart(0);
```

```
 /* ECO takes ~3msec to stabilize. Enable counter 1 to trigger an
interrupt
    *  after 3.5msec. This helps to keep the device in low power mode
for
    *  3.5msec and don't let PMIC to discharge. If we don't do this,
PMIC drains
    *  out */

    /* Enable WDT's  counter 0 to generate an interrupt after 3.5
mseconds */
    WDT_EnableCounter(CY_SYS_WDT_COUNTER0_MASK);

    /* Put the system in deepsleep and Wait for the WDT counter 0
    *  interrupt to wake up the device. On wakeup ECO is up & running
*/
    CySysPmDeepSleep();

    /* Both ECO and WCO are stabilized. Disable the counter 0 */
    WDT_DisableCounter(CY_SYS_WDT_COUNTER0_MASK);
}

/*******************************************************************************
* Function Name: Initialization
********************************************************************************
*
* Summary:
*   This function is used to intialize all blocks of the application
*
* Parameters:
*   none
*
* Return:
*   none
*
*******************************************************************************/
void Initialization(void)
{
    /* Set the divider for ECO, ECO will be used as source when IMO is
switched
    *  off to save power, to drive the HFCLK */
    CySysClkWriteEcoDiv(CY_SYS_CLK_ECO_DIV8);

    /* Do the following for achieving lowest possible WCO & ECO
startup current:
    *  1. Shut down the ECO (to reduce power consumption while WCO is
starting)
    *  2. Enable WDT counter 0 to wakeup the system after 500ms
    *     (500ms = WCO startup time)
    *  3. Configure PSoC 4 BLE device in DeepSleep mode for the 500ms
WCO
    *     startup time
    *  4. After WCO is enabled, restart the ECO so that BLESS
interface can
    *     function
    *  5. Enable WDT counter 1 to wakeup the system after 1ms
    *     (1ms = ECO startup time)
    *  5. Configure PSoC 4 BLE device in DeepSleep mode for the 1ms
ECO startup
    *     time */
```

```
    /* Shutdown the ECO and later re-start in low power mode after WCO
is turned
    *  on. */
    CySysClkEcoStop();

    /* Initialize WDT interrupt */
    WDT_Interrupt_StartEx(WDT_Handler);

    /* Enable WCO & ECO in low power mode using WDT counter 0/1 as
system wakeup
    *  sources respectively */
    WCO_ECO_LowPowerStart();

    /* Start BLE component and register the EddystoneEventHandler
function. This
    *  function exposes the events from BLE component for application
use. */
    CyBle_Start(EddystoneEventHandler);

    cyBle_attValuesLen[16].actualLength = DEFAULT_URL_LENGTH;

    /* Start the ADC component for temperature and battery
measurement. */
    ADC_Start();

    /* Put ADC to sleep and wake it up onlu formeasurements. */
    ADC_Sleep();

    //Inicialización de los AOs
    Opamp1_Start();
    Opamp1_SetPower(Opamp1_HIGHPOWER);

    Opamp2_Start();
    Opamp2_SetPower(Opamp2_HIGHPOWER);
}

/*******************************************************************
* Function Name: LowPower
********************************************************************
*
* Summary:
*   This function is used to set the BLESS and CPU in low power mode
in between
*   the advertising/connection intervals
*
* Parameters:
*   none
*
* Return:
*   none
*
*******************************************************************/
void LowPower(void)
{
    CYBLE_LP_MODE_T pwrState;
    CYBLE_BLESS_STATE_T blessState;
    uint8 intStatus = 0;

    /* Configure BLESS in Deep-Sleep mode */
    pwrState = CyBle_EnterLPM(CYBLE_BLESS_DEEPSLEEP);
```

```
    /* No interrupts allowed while entering system low power modes */
    intStatus = CyEnterCriticalSection();

    /* Get current BLE state. */
    blessState = CyBle_GetBleSsState();

    /* Make sure BLESS is in Deep-Sleep before configuring system in
Deep-Sleep
    */
    if(pwrState == CYBLE_BLESS_DEEPSLEEP)
    {
        if(blessState == CYBLE_BLESS_STATE_ECO_ON || blessState ==

CYBLE_BLESS_STATE_DEEPSLEEP)
        {
            /* System Deep-Sleep. 1.3uA mode */
            CySysPmDeepSleep();
        }
    }
    else if (blessState != CYBLE_BLESS_STATE_EVENT_CLOSE)
    {
        /* Change HF clock source from IMO to ECO, as IMO can be
stopped to save
        *  power. */
        CySysClkWriteHfclkDirect(CY_SYS_CLK_HFCLK_ECO);

        /* Stop IMO for reducing power consumption */
        CySysClkImoStop();

        /* Put the CPU to Sleep. 1.1mA mode */
        CySysPmSleep();

        /* Starts execution after waking up, start IMO */
        CySysClkImoStart();

        /* Change HF clock source back to IMO */
        CySysClkWriteHfclkDirect(CY_SYS_CLK_HFCLK_IMO);
    }

    CyExitCriticalSection(intStatus);
}

/*******************************************************************
* Function Name: GetAdvPacketCount
********************************************************************
*
* Summary:
*   This function returns value of advPacketCount.
*
* Parameters:
*   none
*
* Return:
*   uint32: returns value of advPacketCount
*
*******************************************************************/
uint32 GetAdvPacketCount(void)
{
    return advPacketCount;
}
```

```
/*******************************************************************
* Function Name: SetAdvPacketCount
********************************************************************
*
* Summary:
*   This function sets value of advPacketCount.
*
* Parameters:
*   uint32: returns value of advPacketCount
*
* Return:
*   none
*
*******************************************************************/
void SetAdvPacketCount(uint32 value)
{
    advPacketCount =  value;
}

/*******************************************************************
* Function Name: IncrementAdvPacketCount
********************************************************************
*
* Summary:
*   This function keeps track of adv packets based on BLESS states.
*
* Parameters:
*   none
*
* Return:
*   none
*
*******************************************************************/
void IncrementAdvPacketCount(void)
{
    static bool advOnGoing = false;
    CYBLE_BLESS_STATE_T blessState;

    /* Get current BLE state. */
    blessState = CyBle_GetBleSsState();

    if(CyBle_GetState() == CYBLE_STATE_ADVERTISING)
    {
        if (    (blessState == CYBLE_BLESS_STATE_ACTIVE) ||
                (blessState == CYBLE_BLESS_STATE_ECO_ON) ||
                (blessState == CYBLE_BLESS_STATE_ECO_STABLE))
        {
            advOnGoing = true;
        }
        else
        {
            /* Counts the number of packets that were advertised since
power on.
            *  It misses the count(by 1) when advertisement is stopped
and
            *  started again to change the frames. Increment
advPacketCount only
            *  when an advertisement is completed. */
            if (advOnGoing == true)
            {
                /* Increament advertisment packet count. */
```

```
                advPacketCount++;

                if(advPacketCount == 0)
                {
                    /* SecCnt should be zero if advPacketCount is
reset */
                    SetSecCnt(0);
                }
            }
            advOnGoing = false;
        }
    }
}

/*******************************************************************************
* Function Name: main
********************************************************************************
*
* Summary:
*  Main function.
*
* Parameters:
*  None
*
* Return:
*  None
*
*******************************************************************************/
int main()
{
    /* Enable global interrupt mask */
    CyGlobalIntEnable;

    /* This function will initialize the system resources such as BLE
and ADC */
    Initialization();

    while (1)
    {
        //Actualización de los valores del CAD
        MeasureEMGyPressure();

        /* Process BLESS states */
        IncrementAdvPacketCount();

        /* BLE stack processing state machine interface */
        CyBle_ProcessEvents();

        /* Put CPU and BLESS to low power mode */
        LowPower();

        if(stopAdv && (CyBle_GetState() == CYBLE_STATE_ADVERTISING))
        {
            //Reset the stop advertisement flag.
            stopAdv = false;
            //Stop advertisement.
            CyBle_GappStopAdvertisement();
        }
    }
}
/* [] END OF FILE */
```

3.3.2. Main.h

```
/*****************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : main.h
*****************************************/

#ifndef __MAIN_H__
#define __MAIN_H__

#include <project.h>
#include <stdbool.h>

/***************************************************************************
* Macros and Constants
***************************************************************************/
#define YES                                 (1)
#define NO                                  (0)

#define LED_ON                              (1)
#define LED_OFF                             (0)

#define TEMPERATURE_SENSOR_ENABLE           (NO)
#define BATTERY_MEASUREMENT_ENABLE          (NO)

#define WCO_STARTUP_PERIOD                  ((uint32)(32767 / 2))   /* 500
msec */
#define ECO_STARTUP_PERIOD                  ((uint32)(32 * 3.5))    /* 3.5
msec */

/***************************************************************************
* Function prototype
***************************************************************************/
void LowPower(void);
void SetAdvPacketCount(uint32 value);
uint32 GetAdvPacketCount(void);
bool IsConnAdvStart(void);

#endif  /* __MAIN_H__    */

/* [] END OF FILE */
```

3.3.3. EMGyPressure.c

```
/*****************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : EMGyPressure.c
*****************************************/

#include "main.h"
#include "EMGyPressure.h"

/* Stores measured EMG y Pressure */
static uint16 measuredsignalEMG1;
static uint16 measuredsignalEMG2;
static uint16 measuredsignalPressure1;
static uint16 measuredsignalPressure2;
static uint16 measuredsignalGrove1;
static uint16 measuredsignalGrove2;
static uint8 Pressure1;
static uint8 Pressure2;
uint8 x=0;


/*******************************************************************************
* Function Name: MeasureEMGyPressure
********************************************************************************
*
* Summary:
*   Esta función recibe los datos del sensor EMG y de Presión
*   del CAD en mV. Y posteriormente se tratan estas medidas.
*
* Parameters:
*  None
*
* Return:
*  None
*
*******************************************************************************/
void MeasureEMGyPressure(void)
{
    int16 ADCResultEMG1,ADCResultPressure1,ADCResultGrove1;
    int16 ADCResultEMG2,ADCResultPressure2,ADCResultGrove2;

    /* Wakeup ADC from sleep for measurements. */
    ADC_Wakeup();

    /* Enables injection channel and performs a measurement. */
    ADC_StartConvert();
    ADC_IsEndConversion(ADC_WAIT_FOR_RESULT);

    //Recogida de los datos del CAD y su posterior conversión a mV
    ADCResultEMG1=ADC_GetResult16(ADC_EMG1_CHANNEL);

      measuredsignalEMG1=ADC_CountsTo_mVolts(ADC_EMG1_CHANNEL,ADCResul
      tEMG1);

    ADCResultPressure1=ADC_GetResult16(ADC_Pressure1_CHANNEL);

      measuredsignalPressure1=ADC_CountsTo_mVolts(ADC_Pressure1_CHANNE
      L,ADCResultPressure1);
```

```
ADCResultEMG2=ADC_GetResult16(ADC_EMG2_CHANNEL);

      measuredsignalEMG2=ADC_CountsTo_mVolts(ADC_EMG2_CHANNEL,ADCResul
      tEMG2);

ADCResultPressure2=ADC_GetResult16(ADC_Pressure2_CHANNEL);

      measuredsignalPressure2=ADC_CountsTo_mVolts(ADC_Pressure2_CHANNE
      L,ADCResultPressure2);

ADCResultGrove1=ADC_GetResult16(ADC_Grove1_CHANNEL);

      measuredsignalGrove1=ADC_CountsTo_mVolts(ADC_Grove1_CHANNEL,ADCR
      esultGrove1);

ADCResultGrove2=ADC_GetResult16(ADC_Grove2_CHANNEL);

      measuredsignalGrove2=ADC_CountsTo_mVolts(ADC_Grove2_CHANNEL,ADCR
      esultGrove2);

    /* Put ADC to sleep after measurements are done. */
    ADC_Sleep();

    //Limites en ambos extremos para asegurarnos un dato correcto
    if(measuredsignalEMG1>0x0ce2) measuredsignalEMG1=0x0ce2;
    else if (measuredsignalEMG1<0x0001) measuredsignalEMG1=0x0000;

    if(measuredsignalEMG2>0x0ce2) measuredsignalEMG2=0x0ce2;
    else if (measuredsignalEMG2<0x0001) measuredsignalEMG2=0x0000;

    if(measuredsignalPressure1>0x0ce2) measuredsignalPressure1=0x0ce2;
    else if (measuredsignalPressure1<0x0001)
measuredsignalPressure1=0x0000;

    if(measuredsignalPressure2>0x0ce2) measuredsignalPressure2=0x0ce2;
    else if (measuredsignalPressure2<0x0001)
measuredsignalPressure2=0x0000;

    if(measuredsignalGrove1>0x0ce2) measuredsignalGrove1=0x0ce2;
    else if (measuredsignalGrove1<0x0001) measuredsignalGrove1=0x0000;

    if(measuredsignalGrove2>0x0ce2) measuredsignalGrove2=0x0ce2;
    else if (measuredsignalGrove2<0x0001) measuredsignalGrove2=0x0000;

    //Tratamiento de la señal obtenida
    //Resultado en hexadecimal en g/cm^2
    Pressure1=(measuredsignalPressure1/23.52);
    Pressure2=(measuredsignalPressure2/23.52);

    //Detección de un valor alto de presión
    if((Pressure1)>0x70 || (Pressure2)>0x70)
CriticalPressure_LED_Write(1);
    else CriticalPressure_LED_Write(0);

    //Detección de un valor alto de EMG
    if(measuredsignalEMG2>0x723)  //1827mV
    {CriticalEMG_LED_Write(1);}
    else {CriticalEMG_LED_Write(0);}
```

```
//Cambio entre los diferentes EMGs, activación o desactivación de los
multiplexores
    if(x==1)
    {
        ControlEMG1_Write(1);
        ControlEMG2_Write(1);
        x=0;
    } else{
                ControlEMG1_Write(0);
                ControlEMG2_Write(0);
                x=1;
            }
}

//Funciones de recogida de los datos
uint16 GetMeasuredEMG1(void)
{
    return measuredsignalEMG1;
}
uint16 GetMeasuredEMG2(void)
{
    return measuredsignalEMG2;
}
uint8 GetMeasuredPressure1(void)
{
    return Pressure1;
}
uint8 GetMeasuredPressure2(void)
{
    return Pressure2;
}
uint16 GetMeasuredGrove1(void)
{
    return measuredsignalGrove1;
}
uint16 GetMeasuredGrove2(void)
{
    return measuredsignalGrove2;
}

/* [] END OF FILE */
```

3.3.4. EMGyPressure.h

```
/*****************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : EMGyPressure.h
*****************************************/

#ifndef __TEMPERATURE_H__
#define __TEMPERATURE_H__

#include <project.h>
#include <stdbool.h>

/***************************************************************************
* Constants
***************************************************************************/
#define ADC_EMG1_CHANNEL          0
#define ADC_EMG2_CHANNEL          2
#define ADC_Pressure1_CHANNEL     1
#define ADC_Pressure2_CHANNEL     3
#define ADC_Grove1_CHANNEL        4
#define ADC_Grove2_CHANNEL        5

/***************************************************************************
* Function Prototypes
***************************************************************************/
void MeasureEMGyPressure(void);
uint16 GetMeasuredEMG1(void);
uint16 GetMeasuredEMG2(void);
uint8 GetMeasuredPressure1(void);
uint8 GetMeasuredPressure2(void);
uint16 GetMeasuredGrove1(void);
uint16 GetMeasuredGrove2(void);

#endif

/* [] END OF FILE */
```

3.3.5. Eddystone.c

```
/*****************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : Eddystone.c
*****************************************/

#include <project.h>
#include <stdbool.h>
#include <string.h>
#include "Eddystone.h"
#include "WatchdogTimer.h"
#include "EMGyPressure.h"
#include "main.h"

#define LOCK_CODE_LENGTH                    16
#define MAX_URL_LENGTH                      19
#define DEFAULT_URL_LENGTH                  9
#define CONNECTABLE_STATE_TIMEOUT           30
#define CONNECTABLE_STATE_ADV_INTERVAL_MIN  0x00A0
#define CONNECTABLE_STATE_ADV_INTERVAL_MAX  0x00A0

/***************************************************************************
* Global Variable Declaration
***************************************************************************/

// The default URL
const uint8 DefaultURL[MAX_URL_LENGTH] = DEFAULT_URL;

// The default beacon lock key
const uint8 LOCK[LOCK_CODE_LENGTH] =    {
                            0x00, 0x00, 0x00, 0x00,
                            0x00, 0x00, 0x00, 0x00,
                            0x00, 0x00, 0x00, 0x00,
                            0x00, 0x00, 0x00, 0x00
                                        };

// To decide whether to have TLM packets interleaved or not
static bool isEddystoneTLMPresent = true;

// Selection of UID/URL
static EDDYSTONE_ROLE_T eddystoneImplenmentation = EDDYSTONE_UID;

// Select between UID/URL or TLM
static EDDYSTONE_ROLE_T beaconCurrentRole = EDDYSTONE_UID;

// Stores the current URL being advrtised
uint8 CurrentURL[MAX_URL_LENGTH] = DEFAULT_URL;

// Stores the current URL length being advrtised
uint8 URLLength = DEFAULT_URL_LENGTH;

// Stores the current tx power mode
uint8 currentTxmode = TX_POWER_MODE_LOW;
```

```
// Stores the current advertised tx power levels
uint8 currentTxPowerLevels[MAX_NUM_PWR_LVL] =    {

PWR_LVL_NEG_18_DBM,
                                                    PWR_LVL_NEG_6_DBM,
                                                    PWR_LVL_0_DBM,
                                                    PWR_LVL_3_DBM
                                                };

// Stores the current non-connectable adv interval
uint16 CurrentAdvPeriod = DEFAULT_BEACON_PERIOD;

// Stores the current URL flags
uint8 DefaultURLFlags = DEFAULT_URL_FLAG_VALUE;

//Advertising data when GAP Reol:Peripheral (connectable)
CYBLE_GAPP_DISC_DATA_T CyBleConnectableAdvData =
{
    {
        0x02u, // Length of flags
        0x01u, // Flags
        0x06u, // Flag data
        0x0Du, // length of Local name
        0x09u, // Local name
        'C',
        'Y',
        ' ',
        'E',
        'd',
        'd',
        'y',
        's',
        't',
        'o',
        'n',
        'e'
    },          // uint8 advertising_data[CYBLE_MAX_ADV_DATA_LEN]
        0x11u,  // uint8 adv_data_length
};

// True if an error response is send
static bool errorSent;

/*******************************************************************
* Function Name: WriteAttributeValue
********************************************************************
* Summary:
*  Writes a specified attribute value of certian length to the
appropriate
*  attribute handle present in the  GATT DB
* Parameters:
*  CYBLE_GATT_DB_ATTR_HANDLE_T  :  GATT DB Attribute Handle Type
*  uint8                        :  length of data
*  uint8*                       :  data buffer
*  uint8                        :  flags
* Return:
*  CYBLE_GATT_ERR_CODE_T        : returns the write operation error
code
*
*******************************************************************/
```

```
CYBLE_GATT_ERR_CODE_T WriteAttributeValue    (
                                CYBLE_GATT_DB_ATTR_HANDLE_T
attributeHandle,
                                uint8 length,
                                uint8* data,
                                uint8 flag
                                            )
{
    CYBLE_GATT_HANDLE_VALUE_PAIR_T handlevaluePair;
    CYBLE_GATT_ERR_CODE_T gattErrCode;

    handlevaluePair.attrHandle = attributeHandle;
    handlevaluePair.value.len = length;
    handlevaluePair.value.val = data;
    gattErrCode = CyBle_GattsWriteAttributeValue( &handlevaluePair, 0,
                                                  &cyBle_connHandle,
flag);

    return gattErrCode;
}

/*****************************************************************************
* Function Name: ResetGattDb
******************************************************************************
*
* Summary:
*  Resets all relevant characteristics in the GATT DB
*
* Parameters:
*  None
*
* Return:
*  None
*
*****************************************************************************/
void ResetGattDb(void)
{
    //Default URI Data
    memcpy(CurrentURL, DefaultURL, MAX_URL_LENGTH);

WriteAttributeValue(CYBLE_EDDYSTONE_CONFIGURATION_URI_DATA_CHAR_HANDLE
,
                        sizeof(DefaultURL), (uint8 *)DefaultURL,
                        CYBLE_GATT_DB_LOCALLY_INITIATED);
    URLLength = DEFAULT_URL_LENGTH;
    cyBle_attValuesLen[16].actualLength = URLLength;

    //Default URI Flags

WriteAttributeValue(CYBLE_EDDYSTONE_CONFIGURATION_URI_FLAGS_CHAR_HANDL
E,
                        sizeof(DefaultURLFlags), &DefaultURLFlags,
                        CYBLE_GATT_DB_LOCALLY_INITIATED);

    //Default TX power mode
    currentTxmode = TX_POWER_MODE_LOW;

WriteAttributeValue(CYBLE_EDDYSTONE_CONFIGURATION_TX_POWER_MODE_CHAR_H
ANDLE,
                        sizeof(currentTxmode), &currentTxmode,
                        CYBLE_GATT_DB_LOCALLY_INITIATED);
```

```
    //Default Beacon period
    CurrentAdvPeriod = DEFAULT_BEACON_PERIOD;

WriteAttributeValue(CYBLE_EDDYSTONE_CONFIGURATION_BEACON_PERIOD_CHAR_H
ANDLE,
                        sizeof(CurrentAdvPeriod), (uint8
*)&CurrentAdvPeriod,
                        CYBLE_GATT_DB_LOCALLY_INITIATED);

    //Default LOCK key

WriteAttributeValue(CYBLE_EDDYSTONE_CONFIGURATION_LOCK_CHAR_HANDLE,
                        sizeof(LOCK), (uint8 *)LOCK,
                        CYBLE_GATT_DB_LOCALLY_INITIATED);
}

/*******************************************************************
* Function Name: SendErrorResponse
********************************************************************
*
* Summary:
*  Sends error code for a particular attribute handle
*
* Parameters:
*  CYBLE_GATT_DB_ATTR_HANDLE_T  :  attribute handle
*  CYBLE_GATT_ERR_CODE_T        :  error code to be send
*
* Return:
*  None
*
*******************************************************************/
void SendErrorResponse( CYBLE_GATT_DB_ATTR_HANDLE_T attributeHandle,
                        CYBLE_GATT_ERR_CODE_T errorCode)
{
    CYBLE_GATTS_ERR_PARAM_T errorparam;

    errorparam.attrHandle = attributeHandle;
    errorparam.errorCode = errorCode;
    errorparam.opcode = CYBLE_GATT_WRITE_REQ;
    CyBle_GattsErrorRsp(cyBle_connHandle, &errorparam);
    errorSent = true;
}

/*******************************************************************
* Function Name: UpdateTxPower
********************************************************************
*
* Summary:
*  Updates advertisement transmit power based on the Tx power mode
*
* Parameters:
*  uint8:  Tx power mode to be set
*
* Return:
*  None
*
*******************************************************************/
```

```
void UpdateTxPower(uint8 TxMode)
{
    CYBLE_BLESS_PWR_IN_DB_T txPower;

    // Set channel type as Adv channels
    txPower.bleSsChId = CYBLE_LL_ADV_CH_TYPE;

    // Set the correct power levels
    if (TxMode == TX_POWER_MODE_HIGH)    // +3 dBm */
    {
        txPower.blePwrLevelInDbm = CYBLE_LL_PWR_LVL_3_DBM;
    }
    else if (TxMode == TX_POWER_MODE_MEDIUM)     // 0 dBm
    {
        txPower.blePwrLevelInDbm = CYBLE_LL_PWR_LVL_0_DBM;
    }
    else if (TxMode == TX_POWER_MODE_LOW)    // -6 dBm
    {
        txPower.blePwrLevelInDbm = CYBLE_LL_PWR_LVL_NEG_6_DBM;
    }
    else if (TxMode == TX_POWER_MODE_LOWEST)     // -18 dBm
    {
        txPower.blePwrLevelInDbm = CYBLE_LL_PWR_LVL_NEG_18_DBM;
    }

    // Set Tx power level
    CyBle_SetTxPowerLevel(&txPower);
}

/*******************************************************************
* Function Name: ProcessWriteReq
********************************************************************
*
* Summary:
*  Process all GATT level write requests and responds with appropriate
status
*
* Parameters:
*  CYBLE_GATTS_WRITE_CMD_REQ_PARAM_T:  GATT write command request
prameter
*
* Return:
*  None
*
*******************************************************************/
void ProcessWriteReq(CYBLE_GATTS_WRITE_CMD_REQ_PARAM_T writeCmdReq)
{
    bool value_val;
    uint8 status = LOCKED, key_buf[LOCK_CODE_LENGTH];
    uint16 beaconPeriod = 0;
    CYBLE_GATT_HANDLE_VALUE_PAIR_T valuePairT;

    // Reset error send flag
    errorSent = false;
    // Retrieve the LOCK status from the GATT DB
    valuePairT.attrHandle =

CYBLE_EDDYSTONE_CONFIGURATION_LOCK_STATE_CHAR_HANDLE;
    valuePairT.value.val = (uint8 *)&value_val;
    valuePairT.value.len = sizeof(bool);
```

```
    CyBle_GattsReadAttributeValue( &valuePairT, &cyBle_connHandle,
                                    CYBLE_GATT_DB_LOCALLY_INITIATED );

    // Check the LOCK status
    if(valuePairT.value.val[0] == UNLOCKED)
    {
        //URL Data
        if(writeCmdReq.handleValPair.attrHandle ==

CYBLE_EDDYSTONE_CONFIGURATION_URI_DATA_CHAR_HANDLE)
        {
            // First byte should be scheme prefix and length should be
less than
            //  or equal to MAX_URL_LENGTH
            if( (writeCmdReq.handleValPair.value.len <=
MAX_URL_LENGTH) &&
                (writeCmdReq.handleValPair.value.val[0] <
URL_PREFIX_MAX)   )
            {
                uint8 TempURL[MAX_URL_LENGTH];

                memset(TempURL, 0, MAX_URL_LENGTH);
                memcpy(
                            TempURL,
                            writeCmdReq.handleValPair.value.val,
                            writeCmdReq.handleValPair.value.len
                       );
                if( CYBLE_GATT_ERR_NONE == WriteAttributeValue   (

CYBLE_EDDYSTONE_CONFIGURATION_URI_DATA_CHAR_HANDLE,
                            writeCmdReq.handleValPair.value.len,
                            writeCmdReq.handleValPair.value.val,
                            CYBLE_GATT_DB_PEER_INITIATED        ) )
                {
                    // Update the length as per the new URL data
                    URLLength = writeCmdReq.handleValPair.value.len;
                    cyBle_attValuesLen[16].actualLength = URLLength;
                    // Update the URL data
                    memcpy(CurrentURL, TempURL, MAX_URL_LENGTH);
                }
            }
            else if (writeCmdReq.handleValPair.value.len >
MAX_URL_LENGTH)
            {
                 // Invalid length. Send error response
               SendErrorResponse        (

CYBLE_EDDYSTONE_CONFIGURATION_URI_DATA_CHAR_HANDLE,
                            CYBLE_GATT_ERR_INVALID_ATTRIBUTE_LEN
                                    );
            }
        }
        // Lock Characteristic
        else if(writeCmdReq.handleValPair.attrHandle ==

CYBLE_EDDYSTONE_CONFIGURATION_LOCK_CHAR_HANDLE)
        {
            if(writeCmdReq.handleValPair.value.len ==
LOCK_CODE_LENGTH)
            {
                WriteAttributeValue (
```

```
CYBLE_EDDYSTONE_CONFIGURATION_LOCK_CHAR_HANDLE,
                                writeCmdReq.handleValPair.value.len,
                                writeCmdReq.handleValPair.value.val,
                                CYBLE_GATT_DB_PEER_INITIATED
                                    );

                // Update the LOCK characteristic
                status = LOCKED;
                WriteAttributeValue (

CYBLE_EDDYSTONE_CONFIGURATION_LOCK_STATE_CHAR_HANDLE,
                        sizeof(bool), &status,
                        CYBLE_GATT_DB_LOCALLY_INITIATED
                                    );
            }
            else
            {
                // Invalid length. Send error response

SendErrorResponse(CYBLE_EDDYSTONE_CONFIGURATION_LOCK_CHAR_HANDLE,

CYBLE_GATT_ERR_INVALID_ATTRIBUTE_LEN);
            }
        }
        // Advertised Tx power level
        else if(writeCmdReq.handleValPair.attrHandle ==

CYBLE_EDDYSTONE_CONFIGURATION_ADVERTISED_TX_POWER_LEVELS_CHAR_HANDLE)
        {
            if (writeCmdReq.handleValPair.value.len ==
MAX_NUM_PWR_LVL)
            {
                WriteAttributeValue (

CYBLE_EDDYSTONE_CONFIGURATION_ADVERTISED_TX_POWER_LEVELS_CHAR_HANDLE,
                    writeCmdReq.handleValPair.value.len,
                    writeCmdReq.handleValPair.value.val,
                    CYBLE_GATT_DB_PEER_INITIATED
                                    );

                if (writeCmdReq.handleValPair.value.len ==
MAX_NUM_PWR_LVL)
                {
                    // Update Tx Power levels
                    memcpy  (
                                currentTxPowerLevels,
                                writeCmdReq.handleValPair.value.val,
                                MAX_NUM_PWR_LVL
                            );
                }
                else
                {
                    SendErrorResponse    (

CYBLE_EDDYSTONE_CONFIGURATION_ADVERTISED_TX_POWER_LEVELS_CHAR_HANDLE,
                        CYBLE_GATT_ERR_INVALID_ATTRIBUTE_LEN
                                        );
                }
            }
            else
```

```
            {
                // Invalid length. Send error response
               SendErrorResponse    (

CYBLE_EDDYSTONE_CONFIGURATION_ADVERTISED_TX_POWER_LEVELS_CHAR_HANDLE,
                    CYBLE_GATT_ERR_INVALID_ATTRIBUTE_LEN
                                    );
            }
        }
        // Tx Power Mode
        else if(writeCmdReq.handleValPair.attrHandle ==

CYBLE_EDDYSTONE_CONFIGURATION_TX_POWER_MODE_CHAR_HANDLE)
        {
            if(writeCmdReq.handleValPair.value.val[0] <= 0x03)
            {
                WriteAttributeValue (

CYBLE_EDDYSTONE_CONFIGURATION_TX_POWER_MODE_CHAR_HANDLE,
                        writeCmdReq.handleValPair.value.len,
                        writeCmdReq.handleValPair.value.val,
                        CYBLE_GATT_DB_PEER_INITIATED
                                    );
                currentTxmode =
writeCmdReq.handleValPair.value.val[0];

                UpdateTxPower(currentTxmode);
            }
            else // Invalid value. Write not permitted
            {
                SendErrorResponse    (

CYBLE_EDDYSTONE_CONFIGURATION_TX_POWER_MODE_CHAR_HANDLE,
                        CYBLE_GATT_ERR_WRITE_NOT_PERMITTED
                                    );
            }
        }
        // Beacon Period
        else if(writeCmdReq.handleValPair.attrHandle ==

CYBLE_EDDYSTONE_CONFIGURATION_BEACON_PERIOD_CHAR_HANDLE)
        {
            beaconPeriod =

CyBle_Get16ByPtr(writeCmdReq.handleValPair.value.val);

            // Disable URL FRAMES
            if(beaconPeriod == 0)
            {
                eddystoneImplenmentation = EDDYSTONE_UID;
                WriteAttributeValue (

CYBLE_EDDYSTONE_CONFIGURATION_BEACON_PERIOD_CHAR_HANDLE,
                        writeCmdReq.handleValPair.value.len,
                        writeCmdReq.handleValPair.value.val,
                        CYBLE_GATT_DB_PEER_INITIATED
                                    );
            }
            // Values in valid range
            else if((beaconPeriod >= MIN_BEACON_PERIOD) &&
                    (beaconPeriod <= MAX_BEACON_PERIOD))
```

```
            {
                WriteAttributeValue (

CYBLE_EDDYSTONE_CONFIGURATION_BEACON_PERIOD_CHAR_HANDLE,
                        writeCmdReq.handleValPair.value.len,
                        writeCmdReq.handleValPair.value.val,
                        CYBLE_GATT_DB_PEER_INITIATED
                                    );
                CurrentAdvPeriod = beaconPeriod / 0.625;
                eddystoneImplenmentation = EDDYSTONE_URL;
            }
            else
            {
                uint16 temp = MIN_BEACON_PERIOD;
                // Values not supportes. Write default values
                WriteAttributeValue(

CYBLE_EDDYSTONE_CONFIGURATION_BEACON_PERIOD_CHAR_HANDLE,
                        sizeof(temp),
                        (uint8 *)&temp,
                        CYBLE_GATT_DB_PEER_INITIATED);
                CurrentAdvPeriod =
CYBLE_GAP_ADV_ADVERT_INTERVAL_NONCON_MIN;
                eddystoneImplenmentation = EDDYSTONE_URL;
            }
        }
        // Reset the Configurations to default
        else if((writeCmdReq.handleValPair.attrHandle ==
                CYBLE_EDDYSTONE_CONFIGURATION_RESET_CHAR_HANDLE) &&
                (writeCmdReq.handleValPair.value.val[0] != 0))
        {
            ResetGattDb();
        }
    }
    else if(valuePairT.value.val[0] == LOCKED)
    {
        if(writeCmdReq.handleValPair.attrHandle ==

CYBLE_EDDYSTONE_CONFIGURATION_LOCK_CHAR_HANDLE)
        {
            // Accesing the lock in LOCKED state
            SendErrorResponse(writeCmdReq.handleValPair.attrHandle,

CYBLE_GATT_ERR_INSUFFICIENT_AUTHORIZATION);
        }
    }

    if(writeCmdReq.handleValPair.attrHandle ==

CYBLE_EDDYSTONE_CONFIGURATION_UNLOCK_CHAR_HANDLE)
    {
        if(writeCmdReq.handleValPair.value.len == LOCK_CODE_LENGTH)
        {
            if(valuePairT.value.val[0] == LOCKED)
            {
                int compareResult;
                valuePairT.attrHandle =

CYBLE_EDDYSTONE_CONFIGURATION_LOCK_CHAR_HANDLE;
                valuePairT.value.val = key_buf;
                valuePairT.value.len = sizeof(LOCK);
```

```
                CyBle_GattsReadAttributeValue(&valuePairT,
&cyBle_connHandle,

CYBLE_GATT_DB_LOCALLY_INITIATED);

                compareResult = memcmp   (
                                            valuePairT.value.val,

writeCmdReq.handleValPair.value.val,
                                            LOCK_CODE_LENGTH
                                        );

                if(compareResult == 0)
                {
                    status = UNLOCKED;
                    // Update the LOCK STATE
                    WriteAttributeValue (

CYBLE_EDDYSTONE_CONFIGURATION_LOCK_STATE_CHAR_HANDLE,
                        sizeof(bool), &status,
                        CYBLE_GATT_DB_LOCALLY_INITIATED
                                        );

                    // Reset the LOCK
                    WriteAttributeValue (

CYBLE_EDDYSTONE_CONFIGURATION_LOCK_CHAR_HANDLE,
                                    sizeof(LOCK), (uint8 *)LOCK,
                                    CYBLE_GATT_DB_LOCALLY_INITIATED
                                        );
                }
                else // LOCK not matched
                {

SendErrorResponse(writeCmdReq.handleValPair.attrHandle,

CYBLE_GATT_ERR_INSUFFICIENT_AUTHORIZATION);
                }
            }
        }
        else // Invalid length
        {
            SendErrorResponse(writeCmdReq.handleValPair.attrHandle,

CYBLE_GATT_ERR_INVALID_ATTRIBUTE_LEN);
        }
    }

    if (errorSent == false)
    {
        CyBle_GattsWriteRsp(cyBle_connHandle);
    }
}
```

```
/*******************************************************************
* Function Name: ConfigureAdvPacket
********************************************************************
*
* Summary:
*  Configures the Advertising data such that it transmits UID/URL and
TLM
*  frames
*
* Parameters:
*  bool:  true: configure adv parameters with UID/URL frames
*         false:configures the adv parameters to TLM frames
*
* Return:
*  None
*
*******************************************************************/
void ConfigureAdvPacket(void)
{
    uint16 CurrentEMG1,CurrentGrove1;
    uint16 CurrentEMG2,CurrentGrove2;

    uint8 CurrentPressure1;
    uint8 CurrentPressure2;

    //Recogida de los datos obtenidos del CAD
    CurrentEMG1=GetMeasuredEMG1();
    CurrentPressure1=GetMeasuredPressure1();
    CurrentGrove1=GetMeasuredGrove1();
    CurrentEMG2=GetMeasuredEMG2();
    CurrentPressure2=GetMeasuredPressure2();
    CurrentGrove2=GetMeasuredGrove2();

    // Configure Eddystone packets at run-time
    cyBle_discoveryModeInfo.advParam->advType =

CYBLE_GAPP_NON_CONNECTABLE_UNDIRECTED_ADV;

    if( (beaconCurrentRole == EDDYSTONE_UID) ||
        (beaconCurrentRole == EDDYSTONE_URL))
    {
        UID_LED_Write(LED_ON);

        // ADV packet timeout
        if (isEddystoneTLMPresent == true)
        {
            cyBle_discoveryModeInfo.advTo = APP_UID_URL_TIMEOUT;
        }
        else
        {
            cyBle_discoveryModeInfo.advTo = 0;  // No timeout
        }

        if(beaconCurrentRole == EDDYSTONE_UID)
        {
            // Service Data
            // Length
            cyBle_discoveryData.advData[7] = 0x17;
            // Signifies Eddystone UID
            cyBle_discoveryData.advData[11] = 0x00;
            // Ranging data: -14dB
```

```
            cyBle_discoveryData.advData[12] =

currentTxPowerLevels[currentTxmode];

            // SHA-1 hash of the FQDN (cypress.com) is calculated and
its
            // first 10 bytes are placed here as the Namespace ID, MSB
first
            cyBle_discoveryData.advData[13] =
                  (uint8)((CurrentGrove2 >> 8) & 0xFF);

            cyBle_discoveryData.advData[14] =
                  (uint8)((CurrentGrove2) & 0xFF);

            cyBle_discoveryData.advData[15] =
                  (uint8)((CurrentGrove1 >> 8) & 0xFF);

            cyBle_discoveryData.advData[16] =
                  (uint8)((CurrentGrove1) & 0xFF);

            cyBle_discoveryData.advData[17] =
                  (uint8)((CurrentEMG2 >> 8) & 0xFF);

            cyBle_discoveryData.advData[18] =
                  (uint8)((CurrentEMG2) & 0xFF);

            cyBle_discoveryData.advData[19] =
                  (uint8)((CurrentEMG1 >> 8) & 0xFF);

            cyBle_discoveryData.advData[20] =
                  (uint8)((CurrentEMG1) & 0xFF);

            cyBle_discoveryData.advData[21] = CurrentPressure2;
            cyBle_discoveryData.advData[22] = CurrentPressure1;

            // Instance ID - randomly created
            cyBle_discoveryData.advData[23] = 0x01;  // BID[0]
            cyBle_discoveryData.advData[24] = 0x00;  // BID[1]
            cyBle_discoveryData.advData[25] = 0x00;  // BID[2]
            cyBle_discoveryData.advData[26] = 0x00;  // BID[3]
            cyBle_discoveryData.advData[27] = 0x00;  // BID[4]
            cyBle_discoveryData.advData[28] = 0x00;  // BID[5]
            cyBle_discoveryData.advData[29] = 0x00;  // Reserved
            cyBle_discoveryData.advData[30] = 0x00;  // Reserved

            // ADV packet length
            cyBle_discoveryData.advDataLen = 31;
        }
    }

    //Update the advertisement interval
    cyBle_discoveryModeInfo.advParam->advIntvMin = CurrentAdvPeriod;
    cyBle_discoveryModeInfo.advParam->advIntvMax = CurrentAdvPeriod;
    cyBle_discoveryModeInfo.advData = &cyBle_discoveryData;
}
```

```
/*******************************************************************************
* Function Name: ConfigureConnAdvPacket
********************************************************************************
*
* Summary:
*  Configures the connectable Advertising data
*
* Parameters:
*  None
*
* Return:
*  None
*
*******************************************************************************/
void ConfigureConnAdvPacket(void)
{
    UID_LED_Write(LED_OFF);

    //Update the advertisement interval
    cyBle_discoveryModeInfo.advParam->advIntvMin =

CONNECTABLE_STATE_ADV_INTERVAL_MIN;
    cyBle_discoveryModeInfo.advParam->advIntvMax =

CONNECTABLE_STATE_ADV_INTERVAL_MAX;

    cyBle_discoveryModeInfo.advParam->advType =

CYBLE_GAPP_CONNECTABLE_UNDIRECTED_ADV;

    cyBle_discoveryModeInfo.advTo = CONNECTABLE_STATE_TIMEOUT;

    //Advertising data
    cyBle_discoveryModeInfo.advData = &CyBleConnectableAdvData;
}

/*******************************************************************************
* Function Name: EddystoneEventHandler
********************************************************************************
*
* Summary:
*   This is an event callback function to receive events from the
CYBLE
*   Component.
*
* Parameters:
*   uint8 event:       Event from the CYBLE component.
*   void* eventParams: A structure instance for corresponding event
type. The
*                      list of event structure is described in the
component
*                      datasheet.
* Return:
*   None
*******************************************************************************/
void EddystoneEventHandler(uint32 event, void* eventParam)
{
    CYBLE_API_RESULT_T apiResult;

    // To prevent compiler warning
    eventParam = eventParam;
```

```
    switch (event)
    {
        /*******************************************************
         *                       General Events
         *******************************************************/
        // This event is received when component is Started
        case CYBLE_EVT_STACK_ON:
            // Configure WDT counter 0 with 2 second interval
            WDT_Initialize(CY_SYS_WDT_COUNTER0,
TWO_SECOND_INTERRUPT_COUNT);

            // Enable WDT counter 0
            WDT_EnableCounter(CY_SYS_WDT_COUNTER0_MASK);

            // Ignore the initial delay. Start counter to track the
time since
            //  power ON
            SetEnableSecCnt(true);

            beaconCurrentRole = eddystoneImplenmentation;

ConfigureAdvPacket();//ConfigureAdvPacket(VoltsADC,VoltsP);

            /* Start advertisement */
            apiResult =
CyBle_GappStartAdvertisement(CYBLE_ADVERTISING_CUSTOM);
            if(apiResult != CYBLE_ERROR_OK)
            {
                CYASSERT(0);
            }
            break;
        case CYBLE_EVT_GAPP_ADVERTISEMENT_START_STOP:
            if(CyBle_GetState() != CYBLE_STATE_ADVERTISING)
            {
                /* On advertisement timeout, restart advertisement.
Before
                *  restarting previous type of advertisement, check if
the other
                *  type is triggered. If so, switch to the other type
of
                *  advertisement. */
                 ConfigureAdvPacket();
                 apiResult =

CyBle_GappStartAdvertisement(CYBLE_ADVERTISING_CUSTOM);

                 if(apiResult != CYBLE_ERROR_OK)
                 {
                     CYASSERT(0);
                 }
            }
            else
            {
                SetAdvPacketCount(GetAdvPacketCount() + 1);
            }
            break;
        case CYBLE_EVT_GAP_DEVICE_DISCONNECTED:

CyBle_GattsEnableAttribute(CYBLE_EDDYSTONE_SERVICE_HANDLE);
            beaconCurrentRole = eddystoneImplenmentation;
```

```
            ConfigureAdvPacket();
            CyBle_GappStartAdvertisement(CYBLE_ADVERTISING_CUSTOM);
            break;
        case CYBLE_EVT_GATTS_WRITE_REQ:
            ProcessWriteReq(*(CYBLE_GATTS_WRITE_CMD_REQ_PARAM_T*)
eventParam);
            break;
        default:
            break;
    }
}

/* [] END OF FILE */
```

3.3.6. Eddystone.h

```
/***************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : Eddystone.h
***************************************/

#ifndef __EDDYSTONE_H__
#define __EDDYSTONE_H__

#include <project.h>
#include <stdbool.h>

/***************************************************************************
* Macros and Constants
***************************************************************************/
 /* 65535 = 2 seconds */
#define TWO_SECOND_INTERRUPT_COUNT      (0xFFFF)
/* Default UID/URL Frame timeout */
#define APP_UID_URL_TIMEOUT             0x0001
/* Default TLM Frame timeout */
#define APP_TLM_TIMEOUT                 (0x0001)
/* Minimum supported beacon period */
#define MIN_BEACON_PERIOD
      (CYBLE_GAP_ADV_ADVERT_INTERVAL_NONCON_MIN * 0.625)
/* Maximum supported beacon period */
#define MAX_BEACON_PERIOD
      (CYBLE_GAP_ADV_ADVERT_INTERVAL_MAX * 0.625)
/* Default beacon period */
#define DEFAULT_BEACON_PERIOD           0x00A0

typedef enum
{
    /* Eddystone not active */
    NO_EDDYSTONE,
    /* Eddystone UID adv */
    EDDYSTONE_UID,
    /* Eddystone URL adv */
    EDDYSTONE_URL,
    /* Eddystone TLM adv */
    EDDYSTONE_TLM
} EDDYSTONE_ROLE_T;

typedef enum
{
    /* Characteristics unlocked */
    UNLOCKED,
    /* Characteristics locked */
    LOCKED
} EDDYSTONE_CHAR_STATE_T;

/* Default URL flag value */
#define DEFAULT_URL_FLAG_VALUE          0x01

#define PWR_LVL_3_DBM                   (0x03)  /*   3 dBm */
#define PWR_LVL_0_DBM                   (0x00)  /*   0 dBm */
#define PWR_LVL_NEG_6_DBM               (0xFA)  /*  -6 dBm */
#define PWR_LVL_NEG_18_DBM              (0xEE)  /* -18 dBm */
```

```
/* Index of the Advertised TX Power Levels */
typedef enum
{
    TX_POWER_MODE_LOWEST,
    TX_POWER_MODE_LOW,
    TX_POWER_MODE_MEDIUM,
    TX_POWER_MODE_HIGH,

    /* Maximum number of power levels */
    MAX_NUM_PWR_LVL
} TX_POWER_MODE_T;

/* URL Scheme Prefix */
typedef enum
{
    HTTP_WWW,        /* http://www.  */
    HTTPS_WWW,       /* https://www. */
    HTTP,            /* http://      */
    HTTPS,           /* https://     */
    URL_PREFIX_MAX
} EDDYSTONE_URL_SCHEME_PREFIX_T;

/* Eddystone-URL HTTP URL encoding */
typedef enum
{
    DOT_COM_SLASH,       /* .com/  */
    DOT_ORG_SLASH,       /* .org/  */
    DOT_EDU_SLASH,       /* .edu/  */
    DOT_NET_SLASH,       /* .bet/  */
    DOT_INFO_SLASH,      /* .info/ */
    DOT_BIZ_SLASH,       /* .biz/  */
    DOT_GOV_SLASH,       /* .gov/  */
    DOT_COM,             /* .com   */
    DOT_ORG,             /* .org   */
    DOT_EDU,             /* .edu   */
    DOT_NET,             /* .bet   */
    DOT_INFO,            /* .info  */
    DOT_BIZ,             /* .biz   */
    DOT_GOV,             /* .gov   */
    RESERVED
} EDDYSTONE_URL_HTTP_ENCODING_T;

/* Default URL advertised */
#define DEFAULT_URL                     {                   \
                                            HTTP_WWW,       \
                                            'c',            \
                                            'y',            \
                                            'p',            \
                                            'r',            \
                                            'e',            \
                                            's',            \
                                            's',            \
                                            DOT_COM_SLASH   \
                                        }

#define DEFAULT_URL_LENGTH              9
```

```
/*****************************************************************
* Function prototype
*****************************************************************/
void UpdateTLMAdvPacket(void);
void EddystoneEventHandler(uint32 event, void* eventParam);

#endif  /*  __EDDYSTONE_H__ */

/* [] END OF FILE */
```

3.3.7. WatchdogTimer.c

```
/*****************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : WatchdogTimer.c
*****************************************/

#include <Project.h>
#include "main.h"
#include "WatchdogTimer.h"

#define SEC_CNT_INC_PER_2SEC        (20u)

/*****************************************************************************
* Global variables
*****************************************************************************/
/* This flag when true indicates the BLE stack is on. */
static bool enableSecCnt = false;

/* True when counter1 interrupt is triggred atleast once */
static bool counter1TimedOut;

/* Keeps track of SEC_CNT feild of TLM packet. */
static uint32 SecCnt = 0;

/*****************************************************************************
* Function Name: SetEnableSecCnt
******************************************************************************
*
* Summary:
*  Enable or disable the increment of SEC_CNT feild of TLM packet.
*
* Parameters:
*  bool: 0 - Disable the counter
*        1 - Enable the counter
*
* Return:
*  None
*
*****************************************************************************/
void SetEnableSecCnt(bool value)
{
    enableSecCnt = value;
}

/*****************************************************************************
* Function Name: SetSecCnt
******************************************************************************
*
* Summary:
*  Sets value of SEC_CNT feild of TLM packet.
*
* Parameters:
*  uint32: value to initialize SecCnt
*
* Return:
*  None
*
*****************************************************************************/
```

```
void SetSecCnt(uint32 value)
{
    SecCnt = value;
}

/*******************************************************************
* Function Name: GetSecCnt
********************************************************************
*
* Summary:
*  Returns value of SEC_CNT feild of TLM packet.
*
* Parameters:
*  None
*
* Return:
*  uint32: value of SecCnt
*
*******************************************************************/
uint32 GetSecCnt(void)
{
    return SecCnt;
}

/*******************************************************************
* Function Name: WDT_Handler
********************************************************************
*
* Summary:
*  Watchdog timer(WDT) interrupt handler routine. WDT is used to
wakeup the
*  device after WCO or ECO has started and for advertisement payload
updates.
*
* Parameters:
*  None
*
* Return:
*  None
*
*******************************************************************/
CY_ISR(WDT_Handler)
{
    uint32 tempCnt;

    /* WDT interrupt is only used as a source of wakeup for PSoC 4 BLE
device
    *  in this example project. Clearing the WDT interrupt status is
all that is
    *  required in this example project
    */
    if(CySysWdtGetInterruptSource() & CY_SYS_WDT_COUNTER0_INT)
    {
        /* WDT counter is configured to trigger interrupt at every 2
seconds */
        if(enableSecCnt == true)
        {
            /* Time should be of 0.1 seconds(100ms) resolution. As
interrupt
            *  triggers at every ~2 seconds, hence 2000 / 100 = 20 */
            tempCnt = SecCnt + SEC_CNT_INC_PER_2SEC;
```

```
            /* On timer overflow reset both timer and packet count */
            if(tempCnt < SecCnt)
            {
                /* timeSincePowerOn is reset */
                SecCnt = 0;
                /* advPacketCount is reset */
                SetAdvPacketCount(0);
            }
            else
            {
                SecCnt = tempCnt;
            }
        }

        CySysWdtClearInterrupt(CY_SYS_WDT_COUNTER0_INT);
    }

    if(CySysWdtGetInterruptSource() & CY_SYS_WDT_COUNTER1_INT)
    {
        CySysWdtClearInterrupt(CY_SYS_WDT_COUNTER1_INT);
        counter1TimedOut = true;
    }
}

/*******************************************************************************
* Function Name: WDT_Initialize
********************************************************************************
*
* Summary:
*  Configures a watchdog counter with the given count and interrupt
period.
*
* Parameters:
*  uint32: counter number
*  uint32: set the period for the counter interrupt
*
* Return:
*  None
*
*******************************************************************************/
void WDT_Initialize(uint32 counterNum, uint32 period)
{
    /* Unlock the WDT registers for modification. Note that WDT is
running from
    *  ILO now */
    CySysWdtUnlock();

    /* Configure counter # in interrupt mode */
    CySysWdtWriteMode(counterNum, CY_SYS_WDT_MODE_INT);

    /* counter # with specified period */
    CySysWdtWriteClearOnMatch(counterNum, COUNTER_ENABLE);

    /* counter # with specified period */
    CySysWdtWriteMatch(counterNum, period);

    /* Lock WDT timer */
    CySysWdtLock();
}
```

```
/*******************************************************************************
* Function Name: WDT_EnableCounter
********************************************************************************
*
* Summary:
*  Enables WDT counter #
*
* Parameters:
*  uint32: counter mask
*
* Return:
*  None
*
*******************************************************************************/
void WDT_EnableCounter(uint32 counterMask)
{
    CySysWdtUnlock();

    CySysWdtEnable(counterMask);

    CySysWdtLock();
}

/*******************************************************************************
* Function Name: WDT_DisableCounter
********************************************************************************
*
* Summary:
*  Disable WDT counter #
*
* Parameters:
*  uint32: counter mask
*
* Return:
*  None
*
*******************************************************************************/
void WDT_DisableCounter(uint32 counterMask)
{
    CySysWdtUnlock();

    CySysWdtDisable(counterMask);

    CySysWdtLock();
}

/*******************************************************************************
* Function Name: LowPowerWait
********************************************************************************
*
* Summary:
*   This function waits in low power for a certain period.
*
* Parameters:
*  uint32: period to wait for while in low power state
*
* Return:
*  None
*
*******************************************************************************/
```

```
void LowPowerWait(uint32 period)
{
    /* Reset timeout flag */
    counter1TimedOut = false;

    /* Setup counter0 for ECO startup */
    WDT_Initialize(CY_SYS_WDT_COUNTER1, period);

    /* Enable WDT counter 1 */
    WDT_EnableCounter(CY_SYS_WDT_COUNTER1_MASK);

    do
    {
        /* Put CPU and BLESS to low power mode */
        LowPower();
    } while(counter1TimedOut == false);

    /* Disable counter 1 */
    WDT_DisableCounter(CY_SYS_WDT_COUNTER1_MASK);
}

/* [] END OF FILE */
```

3.3.8. WatchdogTimer.h

```
/*****************************************
* Project Name      : PSoC_4_BLE_Eddystone
* File Name         : WatchdogTimer.h
*****************************************/

/*****************************************************************************
* Description - Header file for Watchdog timer implementation routines
*****************************************************************************/

#ifndef __WATCHDOG_TIMER_H__
#define __WATCHDOG_TIMER_H__

#include <project.h>
#include <stdbool.h>

/*****************************************************************************
* Enums and macros
*****************************************************************************/
#define COUNTER_DISABLE             (0u)
#define COUNTER_ENABLE              (1u)

/*****************************************************************************
* Function declarations
*****************************************************************************/
void WDT_Initialize(uint32 counterNum, uint32 period);
void WDT_EnableCounter(uint32 counterMask);
void WDT_DisableCounter(uint32 counterMask);
void LowPowerWait(uint32 period);
void SetEnableSecCnt(bool value);
void SetSecCnt(uint32 value);
uint32 GetSecCnt(void);

CY_ISR_PROTO(WDT_Handler); /* WDT isr prototype declaration */

#endif /* __WATCHDOG_TIMER_H__ */

/* [] END OF FILE */
```

4. Datasheets

CY8CKIT-042-BLE-A

Bluetooth® Low Energy (BLE) Pioneer Kit Guide

Doc. # 002-11468 Rev. **

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1. Introduction

Thank you for your interest in the CY8CKIT-042-BLE-A Bluetooth® Low Energy (BLE) Pioneer Kit. The BLE Pioneer Kit enables customers to evaluate and develop BLE projects using the PSoC® 4 BLE and PRoC™ BLE (Programmable Radio-on-Chip) devices.

Bluetooth SMART™ or Bluetooth Low Energy (BLE) is a full-featured, layered, communication protocol that includes a 2.4-GHz radio, a link layer, and an application layer. However, you do not need to understand the complex protocol to implement your projects using PSoC 4 BLE or PRoC BLE. The Cypress BLE solution, which includes the device, the BLE Component, and the BLE firmware stack will take care of it for you. The Cypress BLE firmware stack is royalty free.

You will use two software tools, PSoC Creator™ and CySmart™ Central Emulation Tool, to develop and debug your BLE project. PSoC Creator is Cypress' standard integrated design environment (IDE). The BLE protocol has been abstracted into an easy drag-and-drop BLE Component in PSoC Creator. The CySmart Central Emulation Tool is a host tool for Windows PCs, which provides an easy-to-use GUI to enable customers to test and debug their BLE projects.

The BLE Pioneer Kit offers footprint-compatibility with Arduino™ shields as well as 6-pin Digilent® Pmod™ daughter cards. In addition, the kit features a CapSense® slider, an RGB LED, a push-button switch, an onboard programmer/debugger and the USB-UART/I^2C bridge functionality block (KitProg), a coin cell battery holder, and a Cypress F-RAM™. The BLE Pioneer Kit supports 1.9 V, 3 V, 3.3 V, or 5 V as operating voltages. The BLE Pioneer Kit supports two devices:

- PSoC 4 BLE is a 32-bit, 48-MHz ARM® Cortex®-M0 BLE solution with CapSense, 12-bit analog front end (1x SAR ADC, 4x low-power opamps, 2x low-power comparators, and 2x current DACs), 4x TCPWM[1], 2x SCBs[2], 4x UDBs[3], LCD[4], I^2S[5], and 36 GPIOs. PSoC 4 BLE provides a complete solution for sports and fitness monitors, wearable electronics, medical devices, home automation systems, and sensor-based low-power systems for the Internet of Things (IoT).
- PRoC BLE is a 32-bit, 48-MHz ARM Cortex-M0 BLE solution with CapSense, 12-bit ADC, 4x TCPWM[1], 2x SCBs[2], LCD[4], I^2S[5], and 36 GPIOs. PRoC BLE provides a complete solution for BLE connectivity, HID, remote controls, and toys.

Two different versions of the BLE Pioneer Kit are currently available. These kits differ in the BLE modules and the dongle that are included. The baseboard in both kits are identical, so any BLE module can be used interchangeably with either baseboard. Table 1-1 lists the modules and dongle included in each kit.

Table 1-1. Default BLE Modules and BLE Dongle in the Two BLE Pioneer Kits

Kit	PSoC Module	PRoC Module	Dongle	Flash Size	Bluetooth Version
CY8CKIT-042-BLE	CY8CKIT-142	CY5671	CY5670	128 KB	4.1
CY8CKIT-042-BLE-A	CY8CKIT-143A	CY5676A	CY5677	256 KB	4.1 and 4.2

1. Configurable timer, counter, and pulse-width modulator.
2. Serial communication blocks (configurable to I^2C, SPI, or UART).
3. Universal digital blocks
4. Configurable liquid crystal display driver.
5. Configurable integrated interchip sound serial bus interface.

1.1 Kit Contents

The BLE Pioneer Kit contains the following items (see Figure 1-1):

- BLE Pioneer Baseboard preloaded with the CY8CKIT-143A PSoC 4 BLE 256KB Module
- CY5676A PRoC BLE 256KB Module
- CY5677 CySmart BLE 4.2 USB Dongle (BLE Dongle)
- Quick start guide
- USB Standard-A to Mini-B cable
- Four jumper wires (4 inch) and two proximity sensor wires (5 inch)
- Coin cell (3-V CR2032)

Figure 1-1. Kit Contents

If any part of the BLE Pioneer Kit is missing, contact your nearest Cypress sales office for help: www.cypress.com/go/support.

1.2 BLE Pioneer Baseboard Details

The BLE Pioneer Baseboard consists of the blocks shown in Figure 1-2.

1. RGB LED
2. BLE device reset button
3. CapSense proximity header
4. User button
5. CapSense slider
6. Arduino-compatible I/O headers (J2/J3/J4)
7. Arduino-compatible power header (J1)
8. Digilent Pmod-compatible I/O header (J5)
9. Cypress F-RAM 1 Mb (FM24V10-G)
10. PSoC 5LP I/O header (J8)
11. PSoC 5LP programmer and debugger (CY8C5868LTI-LP039)
12. Coin cell holder (bottom side)
13. USB connector (J13)
14. Power LED and Status LED
15. System power supply jumper (J16) - LDO 1.9 V~5 V
16. BLE power supply jumper / current measurement (J15)
17. BLE module headers (J10/J11)

Figure 1-2. BLE Pioneer Baseboard

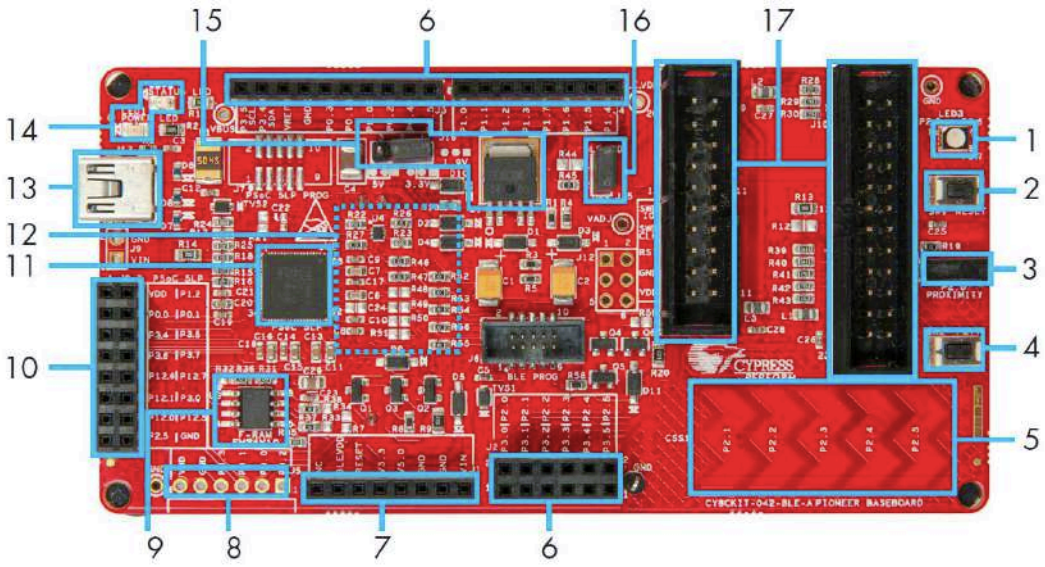


Figure 1-3 shows a markup of the onboard components of the PSoC 4 BLE module (in red) and the PRoC BLE module (in black). See BLE Modules and BLE Dongles Compatible with the BLE Pioneer Kit on page 128 for more details. Figure 1-4 shows the BLE Dongle board blocks.

Figure 1-3. BLE Module Markup

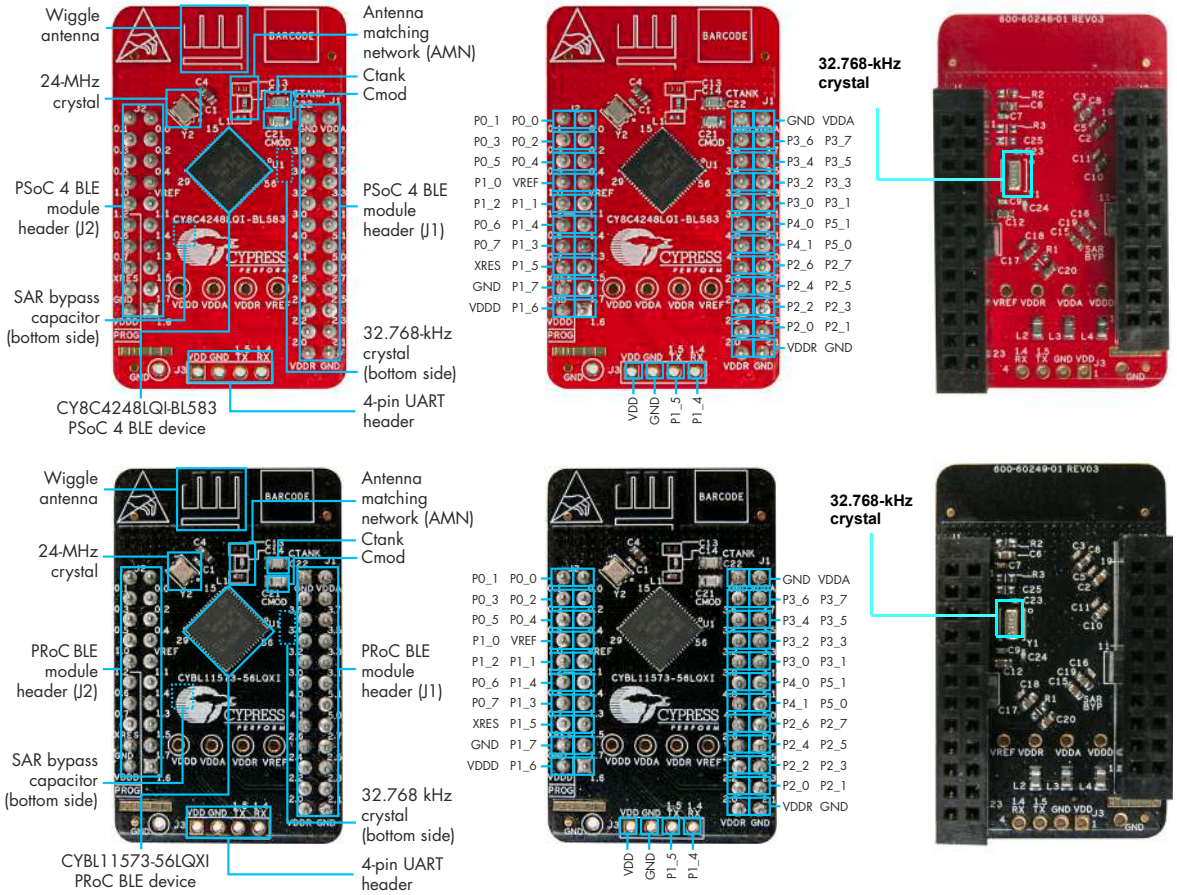
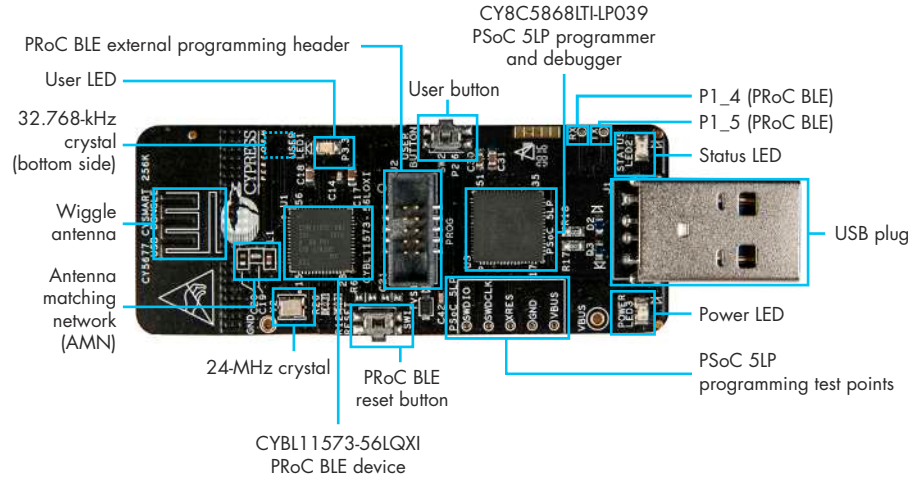


Figure 1-4. BLE Dongle Markup



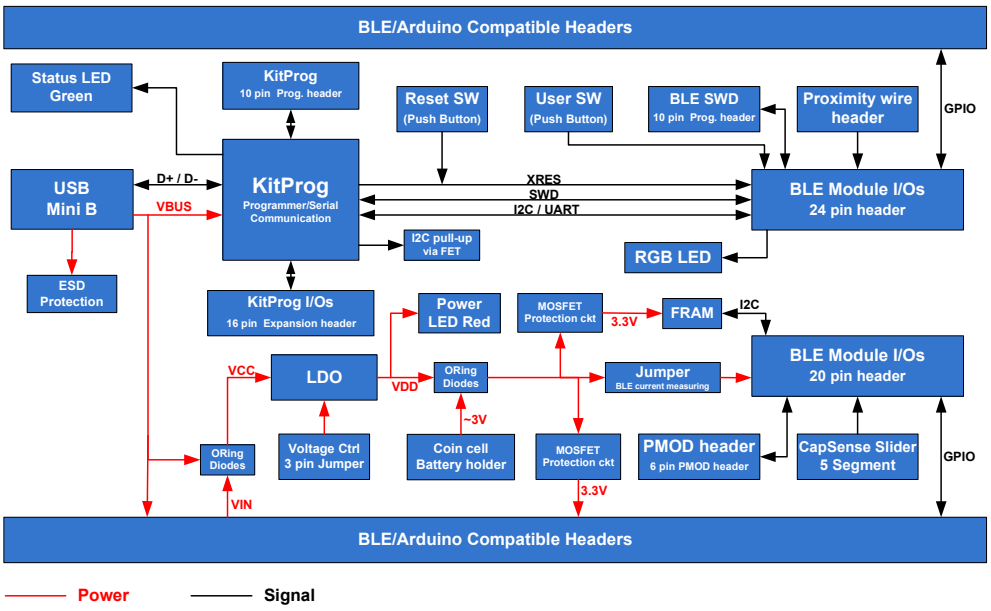
3. Kit Operation

This chapter introduces you to the BLE Pioneer Kit and the features that will be used as part of its operation. We will discuss features such as USB connection, programming/debugging, and programmer firmware update. The chapter also describes the USB-UART and USB-I^{2}C bridges along with the PC tools that can be used to communicate with the BLE device on the BLE Pioneer Kit.

3.1 Theory of Operation

Figure 3-1, Figure 3-2, and Figure 3-3 show the block diagrams for the BLE Pioneer Baseboard, PSoC 4 BLE/PRoC BLE Module, and BLE Dongle.

Figure 3-1. BLE Pioneer Baseboard Block Diagram

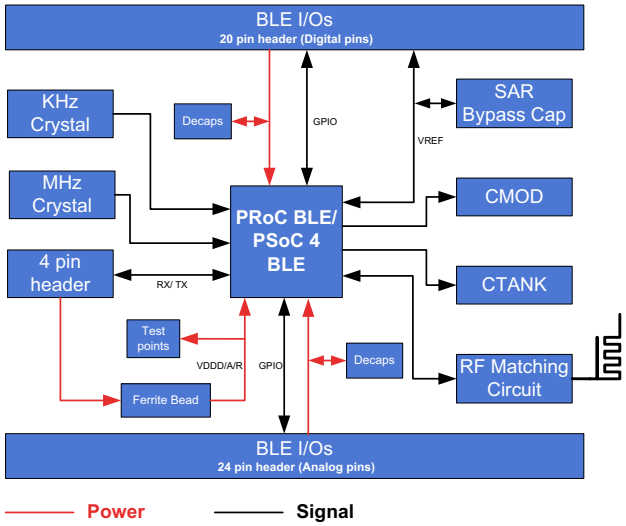


The BLE Pioneer Baseboard acts as the baseboard for the PSoC 4 BLE (red module) and PRoC BLE (black module). The BLE Pioneer Baseboard contains a PSoC 5LP device, that has KitProg firmware, used as an onboard programmer or debugger, and for the USB-Serial interface.

The baseboard is Arduino form-factor compatible, enabling Arduino shields to be connected on top of the board to extend the functionality of BLE modules. The board also features a 1-Mb F-RAM, an RGB LED, a five-segment CapSense slider, a proximity header, a user switch, and a reset switch for the PSoC 4 BLE and PRoC BLE devices on the module. The Pioneer board supports three voltage levels: 1.9 V, 3.3 V, and 5 V.

The BLE Pioneer Baseboard can also be used as a standalone programmer to program and debug other BLE devices using SWD, and as a USB-Serial interface. The KitProg firmware on PSoC 5LP device enables bootloading PSoC 5LP over USB to upgrade the firmware.

Figure 3-2. PSoC 4 BLE/PRoC BLE Module Block Diagram

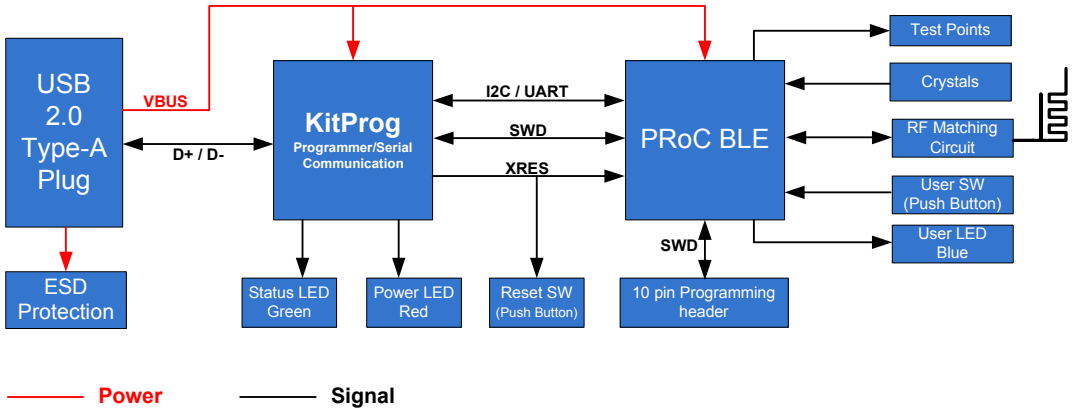


This BLE Pioneer Kit includes two modules. These modules act as a basic breakout board for the CY8C4248LQI-BL583 (PSoC 4 BLE) and CYBL11573-56LQXI (PRoC BLE) device. The PSoC 4 BLE and PRoC BLE Modules are identical except for the BLE device. Besides these two modules, there are additional modules available, which can be ordered separately. The complete list is available in BLE Modules and BLE Dongles Compatible with the BLE Pioneer Kit on page 128.

The BLE Dongle is the wireless interface for the CySmart Central Emulation Tool. It has a PRoC BLE device for BLE communication and KitProg for onboard programming, debugging, and for the USB-Serial interface, as shown in Figure 3-3.

The BLE Dongle has a USB Type-A plug to connect the KitProg to the USB port of the host computer. The KitProg then communicates with the PRoC BLE device over UART or multiplexed I^2C or an SPI bus. The BLE Dongle also features a user LED, a user switch, and a reset switch for the PRoC BLE device. The dongle is powered directly through the USB port (VBUS) at 5.0 V.

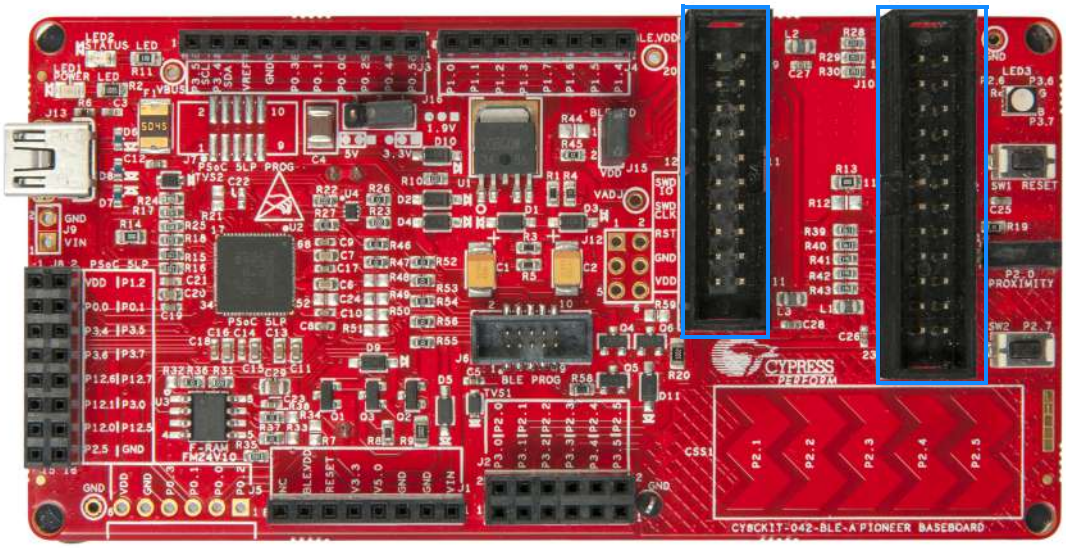
Figure 3-3. BLE Dongle Block Diagram



3.4 Placing Modules on Baseboard

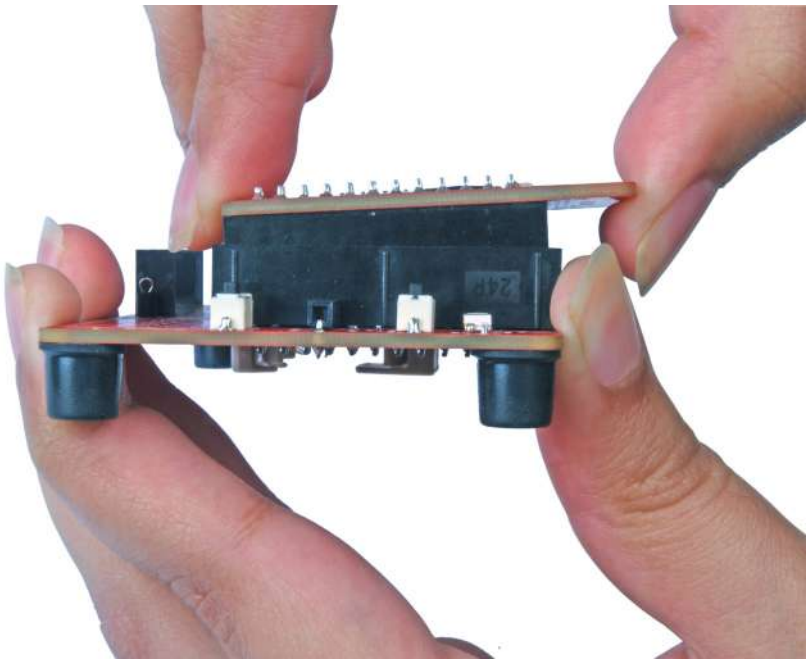
Plug the module into the BLE Pioneer Baseboard on headers J10 and J11, while keeping the antenna directed outside. Note that the two parallel headers J10 and J11 are not equal (24-pin and 20-pin, respectively) and will not allow the module to be inserted in the opposite direction.

Figure 3-5. Baseboard with J10 and J11 Headers to Connect Modules



To remove the modules from the BLE Pioneer Kit, hold the BLE Pioneer Kit in one hand and the module in the other, as shown in Figure 3-6, and pull it out using a rocking motion.

Figure 3-6. Remove Module Connected on BLE Pioneer Kit



3.5 Programming and Debugging BLE Device

The BLE Pioneer Kit and BLE Dongle can be programmed and debugged using the KitProg. Before programming the device, ensure that PSoC Creator and PSoC Programmer are installed on the computer. See Install Software on page 19 for more information.

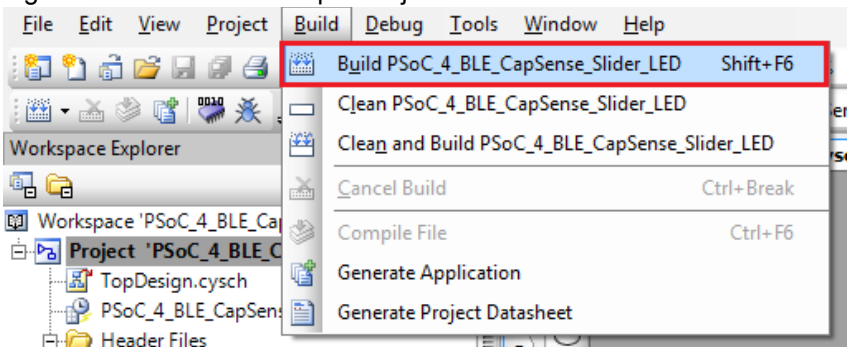
3.5.1 Programming using PSoC Creator

1. Connect the BLE Pioneer Kit/BLE Dongle to the computer's USB port, as shown in Figure 3-7.

Figure 3-7. Connect USB Cable to J13

2. Load the desired example project in PSoC Creator from **File** > **Open** > **Project/Workspace**.
3. Build the project by choosing **Build** > **Build <Project Name>** or **[Shift] [F6]**, as shown in Figure 3-8.

Figure 3-8. Build an Example Project



4. If there are no errors during build, program the firmware by clicking the **Program** button on the tool bar or pressing **[Ctrl] [F5]**, as shown in Figure 3-9. This will program the device on the BLE Pioneer Kit/BLE Dongle and it will be ready for use.

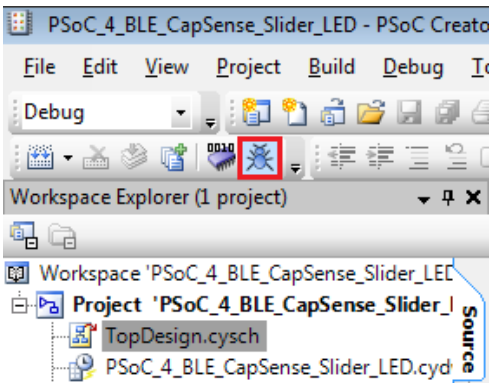
Figure 3-9. Programming Device From PSoC Creator

3.5.2 Debugging using PSoC Creator

For debugging the project using PSoC Creator, follow steps 1 to 5 from Programming using PSoC Creator on page 27 followed by:

1. Click the **Debug** icon or press **[F5]**, as shown in Figure 3-10.

Figure 3-10. Start Debug on PSoC Creator



2. When PSoC Creator opens in debug mode, use the buttons on the toolbar for debugging.

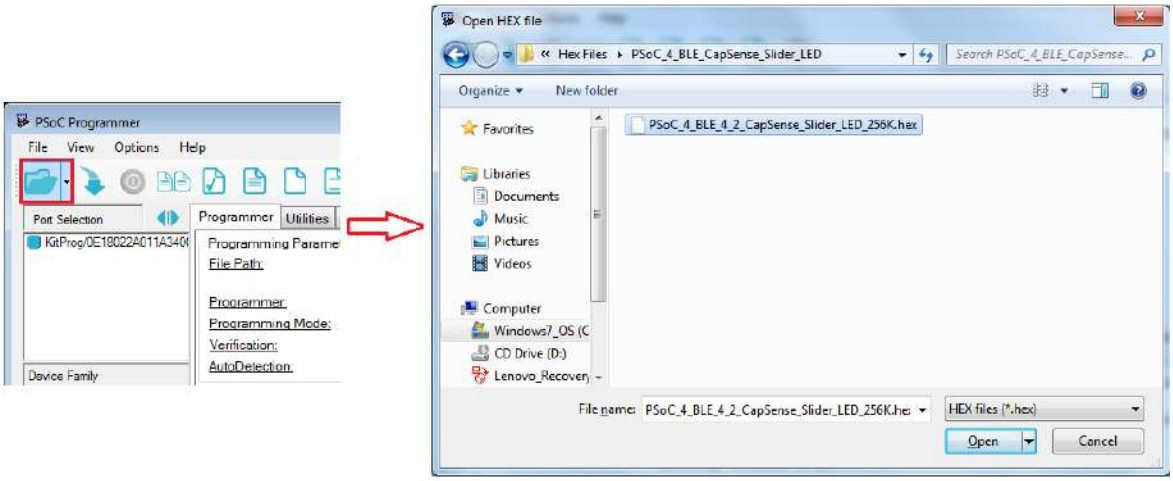
For more details on using the debug features, see the Cypress application note Getting Started with PSoC 4 BLE.

3.5.3 Programming using PSoC Programmer

PSoC Programmer (3.24 or later) can be used to program existing hex files into both BLE Pioneer Kit or BLE Dongle. To do this, follow these steps.

1. Connect the BLE Pioneer Kit or BLE Dongle to a computer and open PSoC Programmer from **Start** > **All Programs** > **Cypress** > **PSoC Programmer <version>** > **PSoC Programmer <version>**.
2. Click the **File Load** button at the top left corner of the window. Browse for the desired hex file and click **Open**.

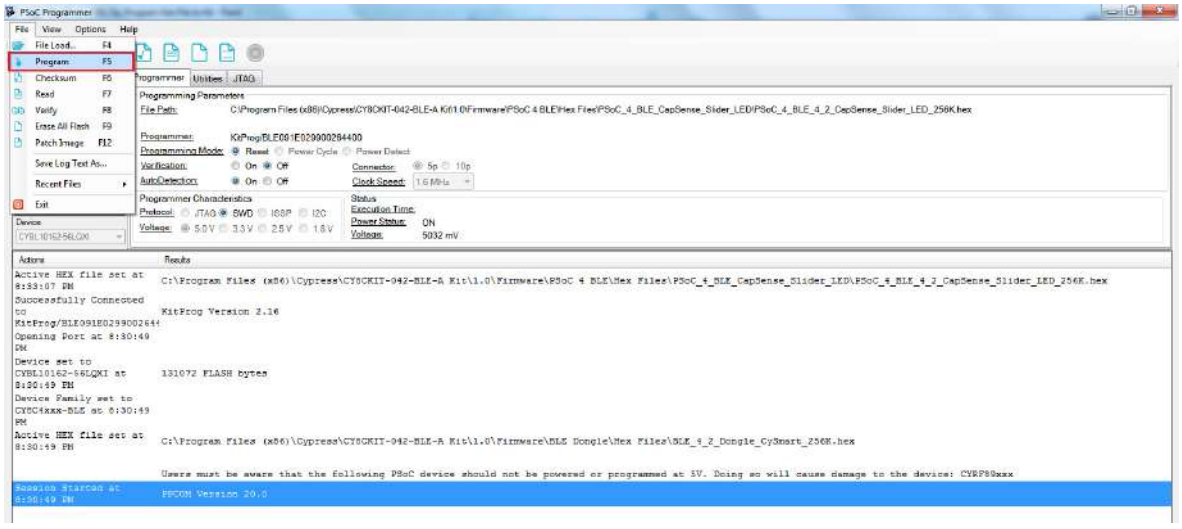
Figure 3-11. Select Hex File



3. Go to **File** > **Program** to start programing the kit with the selected file.

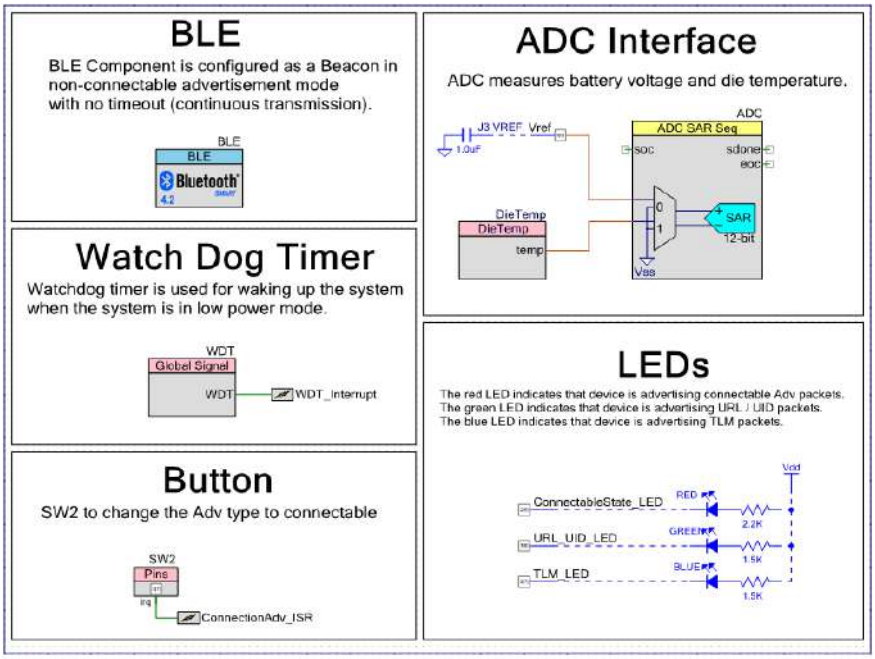
   Note: If the hex file does not match the device selected, then PSoC Programmer will throw an error of device mismatch and terminate programming.

Figure 3-12. Program Hex File to Kit



4. When the programming is finished successfully, indicated by a PASS message on the status bar, the BLE Pioneer Kit/BLE Dongle is ready for use. Close PSoC Programmer.

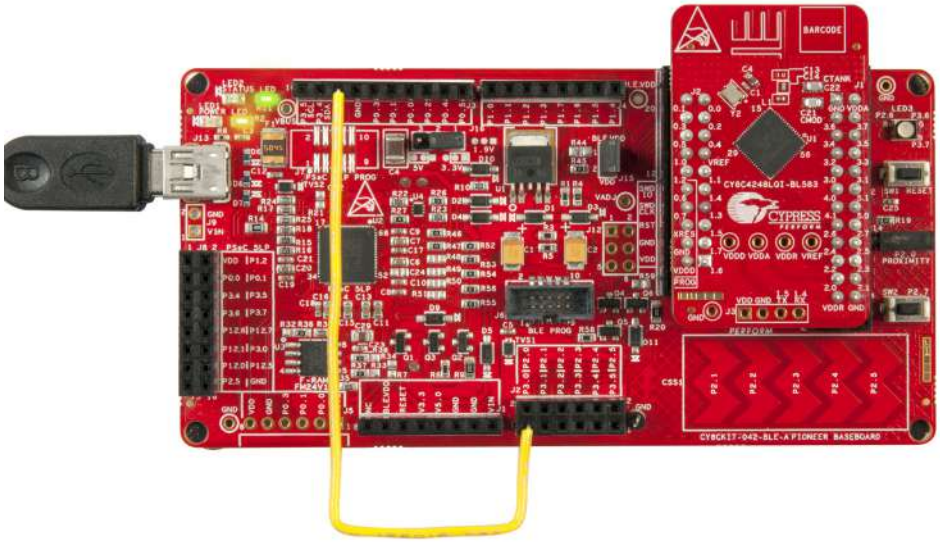
Figure 4-60. Top Design for PSoC_4_BLE_Eddystone and PRoC_BLE_Eddystone Project



4.5.2 Hardware Connection

- Ensure that the correct module is placed on the baseboard corresponding to the project being used. PSoC_4_BLE_Eddystone works with the PSoC 4 BLE Module. PRoC_BLE_Eddystone works with the PRoC BLE Module.
- Connect a wire (provided as part of this kit) between VREF (connector J3) and P3.0 (connector J2) on the baseboard (see Figure 4-61).

Figure 4-61. VREF (J3) and P3.0 (J2) Connectors on BLE Pioneer Kit with PSoC 4 BLE Module



The pin assignment for this project is in *PSoC_4_BLE_Eddystone.cydwr* or *PRoC_BLE_Eddystone.cydwr* in the Workspace Explorer, as shown in Figure 4-62.

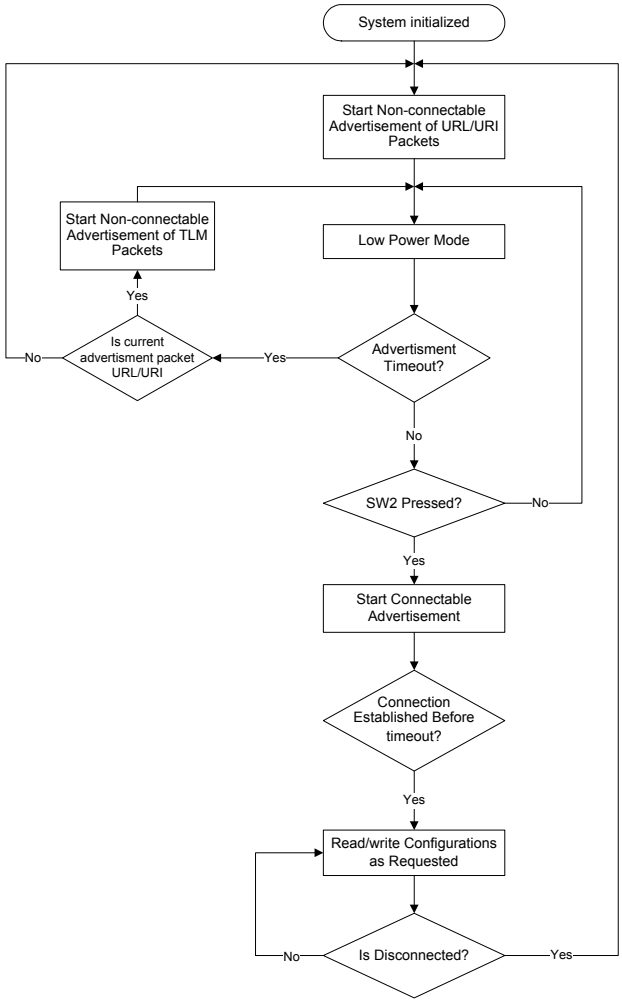
Figure 4-62. Pin Selection for Eddystone Project

	Name	Port	Pin	Lock
	ConnectableState_LED	P2[6]	43	☑
	SW2	P2[7]	44	☑
	TLM_LED	P3[7]	54	☑
	URL_UID_LED	P3[6]	53	☑
	Vref	P3[0]	47	☑

4.5.3 Flow Chart

Figure 4-63 shows the flow chart of code implemented.

Figure 4-63. Eddystone Project Flow Chart



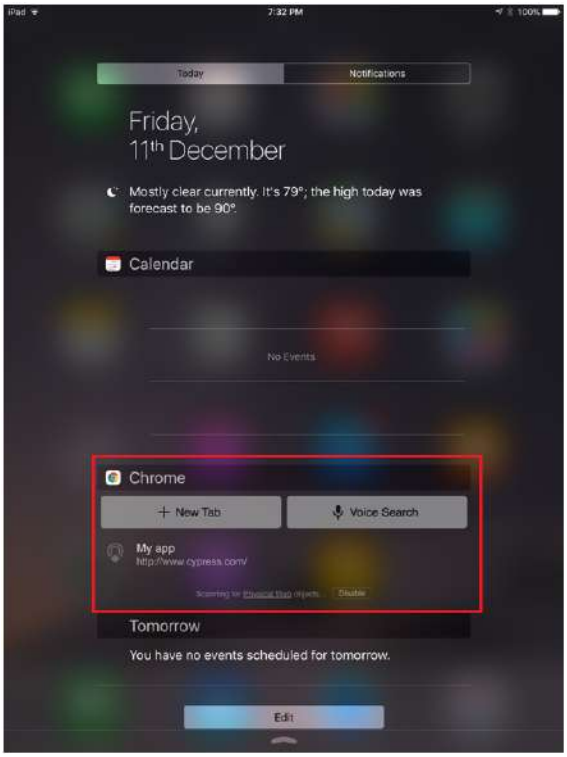
4.5.4 Verify Output

The project can be verified using an Android smart phone or an iOS device (iPhone or iPad). Before proceeding further make sure that a beacon application (such as Locate Beacon for Android or Chrome browser for iOS) and the CySmart app are installed on the smart phone/device. Also make sure that Bluetooth is turned on in the device, and you have a working internet connection.

To verify the Eddystone project in iOS, using Chrome for iOS browser, follow these steps. Before you start, make sure the Chrome browser for iOS is installed in your iOS device and the Chrome widget is added to the widgets view.

1. Place the module on the BLE Pioneer Kit, depending on the project chosen.
2. Power the BLE Pioneer Kit through the USB connector J13.
3. Program the BLE Pioneer Kit with the Eddystone example project. Follow steps in Using Example Projects on page 35 to program the device.
4. After programming successfully, the firmware starts the non-connectable advertisement of UID/URL and TLM packets. Advertisement of UID/URL packets is indicated by the green LED and TLM packets is indicated by blue LED on the baseboard.
5. Pull down the notification area. You should be able to see the link in the notification area as shown in Figure 4-64 on page 76

Figure 4-64. iOS Notification Shade Showing the Beacon Advertised Web Link



6. Touching the link will take you to the website.

To verify the Eddystone project in Android devices using the Locate Beacon application, follow these steps.

1. Place the module on the BLE Pioneer Kit, depending on the project chosen.
2. Power the BLE Pioneer Kit through the USB connector J13.
3. Program the BLE Pioneer Kit with the Eddystone example project. Follow steps in Using Example Projects on page 35 to program the device.
4. After programming successfully, the firmware starts the non-connectable advertisement of UID/URL and TLM packets. Advertisement of UID/URL packets is indicated by the green LED and TLM packets is indicated by blue LED on the baseboard.
5. Launch the **Locate** application on the smart phone/device.

6. Click the **Locate Beacons** button to start scanning for beacons (see Figure 4-65).

Figure 4-65. Locate Beacon App Home Screen

7. In the next screen a list of **Visible Beacons** will be displayed. Click the desired beacon (see Figure 4-66) to display its status and information (see Figure 4-67).

Figure 4-66. Locate Beacon App Showing Discovered Beacons

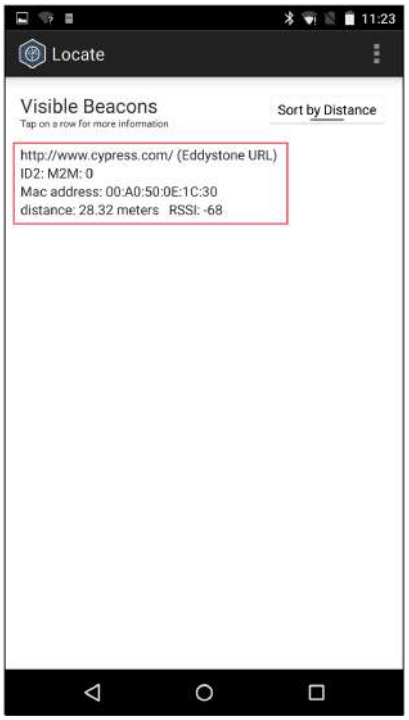


Figure 4-67. Locate Beacon Showing Details about Selected Beacon

To read and write characteristics (using an Android or iOS device, and CySmart app) of the beacon follow these steps.

1. Press **SW2** on the BLE Pioneer Kit baseboard to start the connectable advertisement. The advertisement state is indicated by the red LED.
2. Launch the CySmart app on your Android smart phone/device.
3. Connect to the **CY Eddystone** device from the list by clicking on it (see Figure 4-68).

5. Hardware

This chapter describes the contents of the BLE Pioneer Kit hardware and its different blocks, such as the power block, USB connection, Arduino-compatible headers, module connectors, and CapSense slider.

The schematic and board layouts are available at the following location:
`<Install_Directory>\Cypress\CY8CKIT-042-BLE-A Kit\<version>\Hardware`.

5.1 BLE Pioneer Baseboard

5.1.1 PSoC 5LP

An onboard PSoC 5LP contains the KitProg, which is used to program and debug the BLE device. The PSoC 5LP connects to the USB port of the computer through a USB Mini-B connector and to the SWD interface of the BLE device. PSoC 5LP is a true system-level solution providing MCU, memory, analog, and digital peripheral functions in a single chip. The CY8C58LPxx family offers a modern method of signal acquisition, signal processing, and control with high accuracy, high bandwidth, and high flexibility. The analog capability spans the range from thermocouples (near DC voltages) to ultrasonic signals.

For more information, visit the PSoC 5LP web page.

See Serial Interconnection between KitProg and Module on page 103 for more details.

5.1.2 Power System

The power supply system on the BLE Pioneer Baseboard is versatile, allowing the input supply to come from the following sources:

- 5-V power from the onboard USB connector
- 5-V to 12-V VIN power from the Arduino power header (J1)
- 3-V from the CR2032 coin cell

An adjustable LDO is used to output three different voltage levels (1.9 V, 3.3 V, and 5 V) to power the module. These voltages are selected with the J16 jumper, as shown in Figure 5-1.

Figure 5-1. Schematics and Board Highlight of LDO and Power Selection Jumper

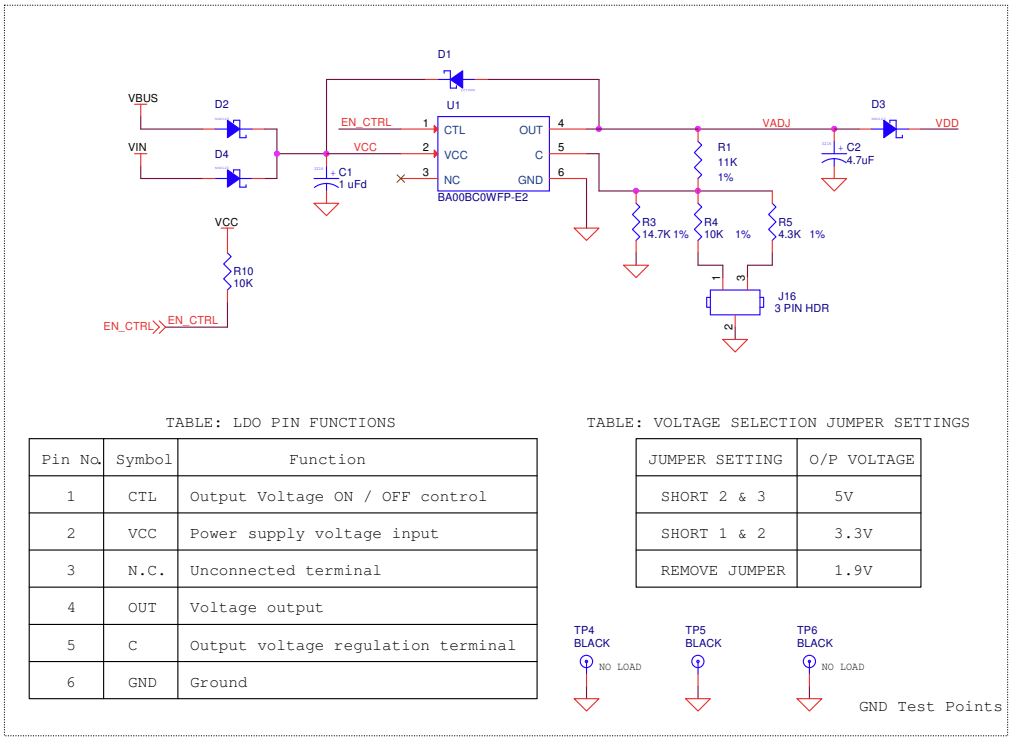
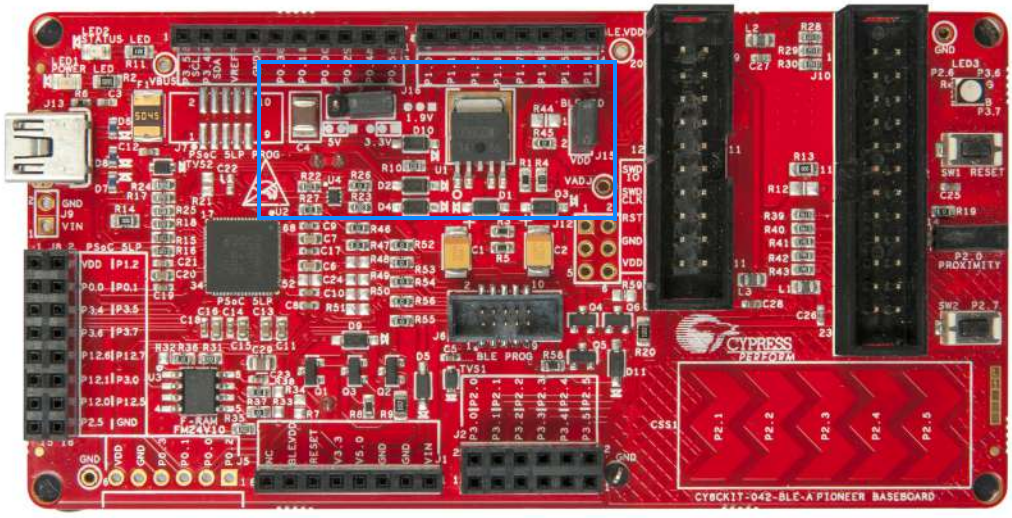


TABLE: LDO PIN FUNCTIONS

Pin No.	Symbol	Function
1	CTL	Output Voltage ON / OFF control
2	VCC	Power supply voltage input
3	N.C.	Unconnected terminal
4	OUT	Voltage output
5	C	Output voltage regulation terminal
6	GND	Ground

TABLE: VOLTAGE SELECTION JUMPER SETTINGS

JUMPER SETTING	O/P VOLTAGE
SHORT 2 & 3	5V
SHORT 1 & 2	3.3V
REMOVE JUMPER	1.9V

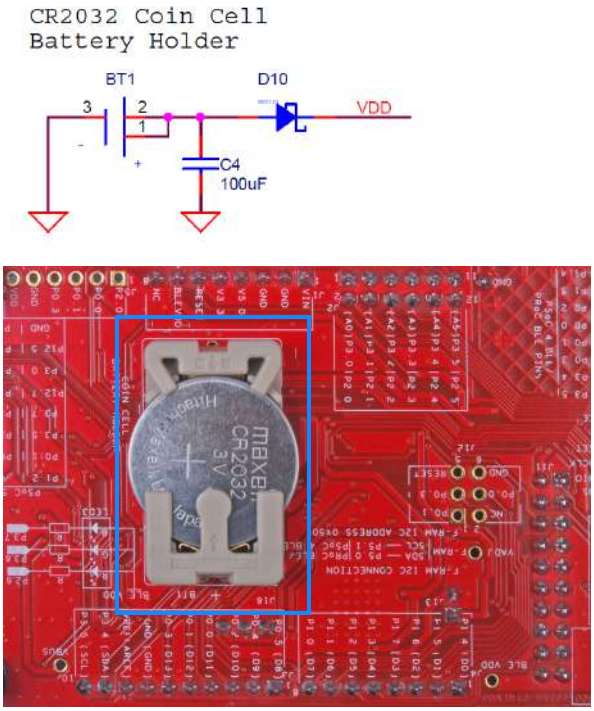


The input to the LDO can come from either the USB, the VIN pin in the Arduino header J1, or header J9.

Note: The typical dropout voltage of the selected LDO is 0.3 V at 500-mA output current. This gives a minimum output of 4.6 V from the input voltage of 5 V from the VBUS. This drop also considers the voltage drop across the Schottky diode connected at the output of the LDO to protect against voltage applied at the output terminal of the regulator. An input voltage supply over 12 V can damage the board.

The BLE Pioneer Baseboard also contains a CR2032 coin cell holder to power it using a coin cell, as shown in Figure 5-2.

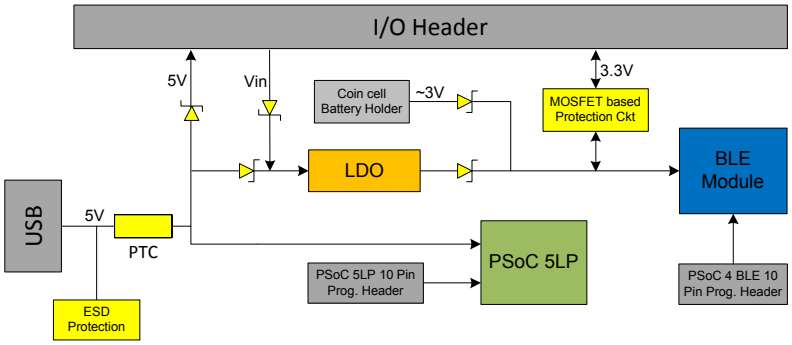
Figure 5-2. Schematics and Board Highlight of Coin Cell Holder



5.1.2.1 *Protection Circuits*

The power supply rail has reverse-voltage, overvoltage, short circuits, and excess current protection features, as shown in Figure 5-3.

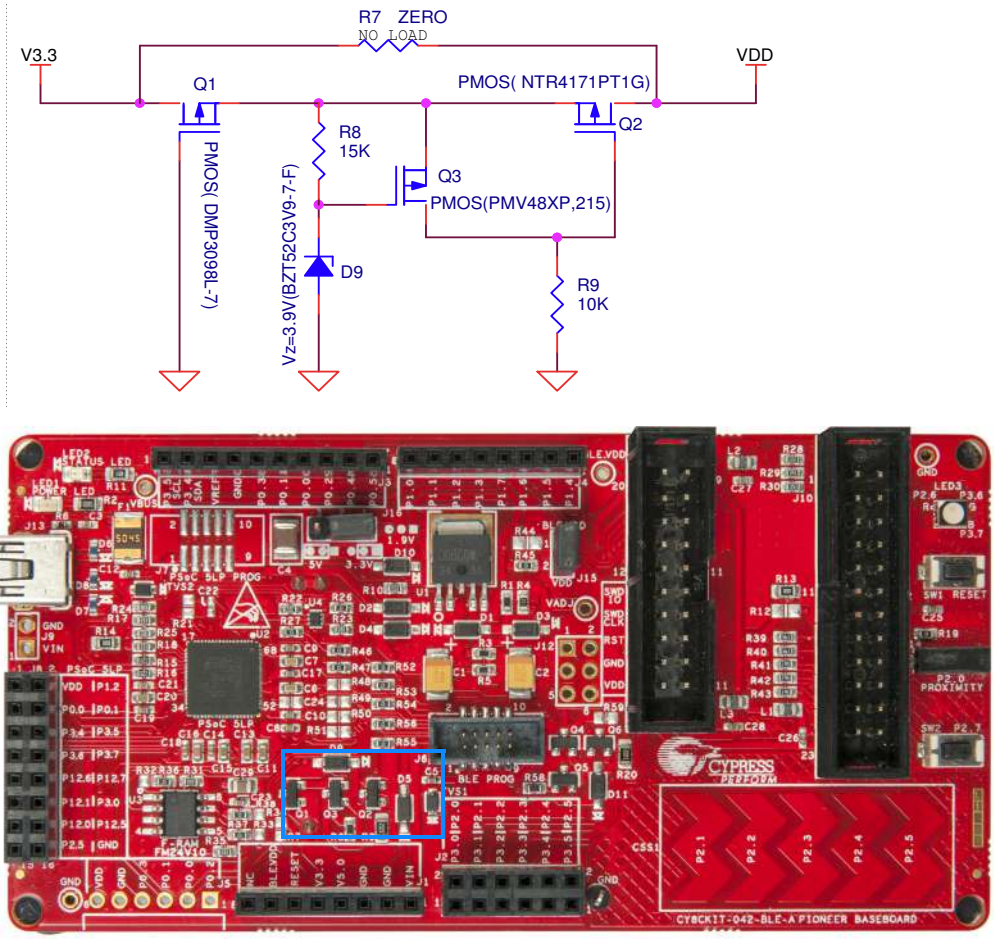
Figure 5-3. Power Supply Block Diagram With Protection Circuits



- A PTC resettable fuse is connected to protect the computer's USB ports from shorts and overcurrent.
- ORing diodes prevent damage to components when the BLE Pioneer Baseboard is powered from different voltage sources at the same time.
- ESD protection is provided for the USB Mini-B connector.

- A MOSFET-based protection circuit is provided for overvoltage and reverse-voltage protection for the 3.3-V rail from J1.5, as shown in Figure 5-4.

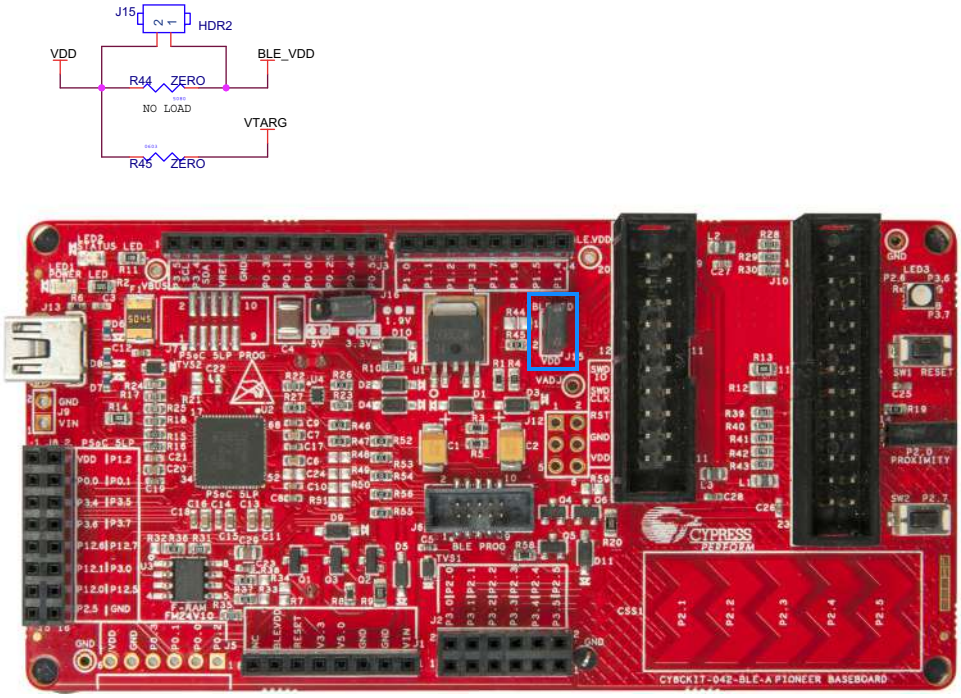
Figure 5-4. Schematics and Board Highlight of MOSFET Protection Circuit for 3.3-V Rail from J1.5



5.1.2.2 *Current Measurement Jumper*

To demonstrate the low power consumption of PSoC 4 BLE/PRoC BLE Module, a two-pin header (J15) is populated in series with the power supply to the module. This can be used to measure current using an ammeter without the need to desolder any component from the BLE Pioneer Baseboard, as shown in Figure 5-5.

Figure 5-5. Schematics and Board Highlight of Current Measurement Jumper

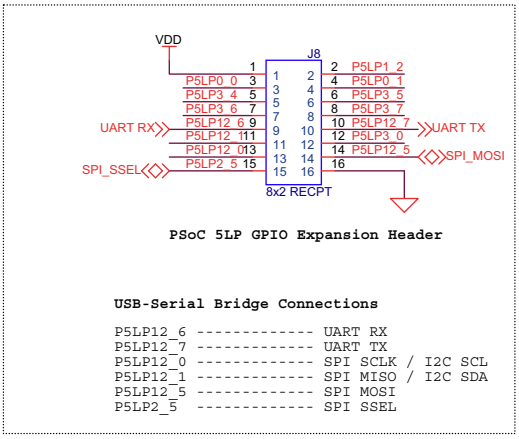


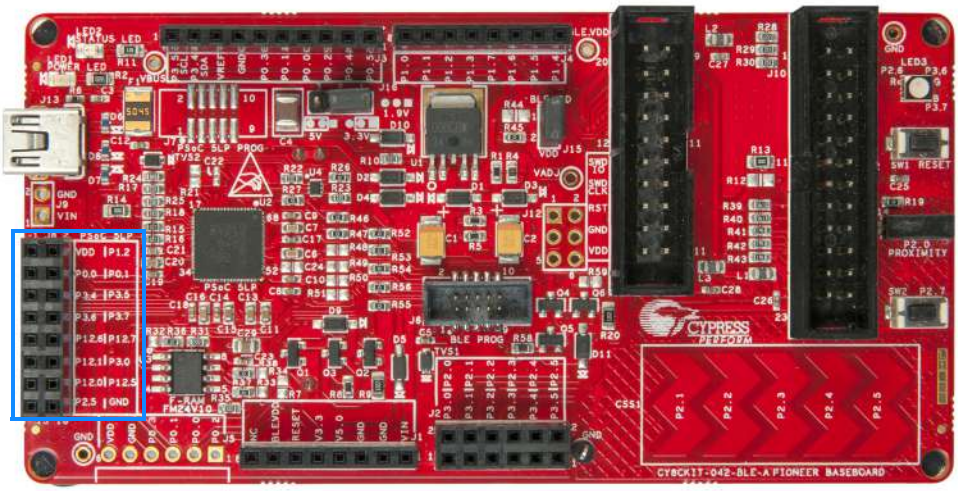
5.1.4.3 PSoC 5LP GPIO Header (J8)

An 8×2 header is provided on the BLE Pioneer Baseboard to pull out several pins of PSoC 5LP to support advanced features such as a low-speed oscilloscope and a low-speed digital logic analyzer (see Figure 5-11). This header also contains the USB-Serial interface pins that can be used when these pins are not accessible on the Arduino headers because a shield is connected.

Note: You can use PSoC 5LP for your own custom firmware.

Figure 5-11. Schematics and Board Highlight of PSoC 5LP GPIO Expansion Header

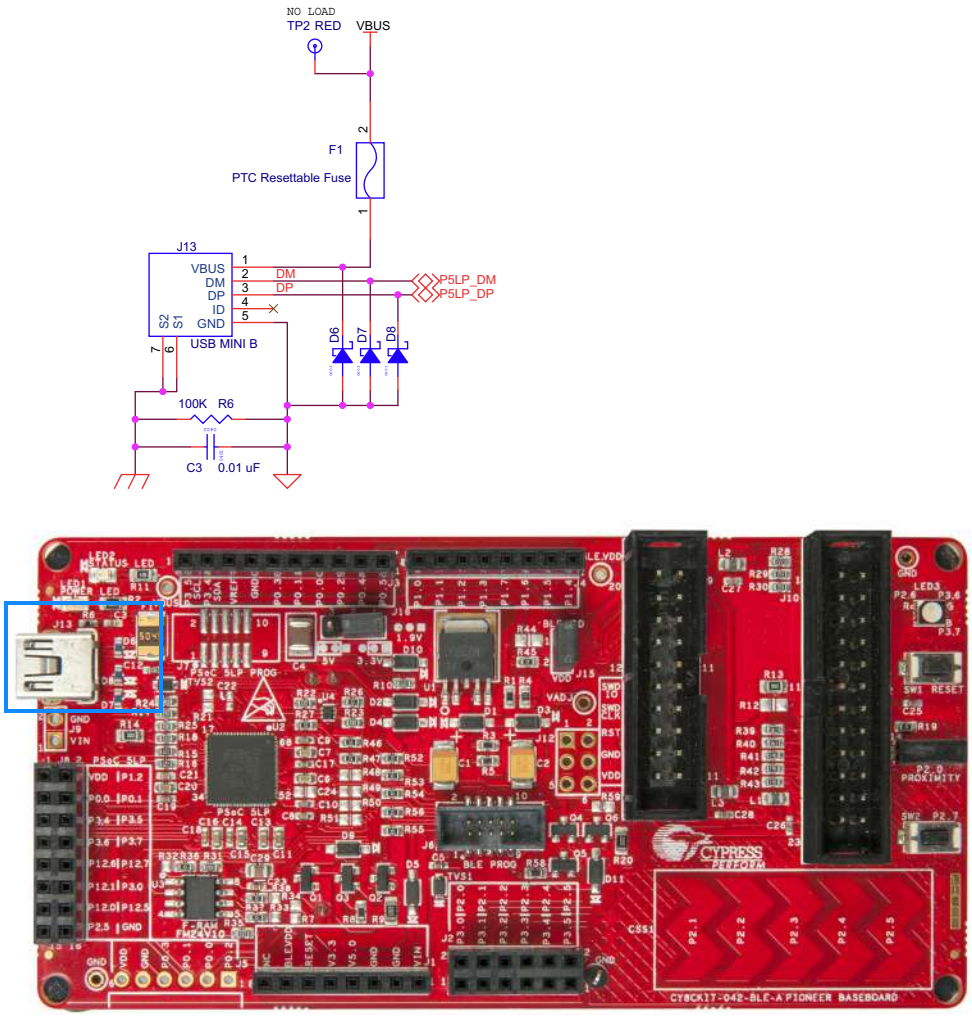




5.1.5 USB Mini-B Connector

The PSoC 5LP connects to the USB port of a computer through a Mini-B connector (see Figure 5-12), which can also be used to power the BLE Pineer Baseboard. A resettable polyfuse is used to protect the computer's USB ports from shorts and overcurrent. If more than 500 mA is drawn from the USB port, the fuse will automatically break the connection until the short or overload is removed.

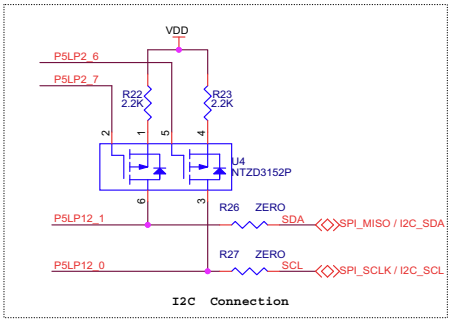
Figure 5-12. Schematics and Board Highlight of USB Mini-B Connector

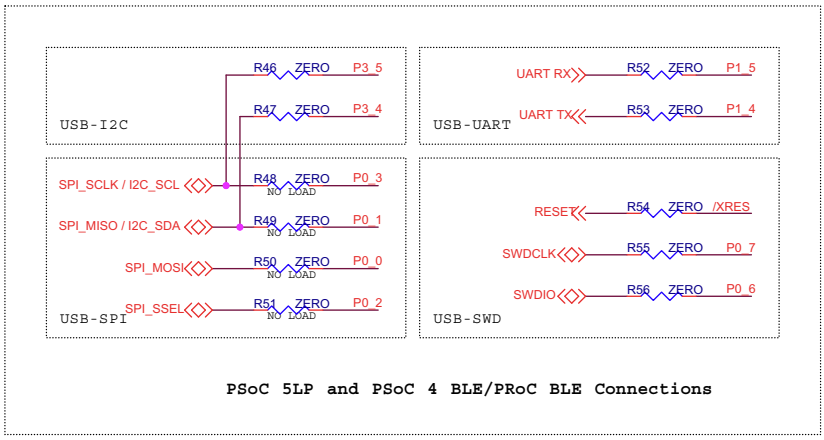


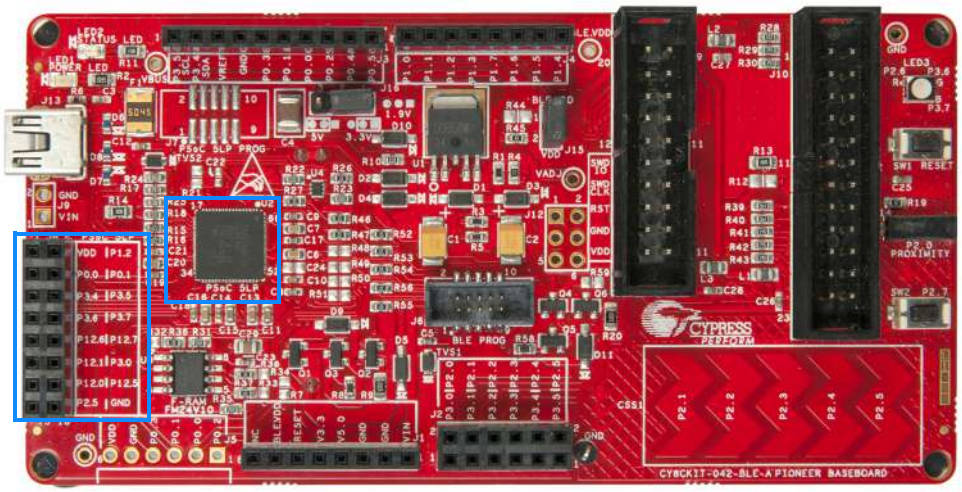
5.1.10 Serial Interconnection between KitProg and Module

The KitProg is also a USB-Serial interface. It supports USB-UART and USB-I^{2}C bridges (see Figure 5-19). The pull-up resistors on the I^{2}C bus are enabled when the protocol is selected from the user interface (such as Bridge Control Panel). The USB-Serial pins of the KitProg are also available on the Arduino header; therefore, it can be used to control Arduino shields with the SPI/I^{2}C/UART interface. Refer USB-UART Bridge on page 32 and USB-I2C Bridge on page 33 for more information on how to use these serial interconnections.

Figure 5-19. Schematics and Board Highlight of Serial Interface and I^{2}C Pull-Up via FET



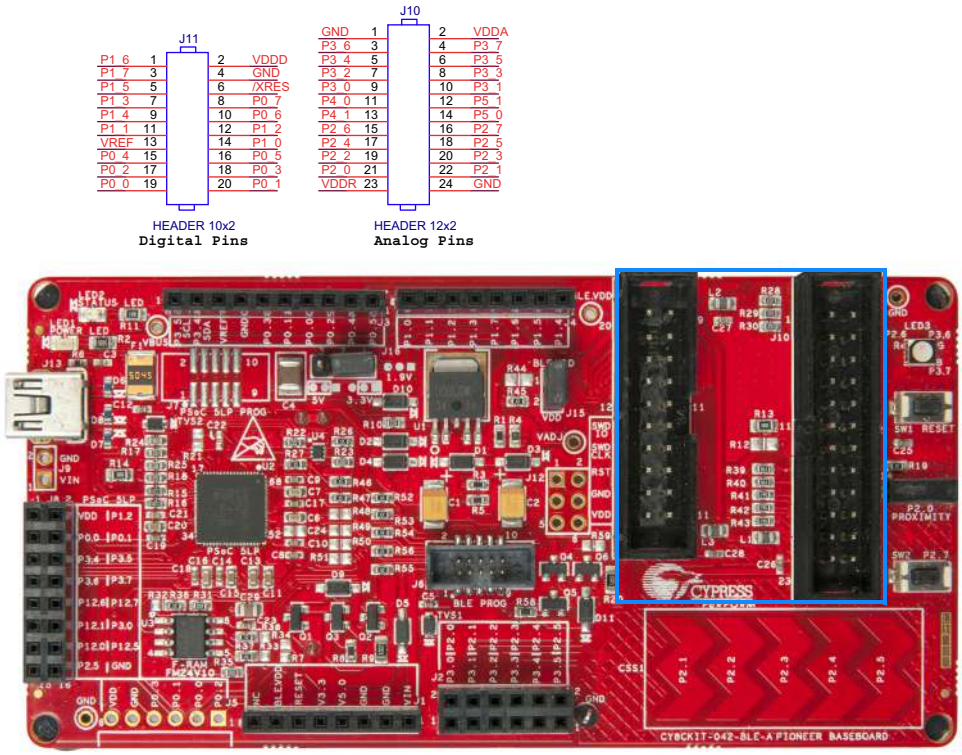




5.1.11 Module Headers

The PSoC 4 BLE and PRoC BLE Modules are connected to the BLE Pioneer Baseboard using the two (24-pin and 20-pin) module headers, as shown in Figure 5-20.

Figure 5-20. Schematics and Board Highlight of Module Headers



For information on how to add these on your own board, refer to Adding BLE Module-Compatible Headers on Your Baseboard on page 126.

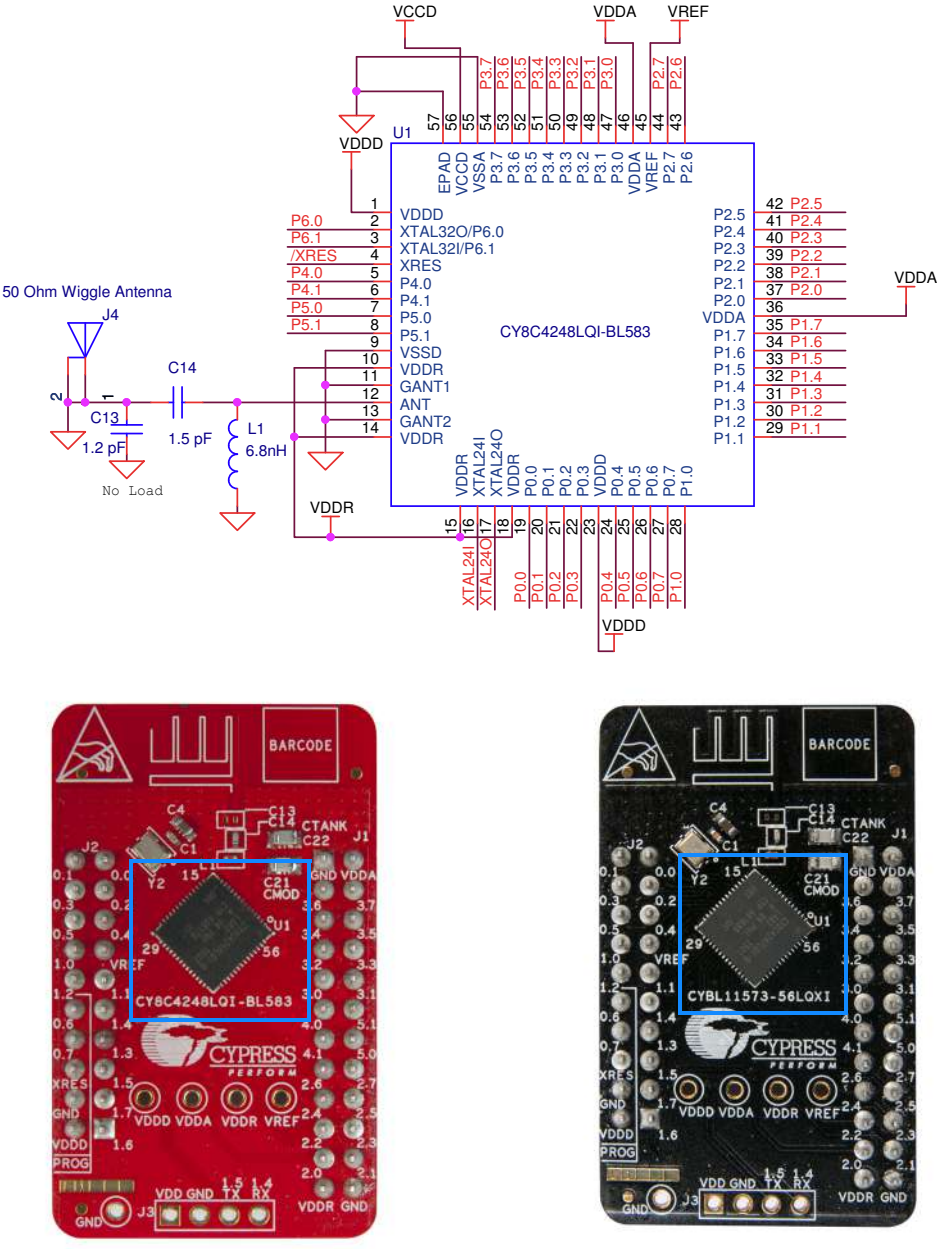
5.2 Module Board

5.2.1 PSoC 4 BLE or PRoC BLE Device

The PRoC BLE or PSoC 4 BLE device is the main component on the module. It provides the RF interface and analog and digital capability. The PRoC BLE or PSoC 4 BLE pins are mapped to the module headers (see Figure 5-21). For more information, refer to the BLE web page.

See BLE Modules and BLE Dongles Compatible with the BLE Pioneer Kit on page 128 for details.

Figure 5-21. Schematics and Board Highlight of Module Headers for BLE Pins

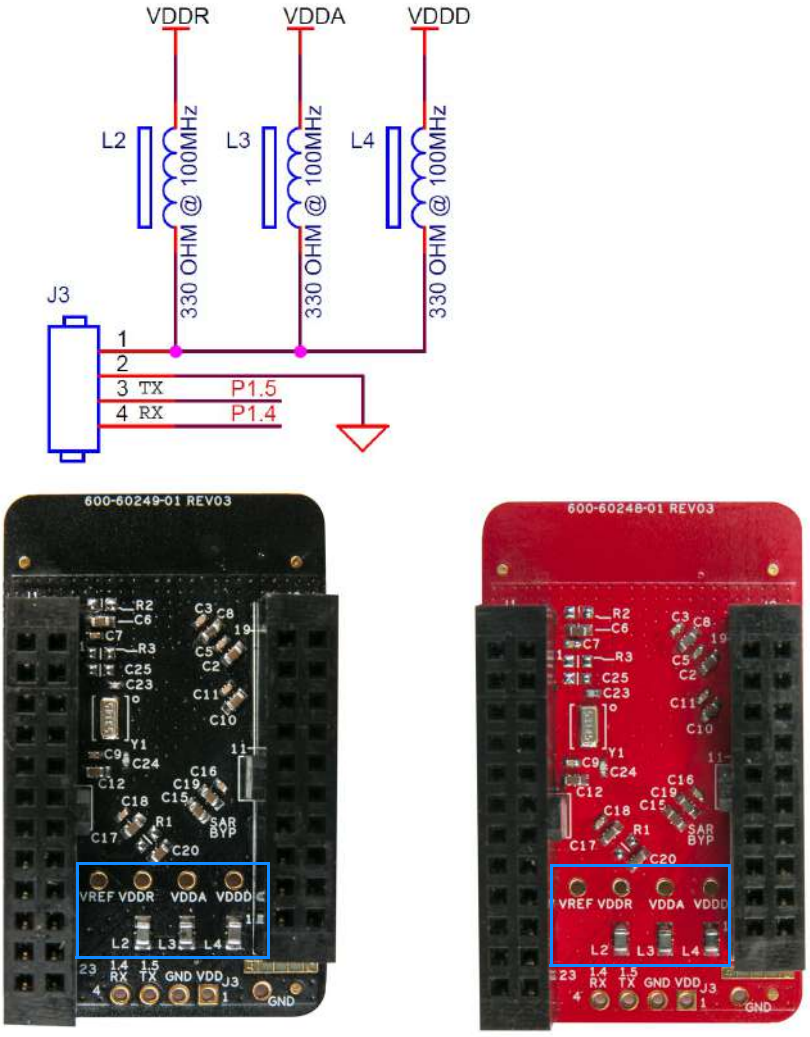


5.2.2 Module Power Connections

The module has three power domains: VDDD, VDDA, and VDDR. The VDDD connection supplies power for digital device operation, VDDA supplies power for analog device operation, and VDDR connection supplies power for the device radio. By default, these domains are shorted using a 330-ohm, 100-MHz ferrite bead. The domains are shorted for standalone usage scenarios of module, such as programming the module using MiniProg 3 or using the module as a standalone data acquisition unit.

It is recommended to place the ferrite bead between the supply to avoid ripple between VDDR and the other two domains. If the supply ripple is less that 100 mV, these can be changed to a zero-ohm resistor.

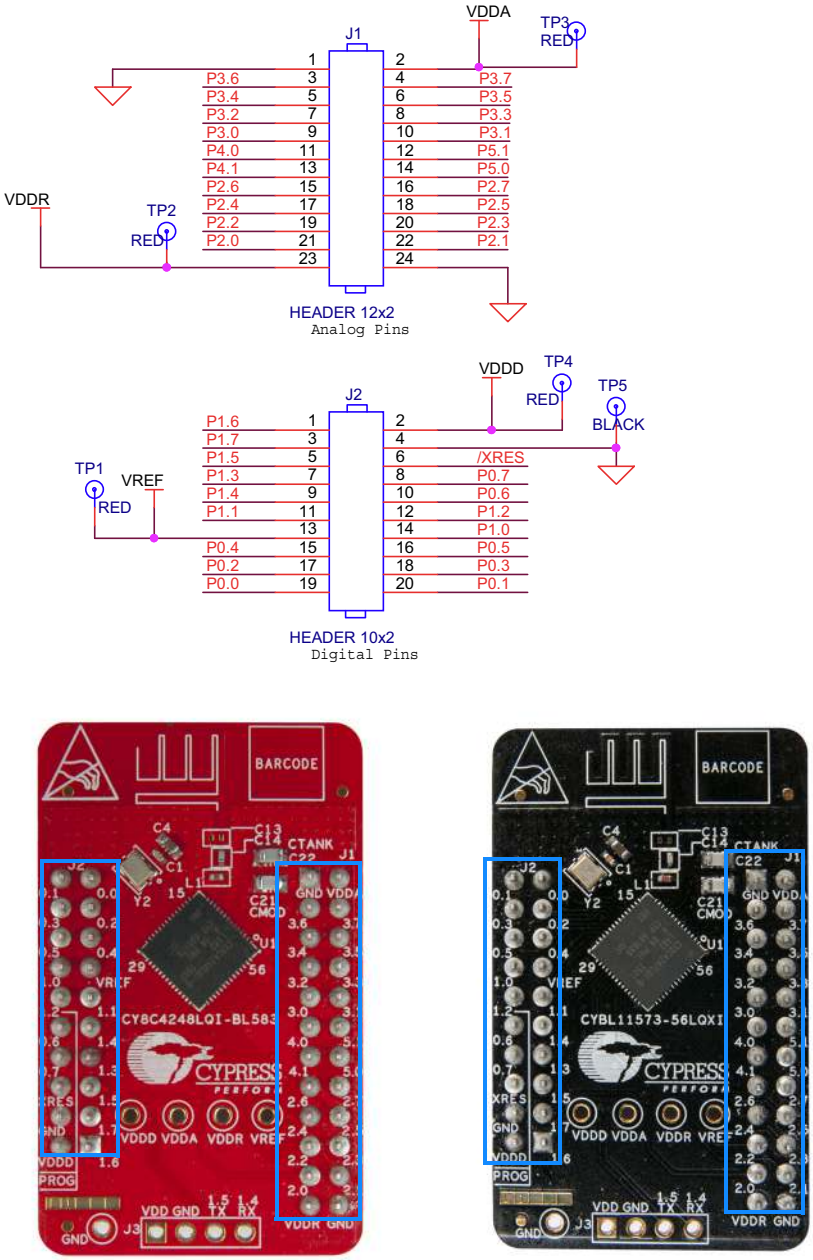
Figure 5-22. Schematics and Board Highlight of Ferrite Bead and Power Pin



5.2.3 Module Headers (20-Pin and 24-Pin Headers)

The PSoC 4 BLE and PRoC BLE Modules connect to the BLE Pioneer Baseboard using two (20-pin and 24-pin) module headers (Figure 5-23). All GPIOs and power domains are brought out to these headers. These headers are the counterparts of the connectors in Expansion Connectors on page 94.

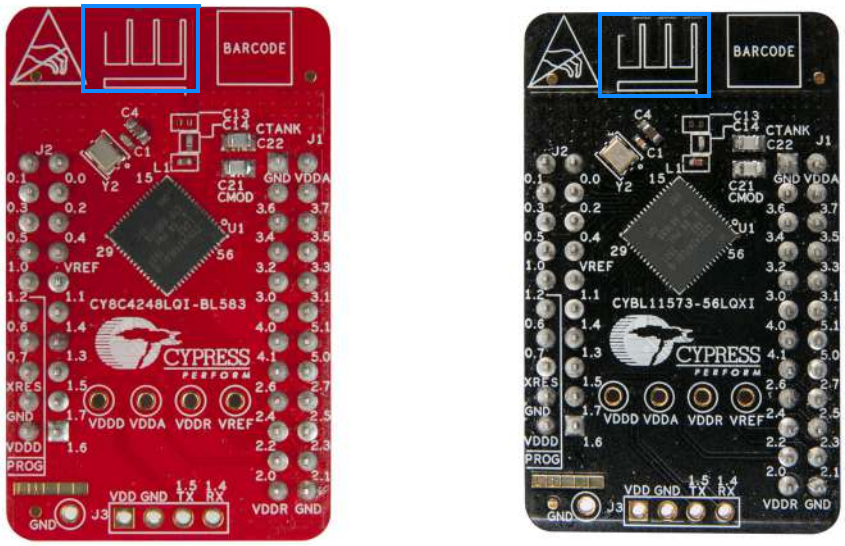
Figure 5-23. Schematics and Board Highlight of Headers



5.2.4 Wiggle Antenna

Both the modules use the wiggle antenna. Refer to the Antenna Design Guide (AN91445) for details.

Figure 5-24. Board Highlight of Wiggle Antenna

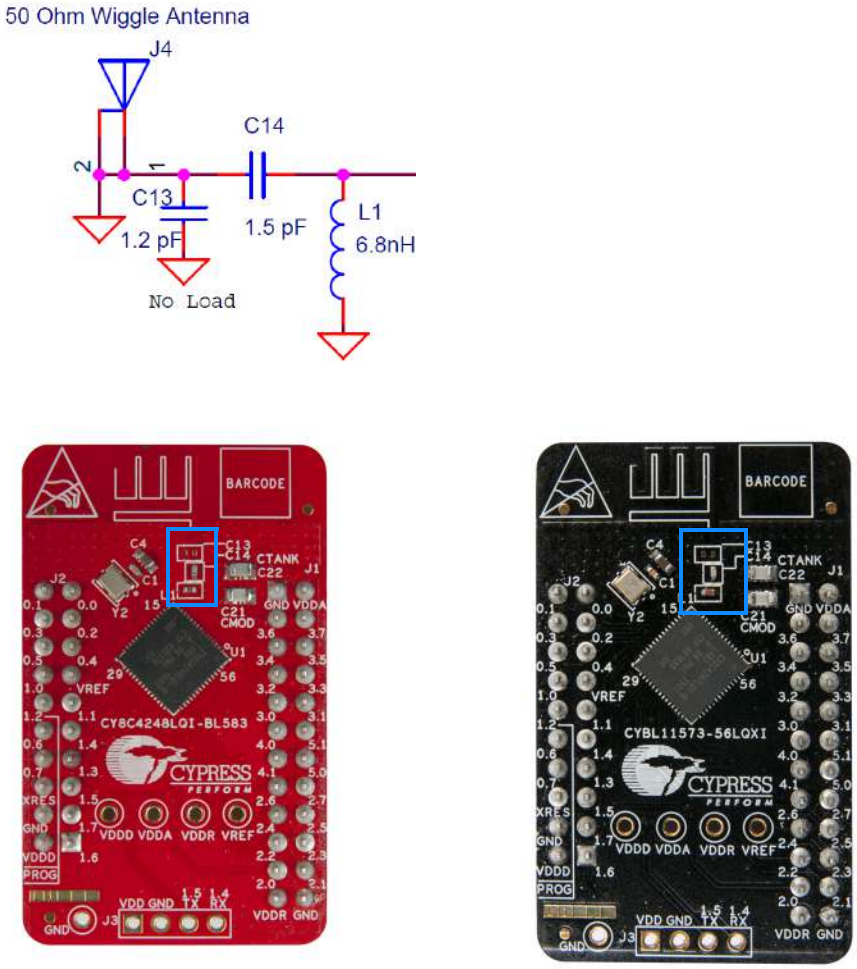


5.2.5 Antenna Matching Network

An Antenna Matching Network is required between the BLE device and the antenna to achieve optimum performance (Figure 5-25). The matching network has four main tasks:

- Transform the balanced output of the radio to an unbalanced connection to the antenna (balun).
- Transform the output impedance of the radio to a 50-ohm antenna.
- Suppress harmonics to a level below the regulations level in TX mode.
- Suppress the local oscillator (LO) leakage in RX mode.

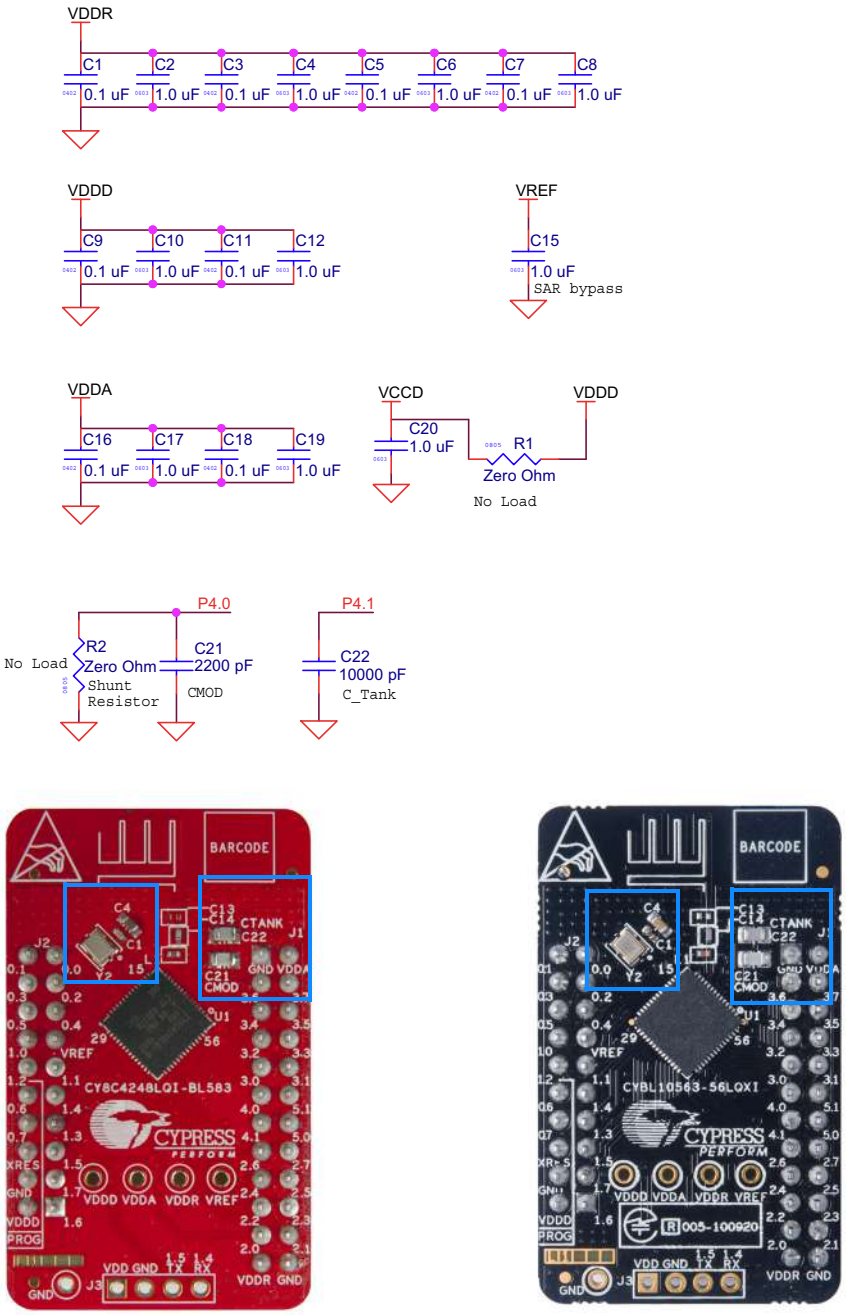
Figure 5-25. Schematics and Board Highlight of Antenna Matching Network and Antenna



5.2.6 BLE Passives

Module boards include a 24-MHz crystal and a 32-kHz crystal, the CMOD and shield (CTANK) circuit for CapSense, a SAR bypass capacitor, and adequate decoupling capacitors for all the power domains, as shown in Figure 5-26.

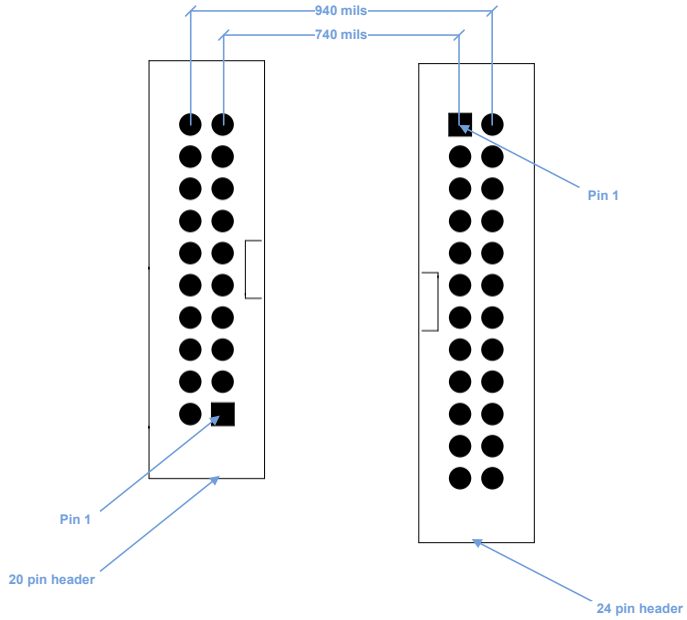
Figure 5-26. Schematics and Board Highlight – External Crystal, CMOD, CTANK, Decaps, Jumpers



A.3 Adding BLE Module-Compatible Headers on Your Baseboard

The baseboard should have a 20-pin header and a 24-pin header. Dimension of these connectors are given here.

Figure A-1. Connectors on BLE Pioneer Kit Baseboard



These headers are available for purchase from Digikey.

Description	Manufacturer	Manufacturer Part Number	Digikey Part Number
CONN HEADER 2.54MM 24POS GOLD	Sullins Connector Solutions	SBH11-PBPC-D12-ST-BK	SBH11-PBPC-D12-ST-BK-ND
CONN HEADER 2.54MM 20POS GOLD	Sullins Connector Solutions	SBH11-PBPC-D10-ST-BK	S9172-ND

PSoC® 4: PSoC 4XX8 BLE 4.2 Family Datasheet

Programmable System-on-Chip (PSoC®)

General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an ARM® Cortex®-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC 4XX8 BLE 4.2 product family, based on this platform, is a combination of a microcontroller with an integrated Bluetooth Low Energy (BLE), also known as Bluetooth Smart, radio and subsystem (BLESS). The other features include digital programmable logic, high-performance analog-to-digital conversion (ADC), opamps with Comparator mode, and standard communication and timing peripherals. The programmable analog and digital subsystems allow flexibility and in-field tuning of the design.

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU with single-cycle multiply and DMA
- Up to 256 KB of flash with Read Accelerator
- Up to 32 KB of SRAM

BLE Radio and Subsystem

- BLE 4.2 support
- 2.4-GHz RF transceiver with 50-Ω antenna drive
- Digital PHY
- Link-Layer engine supporting master and slave modes
- RF output power: –18 dBm to +3 dBm
- RX sensitivity: –92 dBm
- RX current: 18.7 mA
- TX current: 16.5 mA at 0 dBm
- RSSI: 1-dB resolution

Programmable Analog

- Four opamps with reconfigurable high-drive external and high-bandwidth internal drive, Comparator modes, and ADC input buffering capability. Can operate in Deep Sleep mode.
- 12-bit, 1-Msps SAR ADC with differential and single-ended modes; Channel Sequencer with signal averaging
- Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- Two low-power comparators that operate in Deep Sleep mode

Programmable Digital

- Four programmable logic blocks called universal digital blocks, (UDBs), each with eight macrocells and data path
- Cypress-provided peripheral component library, user-defined state machines, and Verilog input

Power Management

- Active mode: 1.7 mA at 3-MHz flash program execution
- Deep Sleep mode: 1.5 µA with watch crystal oscillator (WCO) on
- Hibernate mode: 150 nA with RAM retention
- Stop mode: 60 nA

Capacitive Sensing

- Cypress Capacitive Sigma-Delta (CSD) provides best-in-class SNR (>5:1) and liquid tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning algorithm (SmartSense™)

Segment LCD Drive

- LCD drive supported on all pins (common or segment)
- Operates in Deep Sleep mode with four bits per pin memory

Serial Communication

- Two independent run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality

Timing and Pulse-Width Modulation

- Four 16-bit timer/counter pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Up to 36 Programmable GPIOs

- 7 mm × 7 mm 56-pin QFN package
- 76-ball CSP package
- Any GPIO pin can be CapSense, LCD, analog, or digital
- Two overvoltage-tolerant (OVT) pins; drive modes, strengths, and slew rates are programmable

PSoC Creator™ Design Environment

- Integrated Design Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- API components for all fixed-function and programmable peripherals

Industry-Standard Tool Compatibility

- After schematic entry, development can be done with ARM-based industry-standard development tools

More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PRoC BLE:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes coverting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - AN94020: Getting Started with PRoC BLE
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PRoC BLE functional block
  - Registers TRM describes each of the PRoC BLE registers
- Development Kits:
  - CY8CKIT-042-BLE Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - CY5676, PRoC BLE 256KB Module, features a PRoC BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents

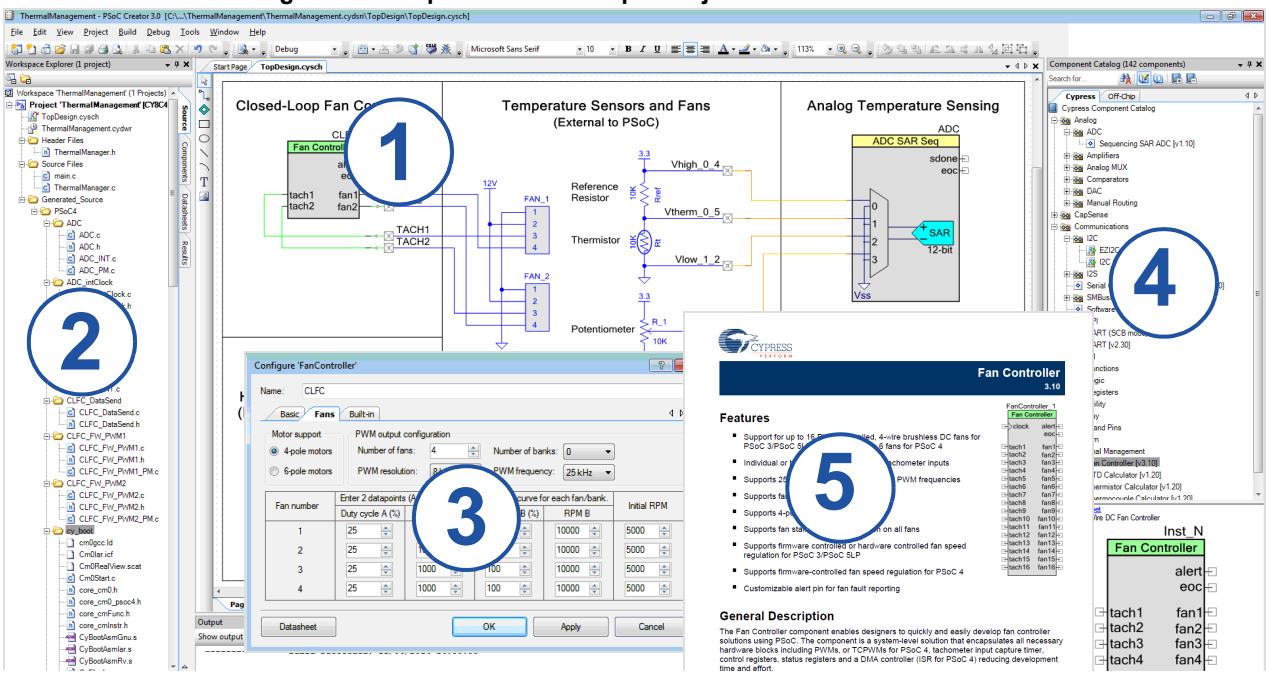
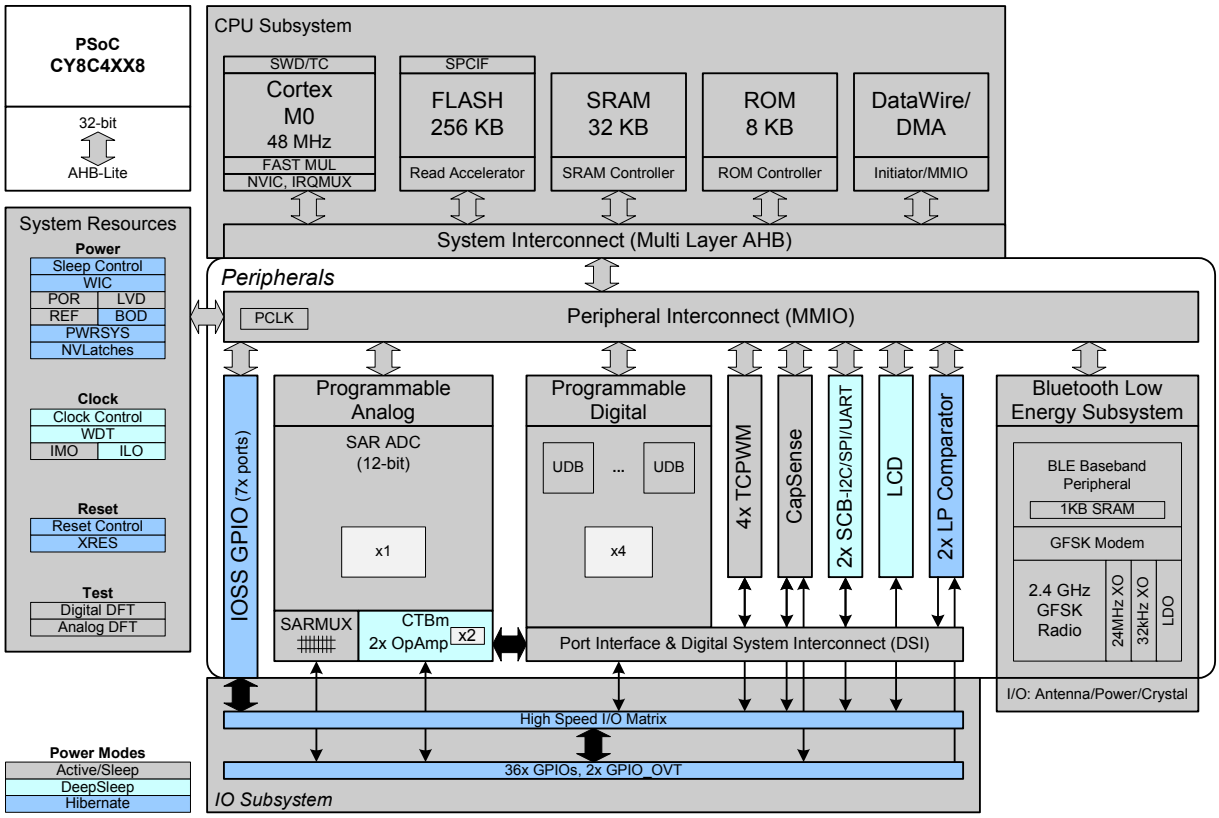


Figure 2. Block Diagram



The PSoC 4XX8 BLE 4.2 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM SWD interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debugging.

The PSoC Creator IDE provides fully integrated programming and debugging support for the PSoC 4XX8 BLE 4.2 devices. The SWD interface is fully compatible with industry-standard third-party tools. With the ability to disable debug features, very robust flash protection, and allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 4XX8 BLE 4.2 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

Debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with the new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4XX8 BLE 4.2 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4XX8 BLE 4.2 allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4XX8 BLE 4.2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher-performance processors such as Cortex-M3 and M4. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to the main processor to be switched off when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a nonmaskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes an SWD interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4XX8 BLE 4.2 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4XX8 BLE 4.2 device has a flash module with either 128 KB or 256 KB of flash memory, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required. Maximum erase and program time is 20 ms per row (256 bytes). This also applies to the emulated EEPROM.

SRAM

SRAM memory is retained during Hibernate.

SROM

The 8-KB supervisory ROM contains a library of executable functions for flash programming. These functions are accessed through supervisory calls (SVC) and enable in-system programming of the flash memory.

DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

The power system is described in detail in the section Power on page 16. It provides an assurance that the voltage levels are as required for the respective modes, and can either delay the mode entry (on power-on reset (POR), for example) until voltage levels are as required or generate resets (brownout detect (BOD)) or interrupts when the power supply reaches a particular programmable level between 1.8 and 4.5 V (low voltage detect (LVD)).

PSoC 4XX8 BLE 4.2 operates with a single external supply (1.71 to 5.5 V without radio, and 1.9 V to 5.5 V with radio). The device has five different power modes; transitions between these modes are managed by the power system. PSoC 4XX8 BLE 4.2 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes. Refer to the *Technical Reference Manual* for more details.

Clock System

The PSoC 4XX8 BLE 4.2 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4XX8 BLE 4.2 consists of the internal main oscillator (IMO), the internal low-speed oscillator (ILO), the 24-MHz external crystal oscillator (ECO) and the 32-kHz watch crystal oscillator (WCO). In addition, an external clock may be supplied from a pin.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 4XX8 BLE 4.2. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low-power oscillator, which is primarily used to generate clocks for the peripheral operation in the Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

External Crystal Oscillator (ECO)

The ECO is used as the active clock for the BLE subsystem to meet the ±50-ppm clock accuracy of the Bluetooth 4.2 Specification. PSoC 4XX8 BLE 4.2 includes a tunable load capacitor to tune the crystal clock frequency by measuring the actual clock frequency. The high-accuracy ECO clock can also be used as a system clock.

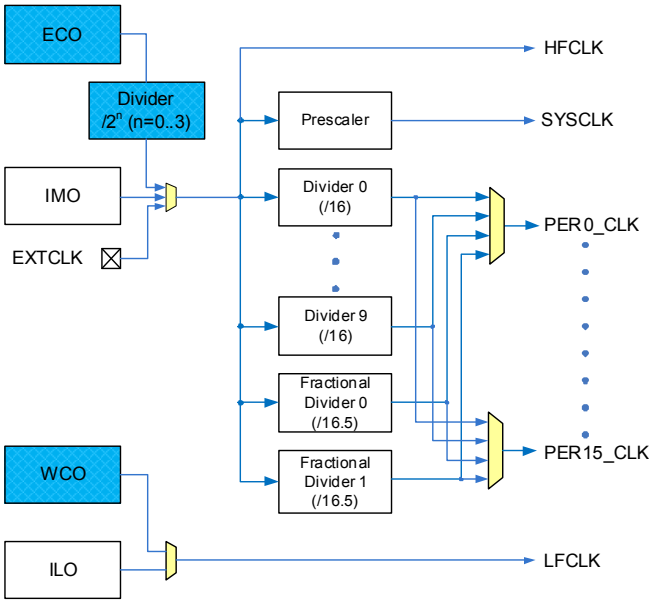
Watch Crystal Oscillator (WCO)

The WCO is used as the sleep clock for the BLE subsystem to meet the ±500-ppm clock accuracy for the Bluetooth 4.2 Specification. The sleep clock provides an accurate sleep timing and enables wakeup at the specified advertisement and connection intervals. The WCO output can be used to realize the real-time clock (RTC) function in firmware.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows the watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register. With the WCO and firmware, an accurate real-time clock (within the bounds of the 32-kHz crystal accuracy) can be realized.

Figure 3. PSoC 4XX8 BLE 4.2 MCU Clocking Architecture



The HFCLK signal can be divided down (see Figure 3) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4XX8 BLE 4.2: ten with 16-bit divide capability and two with 16.5-bit divide capability. This allows the generation of 16 divided clock signals, which can be used by peripheral blocks. The analog clock leads the digital clocks to allow analog events to occur before the digital clock-related noise is generated. The 16-bit and 16.5-bit dividers allow a lot of flexibility in generating fine-grained frequency values and are fully supported in PSoC Creator.

Reset

PSoC 4XX8 BLE 4.2 device can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through resets and allows the software to determine the cause of the reset. An XRES pin is reserved for an external reset to avoid complications with the configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4XX8 BLE 4.2 reference system generates all internally required references. A one-percent voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or use an external reference for the SAR. Refer to Table 19, “SAR ADC AC Specifications,” on page 26 for details.

BLE Radio and Subsystem

PSoC 4XX8 BLE 4.2 incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded AES-128 security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 1 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

The Bluetooth Smart Radio and Subsystem (BLESS) requires a 1.9-V minimum supply (the range varies from 1.9 V to 5.5 V).

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, Out of Band and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
  - LE Secure Connections (Bluetooth 4.2 feature)
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy, Bluetooth 4.2 feature)
- Supports all SIG-adopted BLE profiles

Analog Blocks

12-bit SAR ADC

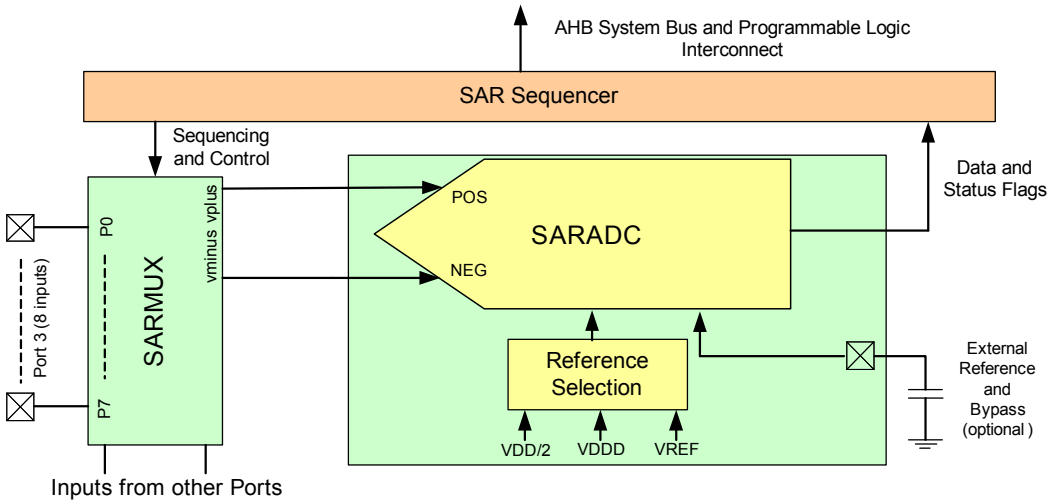
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion (up to 806 Ksps for the PSoC 41X8_BLE derivatives).

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

Figure 4. SAR ADC System Diagram



Opamps (CTBm Block)

PSoC 42X8_BLE has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip, eliminating external components. PGAs, voltage buffers, filters, transimpedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the sample-and-hold circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4XX8 BLE 4.2 has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

Low-Power Comparators

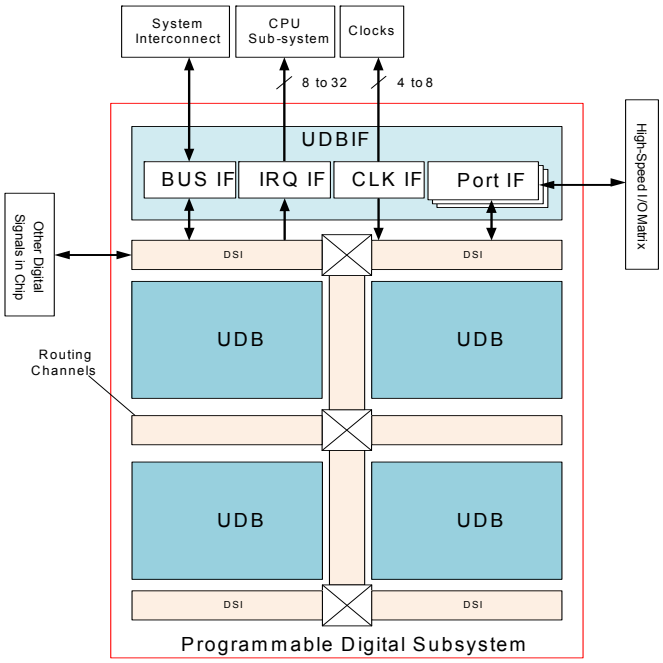
PSoC 4XX8 BLE 4.2 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4XX8 BLE 4.2 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

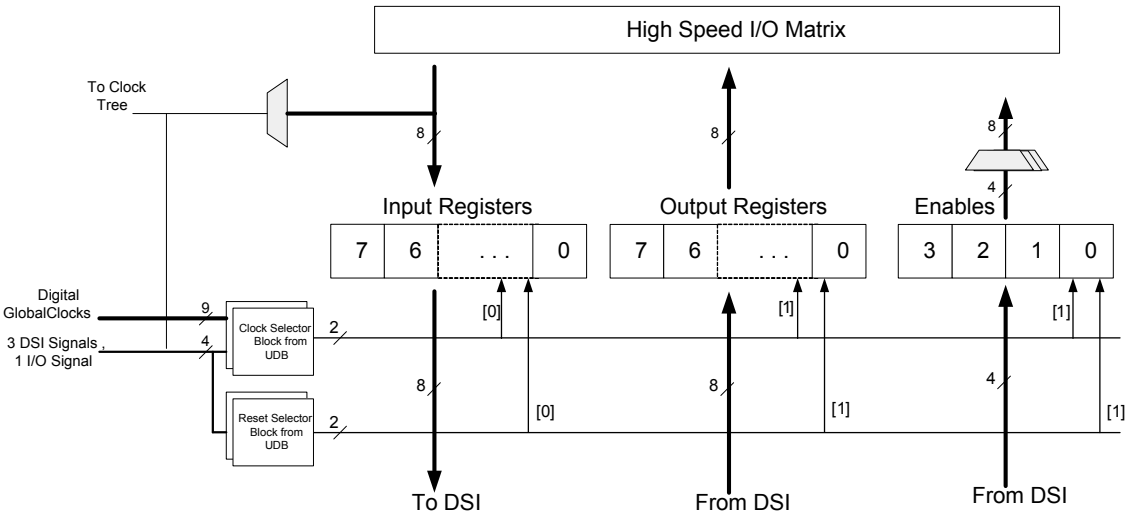
Figure 5. UDB Array



UDBs can be clocked from a clock-divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows a faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 6).

Figure 6. Port Interface



UDBs can generate interrupts (one UDB at a time) to the interrupt controller. UDBs retain the ability to connect to any pin on the chip through the DSI.

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

PSoC 4XX8 BLE 4.2 has two SCBs, each of which can implement an I^2C, UART, or SPI interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of PSoC 4XX8 BLE 4.2 and effectively reduces the I^2C communication to reading from and writing to an array in the memory. In addition, the block supports an 8-deep FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

SCB1 is fully compliant with Standard mode (100 kHz), Fast mode (400 kHz), and Fast-Mode Plus (1 MHz) I^2C signaling specifications when routed to GPIO pins P5[0] and P5[1], except for hot-swap capability during I^2C active communication. The remaining GPIOs do not meet the hot-swap specification (V_{DD} off; draw < 10-µA current) for Fast mode and Fast-Mode Plus, I_{OL} Spec (20 mA) for Fast-Mode Plus, hysteresis spec (0.05 V_{DD}) for Fast mode and Fast-Mode Plus, and minimum fall time spec for Fast mode and Fast-Mode Plus.

- GPIO cells, including P5.0 and P5.1, cannot be hot-swapped or powered up independent of the rest of the I^2C system.
- The GPIO pins P5.0 and P5.1 are over-voltage tolerant but cannot be hot-swapped or powered up independent of the rest of the I^2C system
- Fast-Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; the Slow-Strong mode can help meet this spec depending on the bus load.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO for transmit and receive.

GPIO

PSoC 4XX8 BLE 4.2 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Pins 0 and 1 of Port 5 are overvoltage-tolerant pins
- Individual control of input and output buffer enabling/disabling in addition to drive-strength modes
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin-state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4XX8 BLE 4.2).

Pinouts

Table 1 shows the pin list for the PSoC 4XX8 BLE 4.2 device. Port 3 consists of the high-speed analog inputs for the SAR mux. All pins support CSD CapSense and analog mux bus connections.

Table 1. PSoC 4XX8 BLE 4.2 Pin List (QFN Package)

Pin	Name	Type	Description
1	VDDD	POWER	1.71-V to 5.5-V digital supply
2	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
3	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
4	XRES	RESET	Reset, active LOW
5	P4.0	GPIO	Port 4 Pin 0, lcd, csd
6	P4.1	GPIO	Port 4 Pin 1, lcd, csd
7	P5.0	GPIO	Port 5 Pin 0, lcd, csd
8	P5.1	GPIO	Port 5 Pin 1, lcd, csd
9	VSSD	GROUND	Digital ground
10	VDDR	POWER	1.9-V to 5.5-V radio supply
11	GANT1	GROUND	Antenna shielding ground
12	ANT	ANTENNA	Antenna pin
13	GANT2	GROUND	Antenna shielding ground
14	VDDR	POWER	1.9-V to 5.5-V radio supply
15	VDDR	POWER	1.9-V to 5.5-V radio supply
16	XTAL24I	CLOCK	24-MHz crystal or external clock input
17	XTAL24O	CLOCK	24-MHz crystal
18	VDDR	POWER	1.9-V to 5.5-V radio supply
19	P0.0	GPIO	Port 0 Pin 0, lcd, csd
20	P0.1	GPIO	Port 0 Pin 1, lcd, csd
21	P0.2	GPIO	Port 0 Pin 2, lcd, csd
22	P0.3	GPIO	Port 0 Pin 3, lcd, csd
23	VDDD	POWER	1.71-V to 5.5-V digital supply
24	P0.4	GPIO	Port 0 Pin 4, lcd, csd
25	P0.5	GPIO	Port 0 Pin 5, lcd, csd
26	P0.6	GPIO	Port 0 Pin 6, lcd, csd
27	P0.7	GPIO	Port 0 Pin 7, lcd, csd
28	P1.0	GPIO	Port 1 Pin 0, lcd, csd
29	P1.1	GPIO	Port 1 Pin 1, lcd, csd
30	P1.2	GPIO	Port 1 Pin 2, lcd, csd
31	P1.3	GPIO	Port 1 Pin 3, lcd, csd
32	P1.4	GPIO	Port 1 Pin 4, lcd, csd
33	P1.5	GPIO	Port 1 Pin 5, lcd, csd
34	P1.6	GPIO	Port 1 Pin 6, lcd, csd
35	P1.7	GPIO	Port 1 Pin 7, lcd, csd
36	VDDA	POWER	1.71-V to 5.5-V analog supply
37	P2.0	GPIO	Port 2 Pin 0, lcd, csd
38	P2.1	GPIO	Port 2 Pin 1, lcd, csd
39	P2.2	GPIO	Port 2 Pin 2, lcd, csd

Table 1. PSoC 4XX8 BLE 4.2 Pin List (QFN Package) *(continued)*

Pin	Name	Type	Description
40	P2.3	GPIO	Port 2 Pin 3, lcd, csd
41	P2.4	GPIO	Port 2 Pin 4, lcd, csd
42	P2.5	GPIO	Port 2 Pin 5, lcd, csd
43	P2.6	GPIO	Port 2 Pin 6, lcd, csd
44	P2.7	GPIO	Port 2 Pin 7, lcd, csd
45	VREF	REF	1.024-V reference
46	VDDA	POWER	1.71-V to 5.5-V analog supply
47	P3.0	GPIO	Port 3 Pin 0, lcd, csd
48	P3.1	GPIO	Port 3 Pin 1, lcd, csd
49	P3.2	GPIO	Port 3 Pin 2, lcd, csd
50	P3.3	GPIO	Port 3 Pin 3, lcd, csd
51	P3.4	GPIO	Port 3 Pin 4, lcd, csd
52	P3.5	GPIO	Port 3 Pin 5, lcd, csd
53	P3.6	GPIO	Port 3 Pin 6, lcd, csd
54	P3.7	GPIO	Port 3 Pin 7, lcd, csd
55	VSSA	GROUND	Analog ground
56	VCCD	POWER	Regulated 1.8-V supply, connect to 1.3-µF capacitor.
57	EPAD	GROUND	Ground paddle for the QFN package

Table 2. PSoC 4XX8 BLE 4.2 Pin List (WLCSP Package)

Pin	Name	Type	Description
A1	NC	NC	Do not connect
A2	VREF	REF	1.024-V reference
A3	VSSA	GROUND	Analog ground
A4	P3.3	GPIO	Port 3 Pin 3, analog/digital/lcd/csd
A5	P3.7	GPIO	Port 3 Pin 7, analog/digital/lcd/csd
A6	VSSD	GROUND	Digital ground
A7	VSSA	GROUND	Analog ground
A8	VCCD	POWER	Regulated 1.8-V supply, connect to 1-µF capacitor
A9	VDDD	POWER	1.71-V to 5.5-V digital supply
B1	NB	NO BALL	No Ball
B2	P2.3	GPIO	Port 2 Pin 3, analog/digital/lcd/csd
B3	VSSA	GROUND	Analog ground
B4	P2.7	GPIO	Port 2 Pin 7, analog/digital/lcd/csd
B5	P3.4	GPIO	Port 3 Pin 4, analog/digital/lcd/csd
B6	P3.5	GPIO	Port 3 Pin 5, analog/digital/lcd/csd
B7	P3.6	GPIO	Port 3 Pin 6, analog/digital/lcd/csd
B8	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
B9	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
C1	NC	NC	Do not connect

Table 2. PSoC 4XX8 BLE 4.2 Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Description
C2	VSSA	GROUND	Analog ground
C3	P2.2	GPIO	Port 2 Pin 2, analog/digital/lcd/csd
C4	P2.6	GPIO	Port 2 Pin 6, analog/digital/lcd/csd
C5	P3.0	GPIO	Port 3 Pin 0, analog/digital/lcd/csd
C6	P3.1	GPIO	Port 3 Pin 1, analog/digital/lcd/csd
C7	P3.2	GPIO	Port 3 Pin 2, analog/digital/lcd/csd
C8	XRES	RESET	Reset, active LOW
C9	P4.0	GPIO	Port 4 Pin 0, analog/digital/lcd/csd
D1	NC	NC	Do not connect
D2	P1.7	GPIO	Port 1 Pin 7, analog/digital/lcd/csd
D3	VDDA	POWER	1.71-V to 5.5-V analog supply
D4	P2.0	GPIO	Port 2 Pin 0, analog/digital/lcd/csd
D5	P2.1	GPIO	Port 2 Pin 1, analog/digital/lcd/csd
D6	P2.5	GPIO	Port 2 Pin 5, analog/digital/lcd/csd
D7	VSSD	GROUND	Digital ground
D8	P4.1	GPIO	Port 4 Pin 1, analog/digital/lcd/csd
D9	P5.0	GPIO	Port 5 Pin 0, analog/digital/lcd/csd
E1	NC	NC	Do not connect
E2	P1.2	GPIO	Port 1 Pin 2, analog/digital/lcd/csd
E3	P1.3	GPIO	Port 1 Pin 3, analog/digital/lcd/csd
E4	P1.4	GPIO	Port 1 Pin 4, analog/digital/lcd/csd
E5	P1.5	GPIO	Port 1 Pin 5, analog/digital/lcd/csd
E6	P1.6	GPIO	Port 1 Pin 6, analog/digital/lcd/csd
E7	P2.4	GPIO	Port 2 Pin 4, analog/digital/lcd/csd
E8	P5.1	GPIO	Port 5 Pin 1, analog/digital/lcd/csd
E9	VSSD	GROUND	Digital ground
F1	NC	NC	Do not connect
F2	VSSD	GROUND	Digital ground
F3	P0.7	GPIO	Port 0 Pin 7, analog/digital/lcd/csd
F4	P0.3	GPIO	Port 0 Pin 3, analog/digital/lcd/csd
F5	P1.0	GPIO	Port 1 Pin 0, analog/digital/lcd/csd
F6	P1.1	GPIO	Port 1 Pin 1, analog/digital/lcd/csd
F7	VSSR	GROUND	Radio ground
F8	VSSR	GROUND	Radio ground
F9	VDDR	POWER	1.9-V to 5.5-V radio supply
G1	NC	NC	Do not connect
G2	P0.6	GPIO	Port 0 Pin 6, analog/digital/lcd/csd
G3	VDDD	POWER	1.71-V to 5.5-V digital supply
G4	P0.2	GPIO	Port 0 Pin 2, analog/digital/lcd/csd
G5	VSSD	GROUND	Digital ground

Table 2. PSoC 4XX8 BLE 4.2 Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Description
G6	VSSR	GROUND	Radio ground
G7	VSSR	GROUND	Radio ground
G8	GANT	GROUND	Antenna shielding ground
G9	VSSR	GROUND	Radio ground
H1	NC	NC	Do not connect
H2	P0.5	GPIO	Port 0 Pin 5, analog/digital/lcd/csd
H3	P0.1	GPIO	Port 0 Pin 1, analog/digital/lcd/csd
H4	XTAL24O	CLOCK	24-MHz crystal
H5	XTAL24I	CLOCK	24-MHz crystal or external clock input
H6	VSSR	GROUND	Radio ground
H7	VSSR	GROUND	Radio ground
H8	ANT	ANTENNA	Antenna pin
J1	NC	NC	Do not connect
J2	P0.4	GPIO	Port 0 Pin 4, analog/digital/lcd/csd
J3	P0.0	GPIO	Port 0 Pin 0, analog/digital/lcd/csd
J4	VDDR	POWER	1.9-V to 5.5-V radio supply
J7	VDDR	POWER	1.9-V to 5.5-V radio supply
J8	NO CONNECT	–	–

High-speed I/O matrix (HSIOM) is a group of high-speed switches that routes GPIOs to the resources inside the device. These resources include CapSense, TCPWMs, I^2C, SPI, UART, and LCD. HSIOM_PORT_SELx are 32-bit-wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing as shown in Table 3.

Table 3. HSIOM Port Settings

Value	Description
0	Firmware-controlled GPIO
1	Output is firmware-controlled, but Output Enable (OE) is controlled from DSI.
2	Both output and OE are controlled from DSI.
3	Output is controlled from DSI, but OE is firmware-controlled.
4	Pin is a CSD sense pin
5	Pin is a CSD shield pin
6	Pin is connected to AMUXA
7	Pin is connected to AMUXB
8	Pin-specific Active function #0
9	Pin-specific Active function #1
10	Pin-specific Active function #2

Table 3. HSIOM Port Settings *(continued)*

Value	Description
11	Reserved
12	Pin is an LCD common pin
13	Pin is an LCD segment pin
14	Pin-specific Deep-Sleep function #0
15	Pin-specific Deep-Sleep function #1

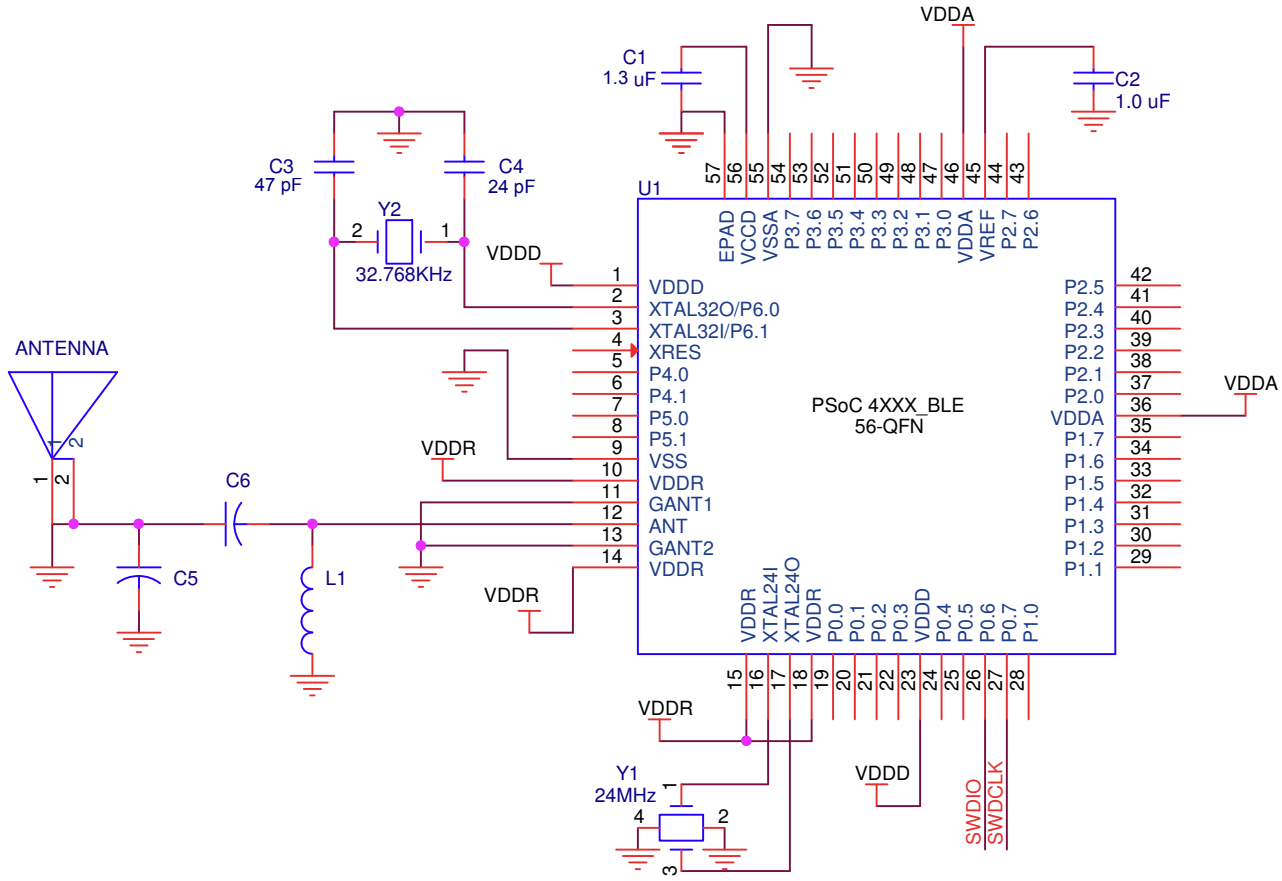
The selection of peripheral function for different GPIO pins is given in Table 4.

Table 4. Port Pin Connections

Name	Analog	Digital					
		GPIO	Active #0	Active #1	Active #2	Deep Sleep #0	Deep Sleep #1
P0.0	COMP0_INP	GPIO	TCPWM0_P[3]	SCB1_UART_RX[1]	–	SCB1_I2C_SDA[1]	SCB1_SPI_MOSI[1]
P0.1	COMP0_INN	GPIO	TCPWM0_N[3]	SCB1_UART_TX[1]	–	SCB1_I2C_SCL[1]	SCB1_SPI_MISO[1]
P0.2	–	GPIO	TCPWM1_P[3]	SCB1_UART_RTS[1]	–	COMP0_OUT[0]	SCB1_SPI_SS0[1]
P0.3	–	GPIO	TCPWM1_N[3]	SCB1_UART_CTS[1]	–	COMP1_OUT[0]	SCB1_SPI_SCLK[1]
P0.4	COMP1_INP	GPIO	TCPWM1_P[0]	SCB0_UART_RX[1]	EXT_CLK[0]/ ECO_OUT[0]	SCB0_I2C_SDA[1]	SCB0_SPI_MOSI[1]
P0.5	COMP1_INN	GPIO	TCPWM1_N[0]	SCB0_UART_TX[1]	–	SCB0_I2C_SCL[1]	SCB0_SPI_MISO[1]
P0.6	–	GPIO	TCPWM2_P[0]	SCB0_UART_RTS[1]	–	SWDIO[0]	SCB0_SPI_SS0[1]
P0.7	–	GPIO	TCPWM2_N[0]	SCB0_UART_CTS[1]	–	SWDCLK[0]	SCB0_SPI_SCLK[1]
P1.0	CTBm1_OA0_INP	GPIO	TCPWM0_P[1]	–	–	COMP0_OUT[1]	WCO_OUT[2]
P1.1	CTBm1_OA0_INN	GPIO	TCPWM0_N[1]	–	–	COMP1_OUT[1]	SCB1_SPI_SS1
P1.2	CTBm1_OA0_OUT	GPIO	TCPWM1_P[1]	–	–	–	SCB1_SPI_SS2
P1.3	CTBm1_OA1_OUT	GPIO	TCPWM1_N[1]	–	–	–	SCB1_SPI_SS3
P1.4	CTBm1_OA1_INN	GPIO	TCPWM2_P[1]	SCB0_UART_RX[0]	–	SCB0_I2C_SDA[0]	SCB0_SPI_MOSI[1]
P1.5	CTBm1_OA1_INP	GPIO	TCPWM2_N[1]	SCB0_UART_TX[0]	–	SCB0_I2C_SCL[0]	SCB0_SPI_MISO[1]
P1.6	CTBm1_OA0_INP	GPIO	TCPWM3_P[1]	SCB0_UART_RTS[0]	–	–	SCB0_SPI_SS0[1]
P1.7	CTBm1_OA1_INP	GPIO	TCPWM3_N[1]	SCB0_UART_CTS[0]	–	–	SCB0_SPI_SCLK[1]
P2.0	CTBm0_OA0_INP	GPIO	–	–	–	–	SCB0_SPI_SS1
P2.1	CTBm0_OA0_INN	GPIO	–	–	–	–	SCB0_SPI_SS2
P2.2	CTBm0_OA0_OUT	GPIO	–	–	–	WAKEUP	SCB0_SPI_SS3
P2.3	CTBm0_OA1_OUT	GPIO	–	–	–	–	WCO_OUT[1]
P2.4	CTBm0_OA1_INN	GPIO	–	–	–	–	–
P2.5	CTBm0_OA1_INP	GPIO	–	–	–	–	–
P2.6	CTBm0_OA0_INP	GPIO	–	–	–	–	–
P2.7	CTBm0_OA1_INP	GPIO	–	–	EXT_CLK[1]/ECO_OUT[1]	–	–
P3.0	SARMUX_0	GPIO	TCPWM0_P[2]	SCB0_UART_RX[2]	–	SCB0_I2C_SDA[2]	–
P3.1	SARMUX_1	GPIO	TCPWM0_N[2]	SCB0_UART_TX[2]	–	SCB0_I2C_SCL[2]	–
P3.2	SARMUX_2	GPIO	TCPWM1_P[2]	SCB0_UART_RTS[2]	–	–	–
P3.3	SARMUX_3	GPIO	TCPWM1_N[2]	SCB0_UART_CTS[2]	–	–	–
P3.4	SARMUX_4	GPIO	TCPWM2_P[2]	SCB1_UART_RX[2]	–	SCB1_I2C_SDA[2]	–
P3.5	SARMUX_5	GPIO	TCPWM2_N[2]	SCB1_UART_TX[2]	–	SCB1_I2C_SCL[2]	–
P3.6	SARMUX_6	GPIO	TCPWM3_P[2]	SCB1_UART_RTS[2]	–	–	–
P3.7	SARMUX_7	GPIO	TCPWM3_N[2]	SCB1_UART_CTS[2]	–	–	WCO_OUT[0]
P4.0	CMOD	GPIO	TCPWM0_P[0]	SCB1_UART_RTS[0]	–	–	SCB1_SPI_MOSI[0]
P4.1	CTANK	GPIO	TCPWM0_N[0]	SCB1_UART_CTS[0]	–	–	SCB1_SPI_MISO[0]
P5.0	–	GPIO	TCPWM3_P[0]	SCB1_UART_RX[0]	EXTPA_EN	SCB1_I2C_SDA[0]	SCB1_SPI_SS0[0]
P5.1	–	GPIO	TCPWM3_N[0]	SCB1_UART_TX[0]	EXT_CLK[2]/ECO_OUT[2]	SCB1_I2C_SCL[0]	SCB1_SPI_SCLK[0]
P6.0_XTAL32O	–	GPIO	–	–	–	–	–
P6.1_XTAL32I	–	GPIO	–	–	–	–	–

The possible pin connections are shown for all analog and digital peripherals (except the radio, LCD, and CSD blocks, which were shown in Table 1). A typical system application connection diagram is shown in Figure 7.

Figure 7. System Application Connection Diagram



Power

The PSoC 4XX8 BLE 4.2 device can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply (VDDD), analog supply (VDDA), and radio supply (VDDR) pins. Internal LDOs in the device regulate the supply voltage to the required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. Analog circuits run directly from the analog supply (VDDA) input. The device uses separate regulators for Deep Sleep and Hibernate (lowered power supply and retention) modes to minimize the power consumption. The radio stops working below 1.9 V, but the device continues to function down to 1.71 V without RF.

Bypass capacitors must be used from VDDx (x = A, D, or R) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (for example, 0.1 µF). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD	The internal bandgap may be bypassed with a 1-µF to 10-µF.
VDDA	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF.
VDDR	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF.
VCCD	1.3-µF ceramic capacitor at the VCCD pin.
VREF (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor.

Electrical Specifications

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Analog, digital, or radio supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	6	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} +0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
BID57	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID58	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
BID61	LU	Pin current for latch-up	–200	–	200	mA	–

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 6. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID6	V_{DD}	Power supply input voltage (V_{DDA} = V_{DDD} = V_{DD})	1.8	–	5.5	V	With regulator enabled
SID7	V_{DD}	Power supply input voltage unregulated (V_{DDA} = V_{DDD} = V_{DD})	1.71	1.8	1.89	V	Internally unregulated Supply
SID8	V_{DDR}	Radio supply voltage (Radio ON)	1.9	–	5.5	V	–
SID8A	V_{DDR}	Radio supply voltage (Radio OFF)	1.71	–	5.5	V	–
SID9	V_{CCD}	Digital regulator output voltage (for core logic)	–	1.8	–	V	–
SID10	C_{VCCD}	Digital regulator output bypass capacitor	1	1.3	1.6	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V							–
SID13	I_{DD3}	Execute from flash; CPU at 3 MHz	–	2.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID14	I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = –40 C to 85 °C
SID15	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID16	I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID17	I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID18	I_{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C

Note
1. Usage above the absolute maximum conditions listed in Table 5 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID19	I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID20	I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID21	I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID22	I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V_{DD} = 1.8 to 5.5 V							
SID23	I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 to 5.5 V							
SID24	I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V							
SID25	I_{DD15}	WDT with WCO on	–	1.5	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID26	I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V							
SID27	I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID28	I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID29	I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
SID30	I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V							
SID31	I_{DD21}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID32	I_{DD22}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V							
SID33	I_{DD23}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID34	I_{DD24}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID35	I_{DD25}	Opamp on	–	–	–	µA	T = 25 °C
SID36	I_{DD26}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.8 to 3.6 V							
SID37	I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3V
SID38	I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 3.6 to 5.5 V							
SID39	I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID40	I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 to 3.6 V							
SID43	I_{DD33}	Stop mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID44	I_{DD34}	Stop mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
SID45	I_{DD35}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID46	I_{DD36}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 to 5.5 V							
SID47	I_{DD37}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID48	I_{DD38}	Stop mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
SID49	I_{DD39}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID50	I_{DD40}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID51	I_{DD41}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C
SID52	I_{DD42}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C

Table 7. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
SID54	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
SID55	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization.
SID56	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID57	T_{STOP}	Wakeup from Stop mode	–	–	2.2	ms	Guaranteed by characterization

GPIO

Table 8. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID58	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
SID59	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
SID60	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	-	V	–
SID61	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3× V_{DD}	V	–
SID62	V_{IH}	LVTTL input, V_{DD} >= 2.7 V	2.0	–	-	V	–
SID63	V_{IL}	LVTTL input, V_{DD} >= 2.7 V	–	–	0.8	V	–
SID64	V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	Ioh = 4-mA at 3.3-V V_{DD}
SID65	V_{OH}	Output voltage HIGH level	V_{DD} –0.5	–	–	V	Ioh = 1-mA at 1.8-V V_{DD}
SID66	V_{OL}	Output voltage LOW level	–	–	0.6	V	Iol = 8-mA at 3.3-V V_{DD}
SID67	V_{OL}	Output voltage LOW level	–	–	0.6	V	Iol = 4-mA at 1.8-V V_{DD}
SID68	V_{OL}	Output voltage LOW level	–	–	0.4	V	Iol = 3-mA at 3.3-V V_{DD}
SID69	Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID70	Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID71	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
SID72	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID73	C_{IN}	Input capacitance	–	–	7	pF	–
SID74	Vhysttl	Input hysteresis LVTTL	25	40		mV	V_{DD} > 2.7 V
SID75	Vhyscmos	Input hysteresis CMOS	0.05 × V_{DD}	–	–	mV	–
SID76	Idiode	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID77	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 9. GPIO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID78	T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID79	T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID80	T_{RISES}	Rise time in Slow-Strong mode	10	–	60	–	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID81	T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	–	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID82	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Fast-Strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 9. GPIO AC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$F_{GPIOUT2}$	GPIO Fout; 1.7 V≤ V_{DD} ≤ 3.3 V. Fast-Strong mode	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID84	$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Slow-Strong mode	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID85	$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V. Slow-Strong mode	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID86	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Table 10. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID71A	I_{IL}	Input leakage current (absolute value), V_{IH} > V_{DD}	–	–	10	µA	25 °C, V_{DD} = 0 V, V_{IH}= 3.0 V
SID66A	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 20-mA, V_{DD} > 2.9-V

Table 11. OVT GPIO AC Specifications (P5_0 and P5_1 Only)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID78A	T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3-V
SID79A	T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3-V
SID80A	T_{RISSS}	Output rise time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%–90%, V_{DD}=3.3-V
SID81A	T_{FALLSS}	Output fall time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%–90%, V_{DD}=3.3-V
SID82A	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID83A	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25-pF load, 60/40 duty cycle

XRES

Table 12. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID87	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID88	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID89	Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID90	C_{IN}	Input capacitance	–	3	–	pF	–
SID91	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID92	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 13. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

Analog Peripherals

Opamp

Table 14. Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{DD} (Opamp Block Current. V_{DD} = 1.8 V. No Load)							
SID94	I_{DD_HI}	Power = high	–	1000	1850	µA	–
SID95	I_{DD_MED}	Power = medium	–	500	950	µA	–
SID96	I_{DD_LOW}	Power = low	–	250	350	µA	–
GBW (Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V)							
SID97	GBW_HI	Power = high	6	–	–	MHz	–
SID98	GBW_MED	Power = medium	4	–	–	MHz	–
SID99	GBW_LO	Power = low	–	1	–	MHz	–
I_{OUT_MAX} (V_{DDA} ≥ 2.7 V, 500 mV From Rail)							
SID100	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	–
SID101	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	–
SID102	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	–
I_{OUT} (V_{DDA} = 1.71 V, 500 mV From Rail)							
SID103	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	–
SID104	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	–
SID105	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	–
SID106	V_{IN}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
SID107	V_{CM}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
V_{OUT} (V_{DDA} ≥ 2.7 V)							
SID108	V_{OUT_1}	Power = high, I_{LOAD}=10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID109	V_{OUT_2}	Power = high, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID110	V_{OUT_3}	Power = medium, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID111	V_{OUT_4}	Power = low, I_{LOAD}=0.1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID112	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID113	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID114	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID115	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID116	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID117	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Low mode
SID118	CMRR	DC	70	80	–	dB	V_{DDD} = 3.6-V
SID119	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DDD} = 3.6-V
Noise							
SID120	V_{N1}	Input referred, 1 Hz–1 GHz, power = high	–	94	–	µVrms	–
SID121	V_{N2}	Input referred, 1-kHz, power = high	–	72	–	nV/rtHz	–

Table 14. Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID122	V_{N3}	Input referred, 10-kHz, power = high	–	28	–	nV/rtHz	–
SID123	V_{N4}	Input referred, 100-kHz, power = high	–	15	–	nV/rtHz	–
SID124	C_{LOAD}	Stable up to maximum load. Performance specs at 50 pF	–	–	125	pF	–
SID125	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V	6	–	–	V/µsec	–
SID126	T_op_wake	From disable to enable, no external RC dominating	–	300	–	µsec	–
Comp_mode (Comparator Mode; 50-mV Drive, $T_{RISE} = T_{FALL}$ (Approx.)							
SID127	T_{PD1}	Response time; power = high	–	150	–	nsec	–
SID128	T_{PD2}	Response time; power = medium	–	400	–	nsec	–
SID129	T_{PD3}	Response time; power = low	–	2000	–	nsec	–
SID130	Vhyst_op	Hysteresis	–	10	–	mV	–
Deep Sleep (Deep Sleep mode operation is only guaranteed for $V_{DDA} > 2.5$ V)							
SID131	GBW_DS	Gain bandwidth product	–	50	–	kHz	–
SID132	IDD_DS	Current	–	15	–	µA	–
SID133	Vos_DS	Offset voltage	–	5	–	mV	–
SID134	Vos_dr_DS	Offset voltage drift	–	20	–	µV/°C	–
SID135	Vout_DS	Output voltage	0.2	–	V_{DD}–0.2	V	–
SID136	Vcm_DS	Common mode voltage	0.2	–	V_{DD}–1.8	V	–

Table 15. Comparator DC Specifications[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID140	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	–
SID141	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±6	mV	–
SID141A	$V_{OFFSET3}$	Input offset voltage, ultra-low-power mode	–	±12	–	mV	$V_{DDD} \geq 2.6$ V for Temp < 0°C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C
SID142	V_{HYST}	Hysteresis when enabled. Common Mode voltage range from 0 to VDD –1	–	10	35	mV	–
SID143	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} –0.1	V	Modes 1 and 2
SID144	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}	V	–
SID145	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} –1.15	V	$V_{DDD} \geq 2.6$ V for Temp < 0°C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C
SID146	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V
SID147	CMRR	Common mode rejection ratio	42	–	–	dB	$V_{DDD} \leq 2.7$ V
SID148	I_{CMP1}	Block current, normal mode	–	–	400	µA	–
SID149	I_{CMP2}	Block current, low power mode	–	–	100	µA	–

Note
3. ULP LCOMP operating conditions:
   - V_{DDD} 2.6 V-5.5 V for datasheet temp range < 0 °C
   - V_{DDD} 1.8 V-5.5 V for datasheet temp range ≥ 0 °C

Table 15. Comparator DC Specifications[3] *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID150	I_{CMP3}	Block current in ultra low-power mode	–	6	–	µA	V_{DDD} ≥ 2.6 V for Temp < 0°C, V_{DDD} ≥ 1.8 V for Temp > 0 °C
SID151	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	–

Table 16. Comparator AC Specifications[4]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID152	T_{RESP1}	Response time, normal mode, 50-mV overdrive	–	38	–	ns	50-mV overdrive
SID153	T_{RESP2}	Response time, low power mode, 50-mV overdrive	–	70	–	ns	50-mV overdrive
SID154	T_{RESP3}	Response time, ultra-low-power mode, 50-mV overdrive	–	2.3	–	µs	200-mV overdrive. V_{DDD} ≥ 2.6 V for Temp < 0°C, V_{DDD} ≥ 1.8 V for Temp > 0 °C

Temperature Sensor

Table 17. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID155	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

SAR ADC

Table 18. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID156	A_RES	Resolution	–	–	12	bits	–
SID157	A_CHNIS_S	Number of channels - single-ended	–	–	16	–	8 full-speed
SID158	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID159	A-MONO	Monotonicity	–	–	–	–	Yes
SID160	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID161	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
SID162	A_ISAR	Current consumption	–	–	1	mA	–
SID163	A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	–
SID164	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	–
SID165	A_INRES	Input resistance	–	–	2.2	kΩ	–
SID166	A_INCAP	Input capacitance	–	–	10	pF	–
SID312	VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024-V)

Note
4. ULP LCOMP operating conditions:
   - V_{DDD} 2.6 V-5.5 V for datasheet temp range < 0 °C
   - V_{DDD} 1.8 V-5.5 V for datasheet temp range ≥ 0 °C

Table 19. SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID167	A_psrr	Power supply rejection ratio	70	–	–	dB	Measured at 1-V reference
SID168	A_cmrr	Common mode rejection ratio	66	–	–	dB	–
SID169	A_samp	Sample rate	–	–	1	Msps	806 Ksps for PSoC 41X8_BLE devices
SID313	Fsarintref	SAR operating speed without external ref. bypass	–	–	100	Ksps	12-bit resolution
SID170	A_snr	Signal-to-noise ratio (SNR)	65	–	–	dB	Fin = 10 kHz
SID171	A_bw	Input bandwidth without aliasing	–	–	A_samp/2	kHz	–
SID172	A_inl	Integral non linearity. V_{DD} = 1.71 to 5.5 V, 1 Msps	–1.7	–	2	LSB	Vref = 1 V to V_{DD}
SID173	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	Vref = 1.71 V to V_{DD}
SID174	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5 V, 500 Ksps	–1.5	–	1.7	LSB	Vref = 1 V to V_{DD}
SID175	A_dnl	Differential non linearity. V_{DD} = 1.71 to 5.5 V, 1 Msps	–1	–	2.2	LSB	Vref = 1 V to V_{DD}
SID176	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6 V, 1 Msps	–1	–	2	LSB	Vref = 1.71 V to V_{DD}
SID177	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5 V, 500 Ksps	–1	–	2.2	LSB	Vref = 1 V to V_{DD}
SID178	A_thd	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz

CSD

Table 20. CSD Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID179	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	–
SID180	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	–
SID181	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	–
SID182	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	–
SID183	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	–
SID184	SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity. Radio is not operating during the scan
SID185	I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	–
SID186	I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	–
SID187	I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	–
SID188	I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	–

Digital Peripherals

Timer

Table 21. Timer DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID189	I_{TIM1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit timer
SID190	I_{TIM2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit timer
SID191	I_{TIM3}	Block current consumption at 48 MHz	–	–	712	µA	16-bit timer

Table 22. Timer AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID192	$T_{TIMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID193	$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID194	$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID195	T_{TIMRES}	Timer resolution	T_{CLK}	–	–	ns	–
SID196	$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID197	$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID198	$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID199	$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Counter

Table 23. Counter DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID200	I_{CTR1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit counter
SID201	I_{CTR2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit counter
SID202	I_{CTR3}	Block current consumption at 48 MHz	–	–	712	µA	16-bit counter

Table 24. Counter AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID203	$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID204	$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID205	$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID206	T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	–
SID207	$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID208	$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID209	$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID210	$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Pulse Width Modulation (PWM)

Table 25. PWM DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID211	I_{PWM1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit PWM
SID212	I_{PWM2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit PWM
SID213	I_{PWM3}	Block current consumption at 48 MHz	–	–	741	µA	16-bit PWM

Table 26. PWM AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID214	$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID215	$T_{PWMPWINT}$	Pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID216	T_{PWMEXT}	Pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID217	$T_{PWMKILLINT}$	Kill pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID218	$T_{PWMKILLEXT}$	Kill pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID219	$T_{PWMEINT}$	Enable pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID220	$T_{PWMENEXT}$	Enable pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID221	$T_{PWMRESWINT}$	Reset pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID222	$T_{PWMRESWEXT}$	Reset pulse width (external)	2 × T_{CLK}	–	–	ns	–

I^2C

Table 27. Fixed I^2C DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID224	I_{I2C2}	Block current consumption at 400 kHz	–	–	155	µA	–
SID225	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID226	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 28. Fixed I^2C AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID227	F_{I2C1}	Bit rate	–	–	1	Mbps	–

LCD Direct Drive

Table 29. LCD Direct Drive DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID228	I_{LCDLOW}	Operating current in low-power mode	–	17.5	–	µA	16 × 4 small segment display at 50 Hz
SID229	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID230	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID231	I_{LCDOP1}	LCD system operating current V_{BIAS} = 5 V.	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
SID232	I_{LCDOP2}	LCD system operating current. V_{BIAS} = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

Table 30. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID233	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Table 31. Fixed UART DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	I_{UART1}	Block current consumption at 100 kbps	–	–	55	µA	–
SID235	I_{UART2}	Block current consumption at 1000 kbps	–	–	360	µA	–

Table 32. Fixed UART AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID236	F_{UART}	Bit rate	–	–	1	Mbps	–

SPI Specifications

Table 33. Fixed SPI DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID237	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID238	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
SID239	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 34. Fixed SPI AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID240	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 35. Fixed SPI Master Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID241	T_{DMO}	MOSI valid after Sclock driving edge	–	–	18	ns	–
SID242	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
SID243	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 36. Fixed SPI Slave Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID244	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID245	T_{DSO}	MISO valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	–
SID246	T_{DSO_ext}	MISO valid after Sclock driving edge in external clock mode	–	–	53	ns	$V_{DD} < 3.0$ V
SID247	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID248	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	–

Memory

Table 37. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID249	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
SID309	T_{WS48}	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
SID310	T_{WS32}	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
SID311	T_{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Table 38. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID250	$T_{ROWWRITE}$[5]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID251	$T_{ROWERASE}$[5]	Row erase time	–	–	13	ms	–
SID252	$T_{ROWPROGRAM}$[5]	Row program time after erase	–	–	7	ms	–
SID253	$T_{BULKERASE}$[5]	Bulk erase time (256 KB)	–	–	35	ms	–
SID254	$T_{DEVPROG}$[5]	Total device program time	–	–	50	seconds	For 256 KB
SID255	F_{END}	Flash endurance	100 K	–	–	cycles	–
SID256	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	–
SID257	F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	–

System Resources

Power-on-Reset (POR)

Table 39. POR DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID258	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	–
SID259	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	–
SID260	$V_{IPORHYST}$	Hysteresis	15	–	200	mV	–

Table 40. POR AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID264	T_{PPOR_TR}	PPOR response time in Active and Sleep modes	–	–	1	µs	–

Table 41. Brown-Out Detect

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID261	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
SID262	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.4	–	–	V	–

Table 42. Hibernate Reset

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID263	$V_{HBRTRIP}$	BOD trip voltage in Hibernate mode	1.1	–	–	V	–

Note

5. It can take as much as 20 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

Voltage Monitors

Table 43. Voltage Monitor DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID265	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
SID266	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
SID267	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
SID268	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
SID269	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
SID270	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
SID271	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
SID272	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
SID273	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
SID274	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
SID2705	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
SID276	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
SID277	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
SID278	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
SID279	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
SID280	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
SID281	LVI_IDD	Block current	–	–	100	µA	–

Table 44. Voltage Monitor AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID282	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	–

SWD Interface

Table 45. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID283	F_SWDCLK1	$3.3\ V \le V_{DD} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID284	F_SWDCLK2	$1.71\ V \le V_{DD} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID285	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID286	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID287	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
SID288	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 46. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID289	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–
SID290	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	–
SID291	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	–
SID292	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	–
SID293	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	–

Table 47. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID296	$F_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
SID297	$F_{IMOTOL3}$	IMO startup time	–	–	12	µs	–

Internal Low-Speed Oscillator

Table 48. ILO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID298	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

Table 49. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID299	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID300	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	–

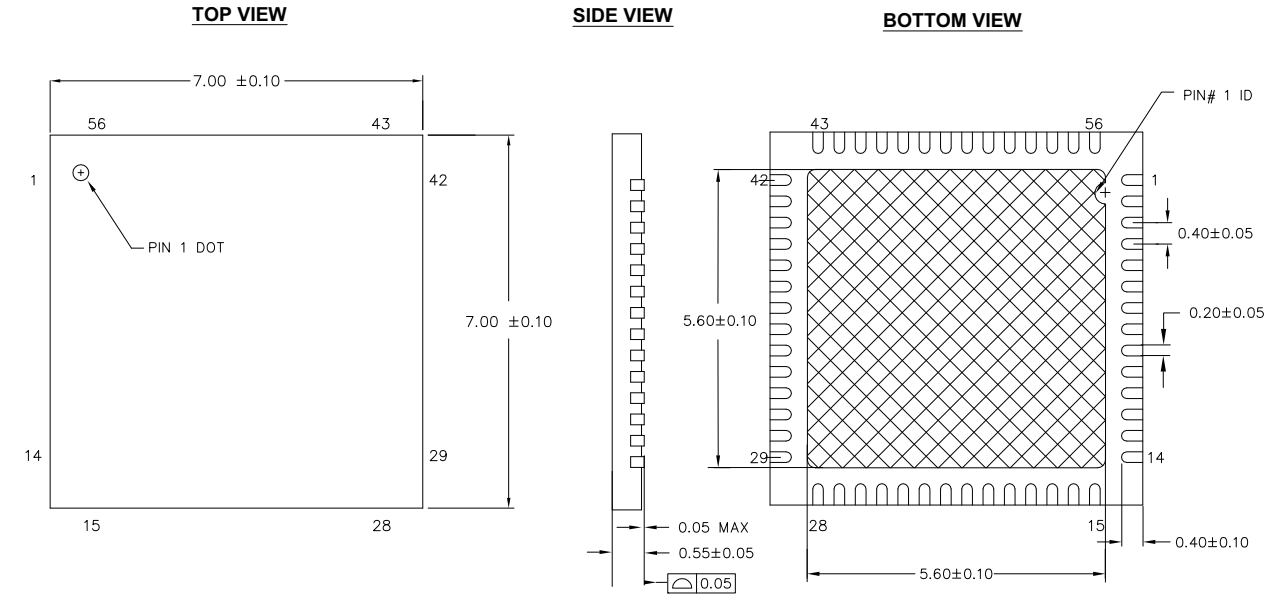
Table 50. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID301	ExtClkFreq	External clock input frequency	0	–	48	MHz	CMOS input level only
SID302	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	CMOS input level only

Table 51. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path performance							
SID303	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID304	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID305	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
PLD Performance in UDB							
SID306	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
Clock to Output Performance							
SID307	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typical	–	15	–	ns	–
SID308	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case	–	25	–	ns	–

Figure 8. 56-Pin QFN 7 × 7 × 0.6 mm



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 *C

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance.

Acronyms

Table 60. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

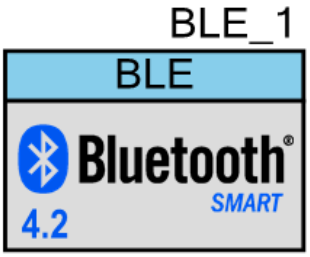
Units of Measure

Table 61. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Bluetooth Low Energy (BLE)

3.10



Features

- Bluetooth v4.2 compliant protocol stack
- Generic Access Profile (GAP) Features
  - Broadcaster, Observer, Peripheral and Central roles
  - Supports role reversal between Peripheral and Central
  - User-defined advertising data
  - Bonding support for up to four devices
  - Security modes 1 and 2
- Generic Attribute Profile (GATT) Features
  - GATT Client and Server
  - 16-, 32-, and 128-bit UUIDs
- Special Interest Group (SIG) adopted GATT-based Profiles and Services, and quick prototype of new profile design through intuitive GUI Custom Profile development; Support of Bluetooth Developer Studio Profile format
- Security Manager features
  - Pairing methods: Just works, Passkey Entry, Out of Band, Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
- Logical Link Adaption Protocol (L2CAP) Connection Oriented Channel
- Link Layer (LL) Features
  - Master and Slave role
  - 128-bit AES encryption
  - Low Duty Cycle Advertising
  - LE Ping

General Description

The Bluetooth Low Energy (BLE) Component provides a comprehensive GUI-based configuration window to facilitate designing applications requiring BLE connectivity. The Component incorporates a Bluetooth Core Specification v4.2 compliant protocol stack and provides APIs to enable user applications to access the underlying hardware via the stack.

When to use the BLE Component

BLE is used in very low power network and Internet of Things (IoT) solutions aimed for low-cost battery operated devices that can quickly connect and form simple wireless links. Target applications include HID, remote controls, sports and fitness monitors, portable medical devices and smart phone accessories, among many others that are being added to a long list of BLE supporting solutions.

SIG adopted Profiles and Services

The BLE Component supports numerous SIG-adopted GATT-based Profiles and Services. Each of these can be configured for either a GATT Client or GATT Server. The Component generates all the necessary code for a particular Profile/Service operation, as configured in the component Configure dialog.

The component can also support several Profiles at a time by adding the required Services of a Profile to a base Profile. For example, you can select HID as a base Profile. Then to add a Find Me Profile, add the Immediate Alert Service to the HID Profile.

See BLE Service-Specific APIs for a list of supported Profiles and Services.

Comprehensive APIs

The BLE Component provides application-level APIs to design solutions without requiring manual stack level configuration. The BLE Component API documentation is also provided in a separate HTML-based file.

Custom Profiles

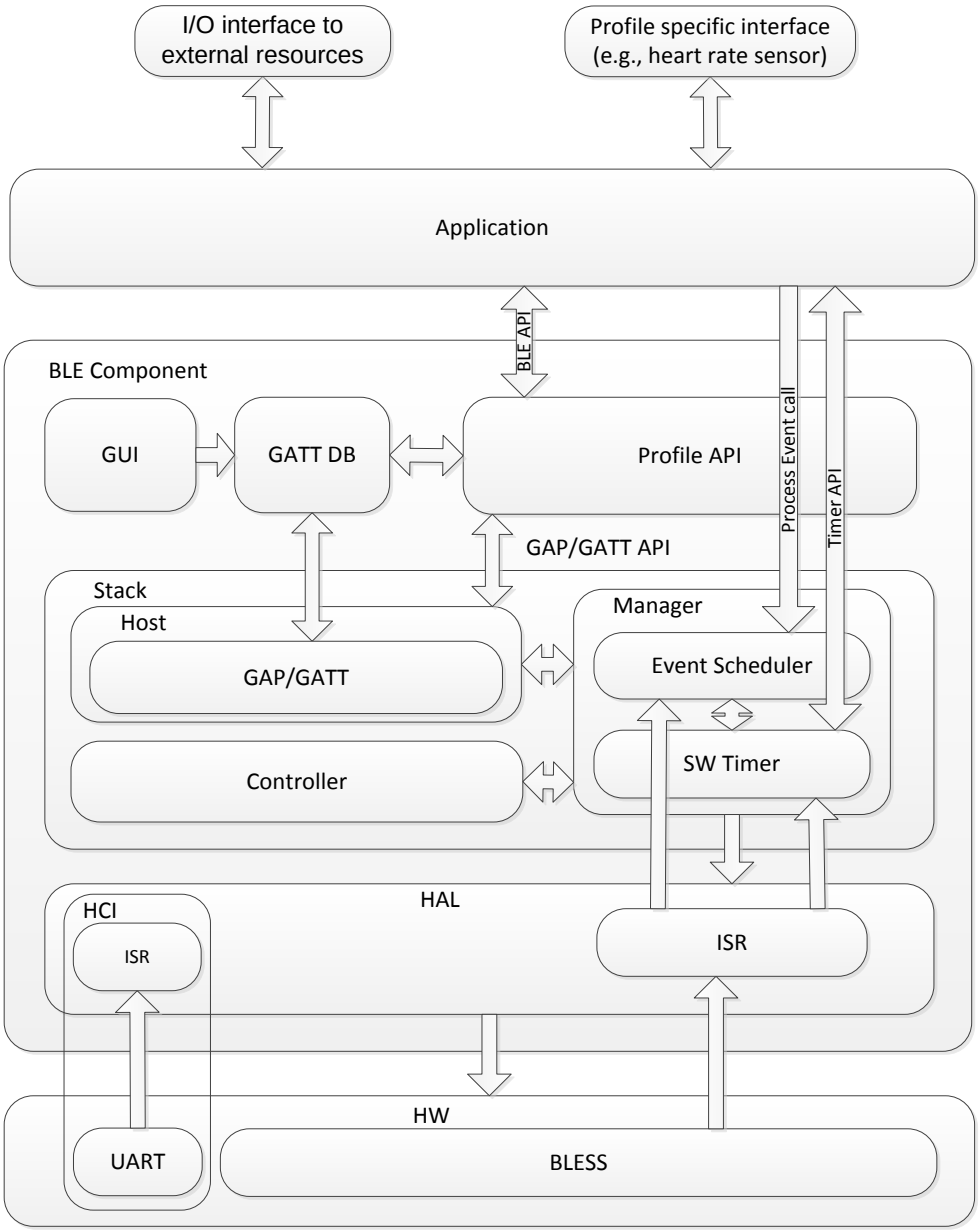
You can create custom Profiles that use existing Services, and you can create custom Services with custom Characteristics and Descriptors. There are no restrictions for GAP roles for a custom Profile.

Debug Support

For testing and debugging, the Component can be configured to HCI mode through a Component embedded UART. For over-the-air verification, Cypress CySmart Central Emulation Tool can be used for generic Bluetooth host stack emulation. To launch this tool, right click on the Component to bring up the context menu, and choose to deploy the CySmart Central Emulation Tool.

BLE Component Architecture

The BLE Component consists of the BLE Stack, BLE Profile, BLE Component Hardware Abstraction Layer (HAL), and the Link Layer. The following figure shows a high-level architecture of the BLE Component, illustrating the relationship between each of the layers and the route in which the application interacts with the Component. Note that the application is informed of the BLE events through the use of callback functions. You may build your state machine using these. Refer to the Callback Functions section for more details.



The following sub-sections give an overview of each of these layers.

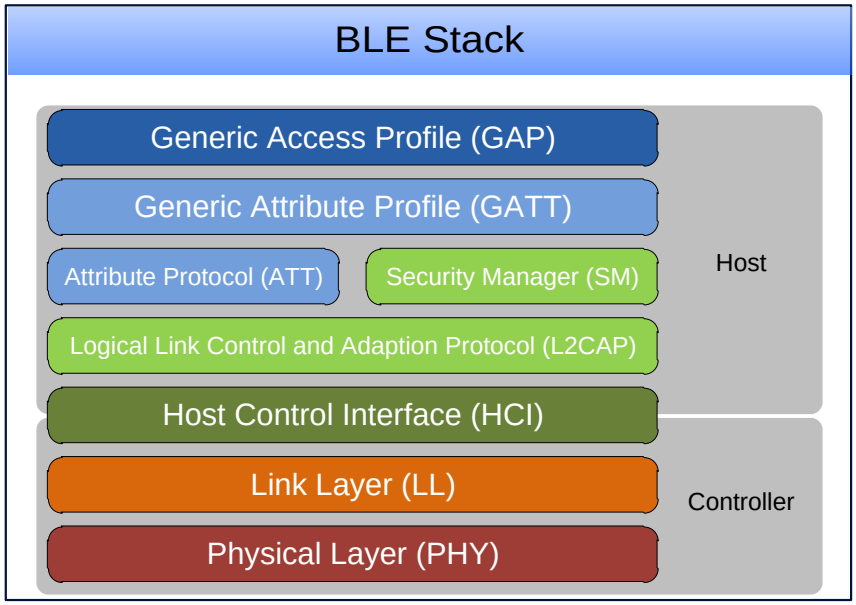
BLE Stack

The BLE stack implements the core BLE functionality as defined in the Bluetooth Core Specification 4.2. The stack is included as a precompiled library and it is embedded inside the BLE Component.

The BLE stack implements all the mandatory and optional features of Low Energy Single Mode compliant to Bluetooth Core Specification 4.2. The following table shows which Bluetooth Core Specification 4.2 features are supported by different devices.

Features	Devices with Bluetooth 4.1	Devices with Bluetooth 4.2
LE Secure connection	✓	✓
LL Privacy	-	✓
LE Data Length Extension	-	✓

The BLE Stack implements a layered architecture of the BLE protocol stack as shown in the following figure.



Generic Access Profile (GAP)

The Generic Access Profile defines the generic procedures related to discovery of Bluetooth devices and link management aspects of connecting to Bluetooth devices. In addition, this profile includes common format requirements for parameters accessible on the user interface level.

The Generic Access Profile defines the following roles when operating over the LE physical channel:

- **Broadcaster role:** A device operating in the Broadcaster role can send advertising events. It is referred to as a Broadcaster. It has a transmitter and may have a receiver.
- **Observer role:** A device operating in the Observer role is a device that receives advertising events. It is referred to as an Observer. It has a receiver and may have a transmitter.
- **Peripheral role:** A device that accepts the establishment of an LE physical link using any of the connection establishment procedures is termed to be in a "Peripheral role." A device operating in the Peripheral role will be in the "Slave role" in the Link Layer Connection State. A device operating in the Peripheral role is referred to as a Peripheral. A Peripheral has both a transmitter and a receiver.
- **Central role:** A device that supports the Central role initiates the establishment of a physical connection. A device operating in the "Central role" will be in the "Master role" in the Link Layer Connection. A device operating in the Central role is referred to as a Central. A Central has a transmitter and a receiver.

Generic Attribute Profile (GATT)

The Generic Attribute Profile defines a generic service framework using the ATT protocol layer. This framework defines the procedures and formats of services and their Characteristics. It defines the procedures for Service, Characteristic, and Descriptor discovery, reading, writing, notifying, and indicating Characteristics, as well as configuring the broadcast of Characteristics.

GATT Roles

- GATT Client: This is the device that wants data. It initiates commands and requests towards the GATT Server. It can receive responses, indications, and notifications data sent by the GATT Server.
- GATT Server: This is the device that has the data and accepts incoming commands and requests from the GATT Client and sends responses, indications, and notifications to a GATT Client.

The BLE Stack can support both roles simultaneously.

Attribute Protocol (ATT)

The Attribute Protocol layer defines a Client/Server architecture above the BLE logical transport channel. The attribute protocol allows a device referred to as the GATT Server to expose a set of attributes and their associated values to a peer device referred to as the GATT Client. These attributes exposed by the GATT Server can be discovered, read, and written by a GATT Client,

and can be indicated and notified by the GATT Server. All the transactions on attributes are atomic.

Security Manager Protocol (SMP)

Security Manager Protocol defines the procedures and behavior to manage pairing, authentication, and encryption between the devices. These include:

- Encryption and Authentication
- Pairing and Bonding
  - Pass Key and Out of band bonding
- Key Generation for a device identity resolution, data signing and encryption
- Pairing method selection based on the IO capability of the GAP central and GAP peripheral device

Logical Link Control Adaptation Protocol (L2CAP)

L2CAP provides a connectionless data channel. LE L2CAP provides the following features:

- Channel multiplexing, which manages three fixed channels. Two channels are dedicated for higher protocol layers like ATT, SMP. One channel is used for the LE-L2CAP protocol signaling channel for its own use.
- Segmentation and reassembly of packets whose size is up to the BLE Controller managed maximum packet size.
- Connection-oriented channel over a specific application registered using the PSM (protocol service multiplexer) channel. It implements credit-based flow control between two LE L2CAP entities. This feature can be used for BLE applications that require transferring large chunks of data.

Host Controller Interface (HCI)

The HCI layer implements a command, event, and data interface to allow link layer access from upper layers such as GAP, L2CAP, and SMP.

Link Layer (LL)

The LL protocol manages the physical BLE connections between devices. It supports all LL states such as Advertising, Scanning, Initiating, and Connecting (Master and Slave). It implements all the key link control procedures such as LE Encryption, LE Connection Update, LE Channel Update, and LE Ping. The Link Layer is a hardware-firmware co-implementation, where the key time critical LL functions are implemented in the LL hardware. The LL firmware maintains

and controls the key LL procedure state machines. It supports all the BLE chip specific low power modes.

The BLE Stack is a pre-compiled library in the BLE Component. The appropriate configuration of the BLE Stack library is linked during a build process based on application. The BLE Stack libraries are ARM Embedded Application Binary Interface (eabi) compliant and they are compiled using ARM compiler version 5.03.

The following table shows the mapping between the BLE Stack library to the user-configured Profile Role in Profile Mode or HCI Mode. Refer to the Generic Tab section for selection of stack configuration.

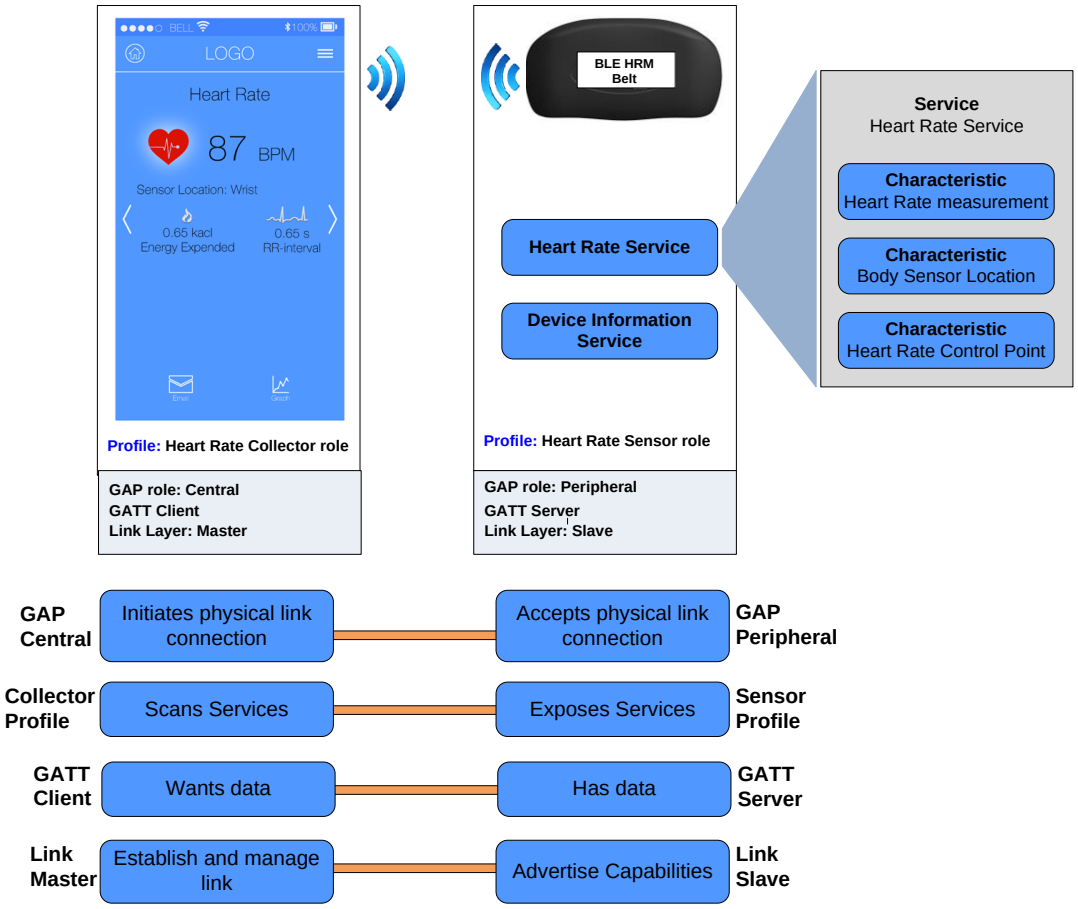
BLE Component Configuration	GAP Role	BLE Stack Library
BLE Profile	Central + Peripheral	CyBLEStack_BLE_SOC_CENTRAL_PERIPHERAL.a
BLE Profile	Central	CyBLEStack_BLE_SOC_CENTRAL.a
BLE Profile	Peripheral	CyBLEStack_BLE_SOC_PERIPHERAL.a
Broadcaster/Observer	Broadcaster	CyBLEStack_BLE_SOC_PERIPHERAL.a
Broadcaster/Observer	Observer	CyBLEStack_BLE_SOC_CENTRAL.a
HCI Mode	N/A	CyBLEStack_HCI_MODE_CENTRAL_PERIPHERAL.a

Profile Layer

In BLE, data is organized into concepts called Profiles, Services, and Characteristics.

- A **Profile** describes how devices connect to each other to find and use Services. It is a definition used by Bluetooth devices to describe the type of application and the general expected behavior of that device. See the Profile parameter for how to configure the BLE Component.
- A **Service** is a collection of data entities called Characteristics. A Service is used to define a certain function in a Profile. A Service may also define its relationship to other Services. A Service is assigned a Universally Unique Identifier (UUID). This is 16 bits for SIG adopted Services and 128 bits for custom Services. See the Toolbar section for information about adding Services to a Profile.
- A **Characteristic** contains a Value and the Descriptor that describes a Characteristic Value. It is an attribute type for a specific piece of information within a Service. Like a Service, each Characteristic is designated with a UUID; 16 bits for SIG adopted Characteristics and 128 bits for custom Characteristics. See the Toolbar section for information about adding Characteristics and Descriptors.

The following diagram shows the relationship between Profiles, Services, and Characteristics in a sample BLE heart rate monitor application using a Heart Rate Profile.



The Heart Rate Profile contains a Heart Rate Service and a Device Information Service. Within the Heart Rate Service, there are three Characteristics, each containing different information. The device in the diagram is configured as a Sensor role, meaning that in the context of the Heart Rate Profile, the device is a GAP Peripheral and a GATT Server. These concepts are explained in the BLE Stack description.

The Profile layer is generated by PSoC Creator using the parameter configurations specified in the GUI. The Profile implements the Profile specific attribute database and APIs required for the application. You can choose to configure the standard SIG adopted Profile and generate a design or define a Custom Profile required by an application. The GUI also allows import/export of a Profile design in XML format for Profile design reuse. In addition, the Bluetooth Developer Studio compliant XML format is available.

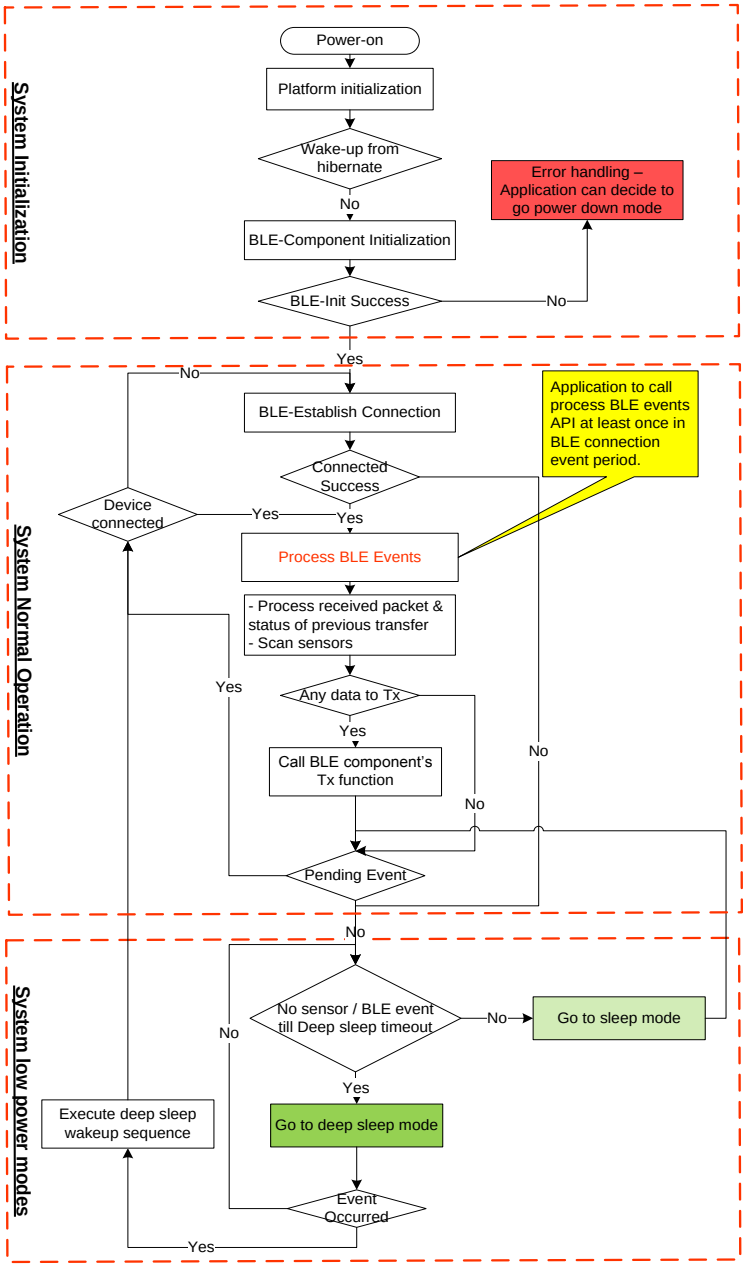
Hardware Abstraction Layer (HAL)

The HAL implements the interface between the BLE stack and the underlying hardware. This layer is meant for the stack only and is not advisable to modify it.

Functional Description

Operation Flow

A typical application code consists of three separate stages: Initialization, Normal operation, and Low power operation.



Once the Component is initialized, it enters normal operation and periodically enters various degrees of low power operation to conserve power. Hence initialization should only happen at

LFCLK configuration

The LFCLK configuration as set in the **Clocks** tab of the Design-Wide Resources (*<project>.cydwr*) file affects the BLE Component's ability to operate in Deep Sleep Mode. If the WCO is chosen, then the Component Deep Sleep Mode is available for use. However, if the ILO is chosen, then the Component cannot enter Deep Sleep.

Note The LFCLK is used in the BLE Component only during Deep Sleep Mode and hence the ILO inaccuracy does not affect the BLE communication.

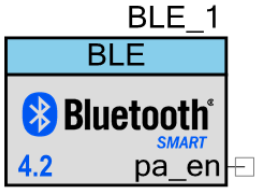
Unsupported Features

The BLE Component stack does not support the following optional Bluetooth v4.2 protocol features, as listed in Vol 6, Part B, section 4.6 of the specification:

- Connection Parameters Request Procedure (Vol 6, Part B, section 4.6.2)
- Extended Reject Indication (Vol 6, Part B, section 4.6.3)
- Slave-initiated Features Exchange (Vol 6, Part B, section 4.6.4)

Input/Output Connections

This section describes the input and output connections for the BLE. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.



pa_en – Output *

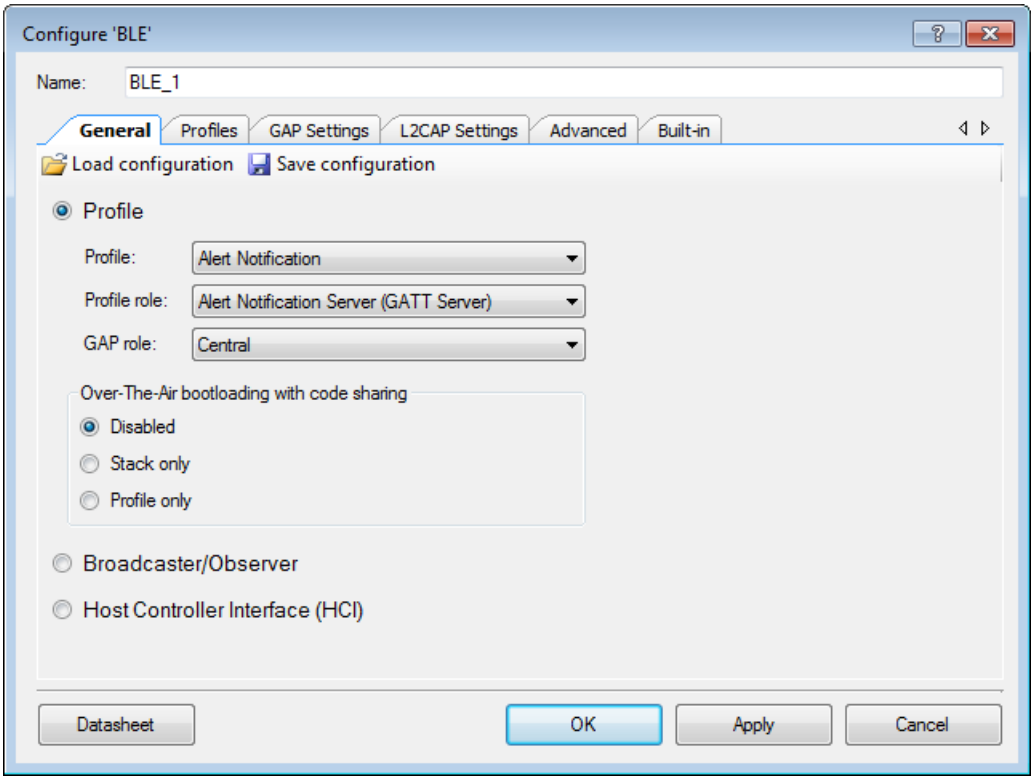
The power amplifier enable (pa_en) output allows you to connect a high active external power amplifier to the device. This output can be routed to the P5[0] digital output pin only. This output is visible if the **Enable external Power Amplifier control** parameter is selected on the **Advanced** tab.

Component Parameters

Drag a BLE Component onto your design and double-click it to open the Configure dialog. This dialog has the following tabs with different parameters.

General Tab

The **General** tab allows general configuration of the BLE Component. This tab contains tools to load and save configurations as also three main areas for the type of configuration.



Load Configuration/Save Configuration

Use the **Load Configuration** button to load the previously saved xml Component configuration; use the Save Configuration button to save the current configuration for use in other designs. It is possible to import and export the customizer configuration in xml format.

Note In order to load or save a Profile in the **Bluetooth Developer Studio** compliant format, use **Load BDS Profile** and **Save Profile in BDS format** toolbar commands on the **Profiles** tab.

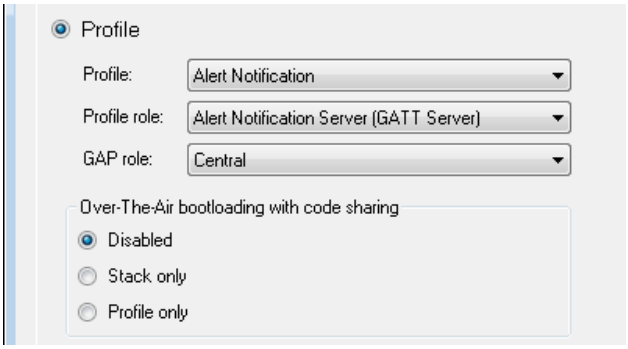
Mode Selection

On the main part of this tab, there are three options to select a mode:

- Profile
- Broadcaster/Observer
- Host Controller Interface

General Tab – Profile

The Profile mode is used to select the target Profile, Profile role, and GAP role, as well as Over-The-Air (OTA) Bootloading options.



Profile

The **Profile** option is used to choose the target Profile from a list of supported Profiles. See Profile, Service, and Characteristic. The following Profiles are available for selection:

Alert Notification

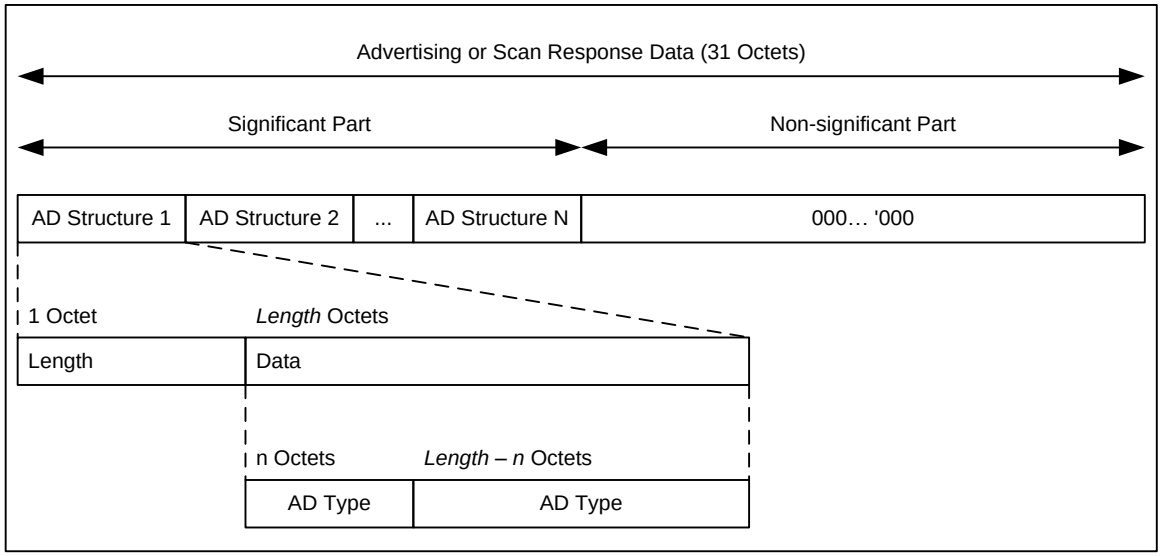
This Profile enables a GATT Client device to receive different types of alerts and event information, as well as information on the count of new alerts and unread items, which exist in the GATT Server device.

- **Alert Notification Server** Profile role – Specified as a GATT Server. Requires the following Service: **Alert Notification Service**.
  - Central GAP role
  - Peripheral and Central GAP role
- **Alert Notification Client** Profile role – Specified as a GATT Client.
  - Peripheral GAP role
  - Peripheral and Central GAP role

Refer to the Alert Notification Profile Specification for detailed information about the Alert Notification Profile.

Advertisement / Scan response data settings

Advertisement (AD) or **Scan response data** packet is a 31 byte payload used to declare the device's BLE capability and its connection parameters. The structure of this data is shown below as specified in the Bluetooth specification.



The data packet can contain a number of AD structures. Each of these structures is composed of the following parameters.

- **AD Length**: Size of the **AD Type** and **AD Data** in bytes.
- **AD Type**: The type of advertisement within the AD structure.
- **AD Data**: Data associated with the **AD Type**.

The total length of a complete Advertising packet cannot exceed 31 bytes.

An example structure for **Advertisement data** or **Scan response data** is as follows.

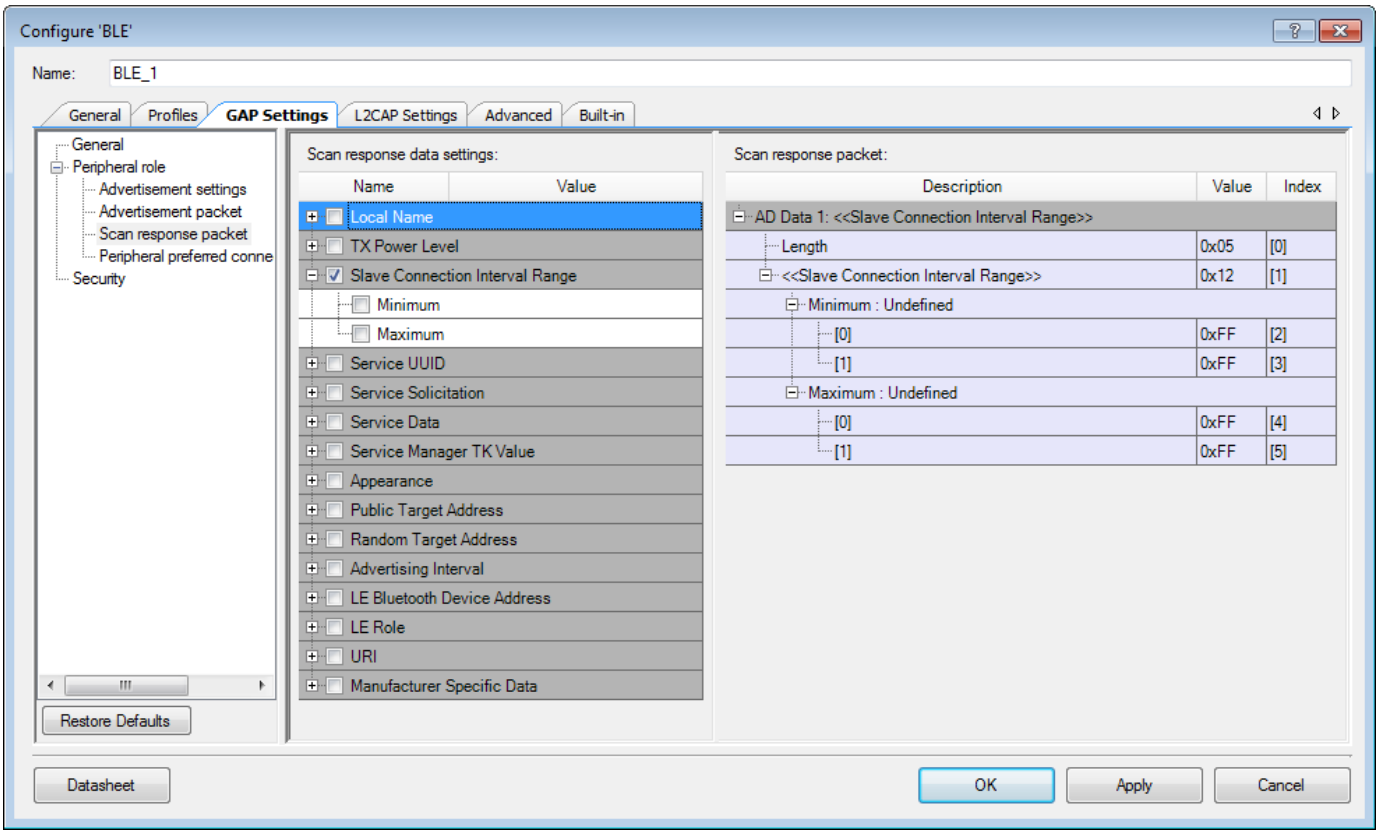
- AD Structure Element Definition:
  - **AD Length**: Size of **AD Type** and associated **AD Data** = 5 bytes
  - **AD Type** (1 byte): 0x03 (Service UUID)
  - **AD Data** (4 bytes): 0x180D, 0x180A (Heart Rate Service, Device Information Service)

The following table shows the **AD Types**.

AD Type	Description
Flags	Flags to broadcast underlying BLE transport capability such as Discoverable mode, LE only, etc.
Local Name	Device Name (complete of shortened). The device name value comes from the **Device name** field on the **GAP Settings** tab, under **General**.
Tx Power Level	Transmit Power Level. Taken from the **Adv/Scan TX power level** field on the **GAP Settings** tab, under **General.**
Slave Connection Interval Range	Preferred connection interval range for the device. Not available in **Broadcaster** GAP role.
Service UUID	List of Service UUIDs to be broadcasted that the device has implemented. There are different AD Type values to advertise 16-bit, 32-bit and 128-bit Service UUIDs. 16-bit and 32-bit Service UUIDs are used if they are assigned by the Bluetooth SIG.
Service Solicitation	List of Service UUIDs from the central device that the peripheral device would like to use. There are different AD Type values to advertise 16-bit, 32-bit and 128-bit Service UUIDs.
Service Data	2/4/16-byte Service UUID, followed by additional Service data.
Security Manager TK value	Temporal key to be used at the time of pairing. Not available in **Broadcaster** GAP role.
Appearance	The external appearance of the device. The value comes from the **Appearance** field on the **GAP Settings** tab, under **General**.
Public Target Address	The public device address of intended recipients.
Random Target Address	The random device address of intended recipients.
Advertising Interval	The Advertising interval value that is calculated as an average of Fast advertising interval minimum and maximum values configured on the **GAP Settings** tab, under **Advertisement Settings**.
LE Bluetooth Device Address	The device address of the local device. The value comes from the **Public** d**evice address** field on the **GAP Settings** tab, under **General**.
LE Role	Supported LE roles. Not available in **Broadcaster** GAP role.
URI	URI, as defined in the IETF STD 66.
Manufacturer Specific Data	2 bytes company identifier followed by manufacturer specific data.

GAP Settings Tab – Scan response packet

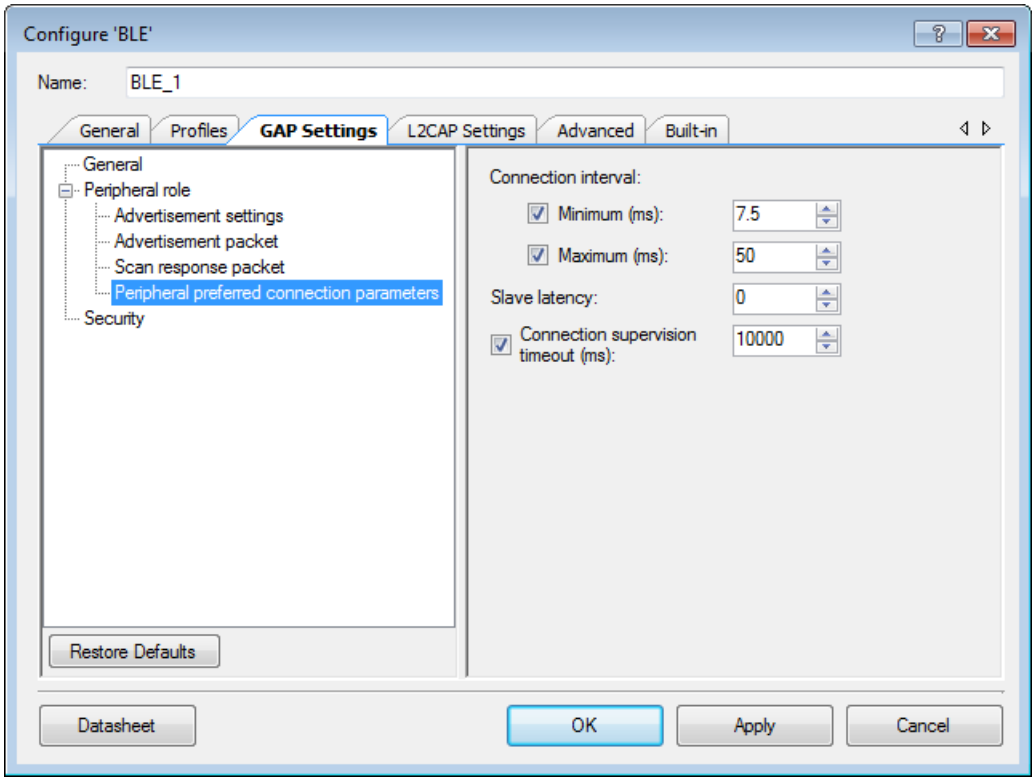
This section displays when the device is configured to contain a "Peripheral," "Broadcaster," or "Peripheral and Central" **GAP role**. It is used to configure the Scan response data packet to be used in response to device scanning performed by a GATT Client device.



The packet structure of a Scan response packet is the same as an Advertisement packet. See Advertisement / Scan response data settings for information on configuring the Scan response packet.

GAP Settings Tab – Peripheral preferred connection parameters

These parameters define the preferred BLE interface connection settings of the Peripheral. After establishing a connection, the Central device may read these settings and update the BLE interface connection parameters accordingly.



Note The scaled values of these parameters used internally by the BLE stack are also shown in the **Peripheral Preferred Connection Parameters** on the **Profiles** tab. These are the actual values sent over the air.

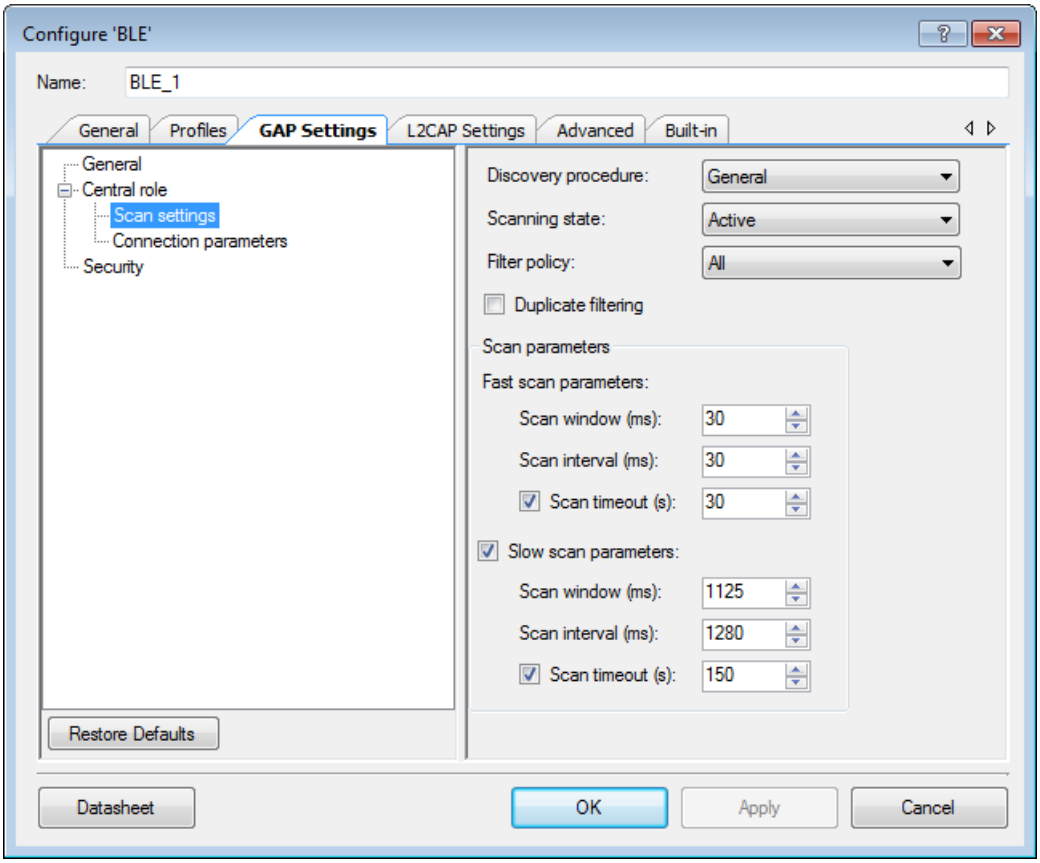
- **Connection interval –** The Central device connecting to a Peripheral device needs to define the time interval for a connection to happen.
  - Minimum (ms): This parameter is the minimum permissible connection time value to be used during a connection event. It is configured in steps of 1.25 ms. The range is from 7.5 ms to 4000 ms. Unchecked means no specific minimum.
  - Maximum (ms): This parameter is the maximum permissible connection time value to be used during a connection event. It is configured in steps of 1.25 ms. The range is from 7.5 ms to 4000 ms. Unchecked means no specific maximum.
- **Slave Latency –** Defines the latency of the slave in responding to a connection event in consecutive connection events. This is expressed in terms of multiples of connection intervals, where only one connection event is allowed per interval. The range is from 0 to 499 events.

- **Connection Supervision Timeout –** This parameter defines the LE link supervision timeout interval. It defines the timeout duration for which an LE link needs to be sustained in case of no response from peer device over the LE link. The time interval is configured in multiples of 10 ms. Unchecked means no specific value. The range is from 100 ms to 32000 ms.

  Note that for proper operation the Connection Supervision Timeout must be larger than **(1 + Slave latency) * Connection Interval * 2** (ms). Refer to Bluetooth Core Specification 4.2 Volume 6, Part B, Chapter 4.5.2 for more information on Connection Supervision Timeout.

GAP Settings Tab – Scan settings

These parameters are available when the device is configured as a "Central," "Peripheral and Central," or “Observer” **GAP role**. Typically during a device discovery, the GATT Client device initiates the scan procedure. It uses **Fast scan parameters** for a period of time, approximately 30 to 60 seconds, and then it reduces the scan frequency using the **Slow scan parameters**.



Note The scan interval needs to be aligned with the user-selected Profile specification.

Discovery procedure

- **Limited –** A device performing this procedure shall discover the device doing limited discovery mode advertising only.
- **General –** A device performing this procedure shall discover the devices doing general and limited discovery advertising.

Scanning state

- **Passive –** In this state a device can only listen to advertisement packets.
- **Active –** In this state a device may ask an advertiser for additional information.

Filter policy

This parameter defines how the advertisement packets are filtered.

- **All** – Process all advertisement packets.
- **White List Only** – Process advertisement packets only from devices in the White List.

Duplicate filtering

When enabled, this activates filtering of duplicated advertisement data. If disabled, the BLE stack will not perform filtering of advertisement data.

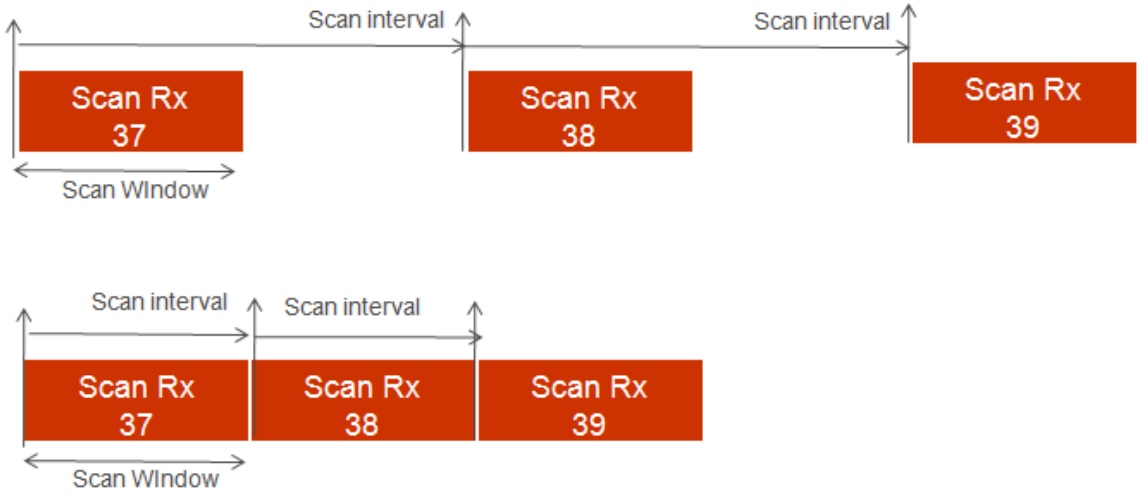
Scan parameters

These parameters define the scanning time and interval between scanning events. Two different sets of Scan parameters are used: **Fast scan parameters** and **Slow scan parameters**. Typically after the device initialization, a central device uses the Fast scan parameters. After the **Fast scan timeout** value expires, and if a connection with a Peripheral device is not established, then the Profile switches to Slow scan parameters to save the battery life. After the **Slow scan timeout** value expires, 'CYBLE_EVT_GAPC_SCAN_START_STOP ' event is generated. See API documentation.

- **Fast scan parameters** – This connection type results in a faster connection between the GATT Client and Server devices than it is possible using a normal connection.
  - **Scan Window**: This parameter defines the scan window when operating in **Fast connection**. The parameter is configured to increment in multiples of 0.625 ms. Valid range is from 2.5 ms to 10240 ms. **Scan Window** must be less than the **Scan Interval**. Default: 30 ms.
  - **Scan Interval**: This parameter defines the scan interval when operating in **Fast connection**. The parameter is configured to increment in multiples of 0.625 ms. Valid range is from 2.5 ms to 10240 ms. Default: 30 ms.

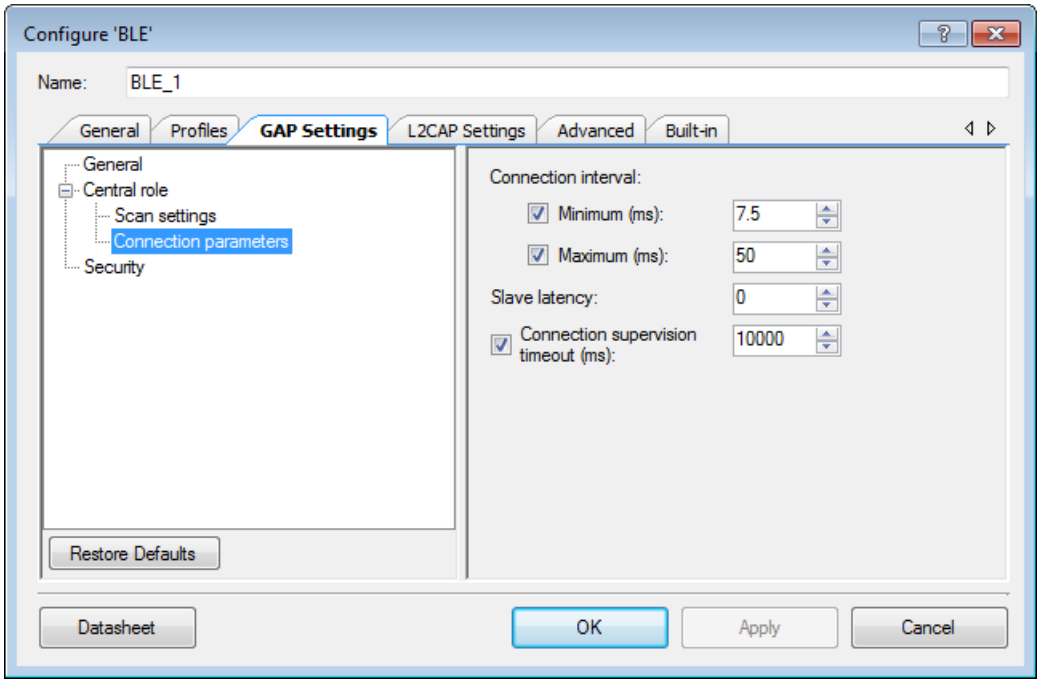
- **Scan Timeout**: The timeout value of scanning with fast scan parameters. Default: 30 s. When unchecked, the device is scanning continuously. The timeout cannot occur before the scanning interval is expired, that is why if a timeout value is less than slow scanning interval minimum value, a warning is displayed.

- **Slow scan parameters** – This connection results in a slower connection between the GATT Client and GATT Server devices than is possible using a normal connection. However this method consumes less power.
  - **Scan Window**: This parameter defines the scan window when operating in **Slow Connection**. The parameter is configured to increment in multiples of 0.625ms. Valid range is from 2.5 ms to 10240 ms. **Scan Window** must be less than the **Scan Interval**. Default: 1125 ms.
  - **Scan Interval**: This parameter defines the scan interval when operating in **Slow Connection**. The parameter is configured to increment in multiples of 0.625 ms. Valid range is from 2.5 ms to 10240 ms. Default: 1280 ms.
  - **Scan Timeout**: The timeout value of scanning with slow scan parameters. Default: 150 s. When unchecked, the device is scanning continuously. The timeout cannot occur before the scanning interval is expired, that is why if a timeout value is less than slow scanning interval minimum value, a warning is displayed.



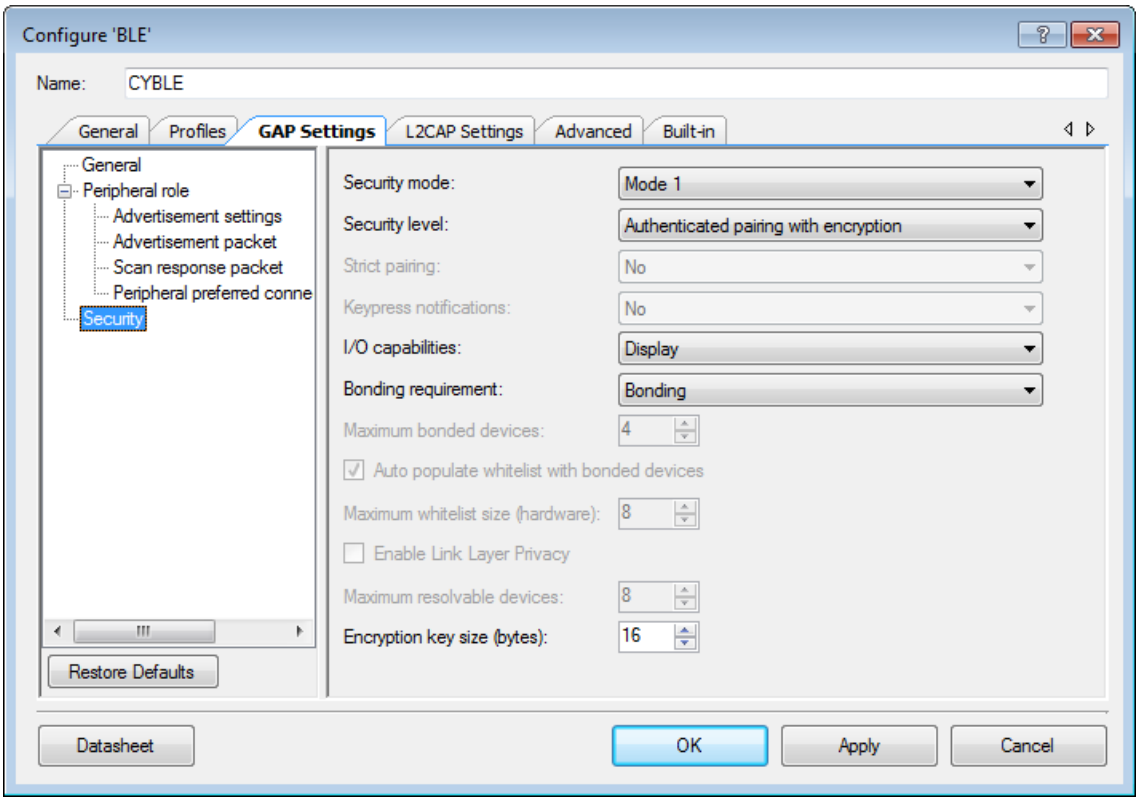
GAP Settings Tab – Connection parameters

This section is the same as Peripheral Preferred Connection Parameters for Advertisement Settings. The only difference is that Central connection parameters will not be shown on the **Peripheral Preferred Connection parameters** on the **Profile** tab.



GAP Settings Tab – Security

This section contains several parameters to configure the global security options for the Component. These parameters are configurable only in **Profile** mode. If the device is configured as a GATT Server, you can optionally set each Characteristic using its own unique security setting in the **Profile Tree**.



Security mode

Defines GAP security modes for the Component. Both available modes may support authentication.

- Mode 1 – Used in designs where data encryption is required.
- Mode 2 – Used in designs where data signing is required.

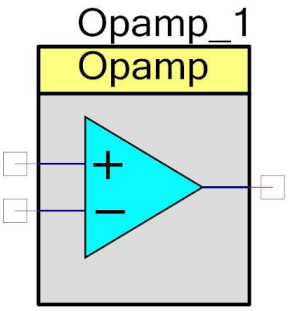
Security level

Enables different levels of security depending on the selected **Security mode**:

- If Mode1 is selected, then the following security levels are available.
  - No Security – With this level of security, the device will not use encryption or authentication.

PSoC 4 Operational Amplifier (Opamp)

1.20



Features

- Follower or Opamp configuration
- Rail-to-rail inputs and output
- Output direct low resistance connection to pin
- 1mA or 10mA output current
- Internal connection for follower

General Description

The Opamp operates as an off-the-shelf operation amplifier. A direct connection is made between the Opamp output and a dedicated GPIO pin for a low output resistance. Two output modes (Internal only and Output to pin) are provided to drive internal or external signals respectively. The Output to pin may drive both internal (SAR component) and external signals. The user also has control of different overall power levels that provide a tradeoff between power and bandwidth.

For all devices, except PSoC 4100/PSoC 4200, the Opamp can operate in Deep Sleep power mode.

Note External resistors are required to perform amplification.

When to Use the Opamp

The following is a list of common use cases for the Opamp component:

- Gain for SAR ADC
- High impedance buffer for SAR ADC
- General purpose signal amplifier
- Active filter

Input/Output Connections

This section describes various input and output connections for the Opamp.

Positive Input – Analog Input

When the Opamp is configured in follower Mode, this I/O is the voltage input. If the Opamp is configured in Opamp Mode, this I/O acts as the standard Opamp noninverting input.

Negative Input – Analog Input*

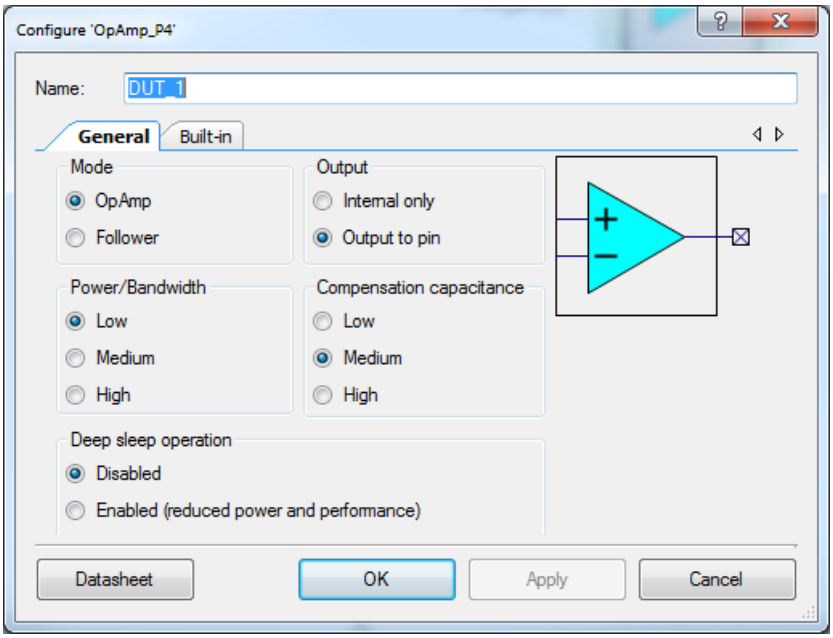
When the Opamp component is configured in Opamp Mode, this I/O is the normal inverting input. When the Opamp is configured in Follower Mode, this I/O is hard-connected to the output and the I/O is unavailable.

Vout – Analog output

The output can be directly connected to a pin and/or routed to an internal load using the Output parameter. The drive strength is selectable as either Output to pin or Internal only. Connections to pins require the Output to pin setting. Internal connections can operate with either the Internal only or Output to pin setting, but should normally be configured for Internal only.

Component Parameters

Drag Opamp onto your design and double-click it to open the Configure dialog.



The Opamp provides the following parameters:

Mode

This parameter allows you to select between two configurations: **Opamp** and **Follower**. **Opamp** is the default configuration. In this mode, all three terminals are available for connection. In the follower mode, the inverting input is internally connected to the output to create a voltage follower.

Power/Bandwidth

The Opamp works over a wide range of operating currents. Higher operating current increases the Opamp bandwidth. The **Power/Bandwidth** parameter allows you to select the power level: High, Medium, and Low.

Output

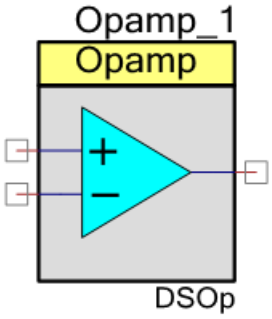
This parameter selects an output mode: Internal only – internal connections or Output to pin – connection to pin (external).

Compensation

The opamp offers three compensation settings: Low, Med and High. This allows reducing the compensation (hence increase the bandwidth) when the Opamp's loop gain is reduced.

Deep sleep operation

This parameter is not available for PSoC 4100/PSoC 4200 devices. It enables the component operation in Deep Sleep mode. If this option is enabled, a "DSOp" label will be displayed under the symbol. If two Opamps of the same CTB/CTBm block are used in the project, both must have the same Deep Sleep settings.



Note Only dedicated pins may be used for operation in Deep Sleep mode.

Note For correct operation in Deep Sleep mode, the V_{DDA} must be larger than 2.5 V. The boost pump does not operate in Deep Sleep mode.

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name "Opamp_1" to the first instance of a component in a given design. You can rename it to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "Opamp"

Functions

Function	Description
Opamp_Start()	Performs all of the required initialization for the component and enables power to the block.
Opamp_Stop()	Turns off the Opamp block.
Opamp_Init()	Initializes or restores the component according to the customizer Configure dialog settings.
Opamp_Enable()	Activates the hardware and begins component operation.
Opamp_SetPower()	Sets the drive power to one of three settings; LOW_POWER, MED_POWER, HIGH_POWER.
Opamp_PumpControl()	Turn the boost pump on or off.
Opamp_Sleep()	This is the preferred API to prepare the component for sleep.
Opamp_Wakeup()	This is the preferred API to restore the component to the state when Opamp_Sleep() was called.

void Opamp_Start(void)

Description: Performs all of the required initialization for the component and enables power to the block. The first time the routine is executed, the Power level, Mode, and Output mode are set. When called to restart the Opamp following a Stop() call, the current component parameter settings are retained.

Parameters: None

Return Value: None

Side Effects: None

void Opamp_Stop(void)

Description: Turn off the Opamp block.

Parameters: None

Return Value: None

Side Effects: Does not affect the Opamp mode or power settings

void Opamp_Init(void)

Description: Initializes or restores the component according to the customizer Configure dialog settings. It is not necessary to call Init() because the Start() API calls this function and is the preferred method to begin the component operation.

Parameters: None

Return Value: None

Side Effects: All the registers will be set to values according to the customizer Configure dialog.

void Opamp_Enable(void)

Description: Activates the hardware and begins the component operation. It is not necessary to call Enable() because the Start() API calls this function, which is the preferred method to begin component operation.

Parameters: None

Return Value: None

Side Effects: None

void Opamp_SetPower(uint32 power)

Description: Sets the opamp to one of three power levels..

Parameters: (uint32) power: Power levels. See table below.

Parameter Value	Description
Opamp_LOW_POWER	Lowest active power.
Opamp_MED_POWER	Medium power.
Opamp_HIGH_POWER	Highest active power.

Return Value: None

void Opamp_PumpControl(uint32 onOff)

Description: Allows the user to turn the Opamp's boost pump on or off. By Default the Opamp_Start() function turns on the pump. Use this command to turn it off. The boost must be turned on when the supply is less than 2.7 volts and off if the supply is more than 4 volts.

Parameters: (uint32) onOff: Control the pump. See the table below.

Parameter Value	Description
Opamp_PUMP_OFF	Turn off the pump
Opamp_PUMP_ON	Turn on the pump

Return Value: None

Side Effects: Turning this pump off will reduce the Opamp input range by 1.8 volts or (Vssa to (Vdda – 1.8 volts)).

void Opamp_Sleep(void)

Description: This is the preferred API to prepare the component for sleep. The Sleep() API saves the current component state and stops the component. Call the Sleep() function before calling the CySysPmDeepSleep() or the CySysPmHibernate() functions. If the "Deep sleep operation" is enabled then this function does nothing and the component continues to operate during low power state.

Parameters: None

Return Value: None

Side Effects: None

void Opamp_Wakeup(void)

Description: This is the preferred API to restore the component to the state when Sleep() is called. If the component has been enabled before the Sleep() function is called, the Wakeup() function will also re-enable the component. If the "Deep sleep operation" is enabled then this function does nothing because the component operates during low power state as well as in active state.

Parameters: None

Return Value: None

Side Effects: Calling the Wakeup() function without first calling the Sleep() function may produce unexpected behavior.

Sample Firmware Source Code

PSoC Creator provides numerous example projects that include schematics and example code in the Find Example Project dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or **File** menu. As needed, use the **Filter Options** in the dialog to narrow the list of projects available to select.

Refer to the "Find Example Project" topic in the PSoC Creator Help for more information.

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined:

- project deviations – deviations that are applicable for all PSoC Creator components
- specific deviations – deviations that are applicable only for this component

This section provides information on the component-specific deviations. The project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The Opamp component has the following specific deviations:

MISRA-C: 2004 Rule	Rule Class (Required/Advisory)	Rule Description	Description of Deviation(s)
19.7	A	A function is used in preference to a function-like macro.	Deviated since function-like macros are used to allow more efficient code.

API Memory Usage

The component memory usage varies significantly, depending on the compiler, device, number of APIs used and component configuration. The following table provides the memory usage for all APIs available in the given component configuration.

The measurements have been done with the associated compiler configured in the Release mode with an optimization set for Size. For a specific design, the map file generated by the compiler can be analyzed to determine the memory usage.

PSoC 4 (GCC)

Configuration		Flash Bytes	SRAM Bytes
Deep sleep operation	Disabled	240	9
	Enabled	188	8

Functional Description

This component is a basic operational amplifier. You may configure power, output strength, and interconnect the Opamp to other components. Low resistive connections are made from the Opamp to three selected pins to provide the optimal performance.

Using the Compensation option

There are recommended settings for the Compensation option:

Loop Gain	Load Capacitance	
	Less than 50 pF	50pF to 125 pF
1-6	Medium	High
7 or more	Low	Medium

These settings are applicable for the Output to pin setting, which is capable to drive a pin. 125 pF is the maximum load capacitance for this output.

Placement

Each Opamp is directly connected to specific GPIOs along with being connected to the internal fabric. The Output connection to a GPIO requires the use of the directly connected pin. Refer to the device datasheet for the part being used for the specific physical pin connections.

Registers

See the chip Technical Reference Manual (TRM) for more information about the registers.

Component Debug Window

PSoC Creator allows viewing debug information about the components in the design. Each component window lists the memory and registers for the instance. For detailed hardware registers descriptions, refer to the appropriate device technical reference manual. For detailed UDB registers descriptions used in the component, refer to the Registers section of this datasheet.

To open the Component Debug window:

1. Make sure the debugger is running or in break mode.
2. Choose **Windows > Components…** from the **Debug** menu.
3. In the Component Window Selector dialog, select the component instances to view and click **OK**.

The selected Component Debug window(s) will open within the debugger framework. Refer to the "Component Debug Window" topic in the PSoC Creator Help for more information.

Resources

The Opamp uses one of the opamp (Constant Time Block – mini (CTBm)) blocks in PSoC 4. No other resources are required.

DC and AC Electrical Characteristics

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Note Final characterization data for PSoC 4000S, PSoC 4100S and PSoC Analog Coprocessor devices is not available at this time. Once the data is available, the component datasheet will be updated on the Cypress web site..

DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
IDD	Opamp Block current. No load.		–	–	–	–
IDD_HI	Power = high		–	1000	1300	µA
IDD_MED	Power = medium		–	320	500	µA
IDD_LOW	Power = low		–	250	350	µA
IDD	Opamp Block current. VDD = 1.8 V. No load.	For PSoC 4200 BLE family	–	–	–	–
IDD_HI	Power = high	For PSoC 4200 BLE family	–	1000	1300	µA
IDD_MED	Power = medium	For PSoC 4200 BLE family	–	500	–	µA
IDD_LOW	Power = low	For PSoC 4200 BLE family	–	250	350	µA
IDD_HI	Power = high	For PSoC 4100M/ PSoC 4200M/ PSoC 4200L	–	1100	1850	µA
IDD_MED	Power = medium	For PSoC 4100M/ PSoC 4200M/ PSoC 4200L	–	550	950	µA
IDD_LOW	Power = low	For PSoC 4100M/ PSoC 4200M/ PSoC 4200L	–	150	350	µA
IOUT_MAX	VDDA ≥ 2.7 V, 500 mV from rail		–	–	–	–
IOUT_MAX_HI	Power = high		10	–	–	mA
IOUT_MAX_MID	Power = medium		10	–	–	mA
IOUT_MAX_LO	Power = low		–	5	–	mA
IOUT	VDDA = 1.71 V, 500 mV from rail		–	–	–	–

Parameter	Description	Conditions	Min	Typ	Max	Units
IOUT_MAX_HI	Power = high		4	–	–	mA
IOUT_MAX_MID	Power = medium		4	–	–	mA
IOUT_MAX_LO	Power = low		–	2	–	mA
VIN	Charge pump on, VDDA ≥ 2.7 V		–0.05	–	VDDA – 0.2	V
VCM	Charge pump on, VDDA ≥ 2.7 V		–0.05	–	VDDA – 0.2	V
VOUT	VDDA ≥ 2.7 V		–	–	–	
VOUT_1	Power = high, Iload=10 mA		0.5	–	VDDA – 0.5	V
VOUT_2	Power = high, Iload=1 mA		0.2	–	VDDA – 0.2	V
VOUT_3	Power = medium, Iload=1 mA		0.2	–	VDDA – 0.2	V
VOUT_4	Power = low, Iload=0.1mA		0.2	–	VDDA – 0.2	V
VOS	Offset voltage	High mode	1	±0.5	1	mV
VOS	Offset voltage	Medium mode	–	±1	–	mV
VOS	Offset voltage	Low mode	–	±2	–	mV
VOS_DR	Offset voltage drift	High mode	–10	±3	10	µV/C
VOS_DR	Offset voltage drift	Medium mode	–	±10	–	µV/C
VOS_DR	Offset voltage drift	Low mode	–	±10	–	µV/C
Cload	Stable up to maximum load. Performance specs at 50 pF.		–	–	125	pF
CMRR	DC	VDDD = 3.6 V	70	80	–	dB
CMRR	DC	For PSoC 4200 BLE family VDDD = 3.6 V, High-Power Mode	65	70	–	dB
CMRR	DC Common mode rejection ratio. High Power mode. Common Model Voltage Range from 0.5V to VDDA - 0.5V.	For PSoC 4100M/ PSoC 4200M/ PSoC 4200L VDDD = 3.6 V	60	70	–	dB
PSRR	At 1 kHz, 100 mV ripple	VDDD = 3.6 V	70	85	–	dB
Deep-Sleep Mode (For PSoC 4200 BLE family; only guaranteed for VDDA > 2.5 V)						
IDD_DS	Current		–	15	–	µA
Vos_DS	Offset voltage		–	5	–	mV
Vos_dr_DS	Offset voltage drift		–	20	–	µV/°C

Parameter	Description	Conditions	Min	Typ	Max	Units
Vout_DS	Output voltage		0.2	–	VDD–0.2	V
Vcm_DS	Common mode voltage		0.2	–	VDD–1.8	V
Deep-Sleep Mode (For PSoC 4100M/PSoC 4200M/ PSoC 4200L; only guaranteed for VDDA ≥ 2.7 V) Mode 2 is lowest current range. Mode 1 has higher GBW.						
IDD_HI_M1	Mode 1, High current	25 °C	-	1400	-	uA
IDD_MED_M1	Mode 1, Medium current	25 °C	-	700	-	uA
IDD_LOW_M1	Mode 1, Low current	25 °C	-	200	-	uA
IDD_HI_M2	Mode 2, High current	25 °C	-	120	-	uA
IDD_MED_M2	Mode 2, Medium current	25 °C	-	60	-	uA
IDD_LOW_M2	Mode 2, Low current	25 °C	-	15	-	uA
VOS_HI_M1	Mode 1, High current	With trim 25 °C, 0.2 V to VDDA-1.5 V	-	5	-	mV
VOS_MED_M1	Mode 1, Medium current	With trim 25 °C, 0.2 V to VDDA-1.5 V	-	5	-	mV
VOS_LOW_M1	Mode 1, Low current	With trim 25 °C, 0.2 V to VDDA-1.5 V	-	5	-	mV
VOS_HI_M2	Mode 2, High current	With trim 25 °C, 0.2 V to VDDA-1.5 V	-	5	-	mV
VOS_MED_M2	Mode 2, Medium current	With trim 25 °C, 0.2 V to VDDA-1.5 V	-	5	-	mV
VOS_LOW_M2	Mode 2, Low current	With trim 25 °C, 0.2 V to VDDA-1.5 V	-	5	-	mV
IOUT_HI_M1	Mode 1, High current	Output is 0.5 V to VDDA-0.5 V	-	10	-	mV
IOUT_MED_M1	Mode 1, Medium current	Output is 0.5 V to VDDA-0.5 V	-	10	-	mV
IOUT_LOW_M1	Mode 1, Low current	Output is 0.5 V to VDDA-0.5 V	-	4	-	mV
IOUT_HI_M2	Mode 2, High current	Output is 0.5 V to VDDA-0.5 V	-	1	-	mV
IOUT_MED_M2	Mode 2, Medium current	Output is 0.5 V to VDDA-0.5 V	-	1	-	mV
IOUT_LOW_M2	Mode 2, Low current	Output is 0.5 V to VDDA-0.5 V	-	0.5	-	mV

AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Load = 20 pF, 0.1 mA. VDDA = 2.7 V		–	–	–	–
GBW_HI	Power = high		6	–	–	MHz

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW_MED	Power = medium		4	–	–	MHz
GBW_LO	Power = low		2	–	–	MHz
GBW_LO	Power = low	For PSoC 4200 BLE family, PSoC 4100M/PSoC 4200M/ PSoC 4200L	–	1	–	MHz
Noise			–	–	–	–
VN1	Input referred, 1 Hz - 1GHz, power = high		–	94	–	µVrms
VN2	Input referred, 1 kHz, power = high		–	72	–	nV/rtHz
VN3	Input referred, 10kHz, power = high		–	28	–	nV/rtHz
VN4	Input referred, 100kHz, power = high		–	15	–	nV/rtHz
Slew_rate	Cload = 50 pF, Power = High, VDDA ≥ 2.7 V		6	–	–	V/µsec
T_op_wake	From disable to enable, no external RC dominating		–	300	–	µSec
T_op_wake	From disable to enable, no external RC dominating	PSoC 4100M/PSoC 4200M/ PSoC 4200L	–	25	–	µSec
Deep-Sleep Mode (For PSoC 4200 BLE family; only guaranteed for VDDA > 2.5 V)						
GBW_DS	Gain bandwidth product		–	50	–	kHz
Deep-Sleep Mode (For PSoC 4100M/PSoC 4200M/ PSoC 4200L; only guaranteed for VDDA ≥ 2.7 V) Mode 2 is lowest current range. Mode 1 has higher GBW.						
GBW_HI_M1	Mode 1, High current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	4	-	MHz
GBW_MED_M1	Mode 1, Medium current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	2	-	MHz
GBW_LOW_M1	Mode 1, Low current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.5	-	MHz
GBW_HI_M2	Mode 2, High current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.5	-	MHz
GBW_MED_M2	Mode 2, Medium current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.2	-	MHz
GBW_LOW_M2	Mode 2, Low current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.1	-	MHz

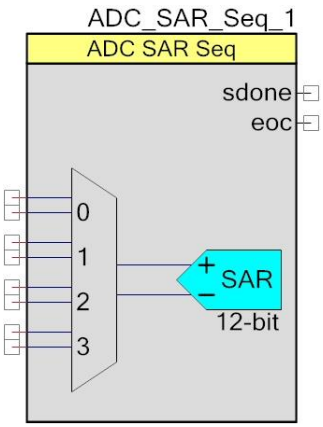
Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.20.a	Edited datasheet.	Final characterization data for PSoC 4000S, PSoC 4100S and PSoC Analog Coprocessor devices is not available at this time. Once the data is available, the component datasheet will be updated on the Cypress web site.
1.20	Added support for PSoC Analog Coprocessor devices.	New device support.
	Edited the datasheet.	Updated Component Parameters section with clarification of the deep sleep operation.
1.10.d	Edited the datasheet.	Minor corrections in parameters naming (AC Specifications section). Updated DC and AC Electrical Characteristics section with PSoC 4200L data.
1.10.c	Edited the datasheet.	Updated Offset voltage and Offset voltage drift parameter names into DC Specifications table. Updated DC and AC Electrical Characteristics section with PSoC 4100M/ PSoC 4200M data.
1.10.b	Edited the datasheet.	Added CMRR parameter values for PSoC 4200 BLE devices.
1.10.a	Edited the datasheet.	Added information that for correct operation in deep sleep mode, V_{DDA} must be larger than 2.5 V.
1.10	Added the Deep sleep operation parameter to control component availability in Deep Sleep mode.	Updates to support PSoC 4200 BLE devices.
	Updated API Memory usage and MISRA compliance sections.	
	Removed references to SaveConfig() and RestoreConfig() APIs because they are empty.	
	Changed output mode parameters from “1mA” and “10mA” to “Internal only” and “Output to pin” respectively.	
1.0.a	Updated datasheet.	Corrected specs to match device datasheet.
1.0	First release	

PSoC 4 Sequencing Successive Approximation ADC (ADC_SAR_Seq)

2.40



Features

- Selectable 8-, 10-, and 12-bit resolutions
- Sample rates of up to 1 Msps with 12-bit resolution
- Supports both Single Ended and Differential inputs
- Different ranges of inputs with multiple reference options
- Scan up to sixteen channels automatically, or just a single input
- Allows an “injection” channel to be added to the scan sequence with firmware control at runtime
- Hardware averaging support

General Description

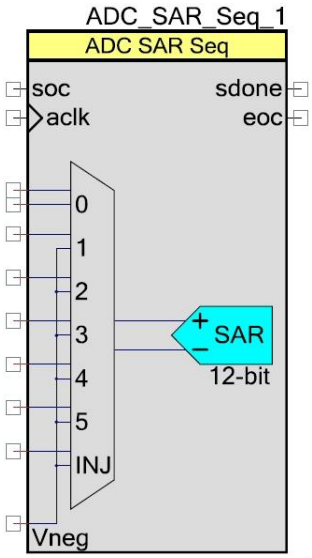
The Sequencing SAR ADC component gives you the ability to configure and use the different operational modes of the SAR ADC on PSoC 4. You have schematic- and firmware-level support for seamless use of the Sequencing SAR ADC in PSoC Creator designs and projects. You also have the ability to configure up to sixteen analog channels (depending on the device) that are automatically scanned with the results placed in individual result registers. An optional “Injection channel” may also be enabled by firmware to occasionally scan a signal that does not need to be scanned at the same rate as other channels.

When to Use a Sequencing SAR ADC

The Sequencing SAR ADC is the component used to access the ADC functionality in PSoC 4. The sequencing and muxing capabilities are integral parts of the SAR hardware. The component can be used in high sample rate systems where you need to sample multiple channels without CPU intervention until all channels are sampled. It can also be used in low sample rate designs or in designs that have just a single channel to sample.

Input/Output Connections

This section describes the various input and output connections for the Sequencing SAR ADC. An asterisk (*) in the list of I/Os states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.



+Input – Analog

This input is the positive analog signal input to the ADC SAR Seq. The conversion result is a function of the +Input signal minus the voltage reference. The voltage reference is either the –Input signal, Vneg, Vref, or Vss.

There are always the same number of analog signal input terminals as there are sequenced channels selected, including the injection channel.

Analog inputs are low impedance. This is solely driven by the need to settle the bus within the short sampling aperture of the Sequencing SAR ADC. Use the operational amplifier as a buffer for the high impedance signals.

–Input – Analog *

The number of negative input terminals varies depending on the number of channels and how many single ended channels are present. When a channel is selected as single ended, all the negative input signals are combined to form a single net internally.

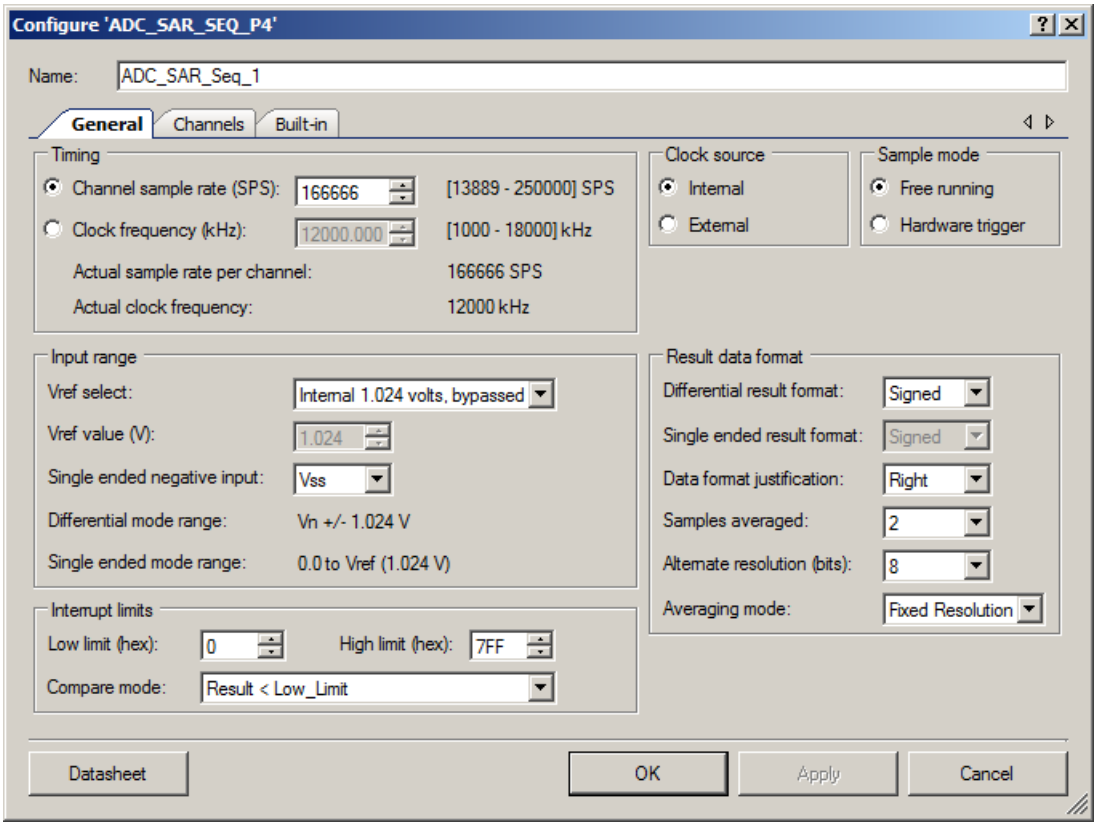
Vneg – Analog *

This is a common negative input reference. This terminal is present only if one or more analog channels are defined as a single ended input and **Single ended negative input** parameter is set to **External**.

Component Parameters

Drag a Sequencing SAR ADC onto your design and double click it to open the Configure dialog.

General Tab



The Sequencing SAR ADC has the following parameters. The option shown in bold is the default.

Sample rate

When selected, the clock rate is automatically calculated based on the number of channels, averaging, resolution, and acquisition time parameters to meet the entered sample rate.

Clock frequency

When selected, enter the desired clock rate. This parameter only applies when an internal clock source is selected. The clock frequency can be anywhere between 1 MHz and 18 MHz (14.508 MHz in CY8C41). If the clock does not fall within these limits, PSoC Creator generates an error during the build process. The actual clock rate may differ based on the available source clock speed and the resulting clock, based on an integer divide of the source clock. The read-only field below this field displays the effective sample rate based on the generated nominal clock frequency taken from the Design-Wide Resources (DWR) Clock Editor.

If the sample rate is fixed, the following parameters will alter the ADC clock frequency parameter:

- Sequenced Channels
- Averaging Enabled ("AVG" check box per channel, averaged samples)
- Acquisition Time
- Alternate resolution

At high sample rates, the ADC can generate large amounts of data. The CPU clock will need to be running fast enough to process the data and the interrupt service routine overhead will need to be minimized. For example, at a conversion rate of 700,000 samples per second and a CPU clock rate of 48 MHz, there are only 48 MHz/700,000 sps = 68 CPU clock cycles per sample. See the Interrupt Service Routine section for guidance on optimizing an ISR.

Actual sample rate

This field displays an actual recalculated sample rate based on the generated nominal clock frequency taken from the DWR Clock Editor. The actual sample rate may differ from “Sample rate” field. This is a read-only field.

Actual clock frequency

This field displays an actual calculated clock frequency rate based on the generated nominal clock frequency taken from the DWR Clock Editor. The actual clock frequency may differ from the Clock frequency field. This value is based on the available source clock speed and the resulting clock, based on an integer divide of the source clock. This is a read-only field.

Clock source

This parameter allows you to select a clock that is **internal** to the component or a clock source outside the component.

Sample mode

Sample mode determines if each scan must be triggered by the SOC terminal or continuously runs after the ADC is enabled and continues until the ADC_StopConvert() API is called.

Sample Mode	Description
Free Running	ADC SAR Seq runs continuously.
Hardware trigger	A rising-edge pulse on the SOC pin starts a single conversion. The ADC_StartConvert() function also starts a single conversion.

Vref select

The **Vref Select** parameter selects the reference voltage that is used for the SAR ADC.

Reference	Allowed Clock Frequency (MHz)	Description
VDDA/2 Internal 1.024 volts	1 ~ 1.6 MHz	Uses the internal reference without a bypass capacitor.
VDDA	1 ~ 9 MHz	Uses the internal VDDA reference without a bypass capacitor.
Internal 1.024 volts, bypassed VDDA/2, bypassed	1 ~ 18 MHz	Uses the internal reference with a bypass capacitor. You must place a bypass capacitor on pin P1[7] or the dedicated Vref pin (depending on the device). [1] [2]
External Vref	1 ~ 18 MHz	Uses an external reference on pin P1[7] or the dedicated Vref pin (depending on device). [2]
Internal Vref Internal Vref, bypassed	1 ~ 18 MHz	These options are supported by PSoC 4100S devices only.

The 1.024 V internal Vref startup time varies with different bypass capacitors. This table lists two common values for the bypass capacitor and its startup time specification.

Internal Vref Startup Time	Maximum Specification
Startup time for reference with external capacitor (1 µF)	2 ms
Startup time for reference with external capacitor (100 nF)	200 µs

Note If “non bypassed” mode is selected, the Acquisition times setting will change from 4 to minimum value (2) to try to achieve clock frequency ranges.

Note The ADC component parameter “Vref select” is set to “Internal 1.024 volts” by default. The PSoC 4100S device family has a voltage reference equal to 1.2 volts, and the “Internal 1.024 volts” setting is not supported. Therefore, for the PSoC 4100S device family, you must set this parameter to “Internal Vref” instead. If you don’t change the parameter value, PSoC Creator will

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[1] The use of an external bypass capacitor is recommended if the internal noise caused by digital switching exceeds an application's analog performance requirements. To use this option, connect an external capacitor with a value between 0.01 µF and 10 µF to port pin P1[7] or the dedicated Vref pin (depending on the device).

[2] Refer to the Pinouts section of the device datasheet for more information.

display the following build error: “Error in component: ADC. The selected type of voltage reference is not supported for the current device type.”

Vref value

This parameter displays the reference voltage value that is used for the SAR ADC reference. If the internal reference is selected with the **Vref select** parameter, this becomes a fixed value. If an internal reference such as VDDA or VDDA/2 is selected, the value is derived from the DWR System Editor Vdda parameter. In cases when Vref is unknown, such as using an external reference (external to the PSoC or component), the value may be entered by the user.

Single ended negative input

This parameter selects where the negative input to the SAR ADC is connected if any channels are configured for single ended operation. This choice affects the voltage range and effective resolution. The analog signals connected to the PSoC must be between V_{SSA} and V_{DDA} regardless of the input range settings.

Negative input	Description
Vss	Input range is 0.0 to Vref, effective resolution will be one bit less than selected in the customizer.
Vref	Input range is 0.0 to Vref*2. When using the internal reference (1.024 V), the usable input range is 0.0 to 2.048 V.
External	This mode is configured for differential inputs. Connect common single ended negative input to Vneg terminal. When using the internal reference (1.024 V), the input range is Vneg ± 1.024 V. For example, if Vneg is connected to 2.048 V, the usable input range is 2.048 ± 1.024 V or 1.024 to 3.072 V. For systems in which both single-ended and differential signals are scanned, connect Vneg to Vssa when scanning a single-ended input. You can use an external reference to provide a wider operating range. You can calculate the usable input range with the same equation, Vneg ± Vref.

Differential mode range

This is a noneditable text box that shows the range for the differential mode inputs. It is based on the **Vref select** and **Vref value** parameters. Examples of this text box are (Vn +/- 1.024 V, Vn +/- Vdda/2, Vn +/- Vdda, etc).

Single ended mode range

This is a noneditable text box that shows the range for the single ended mode inputs. It is based on the **Vref select**, **Vref value** and **Single ended negative input** parameters. Examples of this text box are (0.0 to Vref (1.024V), 0.0 to Vref (2.048 V), 0.0 to Vref (5 V), etc).

Differential result format

This parameter determines whether or not the result from a differential measurement is **Signed** or Unsigned. This is a global setting for all differential channels.

Single ended result format

This parameter determines whether or not the result from a single ended measurement is **Signed** or Unsigned. This is a global setting for all single ended channels.

The following table shows how these parameters affect conversion of the input voltage to the 12 bit digital sample value.

Single / Differential	Signed / Unsigned	Single ended negative input	-Input	+Input	Result Register
Single	Signed	Vss	Vss	Vref Vss -noise	0x07FF 0x0000 0xFFxx
Single	Signed	External	Vneg	Vneg+Vref Vneg Vneg-Vref	0x07FF 0x0000 0xF800
Single	Unsigned	Vref	Vref	2*Vref Vref Vss	0x0FFF 0x0800 0x0000
Single	Signed	Vref	Vref	2*Vref Vref Vss	0x07FF 0x0000 0xF800
Differential	Unsigned	N/A	Vx	Vx+Vref Vx Vx-Vref	0x0FFF 0x0800 0x0000
Differential	Signed	N/A	Vx	Vx+Vref Vx Vx-Vref	0x07FF 0x0000 0xF800

For single-ended conversions with the **Single ended negative input** parameter set to **Vss**, the conversion is effectively 11-bit, because voltages below Vss are illegal on any PSoC 4 pin. Because of this, the “Unsigned” option of the **Single ended result format** parameter is not available. Noise on the **+Input** pin with a level slightly below internal Vss, produces a result that is negative.

Note that single-ended conversions with an external common alternate ground are electrically equivalent to differential mode, where the pin of each differential pair is connected to the common alternate ground. Assuming that the measured signal value (**+Input**) cannot go below that common alternate ground, then these conversions are also effectively 11-bit.

Data Format Justification

This parameter sets whether or not the output data is Left or **Right** justified in a 16-bit word. For signed values, the result is signed extended when in right justification mode. This is a global setting for all channels. This table shows all the details.

Justification	Signed / Unsigned	Resolution	Result register bits ("0" – LSB, "-" – null)															
			15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Right	Unsigned	12	-	-	-	-	11	10	9	8	7	6	5	4	3	2	1	0
		10	-	-	-	-	-	-	9	8	7	6	5	4	3	2	1	0
		8	-	-	-	-	-	-	-	-	7	6	5	4	3	2	1	0
Right	Signed	12	11	11	11	11	11	10	9	8	7	6	5	4	3	2	1	0
		10	9	9	9	9	9	9	9	8	7	6	5	4	3	2	1	0
		8	7	7	7	7	7	7	7	7	7	6	5	4	3	2	1	0
Left	N/A	12	11	10	9	8	7	6	5	4	3	2	1	0	-	-	-	-
		10	9	8	7	6	5	4	3	2	1	0	-	-	-	-	-	-
		8	7	6	5	4	3	2	1	0	-	-	-	-	-	-	-	-

Samples averaged

This parameter sets the averaging rate for any channel with the averaging option enabled. This is a global setting for all channels with averaging enabled. Default value is 2.

Alternate Resolution

This parameter sets the alternate ADC resolution to either **8** or 10 bits. Conversions for each input are selectable as either 12 bits or this alternate resolution.

Averaging Mode

This parameter sets how the averaging mode operates. If the accumulate option is selected, each ADC result is added to the sum and allowed to grow until the sum attempts to outgrow a 16 bit value, at which point it is truncated. If the **Fixed Resolution** mode is selected, the LSb is truncated so that the value does not grow beyond the maximum value for the given resolution.

Compare Mode

The Sequencing SAR ADC supports range detection to allow for the automatic detection of sample values compared to two programmable thresholds without CPU involvement. A range detect is defined by two global thresholds and a condition.

This parameter sets the condition under which a limit condition will occur and trigger a maskable range detect interrupt.

Compare Mode	Description
Result < Low Limit	Below range
Low Limit <= Result < High Limit	Inside range
High Limit <= Result	Above range
(Result < Low Limit) or (High Limit <= Result)	Outside range

Low Limit

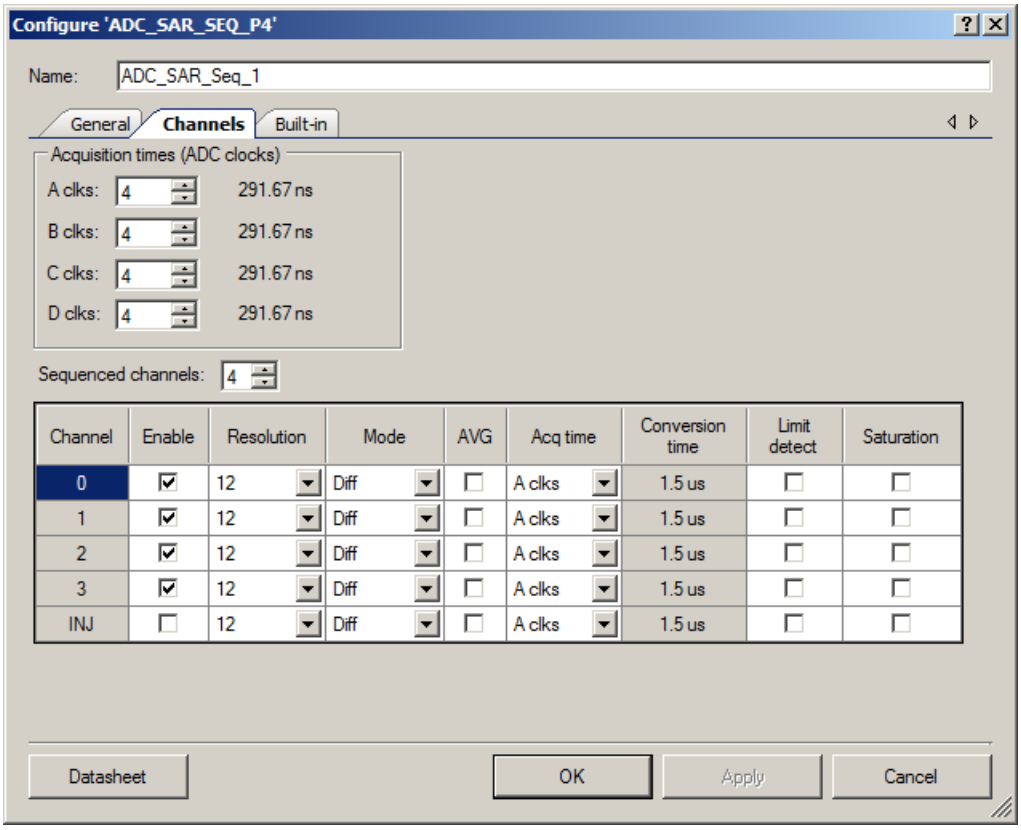
This parameter sets the low threshold for a limit compare. Default value is 0.

High Limit

This parameter sets the high threshold for a limit compare. Default value is 0x7FF.

A range detect is done after averaging, alignment, and sign extension (if applicable). In other words, the thresholds values must have the same data format as the final conversion result.

Channels Tab



Acquisition times

This parameter sets up to four different acquisition times to configure individual channels, entered in ADC clocks. The field to the right of each selection shows the actual delay given the current clock rate. The displayed time is equal to $(N_{clk} - 0.5)*(1/F_{clk})$, where N_{clk} is the number of acquisition ADC clocks, and F_{clk} is the clock frequency. If the clock is changed for any reason (refer to Clock frequency section for details), the time displayed changes as well. The default is **4** clock periods and adjustable from 2 to 1023 clock periods.

Sequenced channels

This parameter selects how many input signals are scanned, not counting the injection channel. The maximum number of channels is either 8 or 16 depending on the device. It depends also on mode (differential or single ended) and available resources outside of the SAR. The minimum number of channels is always 1.

A set of entries is available for each parameter. The actual number of entries depends on the **Sequenced channels** parameter. The injection channel **INJ** parameter is always present. If the injection channel is not enabled, it does not appear on the symbol. The symbol shows as many channels as are selected by the **Sequenced channel** parameter even if the channel is not enabled, except for the injection channel.

Enable

For channels 0 to 7(15), it enables the channel for scanning during runtime. For the injection channel, it determines whether or not the symbol displays the input.

Resolution

This parameter selects either **12** bits or an alternative (ALT) resolution of 8 or 10 bits depending on the **Alternate resolution** parameter.

Mode

This parameter selects the input mode to the ADC as either **differential** or single ended.

AVG

This option selects whether or not the channel is averaged. When selected, the SAR sequencer stays on the channel and takes N readings, then adds the results together. The number of samples taken is determined by the **Samples averaged** parameter. Averaging is available only for the maximum **Resolution** selected in a particular channel. Select ALT resolution for all channels to allow averaging on fewer than 12 bits resolution. Averaging is always right-aligned; therefore, the **Data Format Justification** parameter is ignored.

Acq Time

This parameter selects the acquisition time (sample and hold) during which the SAR input settles. The time is based on the SAR ADC clocks periods. These **Acquisition times** parameters are labeled **A**, B, C, and D.

Limit detect

This option allows you to enable an interrupt if any of the channels 0 through 7(15) or the injection channel trigger the limit criteria set by the **Low limit** or **High limit** and the **Compare mode** parameter.

Saturation

This option allows you to enable an interrupt from any channel where the result is saturated from either a conversion result of 0x0000 or the highest value for the given resolution.

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. This table lists and describes the interface to each function. The following sections cover each function in more detail.

By default, PSoC Creator assigns the instance name "ADC_SAR_Seq_1" to the first instance of a component in a given design. You can rename it to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "ADC".

Note Do not use the ADC_Stop() API to halt conversions. Instead use the ADC_StopConvert() API. If you use the ADC_Stop() API to halt conversions then later use the ADC_Start() and ADC_StartConvert() APIs to resume conversions, the first channel of the scan may be corrupt. The StopConvert() API will enable the Sequencing SAR ADC to complete the current scan of channels. After the channel scan is complete, the Sequencing SAR ADC will stop all conversions, which can be detected by the use of an ISR or the ADC_IsEndConversion() flag.

Functions

Function	Description
ADC_Start()	Performs all required initialization for this component and enables the power. The power will be set to the appropriate power based on the clock frequency.
ADC_Stop()	This function stops ADC conversions and puts the ADC into its lowest power mode.
ADC_StartConvert()	For free running mode, this API starts the conversion process and it runs continuously. In a triggered mode, this routine triggers every conversion.

Function	Description
ADC_StopConvert()	Forces the ADC to stop conversions. If a conversion is currently executing, that conversion will complete, but no further conversions will occur.
ADC_IRQ_Enable()	Enables interrupts to occur at the end of a conversion. Global interrupts must also be enabled for the ADC interrupts to occur.
ADC_IRQ_Disable()	Disables interrupts at the end of a conversion.
ADC_IsEndConversion()	Immediately returns the status of the conversion or does not return (blocking) until the conversion completes, depending on the retMode parameter.
ADC_GetResult16()	Gets the data available in the SAR result register.
ADC_SetChanMask()	Sets the channel enable mask. Sets which channels that will be scanned.
ADC_EnableInjection()	Enables the injection channel for the next scan only.
ADC_SetLowLimit()	This parameter sets the low limit for a limit compare.
ADC_SetHighLimit()	This parameter sets the high limit for a limit compare.
ADC_SetLimitMask()	Sets which channels may cause a limit condition interrupt.
ADC_SetSatMask()	Sets which channels may cause a saturation event interrupt.
ADC_SetOffset()	Sets the offset of the ADC channel.
ADC_SetGain()	Sets the gain in counts per 10 volt for the ADC channel.
ADC_CountsTo_Volts()	Converts the ADC output to volts as a floating point number.
ADC_CountsTo_mVolts()	Converts the ADC output to millivolts.
ADC_CountsTo_uVolts()	Converts the ADC output to microvolts.
ADC_Sleep()	Stops the ADC operation and saves the configuration registers and component enable state.
ADC_Wakeup()	Restores the component enable state and configuration registers.
ADC_SaveConfig()	Save the current configuration of ADC non-retention registers.
ADC_RestoreConfig()	Restores the configuration of ADC non-retention registers.

void ADC_ Start(void)

Description: Performs all required initialization for this component and enables the power. The power will be set to the appropriate power based on the clock frequency.

Parameters: None

Return Value: None

Side Effects: None

void ADC_Stop(void)

Description: This function stops ADC conversions and puts the ADC into its lowest power mode.

Parameters: None

Return Value: None

Side Effects: Don't use the Stop() API to halt conversions. Instead use the StopConvert() API. If you use the Stop() API to halt conversions then later use the ADC_Start() and ADC_StartConvert() APIs to resume conversions, the first channel of the scan may be corrupt. The StopConvert() API will enable the Sequencing SAR ADC to complete the current scan of channels. After the channel scan is complete, the Sequencing SAR ADC will stop all conversions, which can be detected by the use of an ISR or the ADC_IsEndConversion() flag.

void ADC_StartConvert(void)

Description: For free running mode, this API starts the conversion process and it runs continuously.

In **Hardware trigger** mode, the function also acts as a software version of the SOC and every conversion requires a call of this function.

Parameters: None

Return Value: None

Side Effects: None

void ADC_StopConvert(void)

Description: Forces the ADC to stop conversions. If a conversion is currently executing, that conversion will complete, but no further conversions will occur.

Parameters: None

Return Value: None

Side Effects: None

void ADC_IRQ_Enable(void)

Description: Enables interrupts to occur at the end of a conversion. Global interrupts must also be enabled for the ADC interrupts to occur.

Parameters: None

Return Value: None

Side Effects: None

void ADC_IRQ_Disable(void)

Description: Disables end of conversion interrupts.

Parameters: None

Return Value: None

Side Effects: None

uint32 ADC_IsEndConversion(uint32 retMode)

Description: Immediately returns the status of the conversion or does not return (blocking) until the conversion completes, depending on the retMode parameter.

Parameters: retMode: Check conversion return mode. See the following table for options.

Options	Description
ADC_RETURN_STATUS	Immediately returns the conversion status for sequential channels. If the value returned is zero, the conversion is not complete, and this function should be retried until a nonzero result is returned.
ADC_WAIT_FOR_RESULT	Does not return a result until the ADC conversion of all sequential channels is complete.
ADC_RETURN_STATUS_INJ	Immediately returns the conversion status for the injection channel. If the value returned is zero, the conversion is not complete, and this function should be retried until a nonzero result is returned.
ADC_WAIT_FOR_RESULT_INJ	Does not return a result until the ADC completes injection channel conversion.

Return Value: uint8: If a nonzero value is returned, the last conversion is complete. If the returned value is zero, the ADC is still calculating the last result.

Side Effects: This function reads the end of conversion status, and clears it afterward.

int16 ADC_GetResult16(uint32 chan)

Description: Gets the data available in the channel result data register.

Parameters: chan: The ADC channel to read the result from. The first channel is 0 and the injection channel if enabled is the number of valid channels.

Return Value: Returns converted data as a signed 16-bit integer

Side Effects: None.

void ADC_SetChanMask(uint32 mask)

Description: Sets the channel enable mask.

Parameters: mask: Sets which channels that will be scanned. Setting bits for channels that do not exist will have no effect. For example, if only 6 channels were enabled, setting a mask of 0x0103 would only enable the last two channels (0 and 1). This API will not enable the injection channel.

Return Value: None

Side Effects: None

void ADC_EnableInjection(void)

Description: Enables the injection channel for the next scan only.

Parameters: None

Return Value: None

Side Effects: None

void ADC_SetLowLimit(uint32 lowLimit)

Description: Sets the low limit parameter for a limit condition.

Parameters: lowLimit: The low limit for a limit condition.

Return Value: None

Side Effects: None

void ADC_SetHighLimit(uint32 highLimit)

Description: Sets the high limit parameter for a limit condition.

Parameters: highLimit: The high limit for a limit condition.

Return Value: None

Side Effects: None

void ADC_SetLimitMask(uint32 mask)

Description: Sets the channel limit condition mask.

Parameters: mask: Sets which channels that may cause a limit condition interrupt. Setting bits for channels that do not exist will have no effect. For example, if only 6 channels were enabled, setting a mask of 0x0103 would only enable the last two channels (0 and 1).

Return Value: None

Side Effects: None

void ADC_SetSatMask(uint32 mask)

Description: Sets the channel saturation event mask.

Parameters: mask: Sets which channels that may cause a saturation event interrupt. Setting bits for channels that do not exist will have no effect. For example, if only 8 channels were enabled, setting a mask of 0x01C0 would only enable two channels (6 and 7).

Return Value: None

Side Effects: None

void ADC_SetOffset(uint32 chan, int16 offset)

Description: Sets the ADC offset which is used by the functions ADC_CountsTo_uVolts, ADC_CountsTo_mVolts and ADC_CountsTo_Volts to subtract the offset from the given reading before calculating the voltage conversion.

Parameters: chan: ADC channel number.

offset: This value is a measured value when the inputs are shorted or connected to the same input voltage.

Return Value: None

Side Effects: None.

void ADC_SetGain(uint32 chan, int32 adcGain)

Description: Sets the ADC gain in counts per 10 volt for the voltage conversion functions below. This value is set by default by the reference and input range settings. It should only be used to further calibrate the ADC with a known input or if an external reference is used. Affects the ADC_CountsTo_uVolts, ADC_CountsTo_mVolts and ADC_CountsTo_Volts functions by supplying the correct conversion between ADC counts and voltage.

Parameters: chan: ADC channel number.

adcGain: ADC gain in counts per 10 volt.

Return Value: None

Side Effects: None.

float32 ADC_CountsTo_Volts(uint32 chan, int16 adcCounts)

Description: Converts the ADC output to Volts as a floating point number. For example, if the ADC measured 0.534 volts, the return value would be 0.534. The calculation of voltage depends on the value of the voltage reference. When the Vref is based on Vdda, the value used for Vdda is set for the project in the System tab of the DWR.

Parameters: chan: ADC channel number.

adcCounts: Result from the ADC conversion

Return Value: Result in Volts

Side Effects: None

int16 ADC_CountsTo_mVolts(uint32 chan, int16 adcCounts)

Description: Converts the ADC output to millivolts as a 16-bit integer. For example, if the ADC measured 0.534 volts, the return value would be 534. The calculation of voltage depends on the value of the voltage reference. When the Vref is based on Vdda, the value used for Vdda is set for the project in the System tab of the DWR.

Parameters: chan: ADC channel number.

adcCounts: Result from the ADC conversion.

Return Value: Result in mV.

Side Effects: None

int32 ADC_CountsTo_uVolts(uint32 chan, int16 adcCounts)

Description: Converts the ADC output to microvolts as a 32-bit integer. For example, if the ADC measured 0.534 volts, the return value would be 534000. The calculation of voltage depends on the value of the voltage reference. When the Vref is based on Vdda, the value used for Vdda is set for the project in the System tab of the DWR.

Parameters: chan: ADC channel number.

adcCounts: Result from the ADC conversion

Return Value: Result in µV

Side Effects: None

void ADC_Sleep(void)

Description: This is the preferred routine to prepare the component for sleep. The ADC_Sleep() routine saves the current component state. Then it calls the ADC_Stop() function and calls ADC_SaveConfig() to save the hardware configuration.

Call the ADC_Sleep() function before calling the CySysPmDeepSleep() or the CySysPmHibernate() function. See the PSoC Creator *System Reference Guide* for more information about power-management functions.

Parameters: None

Return Value: None

Side Effects: If this function is called twice in the enable state of the component, the disabled state of the component will be stored. So ADC_Enable() and ADC_StartConvert() must be called after ADC_Wakeup() in this case.

void ADC_Wakeup(void)

Description: This is the preferred routine to restore the component to the state when ADC_Sleep() was called. The ADC_Wakeup() function calls the ADC_RestoreConfig() function to restore the configuration. If the component was enabled before the ADC_Sleep() function was called, the ADC_Wakeup() function also re-enables the component.

Parameters: None

Return Value: None

Side Effects: Calling this function without previously calling ADC_Sleep() may lead to unpredictable results.

void ADC_SaveConfig(void)

Description: This function saves the component configuration and nonretention registers. It also saves the current component parameter values, as defined in the Configure dialog or as modified by the appropriate APIs. This function is called by the ADC_Sleep() function.

Parameters: None

Return Value: None

Side Effects: All ADC configuration registers are retained. This function does not have an implementation and is meant for future use. It is provided here so that the APIs are consistent across components.

void ADC_RestoreConfig(void)

Description: This function restores the component configuration and nonretention registers. It also restores the component parameter values to what they were before calling the ADC_Sleep() function.

Parameters: None

Return Value: None

Side Effects: Calling this function without previously calling ADC_SaveConfig() or ADC_Sleep() may produce unexpected behavior. This function does not have an implementation and is meant for future use. It is provided here so that the APIs are consistent across components.

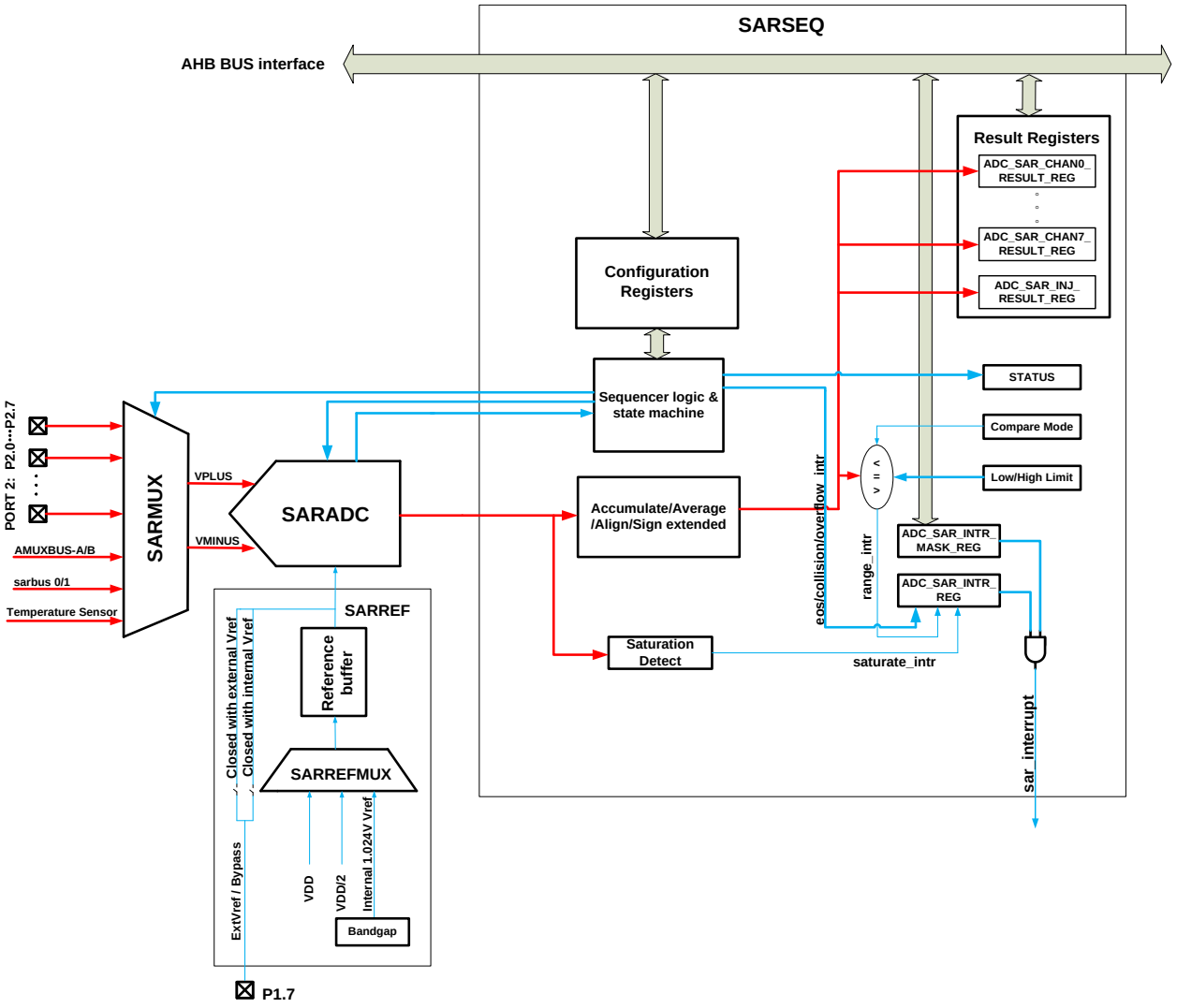
Global Variables

Function	Description
ADC_initVar	The initVar variable is used to indicate initial configuration of this component. The variable is initialized to zero and set to 1 the first time ADC_Start() is called. This allows for component initialization without reinitialization in all subsequent calls to the ADC_Start() routine. If reinitialization of the component is required, then the ADC_Init() function can be called before the ADC_Start() or ADC_Enable() functions.
ADC_offset[]	This array calibrates the offset for each channel. It is set to 0 the first time ADC_Start() is called and can be modified using ADC_SetOffset(). The array affects the ADC_CountsTo_Volts(), ADC_CountsTo_mVolts(), and ADC_CountsTo_uVolts() functions by subtracting the given offset.
ADC_countsPer10Volt[]	This array is used to calibrate the gain for each channel. It is calculated the first time ADC_Start() is called. The value depends on channel resolution and voltage reference. It can be changed using ADC_SetGain(). This array affects the ADC_CountsTo_Volts(), ADC_CountsTo_mVolts(), and ADC_CountsTo_uVolts() functions by supplying the correct conversion between ADC counts and the applied input voltage.

Usable Constants

Function	Description
ADC_SEQUENCED_CHANNELS_NUM	This constant represents the amount of input sequencing channels available for scanning.
ADC_TOTAL_CHANNELS_NUM	This constant represents the total number of input channels including the injection channel.

Block Diagram



DMA Support

The DMA component can be used to transfer data from the component registers to RAM or another component.

Name of DMA Source	Width	Direction	DMA Req Signal	DMA Trigger Type	Description
(ADC_SAR_CHAN_RESULT_PTR + (***X*** << 2u)) * or ADC_SAR_CHAN***X***_RESULT_PTR *	32	Source	eoc	Pulse	Channel result data register. This 32-bit register contains 16-bit ADC results.

* where ***X*** – is a channel number. The first channel is 0.

Note The component has a DMA bus interface that supports 32-bit (word) transfers only. If the data element size used for DMA transfer is less than a word, set the DMA descriptor with the correct width; for example, data element size is halfword (2 bytes). The component register is used as Source; make sure the DMA descriptor is configured as "Word to Halfword."

Registers

Channel result data registers

This 32-bit register contains 16-bit ADC results from channel 0 along with 3 status bits that describe the results correctness.

ADC_SAR_CHAN_RESULT_REG

Bits	Name	Description
15:0	Data	SAR conversion result of the first channel. The data is copied here from the work field after all enabled channels in this scan have been sampled.
29	ADC_SATURATE_INTR_MIR	Mirror bit of corresponding bit in ADC_SAR_SATURATE_INTR_REG register
30	ADC_RANGE_INTR_MIR	Mirror bit of corresponding bit in ADC_SAR_RANGE_INTR_REG register
31	ADC_CHAN_RESULT_VALID_MIR	Mirror bit of corresponding bit in ADC_SAR_CHAN_RESULT_VALID_REG register

Result registers for the remaining channels are located sequentially in the memory. Direct defines for each channel are provided: ADC_SAR_CHAN*X*_RESULT_REG, were *X* is the channel number from 0 to 7(15).

ADC_SAR_INJ_RESULT_REG

Bits	Name	Description
15:0	Data	SAR conversion result of the injection channel.
28	ADC_INJ_COLLISION_INTR_MIR	Mirror bit of corresponding bit in ADC_SAR_INTR_REG register
29	ADC_INJ_SATURATE_INTR_MIR	Mirror bit of corresponding bit in ADC_SAR_INTR_REG register
30	ADC_INJ_RANGE_INTR_MIR	Mirror bit of corresponding bit in ADC_SAR_INTR_REG register
31	ADC_INJ_EOC_INTR_MIR	Mirror bit of corresponding bit in ADC_SAR_INTR_REG register

MCP73831/2

Miniature Single-Cell, Fully Integrated Li-Ion, Li-Polymer Charge Management Controllers

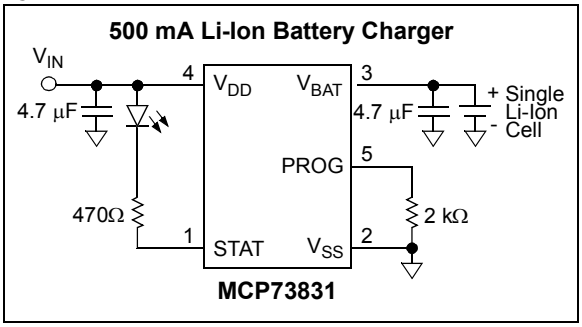
Features:

- Linear Charge Management Controller:
  - Integrated Pass Transistor
  - Integrated Current Sense
  - Reverse Discharge Protection
- High Accuracy Preset Voltage Regulation: ± 0.75%
- Four Voltage Regulation Options:
  - 4.20V, 4.35V, 4.40V, 4.50V
- Programmable Charge Current: 15 mA to 500 mA
- Selectable Preconditioning:
  - 10%, 20%, 40%, or Disable
- Selectable End-of-Charge Control:
  - 5%, 7.5%, 10%, or 20%
- Charge Status Output
  - Tri-State Output - MCP73831
  - Open-Drain Output - MCP73832
- Automatic Power-Down
- Thermal Regulation
- Temperature Range: -40°C to +85°C
- Packaging:
  - 8-Lead, 2 mm x 3 mm DFN
  - 5-Lead, SOT-23

Applications:

- Lithium-Ion/Lithium-Polymer Battery Chargers
- Personal Data Assistants
- Cellular Telephones
- Digital Cameras
- MP3 Players
- Bluetooth Headsets
- USB Chargers

Typical Application



Description:

The MCP73831/2 devices are highly advanced linear charge management controllers for use in space-limited, cost-sensitive applications. The MCP73831/2 are available in an 8-Lead, 2 mm x 3 mm DFN package or a 5-Lead, SOT-23 package. Along with their small physical size, the low number of external components required make the MCP73831/2 ideally suited for portable applications. For applications charging from a USB port, the MCP73831/2 adhere to all the specifications governing the USB power bus.

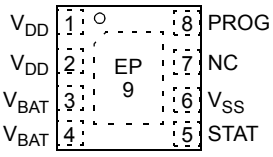
The MCP73831/2 employ a constant-current/constant-voltage charge algorithm with selectable preconditioning and charge termination. The constant voltage regulation is fixed with four available options: 4.20V, 4.35V, 4.40V or 4.50V, to accommodate new, emerging battery charging requirements. The constant current value is set with one external resistor. The MCP73831/2 devices limit the charge current based on die temperature during high power or high ambient conditions. This thermal regulation optimizes the charge cycle time while maintaining device reliability.

Several options are available for the preconditioning threshold, preconditioning current value, charge termination value and automatic recharge threshold. The preconditioning value and charge termination value are set as a ratio or percentage of the programmed constant current value. Preconditioning can be disabled. Refer to **Section 1.0 "Electrical Characteristics"** for available options and the **Product Identification System** for standard options.

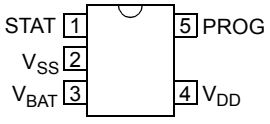
The MCP73831/2 devices are fully specified over the ambient temperature range of -40°C to +85°C.

Package Types

MCP73831/2
2×3 DFN*

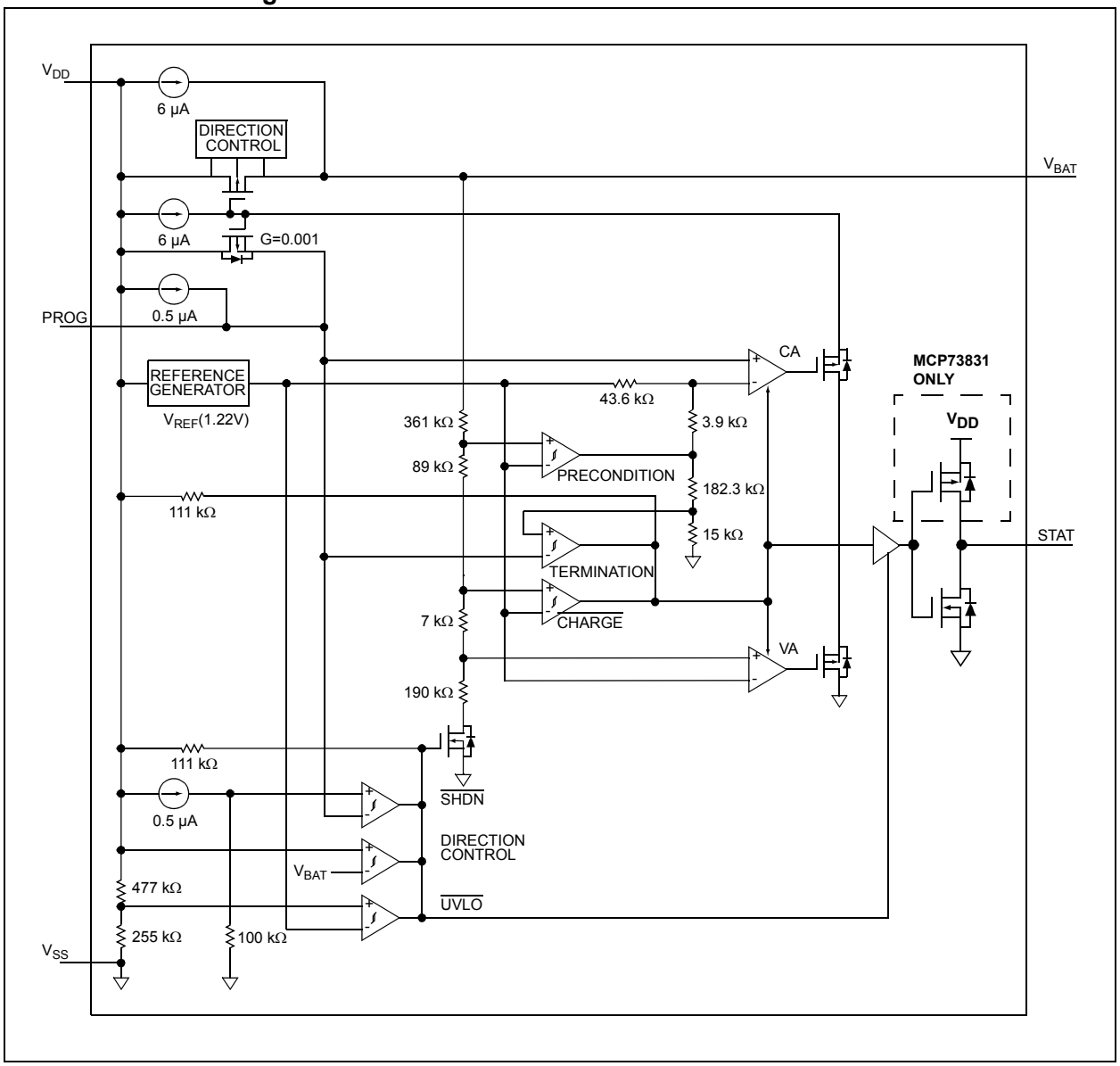


MCP73831/2
SOT-23-5



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}.....7.0V
All Inputs and Outputs w.r.t. V_{SS} ..... -0.3 to (V_{DD}+0.3)V
Maximum Junction Temperature, T_J .....Internally Limited
Storage temperature .....-65°C to +150°C
ESD protection on all pins:
Human Body Model (1.5 kΩ in Series with 100 pF).....≥ 4 kV
Machine Model (200 pF, No Series Resistance).....400V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{DD}= [V_{REG}(typical) + 0.3V] to 6V, T_A = -40°C to +85°C. Typical values are at +25°C, V_{DD} = [V_{REG} (typical) + 1.0V]

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Input						
Supply Voltage	V_{DD}	3.75	—	6	V	
Supply Current	I_{SS}	—	510	1500	µA	Charging
		—	53	200	µA	Charge Complete, No Battery
		—	25	50	µA	PROG Floating
		—	1	5	µA	$V_{DD} \leq (V_{BAT}$ - 50 mV)
		—	0.1	2	µA	$V_{DD} < V_{STOP}$
UVLO Start Threshold	V_{START}	3.3	3.45	3.6	V	V_{DD} Low-to-High
UVLO Stop Threshold	V_{STOP}	3.2	3.38	3.5	V	V_{DD} High-to-Low
UVLO Hysteresis	V_{HYS}	—	70	—	mV	
Voltage Regulation (Constant-Voltage Mode)						
Regulated Output Voltage	V_{REG}	4.168	4.20	4.232	V	MCP7383X-2
		4.317	4.35	4.383	V	MCP7383X-3
		4.367	4.40	4.433	V	MCP7383X-4
		4.466	4.50	4.534	V	MCP7383X-5
						V_{DD} = [V_{REG}(typical)+1V] I_{OUT} = 10 mA T_A = -5°C to +55°C
Line Regulation	$\lvert(\Delta V_{BAT}/V_{BAT})/\Delta V_{DD}\rvert$	—	0.09	0.30	%/V	V_{DD} = [V_{REG}(typical)+1V] to 6V, I_{OUT} = 10 mA
Load Regulation	$\lvert\Delta V_{BAT}/V_{BAT}\rvert$	—	0.05	0.30	%	I_{OUT} = 10 mA to 50 mA V_{DD} = [V_{REG}(typical)+1V]
Supply Ripple Attenuation	PSRR	—	52	—-	dB	I_{OUT}=10 mA, 10Hz to 1 kHz
		—	47	—	dB	I_{OUT}=10 mA, 10Hz to 10 kHz
		—	22	—	dB	I_{OUT}=10 mA, 10Hz to 1 MHz
Current Regulation (Fast Charge Constant-Current Mode)						
Fast Charge Current Regulation	I_{REG}	90	100	110	mA	PROG = 10 kΩ
		450	505	550	mA	PROG = 2.0 kΩ, **Note 1**
		12.5	14.5	16.5	mA	PROG = 67 kΩ
						T_A = -5°C to +55°C

Note 1: Not production tested. Ensured by design.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{DD}= [V_{REG}(typical) + 0.3V] to 6V, T_A = -40°C to +85°C. Typical values are at +25°C, V_{DD} = [V_{REG} (typical) + 1.0V]

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Preconditioning Current Regulation (Trickle Charge Constant-Current Mode)						
Precondition Current Ratio	I_{PREG} / I_{REG}	7.5	10	12.5	%	PROG = 2.0 kΩ to 10 kΩ
		15	20	25	%	PROG = 2.0 kΩ to 10 kΩ
		30	40	50	%	PROG = 2.0 kΩ to 10 kΩ
		—	100	—	%	No Preconditioning
						T_A = -5°C to +55°C
Precondition Voltage Threshold Ratio	V_{PTH} / V_{REG}	64	66.5	69	%	V_{BAT} Low-to-High
		69	71.5	74	%	V_{BAT} Low-to-High
Precondition Hysteresis	V_{PHYS}	—	110	—	mV	V_{BAT} High-to-Low
Charge Termination						
Charge Termination Current Ratio	I_{TERM} / I_{REG}	3.75	5	6.25	%	PROG = 2.0 kΩ to 10 kΩ
		5.6	7.5	9.4	%	PROG = 2.0 kΩ to 10 kΩ
		8.5	10	11.5	%	PROG = 2.0 kΩ to 10 kΩ
		15	20	25	%	PROG = 2.0 kΩ to 10 kΩ
						T_A = -5°C to +55°C
Automatic Recharge						
Recharge Voltage Threshold Ratio	V_{RTH} / V_{REG}	91.5	94.0	96.5	%	V_{BAT} High-to-Low
		94	96.5	99	%	V_{BAT} High-to-Low
Pass Transistor ON-Resistance						
ON-Resistance	R_{DSON}	—	350	—	mΩ	V_{DD} = 3.75V, T_J = 105°C
Battery Detection						
Battery Detection Current	I_{BAT_DET}	—	6	—	µA	V_{BAT} Source Current
No-Battery-Present Threshold	V_{NO_BAT}	—	V_{REG} + 100 mV	—	V	V_{BAT} Voltage ≥ V_{NO_BAT} for No Battery condition
No-Battery-Present Impedance	Z_{NO_BAT}	2	—	—	MΩ	V_{BAT} Impedance ≥ Z_{NO_BAT} for No Battery condition, **Note 1**
Battery Discharge Current						
Output Reverse Leakage Current	$I_{DISCHARGE}$	—	0.15	2	µA	PROG Floating
		—	0.25	2	µA	V_{DD} Floating
		—	0.15	2	µA	V_{DD} < V_{STOP}
		—	-5.5	-15	µA	Charge Complete
Status Indicator – STAT						
Sink Current	I_{SINK}	—	—	25	mA	
Low Output Voltage	V_{OL}	—	0.4	1	V	I_{SINK} = 4 mA
Source Current	I_{SOURCE}	—	—	35	mA	
High Output Voltage	V_{OH}	—	V_{DD}-0.4	V_{DD} - 1	V	I_{SOURCE} = 4 mA (MCP73831)
Input Leakage Current	I_{LK}	—	0.03	1	µA	High-Impedance
PROG Input						
Charge Impedance Range	R_{PROG}	2	—	67	kΩ	
Minimum Shutdown Impedance	R_{PROG}	70	—	200	kΩ	
Automatic Power Down						
Automatic Power Down Entry Threshold	$V_{PDENTER}$	V_{DD}<(V_{BAT} +20 mV)	V_{DD}<(V_{BAT} +50 mV)	—		3.5V ≤ V_{BAT} ≤ V_{REG} V_{DD} Falling

Note 1: Not production tested. Ensured by design.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{DD}= [V_{REG}(typical) + 0.3V] to 6V, T_A = -40°C to +85°C. Typical values are at +25°C, V_{DD} = [V_{REG} (typical) + 1.0V]

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Automatic Power Down Exit Threshold	V_{PDEXIT}	—	V_{DD}<(V_{BAT} +150 mV)	V_{DD}<(V_{BAT} +200 mV)		3.5V ≤ V_{BAT} ≤ V_{REG} V_{DD} Rising
Thermal Shutdown						
Die Temperature	T_{SD}	—	150	—	°C	
Die Temperature Hysteresis	T_{SDHYS}	—	10	—	°C	

Note 1: Not production tested. Ensured by design.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{DD} = [V_{REG} (typical) + 0.3V] to 12V, T_A = -40°C to +85°C. Typical values are at +25°C, V_{DD} = [V_{REG} (typical) + 1.0V]

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
UVLO Start Delay	t_{START}	—	—	5	ms	V_{DD} Low-to-High
Constant-Current Regulation						
Transition Time Out of Preconditioning	t_{DELAY}	—	—	1	ms	V_{BAT} < V_{PTH} to V_{BAT} > V_{PTH}
Current Rise Time Out of Preconditioning	t_{RISE}	—	—	1	ms	I_{OUT} Rising to 90% of I_{REG}
Termination Comparator Filter	t_{TERM}	0.4	1.3	3.2	ms	Average I_{OUT} Falling
$\overline{\text{Charge}}$ Comparator Filter	t_{CHARGE}	0.4	1.3	3.2	ms	Average V_{BAT}
Status Indicator						
Status Output turn-off	t_{OFF}	—	—	200	µs	I_{SINK} = 1 mA to 0 mA
Status Output turn-on	t_{ON}	—	—	200	µs	I_{SINK} = 0 mA to 1 mA

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{DD} = [V_{REG} (typical) + 0.3V] to 12V. Typical values are at +25°C, V_{DD} = [V_{REG} (typical) + 1.0V]

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
5-Lead, SOT-23	θ_{JA}	—	230	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection **(Note 2)**
8-Lead, 2 mm x 3 mm, DFN	θ_{JA}	—	76	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection **(Note 1)**

Note 1: This represents the minimum copper condition on the PCB (Printed Circuit Board).

2: With large copper area on the PCB, the SOT-23-5 thermal resistance (θ_{JA}) can reach a typical value of 130°C/W or better.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = [V_{REG}(typical) + 1V], I_{OUT} = 10 mA and T_A= +25°C, Constant-Voltage mode.

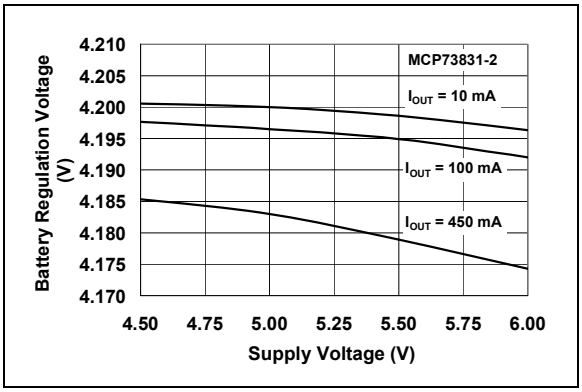


FIGURE 2-1: *Battery Regulation Voltage (V_{BAT}) vs. Supply Voltage (V_{DD}).*

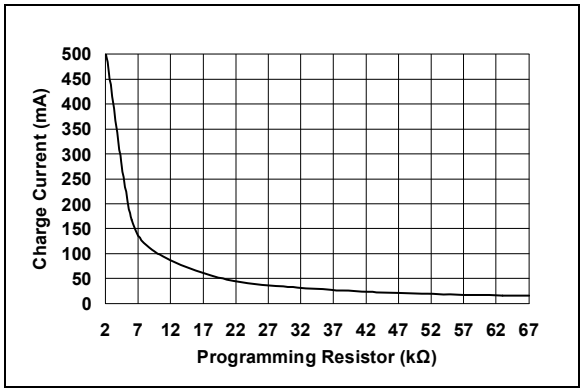


FIGURE 2-4: *Charge Current (I_{OUT}) vs. Programming Resistor (R_{PROG}).*

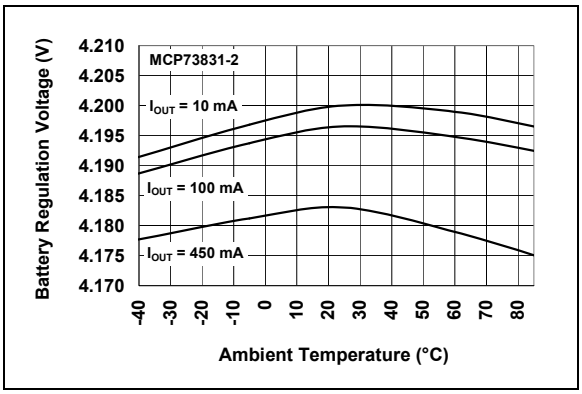


FIGURE 2-2: *Battery Regulation Voltage (V_{BAT}) vs. Ambient Temperature (T_A).*

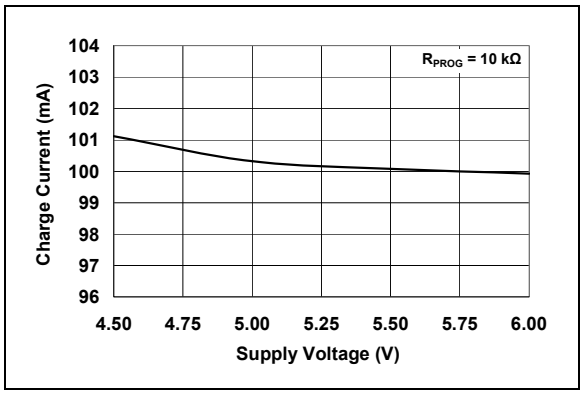


FIGURE 2-5: *Charge Current (I_{OUT}) vs. Supply Voltage (V_{DD}).*

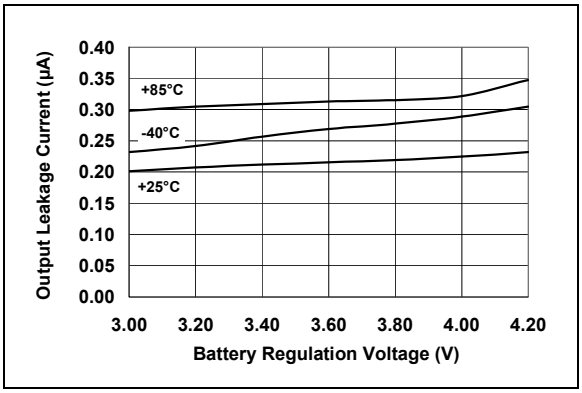


FIGURE 2-3: *Output Leakage Current ($I_{DISCHARGE}$) vs. Battery Regulation Voltage (V_{BAT}).*

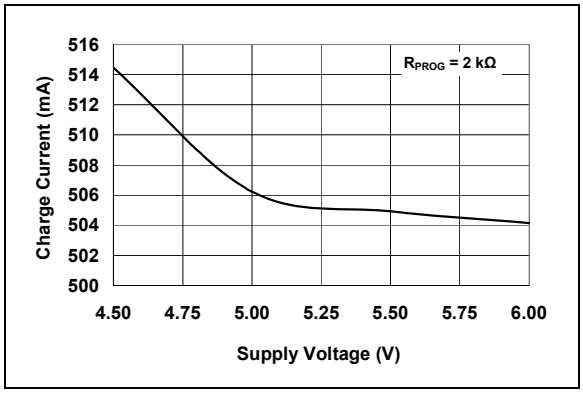


FIGURE 2-6: *Charge Current (I_{OUT}) vs. Supply Voltage (V_{DD}).*

TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, V_{DD} = [V_{REG}(typical) + 1V], I_{OUT} = 10 mA and T_A= +25°C, Constant-Voltage mode.

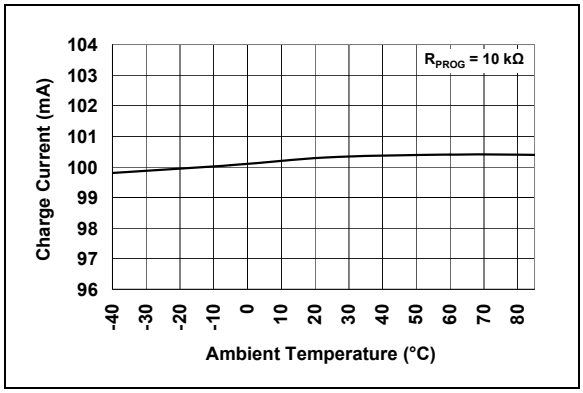


FIGURE 2-7: *Charge Current (I_{OUT}) vs. Ambient Temperature (T_A).*

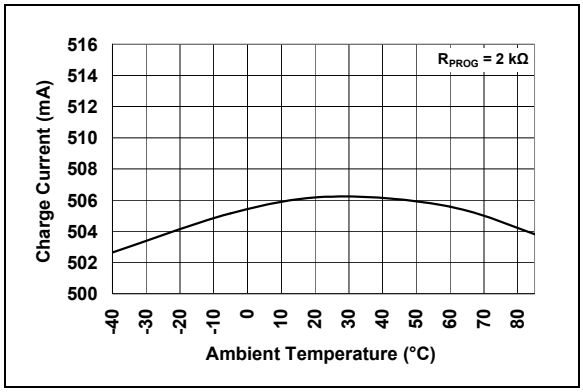


FIGURE 2-8: *Charge Current (I_{OUT}) vs. Ambient Temperature (T_A).*

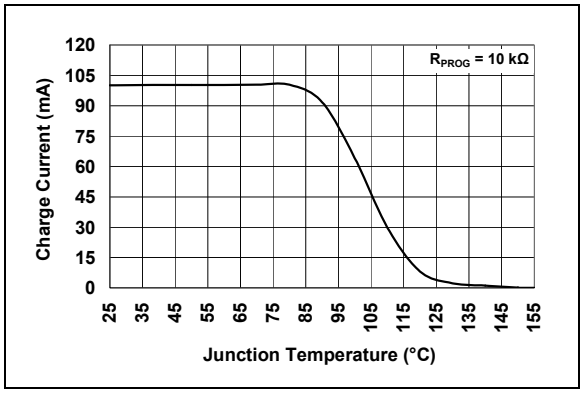


FIGURE 2-9: *Charge Current (I_{OUT}) vs. Junction Temperature (T_J).*

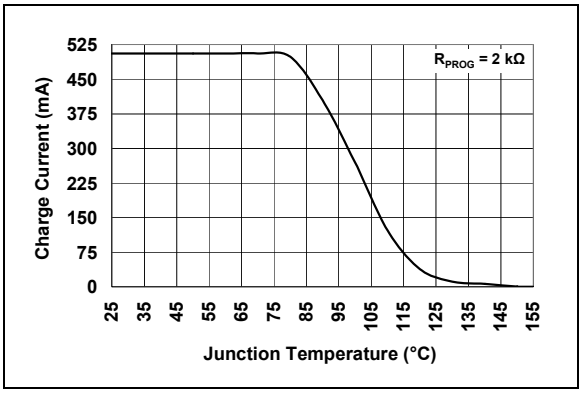


FIGURE 2-10: *Charge Current (I_{OUT}) vs. Junction Temperature (T_J).*

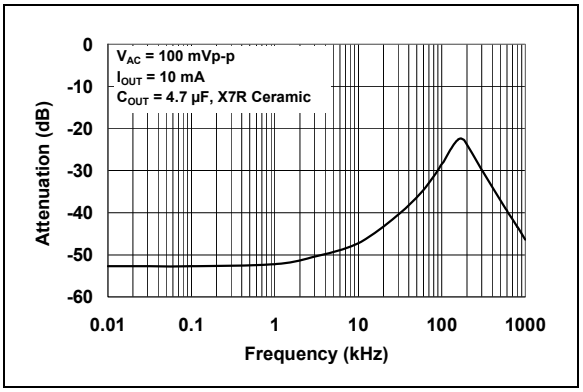


FIGURE 2-11: *Power Supply Ripple Rejection (PSRR).*

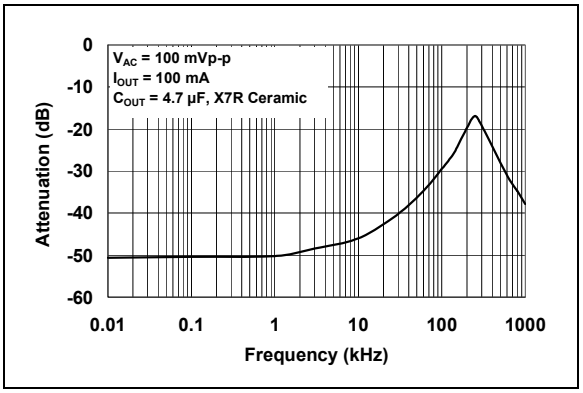


FIGURE 2-12: *Power Supply Ripple Rejection (PSRR).*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLES

Pin No.		Symbol	Function
DFN	SOT-23-5		
1	4	V_{DD}	Battery Management Input Supply
2	—	V_{DD}	Battery Management Input Supply
3	3	V_{BAT}	Battery Charge Control Output
4	—	V_{BAT}	Battery Charge Control Output
5	1	STAT	Charge Status Output
6	2	V_{SS}	Battery Management 0V Reference
7	—	NC	No Connection
8	5	PROG	Current Regulation Set and Charge Control Enable
9	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

3.1 Battery Management Input Supply (V_{DD})

A supply voltage of [V_{REG} (typical) + 0.3V] to 6V is recommended. Bypass to V_{SS} with a minimum of 4.7 µF.

3.2 Battery Charge Control Output (V_{BAT})

Connect to positive terminal of battery. Drain terminal of internal P-channel MOSFET pass transistor. Bypass to V_{SS} with a minimum of 4.7 µF to ensure loop stability when the battery is disconnected.

3.3 Charge Status Output (STAT)

STAT is an output for connection to an LED for charge status indication. Alternatively, a pull-up resistor can be applied for interfacing to a host microcontroller.

STAT is a tri-state logic output on the MCP73831 and an open-drain output on the MCP73832.

3.4 Battery Management 0V Reference (V_{SS})

Connect to negative terminal of battery and input supply.

3.5 Current Regulation Set (PROG)

Preconditioning, fast charge and termination currents are scaled by placing a resistor from PROG to V_{SS}.

The charge management controller can be disabled by allowing the PROG input to float.

3.6 Exposed Thermal Pad (EP)

An internal electrical connection exists between the Exposed Thermal Pad (EP) and the V_{SS} pin. They must be connected to the same potential on the Printed Circuit Board (PCB).

For better thermal performance, it is recommended to add vias from the land area of EP to a copper layer on the other side of the PCB.

4.0 DEVICE OVERVIEW

The MCP73831/2 are highly advanced linear charge management controllers. Figure 4-1 depicts the operational flow algorithm from charge initiation to completion and automatic recharge.

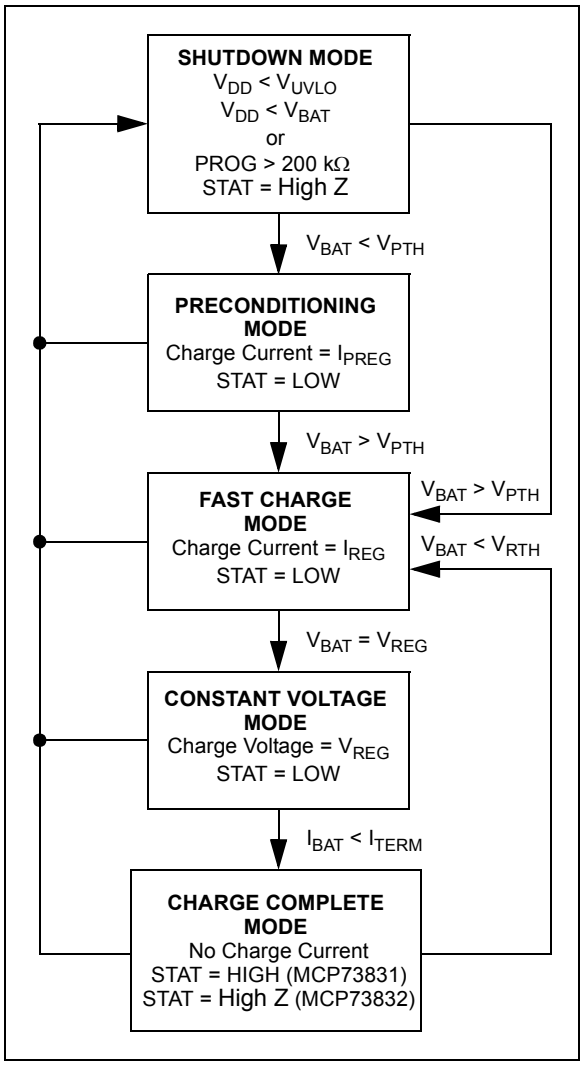


FIGURE 4-1: *Flowchart.*

4.1 Undervoltage Lockout (UVLO)

An internal UVLO circuit monitors the input voltage and keeps the charger in Shutdown mode until the input supply rises above the UVLO threshold. The UVLO circuitry has a built in hysteresis of 100 mV.

In the event a battery is present when the input power is applied, the input supply must rise to a level 150 mV above the battery voltage before the MCP73831/2 become operational.

The UVLO circuit places the device in Shutdown mode if the input supply falls to within +50 mV of the battery voltage. Again, the input supply must rise to a level 150 mV above the battery voltage before the MCP73831/2 become operational.

The UVLO circuit is always active. Whenever the input supply is below the UVLO threshold or within +50 mV of the voltage at the V_{BAT} pin, the MCP73831/2 are placed in Shutdown mode.

During any UVLO condition, the battery reverse discharge current is less than 2 µA.

4.2 Battery Detection

A 6 µA (typical) current is sourced by the V_{BAT} pin to determine if a battery is present or not. If the voltage at V_{BAT} rises to V_{REG} + 100 mV (typical), the device assumes that a battery is not present. If the voltage stays below V_{REG} + 100 mV (typical), the device assumes that a battery is detected. In order to correctly detect a battery insertion, the impedance seen by the V_{BAT} pin before the battery is connected must be greater than 2 MΩ.

4.3 Charge Qualification

For a charge cycle to begin, all UVLO conditions must be met and a battery or output load must be present. A charge current programming resistor must be connected from PROG to V_{SS}. If the PROG pin is open or floating, the MCP73831/2 are disabled and the battery reverse discharge current is less than 2 µA. In this manner, the PROG pin acts as a charge enable and can be used as a manual shutdown.

4.4 Preconditioning

If the voltage at the V_{BAT} pin is less than the preconditioning threshold, the MCP73831/2 enter a preconditioning or Trickle Charge mode. The preconditioning threshold is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for preconditioning threshold options and the **Product Identification System** for standard options.

In this mode, the MCP73831/2 supply a percentage of the charge current (established with the value of the resistor connected to the PROG pin) to the battery. The percentage or ratio of the current is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for preconditioning current options and the **Product Identification System** for standard options.

When the voltage at the V_{BAT} pin rises above the preconditioning threshold, the MCP73831/2 enter the Constant-Current or Fast Charge mode.

4.5 Fast Charge Constant-Current Mode

During the Constant-Current mode, the programmed charge current is supplied to the battery or load. The charge current is established using a single resistor from PROG to V_{SS}. Constant-Current mode is maintained until the voltage at the V_{BAT} pin reaches the regulation voltage, V_{REG}.

4.6 Constant-Voltage Mode

When the voltage at the V_{BAT} pin reaches the regulation voltage, V_{REG}, constant voltage regulation begins. The regulation voltage is factory set to 4.2V, 4.35V, 4.40V or 4.50V with a tolerance of ±0.75%.

4.7 Charge Termination

The charge cycle is terminated when, during Constant-Voltage mode, the average charge current diminishes below a percentage of the programmed charge current (established with the value of the resistor connected to the PROG pin). A 1 ms filter time on the termination comparator ensures that transient load conditions do not result in premature charge cycle termination. The percentage or ratio of the current is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for charge termination current options and the **Product Identification System** for standard options.

The charge current is latched off and the MCP73831/2 enter a Charge Complete mode.

4.8 Automatic Recharge

The MCP73831/2 continuously monitor the voltage at the V_{BAT} pin in the Charge Complete mode. If the voltage drops below the recharge threshold, another charge cycle begins and current is once again supplied to the battery or load. The recharge threshold is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for recharge threshold options and the **Product Identification System** for standard options.

4.9 Thermal Regulation

The MCP73831/2 limit the charge current based on the die temperature. The thermal regulation optimizes the charge cycle time while maintaining device reliability. Figure 4-2 depicts the thermal regulation for the MCP73831/2.

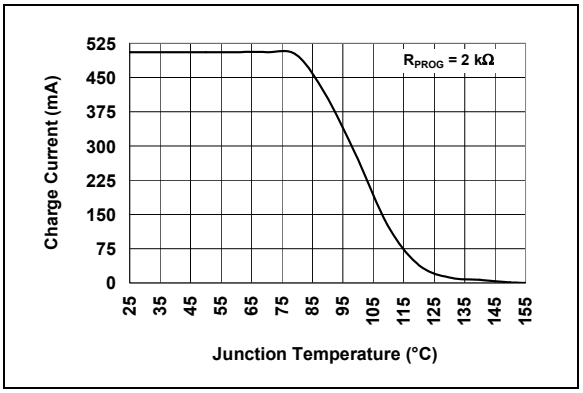


FIGURE 4-2: *Thermal Regulation.*

4.10 Thermal Shutdown

The MCP73831/2 suspend charge if the die temperature exceeds 150°C. Charging will resume when the die temperature has cooled by approximately 10°C.

5.0 DETAILED DESCRIPTION

5.1 Analog Circuitry

5.1.1 BATTERY MANAGEMENT INPUT SUPPLY (V_{DD})

The V_{DD} pin is the input supply pin for the MCP73831/2 devices. The MCP73831/2 automatically enter a Power-Down mode if the voltage on the V_{DD} input falls below the UVLO voltage (V_{STOP}). This feature prevents draining the battery pack when the V_{DD} supply is not present.

5.1.2 CURRENT REGULATION SET (PROG)

Fast charge current regulation can be scaled by placing a programming resistor (R_{PROG}) from the PROG input to V_{SS}. The program resistor and the charge current are calculated using the following equation:

$$I_{REG} = \frac{1000V}{R_{PROG}}$$

Where:

R_{PROG} = kOhms

I_{REG} = milliampere

The preconditioning trickle charge current and the charge termination current are ratiometric to the fast charge current based on the selected device options.

5.1.3 BATTERY CHARGE CONTROL OUTPUT (V_{BAT})

The battery charge control output is the drain terminal of an internal P-channel MOSFET. The MCP73831/2 provide constant current and voltage regulation to the battery pack by controlling this MOSFET in the linear region. The battery charge control output should be connected to the positive terminal of the battery pack.

5.2 Digital Circuitry

5.2.1 STATUS INDICATOR (STAT)

The charge status output of the MCP73831 has three different states: High (H), Low (L), and High-Impedance (High Z). The charge status output of the MCP73832 is open-drain. It has two different states: Low (L) and High-Impedance (High Z). The charge status output can be used to illuminate one, two or tri-color LEDs. Optionally, the charge status output can be used as an interface to a host microcontroller.

Table 5-1 summarizes the state of the status output during a charge cycle.

TABLE 5-1: STATUS OUTPUT

Charge Cycle State	STAT1	
	MCP73831	MCP73832
Shutdown	High Z	High Z
No Battery Present	High Z	High Z
Preconditioning	L	L
Constant-Current Fast Charge	L	L
Constant Voltage	L	L
Charge Complete – Standby	H	High Z

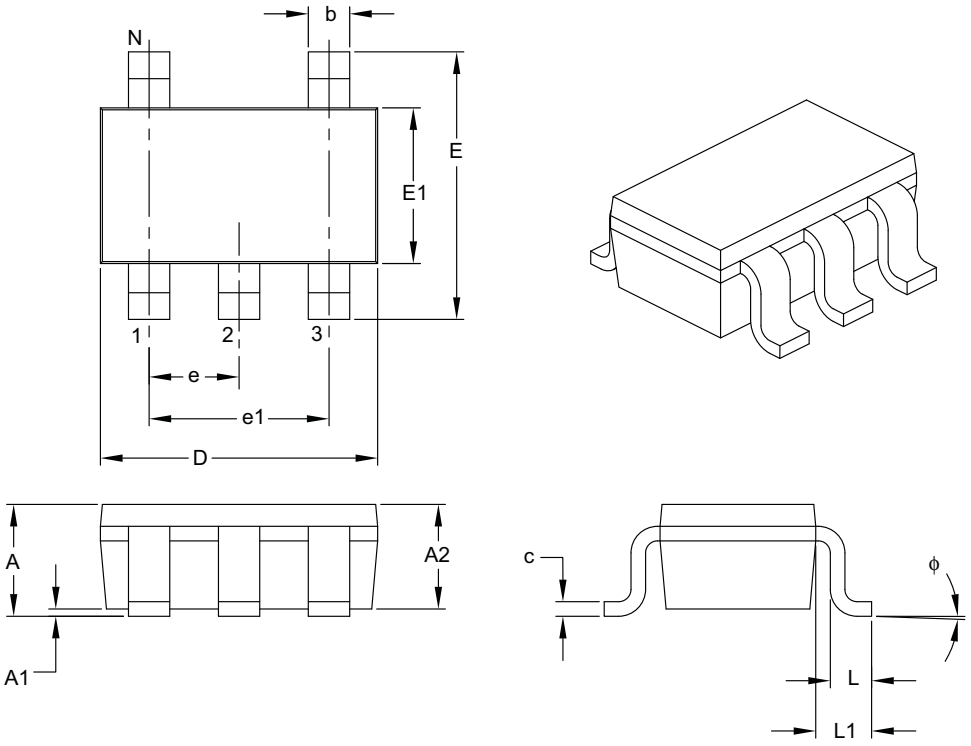
5.2.2 DEVICE DISABLE (PROG)

The current regulation set input pin (PROG) can be used to terminate a charge at any time during the charge cycle, as well as to initiate a charge cycle or initiate a recharge cycle.

Placing a programming resistor from the PROG input to V_{SS} enables the device. Allowing the PROG input to float or by applying a logic-high input signal, disables the device and terminates a charge cycle. When disabled, the device's supply current is reduced to 25 µA, typically.

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

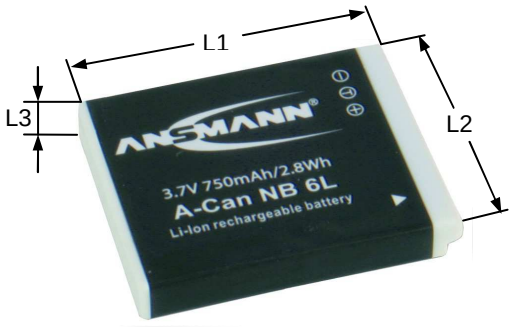
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

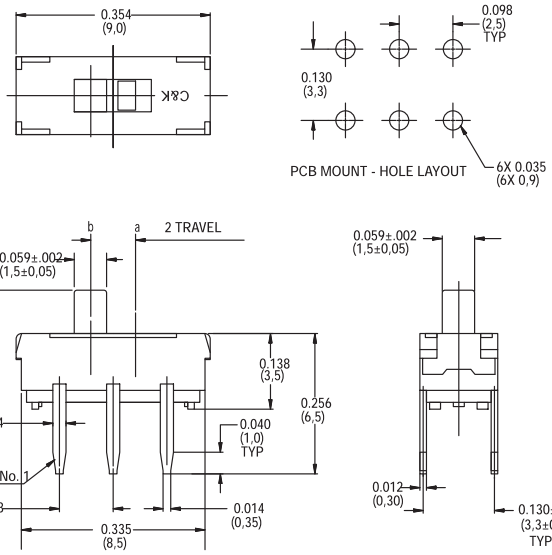
data sheet

system:	Lithium-Ion-Battery	
nominal voltage:	3.7V	
end charge voltage:	4.2V	
max. charge current:	750mA	
charge conditions		
standard charge:	325mA	for 3.5h min.
fast charge:	650mA	for 2.5h min.
charging method:	CC-CV (constant current and constant voltage)	
capacity	after standard charge	
nominal:	750mAh	at 0.2C discharge to 2.75V
minimal:	750mAh	at 0.2C discharge
	675mAh	at 1C discharge
energy:	2.8Wh	
max. continuous discharge current:	750mA	
internally safety system:	protection circuit board (pcb) with protection against overcharge, deep discharge and overload	
life time expectancy:	> 300 cycles	
ambient temperature range		
charge:	0…45°C	
discharge:	-20…60°C	
long term storage:	-20…35°C (less than 1 year)	
QCT3:	620/590	
weight:	approx. 20g	
dimensions:	L1: 41.7 ± 0.3mm L2: 34.7 ± 0.3mm L3: 7.2 ± 0.2mm	



ANSMANN®	Specifications for model/type:	A – Can NB-6L
	Ansmann drawing number / part number:	5044453
	supplier no.:	701556
	author / date:	TG / 23.10.2013

PC THRU-HOLE



Part Number
JS202011CQN
DPDT

Shown in position a

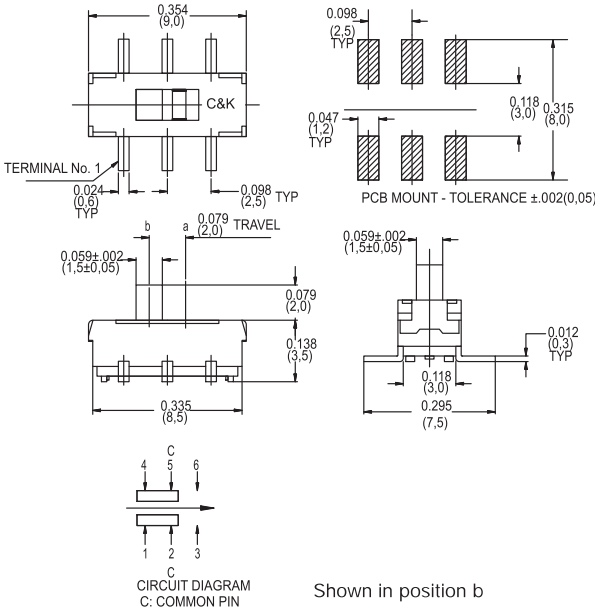
Shown in position b

SURFACE MOUNT

Part number
JS202011SCQN
DPDT

Shown in position b. Quantity per reel 1000

Available in tape & reel only, see page I-58

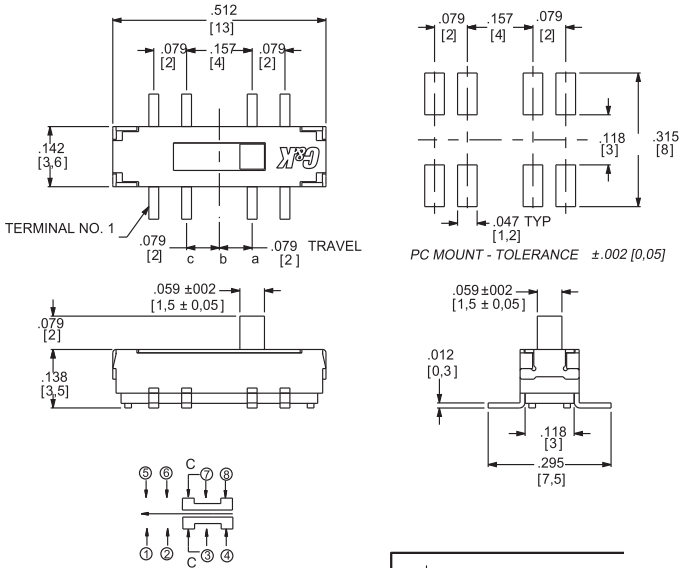


Shown in position b

Part number
JS203011SCQN
DP3T

Quantity per reel 900

Available in tape & reel only, see page I-60



CIRCUIT DIAGRAM
C: COMMON PIN

Shown in position a

Third Angle Projection

Dimensions are shown: Inches (mm)
Specifications and dimensions subject to change

TPS6300x High-Efficient Single Inductor Buck-Boost Converter With 1.8-A Switches

1 Features

- Input Voltage Range: 1.8 V to 5.5 V
- Fixed and Adjustable Output Voltage Options from 1.2 V to 5.5 V
- Up to 96% Efficiency
- 1200-mA Output Current at 3.3 V in Step-Down Mode (V_{IN} = 3.6 V to 5.5 V)
- Up to 800-mA Output Current at 3.3 V in Boost Mode (V_{IN} > 2.4 V)
- Automatic Transition Between Step-Down and Boost Mode
- Device Quiescent Current less than 50 µA
- Power-Save Mode for Improved Efficiency at Low Output Power
- Forced Fixed Frequency Operation and Synchronization Possible
- Load Disconnect During Shutdown
- Overtemperature Protection
- Available in a Small 3-mm × 3-mm 10-Pin VSON Package (QFN)

2 Applications

- All Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products
- Portable Audio Players
- Smart Phones
- Personal Medical Products
- White LEDs

3 Description

The TPS6300x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-ion or Li-polymer battery. Output currents can go as high as 1200 mA while using a single-cell Li-ion or Li-polymer battery, and discharge it down to 2.5 V or lower. The buck-boost converter is based on a fixed frequency, pulse width modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters power-save mode to maintain high efficiency over a wide load current range. The power-save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 1800 mA. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery.

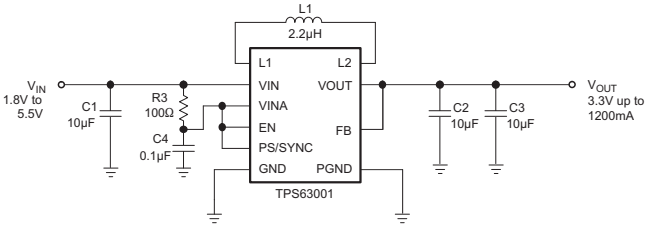
The TPS6300x devices operate over a free air temperature range of –40°C to 85°C. The devices are packaged in a 10-pin VSON package (QFN) measuring 3 mm × 3 mm (DRC).

Device Information(1)

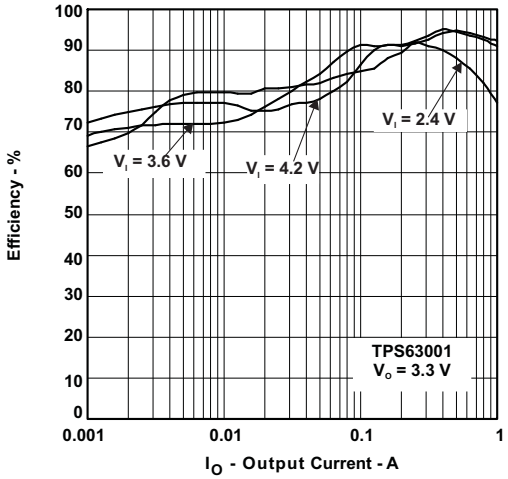
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63000	VSON (10)	3.00 mm x 3.00 mm
TPS63001		
TPS63002		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic

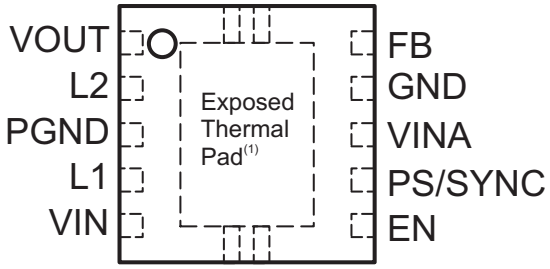


Efficiency vs Output Current



5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



(1) The exposed thermal pad is connected to PGND.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	6	IN	Enable input (1 enabled, 0 disabled)
FB	10	IN	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	9	—	Control / logic ground
L1	4	IN	Connection for inductor
L2	2	IN	Connection for inductor
PGND	3	—	Power ground
PS/SYNC	7	IN	Enable / disable power-save mode (1 disabled, 0 enabled, clock signal for synchronization)
VIN	5	IN	Supply voltage for power stage
VINA	8	IN	Supply voltage for control stage
VOUT	1	OUT	Buck-boost converter output
Exposed Thermal Pad	—	—	The exposed thermal pad is connected to PGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage on VIN, VINA, L1, L2, VOUT, PS/SYNC, EN, FB	–0.3	7	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage at VIN, VINA	1.8	5.5	V
Operating free air temperature, T_A	–40	85	°C
Operating virtual junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS6300x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE							
V_{IN}	Input voltage range			1.8		5.5	V
V_{IN}	Input voltage range for start-up			1.9		5.5	V
V_{OUT}	TPS63000 output voltage range			1.2		5.5	V
V_{FB}	TPS63000 feedback voltage		PS/SYNC = V_{IN}	495	500	505	mV
f	Oscillator frequency			1250		1500	kHz
	Frequency range for synchronization			1250		1800	kHz
I_{SW}	Switch current limit		V_{IN} = V_{INA} = 3.6 V, T_A = 25°C	1600	1800	2000	mA
	High-side switch ON-resistance		V_{IN} = V_{INA} = 3.6 V		100		mΩ
	Low-side switch ON-resistance		V_{IN} = V_{INA} = 3.6 V		100		mΩ
	Line regulation					0.5%	
	Load regulation					0.5%	
I_q	Quiescent current	VIN	I_{OUT} = 0 mA, V_{EN} = V_{IN} = V_{INA} = 3.6 V, V_{OUT} = 3.3 V		1	1.5	µA
		VINA			40	50	µA
		VOUT (adjustable output voltage)			4	6	µA
	FB input impedance (fixed output voltage)				1		MΩ
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = V_{INA} = 3.6 V		0.1	1	µA
CONTROL STAGE							
V_{UVLO}	Undervoltage lockout threshold		V_{INA} voltage decreasing	1.5	1.7	1.8	V
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped on GND or VINA		0.01	0.1	µA
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

7 Detailed Description

7.1 Overview

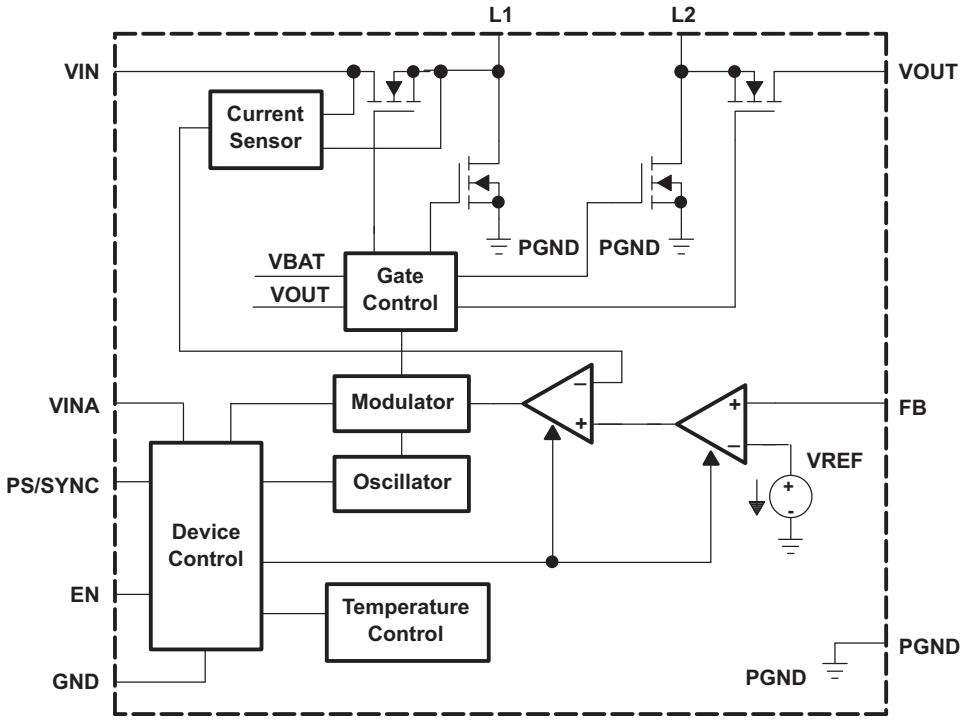
The controlling circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages a resistive voltage divider must be connected to that pin. At fixed output voltages FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The controller circuit also senses the average input current as well as the peak input current. With this, maximum input power can be controlled as well as the maximum peak current to achieve a safe and stable operation under all possible conditions. To finally protect the device from overheating, an internal temperature sensor is implemented.

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter.

7.2 Functional Block Diagram



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS6300x DC–DC converters are intended for systems powered by one-cell Li-ion or Li-polymer battery with a typical voltage between 2.3 V and 4.5 V. They can also be used in systems powered by a double or triple cell alkaline, NiCd, or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. Additionally, any other voltage source with a typical output voltage between 1.8 V and 5.5 V can power systems where the TPS6300x is used.

8.2 Typical Application

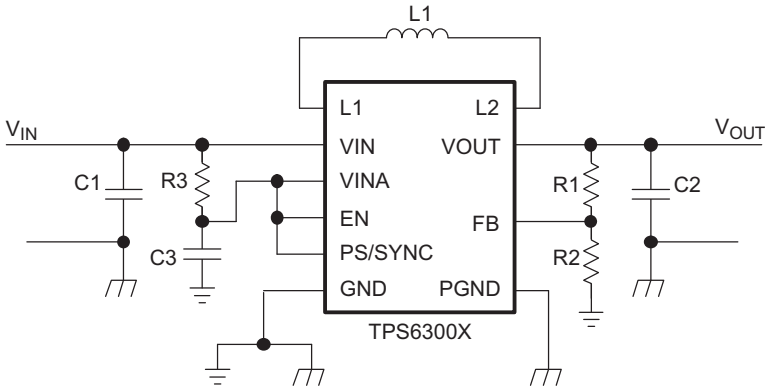


Figure 2. Typical Application Circuit for Adjustable Output Voltage Option

8.2.1 Design Requirements

The TPS63000 series of buck-boost converters have internal loop compensation. Therefore, the external LC filter has to be selected according to the internal compensation.

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions*.

For the fixed output voltage option the feedback pin needs to be connected to VOUT.

Table 1 shows the list of components for the application curves.

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63000 / TPS63001 / TPS63002	Texas Instruments
L1	VLF4012-2R2	TDK
C1	10 µF 6.3 V, 0603, X7R ceramic	
C2	2 × 10 µF 6.3 V, 0603, X7R ceramic	
C3	0.1 µF, X7R ceramic	
R3	100 Ω	
R1, R2	Depending on the output voltage at TPS63000, not used at TPS63001 / TPS63002	

8.2.2 Detailed Design Procedure

8.2.2.1 Programming the Output Voltage

Within the TPS6300x family, there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. At the adjustable output voltage versions, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on those two values, the recommended value for R_2 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. TI recommends to keep the value for this resistor in the range of 200 kΩ. From that, the value of the resistor connected between VOUT and FB, R_1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 1.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor should be chosen for R_1. To improve control performance using a feedforward capacitor in parallel to R_1 is recommended. The value for the feedforward capacitor can be calculated using Equation 2.

$$C_{ff} = \frac{2.2\ \mu s}{R_1} \quad (2)$$

8.2.2.2 Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into power-save mode, and efficiency. See Table 2 for typical inductors.

Table 2. List of Recommended Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	LPS3015
	LPS4012
Murata	LQH3NP
Tajo Yuden	NR3015
TDK	VLF3215
	VLF4012

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady-state operation is calculated using Equation 4. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{3}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{4}$$

where

- D = Duty Cycle in Boost mode
- f = Converter switching frequency (typical 2.5MHz)
- L = Inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)

NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. ITI recommends to choose an inductor with a saturation current 20% higher than the value calculated using Equation 4. Possible inductors are listed in Table 2.

8.2.2.3 Capacitor Selection

8.2.2.3.1 *Input Capacitor*

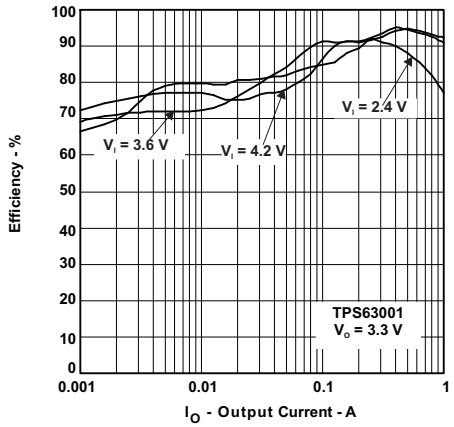
At least a 4.7-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

8.2.2.3.2 *Output Capacitor*

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. The recommended nominal output capacitance value is 15 µF.

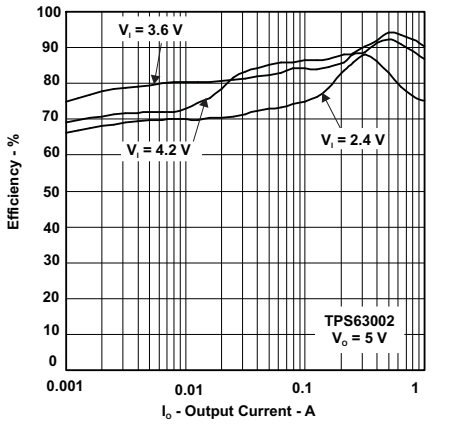
There is also no upper limit for the output capacitance value. Larger capacitors causes lower output voltage ripple as well as lower output voltage drop during load transients.

8.2.3 Application Curves



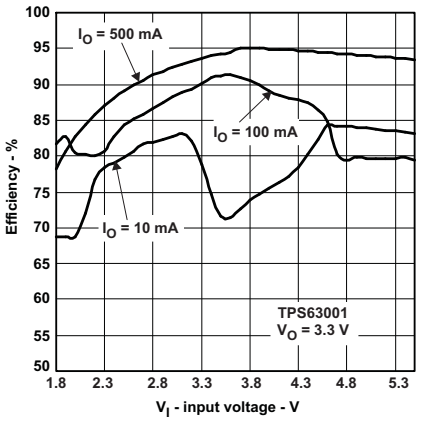
V_O = 3.3 V Power Save enabled

Figure 3. Efficiency vs Output Current (TPS63001)



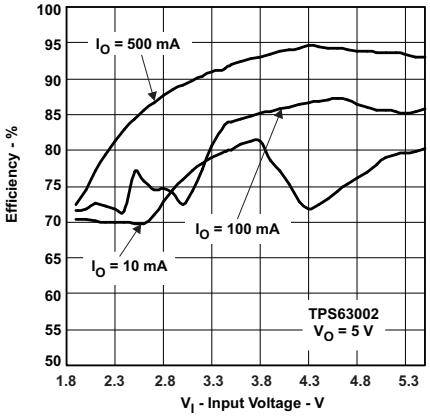
V_O = 5 V Power Save enabled

Figure 4. Efficiency vs Output Current (TPS63002)



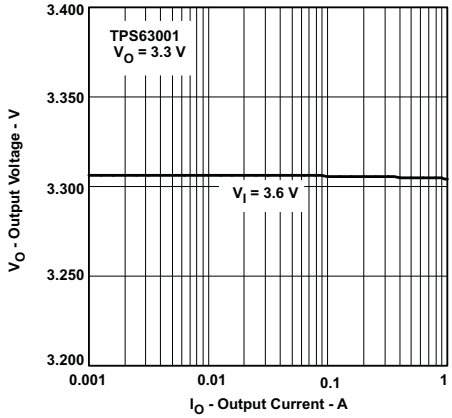
V_O = 3.3 V Power Save enabled

Figure 5. Efficiency vs Input Voltage (TPS63001)



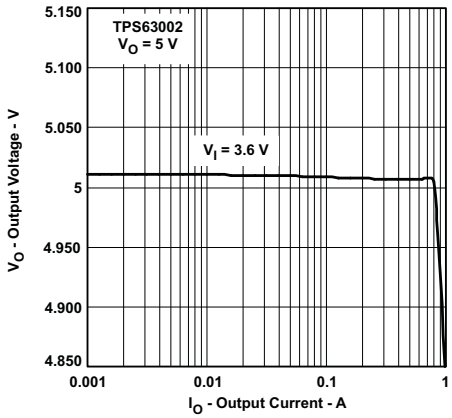
V_O = 5 V Power Save enabled

Figure 6. Efficiency vs Input Voltage (TPS63002)



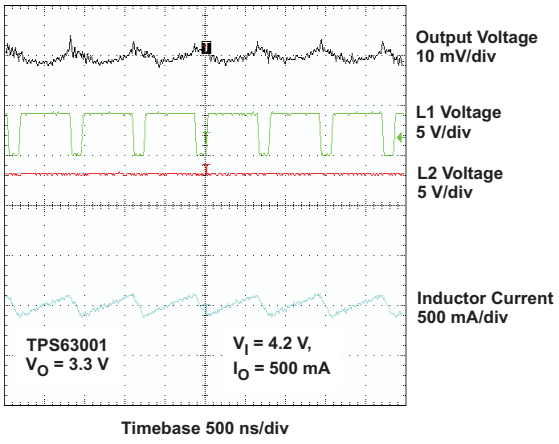
V_O = 3.3 V

Figure 7. Output Voltage vs Output Current (TPS63001)



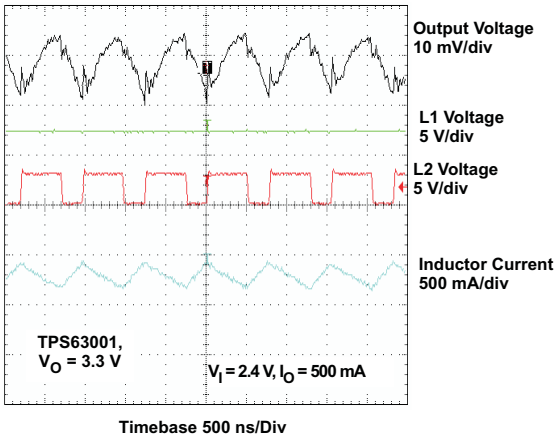
V_O = 5 V

Figure 8. Output Voltage vs Output Current (TPS63002)



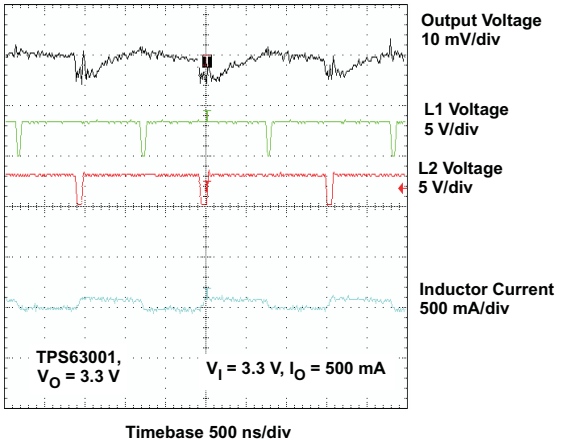
V_O = 3.3 V V_I = 4.2 V I_O = 500 mA

Figure 9. Output Voltage in Continuous Current Mode (TPS63001, V_{IN} > V_{OUT})



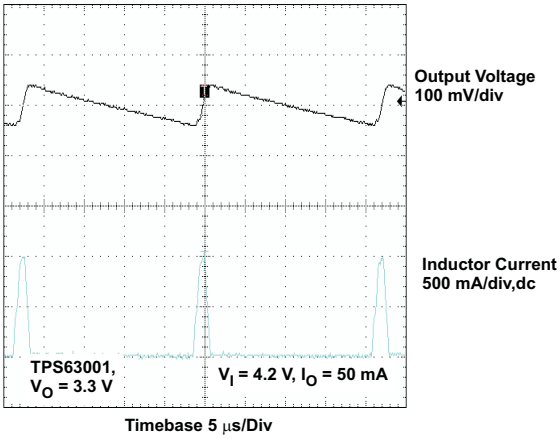
V_O = 3.3 V V_I = 2.4 V I_O = 500 mA

Figure 10. Output Voltage in Continuous Current Mode (TPS63001, V_{IN} > V_{OUT})



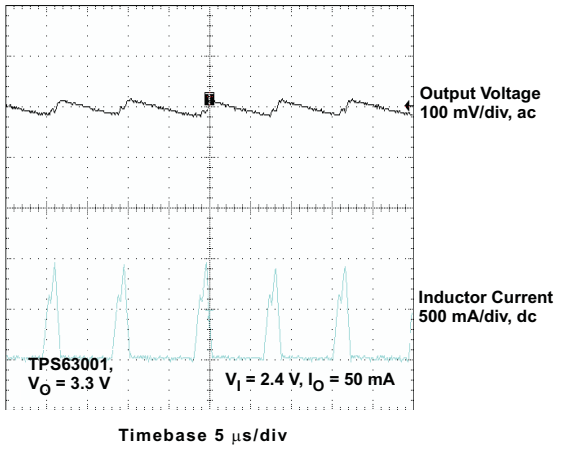
V_O = 3.3 V V_I = 3.3 V I_O = 500 mA

Figure 11. Output Voltage in Continuous Current Mode ($TPS63001$, $V_{IN} = V_{OUT}$)



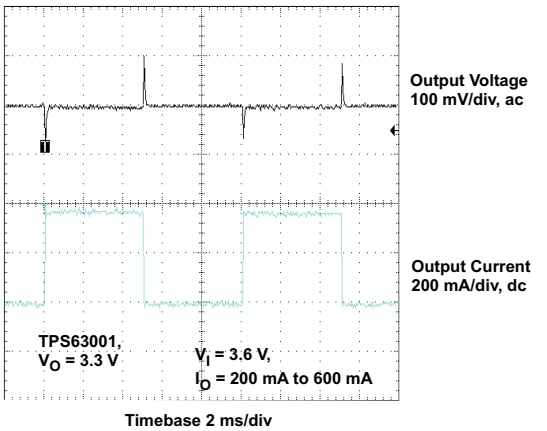
V_O = 3.3 V V_I = 4.2 V I_O = 50 mA

Figure 12. Output Voltage in Power-Save Mode ($TPS63001$, $V_{IN} > V_{OUT}$)



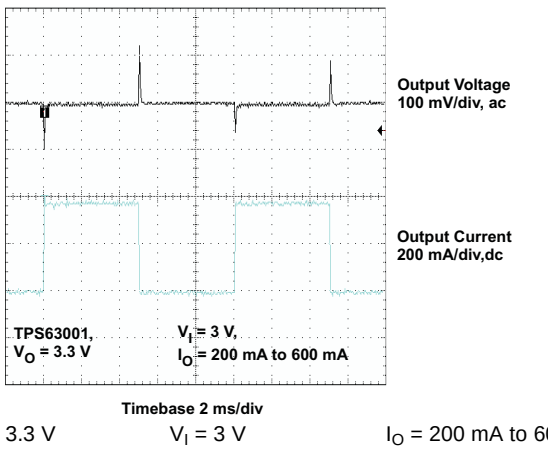
V_O = 3.3 V V_I = 2.4 V I_O = 50 mA

Figure 13. Output Voltage in Power-Save Mode ($TPS63001$, $V_{IN} < V_{OUT}$)



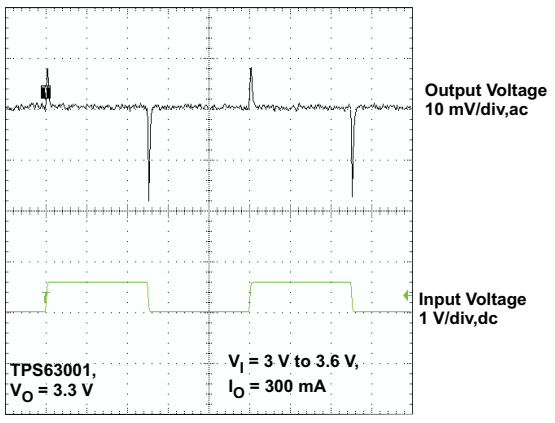
V_O = 3.3 V V_I = 3.6 V I_O = 200 mA to 600 mA

Figure 14. Load Transient Response ($TPS63001$, $V_{IN} > V_{OUT}$)



V_O = 3.3 V V_I = 3 V I_O = 200 mA to 600 mA

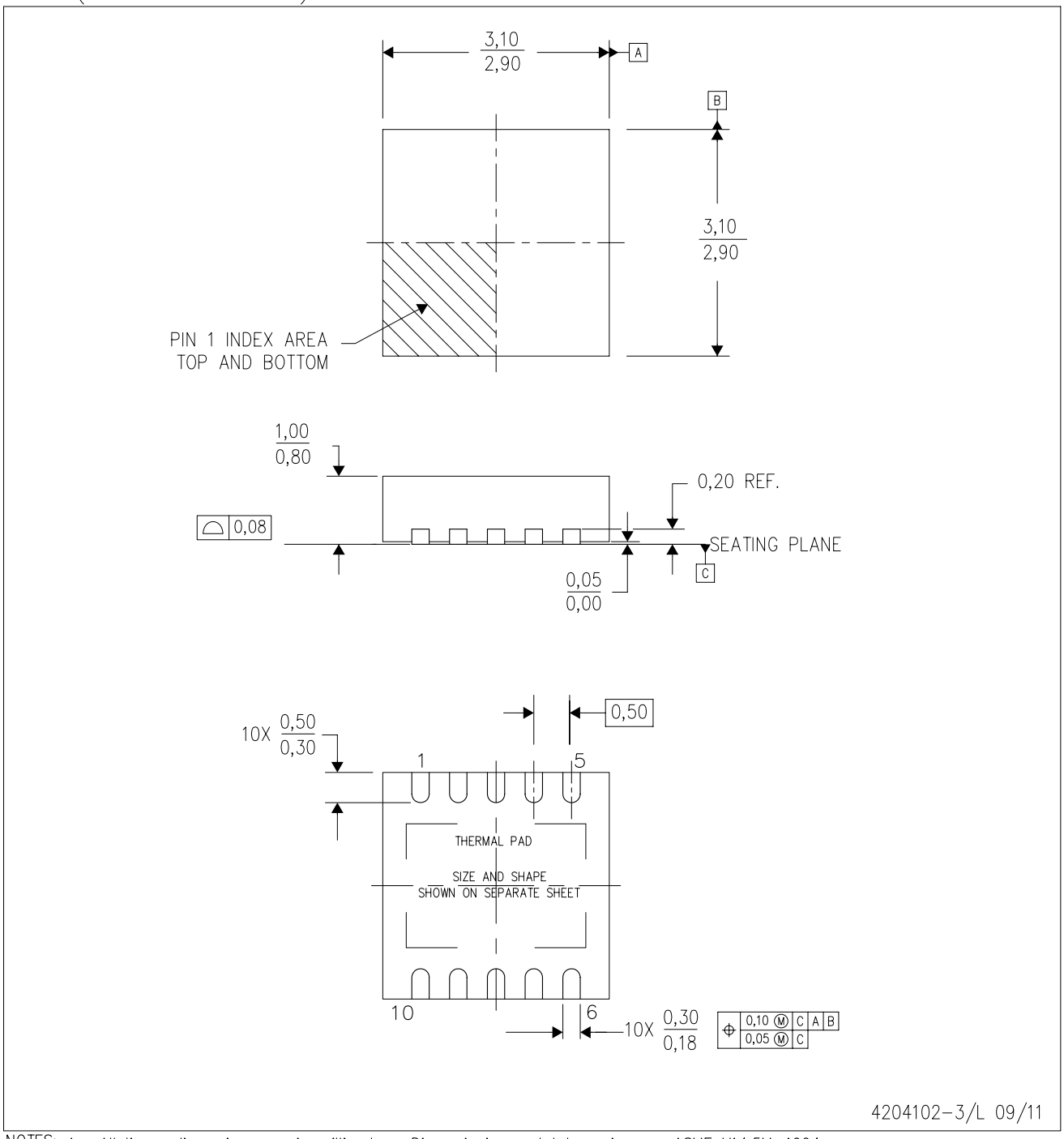
Figure 15. Load Transient Response ($TPS63001$, $V_{IN} < V_{OUT}$)



V_O = 3.3 V V_I = 3 V to 3.6 V I_O = 300 mA

Figure 16. Line Transient Response ($TPS63001$, I_{OUT} = 300 mA)

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

TLV743P 300-mA, Low-Dropout Regulator

1 Features

- Input Voltage Range: 1.4 V to 5.5 V
- Stable Operation With 1-µF Ceramic Output Capacitor
- Foldback Overcurrent Protection
- Packages:
  - SOT-23 (5)
- Very Low Dropout: 125 mV at 300 mA (3.3 V_{OUT})
- Accuracy: 1% (Typical), 1.4% (Maximum)
- Low I_Q: 34 µA
- Available in Fixed-Output Voltages: 1 V to 3.3 V
- High PSRR: 50 dB at 1 kHz
- Active Output Discharge

2 Applications

- Tablets
- Smartphones
- Notebook and Desktop Computers
- Portable Industrial and Consumer Products
- WLAN and Other PC Add-On Cards
- Camera Modules

3 Description

The TLV743P low-dropout linear regulator (LDO) is an ultra-small, low quiescent current LDO that sources 300 mA with good line and load transient performance. The device provides a typical accuracy of 1%.

The TLV743P is designed to be stable with a small output capacitor with a value of 1 µF. The TLV743P device provides foldback current control during device power up and enabling. This functionality is especially important in battery-operated devices.

The TLV743P provides an active pulldown circuit to quickly discharge output loads when the device is disabled.

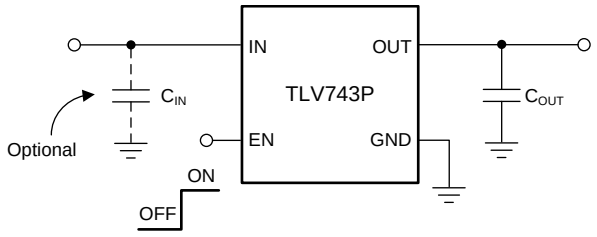
The TLV743P is available in a standard DBV (SOT-23) package.

Device Information[1]

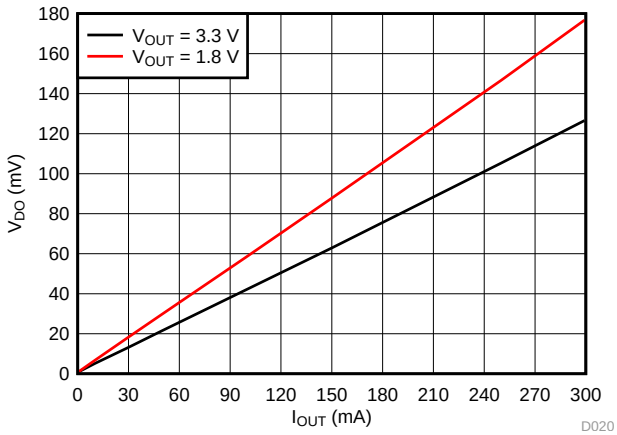
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV743P	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application Circuit

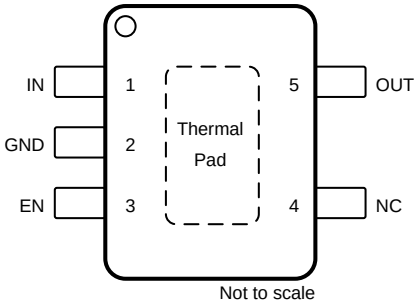


Dropout Voltage vs Output Current



5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

NC- no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Drive EN greater than 0.9 V to turn on the regulator. Drive EN less than 0.35 V to put the LDO into shutdown mode.
GND	2	—	Ground pin
IN	1	I	Input pin. A small capacitor is recommended from this pin to ground. See *Input and Output Capacitor Selection* for more details.
NC	4	—	No internal connection
OUT	5	O	Regulated output voltage pin. For best transient response, use a small 1-μF ceramic capacitor from this pin to ground. See *Input and Output Capacitor Selection* for more details.
Thermal pad	—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	V_{IN} + 0.3	
	V_{OUT}	–0.3	3.6	
Current	I_{OUT}	Internally limited		A
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	160	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input range	1.4		5.5	V
V_{OUT}	Output range	1		3.3	V
I_{OUT}	Output current	0		300	mA
V_{EN}	Enable range	0		V_{IN}	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV743P DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted). All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.4		5.5	V
	DC output accuracy	T_J = 25°C		–1%		1%	
		–40°C ≤ T_J ≤ 125°C		–1.4%		1.4%	
UVLO	Undervoltage lockout	V_{IN} rising			1.3	1.4	V
		V_{IN} falling			1.25		
$\Delta V_{O(\Delta VI)}$	Line regulation	ΔVI = $V_{IN(nom)}$ to $V_{IN(nom)}$ + 1			1		mV
$\Delta V_{O(\Delta IO)}$	Load regulation	ΔIO = 1 mA to 300 mA	DBV package		16		mV
					25		
V_{DO}	Dropout voltage(1)	V_{OUT} = 0.98 × $V_{OUT(nom)}$, I_{OUT} = 300 mA	V_{OUT} = 1.1 V, –40°C ≤ T_J ≤ 85°C			480	mV
			1.2 V ≤ V_{OUT} < 1.5 V, –40°C ≤ T_J ≤ 85°C			420	
			1.5 V ≤ V_{OUT} < 1.8 V, –40°C ≤ T_J ≤ 85°C			370	
			1.8 V ≤ V_{OUT} < 2.5 V, –40°C ≤ T_J ≤ 85°C			270	
			2.5 V ≤ V_{OUT} < 3.3 V, –40°C ≤ T_J ≤ 85°C			260	
			V_{OUT} = 3.3 V, –40°C ≤ T_J ≤ 85°C		125	220	
			1.2 V ≤ V_{OUT} < 1.5 V, –40°C ≤ T_J ≤ 125°C			450	
			1.5 V ≤ V_{OUT} < 1.8 V, –40°C ≤ T_J ≤ 125°C			400	
			1.8 V ≤ V_{OUT} < 2.5 V, –40°C ≤ T_J ≤ 125°C			300	
			2.5 V ≤ V_{OUT} < 3.3 V, –40°C ≤ T_J ≤ 125°C			290	
			V_{OUT} = 3.3 V, –40°C ≤ T_J ≤ 125°C		125	270	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			34	60	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.35 V, 2 V ≤ V_{IN} ≤ 5.5 V, T_J = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8 V, I_{OUT} = 300 mA	f = 100 Hz		68		dB
			f = 10 kHz		35		
			f = 100 kHz		28		
V_n	Output noise voltage	Bandwidth = 10 Hz to 100 kHz, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			120		μV_{RMS}
$V_{EN(HI)}$	EN pin high voltage (enabled)			0.9	0.63		V
$V_{EN(LO)}$	EN pin low voltage (disabled)				0.52	0.35	V
I_{EN}	EN pin current	V_{EN} = 5.5 V			0.01		µA

(1) Dropout voltage for the TLV743P is not valid at room temperature. The device engages undervoltage lockout (V_{IN} < $UVLO_{FALL}$) before the dropout condition is met.

Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted). All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Startup time	Time from EN assertion to 98% × V_{OUT}(nom) V_{OUT} = 1 V I_{OUT} = 0 mA		250		µs
		Time from EN assertion to 98% × V_{OUT}(nom) V_{OUT} = 3.3 V I_{OUT} = 0 mA		800		
	Pulldown resistor	V_{IN} = 2.3 V		120		Ω
I_{LIM}	Output current limit		360			mA
I_{OS}	Short-circuit current limit	V_{OUT} shorted to GND V_{OUT} = 1 V		150		mA
		V_{OUT} shorted to GND V_{OUT} = 3.3 V		170		
T_{sd}	Thermal shutdown	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

7 Typical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

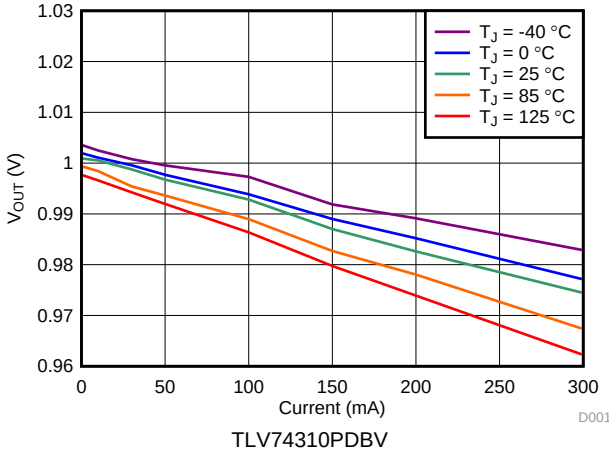


Figure 1. 1-V Load Regulation vs I_{OUT} and Temperature

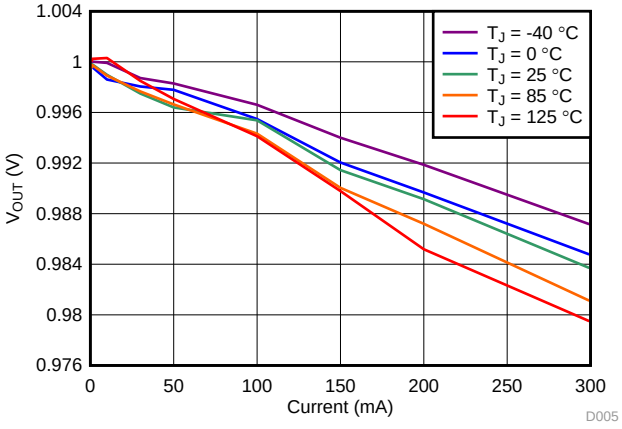


Figure 2. 1-V Load Regulation vs I_{OUT} and Temperature

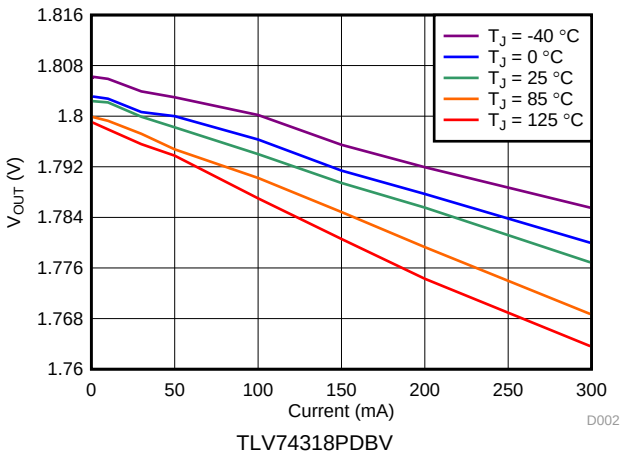


Figure 3. 1.8-V Load Regulation vs I_O and Temperature

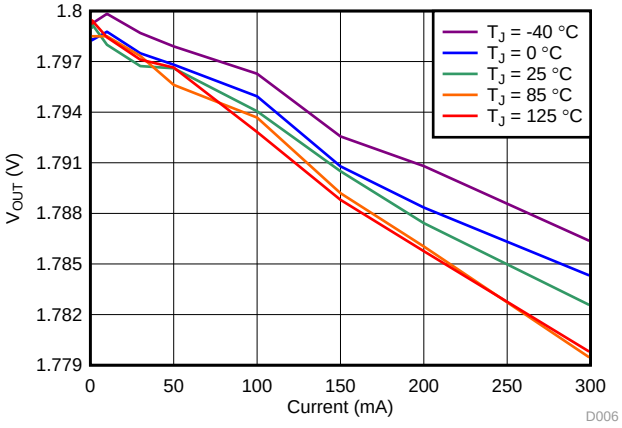


Figure 4. 1.8-V Load Regulation vs I_{OUT} and Temperature

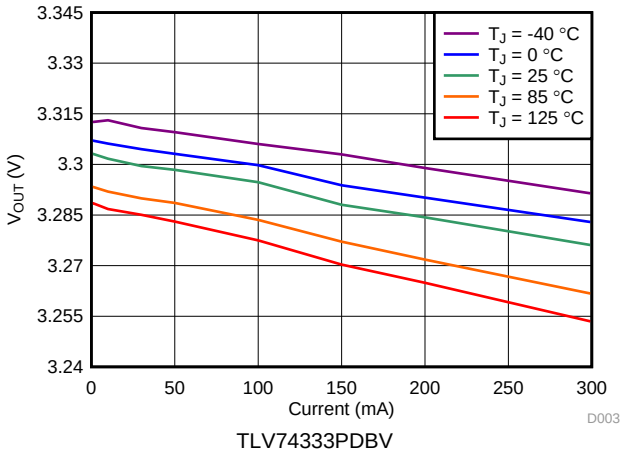


Figure 5. 3.3-V Load Regulation vs I_{OUT} and Temperature

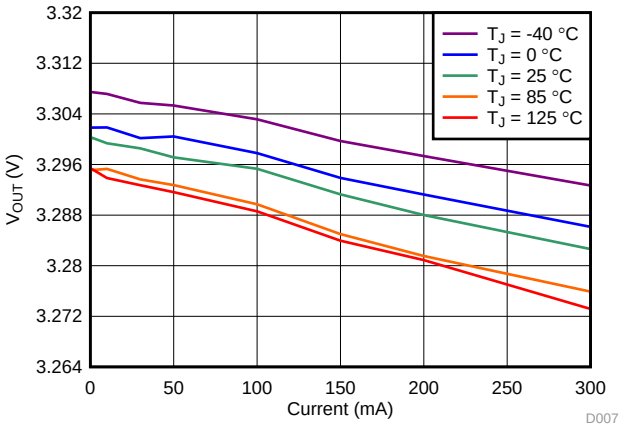


Figure 6. 3.3-V Load Regulation vs I_{OUT} and Temperature

Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

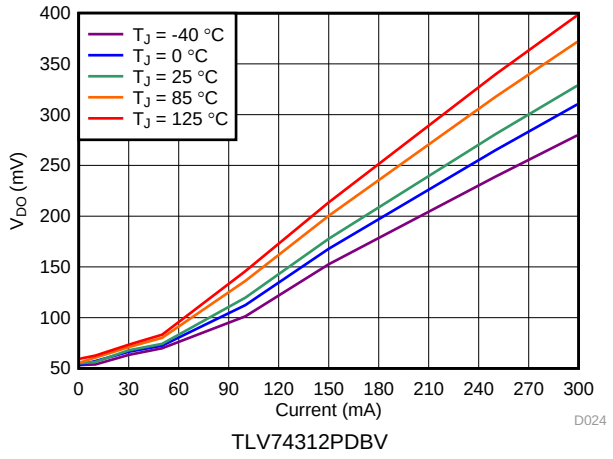


Figure 7. 1.2-V Dropout Voltage vs I_{OUT} and Temperature

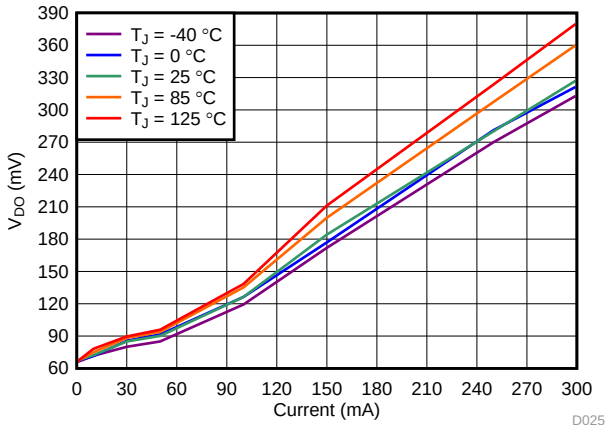


Figure 8. 1.2-V Dropout Voltage vs I_{OUT} and Temperature

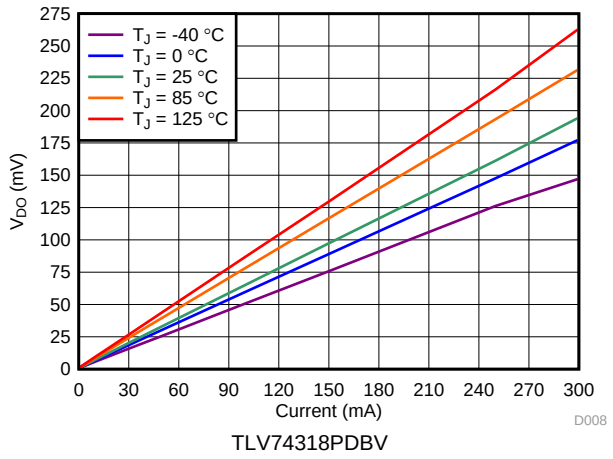


Figure 9. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

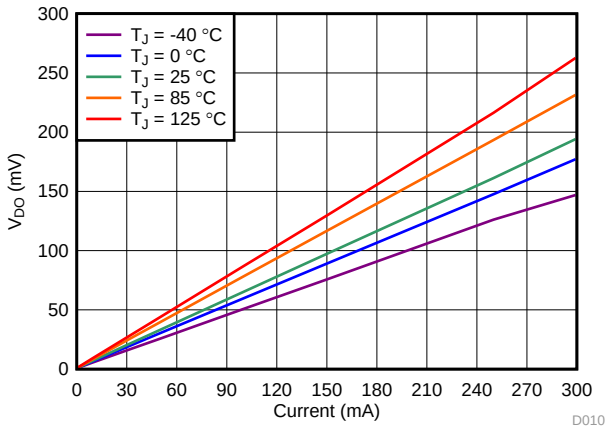


Figure 10. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

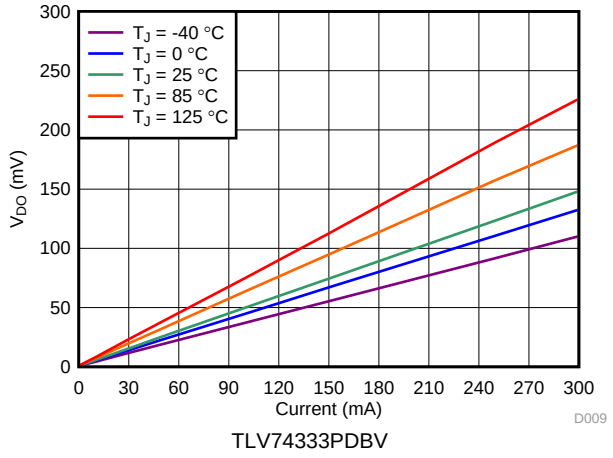


Figure 11. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

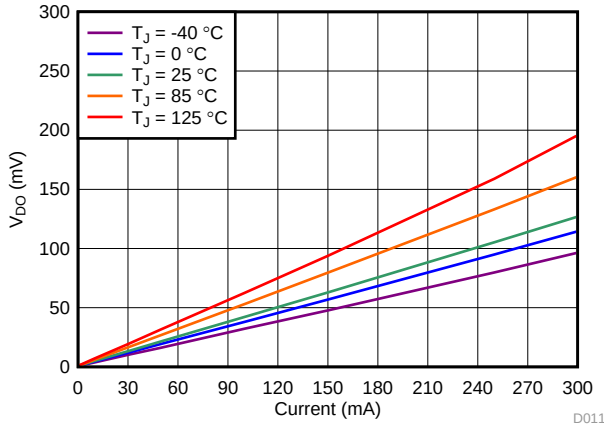


Figure 12. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

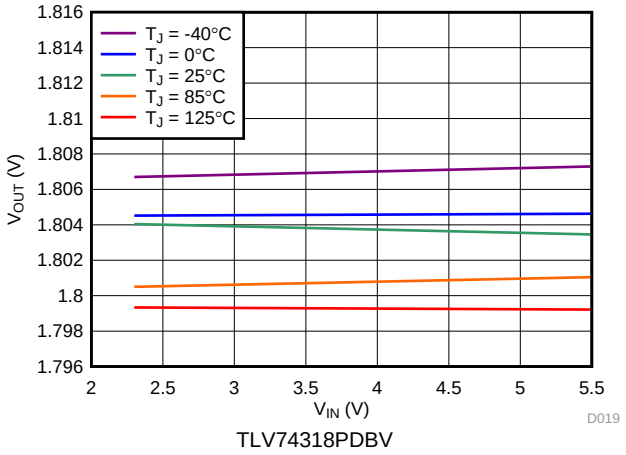


Figure 13. 1.8-V Regulation vs V_{IN} (Line Regulation) and Temperature

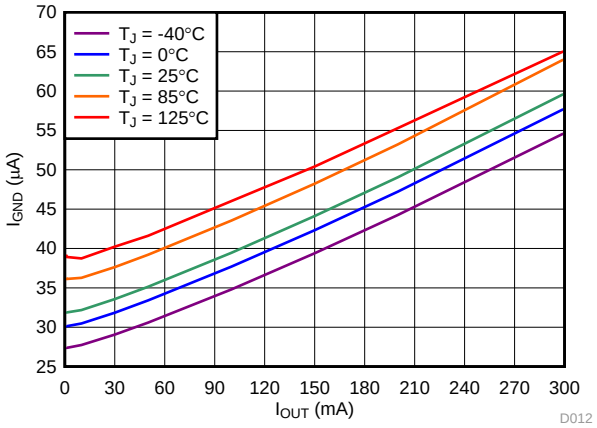


Figure 14. Ground Pin Current vs I_{OUT} and Temperature

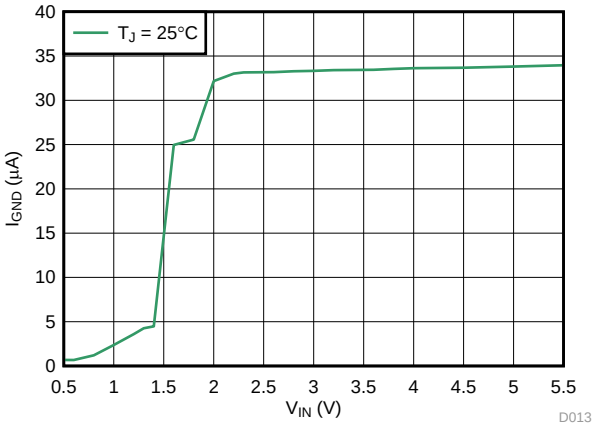


Figure 15. Ground Pin Current vs V_{IN}

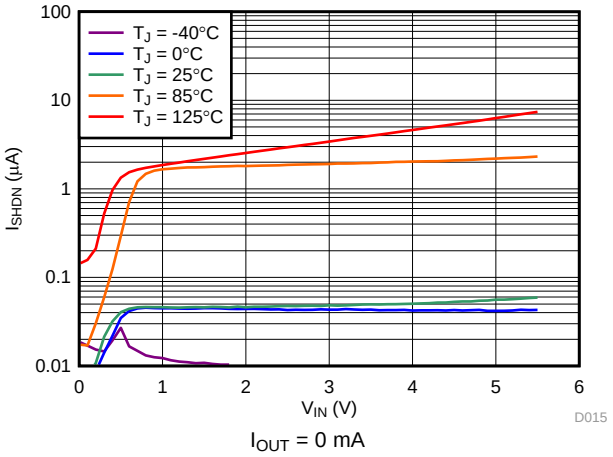


Figure 16. Shutdown Current vs V_{IN} and Temperature

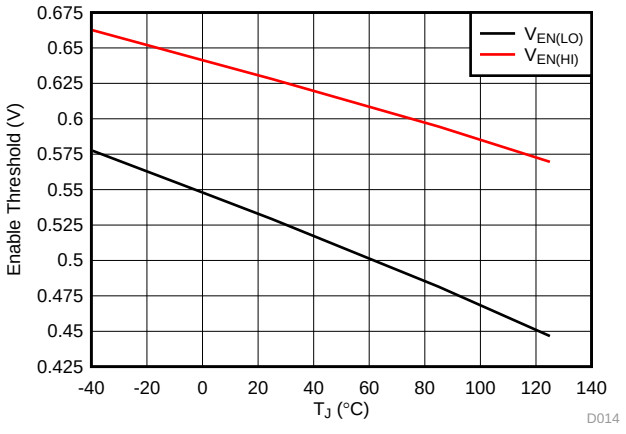


Figure 17. Enable Threshold vs Temperature

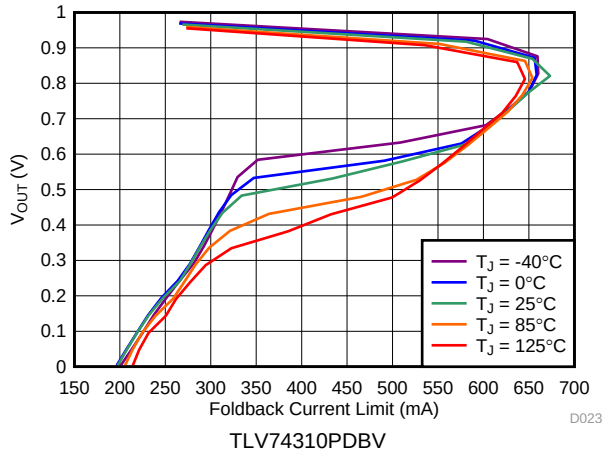


Figure 18. 1-V Foldback Current Limit vs I_{OUT} and Temperature

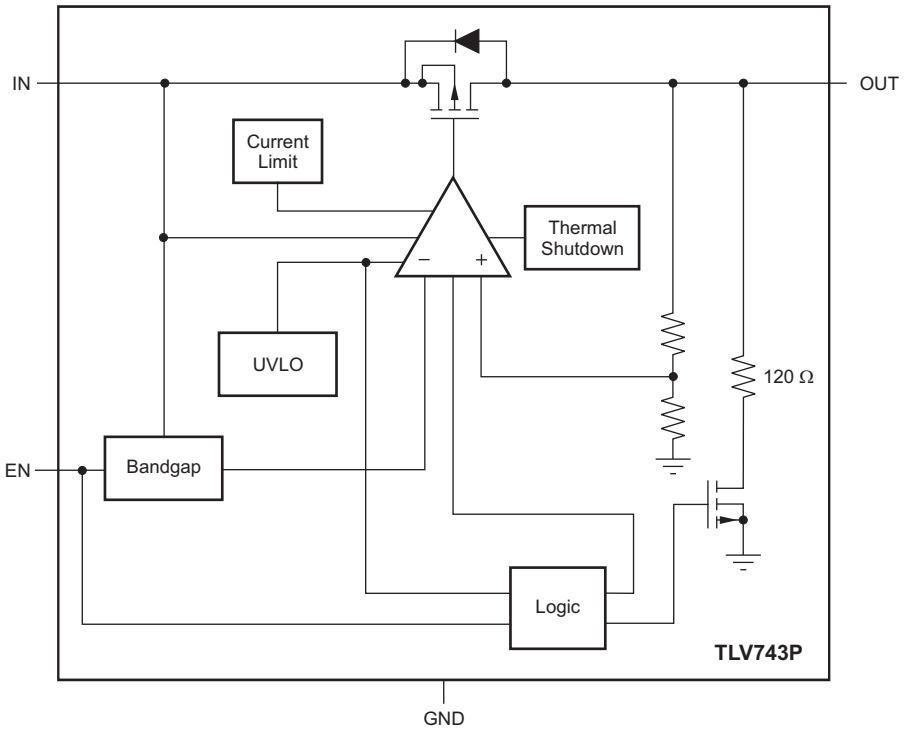
8 Detailed Description

8.1 Overview

The TLV743P device belongs to a new family of next-generation, low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low-dropout voltage, make this device well-suited for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The TLV743P device uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage, $UVLO_{RISE}$. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. During UVLO disable, the output connects to ground with a 120-Ω pulldown resistor.

8.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.35 V. If shutdown capability is not required, connect EN to IN.

The TLV743P device has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in Equation 1:

$$t = \frac{120 \times R_L}{120 + R_L} \times C_{OUT} \quad (1)$$

8.3.3 Internal Foldback Current Limit

The TLV743P device has an internal foldback current limit that protects the regulator during fault conditions. The current allowed through the device is reduced as the output voltage falls. When the output is shorted, the LDO supplies a typical current of 150 mA. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output is shorted, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{OS}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Information* for more details.

The foldback current limit circuit limits the current allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{LIM}) during startup. See Figure 18 to Figure 20 for typical foldback current limit values. If the output is loaded by a constant-current load during startup, or if the output voltage is negative when the device is enabled, then the required load current by the load may exceed the foldback current limit and the device may not rise to the full output voltage. For constant current loads, disable the output load until the TLV743P has risen to the nominal output voltage.

The TLV743P PMOS pass element has an intrinsic body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. Do not force the output voltage to exceed the input voltage because excessively high current may flow through the body diode.

8.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 160°C. Disabling the device eliminates power dissipated by the device, which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, which protects the device from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV743P internal protection circuitry protects against overload conditions, but is not intended to be active in normal operation. Continuously running the TLV743P device into thermal shutdown degrades device reliability.

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the thermal shutdown temperature.

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

When the device is disabled, the active pulldown resistor discharges the output.

Table 1 lists the conditions that result in different operating modes.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT}(nom) + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT}(nom) + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 160°C$

9 Application and Implementation

9.1 Application Information

9.1.1 Input and Output Capacitor Selection

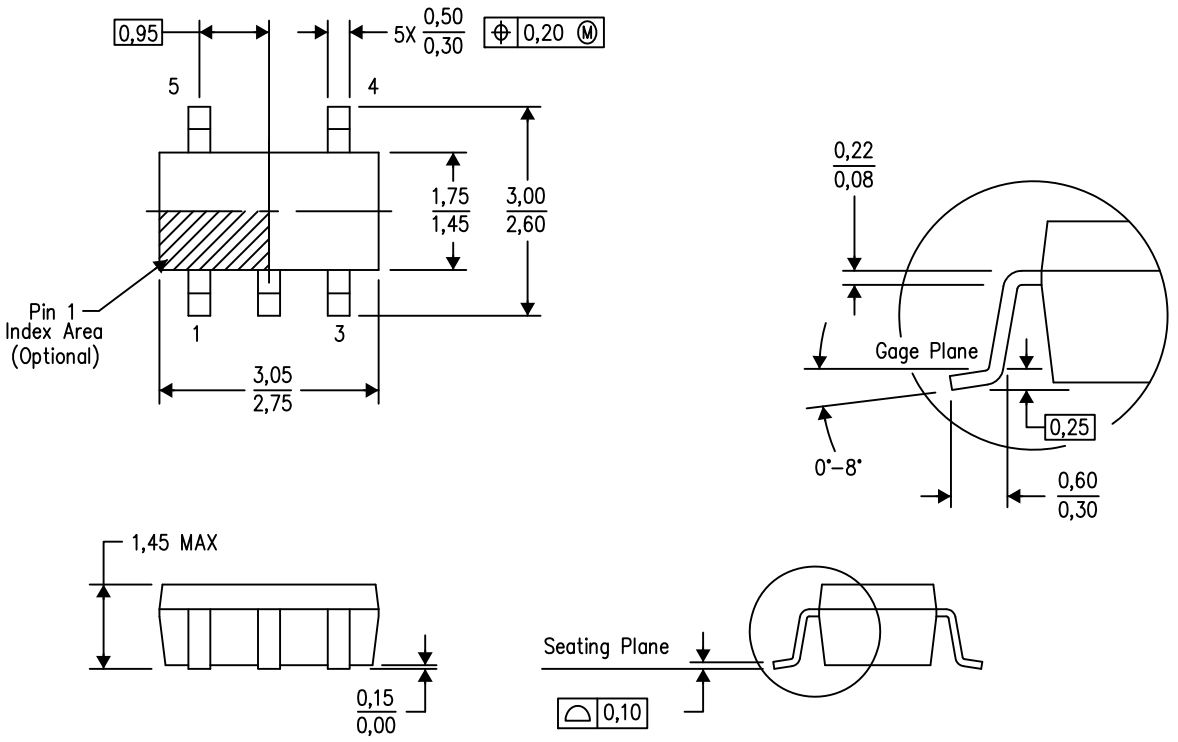
The TLV743P device uses an advanced internal control loop to obtain stable operation with the use of input or output capacitors. An output capacitance of 1 μF or larger generally provides good dynamic response. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, increased output impedance from the input supply may compromise the performance of the TLV743P. Good analog design practice is to connect a 0.1-μF to 1-μF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is greater than 0.5 Ω. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

9.1.2 Dropout Voltage

The TLV743P device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See Figure 7 to Figure 12 for typical dropout values.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

LM4041-N-xx Precision Micropower Shunt Voltage Reference

1 Features

- Qualified for Automotive Applications
- SEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Temperature Range
  - Device Temperature Grade 3: –40°C to +85°C Ambient Temperature Range (For SOT-23 Only)
- Available in Standard, AEC Q-100 Grade 1 (Extended Temperature Range), and Grade 3 (Industrial Temperature Range) Qualified Versions (SOT-23 Only)
- Small Packages: SOT-23, TO-92, and SC70
- No Output Capacitor Required
- Tolerates Capacitive Loads
- Reverse Breakdown Voltage Options of 1.225 V and Adjustable
- Output Voltage Tolerance (A grade, 25°C) = ±0.1%(Maximum)
- Low Output Noise (10 Hz to 10kHz) = 20 μV_{rms}
- Wide Operating Current Range of 60 µA to 12 mA
- Industrial Temperature Range (LM4041A/B-N, LM4041-N-Q1A/Q1B) of −40°C to +85°C
- Extended Temperature Range (LM4041C/D/E-N, LM4041-N-Q1C/Q1D/Q1E) of −40°C to +125°C
- Low Temperature Coefficient of 100 ppm/°C (Maximum)

2 Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Automotive
- Precision Audio Components

3 Description

Ideal for space-critical applications, the LM4041-N precision voltage reference is available in the sub-miniature SC70 and SOT-23 surface-mount packages. The advanced design of the LM4041-N eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4041-N easy to use. Further reducing design effort is the availability of a fixed (1.225 V) and adjustable reverse breakdown voltage. The minimum operating current is 60 µA for the LM4041-N 1.2 and the LM4041-N ADJ. Both versions have a maximum operating current of 12 mA.

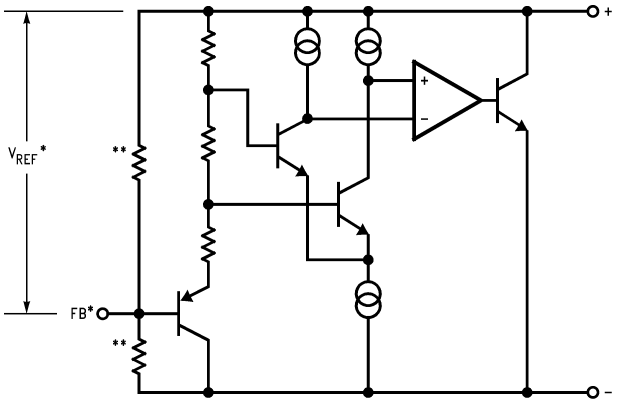
The LM4041-N uses fuse and Zener-zap reverse breakdown or reference voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM4041-N	SC70 (5)	1.25 mm × 2.00 mm
	SOT-23 (3)	1.30 mm × 2.92 mm
	TO-92 (3)	4.30 mm × 4.30 mm
LM4041-N-Q1	SOT-23 (3)	1.30 mm × 2.92 mm

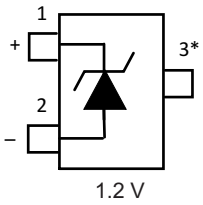
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

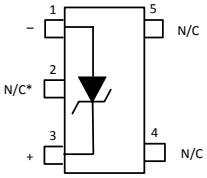


5 Pin Configuration and Functions

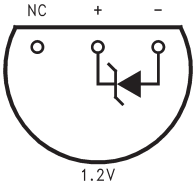
DBZ Package
3-Pin SOT-23
Top View



DCK Package
5-Pin SC70
Top View



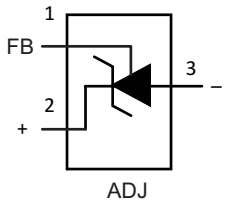
LP Package
3-Pin TO-92
Top View



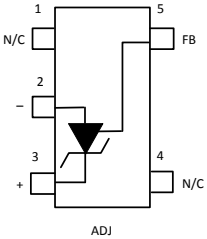
Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOT-23	SC70	TO-92		
Anode	2	1	1	O	Anode pin, normally grounded
Cathode	1	3	2	I/O	Shunt current and output voltage
FB	—	—	—	I	Feedback pin for adjustable output voltage
NC**	3	2	—	—	**Must float or connect to anode
NC	—	4, 5	3	—	No connect

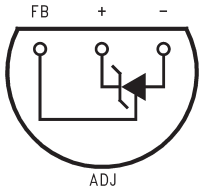
DBZ Package
3-Pin SOT-23
Top View



DCK Package
5-Pin SC70
Top View



LP Pakage
3-Pin TO-92
Bottom View



Pin Functions: ADJ Pinouts

PIN				I/O	DESCRIPTION
NAME	SOT-23	SC70	TO-92		
Anode	3	2	1	O	Anode pin, normally grounded
Cathode	2	3	2	I/O	Shunt current and output voltage
FB	1	5	3	I	Feedback pin for adjustable output voltage
NC**	—	—	—	—	**Must float or connect to anode
NC	—	1, 4	—	—	No connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Reverse current				20	mA
Forward current				10	mA
Maximum output voltage (LM4041-N ADJ, LM4041-N-Q1 ADJ)				15	V
Power dissipation (T_A = 25°C)(3)		DBZ package		306	mW
		LP package		550	mW
		DCK package		241	mW
Lead temperature	DBZ packages	Vapor phase (60 seconds)		215	°C
		Infrared (15 seconds)		220	°C
	LP package	Soldering (10 seconds)		260	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/R_{\theta JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower. For the LM4041-N, T_{Jmax} = 125°C, and the typical thermal resistance ($R_{\theta JA}$), when board mounted, is 326°C/W for the SOT-23 package, 415°C/W for the SC70 package and 180°C/W with 0.4-in lead length and 170°C/W with 0.125-in lead length for the TO-92 package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±200	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin. All pins are rated at 2 kV for human-body model, but the feedback pin which is rated at 1 kV.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

See (1)

		MIN	NOM	MAX	UNIT
Temperature		T_{min}	T_A	T_{max}	°C
Industrial temperature		–40	T_A	85	°C
Extended temperature		–40	T_A	125	°C
Reverse current	LM4041-N 1.2, LM4041-N-Q1 1.2	60		1200	µA
	LM4041-N ADJ, LM4041-N-Q1 ADJ	60		1200	µA
Output voltage	LM4041-N ADJ, LM4041-N-Q1 ADJ	1.24		10	V

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

6.4 Thermal Information

THERMAL METRIC (1)		LM4041-N		LM4041-N, LM4041-N-Q1	UNIT
		SC70	TO-92	SOT-23	
		5 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	265.3	161.5	291.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.1	84.5	114.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	—	62.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	28.4	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.9	140.6	61	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 LM4041-N-xx 1.2 Electrical Characteristics (Industrial Temperature Range)

All limits $T_A = T_J = 25°C$ for the LM4041xAIM3, LM4041xBIM3, LM4041AIZ, LM4041BIZ and LM4041BIM7 devices, unless otherwise specified. The grades A and B designate initial reverse breakdown voltage tolerances of ±0.1% and ±0.2%, respectively.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_R	Reverse breakdown voltage	I_R = 100 µA			1.225		V
	Reverse breakdown voltage tolerance(3)	I_R = 100 µA	LM4041AIM3, LM4041QAIM3 LM4041AIM3, LM4041AIZ			±1.2	mV
			LM4041BIM3, LM4041QBIM3 LM4041BIZ, LM4041BIM7			±2.4	
		$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041AIM3, LM4041QAIM3 LM4041AIM3, LM4041AIZ			±9.2	
			LM4041BIM3, LM4041QBIM3 LM4041BIZ, LM4041BIM7			±10.4	
I_{RMIN}	Minimum operating current	$T_A = T_J = 25°C$			45	60	µA
		$T_A = T_J = T_{MIN}$ to T_{MAX}				65	
$\Delta V_R/\Delta T$	Average reverse breakdown voltage temperature Coefficient(3)	I_R= 10 mA			±20		ppm/°C
		I_R = 1 mA	$T_A = T_J = 25°C$		±15		
			$T_A = T_J = T_{MIN}$ to T_{MAX}			±100	
		I_R = 100 µA			±15		
$\Delta V_R/\Delta I_R$	Reverse breakdown voltage change with operating current change(4)	$I_{RMIN} \le I_R \le 1$ mA	$T_A = T_J = 25°C$		0.7	1.5	mV
			$T_A = T_J = T_{MIN}$ to T_{MAX}			2	
		1 mA ≤ I_R ≤ 12 mA	$T_A = T_J = 25°C$		4	6	
			$T_A = T_J = T_{MIN}$ to T_{MAX}			8	
Z_R	Reverse dynamic impedance	I_R = 1 mA, f = 120 Hz, I_{AC}= 0.1 I_R			0.5	1.5	Ω
e_N	Wideband noise	I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz			20		μV_{rms}
ΔV_R	Reverse breakdown voltage long-term stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 µA			120		ppm
V_{HYST}	Thermal hysteresis(5)	ΔT = −40°C to +125°C			0.08%		

(1) Limits are 100% production tested at 25°C. Limits over temperature are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate AOQL.

(2) Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

(3) The overtemperature limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ±[(ΔV_R↱ΔT)(V_R)]. Where, $\Delta V_R/\Delta T$ is the V_R temperature coefficient, maxΔT is the maximum difference in temperature from the reference point of 25 °C to T_{MAX} or T_{MIN}, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades in the industrial temperature range where maxΔT = 65°C is shown below:
A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±2.0% ±150 ppm/°C × 65°C
The total over-temperature tolerance for the different grades in the extended temperature range where max ΔT = 100 °C is shown below:
B-grade: ±1.2% = ±0.2% ±100 ppm/°C × 100°C
C-grade: ±1.5% = ±0.5% ±100 ppm/°C × 100°C
D-grade: ±2.5% = ±1.0% ±150 ppm/°C × 100°C
E-grade: ±4.5% = ±2.0% ±150 ppm/°C × 100°C
Therefore, as an example, the A-grade LM4041-N 1.2 has an over-temperature Reverse Breakdown Voltage tolerance of ±1.2 V × 0.75% = ±9.2 mV.

(4) Load regulation is measured on pulse basis from no load to the specified load current. Output changes due to die temperature change must be taken into account separately.

(5) Thermal hysteresis is defined as the difference in voltage measured at +25°C after cycling to temperature –40°C and the +25°C measurement after cycling to temperature +125°C.

6.6 LM4041-N-xx 1.2 Electrical Characteristics (Industrial Temperature Range)

All limits $T_A = T_J = 25°C$. unless otherwise specified. The grades C, D, and E designate initial reverse breakdown voltage tolerances of ±0.5%, ±1.0%, and ±2.0%, respectively.

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(2)	MAX(1)	UNIT
V_R	Reverse Breakdown Voltage	I_R = 100 µA				1.225		V
V_R	Reverse breakdown voltage tolerance(3)	I_R = 100 µA	$T_A = T_J = 25°C$	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			±6	mV
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			±12	
				LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			±25	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			±14	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			±24	
				LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			±36	
I_{RMIN}	Minimum operating current	$T_A = T_J = 25°C$		LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		45	60	µA
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			65	
		$T_A = T_J = T_{MIN}$ to T_{MAX}		LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			65	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			70	
$\Delta V_R/\Delta T$	V_R Temperature coefficient(3)	I_R = 10 mA				±20		ppm/°C
		I_R = 1 mA	$T_A = T_J = 25°C$			±15		
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			±100	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			±150	
		I_R= 100 µA				±15		

(1) Limits are 100% production tested at 25°C. Limits over temperature are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate AOQL.

(2) Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

(3) The overtemperature limit for reverse breakdown voltage tolerance is defined as the room temperature reverse breakdown voltage tolerance ±[(ΔV_R↱ΔT)(max ΔT)(V_R)]. Where, $\Delta V_R/\Delta T$ is the V_R temperature coefficient, maxΔT is the maximum difference in temperature from the reference point of 25 °C to T_{MAX} or T_{MIN}, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades in the industrial temperature range where maxΔT = 65°C is shown below:
A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±2.0% ±150 ppm/°C × 65°C
The total over-temperature tolerance for the different grades in the extended temperature range where max ΔT = 100 °C is shown below:
B-grade: ±1.2% = ±0.2% ±100 ppm/°C × 100°C
C-grade: ±1.5% = ±0.5% ±100 ppm/°C × 100°C
D-grade: ±2.5% = ±1.0% ±150 ppm/°C × 100°C
E-grade: ±4.5% = ±2.0% ±150 ppm/°C × 100°C
Therefore, as an example, the A-grade LM4041-N 1.2 has an over-temperature reverse breakdown voltage tolerance of ±1.2 V × 0.75% = ±9.2 mV.

LM4041-N-xx 1.2 Electrical Characteristics (Industrial Temperature Range) (continued)

All limits $T_A = T_J = 25°C$. unless otherwise specified. The grades C, D, and E designate initial reverse breakdown voltage tolerances of ±0.5%, ±1.0%, and ±2.0%, respectively.

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(2)	MAX(1)	UNIT
$\Delta V_R/\Delta I_R$	Reverse breakdown voltage change with operating current change(4)	$I_{RMIN} \le I_R \le 1$ mA	$T_A = T_J = 25°C$	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		0.7	1.5	mV
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 (LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			2	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			2	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7)			2.5	
		1 mA ≤ I_R ≤ 12 mA	$T_A = T_J = 25°C$	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		2.5	6	mV
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			8	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			8	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			10	
Z_R	Reverse dynamic impedance	I_R = 1 mA, f = 120 Hz I_{AC} = 0.1 I_R		LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		0.5	1.5	Ω
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7 LM4041EIM3, LM4041QEIM3, LM4041EIZ, LM4041EIM7			2	
e_N	Wideband noise	I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz				20		μV_{rms}
ΔV_R	Reverse breakdown voltage long-term stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 µA				120		ppm
V_{HYST}	Thermal hysteresis(5)	ΔT = −40°C to +125°C				0.08%		

(4) Load regulation is measured on pulse basis from no load to the specified load current. Ouput changes due to die temperature change must be taken into account separately.
(5) Thermal hysteresis is defined as the difference in voltage measured at +25°C after cycling to temperature –40°C and the +25°C measurement after cycling to temperature +125°C.

6.7 LM4041-N-xx 1.2 Electrical Characteristics (Extended Temperature Range)

All limits $T_A = T_J = 25°C$, unless otherwise specified. The grades C, D, and E designate initial reverse breakdown voltage tolerance of ±0.5%, ±1.0%, and ±2.0% respectively.

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(2)	MAX(1)	UNIT
V_R	Reverse breakdown voltage	I_R = 100 µA				1.225		V
V_R	Reverse breakdown voltage error(3)	I_R = 100 µA	$T_A = T_J = 25°C$	LM4041CEM3, LM4041QCEM3			±6	mV
				LM4041DEM3, LM4041QDEM3			±12	
				LM4041EEM3, LM4041QEEM3			±25	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3			±18.4	
				LM4041DEM3, LM4041QDEM3			±31	
				LM4041EEM3, LM4041QEEM3			±43	
I_{RMIN}	Minimum operating current	$T_A = T_J = 25°C$		LM4041CEM3, LM4041QCEM3		45	60	µA
				LM4041DEM3, LM4041QDEM3 LM4041EEM3, LM4041QEEM3			65	
		LM4041EEM3, LM4041QEEM3		LM4041CEM3, LM4041QCEM3			68	
				LM4041DEM3, LM4041QDEM3 LM4041EEM3, LM4041QEEM3			73	
$\Delta V_R/\Delta T$	VR temperature coefficient(3)	LM4041EEM3, LM4041QEEM3				±20		ppm/°C
		I_R = 1 mA	$T_A = T_J = 25°C$			±15		
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3			±100	
				LM4041DEM3, LM4041QDEM3 LM4041EEM3, LM4041QEEM3			±150	
		LM4041EEM3, LM4041QEEM3				±15		

(1) Limits are 100% production tested at 25°C. Limits over temperature are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate AOQL.
(2) Typicals are at T_J = 25°C and represent most likely parametric norm.
(3) The overtemperature limit for reverse breakdown voltage tolerance is defined as the room temperature reverse breakdown voltage tolerance ±[(ΔV_R↱ΔT)(max ΔT)(V_R)]. Where, $\Delta V_R/\Delta T$ is the V_R temperature coefficient, maxΔT is the maximum difference in temperature from the reference point of 25 °C to T_{MAX} or T_{MIN}, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades in the industrial temperature range where maxΔT = 65°C is shown below:
A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±2.0% ±150 ppm/°C × 65°C
The total over-temperature tolerance for the different grades in the extended temperature range where max ΔT = 100 °C is shown below:
B-grade: ±1.2% = ±0.2% ±100 ppm/°C × 100°C
C-grade: ±1.5% = ±0.5% ±100 ppm/°C × 100°C
D-grade: ±2.5% = ±1.0% ±150 ppm/°C × 100°C
E-grade: ±4.5% = ±2.0% ±150 ppm/°C × 100°C
Therefore, as an example, the A-grade LM4041-N 1.2 has an over-temperature reverse breakdown voltage tolerance of ±1.2 V × 0.75% = ±9.2 mV.

LM4041-N-xx 1.2 Electrical Characteristics (Extended Temperature Range) (continued)

All limits $T_A = T_J = 25°C$, unless otherwise specified. The grades C, D, and E designate initial reverse breakdown voltage tolerance of ±0.5%, ±1.0%, and ±2.0% respectively.

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(2)	MAX(1)	UNIT
$\Delta V_R/\Delta I_R$	Reverse breakdown change with current(4)	$I_{RMIN} \le I_R \le 1.0$ mA	$T_A = T_J = 25°C$	LM4041CEM3, LM4041QCEM3		0.7	1.5	mV
				LM4041DEM3, LM4041QDEM3 LM4041EEM3, LM4041QEEM3			2	
			LM4041EEM3, LM4041QEEM3	LM4041CEM3, LM4041QCEM3			2	
				LM4041DEM3, LM4041QDEM3 M4041EEM3, LM4041QEEM3			2.5	
		1 mA ≤ I_R ≤ 12 mA	LM4041EEM3, LM4041QEEM3	LM4041CEM3, LM4041QCEM3		2.5	6	mV
				LM4041DEM3, LM4041QDEM3 LM4041EEM3, LM4041QEEM3			8	
			LM4041EEM3, LM4041QEEM3	LM4041CEM3, LM4041QCEM3			8	
				LM4041DEM3, LM4041QDEM3 LM4041EEM3, LM4041QEEM3			10	
Z_R	Reverse dynamic impedance	I_R = 1 mA, f = 120 Hz, I_{AC}= 0.1 I_R	$T_A = T_J = 25°C$			0.5		Ω
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3			1.5	
				LM4041DEM3, LM4041QDEM3 LM4041EEM3, LM4041QEEM3			2	
e_N	Noise voltage	I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz				20		μV_{rms}
ΔV_R	Long-term stability (non-cumulative)	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 µA				120		ppm
V_{HYST}	Thermal hysteresis(5)	ΔT = −40°C to +125°C				0.08%		

(4) Load regulation is measured on pulse basis from no load to the specified load current. Ouput changes due to die temperature change must be taken into account separately.
(5) Thermal hysteresis is defined as the difference in voltage measured at +25°C after cycling to temperature –40°C and the +25°C measurement after cycling to temperature +125°C.

6.8 LM4041-N-xx ADJ (Adjustable) Electrical Characteristics (Industrial Temperature Range)

All limits T_J = 25°C, unless otherwise specified (SOT-23, see(1)),
$I_{RMIN} \le I_R \le 12$ mA, $V_{REF} \le V_{OUT} \le 10$ V. The grades C and D designate initial Reference Voltage Tolerances of ±0.5% and ±1%, respectively for V_{OUT} = 5 V.

PARAMETER		TEST CONDITIONS			MIN(2)	TYP(3)	MAX(2)	UNIT
V_{REF}	Reference voltage	I_R = 100 µA, V_{OUT} = 5 V				1.233		V
	Reference voltage tolerance(4)	I_R = 100 µA, V_{OUT} = 5 V	T_J = 25°C	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			±6.2	mV
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			±12	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			±14	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			±24	
I_{RMIN}	Minimum operating current	T_J = 25°C		LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		45	60	µA
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			65	
		$T_A = T_J = T_{MIN}$ to T_{MAX}		LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			65	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			70	
$\Delta V_{REF}/\Delta I_R$	Reference voltage change with operating current change(5)	$I_{RMIN} \le I_R \le 1$ mA SOT-23: $V_{OUT} \ge 1.6$ V(1)	T_J = 25°C	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		0.7	1.5	mV
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			2	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			2	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			2.5	
		1 mA ≤ I_R ≤ 12 mA SOT-23: $V_{OUT} \ge 1.6$ V(1)	T_J = 25°C	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		2	4	mV
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			6	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			6	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			8	
$\Delta V_{REF}/\Delta V_O$	Reference voltage change with output voltage change	I_R = 1 mA	T_J = 25°C	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		–1.55	–2	mV/V
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			–2.5	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			–2.5	
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			–3	
I_{FB}	Feedback current	T_J = 25°C		LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7		60	100	nA
				LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			150	
		$T_A = T_J = T_{MIN}$ to T_{MAX}					120	

(1) When $V_{OUT} \le 1.6$ V, the LM4041-N ADJ in the SOT-23 package must operate at reduced I_R. This is caused by the series resistance of the die attach between the die (–) output and the package (–) output pin. See the *Output Saturation (SOT-23 only)* curve in the *Typical Characteristics* section.
(2) Limits are 100% production tested at 25°C. Limits over temperature are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate AOQL.
(3) Typicals are at T_J = 25°C and represent most likely parametric norm.
(4) Reference voltage and temperature coefficient will change with output voltage. See *Typical Characteristics* curves.
(5) Load regulation is measured on pulse basis from no load to the specified load current. Ouput changes due to die temperature change must be taken into account separately.

LM4041-N-xx ADJ (Adjustable) Electrical Characteristics (Industrial Temperature Range) (continued)

All limits T_J = 25°C, unless otherwise specified (SOT-23, see(1)),
$I_{RMIN} \le I_R \le 12$ mA, $V_{REF} \le V_{OUT} \le 10$ V. The grades C and D designate initial Reference Voltage Tolerances of ±0.5% and ±1%, respectively for V_{OUT} = 5 V.

PARAMETER		TEST CONDITIONS				MIN(2)	TYP(3)	MAX(2)	UNIT
$\Delta V_{REF}/\Delta T$	Average reference voltage temperature coefficient(4)	V_{OUT} = 5 V	I_R = 10 mA				20		ppm/°C
			I_R = 1 mA	T_J = 25°C			15		
				$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CIM3, LM4041QCIM3, LM4041CIZ, LM4041CIM7			±100	
					LM4041DIM3, LM4041QDIM3, LM4041DIZ, LM4041DIM7			±150	
			I_R = 100 µA				15		
Z_{OUT}	Dynamic output impedance	I_R = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_R					0.3		Ω
		$V_{OUT} = V_{REF}$ V_{OUT} = 10 V					2		
e_N	Wideband noise	$V_{OUT} = V_{REF}$ I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz					20		μV_{rms}
ΔV_{REF}	Reference voltage long-term stability	t = 1000 hrs, I_R = 100 µA, T = 25°C ±0.1°C					120		ppm
V_{HYST}	Thermal hysteresis(6)	ΔT = −40°C to +125°C					0.08%		

(6) Thermal hysteresis is defined as the difference in voltage measured at +25°C after cycling to temperature –40°C and the +25°C measurement after cycling to temperature +125°C.

6.9 LM4041-N-xx ADJ (Adjustable) Electrical Characteristics (Extended Temperature Range)

All limits T_J = 25°C, unless otherwise specified (SOT-23, see(1)), $I_{RMIN} \le I_R \le 12$ mA, $V_{REF} \le V_{OUT} \le 10$ V. The grades C and D designate initial Reference Voltage Tolerances of ±0.5% and ±1%, respectively for V_{OUT} = 5 V.

PARAMETER		TEST CONDITIONS				MIN(2)	TYP(3)	MAX(2)	UNIT
V_{REF}	Reference voltage	I_R = 100 µA, V_{OUT} = 5 V					1.233		V
	Reference voltage tolerance(4)	I_R = 100 µA, V_{OUT} = 5 V	T_J = 25°C	LM4041CEM3, LM4041QCEM3				±6.2	mV
				LM4041DEM3, LM4041QDEM3				±12	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3				±18	
				LM4041DEM3, LM4041QDEM3				±30	
I_{RMIN}	Minimum operating current	T_J = 25°C		LM4041CEM3, LM4041QCEM3			45	60	µA
				LM4041DEM3, LM4041QDEM3				65	
		$T_A = T_J = T_{MIN}$ to T_{MAX}		LM4041CEM3, LM4041QCEM3				68	
				LM4041DEM3, LM4041QDEM3				73	
$\Delta V_{REF}/\Delta I_R$	Reference voltage change with operating current change(5)	$I_{RMIN} \le I_R \le 1$ mA SOT-23: $V_{OUT} \ge 1.6$ V(1)	T_J = 25°C	LM4041CEM3, LM4041QCEM3			0.7	1.5	mV
				LM4041DEM3, LM4041QDEM3				2	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3				2	
				LM4041DEM3, LM4041QDEM3				2.5	
		1 mA ≤ I_R ≤ 12 mA SOT-23: $V_{OUT} \ge 1.6$ V(1)	T_J = 25°C	LM4041CEM3, LM4041QCEM3			2	8	mV
				LM4041DEM3, LM4041QDEM3				10	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3				6	
				LM4041DEM3, LM4041QDEM3				8	
$\Delta V_{REF}/\Delta V_O$	Reference voltage change with output voltage change	I_R = 1 mA	T_J = 25°C	LM4041CEM3, LM4041QCEM3			–1.55	–2	mV/V
				LM4041DEM3, LM4041QDEM3				–2.5	
			$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3				–3	
				LM4041DEM3, LM4041QDEM3				–4	
I_{FB}	Feedback current	T_J = 25°C		LM4041CEM3, LM4041QCEM3			60	100	nA
				LM4041DEM3, LM4041QDEM3				150	
		$T_A = T_J = T_{MIN}$ to T_{MAX}		LM4041CEM3, LM4041QCEM3				120	
				LM4041DEM3, LM4041QDEM3				200	
$\Delta V_{REF}/\Delta T$	Average reference voltage temperature coefficient(4)	V_{OUT} = 5 V,	I_R = 10 mA				20		ppm/°C
			I_R = 1 mA	T_J = 25°C			15		
				$T_A = T_J = T_{MIN}$ to T_{MAX}	LM4041CEM3, LM4041QCEM3			±100	
					LM4041DEM3, LM4041QDEM3			±150	
			I_R = 100 µA				15		
Z_{OUT}	Dynamic output impedance	I_R = 1 mA, f = 120 Hz,					0.3		Ω
		I_{AC} = 0.1 I_R							
			$V_{OUT} = V_{REF}$						
			V_{OUT} = 10 V				2		
e_N	Wideband noise	I_R = 100 µA,	$V_{OUT} = V_{REF}$				20		μV_{rms}
		10 Hz ≤ f ≤ 10 kHz							
ΔV_{REF}	Reference voltage long-term stability	t = 1000 hrs, I_R = 100 µA, T = 25°C ±0.1°C					120		ppm
V_{HYST}	Thermal hysteresis(6)	ΔT = −40°C to +125°C					0.08%		

(1) When $V_{OUT} \le 1.6$ V, the LM4041-N ADJ in the SOT-23 package must operate at reduced I_R. This is caused by the series resistance of the die attach between the die (–) output and the package (–) output pin. See the *Output Saturation (SOT-23 only)* curve in the *Typical Characteristics* section.
(2) Limits are 100% production tested at 25°C. Limits over temperature are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate AOQL.
(3) Typicals are at T_J = 25°C and represent most likely parametric norm.
(4) Reference voltage and temperature coefficient will change with output voltage. See *Typical Characteristics* curves.
(5) Load regulation is measured on pulse basis from no load to the specified load current. Ouput changes due to die temperature change must be taken into account separately.
(6) Thermal hysteresis is defined as the difference in voltage measured at +25°C after cycling to temperature –40°C and the +25°C measurement after cycling to temperature +125°C.

6.10 Typical Characteristics

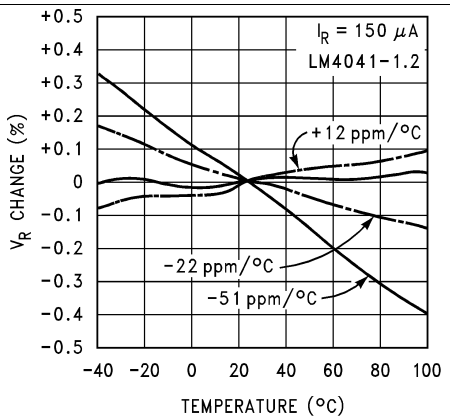


Figure 1. Temperature Drift for Different Average Temperature Coefficient

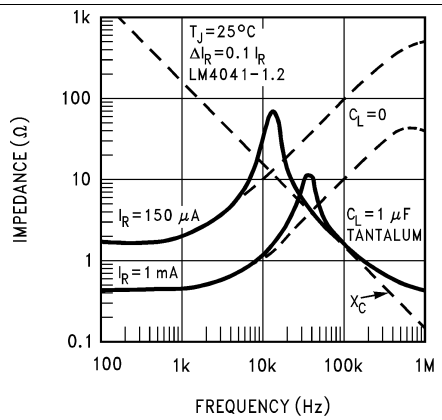


Figure 2. Output Impedance vs Frequency

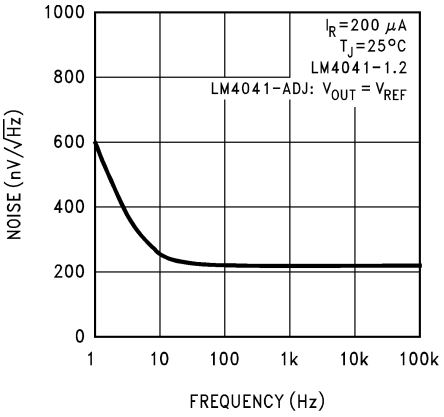


Figure 3. Noise Voltage

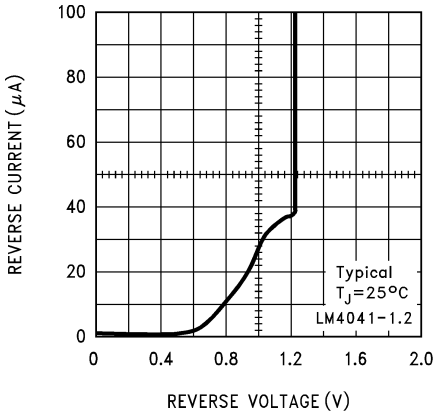


Figure 4. Reverse Characteristics and Minimum Operating Current

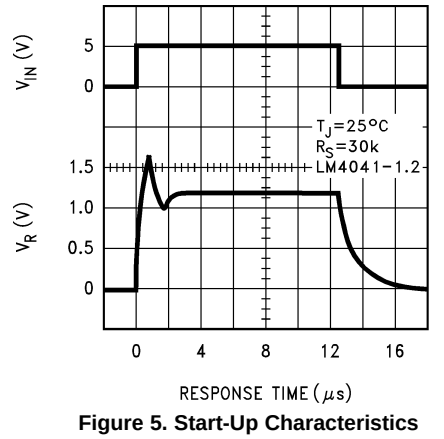


Figure 5. Start-Up Characteristics

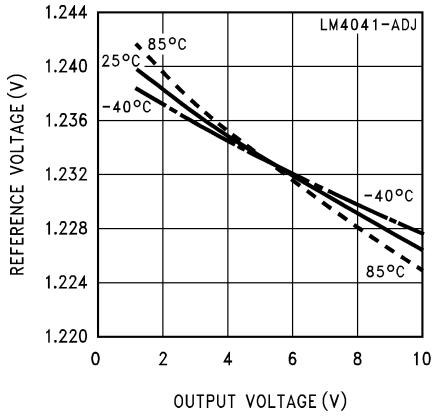


Figure 6. Reference Voltage vs Output Voltage and Temperature

Typical Characteristics (continued)

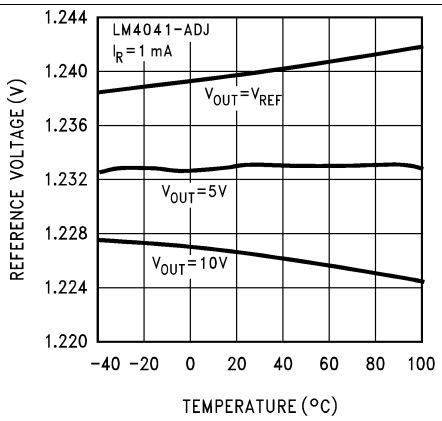


Figure 7. Reference Voltage vs Temperature and Output Voltage

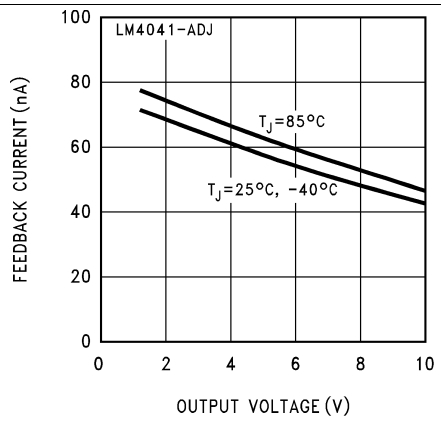


Figure 8. Feedback Current vs Output Voltage and Temperature

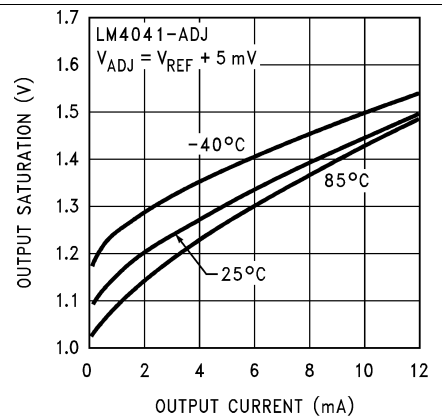


Figure 9. Output Saturation (SOT-23 Only)

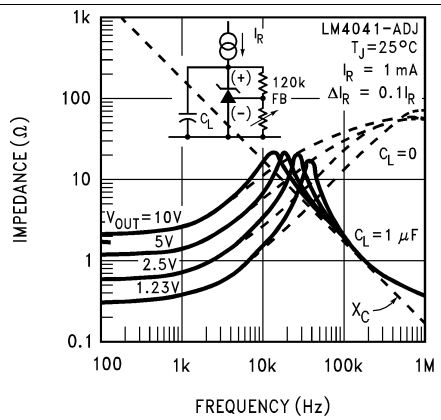


Figure 10. Output Impedance vs Frequency

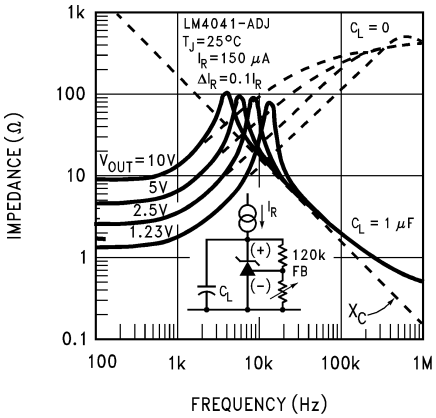


Figure 11. Output Impedance vs Frequency

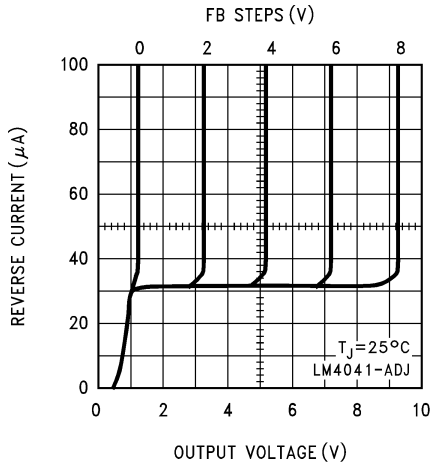


Figure 12. Reverse Characteristics

7 Parameter Measurement Information

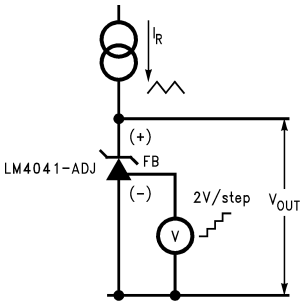


Figure 14. Adjustable Output Test Circuit

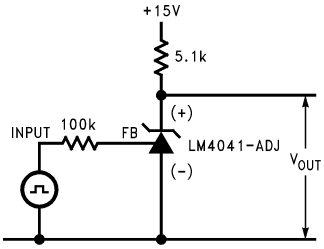


Figure 15. Line Transient Test Circuit

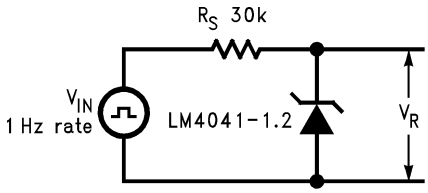


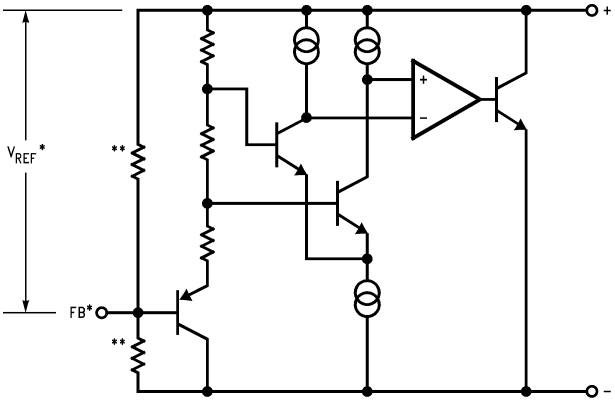
Figure 16. Start-Up and Shutdown Test Circuit

8 Detailed Description

8.1 Overview

The LM4041 is a precision micro-power shunt voltage reference available in both a fixed and output voltage and adjustable output voltage options. The part has three different packages available to meet small footprint requirements. It is also available in five different tolerance grades.

8.2 Functional Block Diagram



*LM4041-N ADJ only
**LM4041-N 1.2 only

8.3 Feature Description

The LM4041 is effectively a precision Zener diode. The part requires a small quiescent current for regulation, and regulates the output voltage by shunting more or less current to ground, depending on input voltage and load. The only external component requirement is a resistor between the cathode and the input voltage to set the input current. An external capacitor can be used on the input or output, but is not required.

Typical Applications (continued)

9.2.1.3 Application Curve

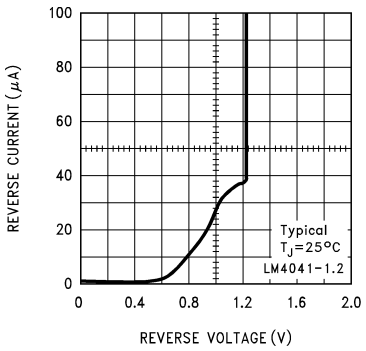
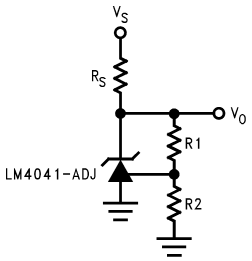


Figure 18. Reverse Characteristics and Minimum Operating Current

9.2.2 Adjustable Shunt Regulator



$V_O = V_{REF}[(R2/R1) + 1]$

Figure 19. Adjustable Shunt Regulator

9.2.2.1 Design Requirements

$V_{IN} > V_{OUT}$

V_{OUT} = 2.5 V

Select R_S with Equation 7.

$I_{RMIN} < L_R < I_{RMAX}$

where

- I_{RMAX} = 15 mA (7)

See the electrical characteristics tables in the *Specifications* for minimum operating current for each voltage option and grade.

9.2.2.2 Detail Design Procedure

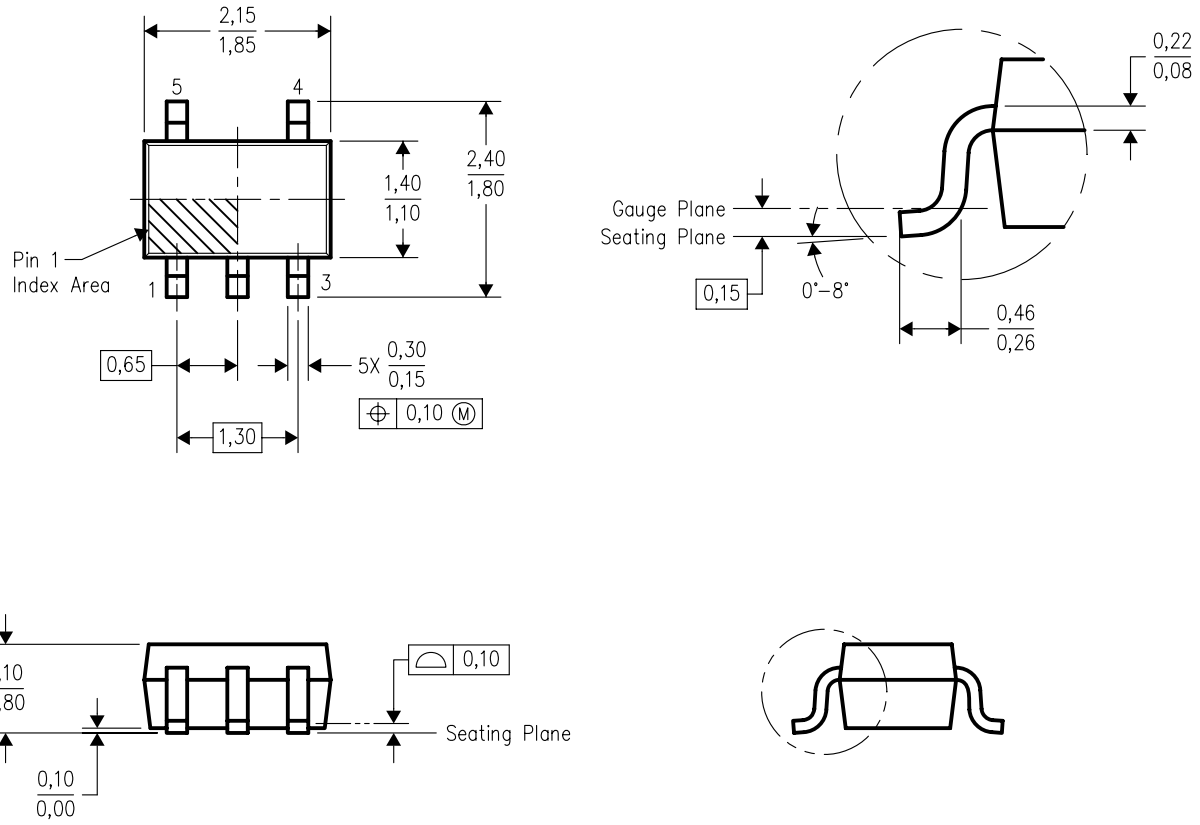
Select a value of R_S based on the same method shown in *Detailed Design Procedure*.

Set feedback resistors R_1 and R_2 for a resistor divider on the equation shown in *Application Information* that is reproduced here as Equation 8.

$V_{OUT} + V_{REF} \times ((R_2/R_1)+1)$ (8)

So, for a 2.5-V reference, of V_{REF} is 1.24 V, then R_2/R_1 = 1.01. Select R_2= 1.01 kΩ and R_1= 1.0 kΩ.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

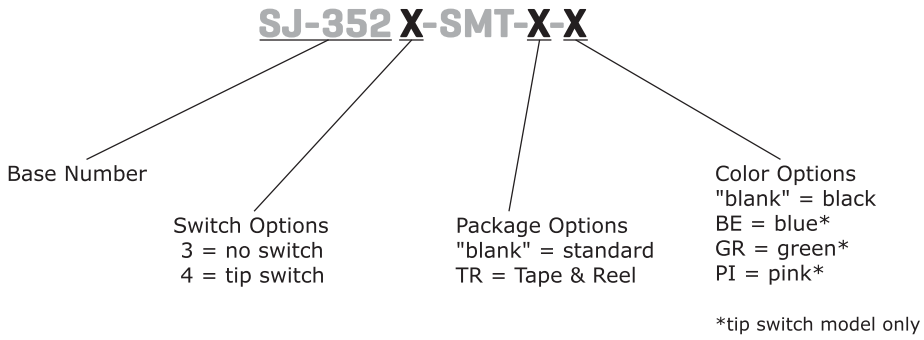
CUI INC®

SERIES: SJ-352X-SMT | DESCRIPTION: 3.5 MM AUDIO JACKS

FEATURES
- low profile design
- switch options include:
  - no switch
  - tip switch

RoHS

PART NUMBER KEY



SPECIFICATIONS

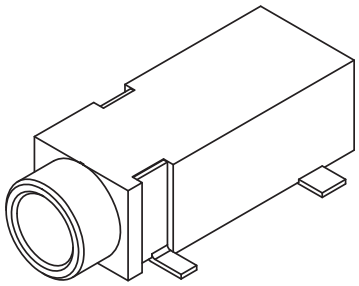
parameter	conditions/description	min	typ	max	units
rated input voltage			12		Vdc
rated input current				1	A
contact resistance	between terminal and mating plug between terminal in a closed circuit[1]			50 30	mΩ mΩ
insulation resistance	at 500 Vdc	100			MΩ
voltage withstand	at 50/60Hz for 1 minute			500	Vac
insertion/withdrawl force		0.3		3	kg
terminal strength	any direction for 10 seconds			500	g
operating temperature		-25		85	°C
life			5,000		cycles

Notes: 1. When measured at a current of less than 100 mA / 1 kHz

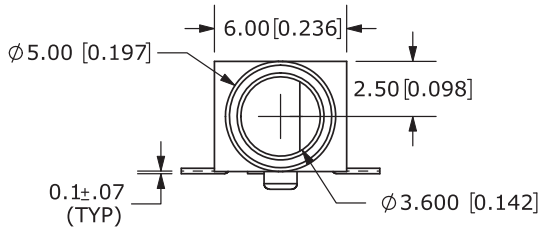
MECHANICAL DRAWING

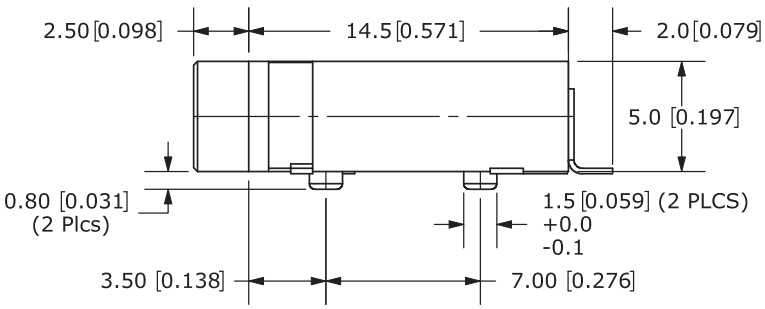
units: mm[inches]

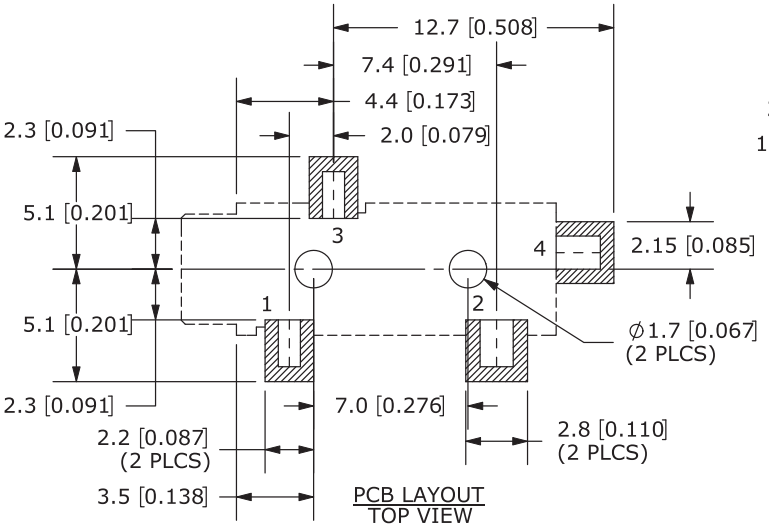
TOLERANCE:
X.X ±0.2mm
X.XX ±0.1mm
X.XXX ±0.05mm

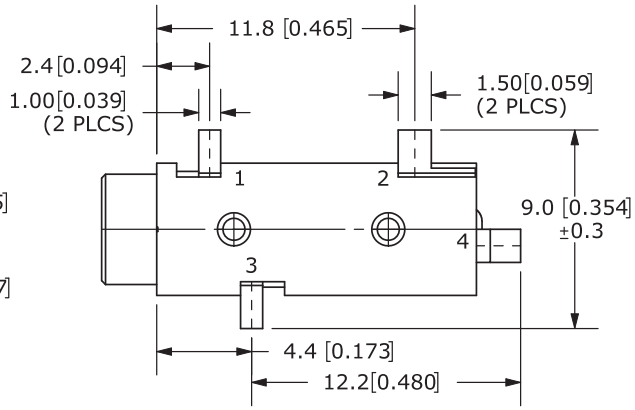


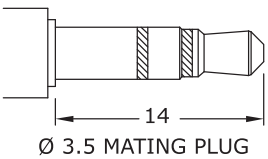
	MATERIAL	PLATING
terminal 1	copper alloy	silver
terminal 2	copper alloy	silver
terminal 3	copper alloy	silver
terminal 10	brass	silver
plastic	PA6T	

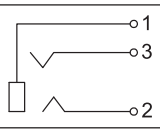
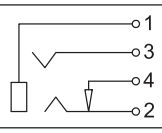










Model No.	SJ-3523-SMT	SJ-3524-SMT
Schematic		
PIN		
1	sleeve	sleeve
2	tip	tip
3	ring	ring
4	NP	tip switch

2.5 V/3.3 V, 2:1 Multiplexer/ Demultiplexer Bus Switch

ADG3248

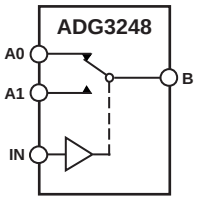
FEATURES

- 225 ps propagation delay through the switch
- 4.5 Ω switch connection between ports
- Data rate 1.244 Gbps
- 2.5 V/3.3 V supply operation
- Level translation
  - 3.3 V to 2.5 V
  - 2.5 V to 1.8 V
- Small signal bandwidth 610 MHz
- 6-lead SC70 package

APPLICATIONS

- 3.3 V to 2.5 V voltage translation
- 2.5 V to 1.8 V voltage translation
- Bus switching
- Docking stations
- Memory switching
- Analog switch applications

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. SWITCHES SHOWN FOR A LOGIC 0 INPUT

04404-001

Figure 1.

GENERAL DESCRIPTION

The ADG3248 is a 2.5 V or 3.3 V, high performance 2:1 multiplexer/demultiplexer. It is designed on a low voltage CMOS process, which provides low power dissipation yet gives high switching speed and very low on resistance. The low on resistance allows the input to be connected to the output without additional propagation delay or generating additional ground bounce noise.

Each switch of the ADG3248 conducts equally well in both directions when on. The ADG3248 exhibits break-before-make switching action, preventing momentary shorting when switching channels.

The ADG3248 is available in a tiny 6-lead SC70 package.

Table 1. ADG3248 Truth Table

IN Pin Logic Level	Function
Low (L)	B = A0
High (H)	B = A1

PRODUCT HIGHLIGHTS

1. 3.3 V or 2.5 V supply operation.
2. Extremely low propagation delay through switch.
3. 4.5 Ω switches connect inputs to outputs.
4. Tiny SC70 package.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

SPECIFICATIONS

V_{CC} = 2.3 V to 3.6 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Symbol	Conditions	B Version			Unit
			Min	Typ[2]	Max	
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}	V_{CC} = 2.7 V to 3.6 V	2.0			V
	V_{INH}	V_{CC} = 2.3 V to 2.7 V	1.7			V
Input Low Voltage	V_{INL}	V_{CC} = 2.7 V to 3.6 V			0.8	V
	V_{INL}	V_{CC} = 2.3 V to 2.7 V			0.7	V
Input Leakage Current	I_I			±0.01	±1	µA
Off State Leakage Current	I_{OZ}	0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
On State Leakage Current	I_{OL}	0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
Maximum Pass Voltage	V_P	V_A/V_B = V_{CC} = 3.3 V, I_O = −5 µA	2.0	2.5	2.9	V
		V_A/V_B = V_{CC} = 2.5 V, I_O= −5 µA	1.5	1.8	2.1	V
CAPACITANCE[3]						
A Port Off Capacitance	C_A Off	f = 1 MHz		3.5		pF
B Port Off Capacitance	C_B Off	f = 1 MHz		4.5		pF
A, B Port On Capacitance	C_A, C_B On	f = 1 MHz		8.5		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		4		pF
SWITCHING CHARACTERISTICS[3]						
Propagation Delay A to B or B to A, t_{PD}[4]	t_{PHL}, t_{PLH}	C_L = 50 pF, V_{CC} = 3 V			0.225	ns
Propagation Delay Matching[5]					5	ps
Transition Time	t_{TRANS}	R_L = 510 Ω, C_L = 50 pF		16	29	ns
Break-Before-Make Time	t_{BBM}	R_L = 510 Ω, C_L = 50 pF	5	10		ns
Maximum Data Rate		V_{CC} = 3.3 V; V_A/V_B = 2 V		1.244		Gbps
Channel Jitter		V_{CC} = 3.3 V; V_A/V_B = 2 V		45		ps p-p
DIGITAL SWITCH						
On Resistance	R_{ON}	V_{CC} = 3 V, V_A = 0 V, I_{BA} = 8 mA		4.5	8	Ω
		V_{CC} = 3 V, V_A = 1.7 V, I_{BA} = 8 mA		12	28	Ω
		V_{CC} = 2.3 V, V_A = 0 V, I_{BA} = 8 mA		5	9	Ω
		V_{CC} = 2.3 V, V_A = 1 V, I_{BA} = 8 mA		9	18	Ω
On-Resistance Matching	ΔR_{ON}	V_{CC} = 3 V, V_A = 0 V, I_A = 8 mA		0.1	0.5	Ω
POWER REQUIREMENTS						
V_{CC}			2.3		3.6	V
Quiescent Power Supply Current	I_{CC}	Digital inputs = 0 V or V_{CC}		0.01	1	µA

[1] Temperature range is as follows for B Version: −40°C to +85°C.
[2] Typical values are at 25°C, unless otherwise stated.
[3] Guaranteed by design, not subject to production test.
[4] The digital switch contributes no propagation delay other than the resistance-capacitance (RC) delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
[5] Propagation delay matching between channels is calculated from the on-resistance matching and load capacitance of 50 pF.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.5 V to +4.6 V
Digital Inputs to GND	−0.5 V to +4.6 V
DC Input Voltage	−0.5 V to +4.6 V
DC Output Current	25 mA per channel
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	332°C/W
Lead Soldering	
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C
Pb-Free Soldering	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

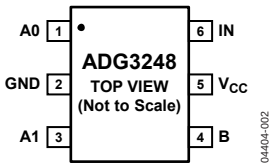


Figure 2. 6-Lead SC70

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Port A0, Input or Output.
2	GND	Ground Reference.
3	A1	Port A1, Input or Output.
4	B	Port B, Input or Output.
5	V_{CC}	Positive Power Supply Voltage.
6	IN	Channel Select.

TYPICAL PERFORMANCE CHARACTERISTICS

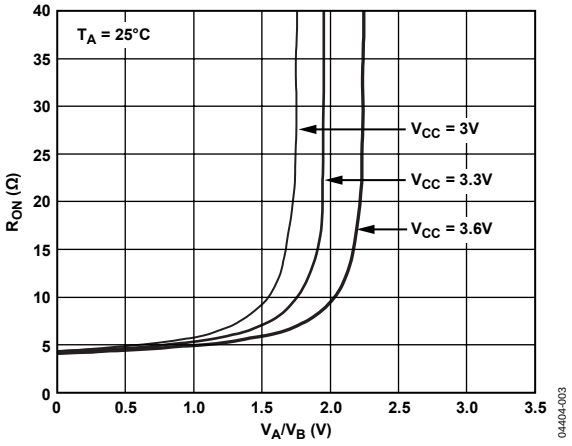


Figure 3. On Resistance vs. Input Voltage

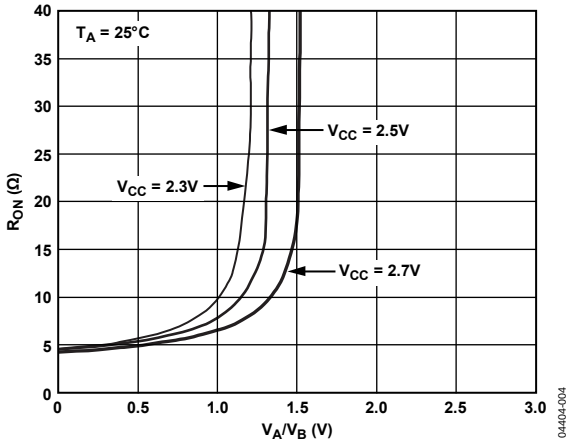


Figure 4. On Resistance vs. Input Voltage

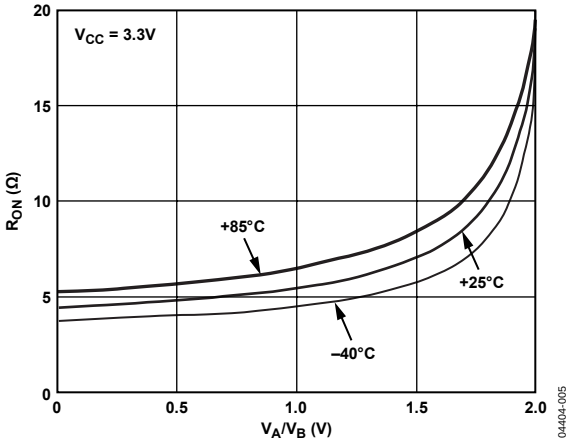


Figure 5. On Resistance vs. Input Voltage for Different Temperatures

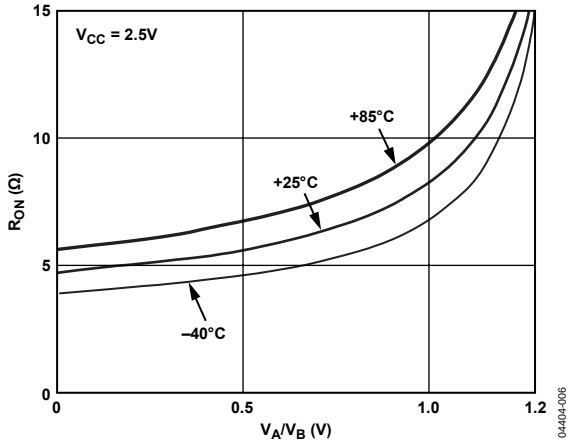


Figure 6. On Resistance vs. Input Voltage for Different Temperatures

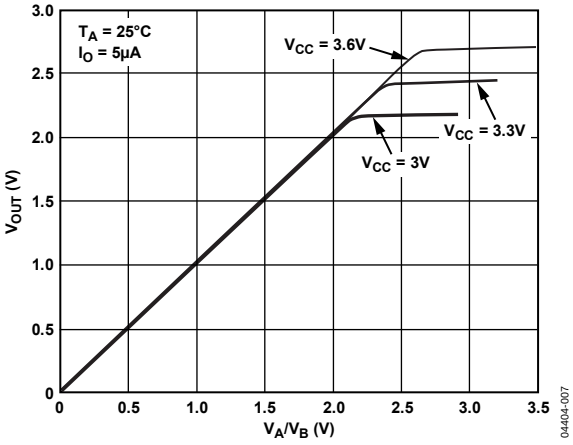


Figure 7. Pass Voltage vs. V_{CC}

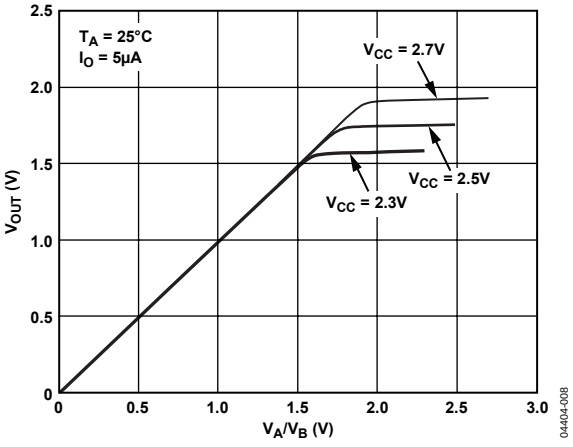


Figure 8. Pass Voltage vs. V_{CC}

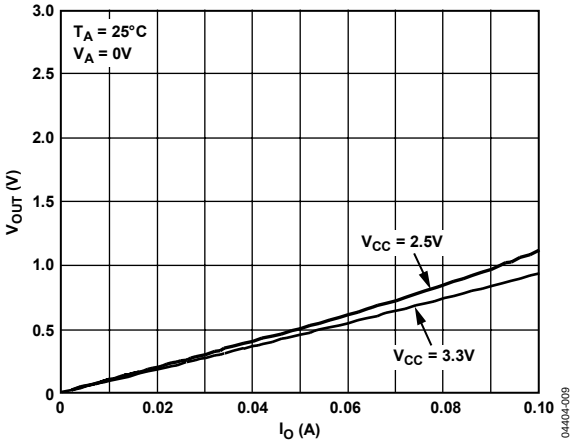


Figure 9. Output Low Characteristic

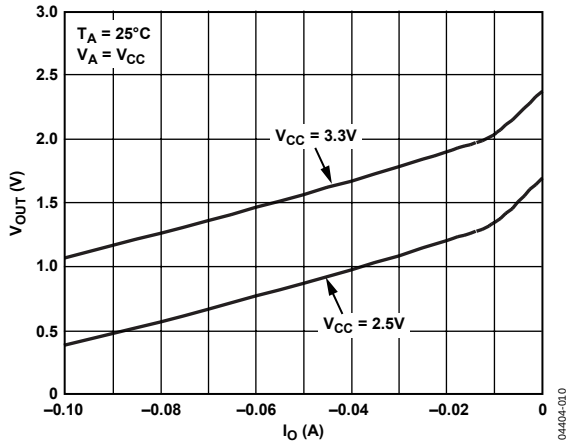


Figure 10. Output High Characteristic

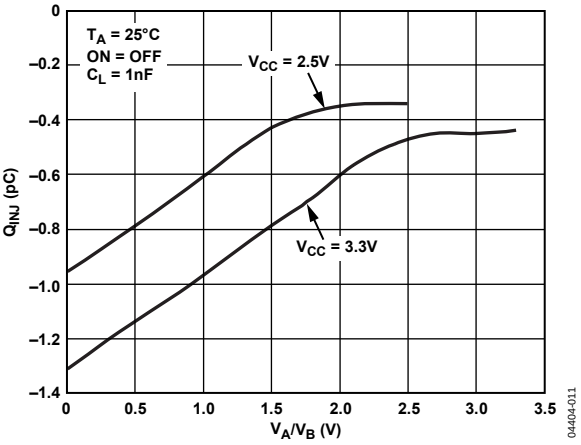


Figure 11. Charge Injection vs. Input Voltage

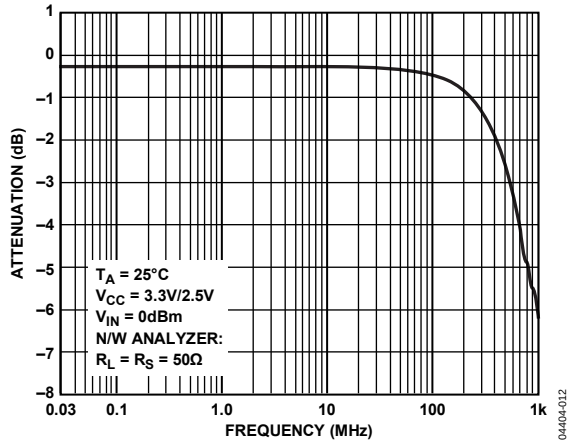


Figure 12. Bandwidth vs. Frequency

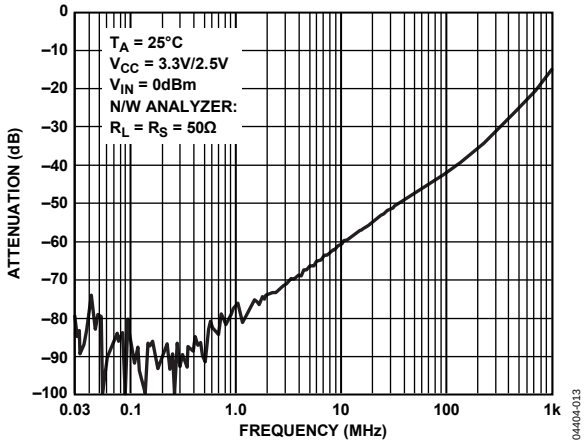


Figure 13. Crosstalk vs. Frequency

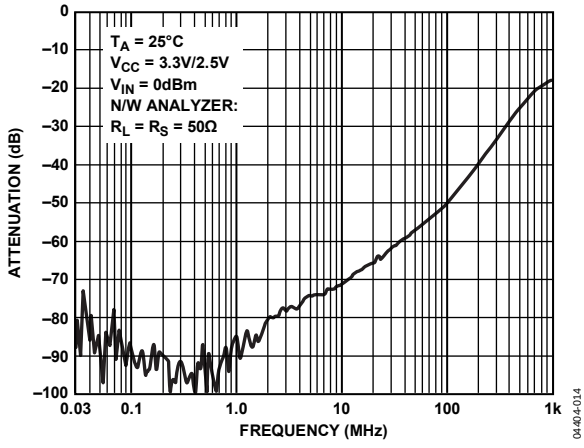


Figure 14. Off Isolation vs. Frequency

BUS SWITCH APPLICATIONS

MIXED VOLTAGE OPERATION, LEVEL TRANSLATION

Bus switches can provide an ideal solution for interfacing between mixed voltage systems. The ADG3248 is suitable for applications in which voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 2.5 V to 1.8 V or bidirectionally from 3.3 V directly to 2.5 V.

Figure 20 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs; therefore, placing the ADG3248 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

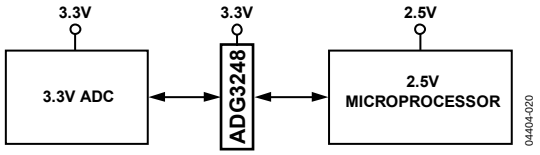


Figure 20. Level Translation Between a 3.3 V ADC and a 2.5 V Microprocessor

3.3 V to 2.5 V Translation

When V_{CC} is 3.3 V and the input signal range is 0 V to V_{CC}, the maximum output signal is clamped to within a voltage threshold below the V_{CC} supply.

In this case, the output is limited to 2.5 V, as shown in Figure 22. This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

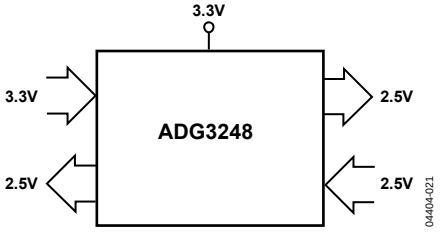


Figure 21. 3.3 V to 2.5 V Voltage Translation

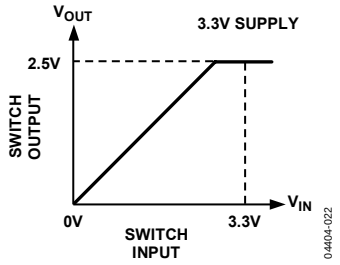


Figure 22. 3.3 V to 2.5 V Voltage Translation

2.5 V to 1.8 V Translation

When V_{CC} is 2.5 V and the input signal range is 0 V to V_{CC}, the maximum output signal is, as before, clamped to within a voltage threshold below the V_{CC} supply. In this case, the output is limited to approximately 1.8 V, as shown in Figure 24.

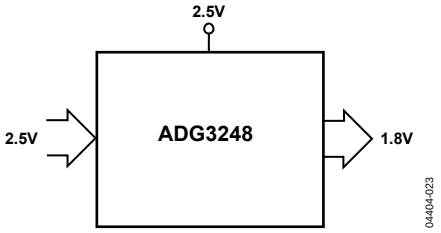


Figure 23. 2.5 V to 1.8 V Voltage Translation

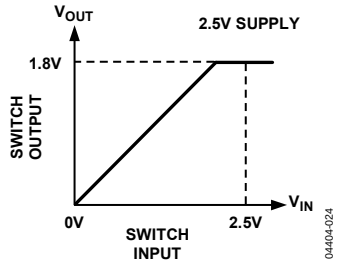


Figure 24. 2.5 V to 1.8 V Voltage Translation

ANALOG SWITCHING

Bus switches can be used in many analog switching applications, for example, video graphics. Bus switches can have lower on resistance, smaller on and off channel capacitance, and thus better frequency performance than their analog counterparts. The bus switch channel itself, consisting solely of an NMOS switch, limits the operating voltage (see Figure 3 for a typical plot) but, in many cases, this does not present an issue.

MULTIPLEXING

Many systems, such as docking stations and memory banks, have a large number of common bus signals. Common problems faced by designers of these systems include

- Large delays caused by capacitive loading of the bus
- Noise due to simultaneous switching of the address and data bus signals

Figure 25 shows an array of memory banks in which each address and data signal is loaded by the sum of the individual loads. If a bus switch is used as shown in Figure 26, the output load on the memory address and data bits is halved. The speed at which data from the selected bank can flow is much improved because the capacitance loading is halved and the switches introduce negligible propagation delay. Bus noise is also reduced.

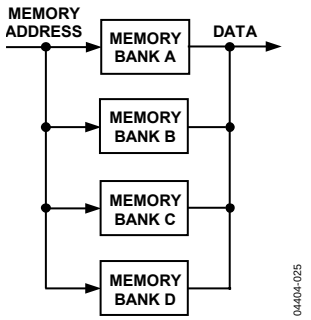


Figure 25. All Memory Banks Are Permanently Connected to the Bus

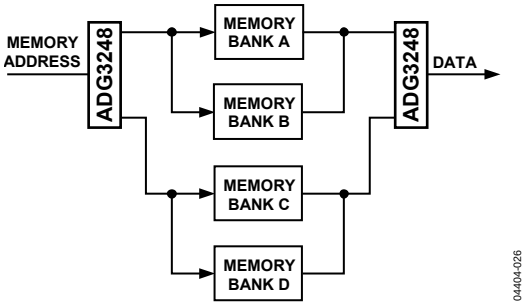


Figure 26. ADG3248 Used to Reduce Both Access Time and Noise

OUTLINE DIMENSIONS

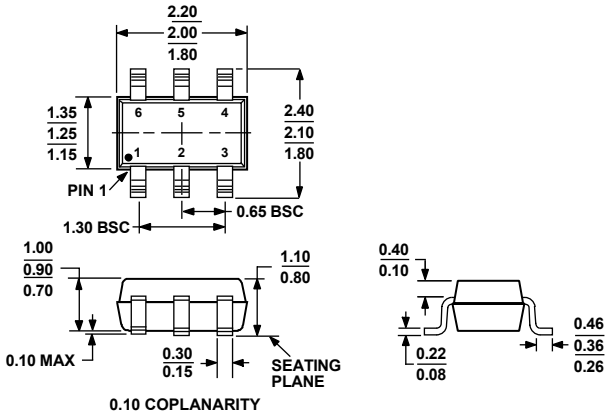


Figure 27. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG3248BKS-R2	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SMA
ADG3248BKS-REEL	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SMA
ADG3248BKS-REEL7	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SMA
ADG3248BKSZ-REEL7[1]	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	S1W

[1] Z = RoHS Compliant Part.

D04404-0-10/07(A)

SBOS215C – DECEMBER 2001 – REVISED APRIL 2005

Low-Power, Single-Supply, CMOS INSTRUMENTATION AMPLIFIERS

FEATURES

- DESIGNED FOR LOW COST
- HIGH GAIN ACCURACY: G = 5, 0.02%, 2ppm/°C
- GAIN SET WITH EXT. RESISTORS FOR > 5V/V
- LOW OFFSET VOLTAGE: ±250μV
- HIGH CMRR: 94dB DC, 50dB at 45kHz
- LOW BIAS CURRENT: 0.5pA
- BANDWIDTH, SLEW RATE: 2.0MHz, 5V/μs
- RAIL-TO-RAIL OUTPUT SWING: (V+) – 0.02V
- WIDE TEMPERATURE RANGE: –55°C to +125°C
- LOW QUIESCENT CURRENT: 490μA max/chan
- SHUT DOWN: 0.01μA
- MSOP-8 SINGLE AND TSSOP-14 DUAL PACKAGES

APPLICATIONS

- INDUSTRIAL SENSOR AMPLIFIERS: Bridge, RTD, Thermocouple, Position
- PHYSIOLOGICAL AMPLIFIERS: ECG, EEG, EMG
- A/D CONVERTER SIGNAL CONDITIONING
- DIFFERENTIAL LINE RECEIVERS WITH GAIN
- FIELD UTILITY METERS
- PCMCIA CARDS
- AUDIO AMPLIFIERS
- COMMUNICATION SYSTEMS
- TEST EQUIPMENT
- AUTOMOTIVE INSTRUMENTATION

DESCRIPTION

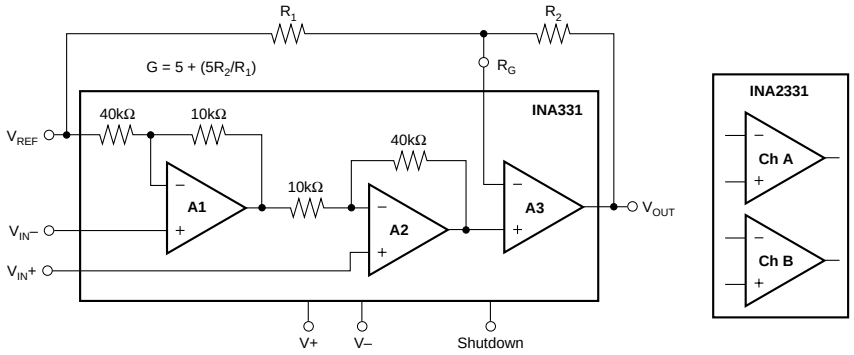
The INA331 and INA2331 are rail-to-rail output, low-power CMOS instrumentation amplifiers that offer wide range, single-supply operation as well as bipolar-supply operation. The INA331 family provides low-cost, low-noise amplification of differential signals with a low quiescent current of 415μA (dropping to 0.01μA when shutdown). Returning to normal operation within microseconds, this INA can be used for battery or multi-channel applications.

Configured internally in a gain of 5V/V, the INA331 offers flexibility in higher gains by choosing external resistors.

The INA331 rejects line noise and its harmonics, because common-mode error remains low even at higher frequencies.

High bandwidth and slew rate makes the INA331 ideal for directly driving sampling Analog-to-Digital (A/D) converters as well as general-purpose applications.

With high precision, low cost, and small packages, the INA331 outperforms discrete designs. They are specified for a wide temperature range of –55°C to +125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V–	7.5V
Signal Input Terminals, Voltage(2)	(V–) – 0.5V to (V+) + 0.5V
Current(2)	10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

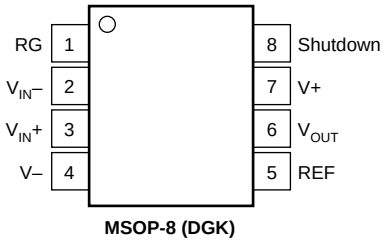
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
Single			
INA331IDGK	MSOP-8	DGK	C31
INA331AIDGK	MSOP-8	DGK	C31
Dual			
INA2331AIPW	TSSOP-14	PW	2331A

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION

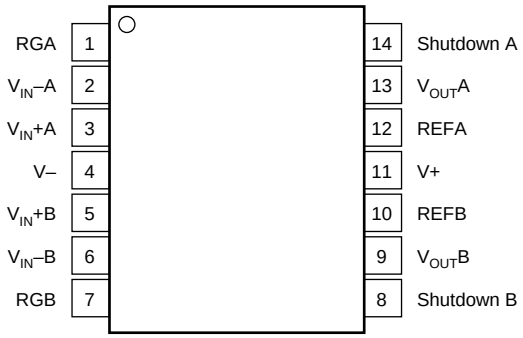
Top View

INA331



MSOP-8 (DGK)

INA2331



Dual, TSSOP-14 (PW)

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –55°C to 125°C.**

At T_A = +25°C, R_L = 10kΩ, G = 25, and V_{REF} = V_S/2, unless otherwise noted.

PARAMETER		CONDITION	INA331IDGK MIN	INA331IDGK TYP	INA331IDGK MAX	INA331AIDGK INA2331AIPW MIN	INA331AIDGK INA2331AIPW TYP	INA331AIDGK INA2331AIPW MAX	UNITS
INPUT									
Input Offset Voltage, RTI		V_S = +5V		±250	±500		*	±1000	µV
Over Temperature	**V_{OS}**				**±1.7**			**±2.1**	**mV**
Temperature Coefficient	**dV_{OS}/dT**			**±5**			★		**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V		±50	±200		*	*	µV/V
vs Temperature					**±220**			★	**µV/V**
Long-Term Stability				±0.4			*		µV/month
Input Impedance				10^{13} || 3			*		Ω || pF
Input Common-Mode Range		V_S = 2.7V	0.35		1.5	*		*	V
		V_S = 5V	0.55		3.8	*		*	V
Common-Mode Rejection	CMRR	V_S = 5V, V_{CM} = 0.55V to 3.8V	90	94		80	*		dB
–40°C to +85°C		V_S = 5V, V_{CM} = 0.55V to 3.8V	77			75			dB
Over Temperature		**V_S = 5V, V_{CM} = 0.55V to 3.8V**	**72**			**70**			**dB**
		V_S = 2.7V, V_{CM} = 0.35V to 1.5V		94			*		dB
Crosstalk, Dual							114		dB
INPUT BIAS CURRENT		V_{CM} = V_S/2							
Bias Current	I_B			±0.5	±10		*	*	pA
Offset Current	I_{OS}			±0.5	±10		*	*	pA
NOISE, RTI		R_S = 0Ω							
Voltage Noise: f = 10Hz	e_N			280			*		nV/√Hz
f = 100Hz				96			*		nV/√Hz
f = 1kHz				46			*		nV/√Hz
f = 0.1Hz to 10Hz				7			*		μV_{PP}
Current Noise: f = 1kHz	i_N			0.5			*		fA/√Hz
GAIN[1]									
Gain Equation, Externally Set		G > 5		G = 5 + ($5R_2/R_1$)			*		
Range of Gain			5		1000	*		*	V/V
Gain Error		G = 5		±0.02	±0.1		*	*	%
vs Temperature		**G = 5**		**±2**	**±10**		★	★	**ppm/°C**
Nonlinearity		G = 25[2], V_S = 5V, V_O = 0.05 to 4.95		±0.001	±0.010		*	*	% of FS
Over Temperature				**±0.002**	**±0.015**		★	★	**% of FS**
OUTPUT									
Output Voltage Swing from Rail[3]		R_L = 10kΩ	50	25		*	*		mV
Over Temperature		**G > 10**	**50**			★			**mV**
Capacitance Load Drive				See Typical Characteristics			*		pF
Short-Circuit Current				+48/–32			*		mA
FREQUENCY RESPONSE									
Bandwidth, –3dB	BW	G = 25		2.0			*		MHz
Slew Rate	SR	V_S = 5V, G = 25		5			*		V/µs
Settling Time, 0.1%	t_S	G = 25, C_L = 100pF, V_O = 2V step		1.7			*		µs
0.01%				2.5			*		µs
Overload Recovery		50% Input Overload G = 25		2			*		µs
POWER SUPPLY									
Specified Voltage Range			+2.7		+5.5	*		*	V
Operating Voltage Range				+2.5 to +5.5			*		V
Quiescent Current per Channel	I_Q	V_{SD} > 2.5[3]		415	490		*	*	µA
Over Temperature					**600**			★	**µA**
Shutdown Quiescent Current/Chan	I_{SD}	V_{SD} < 0.8[3]		0.01	1		*	*	µA
TEMPERATURE RANGE									
Specified/Operating Range			–55		+125	*		*	°C
Storage Range			–65		+150	*		*	°C
Thermal Resistance	θ_{JA}	MSOP-8, TSSOP-14 Surface Mount		150			*		°C/W

* Specifications same as INA331IDGK

NOTES: (1) Does not include errors from external gain setting resistors.

(2) Output voltage swings are measured between the output and power-supply rails. Output swings to rail only if G ≥ 10. Output does not swing to positive rail if gain is less than 10.

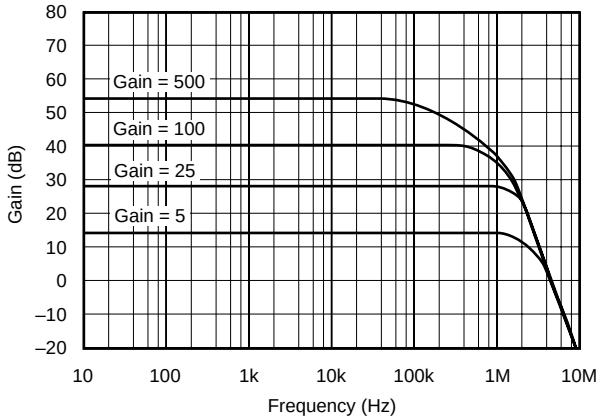
(3) See typical characteristic *Percent Overshoot vs Load Capacitance*.

(4) See typical characteristic *Shutdown Voltage vs Supply Voltage*.

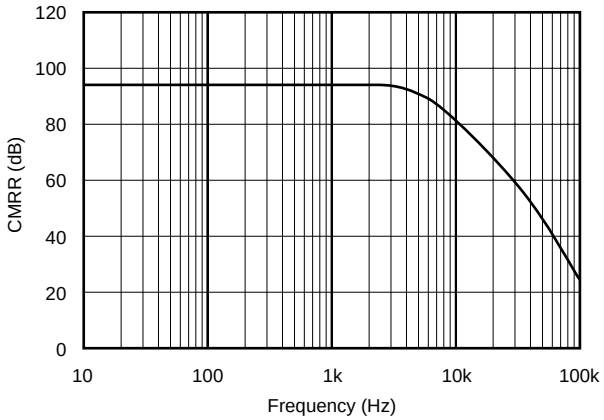
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

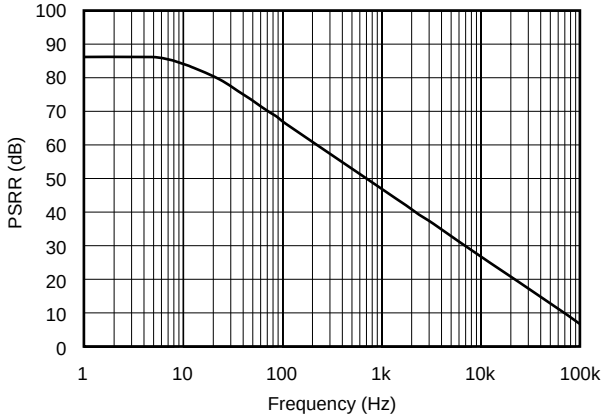
GAIN vs FREQUENCY



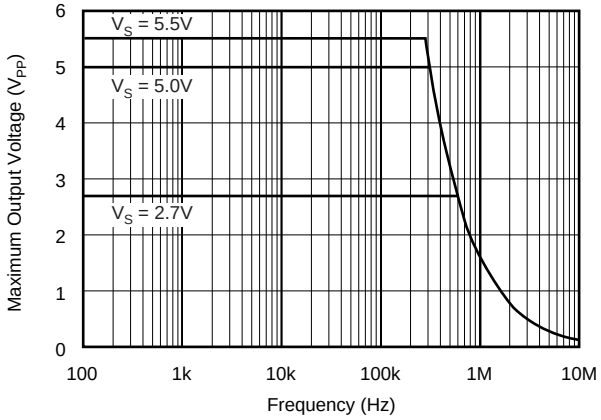
COMMON-MODE REJECTION RATIO vs FREQUENCY



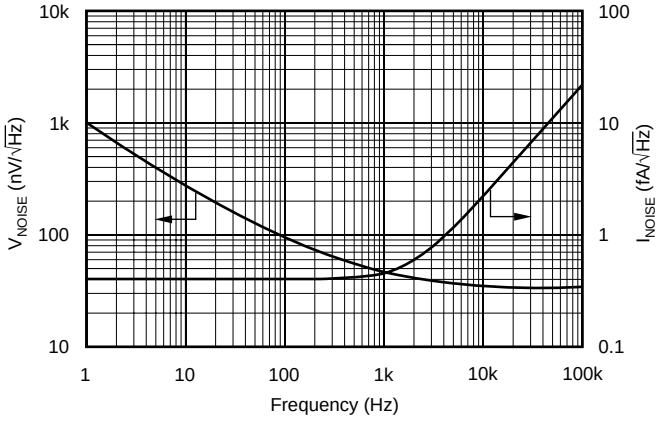
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



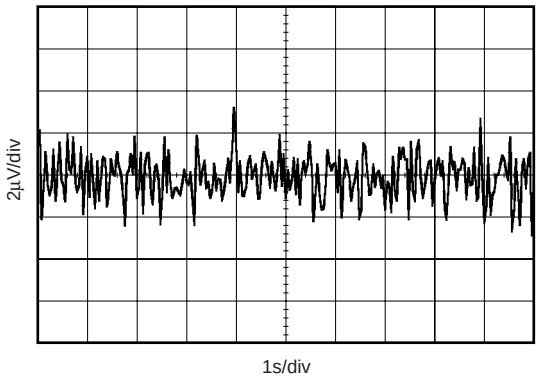
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



NOISE vs FREQUENCY



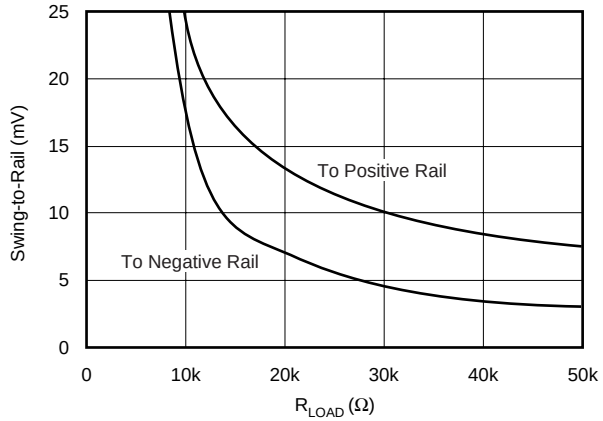
0.1Hz TO 10Hz VOLTAGE NOISE



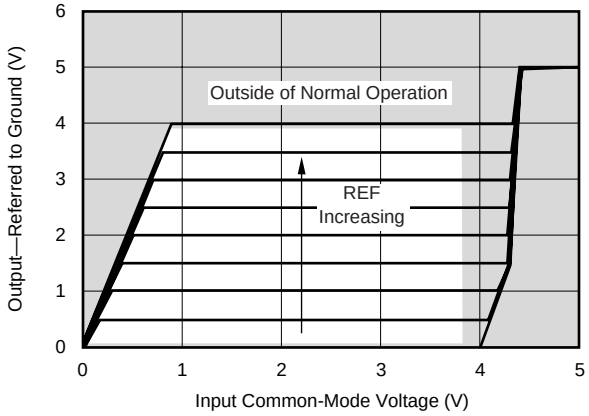
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

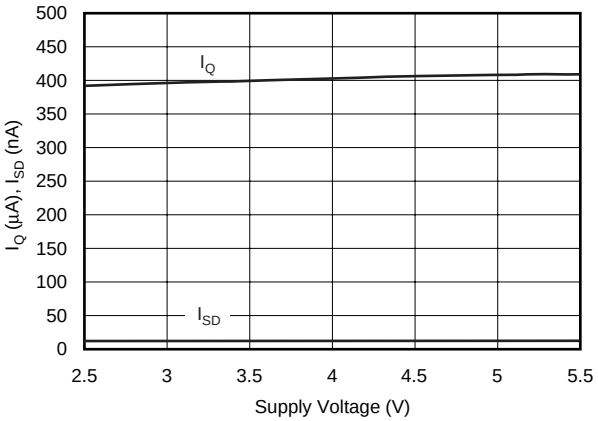
OUTPUT SWING vs LOAD RESISTANCE



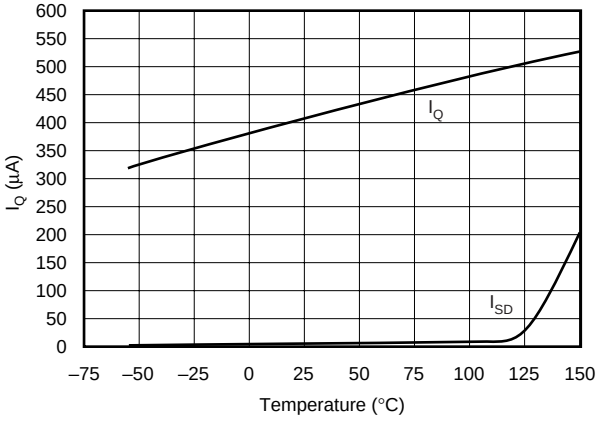
COMMON-MODE INPUT RANGE vs REFERENCE VOLTAGE



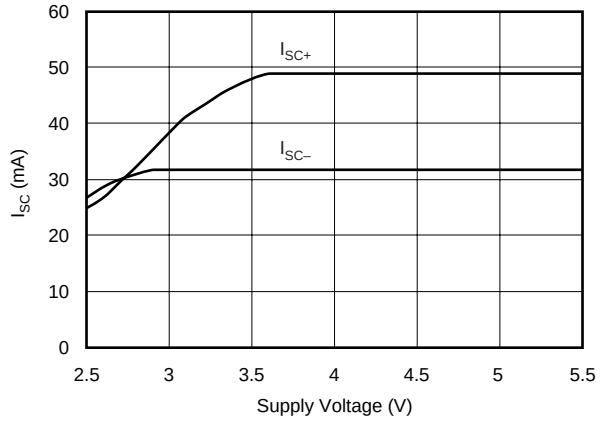
QUIESCENT CURRENT AND SHUTDOWN CURRENT vs POWER SUPPLY



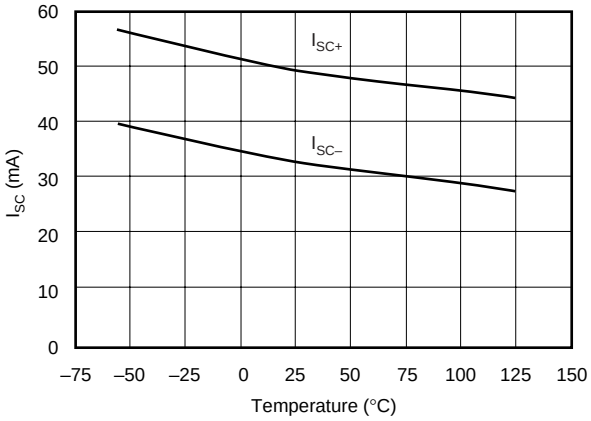
QUIESCENT CURRENT AND SHUTDOWN CURRENT vs TEMPERATURE



SHORT-CIRCUIT CURRENT vs POWER SUPPLY



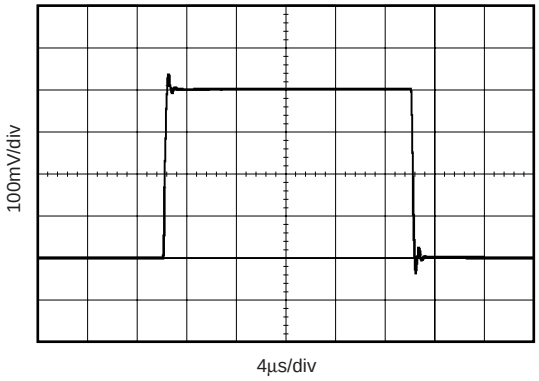
SHORT-CIRCUIT CURRENT vs TEMPERATURE



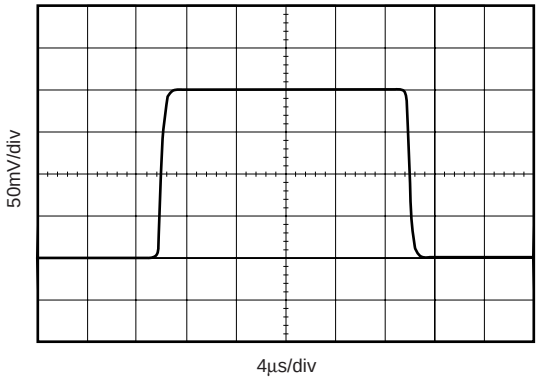
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

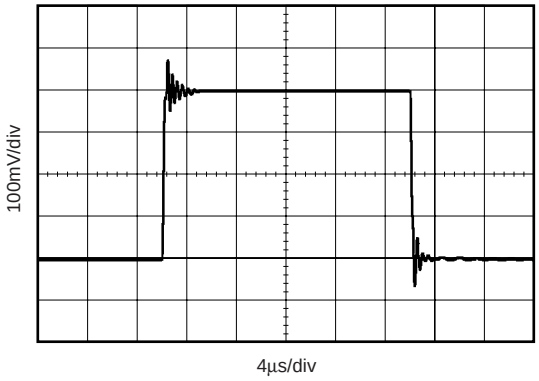
SMALL-SIGNAL STEP RESPONSE (G = 5)



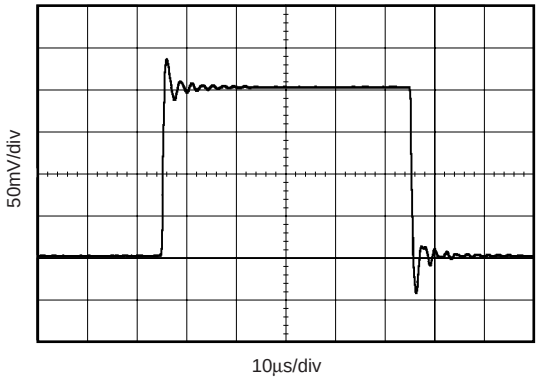
SMALL-SIGNAL STEP RESPONSE (G = 100)



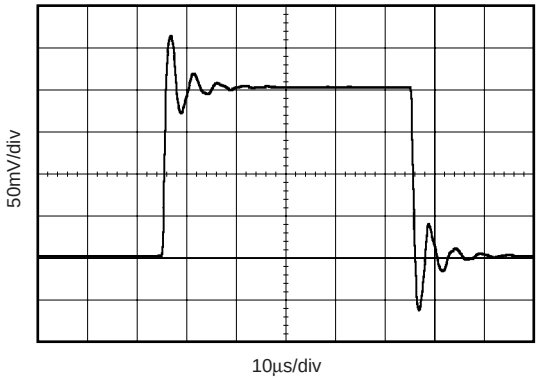
SMALL-SIGNAL STEP RESPONSE
(G = 5, C_L = 1000pF)



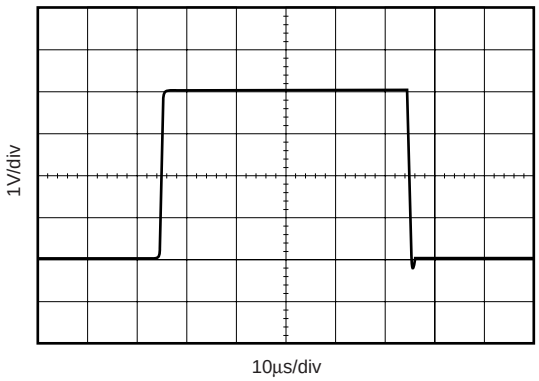
SMALL-SIGNAL STEP RESPONSE
(G = 100, C_L = 1000pF)



SMALL-SIGNAL STEP RESPONSE
(G = 100, C_L = 4700pF)



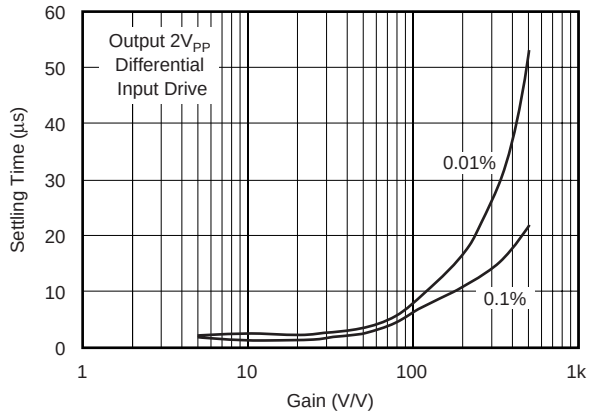
LARGE-SIGNAL STEP RESPONSE (G = 25)



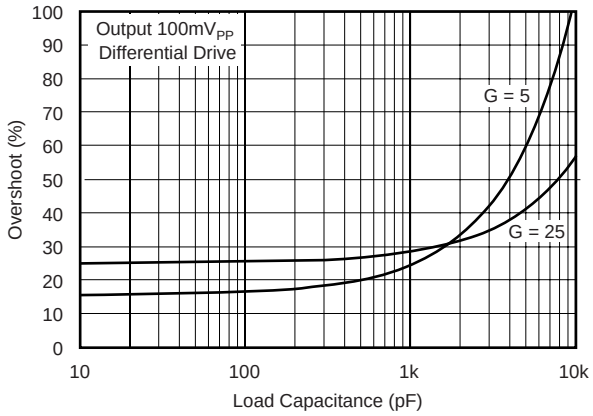
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

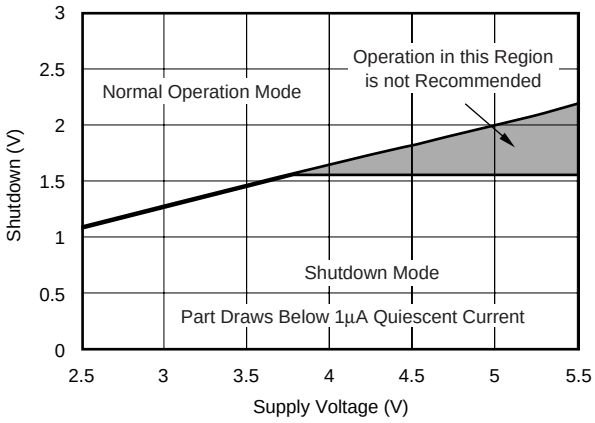
SETTLING TIME vs GAIN



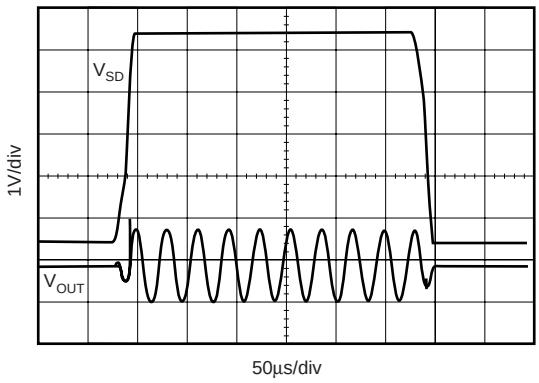
PERCENT OVERSHOOT vs LOAD CAPACITANCE



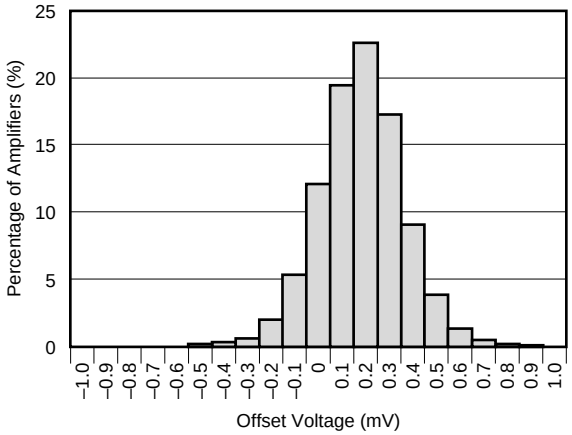
SHUTDOWN VOLTAGE vs SUPPLY VOLTAGE



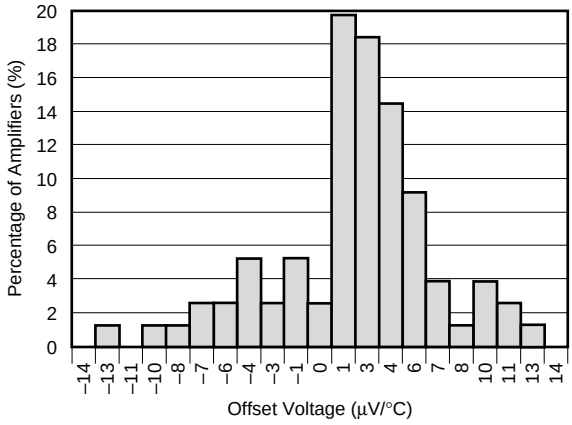
SHUTDOWN TRANSIENT BEHAVIOR



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



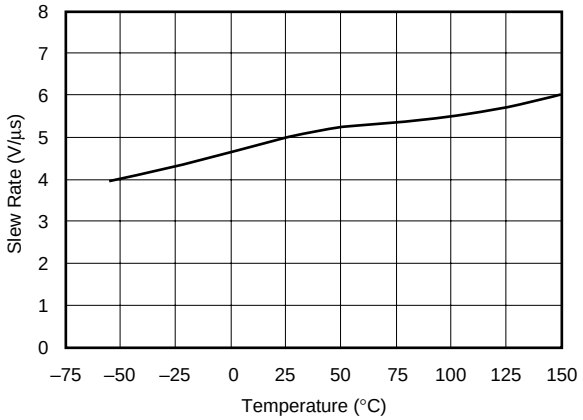
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



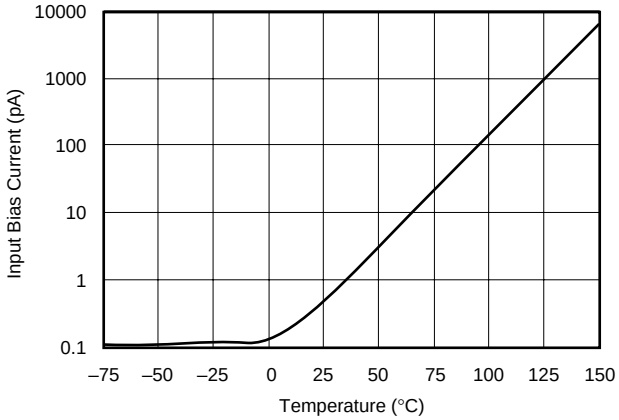
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

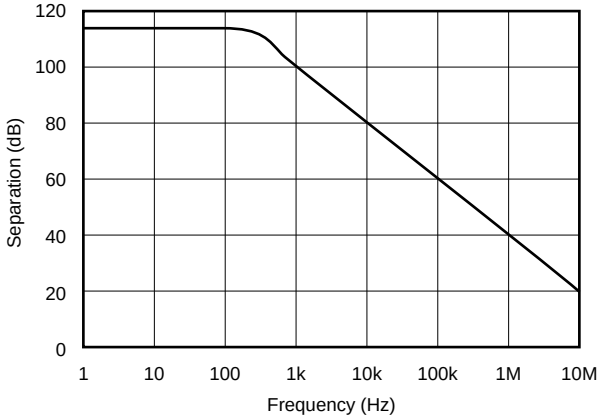
SLEW RATE vs TEMPERATURE



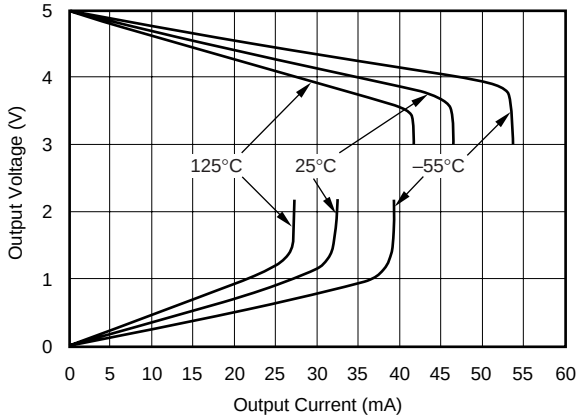
INPUT BIAS CURRENT vs TEMPERATURE



CHANNEL SEPARATION vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

The INA331 is a modified version of the classic “two op amp” instrumentation amplifier, with an additional gain amplifier.

Figure 1 shows the basic connections for the operation of the INA331 and INA2331. The power supply should be capacitively decoupled with 0.1µF capacitors as close to the INA331 as possible for noisy or high-impedance applications.

The output is referred to the reference terminal, which must be at least 1.2V below the positive supply rail.

OPERATING VOLTAGE

The INA331 family is fully specified over a supply range of +2.7V to +5.5V, with key parameters tested over the temperature range of –55°C to +125°C. Parameters that vary significantly with operating conditions, such as load conditions or temperature, are shown in the Typical Characteristics.

The INA331 may be operated on a single supply. Figure 2 shows a bridge amplifier circuit operated from a single +5V supply. The bridge provides a small differential voltage riding on an input common-mode voltage.

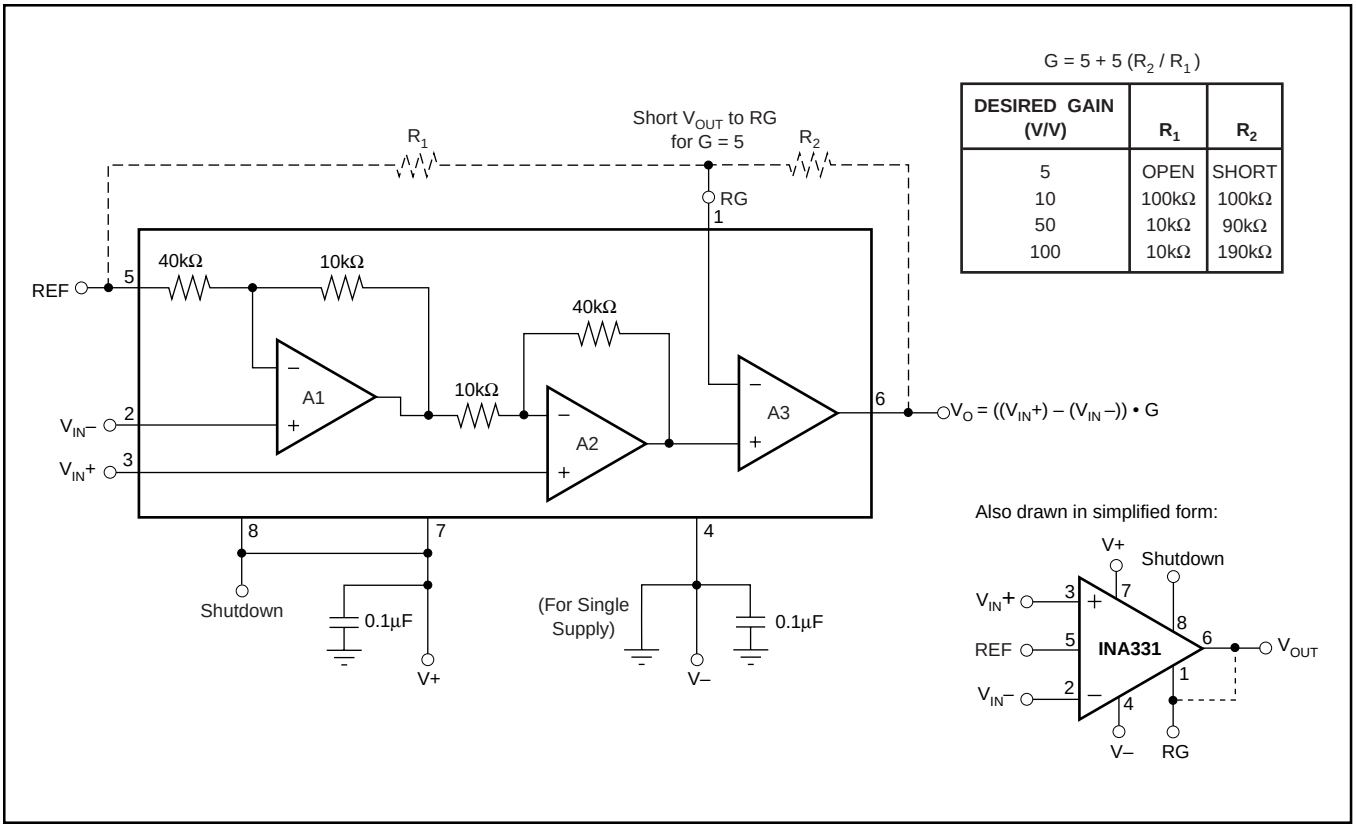


FIGURE 1. Basic Connections.

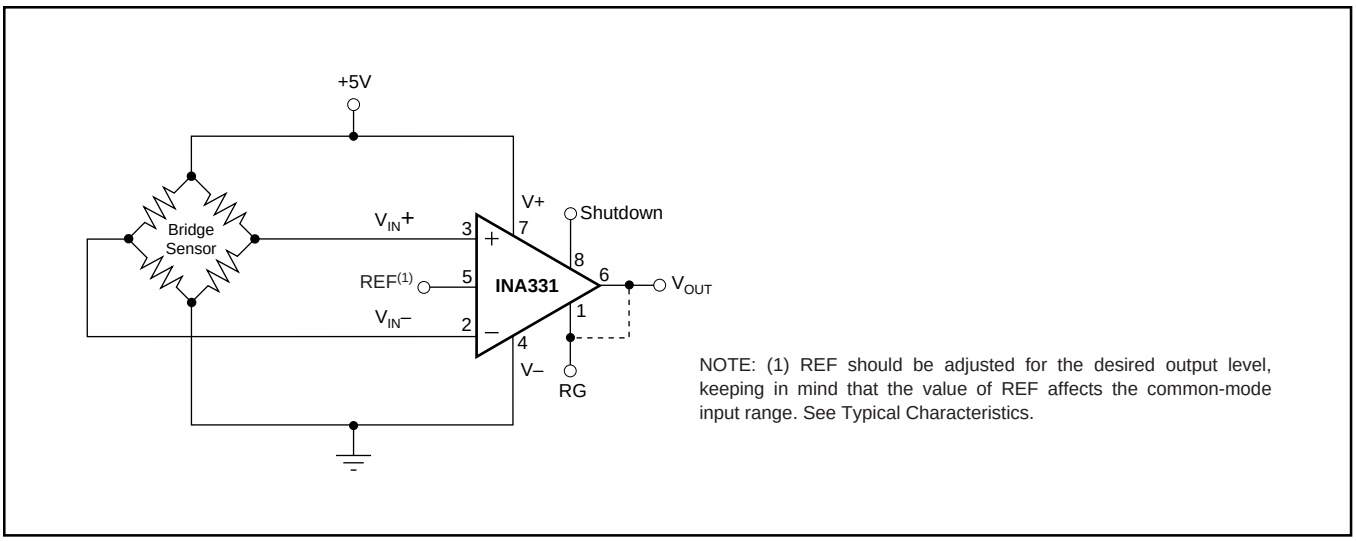


FIGURE 2. Single-Supply Bridge Amplifier.

SETTING THE GAIN

The ratio of R_2 to R_1, or the impedance between pins 1, 5, and 6, determines the gain of the INA331. With an internally set gain of 5, the INA331 can be programmed for gains greater than 5 according to the following equation:

$$G = 5 + 5\ (R_2/R_1)$$

The INA331 is designed to provide accurate gain, with gain error less than 0.1%. Setting gain with matching TC resistors will minimize gain drift. Errors from external resistors will add directly to the error, and may become dominant error sources.

COMMON-MODE INPUT RANGE

The upper limit of the common-mode input range is set by the common-mode input range of the second amplifier, A2, to 1.2V below positive supply. Under most conditions, the amplifier operates beyond this point with reduced performance. The lower limit of the input range is bounded by the output swing of amplifier A1, and is a function of the reference voltage according to the following equation:

$$V_{OA1} = 5/4\ V_{CM} - 1/4\ V_{REF}$$

(See typical characteristics *Common-Mode Input Range vs Reference Voltage*.)

REFERENCE

The reference terminal defines the zero output voltage level. In setting the reference voltage, the common-mode input of A3 should be considered according to the following equation:

$$V_{OA2} = V_{REF} + 5\ (V_{IN}+ - V_{IN}-)$$

For ensured operation, V_{OA2} should be less than $V_{DD} - 1.2V$.

The reference pin requires a low-impedance connection. As little as 160Ω in series with the reference pin will degrade the CMRR to 80dB. The reference pin may be used to compensate for the offset voltage (see Offset Trimming section). The reference voltage level also influences the common-mode input range (see Common-Mode Input Range section).

INPUT BIAS CURRENT RETURN

With a high input impedance of $10^{13}\Omega$, the INA331 is ideal for use with high-impedance sources. The input bias current of less than 10pA makes the INA331 nearly independent of input impedance and ideal for low-power applications.

For proper operation, a path must be provided for input bias currents for both inputs. Without input bias current paths, the inputs will "float" to a potential that exceeds common-mode range and the input amplifier will saturate. Figure 3 shows how the bias current path can be provided in the cases of microphone applications, thermistor applications, ground returns, and dc-coupled resistive bridge applications.

When differential source impedance is low, the bias current return path can be connected to one input. With higher source impedance, two equal resistors will provide a balanced input. The advantages are lower input offset voltage due to bias current flowing through the source impedance and better high-frequency gain.

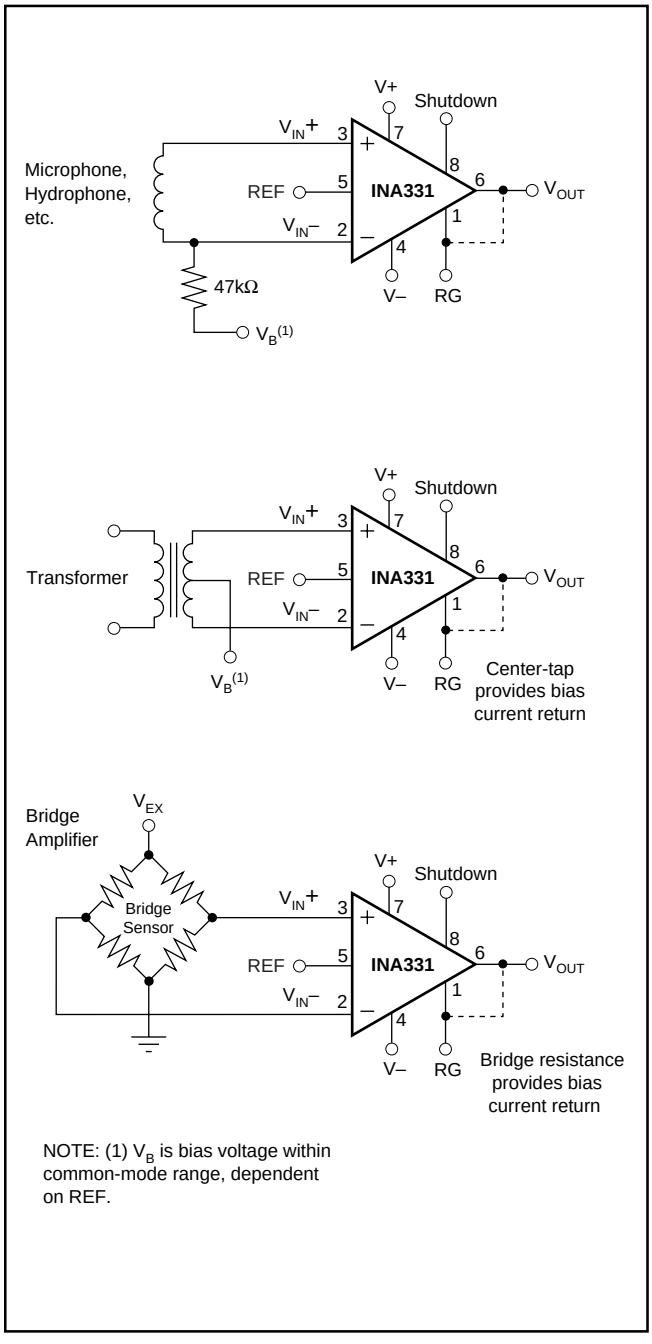


FIGURE 3. Providing an Input Common-Mode Path.

APPLICATION CIRCUITS

MEDICAL ECG APPLICATIONS

Figure 9 shows the INA331 configured to serve as a low-cost ECG amplifier, suitable for moderate accuracy heart-rate applications such as fitness equipment. The input signals are obtained from the left and right arms of the patient. The common-mode voltage is set by two 2MΩ resistors. This potential through a buffer provides an optional right leg drive. Filtering can be modified to suit application needs by changing the capacitor value of the output filter.

LOW-POWER, SINGLE-SUPPLY DATA ACQUISITION SYSTEMS

Refer to Figure 4 to see the INA331 configured to drive an ADS7818. Functioning at frequencies of up to 500kHz, the INA331 is ideal for low-power data acquisition.

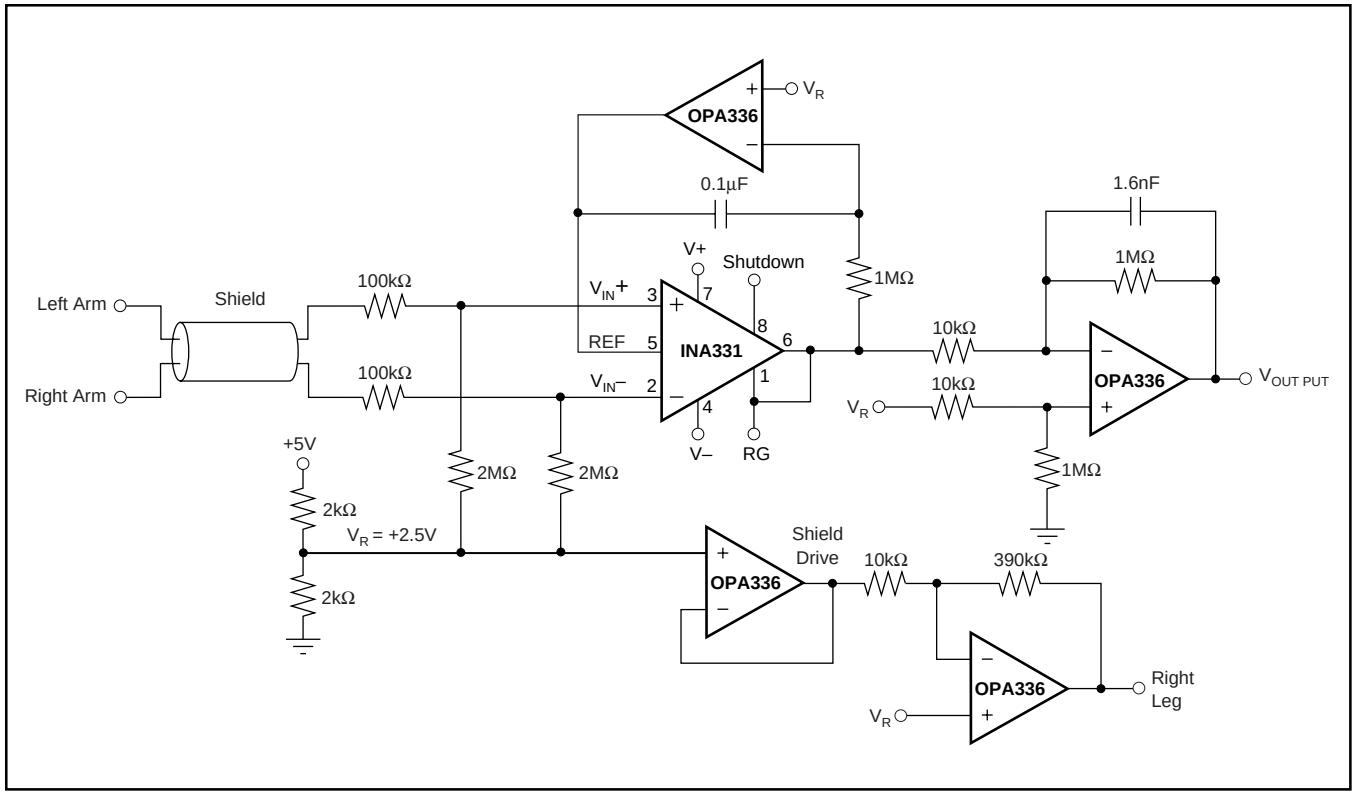
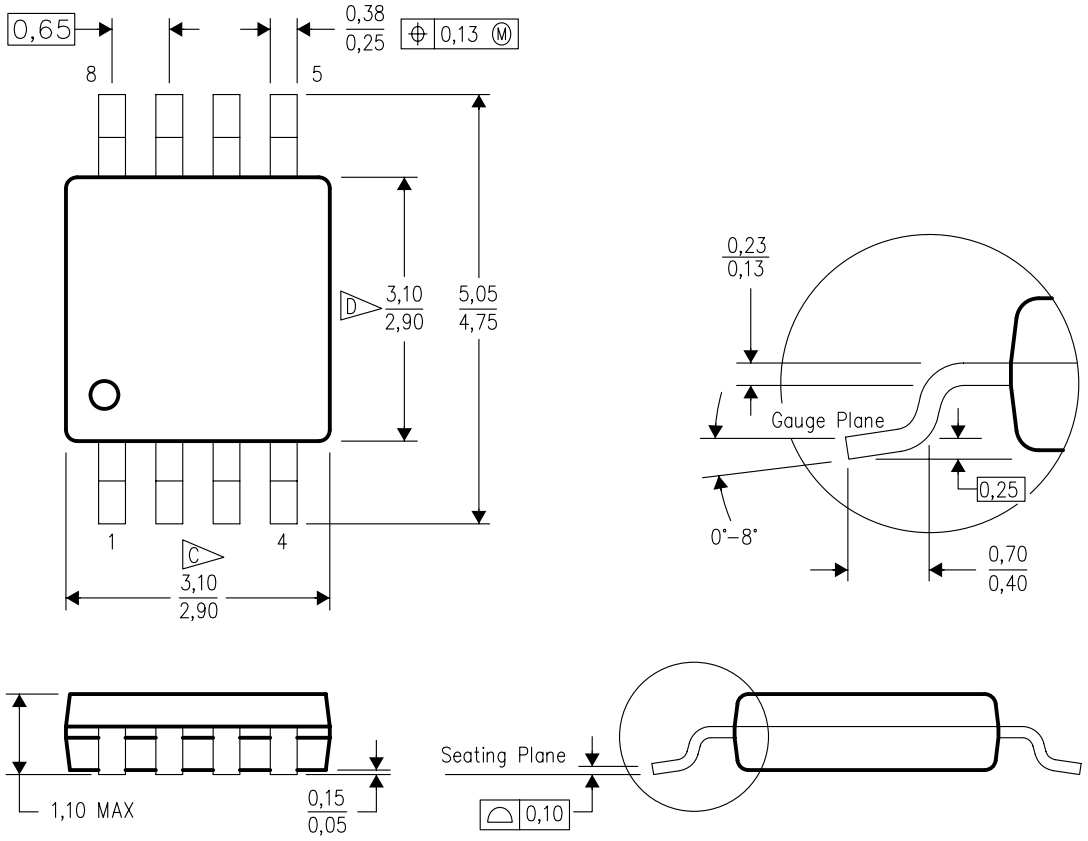


FIGURE 9. Simplified ECG Circuit for Medical Applications.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

TEXAS INSTRUMENTS

OPA330, OPA2330, OPA4330

SBOS432G – AUGUST 2008 – REVISED AUGUST 2016

OPAx330 50-µV V_{OS}, 0.25-µV/°C, 35-µA CMOS Operational Amplifiers Zero-Drift Series

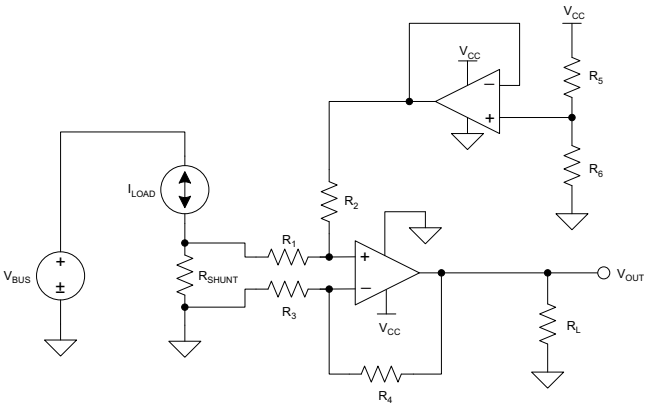
1 Features

- Unmatched Price Performance
- Low Offset Voltage: 50 µV (Maximum)
- Zero Drift: 0.25 µV/°C (Maximum)
- Low Noise: 1.1 μV_{PP}, 0.1 Hz to 10 Hz
- Quiescent Current: 35 µA (Maximum)
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input and Output
- Internal EMI Filtering
- *micro*Size Packages: DSBGA, SC70, VQFN

2 Applications

- Battery-Powered Instruments
- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Handheld Test Equipment
- Current Sense

Bidirectional, Low-Side Current Sense



3 Description

The OPA330 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the Zero-Drift family of amplifiers which use a proprietary auto-calibration technique to simultaneously provide low offset voltage (50-µV maximum) and near-zero drift over time and temperature at only 35 µA (maximum) of quiescent current. The OPA330 family features rail-to-rail input and output in addition to near-flat 1/f noise, making this amplifier ideal for many applications and much easier to design into a system. These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V).

The OPA330 (single version) is available in the 5-pin DSBGA, 5-pin SC70, 5-pin SOT-23, and 8-pin SOIC packages. The OPA2330 (dual version) is offered in 3 mm × 3 mm, 8-pin SON, 8-pin VSSOP, and 8-pin SOIC packages. The OPA4330 is offered in the standard 14-pin SOIC and 14-pin TSSOP packages, as well as in the space-saving 14-pin VQFN package. All versions are specified for operation from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA330	SOIC (8)	4.90 mm × 3.91 mm
	SOT (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
	DSBGA (5)	0.00 mm × 0.00 mm
OPA2330	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SON (8)	3.00 mm × 3.00 mm
OPA4330	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (14)	3.50 mm × 3.50 mm

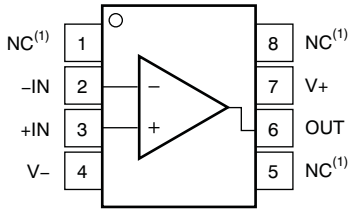
(1) For all available packages, see the orderable addendum at the end of the data sheet.

5 Device Comparison Table

DEVICE	NO OF CHANNELS	PACKAGE-LEADS							
		DSBGA	SOIC	SOT	SC70	VSSOP	SON	VQFN	TSSOP
OPA330	1	5	8	5	5	—	—	—	—
OPA2330	2	—	8	—	—	8	8	—	—
OPA4330	4	—	14	—	—	—	—	14	14

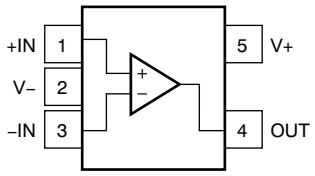
6 Pin Configurations and Functions

OPA330: D Package
8-Pin SOIC
Top View

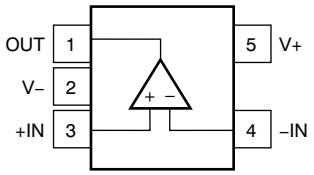


(1) NC denotes no internal connection.

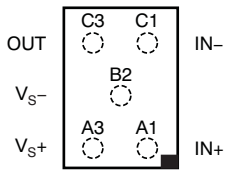
OPA330: DCK Package
5-Pin SC70
Top View



OPA330: DBV Package
5-Pin SOT-23
Top View



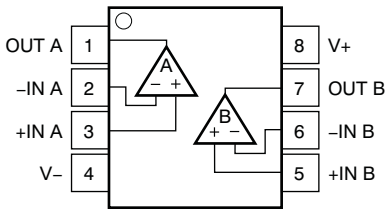
OPA330: YFF Package
5-Pin DSBGA
Top View



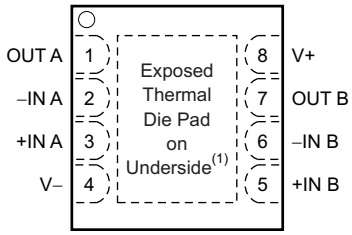
Pin Functions: OPA330

PIN					I/O	DESCRIPTION
NAME	SOIC	SOT-23	SC70	DSBGA		
–IN	2	4	3	C1	I	Negative (inverting) input
+IN	3	3	1	A1	I	Positive (noninverting) input
NC	1, 5, 8	—	—	—	—	No internal connection (can be left floating)
OUT	6	1	4	C3	O	Output
V–	4	2	2	—	—	Negative (lowest) power supply
V+	7	5	5	—	—	Positive (highest) power supply
$V_{S–}$	—	—	—	B2	—	Negative (lowest) power supply
V_{S+}	—	—	—	A3	—	Positive (highest) power supply

OPA2330: D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



OPA2330: DRB Package
8-Pin SON
Top View

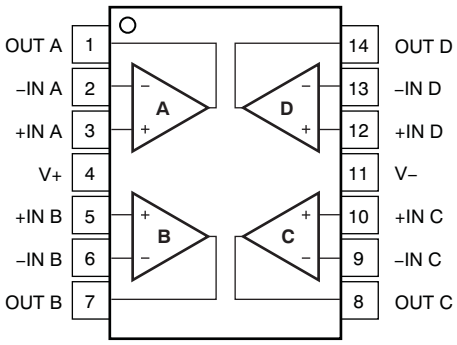


(1) Connect thermal die pad to V–.

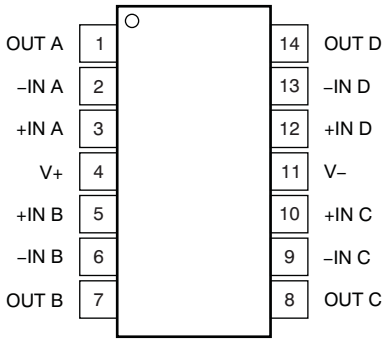
Pin Functions: OPA2330

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP	SON		
–IN A	2	2	I	Negative (inverting) input signal, channel A
+IN A	3	3	I	Positive (noninverting) input signal, channel A
–IN B	6	6	I	Negative (inverting) input signal, channel B
+IN B	5	5	I	Positive (noninverting) input signal, channel B
OUT A	1	1	O	Output channel A
OUT B	7	7	O	Output channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

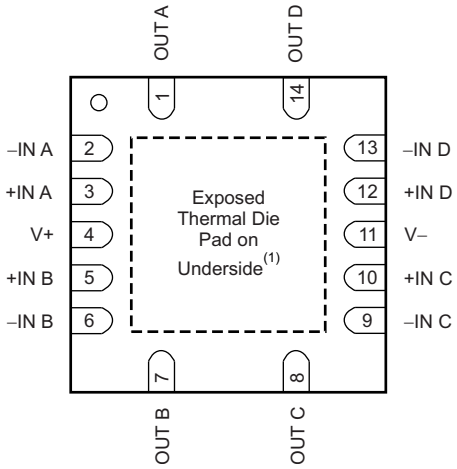
OPA4330: D Package
14-Pin SOIC
Top View



OPA4330: PW Package
14-Pin TSSOP
Top View



OPA4330: RGY Package
14-Pin VQFN
Top View



(1) Connect thermal die pad to V–.

Pin Functions: OPA4330

PIN				I/O	DESCRIPTION
NAME	SOIC	TSSOP	VQFN		
–IN A	2	2	2	I	Negative (inverting) input signal, channel A
+IN A	3	3	3	I	Positive (noninverting) input signal, channel A
–IN B	6	6	6	I	Negative (inverting) input signal, channel B
+IN B	5	5	5	I	Positive (noninverting) input signal, channel B
–IN C	9	9	9	I	Negative (inverting) input signal, channel C
+IN C	10	10	10	I	Positive (noninverting) input signal, channel C
–IN D	13	13	13	I	Negative (inverting) input signal, channel D
+IN D	12	12	12	I	Positive (noninverting) input signal, channel D
OUT A	1	1	1	O	Output channel A
OUT B	7	7	7	O	Output channel B
OUT C	8	8	8	O	Output channel C
OUT D	14	14	14	O	Output channel D
V–	11	11	11	—	Negative (lowest) power supply
V+	4	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_S = (V+) – (V–)		7	V
	Signal input terminals(2) (TBD should terminal be pin?)	(V–) –0.3	(V+) + 0.3	V
Current	Signal input terminals(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Operating range, T_A	–40	150	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
(V+) – (V–)	Supply voltage	±0.9 (1.8)	±2.5 (5)	±2.75 (5.5)	V
T_A	Specified temperature	–40	25	125	°C

7.4 Thermal Information: OPA330

THERMAL METRIC(1)		OPA330				UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	YFF (DSBGA)	
		8 PINS	5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.1	220.8	298.4	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.6	61.7	97.1	51	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2330

THERMAL METRIC(1)		OPA2330			UNIT
		D (SOIC)	DGK (VSSOP)	DRB (SON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124	180.3	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	48.1	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	100.9	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18	2.4	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	22.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	10.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4330

THERMAL METRIC(1)		OPA4330			UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	120.8	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	34.3	75.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	62.8	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	1	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	56.5	19.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_S = 1.8 V to 5.5 V, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V			8	50	µV
dV_{OS}/dT	Input offset voltage versus temperature	At T_A = –40°C to +125°C			0.02	0.25	µV/°C
PSRR	Input offset voltage versus power supply	At T_A = –40°C to +125°C			1	10	µV/V
	Long-term stability(1)	V_S = 1.8 V to 5.5 V			See (1)		
	Channel separation, dc				0.1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	At 25°C			±200	±500	pA
			OPA330YFF, OPA4330		±70	±300	pA
		At T_A = –40°C to +125°C			±300		pA
I_{OS}	Input offset current	At 25°C			±400	±1000	pA
			OPA330YFF, OPA4330		±140	±600	pA
NOISE							
e_n	Input voltage noise density	f = 1 kHz			55		nV/√Hz
	Input voltage noise	f = 0.01 Hz to 1 Hz			0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz			1.1		$µV_{PP}$
i_n	Input current noise	f = 10 Hz			100		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	At T_A = –40°C to +125°C, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V		100	115		dB
		At T_A = –40°C to +125°C, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V		100	115		dB
			OPA330YFF, OPA4330	100	115		dB
INPUT CAPACITANCE							
	Differential				2		pF
	Common-mode				4		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	At T_A = –40°C to +125°C, (V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ		100	115		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 100 pF			350		kHz
SR	Slew rate	G = +1			0.16		V/µs
OUTPUT							
	Voltage output swing from rail	At T_A = –40°C to +125°C			30	100	mV
I_{SC}	Short-circuit current				±5		mA
C_L	Capacitive load drive			See *Typical Characteristics*			
	Open-loop output impedance	f = 350 kHz, I_O = 0 mA			2		kΩ
POWER SUPPLY							
V_S	Specified voltage range			1.8		5.5	V
I_Q	Quiescent current per amplifier	At T_A = –40°C to +125°C, I_O = 0 mA			21	35	µA
	Turnon time	V_S = 5 V			100		µs

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

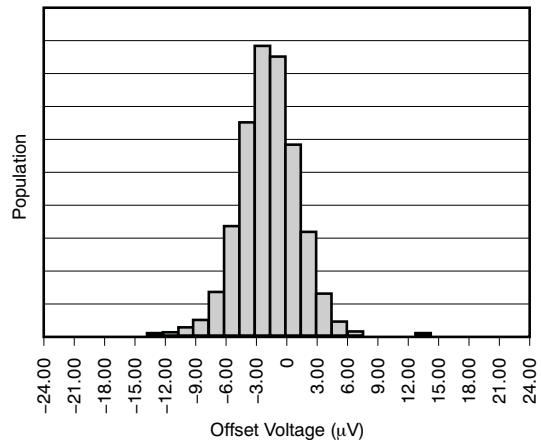


Figure 1. Offset Voltage Production Distribution

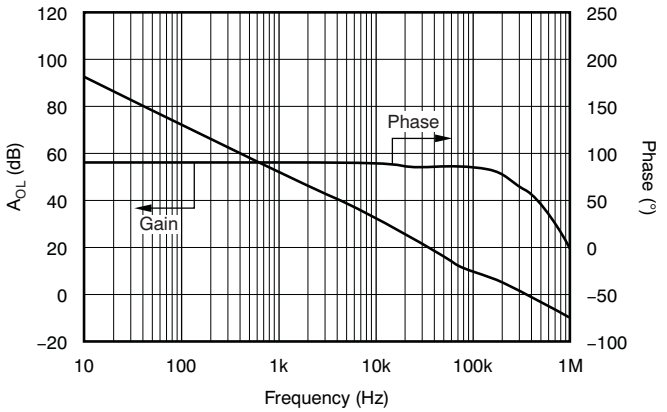


Figure 2. Open-Loop Gain vs Frequency

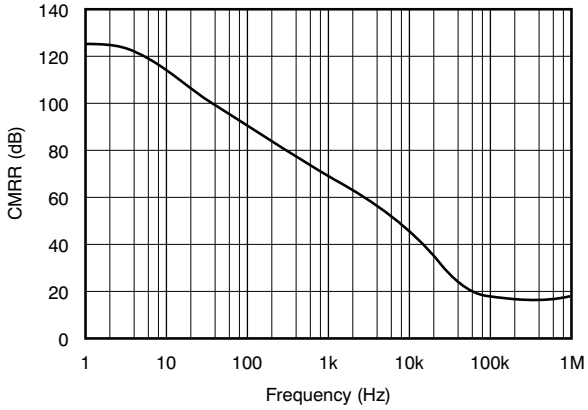


Figure 3. Common-Mode Rejection Ratio vs Frequency

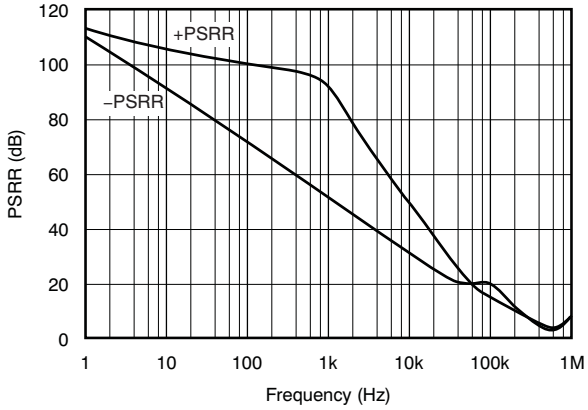


Figure 4. Power-Supply Rejection Ratio vs Frequency

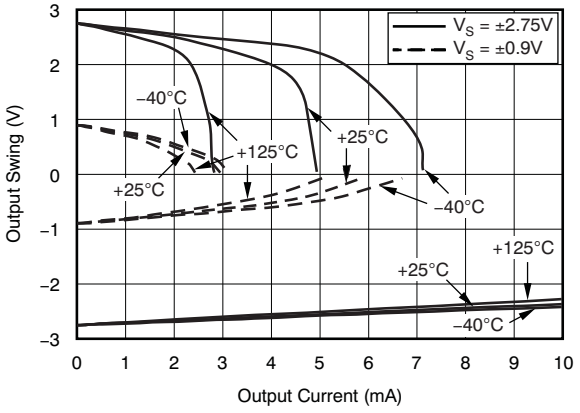


Figure 5. Output Voltage Swing vs Output Current

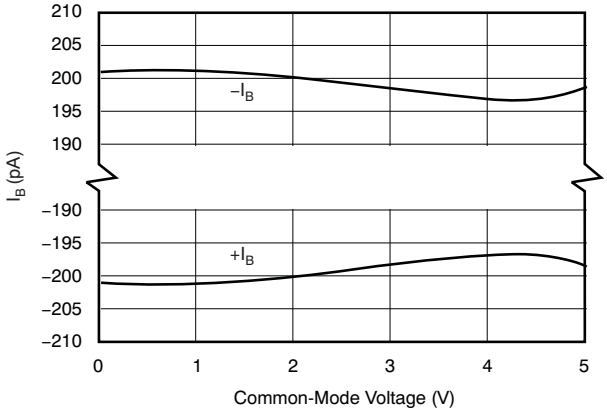


Figure 6. Input Bias Current vs Common-Mode Voltage

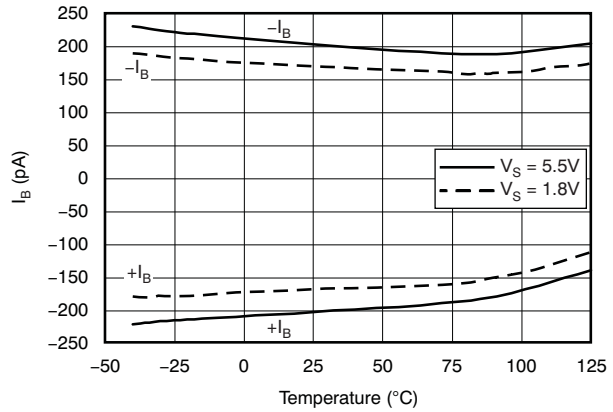


Figure 7. Input Bias Current vs Temperature

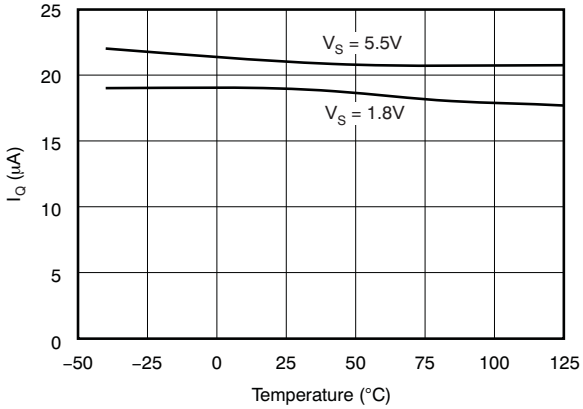


Figure 8. Quiescent Current vs Temperature

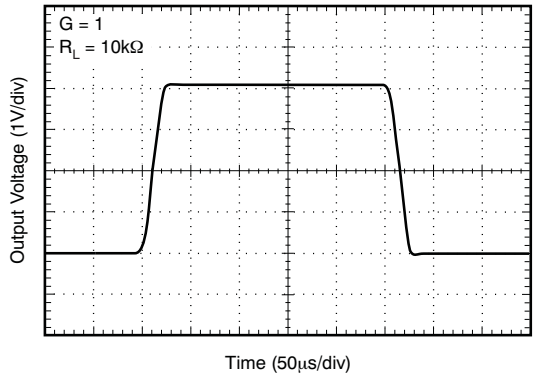


Figure 9. Large-Signal Step Response

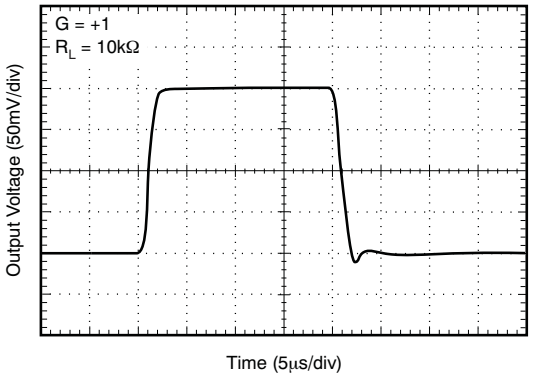


Figure 10. Small-Signal Step Response

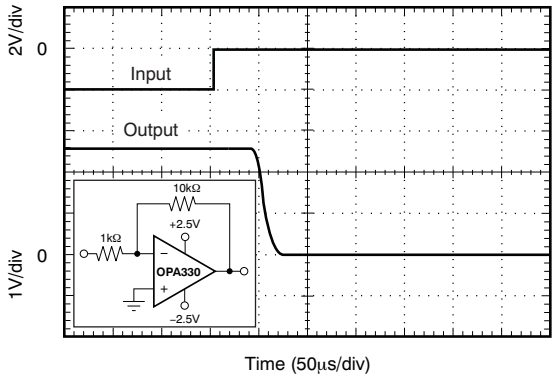


Figure 11. Positive Overvoltage Recovery

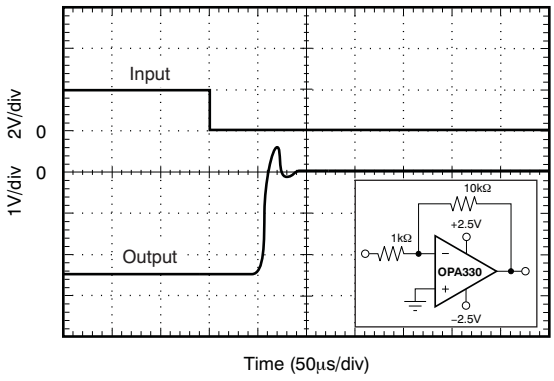


Figure 12. Negative Overvoltage Recovery

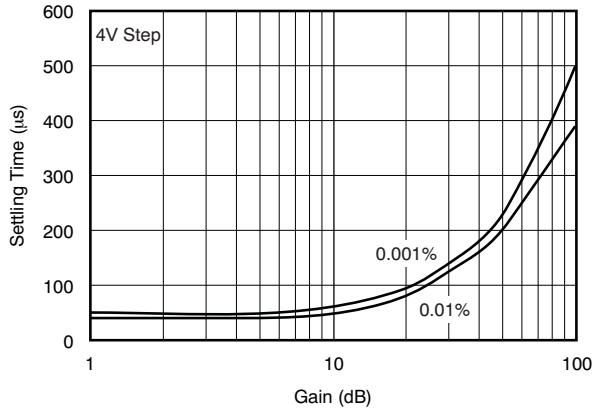


Figure 13. Settling Time vs Closed-Loop Gain

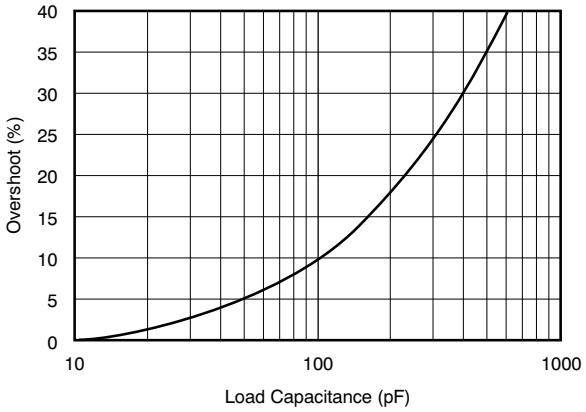


Figure 14. Small-Signal Overshoot vs Load Capacitance

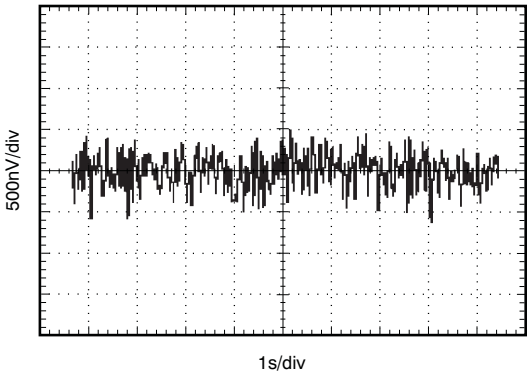


Figure 15. 0.1-Hz to 10-Hz Noise

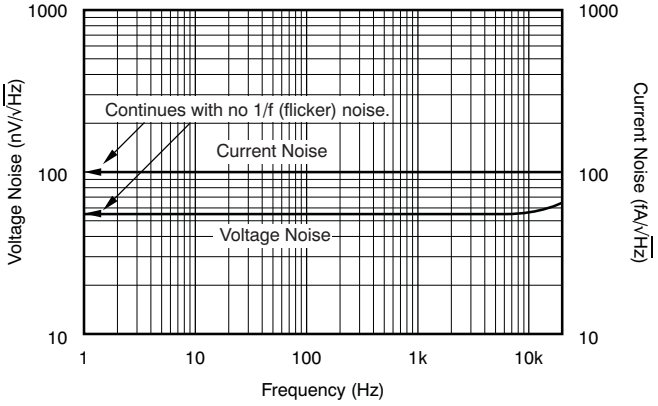


Figure 16. Current and Voltage Noise Spectral Density vs Frequency

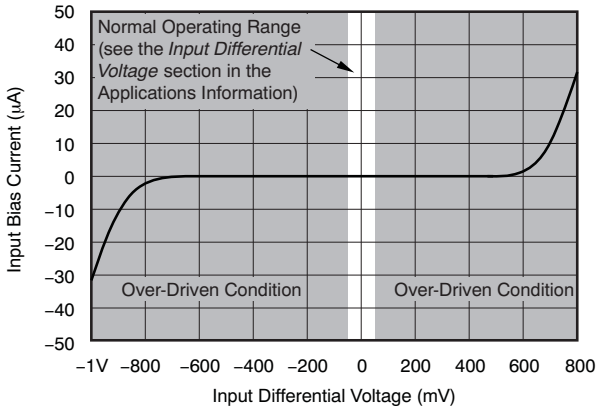


Figure 17. Input Bias Current vs Input Differential Voltage

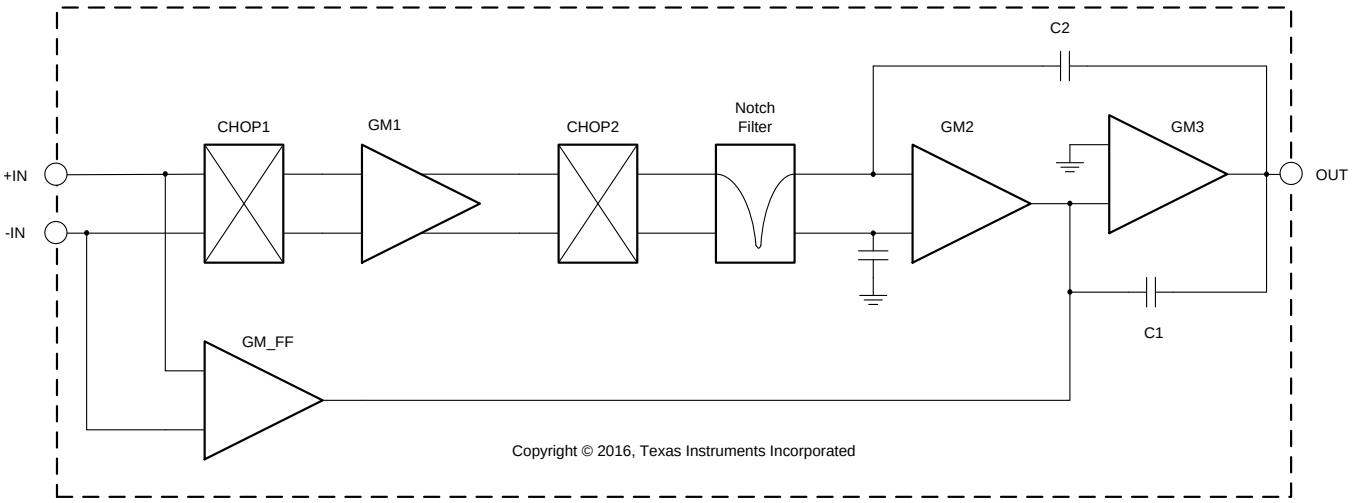
8 Detailed Description

8.1 Overview

The OPA330 family of Zerø-Drift amplifiers feature a proprietary auto-calibration technique to simultaneously achieve near-zero drift over time and temperature at only 35 µA (maximum) of quiescent current while also providing low offset voltage (50 µV maximum). These devices are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. The OPA330 series are also optimized for low-voltage, single-supply operation: as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V).

The proprietary Zerø-Drift circuitry lowers the 1/f noise component as well as offers the advantage of low input offset voltage over time and temperature. The OPA330 series of operational amplifiers are ideal for cost-sensitive applications and applications that operate without regulation directly from battery power.

8.2 Functional Block Diagram



8.3 Feature Description

The OPA33x family is unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout, and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher, depending on materials used.

8.4 Device Functional Modes

The OPAx330 has a single functional mode and is operational when the power-supply voltage is greater than 1.8 V (±0.9 V). The maximum power-supply voltage for the OPAx330 is 5.5 V (±2.75 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA330, OPA2330, and OPA4330 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. The use of proprietary Zerø-Drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPA330 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies and a rail-to-rail output that swings within 100 mV of the supplies under normal test conditions. The OPA330 series are precision amplifiers for cost-sensitive applications.

9.1.1 Operating Voltage

The OPA330 series operational amplifiers can be used with single or dual supplies from an operating range of V_S = 1.8 V (±0.9 V) up to 5.5 V (±2.75 V). Supply voltages greater than 7 V can permanently damage the device (see *Absolute Maximum Ratings*). Key parameters that vary over the supply voltage or temperature range are shown in *Typical Characteristics*.

9.1.2 Input Voltage

The OPA330, OPA2330, and OPA4330 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA330 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 200 pA. Input voltages exceeding the power supplies however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.

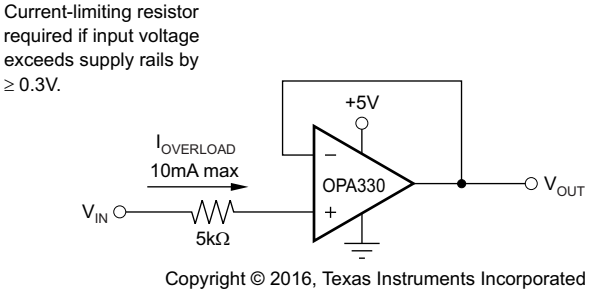


Figure 18. Input Current Protection

9.1.3 Input Differential Voltage

The typical input bias current of the OPA330 during normal operation is approximately 200 pA. In over-driven conditions, the bias current can increase significantly (see Figure 17). The most common cause of an over-driven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit illustrated in Figure 19. Notice that the input bias current remains within specification within the linear region.

Application Information (continued)

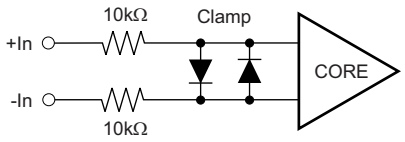


Figure 19. Equivalent Input Circuit

9.1.4 Internal Offset Correction

The OPA330, OPA2330, and OPA4330 operational amplifiers use an auto-calibration technique with a time-continuous, 125-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

9.1.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in their susceptibility to EMI. If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from its nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA330 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8 MHz (–3 dB), with a rolloff of 20 dB per decade.

9.1.6 Achieving Output Swing to the Operational Amplifier Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good single-supply operational amplifier may swing close to single-supply ground, but does not reach ground. The output of the OPA330, OPA2330, and OPA4330 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the operational amplifier negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 20.

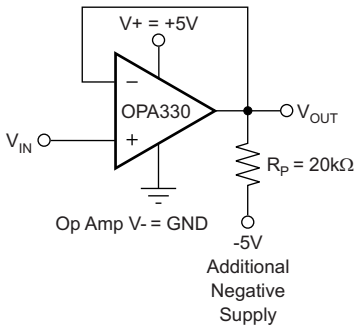
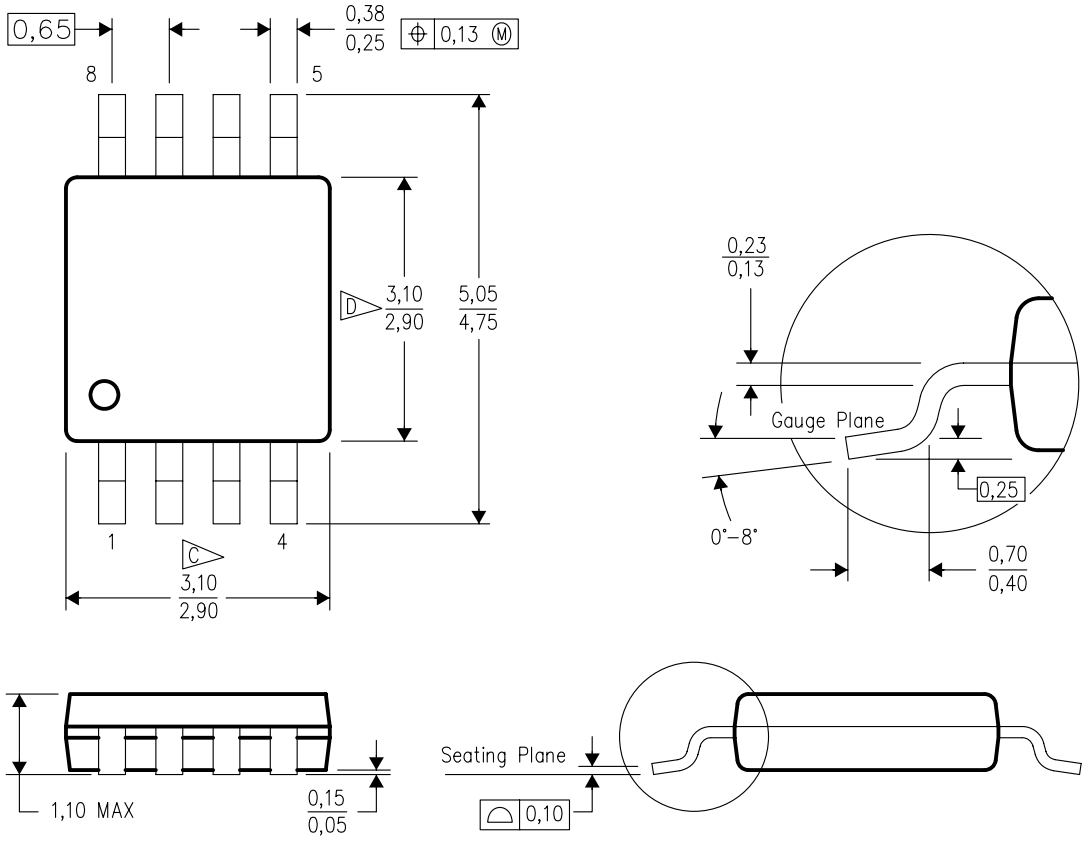


Figure 20. For V_{OUT} Range to Ground

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

CUSTOMER'S NAME

Mouser Electronics

ALPHA REFERENCE NO.
SP15080163

SPECIFICATION

PART NO.	ALPHA MODEL NAME
1.	MF22-N-064-A01

MODEL NAME
MODEL NO.

APPROVAL

PREPARED BY	REVIEWED BY	APPROVED BY

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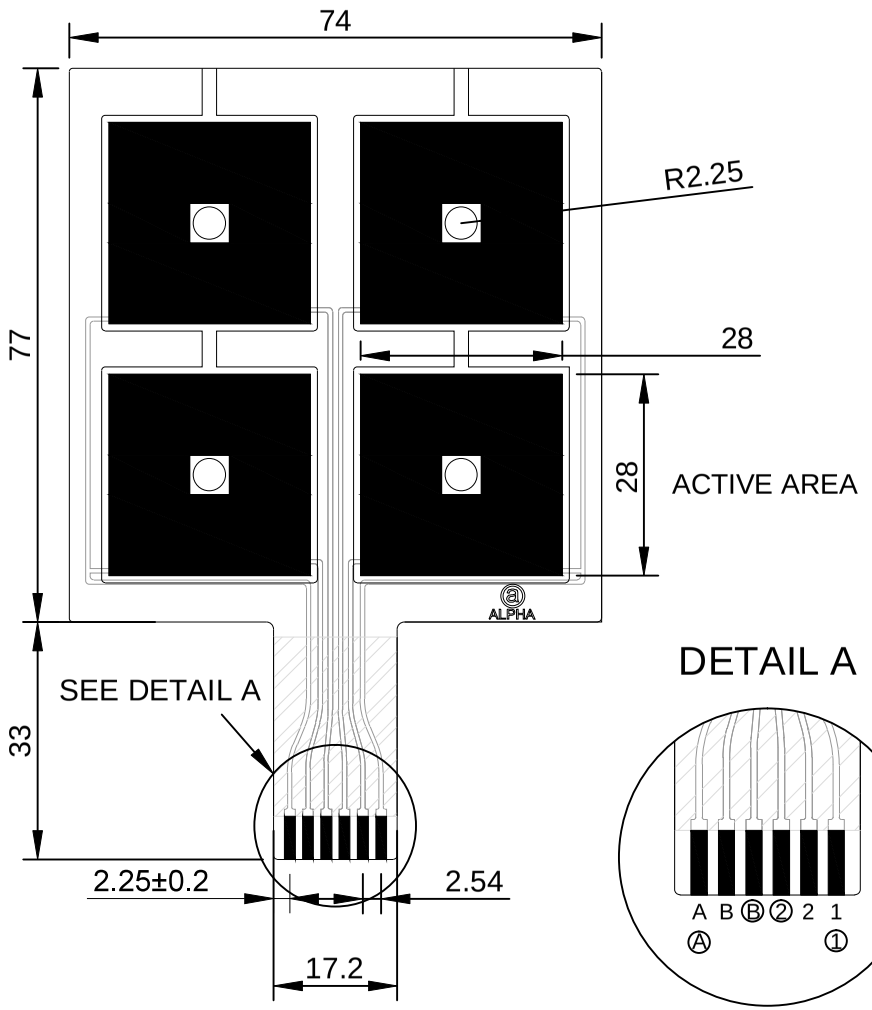
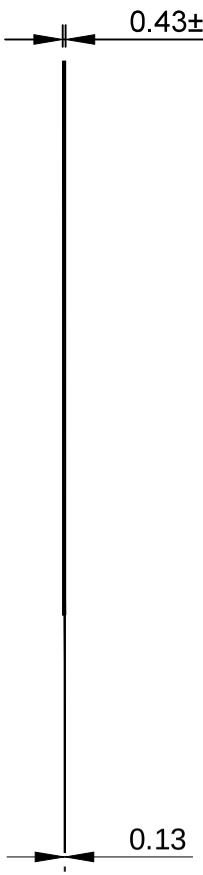
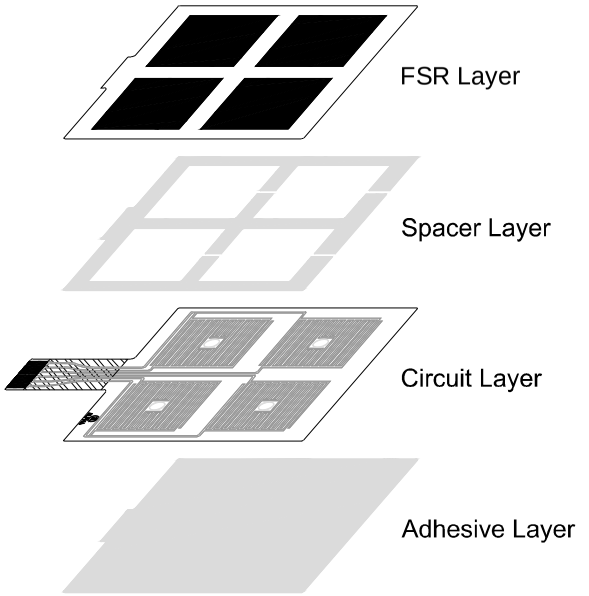
THIRD ANGLE PROJECTION







				TOL.UNILESS OTHERWISE STATED	DIMENSION	SCALE				DRAWING No.
△				less than 4 ±0.1 above 4~14 ±0.2 above 14~63 ±0.2 above 63~250 ±0.3 above 250~600 ±0.4	mm	1:1				MF22-N-064-A01
△										
△										
No.	DATE	DESCRIPTION	MODEL NAME							

TAIWAN ALPHA ELECTRONIC CO., LTD.

規格書

SPECIFICATION

Model name:MF22-N-064-A01

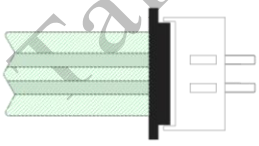
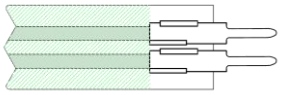
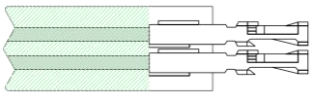
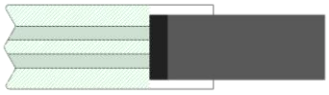
檢驗項目 Inspection Item	規格 SPEC.	備註 Notes
起始按壓力 Actuation Force	50g	
按壓力靈敏度範圍 Force Sensitivity Range	50~1000g(0.5~9.8N)	
解析度 Force Resolution	Continuous(Analog)	
有效區域 Active Area	28mm*28mm	
未按壓阻值 Stand-Off Resistance(Unloaded)	>20MΩ	
反應時間 Response Time	<1ms	
操作溫度 Operation Temp.	-20℃ to +70℃	
使用壽命 Life Cycle	1 million	Without Failure
厚度 Thickness	0.43±0.05mm	

Date：2015/8/17 Ver.：B

Membrane sensor usage tips

Please follow the below stipulate to avoid error conditions such as false triggering, false readings, pre-loading, or gouging and cracking of the sensor.

1. The side of adhesive should be used on the firm, flat and smooth surfaces, can't not be used on the curved surfaces. Also, be careful of trapped air bubbles or dirt particles when laminating the membrane sensor to surface, it cause the sensor to appear loaded in the absence of an external load. Recommended to clean the surface before adhesive.
2. Do not kink, bending or scratches the tail of membrane sensors. The traces should not be bent more than 90° as the silver conductive leads could break. Also, be careful if bending the tail near the active area. This can cause stress on the active area and may result in pre-loading and false readings.
3. Do not block the vent. This vent assures pressure equilibrium with the environment, as well as allowing even loading and unloading of the device. Blocking this vent could cause sensors to respond to any actuation in a non-repeatable manner.
4. Please use an overlay, such as a polycarbonate film or an elastomer, to prevent gouging of the membrane sensors from sharp objects.
5. Do be careful of kinks or dents in active areas. They can cause false triggering of the sensors.
6. Do not apply excessive shear force. This can cause delamination of the layers.
7. Do not exceed 1mA of current per square centimeter of applied force (actuator area). This can irreversibly damage the device.
8. The sensors are not designed for use under water. The sensors are not compatible with direct liquid contact. Sensors are ideally suited to placement behind a waterproof enclosure.
9. With flexible substrates, the solder joint will not hold and the substrate can easily melt and distort if solder directly to the exposed silver traces. Choose standard connection, such as FFC connector, solder tabs, female contacts, or female contact with housing connectors.

FFC Connector	Solder Tabs(pin)	Female contacts	Female contact with housing
			

Date：2015/8/31 Ver.：A