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A CMOS Mixed Mode Non-Linear Processing Unit for Adaptive Sensor Conditioning in Portable Smart Systems

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Abstract

This paper presents the architecture of a novel non-linear digitally programmable analog unit for sensor output conditioning in battery-operated smart systems. Designed in an 180nm 1.8V standard CMOS technology, by properly setting the 6-bit registers in the arithmetic unit, the voltage inputs are weighted before being processed by a non-linear circuit. Thus, a processing system consisting of a set of these devices suitably tuned and interconnected can be applied to condition a non-linear sensor, improving its behavior both in linearity and operating range, while reducing the effects of cross sensitivity. The robustness of the digital weight tuning is tested simulating a chip-on-the-loop training using a Levenberg-Marquardt-based algorithm. Electric simulations of the proposed unit and the results of its application in a complete neural network-based processing system to improve the linear operating range of a thermistor are presented.

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Keywords: artificial neural networks; CMOS; sensor calibration.

1. Introduction

Artificial neural networks (ANNs) are high flexibility computing tools that dynamically establish functional relationships between stimulus-response patterns without previous knowledge of the problem to solve. For its

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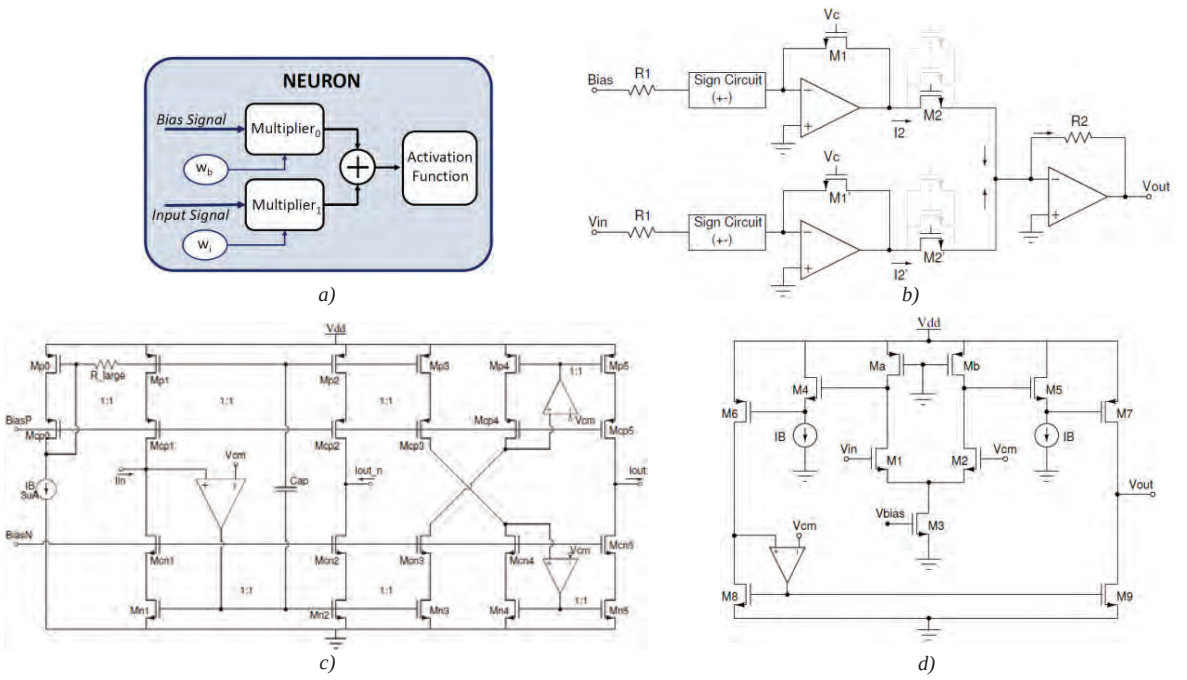


Fig. 1. a) Block diagram of a basic processor unit; b) Block diagram of a 2-input mixed multiplier; c) Sign circuit; d) Non-linear output circuit.

implementation in low-consumption modules, like wireless sensor nodes where operating life must be maximized, it is necessary to reduce even more the power consumption and the device size while keeping its adaptability [1]. To do so, the optimal solution is a mixed integrated implementation including analog processors –to minimize consumption and area– with digital programmability and storage, to facilitate reprogramming the neural network parameters. One example is the design of integrated conditioning and calibration modules for smart-sensors [2], where an analog neural system optimizes the sensor response before its digitalization, minimizing effects due to output drift, nonlinearities, aging and cross-sensitivity.

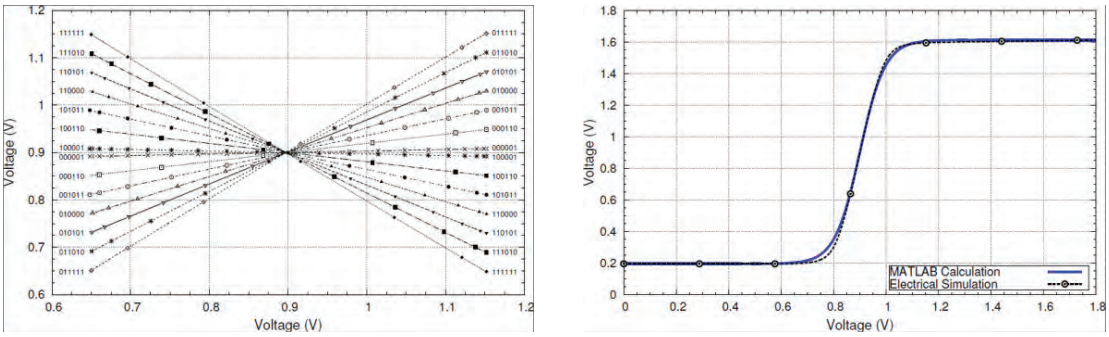
The objective of this work is the design of a 1.8V CMOS-based mixed mode non-linear processing unit for its application in portable sensor conditioning neural-based electronic architectures. This paper is organized as follows: in Section 2, the neuron structure and its main blocks are introduced; also, its electronic implementation is described, presenting some simulation results. Next, the high-level model is described. In Section 3, an application example is presented, where the linear operating range of a thermistor is improved. Finally, in Section 4, conclusions are drawn.

2. Processing Element Building Blocks

The basic processing unit (Fig. 1.a) consists of two main components: the mixed mode multiplier, responsible for weighting the analog input signals by a 5-bit digital coefficient; and the activation function, that provides a non-linear output from the processor weighted inputs. For an electronic implementation, CMOS technology is the most viable option as it is a low cost VLSI mature technology. In this work, design and implementation are done in a standard CMOS 0.18µm technology with 1.8V single supply.

2.1. Multiplier

Fig. 1.b shows the schematic of the analog-digital multiplier (ADM). It consists of a programmable gain amplifier (PGA) and a sign circuit (SC). PGA is a voltage amplifier, employing resistances and M_1-M_2 MOS transistors to set up the gain, these last operating as a MOS current divider (MCD) [3]. Thus, if both transistors are matched, the transfer function of this block is $V_{out}/V_{in} = R_2(W/L)_2/R_1(W/L)_1$. So, the activation coefficient (or gain) can be set by



a) *b)*

Fig. 2. a) Four-quadrant multiplier operation; b) Non-linear circuit behavior.

adjusting the size ratio of the transistors. To do this, single transistors are replaced by an array of x identical transistors in parallel, so that the equivalent MOS transistor width is xW.

In particular, weights are controlled by a 5-bit digital word $(B_4 \dots B_0)$, having 32 possible values between 0 and 1. The maximum gain is 1, so that every transistor M_1 is always on and operating in triode region, while M_2 transistors are controlled by the input digital word. The active cell is a class AB operational transconductance amplifier (OTA) with gain $G_{OTA} = 76\text{dB}$ and output resistance $R_{out} = 160\Omega$. Resistances values are $R_1 = R_2 = 18\text{k}\Omega$.

A sign circuit changes the current direction entering the PGA, thus allowing negative weights. Fig. 1.c shows the implemented sign circuit. It is a dynamic class AB current mirror [4], which provides two output branches: one for the forward current and the other for the inverted current, controlled by the sign bit B_5. Relative error in both output branches is below 1%; and total harmonic distortion (THD) remains below -80dB.

Fig. 2.a shows the simulation results of the proposed ADM for every input digital word, exhibiting a real four-quadrant multiplier operation. By setting the common mode voltage $V_{CM} = 0.9\text{V}$, voltage signals lower than this value are considered negatives, while higher are considered positives. Simulations were made using Cadence software for design and simulation of electronic integrated circuits. The maximum power consumption is 42.8µW under static operation, when the sign bit is '1'.

To sum up all the input weighted signals, currents are added by wiring together the transistors arrays before the second amplifier, as shown in Fig. 1.b.

2.2. Activation function

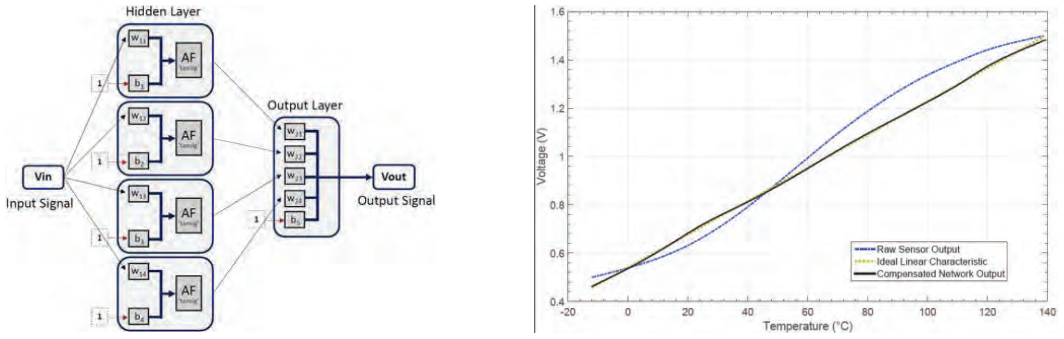
The activation function transforms the input value into an activation state within a range [0, 1]. This work implements a continuous and differentiable sigmoid function that allows using a back-propagation training algorithm. Fig. 1.d shows the implemented electronic circuit, with rail voltages range from 0.2 to 1.6V. It is a voltage amplifier made of a classic input NMOS differential pair with active loads M_a and M_b operating in linear region. The common mode voltage is set to V_{CM} by an auxiliary amplifier implemented with a differential pair.

Fig. 2.b shows the non-linear circuit behavior (black dot line) compared to an ideal hyperbolic tangent function (blue continuous line). The maximum absolute error is 0.04V, corresponding to the non-linear sections of the function. In this case, the static power consumption is 27.88µW.

2.3. High-level model

To simulate a full processing system based on the proposed elements, and its application to a realistic sensor compensation task, high level numerical models have been derived from electrical simulations by using MATLAB. In this way, the mixed mode multiplier operation can be described according to:

$$V_{out} = 0.90001 - (1.0298 \text{ x } 10^{-5}) \cdot V_{in} - (0.8969) \cdot w + (0.9983) \cdot V_{in} \cdot w \quad (1)$$



a) *b)*

Fig. 3. a) Simulated processing architecture; b) Raw sensor output voltage (blue) compared to compensated output (red).

Compared to the multiplier electronic operation (Fig. 2.a), this model has a mean square error $mse = 2.0641 \times 10^{-7}$. Concerning the transfer function, high level description is based on a look-up-table (LUT), giving better results than polynomial numerical approaches.

3. Application Example

The application feasibility to a sensor conditioning process has been verified by linearizing the output of a NTC thermistor placed on a resistive divider. The proposed neural network architecture is shown in Fig. 3.a. It is a multilayer network with 2 inputs, 1 hidden layer with 4 neurons and the output layer. The weights of this architecture are fitted by simulating a chip-in-the-loop Levenberg-Marquardt based algorithm [5], so the circuitry non-idealities are considered.

The results obtained are shown in Fig. 3.b. With quiescent power consumption lower than 668 µW, this architecture extends the linear output of the sensor up to 180% in the analog domain for a maximum error of ±1ºC, thus allowing an optimized data digitalization. Also, there is the possibility of applying the compensated output in control loops or actuation systems without requiring digitalization, so saving computational resources and response time.

4. Conclusions

In this work, the 1.8V-0.18µm CMOS mixed implementation of the main blocks conforming the basic processing unit of a neural network has been presented. It relies on a 6-bit multiplier (5 defining the weight and 1 controlling the operation sign) with a relative error below 1%, while for the activation function block, maximum absolute error is 0.04V. A high level model was completed and its feasibility was verified by extending the linear operating range output of a thermistor in a chip-on-the-loop Levenberg-Marquardt training with a power consumption below 668µW.

Acknowledgements

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