28820 - Electronic Technology II

Información del Plan Docente

Academic Year	2017/18
Faculty / School	175 - Escuela Universitaria Politécnica de La Almunia
Degree	424 - Bachelor's Degree in Mechatronic Engineering
ECTS	6.0
Year	3
Semester	First semester
Subject Type	Compulsory
Module	---

1.General information

1.1.Introduction

1.2.Recommendations to take this course

1.3.Context and importance of this course in the degree

1.4.Activities and key dates

2.Learning goals

2.1.Learning goals

2.2.Importance of learning goals

3.Aims of the course and competences

3.1.Aims of the course

3.2.Competences

4.Assessment (1st and 2nd call)

4.1.Assessment tasks (description of tasks, marking system and assessment criteria)

5.Methodology, learning tasks, syllabus and resources

5.1.Methodological overview

The Electronic Technology II course is designed as a set of contents, but distributed in four blocks. The first block, brings together basic concepts of Digital Electronics, numbering systems, etc. The second and third blocks make up the core that the subject must provide to the student's training. The final block, gathers further interesting complementary knowledge to complete the training in Digital Electronics.

The first three blocks will be dealt with under three fundamental and complementary ways: the theoretical concepts of

each didactic unit, the resolution of problems or questions and lab practice activities, supported in turn by another series of activities such as tutorials and seminars and will be tested individually, regardless of the blocks.

The fourth block will have a different treatment, because the students will work in groups only previously assigned sections, they will be able to express their preferences but all the subjects will have to be assigned to some group. They will prepare presentation materials and defend their work with a public presentation, which will be valued by the rest of the students and the teacher.

The teacher / student interaction is carried out in this way, through a distribution of work and responsibilities between students and teachers. However, it must be taken into account that, to a certain extent, students can set the pace of learning according to their needs and availability, following the guidelines set by the teacher.

The organization of teaching, involves the active participation of the student, and will be carried out following the following guidelines:

- Lectures: Theoretical activities imparted in a fundamentally expositive way by the teacher, in such a way as to expose the theoretical supports of the subject, highlighting the fundamental, structuring the concepts and relating them to each other.

- Practical lessons : The teacher solves problems or practical cases for illustrative purposes. This type of teaching complements the theory explained in the lectures with practical aspects.

- Seminars: The total group of lectures or practical lessons may or may not be divided into smaller groups, as appropriate. They will be used to analyze cases, solve problems, etc. Unlike what happens with the practical lessons, the teacher is not a protagonist, simply listening, counselling, clarifying, evaluating, assessing. It seeks to encourage student participation, as well as making the continuous assessment of students possible and to learn about the performance of learning.

- Lab Practice: The total group of lectures will be divided into several shifts, according to the number of students enrolled, but never with more than 20 students per shift, so that smaller groups can be formed. Students will carry out assemblies, measurements, simulations, etc., in the laboratories in the presence of the trainee teacher.

Practical activities are carried out in groups of two students (or at the most three students) per shift, although for the reports students of two or more shifts can be grouped. For each block, guidelines for practical tasks will be given (compulsory and optional); In addition, the reporting rules will be specified in a guidance document, which will be handed out at the beginning of the practical activities.

Group tutorials : Programmed activities of learning follow-up in which the teacher meets with a group of students to guide their work of autonomous learning and supervision of works directed or requiring a high degree of advice by the teacher.

- Individual tutorials : These are the ones made through the individual attention of the teacher in the department. They aim to help solve the doubts that students come across, particularly those who for various reasons cannot attend group tutorials or need more personalized attention. These tutorials can be classroom or virtual.

5.2.Learning tasks

Generic on-site activities:

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● Lectures : The theoretical concepts of the subject will be explained and illustrative practical examples will be developed as support for the theory when it is deemed necessary.

● Practical lessons : Problems and practical cases will be made as a complement to the theoretical concepts studied.

● Practical tasks : Students will be divided into several groups of no more than 20 students, being guided by the tutorial action of the teacher.

● Defense and presentation of topics: on the particular contents that are assigned to each group of students, corresponding to Block 4

Generic off-site activities:

● Study and assimilation of the theory explained in the lectures.

● Understanding and assimilation of solved cases in practical lessons.

● Preparation of seminars, solving suggested problems, etc.

* Participation in Forums of the subject via Moodle, to provide links of information on the

Internet.

● Preparation and development of scripts and corresponding reports.

● Preparation of written continuous assessment tests, and global assessment tests.

Autonomous tutored activities:

Although they will be done on-site, they have been taken into account separately because of their particular features, they will be focused mainly on seminars and tutorials under the supervision of the teacher.

Reinforcement activities: Off-site activities preferably, via the virtual portal of teaching (Moodle), will be designed to reinforce the basic contents of the subject. These activities can be personalized or not.

5.3.Syllabus

The theoretical contents are divided into four blocks (numbers 1 to 4) preceded by a block 0 of introduction to Digital Electronic Technology. The choice of the content of the blocks has been made looking for the express clarification of the final objective, so that with the union of incidental knowledge, the student obtains a structured knowledge, easily assimilated for the Mechatronics Engineers.

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Each of the blocks is composed of topics, on a weekly basis, one per course week. These topics include the contents necessary for the acquisition of predetermined learning outcomes.

5.3.1. Theoretical contents

Block 0: INTRODUCTION

* Overview of Digital Technology. Components, Functions, Manufacturing techniques, Integration levels.

* Conceptual maps

Block 1: INTRODUCTION TO DIGITAL TECHNIQUES

1.- Basic elements of digital technology

* Numbering systems

* Binary codes

* Boolean Algebra

* Logical doors

2.- Digital Integrated Circuits

* Techniques and manufacturing processes

* Digital technologies and families. Interface

* Technical parameters. Logic levels, delays, speed, etc.

3.- Combinational Logical Design Methods

* Logical gates: Karnaugh methods.

* Integrated circuits with logic gate function

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* Integrated circuits with O-Exclusive function

* O-Exclusive Function: Venn Boards

* Application design and implementation

Block 2: ANALYSIS AND DESIGN OF COMBINATIONAL LOGIC CIRCUITS

4.- Encoders and Decoders

* Integrated circuits with encoder-decoder functions

* Decoder: Summations and positive-negative logic

* Application design and implementation

*** 7-segment BCD and ASCII decoders**

5. Multiplexers and Demultiplexers

* Integrated circuits with Multiplexor-Demultiplexor functions

* Multiplexers: State setting tables

* Application design and implementation

6.- Other Combinational Functions

* Comparators

* Arithmetic circuits

* Parity Generators-detectors

Block 3: ANALYSIS AND DESIGN OF SEQUENTIAL LOGIC CIRCUITS

7.- Basic and synchronized bistables

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* RS bistable and other performances

* Status maps and symbols

* Design and time schedules

* Synchronization by levels and flanks

* JK / Master-Slave

* D / Edge-Triggered

* T-mode behaviors

8.- Digital Counters and Digital Records

* Asynchronous counters and synchronous counters

* Account Modes. Design Processes

* Sequencer counters. Universal counter

* Storage and displacement records

* Serial / parallel inputs. Serial / parallel outputs

* Left / right shift.

* Universal Record. Accumulating Record.

9.- P.L.D and A.S.I.C. Matrix architectures

* Programmable Logic Devices (PLD)

* Evolution of PLDs: PAL, PLA, GAL, Macro-cells, ...

* FPGA, LCA-RAM, EPLD, CPLD, ...

* Development processes with PLD

* Hardware description languages (HDL)

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* Application-Specific Integrated Circuits (ASIC)

* Gate-Array, Standard-Cell, Full-Custom

Block 4: HIGH-DIGITAL INTEGRATION DIGITAL DEVICES

10.- Semiconductor memories

* Architecture: Cells, Addressing

* Volatile memories: Statics and Dynamics

* Non-volatile memories: from ROM to Flash

11.- A / D and D / A Converters

* Direct Digital Analog Converters

* Feedback Analog Digital Converters

* Digital Analog Converters

12.- Computer Systems

* Microcomputers

* Microprocessors

* Programmable Logic Controllers (PLCs)

5.3.2. Practical contents

Each block exposed in the previous section has associated practices in this regard, either through practical assumptions and / or physical or simulated assembly work leading to obtaining results and their analysis and interpretation. As the topics are developed, these Practices will be proposed, preferably in the classroom and also through the Moodle platform.

Practices to be developed in the Laboratory are given below. They will be carried out by the students in one-hour sessions, except in the final practice, in which the three hours of Block 4 are accumulated

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PRACTICE 1: ASSOCIATED WITH BLOCK 1

Exercise 1: Code Changing and Multisim Simulator handling

Use of the logic converter instrument

Use of the word-generating instrument

Using the Logical Analyzer Instrument

Exercise 2: Consultation and interpretation of technical information of digital integrated circuits

Date Query of digital components in PDF

Access to the library data of the simulator Multisim

Measurement of logic levels and delay times in logic inverters

Exercise 3: Design and Simulation Exercises by Karnaugh and O-Exclusive

Logical design processes with the Karnaugh method

Capture of NAND / NOR gates in the simulator.

Logical design processes with the O-Exclusive method

Schemes of NAND / NOR and O-Ex gates in the Multisim simulator

Simulation in Multisim, compiling and checking on Digilent Basys-2

PRACTICE 2: ASSOCIATED WITH BLOCK 2

Exercise 1: Decoder Design and Simulation Exercises

Logical design processes with the Decoder method

Capturing NAND / NOR and Decoder gates in the simulator.

Simulation in Multisim, compiling and checking on Digilent Basys-2

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Exercise 2: Designing and Simulating Exercises by Multiplexers

Logical design processes with the Multiplexers method

Capturing diagrams with multiplexers in the simulator.

Simulation in Multisim, compiling and checking on Digilent Basys-2

Diagram Mounting with Multiplexers and Checking the Operation

Exercise 3: Simulation and / or assembly of other combinational functions

(One among the following)

Digital Comparators

Adder / Subtrator. ALU

BCD / 7-segment decoder

Parity_Detector_Generator

PRACTICE 3: ASSOCIATED WITH BLOCK 3 exercises

Exercise 1: Bistable Design, assembly and simulation

Assembling the RS bistable with NAND and / or NOR gates and checking

Verification of level synchronized bistables (RS-clock, D-clock)

Connection of D-latch bistables (storage register)

Checking JK / Master-Slave and D-Edge-Triggered bistables

JK bistable Cascade mounting in T-mode.

Simulation in Multisim, compiling and checking on Digilent Basys-2

Exercise 2: Counter and Register Application Design and Assembly

Digital Counter Connection such as timer or clock

Checking Universal Counter Functions

Shift Register Architecture

Serial / parallel and parallel / serial conversion

Checking universal register functions

Simulation in Multisim, compiling and checking on Digilent Basys-2

Exercise 3: Application Development with programmable logic devices

HDL Description for Digital Application

Compilation and simulation

Recording of the PLD. Physical verification of operation

PRACTICE 4: ASSOCIATED WITH BLOCK 4

Assembly, setting and documentation of one of the applications related to topics 10 to 12, depending on what is assigned for theoretical defense, so that most of the digital functions studied are used.

5.4.Course planning and calendar

5.4.1. Temporary distribution of a teaching week:

The subject is defined in the Verification Report of the Degree with a low experimental grade, so that the 10 hours a week are distributed as follows:

*** Theory-practical classes** : 3 hours a week (blocks 1, 2 and 3)

5 hours per week (block 4)

*** Practice tasks** : 1 hour per week

*** Other activities** : 6 hours per week (blocks 1, 2 and 3)

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4 hours per week (block 4)

5.4.2. Test schedule

For the assessment tests, described in the continuous assessment process, the following schedule is suggested:

*** Week 3:** Test 1 (Topics 1, 2 and 3)

*** Week 7** : Test 2 (Topics 4, 5 and 6)

*** Week 12** : Test 3 (Items 7, 8 and 9)

5.4.3. Presentation-Defense of Works

The ones belonging to Block 4 (Digital devices of high scale of integration), will be tested orally during the three final week of the course, depending on the number of students and the specific development of the preparatory tasks.

5.5.Bibliography and recommended resources

Basic bibliography:

BLANCO C. **Fundamentos de Electrónica Digital.**

Thomson-Paraninfo 2005, ISBN: 84-9732-342-4

Further Reading:

"THE UPDATED BIBLIOGRAPHY OF THE SUBJECT IS CONSULTED THROUGH THE LIBRARY'S WEB PAGE http://psfunizar7.unizar.es/br13/ eBuscar.php? Tipo=a

Resources:

Theory Notes, PWP presentations, typical problems and Web links, all related to the syllabus, will be provided through the Moodle page of the subject.

Digital circuit simulation software and PLD development (Multisim) and manuals for their use, will be installed in computer room or Laboratory PCs. Download and installation in the personal computers of students will be allowed.

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PCs, Multimeters, Oscilloscopes, Function Generators, Power Supplies, discrete and integrated electronic components, must be part of the Electronics Lab equipment.