A Robust 10-Gb/s Duobinary Transceiver in 0.13-μm SOI CMOS for Short-Haul Optical Networks

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***Abstract*—Duobinary modulation is a robust and attractive coding format for high-speed serial data transmission because it allows an excellent tradeoff between speed, noise and power. However, conventional architectures reported in the literature performing the necessary precodification in a duobinary transceiver suffer from a severe vulnerability to glitches that limits their performances at high data rates. This study presents a new precoder scheme that overcomes this limitation with a very small design, area and power consumption, and a time-domain analysis that confirms the advantages of the proposed solution. The proposed precoder has been implemented in a full duobinary transceiver fabricated in a 0.13-μm partially depleted-silicon on insulator CMOS technology that works at 10 Gb/s. The fabricated precoder consumes 13.8 mW and the decoder consumes 23.2 mW from a single supply of 1.2 V. Experimental results are provided for a simulated channel of 50-m plastic optical fiber.**

***Index Terms*—Analog signal processing, duobinary modulation, graded index POF (GI-POF), high-speed communications, multilevel modulation, SOI-CMOS.**

I. Introduction

DATA traffic in industrial environments increases at a dizzying pace. Applications of serial communications, such as ambient parameter monitoring, chip-to-chip interconnections or industrial Ethernet networks, among many others, are a constant challenge for optimizing the performance and the reliability of the communication link [1]–[3]. This is why the use of techniques to exploit the channel bandwidth such as equalization [4] or signal modulation [5] is required. In this scenario, a very interesting option is the use of amplitude modulation, where three schemes are the most widespread: non return to zero (NRZ), *n*-level pulse amplitude modulation and duobinary.

It is commonly agreed that, among them, duobinary modulation offers the best tradeoff between the three most important figures of merit of a modulation scheme: data rate, signal to noise ratio (SNR) and power consumption [5], [6]. Both duobinary and 4-PAM achieve double data rate compared to NRZ. However, 4-PAM is affected by a higher SNR degradation, producing many more errors than duobinary at high data rates. Moreover, the circuitry needed to perform duobinary modulation consumes less power than that of 4-PAM [6].

The key in duobinary modulation is to take advantage of the intersymbol interference (ISI) caused by the limited bandwidth of the channel, assuming that all the received symbols suffer from it. When an NRZ signal is sent through a band-limited channel, so that its spectrum covers frequencies beyond the channel bandwidth, ISI distorts the signal linearly [7]. If

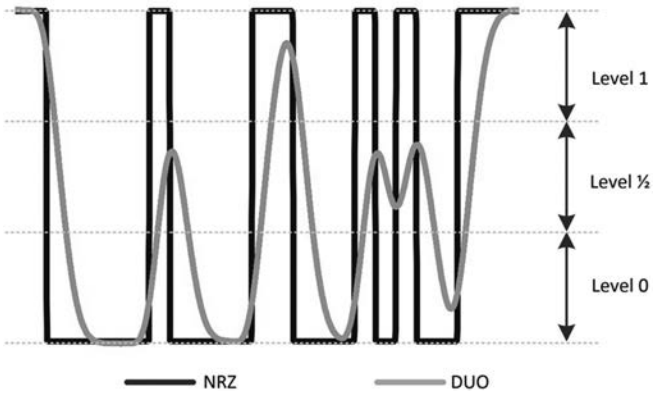

Fig. 1. Transient response of a signal before (NRZ) and after (DUO) passing through a band-limited channel.

TABLE I
DUOBINARY SIGNAL GENERATION PROCESS

NRZ(t-T_b)	NRZ(t)	DUO(t)
0	0	0
1	1	1
0	1	½
1	0	

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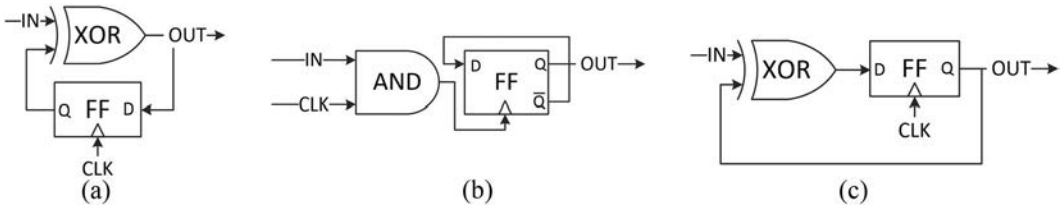

Fig. 2. Block diagram of (a) conventional XOR-based precoder, (b) AND-based precoder, and (c) proposed modified XOR-based precoder.

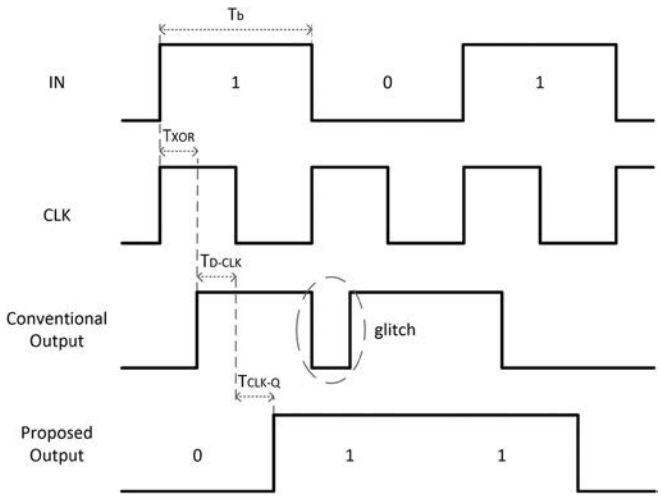

Fig. 3. Waveforms of the most relevant signals in the duobinary XOR-based precodification process. From top to bottom: input NRZ data stream, clock signal, conventional output taken in the XOR gate, and proposed output in the FF.

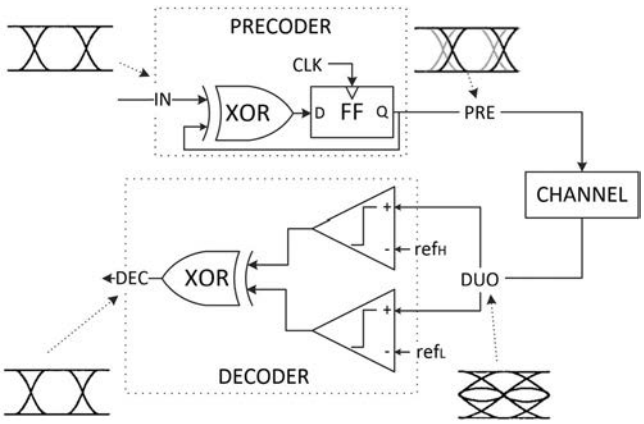

Fig. 4. Block diagram of the proposed duobinary transceiver.

this output signal, whose eye diagram is completely closed, is treated as an NRZ signal, it will be impossible to recover. On the contrary, assuming that the signal has ISI so that the value of the *n*th bit of the output depends on the value of both *n*th and *(n – 1)*th bits of the input, the output can be processed as a three-level signal, as depicted in the waveforms of Fig. 1. Table I indicates how the three levels of the duobinary signal (DUO) are created in a band-limited channel, as a function of the NRZ input bits.

A feasible duobinary transceiver needs two blocks for a correct operation: a precoder in the transmitter and a decoder

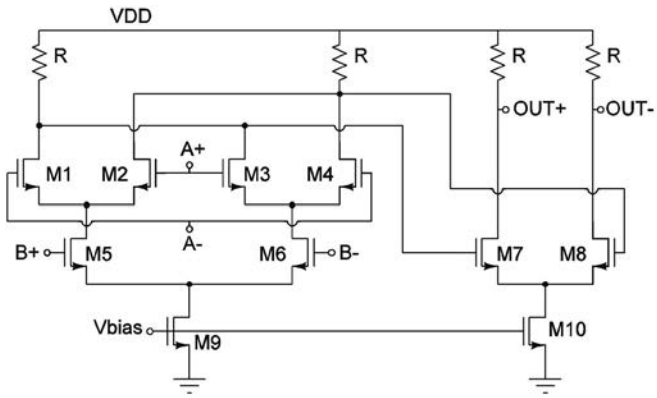

Fig. 5. Schematic of the proposed SCL XOR gate.

in the receiver [6]–[11]. In the literature, several precoder architectures are reported. On one hand, XOR-based precoders are only implemented at system level [8] due to its glitch vulnerability in circuit implementations. On the other hand, AND-based precoders have intrinsically limited speed [9], [10]. Moreover, other papers report complex methods for precoding the signal before a serializer, which enhances the data rate at the cost of design complexity, power, and area consumption [6], [11].

This study proposes a new solution, which is based on the XOR-based structure but does not generate glitches and achieves excellent energy efficiency with small area consumption, improving the reported schemes.

Based on the results of this study, a duobinary transceiver has been implemented in a 0.13-μm 1.2-V partially depleted (PD) silicon on insulator (SOI) CMOS technology. It achieves 10 Gb/s, allowing the use of graded index POF (GI-POF) channels for multigigabit applications with large core diameter (up to 1 mm).

It is worth mentioning that PD-SOI is a very interesting technology for high-speed analog electronics [12]. The silicon wafer contains a layer of silicon oxide of a few hundreds of nanometer that isolates the active elements from the rest of the silicon substrate. This insulation avoids the leakage current typical of bulk Si technologies, which is the cause of several reliability problems, especially in the elevated temperature range. In addition, SOI technology avoids the creation of parasitic NPN and PNP transistors formed by adjacent regions in the substrate, eliminating latch-up failures. The buried oxide layer also yields advantages in terms of radiation hardness against single events, but more importantly for the present application: parasitic capacitances and HF crosstalk through

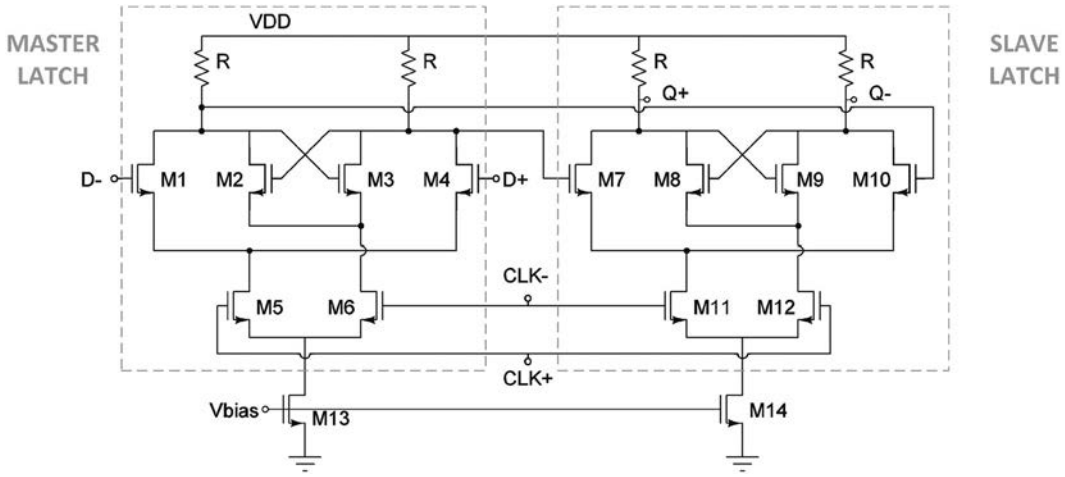

Fig. 6. Schematic of the proposed SCL Flip Flop.

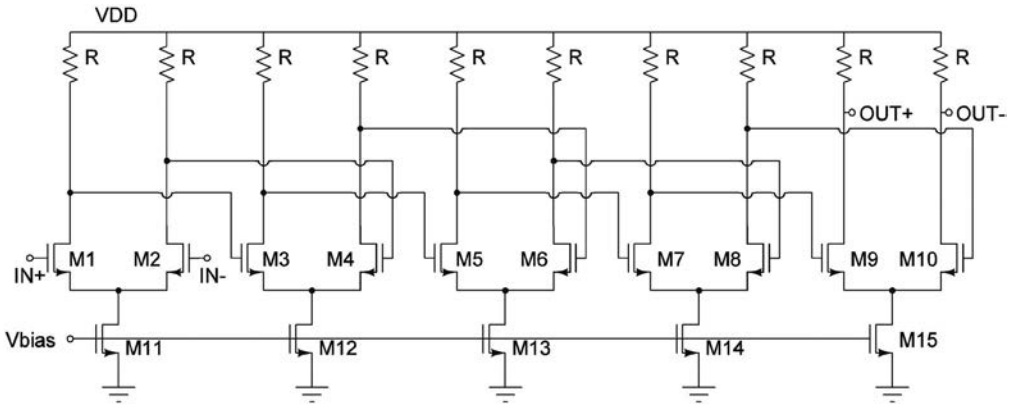

Fig. 7. Schematic of the proposed SCL voltage comparator.

the substrate. Consequently, it is commonly recognized that PD-SOI can bring a reduction of power or an improvement of frequency performance by about 30% over bulk CMOS technology at the same transistor size [13].

This paper is organized as follows. Section II presents the improved precoder technique. Section III describes the main blocks of the proposed architecture. Section IV details the most relevant results. Finally, Section V summarizes the conclusions.

II. Duobinary Precodification

There are two conventional structures to implement a duobinary precoder in a serialized signal: XOR-based and AND-based precoders. The first one is formed by an XOR gate with a feedback loop through a flip-flop (FF), Fig. 2(a). Its major drawback is that it needs a very precise adjustment of the delay time of the cells to ensure a correct operation. Otherwise, the output produces glitches, which ruins the final result. The second structure is formed by an AND gate and a divide-by-2 frequency divider, Fig. 2(b). It avoids the global feedback loop, which removes the restrictions in the time domain. However, it presents a drawback, which is that the AND gate must be able to work at double data rate than the rest of the cells, since

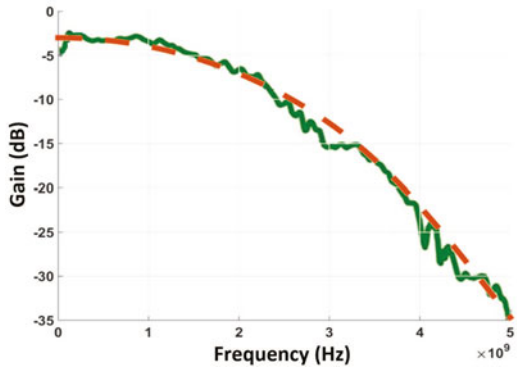

Fig. 8. Modified frequency response of a 50-m 1-mm GI-POF link (solid line) and ninth-order low-pass Bessel filter (dashed line).

one of its inputs is the clock signal, limiting the maximum data rate of this type of precoders. This study proposes the use of the XOR-based architecture but considering that the output of the system is not the output of the XOR gate, but the output of the FF, as shown in Fig. 2(c). This simple and reliable solution, which has not been reported in the literature, solves the issue of the glitches that is found in the conventional structures and relaxes the constraints in the time domain.

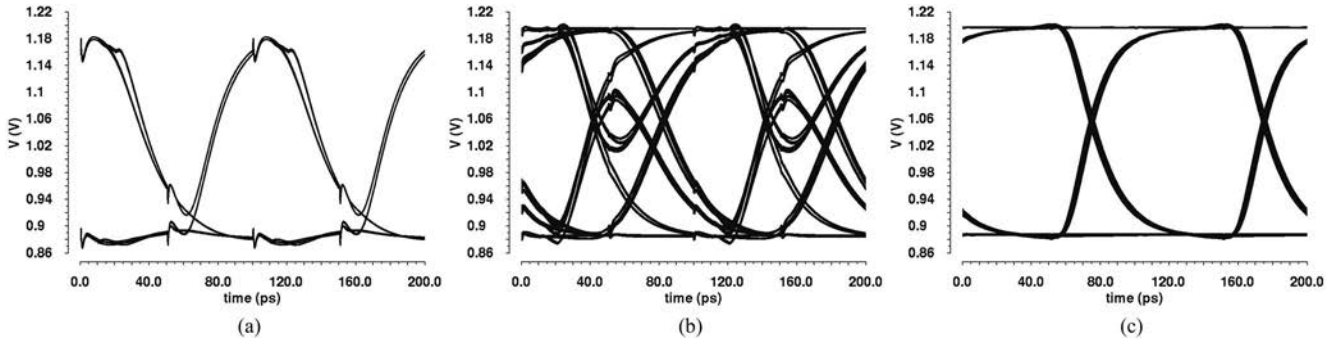

Fig. 9. Simulated eye diagrams of output signals for: (a) AND gate in an AND-based precoder, (b) conventional XOR-based precoder, and (c) proposed XOR-based precoder.

TABLE II
PROCESS CORNER ANALYSES RESULTS AT 27 °C

		Min.	Typ.	Max.
PRE	Eye aperture (mV)	238	294	353
	Jitter (ps)	3.9	4.2	6.7
DEC	Eye aperture (mV)	248	306	365
	Jitter (ps)	21.4	27.2	37.1

TABLE III
TEMPERATURE SIMULATION RESULTS

		−40 °C	27 °C	85 °C
PRE	Eye aperture (mV)	274	294	322
	Jitter (ps)	5.0	4.2	4.9
DEC	Eye aperture (mV)	270	306	352
	Jitter (ps)	28.3	27.2	30.4

The next paragraphs present an analysis of the design constraints of the conventional XOR-based precoder and how they can be hugely relaxed by means of the modified XOR-based precoder proposed in this paper. We define T_{XOR} as the delay in the XOR gate and T_{D-Q} as the delay in the FF, which in turn can be divided into two components: $T_{D-\mathrm{CLK}}$ is the time that passes since the input D experiences a change until the clock flags the sample instant; and $T_{\mathrm{CLK}-Q}$ is the delay between the sample instant and the toggle in the output

$$T_{D-Q} = T_{D-\mathrm{CLK}} + T_{\mathrm{CLK}-Q}. \tag{1}$$

In the conventional structure [see Fig. 2(a)], a necessary condition must be perfectly achieved: the sum of the delay times of the whole feedback loop must be 1-bit period T_b

$$T_{\mathrm{XOR}} + T_{D-Q} = T_b. \tag{2}$$

If (2) is not satisfied, the output signal contains glitches that ruin the final result. The duration of the glitches, T_g, is the difference between the bit period and the loop delay

$$T_{\mathrm{g}} = \left| T_b - T_{\mathrm{XOR}} - T_{D-Q} \right|. \tag{3}$$

On the contrary, in the proposed structure [see Fig. 2(c)], the FF samples the signal once for every bit, so the glitches

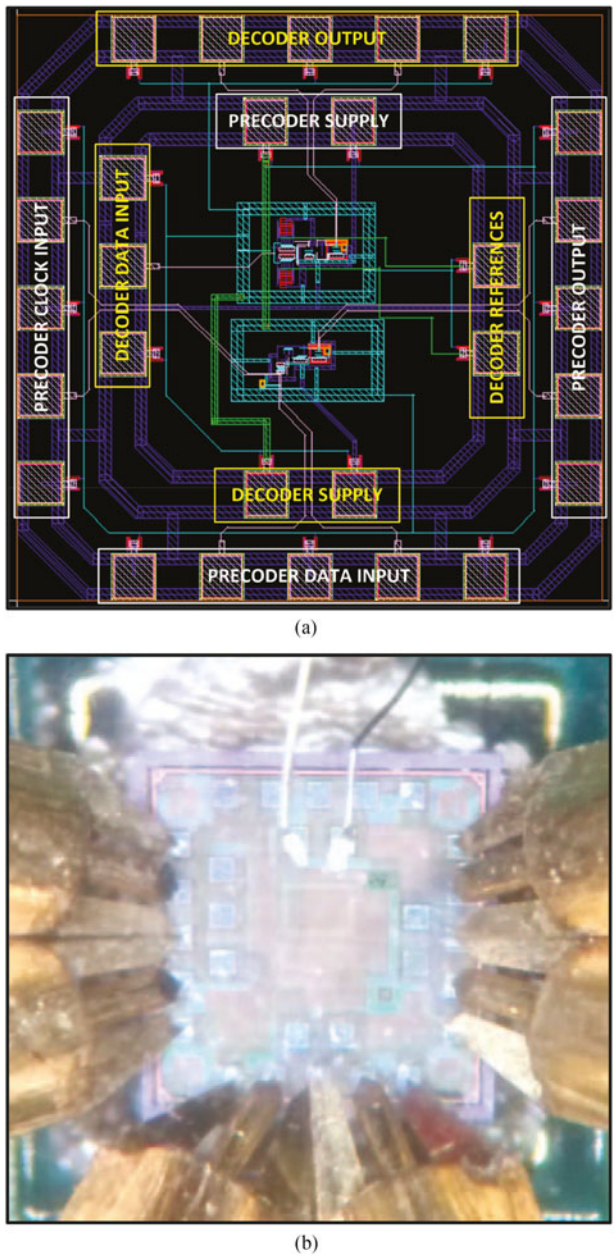

Fig. 10. (a) Screenshot of the full floorplan and (b) photograph of the fabricated die and the precoder on-wafer test setup with GSGSG probes.

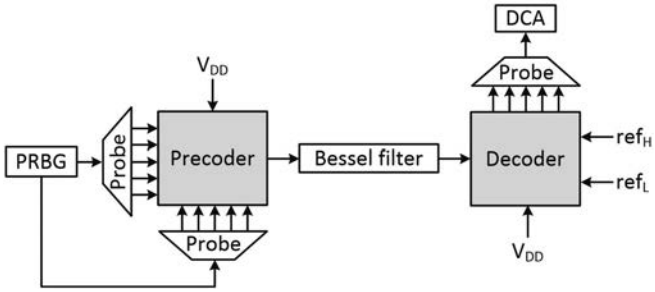

Fig. 11. Block diagram of the experimental setup.

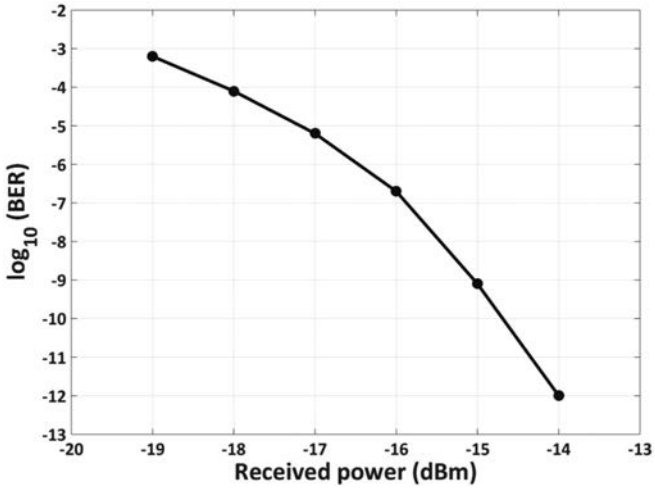

Fig. 12. Bit error rate versus received 10 Gb/s 2^{31}–1 PRBS input signal.

disappear. To achieve a correct operation, the conditions that must be satisfied are

$$T_{\text{XOR}} + T_{D-Q} < 2\,T_b \tag{4}$$

$$T_{\text{XOR}} + T_{\text{CLK}-Q} \leq T_b. \tag{5}$$

While in the conventional structure the delay times have to be perfectly adjusted, in the proposed structure it is enough to minimize them and, even so, the requirements of the circuits are more flexible than in the conventional case. Fig. 3 illustrates how the conventional XOR-based precoder produces glitches when the loop delay is not perfectly adjusted and how the solution proposed in this paper overcomes this limitation.

III. Circuit Design

To demonstrate the correct operation of the proposed precoder, a full duobinary transceiver including a precoder and a decoder has been designed and fabricated. Fig. 4 shows the block diagram of the proposed duobinary transceiver. All the cells have been implemented in the H9SOI-FEM 0.13-μm CMOS technology from STMicroelectronics. Source coupled logic (SCL) cells have been chosen because they can operate at a data rate 30% higher than standard CMOS logic cells for the same technology [10]. SCL cells are built concatenating differential pairs, in such a way that every pair of transistors must be always excited by a differential signal. Typical values for such pairs are $\text{W/L} = 10\,\mu\text{m}/0.13\,\mu\text{m}$ for the transistors, $500\,\Omega$ for the resistors and current sources of 1.5 mA, achieving cells with a bandwidth of 16 GHz and a potential fan-out of 10. All transistors have their body connected to source to avoid floating-body effects in PD-SOI technology.

A. Precoder

The precoder has been implemented by means of the structure proposed in the previous section, with an XOR gate and a FF. Its block diagram is shown in the precoder box in Fig. 4. The input data signal and the output of the FF enter an XOR gate, whose output goes to the input of the FF, which is driven by the clock signal. The schematic of the proposed SCL XOR gate is shown in Fig. 5. The data signal IN goes to the input A, whereas signal PRE is connected to input B. Transistors M1–M6 perform the logic operation and the output differential pair M7–M8 increases the bandwidth of the cell. Transistors M9–M10 carry out the source current that biases the cell. The FF has been implemented with two D-latches in master-slave configuration, and its schematic is shown in Fig. 6. Each latch, M1–M6 and M7-M12, is formed by two differential pairs, one of which is cross-coupled.

B. Decoder

The function of the decoder in a duobinary transceiver is the recovery of the original data sequence from the three-level duobinary signal that comes from the channel. In this study, the decoder has been implemented with a topology formed by a window comparator and an XOR gate. The block diagram is shown in the decoder box of Fig. 4. Both voltage comparators used to implement the window comparator are formed by five differential amplifiers connected in cascade, as can be seen in Fig. 7, achieving the required slew-rate of 25.9 V/ns. The noninverting input of both comparators is connected at the signal DUO, which is the channel output signal. On the other hand, the inverting inputs, ref_H and ref_L, are connected to voltage references. The level of ref_H must be set between the corresponding logic levels 1 and ½ of the DUO signal, whereas the level of ref_L must be established between the 0 and ½ logic levels. The XOR gate structure is the same as that of the precoder, whose schematic is shown in Fig. 5.

C. Channel

Since a duobinary signal is defined as the mean value of the nth and the $(n-1)$th bits of the input, a channel in the z-domain can be expressed as $1+\ z^{-1}$ [9]. A feasible way of implementing this function is a low-pass Bessel filter with an order between fifth and ninth and a bandwidth between $0.2/T_b$ and $0.3/T_b$ [14]. Despite the fact that not all channels present optimum characteristics to be used with duobinary modulation, the features of the channel can be adapted with the corresponding transceiver front-end (including pre-emphasis, equalizer, etc.) to satisfy these requirements. The test setup of this work includes a ninth-order low-pass Bessel filter with 2.2-GHz bandwidth. This configuration has been chosen because it is similar to the

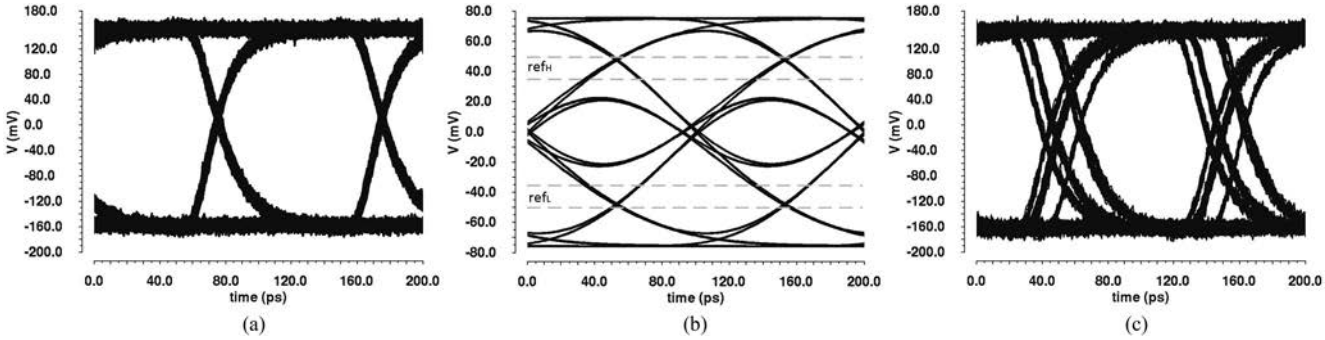

Fig. 13. Experimental eye diagrams of different stages through the transceiver with the proposed precoder: (a) precoder output, (b) channel output, and (c) decoder output.

GI-POF link reported in [15], but the bandwidth has been enhanced up to 2.2 GHz in order to be able to test the transceiver up to 10 Gb/s. Fig. 8 shows the transfer functions of the implemented Bessel filter and the measured modified GI-POF link.

IV. Results

First of all, we are going to demonstrate that the proposed precoder is the most reliable solution among the three precoder architectures described in Section II when the data rate is as high as 10 Gb/s. For that purpose, a set of transistor-level simulations has been carried out. Fig. 9(a) shows the signal of an AND-based precoder at the AND output when it operates at 10 Gb/s. Since the clock signal changes twice a bit period, the AND output should be able to do the same, what makes this system more likely to produce errors in the following frequency divider.

Fig. 9(b) and (c) show the operation of the XOR-based precoder architecture. Fig. 9(b) is the eye diagram taking the conventional output, whereas Fig. 9(c) shows the signal eye diagram at the proposed output. As it can be seen, the output signal of the conventional precoder is full of glitches that ruin the result. However, the proposed solution filters all those glitches, presenting an eye diagram completely open. The transceiver has been found functional for all the corner analyses available in the technology, with a variation of 20% in the vertical aperture of the eye diagrams, due to the variation suffered by the current sources of the cells. The decoder jitter suffers a high variation since it is dominated by the asynchronous comparisons carried out by the voltage comparators. The main results of the process corner analyses and temperature simulations in the range from -40 °C to 85 °C are presented in Tables II and III, respectively.

Finally, the experimental results of the fabricated prototype are presented. Fig. 10(a) shows a screenshot of the floorplan. It has been designed to contain both the precoder and the decoder in the same die of 1 mm^2. Fig. 10(b) shows the photograph of the fabricated die while the precoder is tested in a probe station. The two microwires on the top are soldered to a printed circuit board that biases the ICs, whereas the three differential probes on the left, right, and bottom carry the input and output signals. The low-pass Bessel filter has been implemented with passive elements matched to 50 Ω at both the input and the output and it is placed between the output of the precoder and the input of the decoder. The prototypes have been tested for 10 Gb/s with a pseudorandom bit sequence of $2^{31}-1$ bits using a pseudo-random bit generator Picosecond 12050 and a digital communications analyzer (DCA) Agilent Infiniium DCA-J 86100C, with the experimental setup depicted in Fig. 11. During the test of the full transceiver, two dies have been used, one for the precoder and a different one for the decoder. DC signals and connections with the filter have been made with microwires soldered to the dies, whereas probes have been used for the precoder inputs and the decoder outputs. Fig. 12 shows the bit error ratio (BER) performance of the decoder, which has been estimated from the Q factor of the eye diagrams, and presents a value of 10^{-12} for a received power of -14 dBm.

Fig. 13 shows the eye diagrams through the transceiver at 10 Gb/s decoupled of their dc components: Fig. 13(a) shows the precoder output, presenting an RMS jitter of 4.7 ps and a vertical aperture of 278 mV. Fig. 13(b) shows the decoder input, which is a duobinary signal. Finally, the decoded signal is represented in Fig. 13(c). For an optimal performance of the decoder, the voltage references of the comparators are fixed with temperature compensated voltage references. Fig. 13(b) contains two regions delimited by dashed horizontal lines, 15-mV width each, in which ref_H and ref_L have to be set. The RMS jitter in this eye diagram is 28 ps and the vertical aperture 245 mV. For comparison, Fig. 14 shows the eye diagrams through the transceiver using the conventional XOR-based precoder. The precoder output is completely damaged by glitches, so the same happens with the following stages.

Table IV compares the performance of this transceiver with other reported CMOS duobinary precoders and transceivers. The features of both precoder (TX) and decoder (RX) have been separated in order to highlight the advantages of the proposed precoder architecture. Since [6] and [11] report duobinary precoders, they lack the receiver part. The energy efficiency, in J/bit, is defined as the ratio between the power and the data rate. The experimental uncertainty in the calculation of the energy efficiencies is below 2%. It is worth highlighting that, in this study, the energy efficiency of the precoder is improved to 1.38 pJ/bit with small area consumption, thanks to the power saving advantages of PD-SOI CMOS technology and the new precoder architecture featuring low design and area overheads.

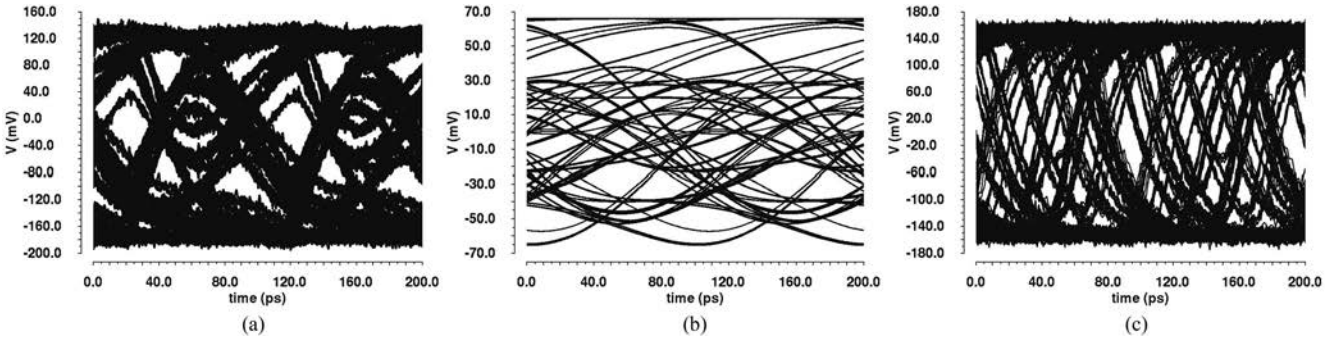

Fig. 14. Experimental eye diagrams of different stages through the transceiver with the XOR-based conventional precoder: (a) precoder output, (b) channel output, and (c) decoder output.

TABLE IV
SUMMARY OF RESULTS

	[6]		[9]		[10]		[11]		This work	
Technology	90 nm CMOS		90 nm CMOS		0.18 μm CMOS		0.18 μm CMOS		0.13 μm PD-SOI CMOS	
Data rate (Gbps)	20		20		3.125		10		10	
Precoder architecture	Pre-serializer		AND-based		AND-based		Pre-serializer		Modified XOR-based	
Supply voltage (V)	1		1.5		1.8		1.8		1.2	
	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX
Power (mW)	122	N/A*	120	75	10.1	17.8	20	N/A*	13.8	23.2
Energy efficiency (pJ/bit)	6.1	N/A*	6	12.5	3.2	5.7	2	N/A*	1.38	2.32
Area (mm^2)	0.17	N/A*	0.21	0.11	N/A*	N/A*	0.035	N/A*	0.006	0.016

*N/A: Not available.

V. CONCLUSION

This study presents a duobinary transceiver fabricated in 0.13-μm PD-SOI CMOS technology. This transceiver uses a new precoder architecture, which overcomes the disadvantages of the other architectures reported in the literature, avoiding the appearance of glitches and achieving robust operation. The proposed transceiver reaches 10 Gb/s, enabling its use in multigigabit applications such as short-reach GI-POF channels. Simulation results already revealed the advantages in terms of glitch robustness of the proposed scheme against the conventional one. Finally, an experimental characterization made with several prototypes is presented that demonstrates robust operation of the proposed duobinary transceiver at 10 Gbps consuming 37 mW from 1.2 V single supply, 13.8 mW corresponded to the precoder and 23.2 mW to the decoder. The full transceiver exhibits a competitive energy efficiency of only 3.7 pJ/bit. A bit error ratio of 10^{-12} for -14 dBm received power has been obtained by using an electrical equivalent model for 1-mm 50-m GI-POF channel.

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