Integrated All-Optical 2-Bit Decoder Based on Semiconductor Optical Amplifiers

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ABSTRACT
In this paper, the architecture of an SOA-based N-bit decoder, with minimum number of SOAs using Cross-Gain Modulation (XGM), is described. A 2-bit decoder is integrated under Multi-Project Wafer (MPW) photonic foundries in indium phosphide (InP) technology. Its output signals are analysed off chip and its performance is evaluated at 10 Gbps with RZ amplitude-modulated signals.
Keywords: semiconductor optical amplifiers, all-optical logic, XGM, decoder, InP.

1. INTRODUCTION

All-optical data processing is a highly desirable technology for optical telecom, since it may allow avoiding opto-electronic and electro-optic conversion, improving speed and network transparency. Nowadays some degree of processing can be present in optical networks, such as wavelength conversion and optical regeneration but their applications are very limited due to the lack of interaction with the signal data. In the last years photonics have demonstrated the capability of performing simple logic operations at very high-speed, mainly by exploiting different non-linear effects of semiconductor optical amplifiers (SOA), such as Four-Wave Mixing (FWM) [1], Cross Gain Modulation (XGM) [2, 3] and Cross Phase Modulation (XPM) [4]. These effects occur in several non-linear optical media, but are particularly efficient in Semiconductor Optical Amplifiers (SOA), limiting their potential for in-line amplification but also enabling their use for optical processing. Taking advantage of these effects several logic gates such as NOT, XOR [3], AND and NAND have been reported in literature, individually or in combination with others, in parallel or in cascade. Larger scale logic like encoders and decoders was simulated in [5,6] and an optical encoder based on Cross-Polarization Modulation (XPolM) with SOAs was demonstrated in [7]. We believe this all-optical processing technology based on SOAs exhibits a great potential and integration is crucial for further scalability. In this document we present an SOA-based 2-bit decoder integrated in InP technology.

2. TWO-BIT DECODER SCHEMATIC

An *N*-bit logic decoder is a logic device with *N* inputs and 2^N outputs that takes the input as a binary-coded decimal number and gives a logic '1' at the correspondent output, identified by such number. Decoders are built up of several logic gates, typically NOT and AND gates. However, by Morgan's law, AND gates can be substituted by NOR gates, as showed in the 2-bit example of Fig. 1.

Both, AND and NOR gates have their counterpart in all-optical logic. The advantage of NOR gates is that they can be easily implemented with a single SOA and the number of input bits can be increased by adding pump signals in different wavelengths. A 4-bit optical NOR in a single SOA was already demonstrated in [8].

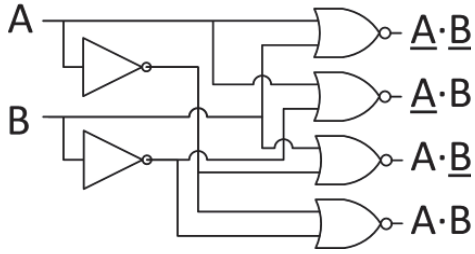


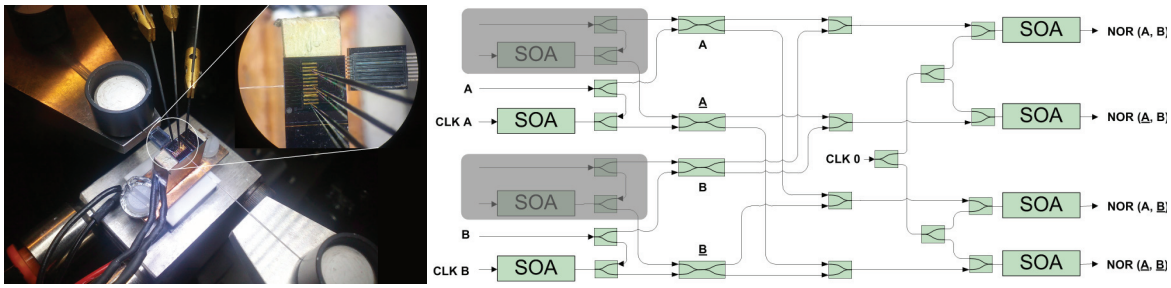
Figure 1. Logic Schematic of the 2-bit decoder.

According to the proposed architecture, we need up to 6 SOAs divided in two stages. The first stage has two SOAs and each of them performing the NOT function of each of the inputs. In the second stage, 4 SOAs act as NOR gates of the different combinations of the inputs and the outputs of the first stage. The photonic circuit integrated in the chip is described in Fig. 2b. Additionally, an arrayed waveguide grating (AWG) before such circuit allowed re-routing of signals within the PIC. Some of the signals have to pass through the gates of first stage and some are directly forming the chip input ports to the second stage. The shaded part represents elements that were not used in this experiment. CLK A and CLK B signals are injected in the PIC as clock signals and act

as Probes for the first stage of logic gates, where they acquire the logic data. The wavelength of the output signal is determined by signal CLK 0, which is guided directly to the second stage and acts as Probe for the four NOR gates. A and B are the Pumps for both NOTs in first stage.

3. SETUP

Gates in first stage were run in counter-propagating configuration, so no filters were needed between stages. Gates in second stage had co-propagating scheme; so they require a filter to extract the output signals, but it was placed off-chip. Figure 2a is a picture of the chip setup. It rests on a copper mount and three probe needles were used to apply a constant supply current to the SOAs. A thermistor inside the mount monitors the temperature and a Peltier module was placed underneath for temperature compensation.



(a) (b)

Figure 2. PIC temperature control and injection setup (a); and schematic of circuit contained in the PIC (b).

The experimental setup of the 2-bit LUT is depicted in Fig. 3. All signals, except for CLK 0, will be generated with DFB lasers emitting a continuous wave of 13 dBm average power. CLK0 will be generated with a 10-dBm TLS. First of all, A and B are amplitude modulated with a 10-Gbps NRZ bit stream and then with a synchronized 10-GHz clock, which turns them into RZ-modulated signals. CLK 0, CLK A and CLK B are modulated only with the clock. The WDM demultiplexer allows us to separate the signals and apply a different delay to each of them in order to compensate the different paths they have to go through inside the PIC. Particularly, A and B have to be delayed several bit periods with respect to each other to provide different data patterns as they reach the logic gates. Finally all signals are polarization controlled and amplified with EDFAs before being injected in the PIC. The fiber amplifier used for signal A has an output power of 15 dBm and the one used for signal B, 19 dBm. The three clock signals are coupled together and amplified in another EDFA with a total output power of 15 dBm.

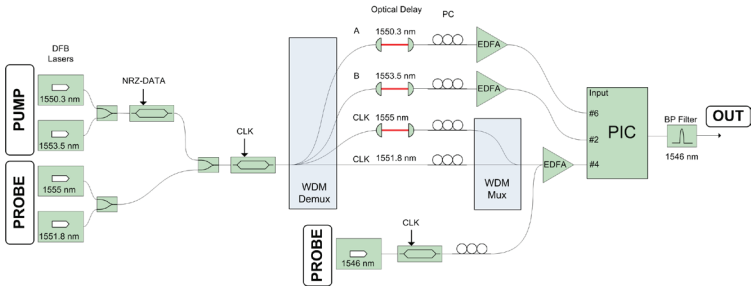


Figure 3. Schematic of the whole experimental setup.

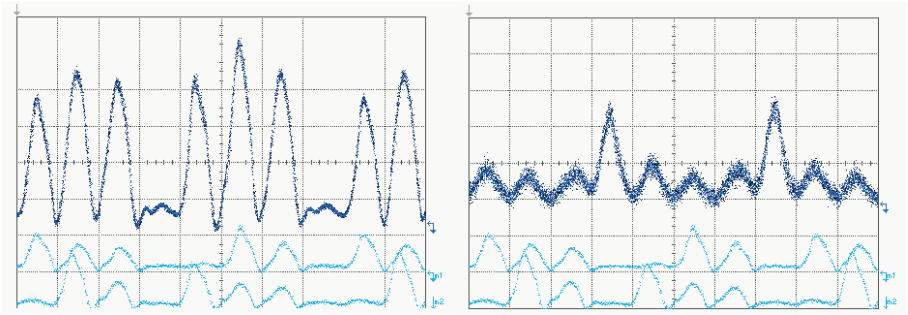
4. RESULTS

In order to analyse the performance of the 2-bit decoder, we defined three types of output, according to the number of SOAs involved its logic function: $\underline{A}\cdot\underline{B}$ with 1 SOA; $\underline{A}\cdot B$ and $A\cdot\underline{B}$ with 2; and $A\cdot B$, where three SOAs were working at the same time were needed.

4.1 Logic function $\underline{A}\cdot\underline{B}$

The best case scenario in the optical decoder was when only top-right SOA is on: the one that performs the NOR ($\underline{A}\cdot\underline{B}$). In this case both Pumps (of course, CLK 0 as well) go directly to the second stage, instead of coming from any of the NOT gates. So all signals only have to pass through only one logic gate.

One of the main disadvantages of InP with respect to silicon is the insertion loss of the waveguides (about 3.5 dB/cm). However, in a circuit with this complexity, most of the insertion loss will come from other passive elements such as splitters, couplers and the AWG. With a 3-dB theoretical loss for couplers and splitters, we can estimate in-chip losses to be at least 9 dB for CLK 0 and 12 dB for A and B. That is the reason why the maximum amplification possible is required at the inputs fibers.



(a) (b)

Figure 4. Input signals traces of the NOR gate of first case, separately and summed (a); and output signal of first case as corresponded to input traces (b) (x: time [100 ps/div], y: power [a.u.]).

Figure 4a shows the sum of both signals A and B, without any filtering, monitored at the output of the SOA in dark blue and both separated in light blue; although the scale is not the same. To achieve the logic function of A and B, we inject as well signal CLK 0 and filter off-chip with filter pass-band at CLK 0 wavelength (1546 nm + detuning).

According to the behavior of a NOR gate, pulses should come out only when Pump signals are zero. Whenever A or B are one, the gain should decrease and leave output at zero. Figure 4b shows the output signal of the NOR (A,B) at 10 Gbps after filtering at 1546 nm (detuning +0.3 nm, -37.4 GHz detuning with 87.4 GHz bandwidth). It does perform the logic function correctly at an optimum bias current of 235 mA. The noise has increased with respect to the input signals but pulses are still noticed. The main reason for such signal-to-noise ratio deterioration is the inclusion of very lossy band pass filter. The filter's insertion loss is as high as 10 dB in the pass band. There is, however, a non-zero power level for the rest of bits that appear as small and more noisy pulses in the bit trace. They can be seen as an uneven '0' level. This effect is typically due to different pulse peak levels in the total Pump signal (Fig. 4a), but should disappear when the Pump power is high enough. Since we cannot increase the Pump power; another option is to reduce the Probe power, in search for a quasi-optimum power balance. However, the signal analyser sensitivity is low and the correspondent output power would not be enough display the signal.

4.2 Logic functions $\underline{A}\cdot B$, $A\cdot\underline{B}$

The next case we studied is when one of the data signals involved in the NOR comes from another logic gate. In this case, signal $\underline{A}$ ($\underline{B}$) is formed in one of the NOTs from signals A (B) and CLK A (CLK B); instead of coming directly from the input waveguides. Signals B (A) and CLK 0 were again injected directly, as it happened in previous case. The setup also remained the same and this logic gate was performed in parallel and designed to be performed, eventually, at the same time. These measurements, however, were performed separately and every measurement needed realigning and readjusting parameters such as polarization control. The SOAs were biased with 333 mA for the NOT(A) and 270 mA for NOR($\underline{A}$,B). As observed in Fig. 5 the logic function was performed correctly and output pulses showed up only when both data signals are zero. The signal quality, however, is worse than in previous case. The small pulses corresponding to '0' bits a now higher and have two different sizes, which could already be envisaged in previous case and are clearly defined in this case.

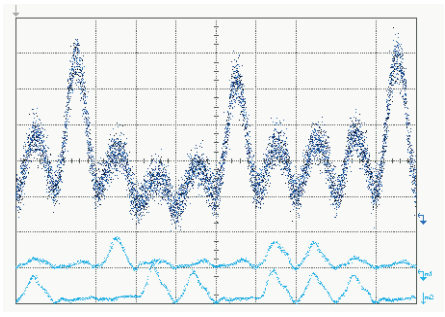


Figure 5. Output traces of the $A\cdot\underline{B}$ output, as corresponded to $\underline{A}$ and B traces (x: time [100 ps/div], y: power [a.u.]).

4.3 Logic function A·B

The worst case scenario in the decoder is when both data signals come from another SOA. That is the case of A·B, which is equivalent to NOR ($\underline{A}$,$\underline{B}$), where both signals are formed in SOAs of the first stage (NOTs), as observed in Fig. 1b. The two SOAs acting as NOTs are biased with 280 and 268 mA respectively. The one performing NOR($\underline{A}$,$\underline{B}$) function has a bias current of 215 mA. First, both NOT gates are performed in counter-

propagating setup, so their respective Probe signals are passed, not only to the NOR gate, but also back out of the chip through different input waveguides. Once we have checked that both NOTs in the first stage work at the same time, we can inject the CLK 0 signal and set the bias current of the bottom-right SOA at 215 mA. Figure 6 shows the output signal of the NOR filtered off-chip at 1546 nm. The extinction ratio has been reduced again, with respect to previous cases. Now most of the undesired pulses reach half the power of the actual '1' pulses and some of them even more and noise has increase. However, the logic function can still be seen in the trace, as pulses reach their maximum power only when both data signals are '0'.

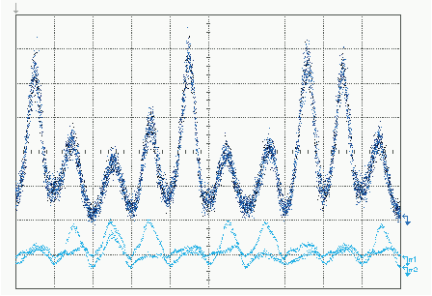


Figure 6. Output traces of the A·B output, as corresponded to A and B traces (x: time [100 ps/div], y: power [a.u.]).

5. CONCLUSIONS

An integrated 2-bit all-optical decoder is implemented and analysed at 10 Gbps. Some signs of signal degradation were noticed, such as undesired pulses when the signal amplitude should be zero. Those led to reduction the output signal extinction ratio and even multi-level amplitude for '0' bits. This normally happens when input signals do not have enough power to suppress the gain in the SOA completely, due in this case to inefficiencies of additional elements in the circuit. The logic expected could be achieved, as observed in the output RZ-modulated signals.

ACKNOWLEDGEMENTS

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