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Towards a More Flexible, Sustainable, Efficient and Reliable Induction Cooking: A Power Semiconductor Device Perspective

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A POWER SEMICONDUCTOR DEVICE PERSPECTIVE

Thesis dissertation presented to obtain the qualification of Doctor of Philosophy from the Electronic Engineering Department of University of Zaragoza

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PUBLICATIONS COMPENDIUM

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[1] M. Fernández, X. Perpiñà, J. Rebollo, M. Vellvehi, D. Sánchez, T. Cabeza, S. Llorente, and X. Jordà, "Solid State Relay Solutions for Induction Cooking Applications based on Advanced Power Semiconductor Devices," *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2018.2838093. (In press). (Impact Factor: 7.050) URL: https://ieeexplore.ieee.org/document/8365104/

[2] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, X. Jordà, and M. Tack, "P-GaN HEMTs Drain and Gate Current Analysis Under Short-Circuit," *IEEE Electron Device Letters*, vol. 38, no. 4, pp. 505-508, April 2017, doi: 10.1109/LED.2017.2665163.
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[3] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, M. Tack, and X. Jordà, "Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9012-9022, Nov. 2017, doi: 10.1109/TIE.2017.2719599.
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[4] M. Fernández, X. Perpiñà, M. Vellvehi, X. Jordà, T. Cabeza, and S. Llorente, "Analysis of solid state relay solutions based on different semiconductor technologies," in *Proc. European Conference on Power Electronics and Applications* (EPE), Warsaw, Sept. 2017, pp. P.1-P.9, doi: 10.23919/EPE17ECCEEurope.2017.8099012.
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[5] M. Fernández, X. Perpiñà, M. Vellvehi, D. Sánchez, X. Jordà, J. Millán, T. Cabeza and, S. Llorente, "Analysis of bidirectional switch solutions based on different power devices," in *Proc. Spanish Conference on Electron Devices* (CDE)*,* Barcelona, Feb. 2017, pp. 1-4, doi: 10.1109/CDE.2017.7905220.
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[6] M. Fernández, X. Perpiñà, M. Vellvehi, X. Jordà, J. Roig, F. Bauwens and M. Tack, "Short-circuit capability in p-GaN HEMTs and GaN MISHEMTs," in *Proc. International Symposium on Power Semiconductor Devices and ICs* (ISPSD), Sapporo, May 2017, pp. 455-458. doi: 10.23919/ISPSD.2017.7988916.
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[8] T. Cabeza, M. Fernández, X. Jordà, S. Llorente, I. Millán, X. Perpiñà, D. Sánchez, and M. Vellvehi, "Haushaltsgerätevorrichtung", Application number: DE201710222394 (11-12-2017), Priority number: ES20160031613 (19.12.2016).

The publications that are part of the thesis and are in writing process:

[9] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, S. Llorente, and X. Jordà, “Feedback Oscillations in Super-Junction MOSFET-based Solid State Relays,” *IEEE Transactions on Power Electronics* (In writing process).

[10] M. Fernández, M. Vellvehi, X. Jordà, and Xavier Perpiñà, “Power Losses and Current Distribution Extraction in IGBTs under Resonant Load and ZVS Condition,” *IEEE Transactions on Power Electronics*. (In writing process).

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Dedicated to my beloved family; my parents and my brother. The perfect image of honesty.

ABSTRACT

This thesis is focused on addressing a more flexible, sustainable, efficient and reliable induction cooking approach from a power semiconductor device perspective. In this framework, this PhD thesis has identified the following activities to cover such demands:

- In view of the growing interest for an effective power multiplexing in Induction Heating (IH) applications, improved and efficient Solid State Relay (SSR) alternatives to electromechanical relays (EMRs) are deeply investigated. In this context, emerging Gallium Nitride (GaN) High-Electron-Mobility Transistors (GaN HEMTs) and Silicon Carbide (SiC) based devices are identified as potential candidates for the mentioned application, featuring several improved characteristics over EMRs. On the contrary, other solutions, which seemed to be very promising, resulted to suffer from anomalous behaviors; i.e. SJ MOSFETs, and are thoroughly analysed from electro-thermal physical simulations at the device level.
- Additionally, the SC capability of power semiconductor devices employed or with potential to be used in IH appliances is also analysed. On the one hand, conventional IGBTs SC behavior is evaluated under different test conditions so that to obtain the trade-off between ruggedness and a low power losses. Moreover, ruggedness and reliability of several normally-off 600-650 V GaN HEMTs are deeply investigated by experimentation and physics-based simulation.
- Finally, power losses calculation at die-level is performed for resonant power converters by means of using Infrared Lock-in Thermography (IR-LIT). This method assists to determine, at the die level, the power losses and current distribution in IGBTs used in resonant soft-switching power converters when functioning within or outside the Zero Voltage Switching (ZVS) condition. As a result, relevant information is obtained related to decreasing the power losses during commutation in the final application, and a thermal model is extracted for simulation purposes.

RESUMEN

Esta tesis tiene como objetivo fundamental la mejora de la flexibilidad, sostenibilidad, eficiencia y fiabilidad de las cocinas de inducción por medio de la utilización de dispositivos semiconductores de potencia:

- Dentro de este marco, existe una funcionalidad que presenta un amplio rango de mejora. Se trata de la función de multiplexación de potencia, la cual pretende resolverse de una manera más eficaz por medio de la sustitución de los comúnmente utilizados relés electromecánicos por dispositivos de estado sólido. De entre todas las posibles implementaciones, se ha identificado entre las más prometedoras a aquellas basadas en dispositivos de alta movilidad de electrones (HEMT) de Nitruro de Galio (GaN) y de aquellas basadas en Carburo de Silicio (SiC), pues presentan unas características muy superiores a los relés a los que se pretende sustituir. Por el contrario, otras soluciones que inicialmente parecían ser muy prometedoras, como los MOSFETs de Súper-Unión, han presentado una serie de comportamientos anómalos, que han sido estudiados minuciosamente por medio de simulaciones físicas a nivel de chip.
- Además, se analiza en distintas condiciones la capacidad en cortocircuito de dispositivos convencionalmente empleados en cocinas de inducción, como son los IGBTs, tratándose de encontrar el equilibrio entre un comportamiento robusto al tiempo que se mantienen bajas las pérdidas de potencia. Por otra parte, también se estudia la robustez y fiabilidad de varios GaN HEMT de 600-650 V tanto de forma experimental como por medio de simulaciones físicas.
- Finalmente se aborda el cálculo de las pérdidas de potencia en convertidores de potencia resonantes empleando técnicas de termografía infrarroja. Por medio de esta técnica no solo es posible medir de forma precisa las diferentes contribuciones de las pérdidas, sino que también es posible apreciar cómo se distribuye la corriente a nivel de chip cuando, por ejemplo, el componente opera en modo de conmutación dura. Como resultado, se obtiene información relevante relacionada con modos de fallo. Además, también ha sido aprovechar las caracterizaciones realizadas para obtener un modelo térmico de simulación.

SUMMARY

LIST OF ABBREVIATIONS

2DEG	Two-Dimensional Electron Gas
AUX	Auxiliary switch
BDS	Bidirectional Switch
BJT	Bipolar Junction Transistor
CCD	Charge-Coupled Device
CMOS	Complementary Metal-Oxide-Semiconductor
CTM	Compact Thermal Model
DFN	Dual Flat No-lead
DUT	Device Under Test
EHEMTs	Enhancement-mode HEMTs
EMI	Electro-Magnetic Interference
EMR	Electromechanical Relay
FEM	Finite Element Methods
FMT	Fluorescence Microthermography
FOM	Figure Of Merit
FUL	Fault Under Load
FWD	Free Wheeling Diode
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
HSF	Hard Switch Fault
IGBT	Insulated Gate Bipolar Transistor
IH	Induction Heating
IR	Infrared
JFET	Junction Field-Effect Transistor
LCT	Liquid Crystal Thermography
MDR	Mercury Displacement Relays
MEMS	Micro-Electro-Mechanical Switches
MISHEMT	Metal-Insulator-Semiconductor High-Electron-Mobility Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NETD	Noise Equivalent Temperature Difference
PCB	Printed Circuit Board
RB-IGBT	Reverse-Blocking IGBT
RC-IGBT	Reverse-Conduction IGBT
RFI	Radio Frequency Interference
SAM	Scanning Acoustic Microscope
SC	Short-Circuit
SiC	Silicon Carbide
SJ	Super-Junction
SOA	Safe Operating Area
SPDT	Single-Pole, Double-Throw
SPICE	Simulation Program with Integrated Circuits Emphasis
SPST	Single-Pole, Single-Throw

SSR	Solid State Relay
TIM	Thermal Interface Material
TRIAC	Triode for Alternating Current
TSEP	Thermo-Sensitive Electrical Parameter
TSEP	Thermo-Sensitive Electrical Parameter
WBG	Wide-bandgap
ZVS	Zero Voltage Switching

PUBLICATIONS SUMMARY

This work has been developed at the Instituto de Microelectrónica de Barcelona-Centro Nacional de Microelectrónica (IMB-CNM) of Consejo Superior de Investigaciones Científicas (CSIC), Bellaterra, Spain, under a partnership with BSH Electrodomésticos España.

It is focused on power semiconductor device solutions and die-level investigations for a more flexible, sustainable, efficient and reliable induction cooking. The development of these contents is distributed in three main sections: the first one concerns a deep analysis and implementation of multiple Solid-State Relay (SSR) solutions based on advanced power semiconductor devices. The second one is focused on the ruggedness and reliability for both currently used and future power semiconductor devices. Finally, the extraction of Insulated Gate Bipolar Transistors (IGBTs) junction temperature (T_j) and the identification of their potential weak spots using innovative infrared (IR) techniques is evaluated in the last section.

The different approaches performed to each of the mentioned subjects have found academic recognition along the doctoral research period, and are summarized in this manuscript into a compendium of the following journal and conference publications, and a patent:

1. Development of compact SSR based on advanced power semiconductor devices:
    a. Journal Publication

[1] M. Fernández, X. Perpiñà, J. Rebollo, M. Vellvehi, D. Sánchez, T. Cabeza, S. Llorente, and X. Jordà, "Solid State Relay Solutions for Induction Cooking Applications based on Advanced Power Semiconductor Devices," *IEEE Transactions on Industrial Electronics*. doi: 10.1109/TIE.2018.2838093. (In press).
URL: https://ieeexplore.ieee.org/document/8365104/

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- Status: In press (available online).
- Impact Factor: 7.050.

- Categories:
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    - Engineering, Electrical & Electronic - Q1 - 13/260.
    - Instruments & Instrumentation - Q1 - 1/61.

b. Conference Publications

[2] M. Fernández, X. Perpiñà, M. Vellvehi, X. Jordà, T. Cabeza, and S. Llorente, "Analysis of solid state relay solutions based on different semiconductor technologies," in *Proc. European Conference on Power Electronics and Applications* (EPE), Warsaw, Sept. 2017, pp. P.1-P.9, doi: 10.23919/EPE17ECCEEurope.2017.8099012.
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c. In Writing Process

[4] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, S. Llorente, and X. Jordà, "Feedback Oscillations in Super-Junction MOSFET-based Solid State Relays," *IEEE Transactions on Power Electronics* (In writing process).

d. Patent

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[6] T. Cabeza, M. Fernández, X. Jordà, S. Llorente, I. Millán, X. Perpiñà, D. Sánchez, and M. Vellvehi, “Haushaltsgerätevorrichtung”, Application number: DE201710222394 (11-12-2017), Priority number: ES20160031613 (19.12.2016).

2. Ruggedness and reliability studies of several power semiconductor devices:

a. Journal Publications

[7] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, X. Jordà, and M. Tack, “P-GaN HEMTs Drain and Gate Current Analysis Under Short-Circuit,” *IEEE Electron Device Letters*, vol. 38, no. 4, pp. 505-508, April 2017, doi: 10.1109/LED.2017.2665163.
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- Journal: IEEE Electron Device Letters.
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- Categories:
    - Engineering, Electrical & Electronic - Q1 - 53/260.

[8] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, M. Tack, and X. Jordà, “Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs,” *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9012-9022, Nov. 2017, doi: 10.1109/TIE.2017.2719599.
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b. Conference Publication

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3. Junction temperature extraction and device weak spots identification under real conditions:

a. In Writing Process

[10] M. Fernández, M. Vellvehi, X. Jordà, and Xavier Perpiñà, “Power Losses and Current Distribution Extraction in IGBTs under Resonant Load and ZVS Condition,” *IEEE Transactions on Power Electronics*. (In writing process).

Chapter 1: INDUCTION COOKING SYSTEMS GENERAL OVERVIEW AND NEW REQUIREMENTS

1.1. Home Appliance Induction Cooking System Description

Induction cookers make use of the electromagnetic induction process (Faraday, 1831) to generate heat directly inside the base of electrically conducting cookware by means of Foucalt/eddy currents (I_{eddy}) combined with energy dissipation by the Joule effect and ferromagnetic hysteresis. Thanks to this process, the energy transfer efficiency is improved since any of the intermediate layers between the inductor and the recipient needs to be heated up. In order to reach the mentioned I_{eddy} at the vessel, alternating electromagnetic fields (B) are generated at the power inductor, where high frequency currents (I) are involved. These layers are depicted in Fig. 1.1-1.

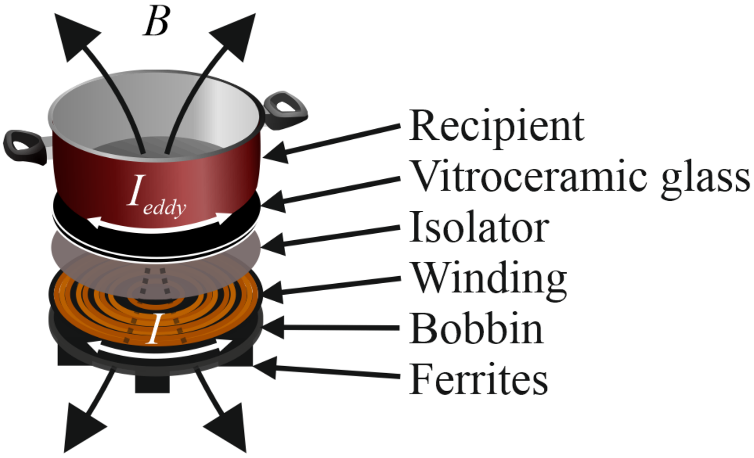


Fig. 1.1-1. Inductor-vessel system.

In this framework, the energy transfer from mains to the induction coils involves a two-stage power conversion which can be outlined as follows [11][12]:

- First, mains AC voltage is filtered and then rectified by a diode bridge.
- Resulting DC bus voltage (V_{BUS}) is connected to resonant switching inverters to supply the high-frequency current to the power inductors.

The most commonly used circuit topologies for Induction Heating (IH) applications are the half-bridge, full-bridge and single switch inverter topologies [13]. From all of

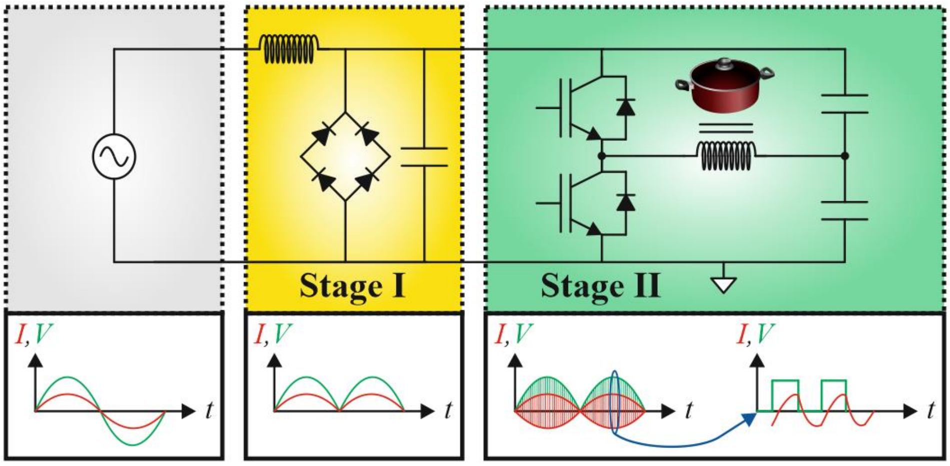


Fig. 1.1-2. Block diagram of an IH application, based on a half-bridge topology.

them, the half-bridge inverter is the most extended one, owing to its higher robustness and favourable balance among simplicity and performance above full-bridge and single switch based topologies [12][13]. However, despite their lower efficiency and most demanding requirements for the power switches, single-ended quasi-resonant topologies are also extensively used due to their lower complexity and subsequent costs [13]. Fig. 1.1-2 depicts the blocks diagram of the mentioned power stages, exemplified for a half-bridge power inverter.

Concerning their implementation, power inverters for IH are based on IGBTs as main semiconductor devices, which are positioned as cost-effective solutions due to their high-frequency and high-current capabilities, while ensuring sufficiently low power losses and an adequate thermal performance. Nowadays, IGBT trench field stop technology is widespread since it allows to reach some of the lowest power losses. However, the application of IGBTs to resonant inverters implies the integration of additional freewheeling diodes. In this sense, each manufacturer provides its own solution, where the IGBT can be either co-packaged together with an optimized diode or integrated monolithically with the diode (Reverse-Conducting IGBT (RC-IGBT)). The latter approach involves reduced costs for the manufacturers in terms of test, assembly [14] and a slightly reduced chip size for the same active area, as one of the edge regions is removed [15]; at the cost of worsened reverse recovery diode characteristics [16], which makes RC-IGBTs only suitable for soft-switching applications [17], i.e. induction cookers. Therefore, it becomes essential using snubber capacitances to reduce the device turn-off switching losses. Moreover, operating under Zero Voltage Switching (ZVS) condition will also contribute to have reduced turn-on switching losses by commutating the IGBT during the diode conduction window.

1.2. Open Quests and Demands in Induction Cooking Systems: Flexibility, Sustainability, Efficiency and Reliability in Induction Cooking

One of the major concerns of IH appliances manufacturers is to improve the user experience by extending the flexibility of the cooking zones. Based on this concept, high-end market segment products have evolved towards solutions without serigraphy, where the user may distribute the cookware of whatever size or shape all along the cooktop and at whatever position (two dimensions flexibility). This solution is conventionally realized from large number of inductors which can be connected and disconnected from several power inverters, and a high resolution pot detection system, which in combination with control techniques allows the implementation of different functions to increase the feeling of flexibility.

A different approach considers the division of the cooktop into different heating zones where varied size and shape cookware can be arranged with a lower resolution and one dimension flexibility. Usually, these zones are combined with ring or combi induction zones, constituting the value-added market segment together with conventional ring induction cooktops, where each cooking zone is assigned to a single inverter that can be enabled or disabled to the rectifying stage. Fig. 1.2-1 (a)-(b) illustrates an example of high-end and value-added oriented products, respectively.

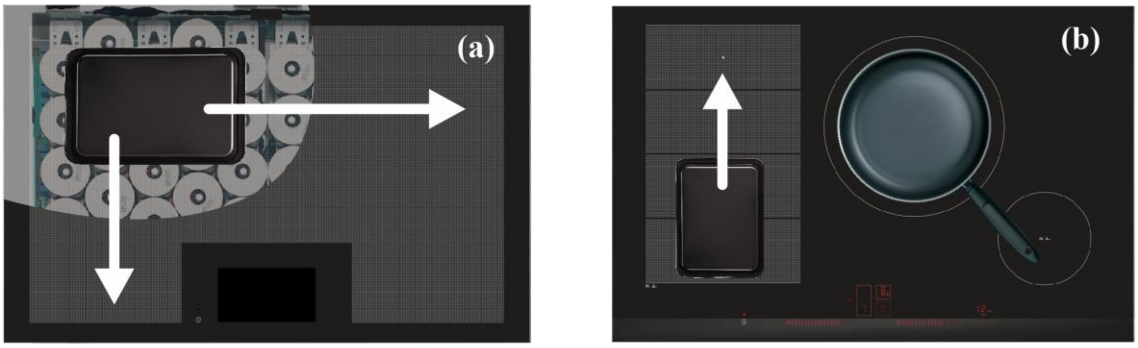


Fig. 1.2-1. Cooktop flexibility examples oriented to (a) high-end and (b) value-added market segments (one dimension flexibility cooktop combined with ring cooking zones).

In addition, a more energy-efficient and low cost appliance can be attained from the power multiplexing of different loads [18][19]. A simplified schematic of this method is presented in Fig. 1.2-2. It is based on using several switches which permit a time-commutated connection (bidirectional current conduction flow, I_{BDS}) and disconnection (bidirectional voltage blocking, V_{BDS}) of the induction coils ($L_{\mathrm{eq},1}$, $L_{\mathrm{eq},2}$, …), in resonance with capacitor banks (C_{res}), to any of the available power inverters. Also, they provide the inverters parallel operation, leading to a relevant cost reduction of the over-all system. Thereby, this platform constitutes the entry market segment.

Accordingly, one of the key elements for improving the flexibility and efficiency at all IH platforms is the electromechanical relay (EMR). However, it presents a set of drawbacks when it concerns to providing flexibility through the power multiplexing function. This constitutes an open demand that can be addressed from power semiconductor devices based designs.

Another concern of IH cooking systems is to reduce the power losses at the inverter, since it is one of the first elements to restrict the appliance performance. Currently, one solution to reduce the conduction losses of insulated gate semiconductor devices for power converters mainly consists of triggering them at gate voltages higher than the nominal ones, resulting in increased charge densities at the channel and lower on-state resistance [20]. However, increasing their gate control input voltages close to the maximum allowed may lead to reduced ruggedness and reliability and, the gate dielectric being the most affected part. In this sense, an adequate characterization of the semiconductor devices to fully exploit their potential will be beneficial for improving the efficiency, leading towards a higher sustainability for home appliances. In addition, a thorough evaluation of device power losses at die-level will provide useful information concerning the effect of different driving concepts, such as the operation outside ZVS condition or the use of capacitive snubbers. Furthermore, by extending this analysis to a die-level, it will also be possible to identify the devices weak spots, acting as a failure precursor.

Moreover, due to the higher complexity of modern appliances, under certain circumstances of varying origin, the power devices can be subjected to high voltage and current stress. Consequently, analysing their behaviour under such faulty conditions

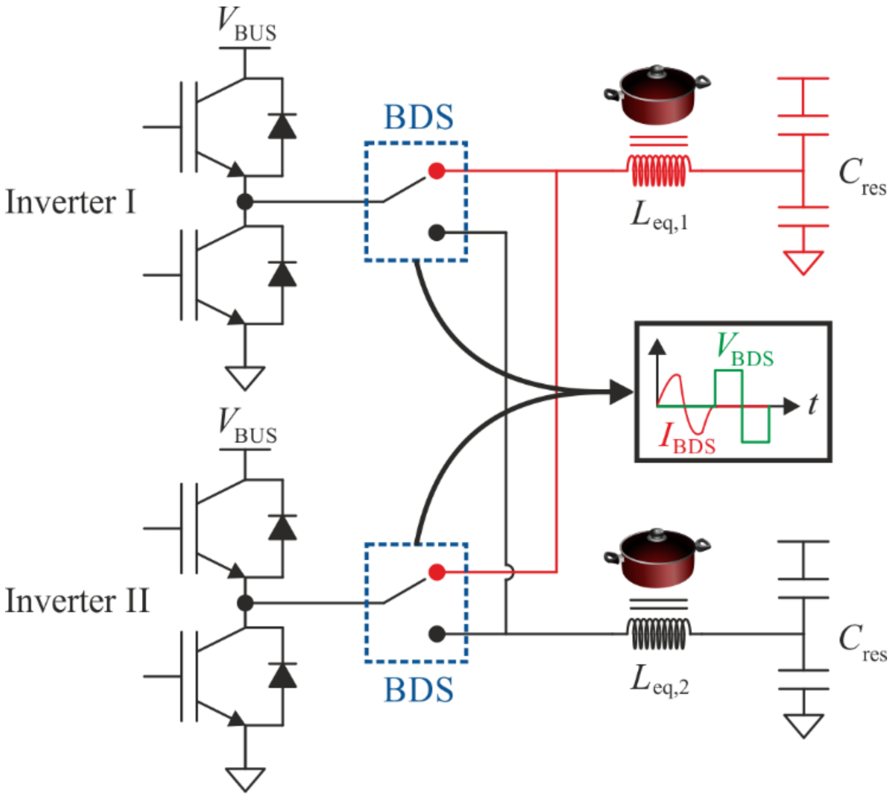


Fig. 1.2-2. Simplified schematic of an IH system using the power multiplexing function. Figure extracted from [1].

becomes crucial to determine their ruggedness and reliability. Every year a certain percentage of total production of induction cooktops is scrapped, which adds to those ending their useful life. These facts provoke a significant environmental impact. In this sense, home appliances industrial manufacturers aim at reducing their failure rate and extending their products lifetime above 10 years, always taking into account that these appliances must provide uniform performances for a domestic use (limited hours per day). In this field, the contribution of power semiconductor devices is linked to an improved ruggedness.

1.3. Flexibility in Induction Cooking

1.3.1 Limitations of Multiplexing Approach

One of the main benefits of EMRs is a very low on-state resistance, in the range of 5-10 mΩ. In addition, the EMR producers invest large amounts on developing the manufacturing technology for fabricating these components into high volumes, constituting the most widespread and lowest cost solution for the commutation of power sub-circuit blocks.

However, their application to power multiplexing evidences a set of limitations which are summarized below:

- They present moving parts, which are susceptible to wear and be affected by vibration or physical shock, with a consequent short service life.
- In addition, they present electric arcs during commutation, with a resulting risk of terminals welding.
- They are commonly packaged using plastic cases, which will not provide enough protection (hermeticity) against external pollutants.
- They produce acoustical noise when contacts are switched.
- They present large electromagnetic interferences.
- High inrush current and input power consumption.
- Very slow response (in the order of ms), thereby limiting the multiplexing rate.
- Large size and weight.

1.3.2 Power Multiplexing function for IH

For the specific case of IH appliances, some of the above-mentioned limitations remain unacceptable. Therefore, an EMR-based power multiplexing function involves additional restrictions.

The inverter power devices specification for the studied application usually considers voltage and current ratings of 600-650 V and 30-40 A at 100 °C. However, conventionally used EMR might consider AC voltage and current ratings of 300-400 V and 16-30 A at 100 °C as it is established by the automotive industry. Depending on the IH platform and operating modes, many elements can be responsible for the application of a power regulation caused by overtemperature: the inductors, the inverter power devices (usually IGBTs) or even the EMR. In the scenario of a power multiplexing platform, the EMR is the receiver of the highest thermal loads. Unfortunately, the higher sizes for the next current steps leads to a trade-off against a solution based on two parallelized EMR, together with the consequent costs increase. Therefore, the EMR current rating constrains the maximum supplied power, which would require a multiple

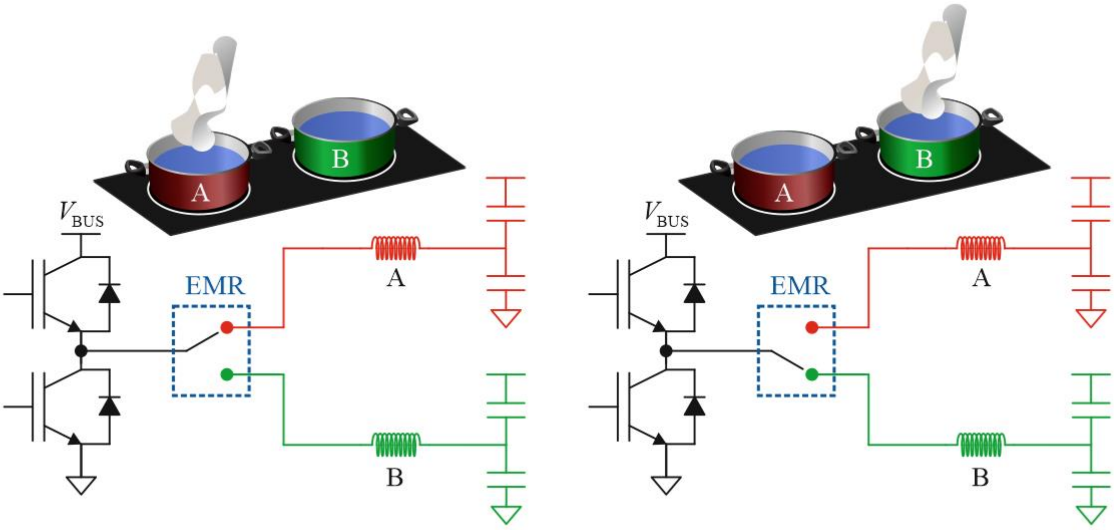


Fig. 1.3-1. Water boiling effect.

inverters parallelization.

Consequently, arcing under such current/voltage conditions need to be avoided to prevent the terminals welding. This can be achieved by turning-off the inverter prior to the EMR commutation for a specified transition time, which unfortunately highlights a significant dispersion. Once the EMR has been detected to have finished its movement, the inverter is, again, switched on. Moreover, the inverters deactivations/activations have to be performed by ramping the inverters frequency to prevent the high magnetic field from inducing additional noise at the recipient.

A direct consequence of such a low multiplexing rate occurs when a single EMR is time-multiplexed for liquid boiling at multiple loads for recipients with a low thermal inertia and for which a high sum power is selected. As a result, water boiling can intermittently stop and might give a misleading impression of a performance loss event (Fig. 1.3-1), unless multiplexing of different inverters with no involved EMR commutation is possible. Also, increasing the multiplexing rate will reduce the EMR service time. Furthermore, the EMR acoustical noise under multiplexing conditions is quite high. In this context, efforts are being made in the industry to reduce this nuisance for the final user [21].

Since most of these drawbacks can be downsized or removed by power semiconductor devices based SSR design, one of the research targets of this PhD is investigating possible replacing solutions based on them.

For the specific case of the power multiplexing function, this method can be implemented using SPDT (Single-Pole, Double-Throw) bidirectional switches (BDS), as shown by Fig. 1.2-2. However, this work focuses on analyzing different static implementations of the Single-Pole, Single-Throw (SPST) BDS switching function as the main step for SPDT implementation, so that all results stemming from this study can be extended to the mentioned SPDT relay.

1.3.3 State-of-the-art in SSR

First, an exhaustive research resulted into a complete state-of-the-art where any existing and emerging technological options to implement the mentioned relay or power multiplexer function in the framework of the IH applications was identified. The main objective of this analysis is to get data from each technology and make a quantitative comparative study, so that a set of potential possible alternatives to EMRs are selected for deeper study. Besides the EMRs, five technological families are identified:

1) Dry reed relays: these relays can commutate faster than EMRs with a lower input power consumption. In addition, they highlight a longer service life. However, they present a higher contact resistance and due to their smaller contacts, they are limited to low currents, in the range of 2-3 A [22].

2) Mercury Displacement Relays (MDR): which can be categorized as a type of reed relays [23]. MDRs combine the absence of mobile contacts, as a relevant advantage over EMRs, and the lack of heatsinks, as a relevant advantage over SSRs [24]. However, they are not suitable for a high-frequency operation and became obsolete due to the mercury toxicity.

3) Micro-Electro-Mechanical Switches (MEMS): whose main switch element is a freestanding mechanical cantilever. This technology is conventionally used for low power; however, the parallel connection of multiple MEMS arrays has been demonstrated to resist more than 300 V, with low on-state resistances, in the range of 100 mΩ, and with a fast arc-free switching speed, in the μs range [25]. Unfortunately, this solution presents a very low current-carrying capability, around 5 A, and very high-voltage driving requirements, around 80 V. This technology is

presently under development and therefore it is expected a future improvement of its performance.

4) Standard SSR solutions: which make use of power semiconductor devices for realizing the BDS function. This type of switches is industrially available with both control and power stages integrated into single parts. Concerning their output stages, they are conventionally Thyristor or Triode for Alternating Current (TRIAC) based for AC loads and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) based for AC/DC loads [26]. Notwithstanding, the first ones are only spread for AC applications at mains frequency, in the range of 0 to 1.5 kV. As a consequence, they are not suitable for the high-frequency operating currents involved in the studied framework. Alternatively, SSR solutions based on new power semiconductor device technologies will be deeply evaluated in the next chapters.
5) Specific hybrid solutions, based on different combinations of semiconductor power devices or even with EMR, i.e. an EMR parallelized with a TRIAC based SSR, where a control circuit first switches on the SSR, so that to handle the load inrush current, and then the EMR, at no load, to handle the corresponding load current [24].

All technological options have been categorized in view of their conduction and switching power losses, switching speeds, driving needs, isolation, input power consumptions, controllability, service life, typical failure state, size, weight, existence of arcs, magnetic interaction, noise and EMI, presence of mechanical/moving parts, environment (vibration, shock, altitude, position, interaction) and comparative costs.

From the characteristics of each technology, it is concluded that the only practical solution for the induction cooking application is based on the use of advanced SSRs, since any of the other technological families will find a technical advantage [1]. For that reason, this thesis performs, for the first time, an exhaustive comparison among the electric and electronic options available to implement the BDS function for EMR replacement based on power device assemblies, analyzing their pros and cons and including emerging technologies such as Wide-bandgap (WBG) power devices. In addition, a Figure Of Merit (FOM) is proposed to extend the comparison from specific device references to the different device technologies. These topics are developed in Chapter 3.

1.4. Ruggedness and Reliability Studies of Power Semiconductor Devices

1.4.1 Standard Reliability Tests at System Level

Short-Circuit (SC) protection is not usual at IH appliances, since the power inductors are electrically isolated for high temperatures and from the heated recipient. Therefore, the possibility of a complete inductor SC is reduced.

As a consequence, the performed endurance tests mainly consist of the development of accelerated aging tests.

However, since novel inverter topologies are becoming more complex, the risk for a SC event is increased. Some examples are:

- Welding of EMR contacts at multiplexed topologies.
- Erratic driving strategy, resulting either into too short dead times or high frequency modulation at no load.

In addition, despite it is not a SC event, the use of an Aluminum recipient for the same maximum load power than for a non-ferromagnetic recipient results into many times higher currents flowing through the inverter devices [27].

Also, similar unlikely failure modes may occur leading to a SC event as for any other industrial application, i.e. faulty gate control signals, defective collector-emitter or gate-emitter overvoltage protections, etc.

Each of the mentioned scenarios result into completely different SC current profiles and electric signatures which might not be possible to identify during aging tests. Therefore, a ruggedness failure analysis is proposed in the next section.

Moreover, apart from studying how a specific power device technology would reach destruction, it becomes also very important to identify precursor parameters which can reveal how the device might be degraded under certain operating conditions, in order to have an estimation of its expected service life. In this sense, the use of junction temperature (T_j) monitoring as a lifetime indicator is also presented.

1.4.2 Power Device Ruggedness against Overloading Stresses: SC Studies as a Test for Overcurrent in IH

In general, electro-thermal overloading stresses result from abnormal working conditions or events, in which the device is set outside its Safe Operating Area (SOA). They can be categorized into overvoltage, overcurrent and overtemperature. Another abnormal event is that originated from an electrical SC during the regular operation of the device; where the switch withstands the whole V_{BUS}, while conducts current. As a result, the power device can reach destruction [28][29]. This occurs within the die, starts from a local electro-thermal phenomenon (high temperature and current levels reached locally) at very short timescales (ns-µs range). Sometimes, the origin of such catastrophic phenomena is unknown, is non-repetitive, and depends on the device layout or its inherent structure (weak spots) [30]. All such abnormal events (i.e., SC, overcurrent, or overvoltage) can come from dysfunctions on the driving process, [28][31][32] environmental conditions or load variations [33]; thus compromising the reliability of the power system. From a final user point of view, a first approach to face such abnormal events is the use of ruggedness tests to select the devices, which can overcome such stressful conditions. Jointly with endurance tests, this helps to enhance the converter reliability. Moreover, from the electrical failure signature, a more complex solution involving the driver circuit can be performed. The driver constantly surveils any failure indicator occurrence, prepared for actuating to avoid the power device destruction. Unfortunately, such ruggedness tests (also known as test at limit) have been designed by power devices manufacturers and not always are representative of the final application.

In the case of IH applications, SC test is some of the closer one to replicate the situation of an overcurrent event due to the snubber discharge when the maximum current is passing through the device, especially as a consequence of losing ZVS condition. In fact, X. Perpiñà et al. determined in [34] that a modified SC tests could be a good approach to replicate this and useful for the selection of more rugged power semiconductor devices. This work suggests that setting gate-emitter voltages (V_{GE}) at 10 V under a SC condition reproduces the situation typical of an overcurrent event due to the snubber discharge when the maximum current is passing through the device as a consequence of losing ZVS. Moreover, it has already been demonstrated that the limits of Trench IGBT for medium voltage applications devices are mainly thermal under SC events [35][36]. This is supported by its thin drift region. This situation is going to worsen as IGBTs manufacturing trends target at thinner dies and smaller cell pitch [20]. This increases the power density generated within them under operating conditions. Traditionally, another purpose of SC tests is to evaluate if, for a given V_{BUS}, the SC withstand time (t_{on}) is long enough so that the SC condition can be detected by a controller or driver, and safely interrupted by switching-off the tested device with no electrical damage for the power converter [37]. According to the available drivers, the fault detection time is conservatively estimated to be below 6 µs [38].

To provide more details in this sense, the aim of SC test is to reproduce a SC fault in the converter, which must be withstood by the device without destruction or degradation, and/or detected by its driver to turn it off safely. The Hard Switch Fault test (HSF, SC I) is the most commonly used by power device manufacturers [39], despite being less demanding for the device than Fault Under Load test (FUL, SC II). Under a SC I condition, the Device Under Test (DUT) is gated on into a faulty event, while under SC II, the device is on-state when SC fault occurs. Consequently, SC current flows through it while withstanding V_{BUS}, eventually giving rise to its destruction in a certain time to failure (t_{SC}). For a given V_{BUS}, this test aims at evaluating whether the SC time duration is long enough to detect the SC condition with a controller or driver, and safely switch the device off without any converter electrical failure [40]. This situation can be envisaged more stressful in IH due to the devices gate control. As a consequence of the higher involved V_{GE}, the devices SC current is higher, and therefore t_{SC} is reduced. In this topic, passing SC I tests becomes essential prior to integrating the devices in the studied application.

1.4.3 Power Device Degradation due to Ageing: T_{j} Monitoring

As Arrhenius law dictates, the material properties of the different parts of the power converter evolve and change along endurance tests according to their operation temperature. As a consequence, the power semiconductor devices performance can degrade. Thus, the role of temperature as an acceleration factor is critical in IH, as the cooktops are always mounted on top of ovens and their worst working scenario contemplates both under operation. This forces the switches to operate at temperatures near to their limit (150 °C) or higher enough to fasten their ageing. For this reason, investigation efforts in last years have been focused on reducing the power losses in power devices, as performed, e.g., with soft-switching strategies under ZVS condition. For all these reasons, temperature is a parameter susceptible of being monitored not only during its thermal design, but also in the final cooktop. Unfortunately, measuring T_j in power devices is not a common practice in such systems. Usually, this is estimated by means of circuit level simulations thanks to the electro-thermal compact models of the device jointly with its dissipation system. Moreover, there is also a lack of commercial systems which allows locally monitoring T_j within commercially available power devices. Therefore, two clear needs have been identified:

- The measurement of the average T_j is crucial to maintaining the device operating temperature below a maximum value, aiding and assessing the thermal management design of the power converter. However, with a heat dissipation system, it is not possible to control local temperature rises due to electrothermal coupling.
- Within the device itself, local temperature can reveal structural weak spots or current crowding problems, as current density extremely increases. This is linked with the local electro-thermal aspects stated in 1.4.2. Due to the local high dissipation in such processes, burnout failures or die cracking can induce the device failure, leaving some signatures interesting to be located for the die posterior analysis. In fact, to better withstand such high stress conditions, power devices are being designed with improved local electro-thermal behaviour, by performing accurate simulations. Nonetheless, the simulation of their thermal failure phenomena requires transient temperature-field data for verification and improvement of the model parameters used.

For a long time, thermometry in power devices has been based on the use of Thermo-Sensitive Electrical Parameters (TSEP) [41]. The most used TSEP in power electronics is the voltage drop of a PN junction forward biased by a low current level, since all power devices contain inherent PN junctions inside them. Apart from the voltage drop in the PN junction of a power diode, some examples are the voltage drop between collector-emitter terminals of a bipolar or IGBT in saturation regime. Other TSEP very used in MOS-controlled power devices is the threshold voltage. Despite the threshold voltage is less linear and sensitive than the forward biased PN junction; it allows an extraction of a maximum operation temperature much more precise and accurate depending on the operation regimes of the DUT, e.g., SC for IGBTs [42]. As major advantages of the TSEPs use, temperature measurements can be performed on fully packaged devices with little or no modification, directly measuring the temperature within the device. However, an average value of device temperature is obtained, because of the calibration experimental conditions [43][44]. This calibration is performed measuring the desired TSEP once the whole device is just heated and stabilized to a given steady-state temperature.

In contrast to this, other techniques have appeared to allow local monitoring at die-level. Basically, they may be categorized in laser probing or surface thermal imaging techniques [45]. The former consists in using as a probe a laser beam, where the thermo-sensitive magnitudes are its power, propagation direction, or phase. Thus, according to the monitored beam characteristic, internal infrared (IR)-Laser Deflection (beam deflection) and interferometric (phase shift) thermometry are distinguished. However, sometimes they require an extra step for DUT conditioning before the measurement and their use is restricted in laboratory environments as integrating them in a real working scenario is very difficult. As for surface thermal imaging techniques, they determine the temperature distribution on the die top surface by means of a Charge-Coupled Device (CCD) camera. This process may be performed by either directly measuring the radiated heat flux with an IR camera (IR thermography) [46] or previously depositing a thermo-sensitive film on the inspected surface as Liquid Crystal Thermography (LCT) or Fluorescence Microthermography (FMT). As a result, an image containing the die surface thermal mapping is recorded with a camera. All these techniques are very useful for hot spot determination especially when lock-in strategies are used [47]. With this approach, the thermographic system signal-to-noise ratio is extremely increased, while the spatial resolution of hot spots is improved by frequency modulation. This allows determining the locations where the failure or any current crowding occur.

1.5. Current Approaches for Efficiency Assessment in Induction Cooking Systems

1.5.1 Power Losses Evaluation by Electrical Means

The electrical measurement [48]-[53] uses the product of voltage and current, which gives an electrical quantity equivalent to power. Power measurement can be performed by measuring the voltage drop across the device and the current flowing through it using electrical instruments. In DC and low-frequency AC circuits, it is common to measure power directly by using analog electronic equipment: voltmeters for voltage measurements and ammeters for current measurements, or a combined measurement using a wattmeter. However, for high-frequency signal and highly distorted signals, such as pulse width modulation, conventional meters are no longer suitable because of their limited bandwidth and dynamic frequency response. Digital instruments have gained popularity for obtaining the required resolution. This kind of digital meter takes simultaneous samplings of voltage and current waveforms, digitizes these values, and provides arithmetic multiplication and averaging using digital techniques to obtain a power measurement. An appealing advantage of the electrical methods is that they are easy to perform and to reproduce a measurement. It is suitable for steady state as well as transient measurements. However, high *dI/dt* and *dV/dt* introduce serious Radio Frequency Interference/Electro-Magnetic Interference (RFI/EMI) problems since digital instruments are very sensitive to noise. The accuracy of digital measurement is also affected by the delays introduced between probes, phase shifts between sampling channels of digitizer, sampling errors, and nonlinearities of analog-to-digital converter. No instrument known to man can accurately record the hard-switched output voltage waveforms when *dV/dt* is very high [54].

To date, the most common methods of determining power loss have been the conventional input-output procedure by taking the difference between the measured input and output power. From the basic definition of losses, this is a natural choice. There is always considerable error associated with the subtraction of two nearly equal numbers for high-efficiency system, whichever method is used to measure input and output power.

1.5.2 Power Losses Evaluation by Calorimetry Means

In theory, higher accuracy is possible by measuring loss directly. Since the total power losses dissipate as heat, the effect caused by the heat can be measured to determine the losses. This can be achieved by calorimetric methods. Consequently, calorimetric method based on direct loss measurement provides a more accurate measurement technique. Calorimetric methods have been widely used in power electronics to measure the power losses of magnetic components [55]-[59], capacitors [60], switching semiconductors [61][62], power converters [63], and electrical machines [63]-[72]. Consequently, the calorimetric principle is the most promising of the methods available for accurate power loss measurements [72][73]. This method has the advantage of being able to measure the power losses under normal operating conditions and being independent of electrical quantities of the device under test. The disadvantages are that it is usually limited to steady state and that measurement procedure is time consuming.

1.6. Thesis Thematic Unit and Scope

Current trends in induction cooking propose to design the new cooktops for being more flexible, sustainable, efficient and reliable. In this way, new products with a lower cost, longer lifetime and more rational use of energy could be commercially available. In this regard, power semiconductor devices emerge as promising pillars to achieve such targets. However, a long pathway of technological exploration is still required. This thesis faces some of such topics from semiconductor power device point of view, either proposing new applications or starting new ways to better study them at die-level. Bearing in mind several semiconductor technologies, this PhD work proposes several solutions in the following fields: SSR, power losses calculation in resonant power converters and ruggedness study on semiconductor devices employed or with potential to be used in induction cooking appliances.

With regards to SSR, a suitable replacing technology for the EMR is investigated in the framework of induction cooking appliances, mainly intended to provide flexibility through the power multiplexing function. Existing and emerging technological options are studied and the most promising identified solutions are completely developed, bringing them closer to the practical application scenario from fully functional prototypes.

Moreover, ruggedness tests are performed to much better study the suitability of new power device references in induction cookers: SC tests at high V_{GE} values (up to 20 V), to explore if they have such capability and exploit this to improve the induction cooker reliability. In this last point, the suitability of medium voltage Gallium Nitride (GaN) High-Electron-Mobility Transistor (HEMT) devices for induction cooking appliances is also considered in terms of their SC capability.

Finally, in relation to efficiency and reliability aspects in induction cooking, several working scenarios are considered. Firstly, the working T_j evolution of the IGBT semiconductor devices used in induction cooking appliances is unknown and is a completely new topic to be investigated. It will be interesting having a procedure to accurately evaluate the power losses in devices (power dissipation model), as well as a predictive thermal model of the used components, accounting for all effects involved from the device to external boundary conditions. Therefore, establishing a losses evaluation procedure, jointly with a validation protocol by means of an IR camera, could aid to a more accurate modelling. Secondly, the power dissipated due to switching losses (thermal cycles with higher frequency and lower temperature swing) are analysed if higher time resolution can be achieved by alternative post-processing approaches of IR thermal maps. This helps to determine the effects of IGBT recombination processes after turn-off in such a modelling to further understand the IGBT behaviour and decrease its losses under soft-switching conditions.

Chapter 2: THESIS OBJECTIVES AND STRUCTURE

2.1. Main Objectives

The main objectives of this PhD Thesis are:

- An improvement of IH appliances by increasing their flexibility, sustainability, efficiency and reliability levels, based on power semiconductor devices. This goal is achieved from:
  - Studying the implementation of SSR based on advanced power semiconductor devices to improve the performance reached by EMR. Different technological solutions are evaluated and a specifically designed dynamic test circuit is developed.
  - Robustness analysis of the power semiconductor devices used in IH appliances. Studying the robustness of emerging power devices to be used for IH. Using the SC tests as a ruggedness evaluation tool in line with the standards used by the power semiconductor devices manufacturers. To this end, an already available test platform is optimized to perform those measurements.
  - Extraction of T_j distribution of the power semiconductor devices as a means of evaluation of the devices power losses and weak spots identification under real condition. For this purpose, a specific measurement test platform needs to be designed and implemented. It is worth to point out that under ZVS conditions and the presence of a snubber capacitor, the measurements of the total electrical power losses become more complex and further approximations are required. These facts help to improve the design for reliability at system level by allowing the validation of the suitability of electrical models for its simulation. Moreover, local analyses of the temperature distribution are used for the extraction of the devices current distribution, which provides useful information to identify the device weak spots which might originate the component destruction.

- Establishing criteria/protocols for power semiconductor devices selection representative of IH appliances requirements, in order to mitigate future reliability problems.

2.2. PhD Thesis structure:

To cover the outlined goals, this thesis is organized in the next chapters as follows. Chapter 3 addresses the SSR BDS implementations. First, the objectives and PhD student's role is described. Then, the implementation of the studied BDS into test vehicles, together with its characterization, is addressed in section 3.2. Moreover, section 3.3 is focused on their performances and characteristics, which are evaluated from static and dynamic analysis. In addition, a simulation approach is also developed so as to fully understand the devices oscillatory phenomena at the blocking instant (Simulation Program with Integrated Circuits Emphasis (SPICE) simulation) and the identified abnormal behaviours using Finite Element Methods (FEM) based simulations. Besides, it is addressed the implementation of a functional prototype and its final evaluation at an IH appliance. Finally, this chapter ends with the main conclusions.

In Chapter 4, ruggedness and reliability studies in power semiconductor devices in the framework of induction cooking are addressed. First, the objectives and PhD student's role is described. Then, the used test platform for performing SC tests in IGBTs and GaN HEMTs is described, together with a brief description of the studied devices characteristics. Afterwards, the results of the SC tests are discussed. Finally, the chapter ends with the conclusions.

Chapter 5 addresses T_j extraction and device weak spots identification under real operating conditions. This chapter starts with the objectives and PhD student's role. Then, the selected devices and the used test setups are described. Moreover, the extraction of the devices Compact Thermal Model (CTM) is addressed. Furthermore, this chapter describes the development of a simulation thermal model based on the obtained CTM. Finally, the conclusions are discussed.

Chapter 6 concludes this PhD Thesis with an outline of the general conclusions and a proposal of future works.

Chapter 3: SSR BDS IMPLEMENTATIONS

3.1. Objectives and PhD student's role

As it has been already stated, one of the objectives of the present research was the analysis of innovative options for replacing the EMR as a key component for enhancing the flexibility of future induction cooking systems. In this sense, SSR solutions based on advanced power semiconductor devices have been experimentally analysed by the PhD student in the context found in IH converters for home appliances. Emerging Silicon Carbide (SiC) and GaN WBG based implementations are compared to the most performant Silicon (Si) based devices (i.e.: TRIACs, Si IGBT+diode, RC-IGBTs, Reverse-Blocking IGBTs (RB-IGBTs), Si Super-Junction (SJ) MOSFETs, SiC Junction Field-Effect Transistors (JFETs), SiC MOSFETs, GaN HEMTs, GaN Cascodes etc.). Up to 20 test vehicles have been implemented with these devices and assessed with specifically designed test platforms and set-ups, providing for the first time an exhaustive evaluation and comparison among SSRs developed with all the commercially available power semiconductor devices. The results obtained from the tests have been presented in national and international conferences in order to promote a fruitful exchange with other researchers and to detect any possible alternatives of interest to be included in the study. In particular, in [3] the electrical characterization approach taken for the SSR test vehicles evaluation was presented, as well as the results obtained from the first prototypes developed with the anti-series connection of devices (Si IGBT+diode, RC-IGBT, SJ-MOSFET, SiC MOSFET, SiC JFET and GaN HEMT). In [2] the experimental results concerning single chip solutions (Si TRIACs) and anti-parallel combination of RB-IGBTs were also presented. Finally, the complete study adding the last device references appeared in the market (SiC Bipolar Junction Transistors (BJTs), SiC cascodes and GaN cascodes) was published in [1]. In this paper, original concepts for SSR electrical characterization from the static (definition of a new FOM) and dynamic (new test platform concept) point of view were presented, as well as the validation of one of the most promising solutions (GaN HEMT based SSR) in a real induction cooker. Using this GaN-based SSR prototype, special attention to the thermal management issues was also addressed. The most tangible conclusion derived from the present PhD objective (analysis of new SSR concepts) has been a patent application claiming for a SSR solution based on GaN HEMTs [5][6]. The benefits and potential of such innovation is directly derived from the exhaustive study performed by the PhD, which is described in the mentioned references. Another significant conclusion obtained in this work was the identification of abnormal failure mechanisms detected for the first time in RC-IGBTs and SJ MOSFETs [4]. The explanation of these unexpected results required an in-depth analysis of the device structure and operation, and justify in fact the research effort devoted on each new SSR solution analysed. The next sections summarize the main results concerning the development and characterization of the proposed SSR solutions.

3.2. SSR Test Vehicles Design, Development and Characterization

3.2.1 Semiconductor Power Devices Selection for SSR

The requirement of power semiconductor devices to IH appliances comes almost from its very beginning [74], imposed by the commutation of the high-frequency currents for the power inverters: 20-40 kHz. Nowadays, the upper limits have been extended up to 80-100 kHz and are limited by the switching losses of the involved power semiconductor devices, conventionally Si IGBTs.

Concerning the power multiplexing function, the requirement of a soft-stop/start function of the power inverter is removed when SSR solutions are employed, except for the TRIAC. In contrast, a zero-crossing current detection circuit is required. Moreover, the EMRs are commutated at very low switching frequencies. Consequently, it exists a clear predominance of the conduction power losses, well above the switching power losses, when SSR-based implementations are considered. Therefore, despite the mentioned drawbacks of EMRs, their application is preferred because of their lower on-state power losses, compactness and reduced costs. However, recent improvements on Si-based devices and the excellent properties of emerging WBG-based devices open up the possibility for SSRs with comparable efficiencies and improved switching characteristics, when compared to EMRs. Moreover, in so far as the need for higher EMR current rating grows, the cost of SSR BDS will be more competitive.

The studied framework involves 600-1200 V and 20-70 A for the power devices included in this work, so as to extend the coverage of the analysis to the biggest possible number of power semiconductor devices families. For simplicity, all the developed implementations are based on commercially available devices.

3.2.1.1 Si Devices Technologies

From Si-based device technologies, Si TRIACs and Si SJ MOSFETs were initially identified as some of the most promising solutions to replace the EMR.

Concerning the Si TRIAC, the main advantage of this device above the rest of the studied semiconductor devices is that it implements a BDS just by itself. Unfortunately, at the same time it is the only one that conceptually fails at switching off the involved high-frequency AC currents, due to highly exceeding the devices turn-off maximum rate of current change. Therefore, a solution based on Si TRIACs would imply the need for deactivating the power inverter prior to the device commutation, as it happens for EMRs. In addition, despite these devices highlight some of the highest current densities [1], the device power losses are high when compared to EMR due to the intrinsic voltage drop of its PN junctions, which will involve the need for additional dissipation heatsinks. Notwithstanding, a solution based on Si TRIACs will allow a higher multiplexing rates (with the above-mentioned restrictions) and therefore improve the application performance by eliminating the irregular water boiling issues and completely removing the acoustical noise.

With regards to Si MOSFETs, the development of SJ technology in 1997 was capable of breaking the called “limit of Silicon”, which had been established during 1980s. This limit fixed the lowest possible on-state resistances for specified breakdown voltages. SJ technology gave rise to a power device with one of the lowest on-state resistances: featuring <20 mΩ at 650 V. Though, a BDS solution based on these devices revealed an abnormal oscillatory phenomenon when turned-off, as it has been demonstrated for the first time by experiments and physics-based simulations. It is addressed in [4].

Other Si-based technologies are interesting for SSR implementation, in particular RC-IGBTs and RB-IGBTs. Nevertheless, such bipolar power devices show an unavoidable off-set voltage drop (higher than that of TRIACs) responsible for relatively high conduction power losses [1][75][76].

Given that the most performing Si-based BDS alternatives to EMR in terms of the conduction power losses highlight several limitations, and that Si-based technologies have already reached a significant degree of maturity, the focus is placed at innovative WBG-based power semiconductor devices, with the expectations of higher performances and projected costs drop in the medium/short-terms.

3.2.1.2 WBG Devices Technologies

WGB semiconductor devices highlight superior switching and thermal characteristics compared to its Si counterparts, enabling a reduction of the passive elements. Therefore, power devices technologies based on those materials are emerging as potential candidates for those applications in which Si devices present a limited operation [77].

Among WBG materials, GaN and SiC materials are the most promising ones. While GaN HEMTs highlight lower on-state resistances than SiC, the latter provides higher breakdown voltages. In this sense, there is a crossing point around 600-1000 V from which the balance is shifted in favour of SiC [78]. Concerning GaN devices, they can be grown in both Si and GaN substrates, but Si substrates provide substantial costs decrease and takes advantage of keeping the same semiconductor devices manufacturing lines used for nowadays Si-based devices.

Natively, GaN HEMTs are normally-on switches, which result critical for appliances with fail-safe requirements. In response to this, GaN cascodes and Enhancement-mode HEMTs (EHEMTS) have appeared as a normally-off solution [79][80]. In this scenario, p-GaN HEMTs and Metal-Insulator-Semiconductor HEMTs (MISHEMTs) are consolidating as the most promising commercially available EHEMTs. An implementation of a SSR BDS based on GaN MISHEMTs is addressed in this chapter, where this solution highlights the lowest on-state resistance and the highest integration characteristics, from the possibility of implementing the BDS monolithically.

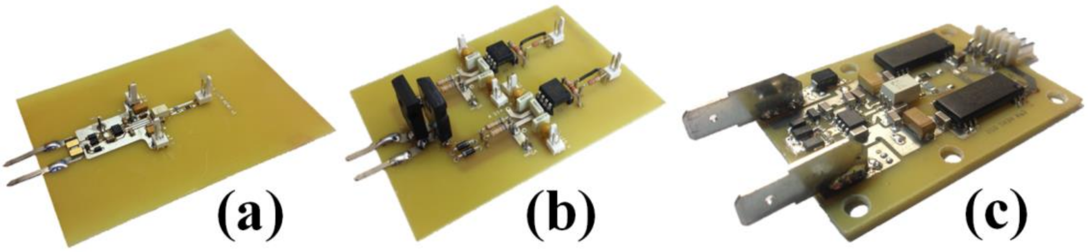


Fig. 3.2-1. Test vehicles for implementing a BDS from (a) GaN HEMTs and (b) RB-IGBTs; and (c) GaN HEMT SSR functional prototype. Figure extracted from [1].

3.2.2 SSR Test Vehicles Development

The driving conditions and control complexity of each solution is used to implement a set of different test vehicles based on the different power devices. A total of twenty implementations have been developed and evaluated, from which thirteen are based on different device technologies and semiconductor structures. Their operation is conditioned by the number of required power devices, the way they are arranged in the BDS and their driving requirements: voltage/current control, operating modes (normally-on/normally-off), etc. Therefore, particular driving circuitry is designed for each solution.

An example of some of them is shown in Fig. 3.2-1 (a)-(b).

On the one hand, the complexity of the control system is subjected to analysis in view of the following characteristics:

- Number of combined devices and their interconnection scheme.
- Switching characteristics.
- Operating modes.
- Number of required power supplies.
- Number and type of the required drivers.
- Control signals.

In addition, the power losses of the control system are also evaluated, with the following data collected for each solution:

- Input power losses (related to control signal) for each type of driver.
- Voltage between terminals for each power source present in the control stage of the BDS in both states:

    - On-state (BDS in conduction)
    - Off-state (BDS in open circuit)
- Average current consumption for each power source under the aforementioned conditions.

From this information, on-state and off-state power losses are calculated, together with an average power consumption for comparison purposes.

Finally, the cost for each implementation is calculated, based on the quotations provided by the biggest electronic devices suppliers, including the isolation and driving requirements, power sources and passive elements.

Publication [1] provides a qualitative analysis of the obtained results concerning the control stage characteristics. This topic can be critical concerning the production of SSRs at industrial level, where the cost of every part is critical for obtaining a reasonable commercial success. The performed analysis shows the main trends concerning the control stage characteristics and issues, although in this work the power stage analysis is focused more in detail.

3.3. Evaluation of Performances and Characteristics

3.3.1 Static Analyses and FOM Definition

In the studied framework, the BDSs are commutated at very low switching frequencies. Therefore, it exists a clear predominance of the conduction power losses above the switching power losses. For this reason, the static *I-V* curves for each BDS test vehicle are extracted in forward and blocking modes, using standard curve tracers (TEK 371A).

The characterization data provides the basic set of parameters to compare the considered devices among and to understand their behaviour under operation. However, a static analysis based on those measurements allows only a comparison between specific device references. This analysis can be enhanced from the extraction of the devices active areas and expressing the static characteristics in terms of current density. However, those areas cannot be precisely differed from the whole chip size.

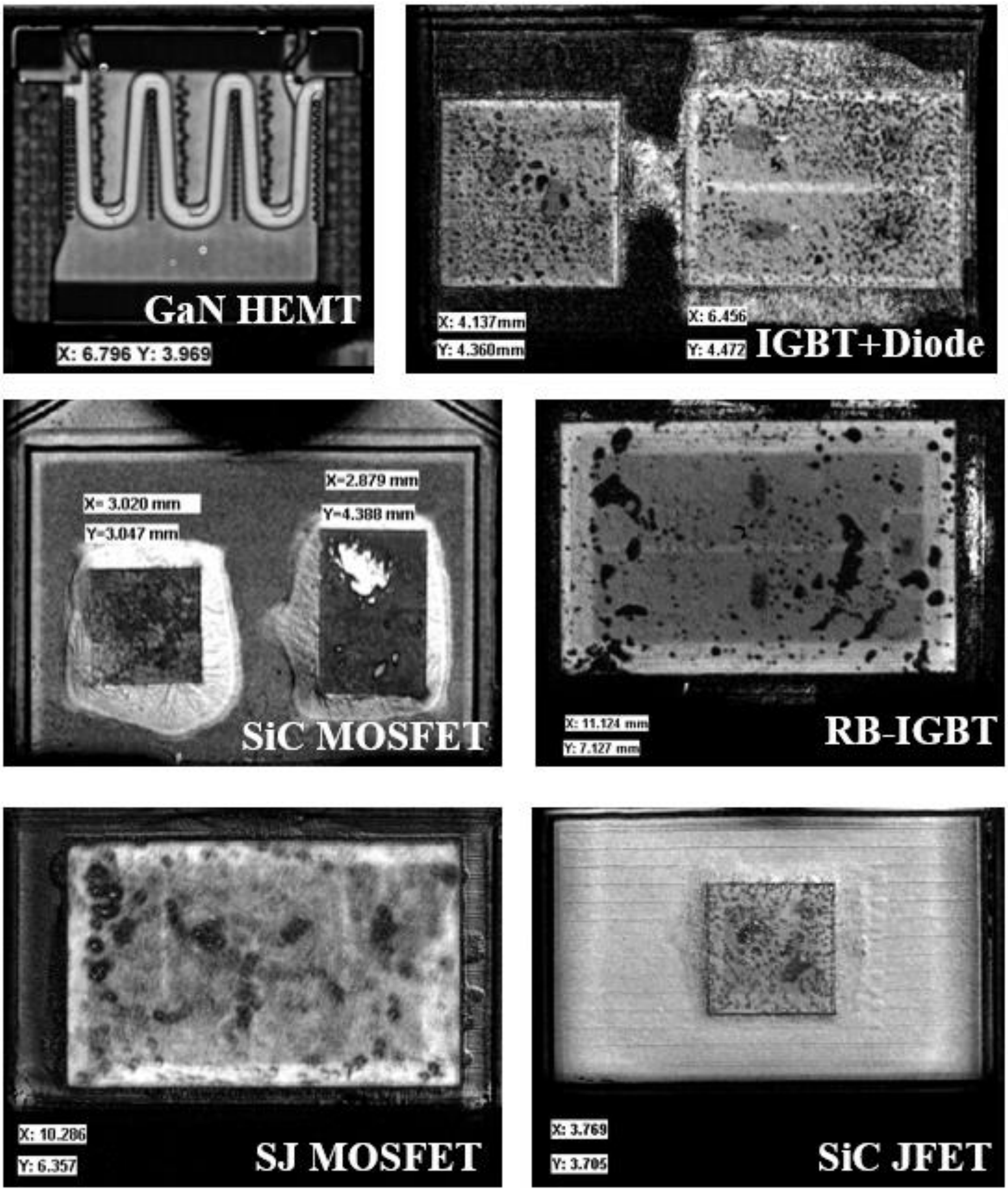


Fig. 3.3-1. Bare die areas of several power semiconductor devices.

Therefore, using a Scanning Acoustic Microscope (SAM) Sonoscan GEN-5 the devices bare die areas are measured (Fig. 3.3-1) and the static current densities (J_D) are obtained.

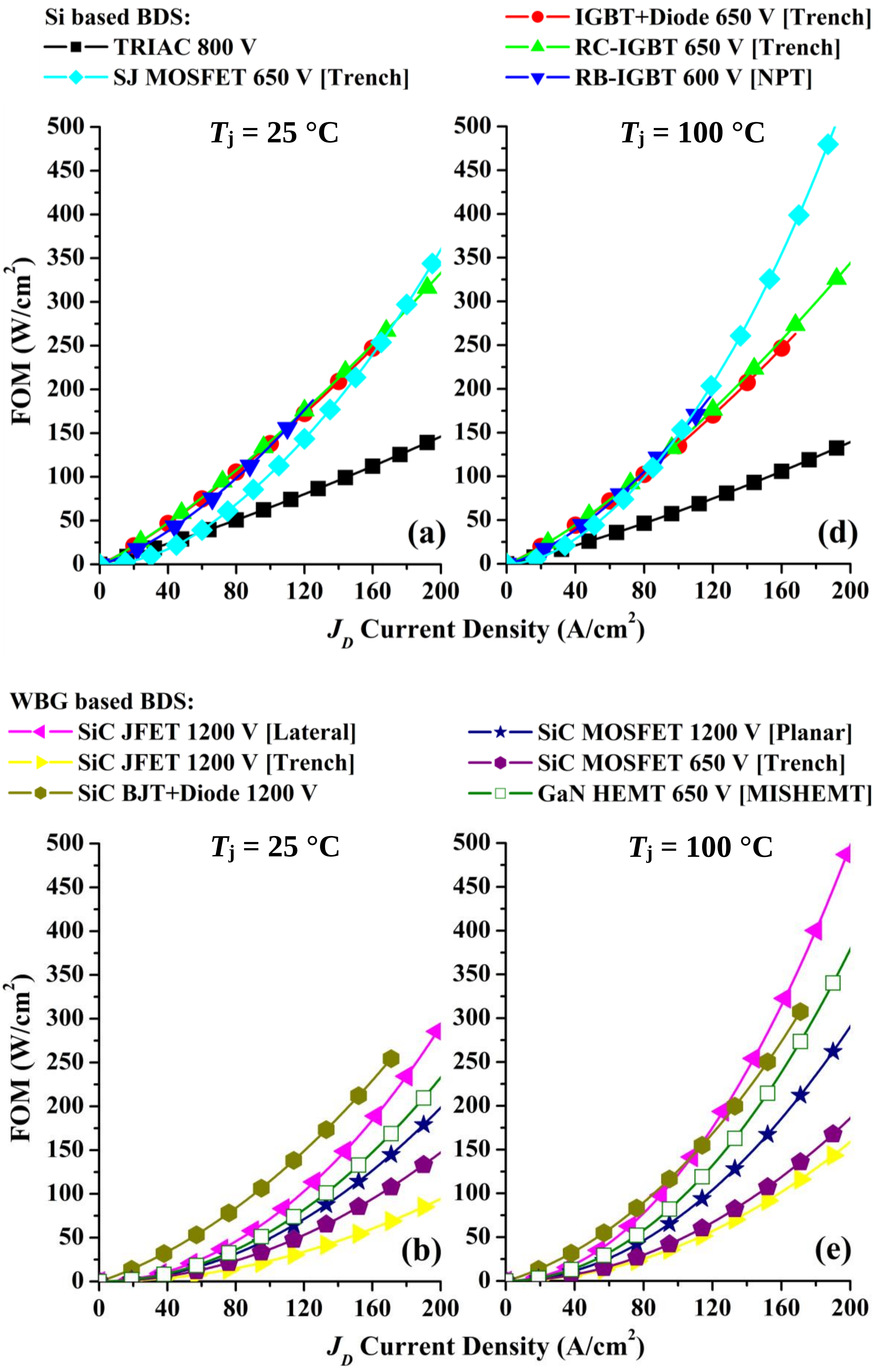
As a result, J_D-V_{BDS} curves are calculated for each solution, so that the static analysis can be extended from specific references to device technologies. In this calculation, the bare die areas are totalled when more than one device is simultaneously conducting current (i.e. GaN or SiC cascodes).

Still, the devices performance concerning their conduction power losses are highly dependent on their current waveform amplitude and morphology. In the literature, the existent FOM for high-frequency converters apply for evaluating the power density among different semiconductor materials [81] or different technologies of the same power devices [82]. However, any of them applies for the comparison of different power semiconductor devices (and different technologies) operating in SSRs involving AC currents and voltages. Therefore, to perform a representative evaluation of the different power devices technologies for IH (or inductive load applications, in general), a FOM with a tolerable cross-correlation is defined as the dissipated power per semiconductor unit area for a sinusoidal current density ($J_D(t)$) with amplitude (J_D) and period T_p (1):

$$\mathrm{FOM}(J_D) = \frac{1}{T_p} \int_{t\,=\,0}^{t\,=\,T_p} J_D(t) \cdot V_{\mathrm{BDS}}(J_D(t)) \cdot dt \qquad (1)$$

where $J_D(t) = J_D \cdot \sin(2\pi t/T_p)$. This FOM is presented in Fig. 3.3-2 into three categories, depending on the semiconductor material of the involved technologies under test: Si, WBG and hybrid (cascodes based on Si and WBG devices combination). In addition, the operating temperature in a real application is also considered in this analysis, as it will differ from the studied at 25 °C. In order to evaluate how the BDS performances are influenced by the effect of the operating temperature, the FOMs are also calculated when T_j = 100 °C is imposed.

All acquired experimental data is processed and arranged in publication [1] where a comprehensive comparative analysis among the studied devices and a discussion of the main conclusions is assessed.


Si based BDS:
TRIAC 800 V
SJ MOSFET 650 V [Trench]
IGBT+Diode 650 V [Trench]
RC-IGBT 650 V [Trench]
RB-IGBT 600 V [NPT]
T_j = 25 °C
T_j = 100 °C
(a)
(d)
FOM (W/cm^2)
0
50
100
150
200
250
300
350
400
450
500
0
40
80
120
160
200
J_D Current Density (A/cm^2)
WBG based BDS:
SiC JFET 1200 V [Lateral]
SiC JFET 1200 V [Trench]
SiC BJT+Diode 1200 V
SiC MOSFET 1200 V [Planar]
SiC MOSFET 650 V [Trench]
GaN HEMT 650 V [MISHEMT]
T_j = 25 °C
T_j = 100 °C
(b)
(e)
FOM (W/cm^2)
J_D Current Density (A/cm^2)

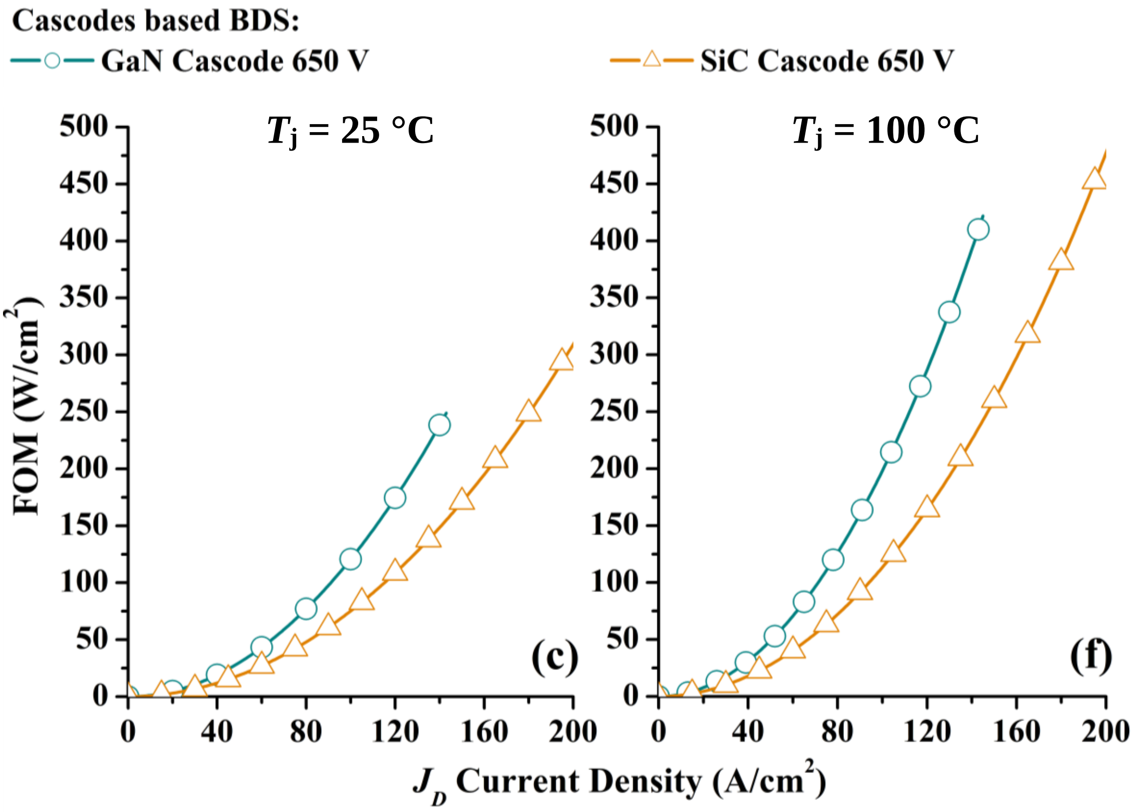


Fig. 3.3-2. FOM vs J_D at 25 °C and 100 °C for (a, d) Si, (b, e) WBG and (c, f) cascodes based BDS respectively. Figure extracted from [1].

A summary of the main conclusions reached from the performed static analysis is presented:

- Si based BDS are scarcely affected by the temperature (except for SJ MOSFETs), while WBG devices are highly affected.
- Power TRIACs highlight the lowest (the best) FOM of the many Si based solutions followed by Si SJ MOSFETs.
- 1200 V trench SiC JFETs present the better performance when compared to 650 V WBG based BDS, closely followed by trench and planar SiC MOSFETs and GaN HEMTs.
- 650 V cascoded SiC JFET alternative presents a better performance than that of the cascoded GaN HEMT.
- It exists a close proximity between SiC based devices and GaN HEMTs power densities.
- Current scalability of the BDS solutions by the power devices parallelization is possible, except for the case of the TRIAC.

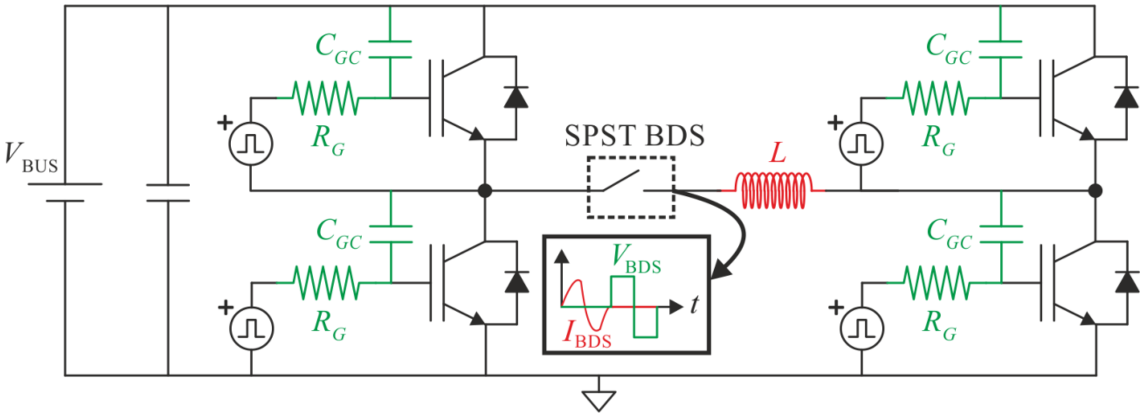


Fig. 3.3-3. Schematic of the designed test platform with flexible *dV/dt* (green) and/or *dI/dt* (red) adjustment. Figure extracted from [1].

In addition, Publication [1] addresses the power stage analysis in view of its characteristics, integration and power losses and costs.

3.3.2 Dynamic Analyses

A specifically designed test platform is designed and fabricated for studying the response of the different analysed technologies under the power multiplexing conditions. It is based on a full-bridge topology where the SSR under test is series-connected with an inductive load. The schematic of the designed test platform is depicted in Fig. 3.3-3. This setup permits to study the integrity of the high-frequency AC currents (tens of kHz) delivered to the load through the different relay technologies. Therefore, short duration (few periods) AC voltages and currents with the same *dV/dt* and *dI/dt* than the ones found in induction cookers and reproducing the power multiplexing scenario are applied to the test vehicles, while providing enough flexible parameters to guarantee a complete analysis.

Critical aspects such as zero-current crossing issues and controllability of the solutions are relevant results of this study.

Concerning its implementation, a control board (Fig. 3.3-4 (a)) establishes the specific switching conditions (e.g. flexible dead times for the IGBTs, frequency of the output waveforms, etc.) using several potentiometers and a Complementary Metal-Oxide-Semiconductor (CMOS) dual monostable multivibrator. Moreover, a power board (Fig. 3.3-4 (b)-(c)) applies square and triangular voltage and current shapes at the inductive load, respectively. A picture of the designed boards mounted on a support structure is shown in (Fig. 3.3-4 (d)). In this platform, the achieved *dV/dt* and *dI/dt* values are flexible and can be modified independently:

- *dV/dt* values are adjusted through capacitances connected between the gate-collector terminals of the inverter switches (C_{GC}), which provide a rough tuning. In addition, using different gate resistance values (R_G) provides the *dV/dt* fine tuning.
- *dI/dt* can be independently modified by changing the load inductance (L) of the bridge.

Both capabilities have been experimentally demonstrated for *dV/dt* from 350 V/µs to 5000 V/µs and *dI/dt* from 40 A/ms to 7000 A/ms, as shown in Fig. 3.3-5. Moreover, a simplified SPICE simulation model of the whole platform is used to calculate the applicable C_{GC}, R_G and L values for a specified set of *dV/dt* and *dI/dt* test conditions.

The dynamic behaviour of the different BDS implementations is analysed when commutated from conduction to blocking state. To do so, first a 15 A current amplitude triangular AC current, with a *dI/dt* = 6765 A/ms, flows through the BDS. Then it is switched to blocking state at V_{BUS} = 300 V, with a *dV/dt* = 520 V/µs, and alternately subjected to a bidirectional voltage between its terminals. This test evaluates the devices susceptibility to spurious turn-on impulse by the high *dV/dt* values. The mentioned *dV/dt* and *dI/dt* values are typical of IH appliances under real operating conditions.

Fig. 3.3-6 depicts some of the experimental results of the dynamic tests, for reference. In those graphs:

- Green waveforms are the BDS control signal V_{CON}.
- Blue waveforms represent the current through the BDS, I_{BDS}.
- Black waveforms are the voltage drop between the BDS terminals, V_{BDS}.
- Orange waveforms illustrate the collector-emitter voltage at the lower left IGBT ($V_{CE(\mathrm{LL})}$) of the test platform bridge.

As shown in Fig. 3.3-6 (a), GaN HEMTs based BDS successfully passed the dynamic tests. Instead, TRIAC is not capable of switching off due to the high *dI/dt* zero crossing current. The full experimental results are discussed in Publication [1].

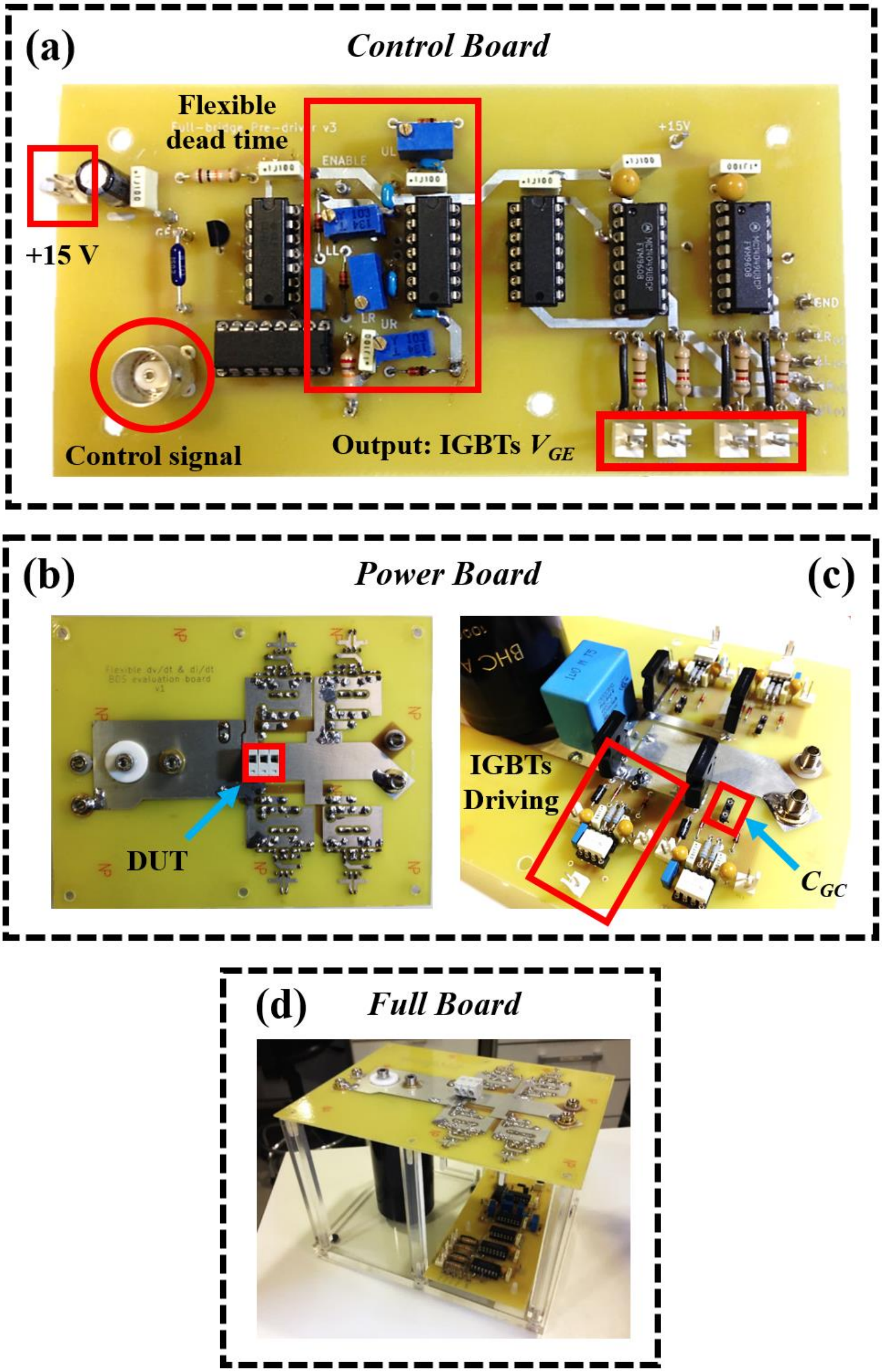


Fig. 3.3-4. Detailed view of the (a) control board and (b, c) up side and bottom side of the power board and (d) full board picture.

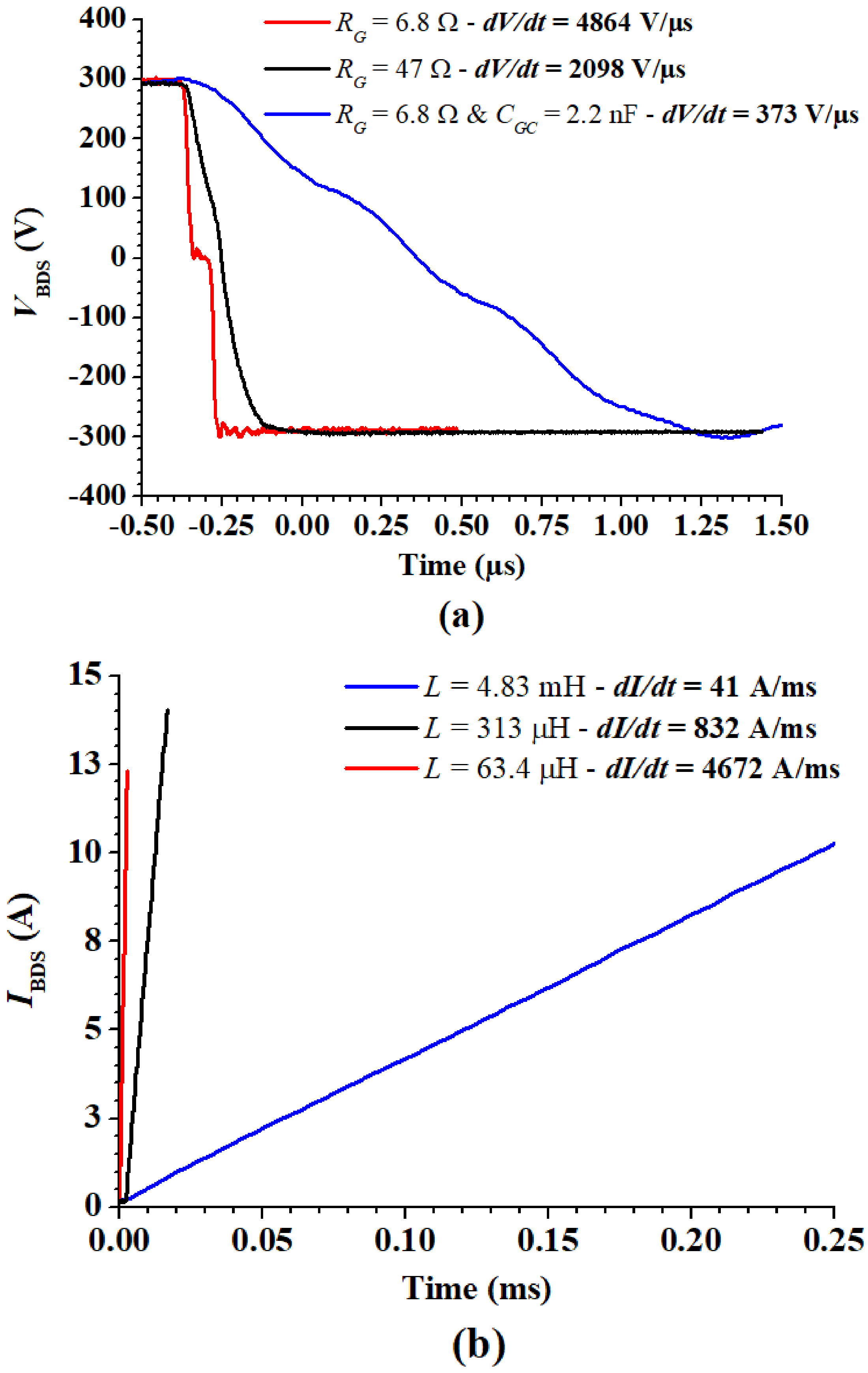


Fig. 3.3-5. Voltage (a) and current (b) waveforms showing different *dV/dt* and *dI/dt* values applied to the SSR test vehicles by the developed test platform.

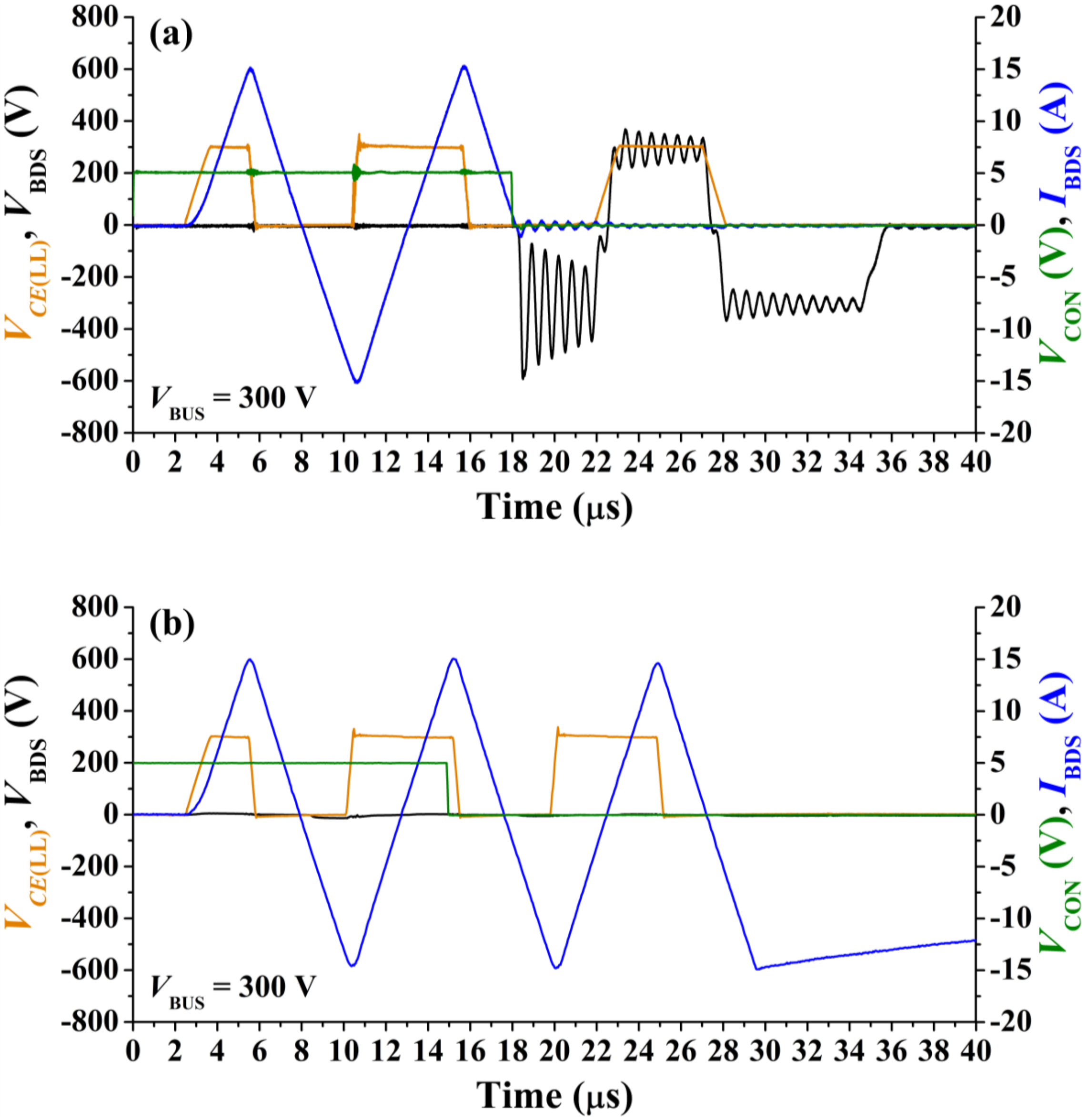


Fig. 3.3-6. Dynamic analysis of (a) GaN HEMTs and (b) Si TRIAC based BDS at different applied V_{BUS} voltages. Figure extracted from [1].

3.3.3 Simulation of the Voltage Oscillations

Except for the TRIAC, in a functional BDS it is expected that at the blocking instant I_{BDS} reaches zero just while the BDS starts to withstand V_{BUS}. Then, the parasitic RLC elements of the test circuit induce voltage and current oscillations. The different contributions depending on the evaluated BDS are dependent on the devices non-linear parasitic capacitances.

Moreover, possible models are developed for circuital simulation in order to understand the behaviour of the DUT. To investigate the zero-crossing current and consequent voltage overshoot during turn-off of the BDS, simulation of a SSR based on two standard IGBTs (blue solid line) and another SSR based on two IGBTs with increased parasitic collector-emitter capacitance (C_{CE}) (red solid line) are run. The test results are depicted in Fig. 3.3-7.

As it has been demonstrated from experimental results and simulation, the amplitude and frequency of the current oscillations are linked to the devices output capacitances (C_{OSS}). This fact explains the lower oscillation frequencies observed in slower devices with higher output capacitances.

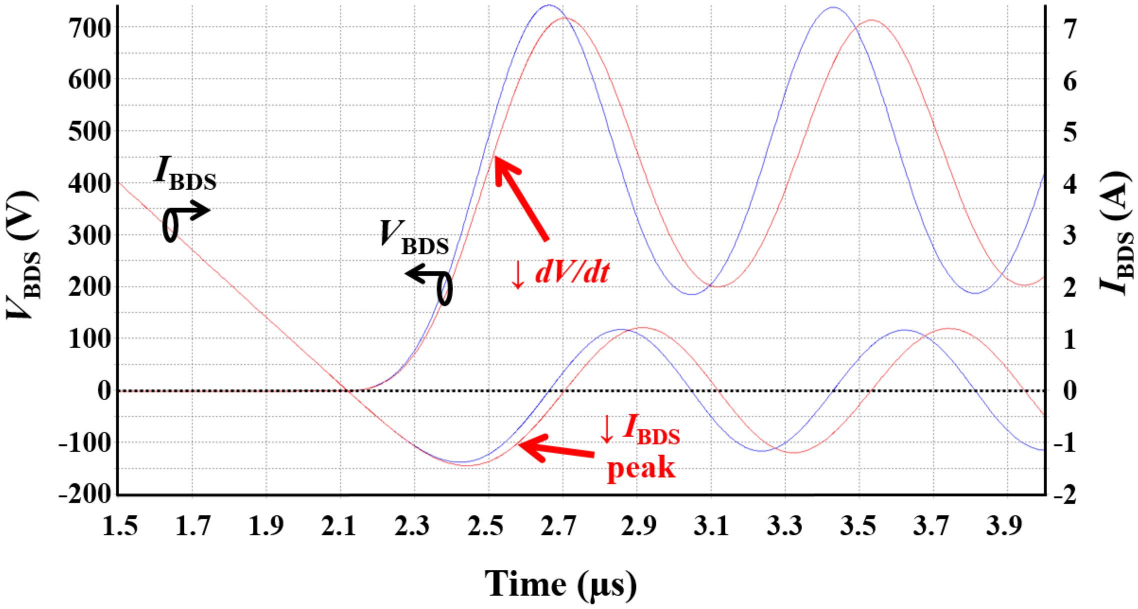


Fig. 3.3-7. SPICE Simulation: SSR BDS based on standard IGBTs (blue line) vs SSR BDS based on IGBTs with increased C_{CE} (red line)

3.3.4 SJ-based BDS Abnormal Behaviour

One of the findings of this PhD Thesis is the description of the abnormal behaviour of promising semiconductor technologies for implementing the BDS function which have not been reported before.

A remarkable result concerns the SJ MOSFET based BDS. As shown in Fig. 3.3-8, once this solution is switched to blocking state, two problems are immediately evident: first, an abnormal voltage peak close to the device nominal BV, even at a low 150 V V_{BUS} voltage. Second, the significantly high-current peaks flowing through the devices after turn-off. Those behaviours are linked to the devices internal structure, based on highly doped pillars, and the response of the inductive load to its carrier dynamics. Further analyses are undertaken in Publication [4], where FEM based simulations help to elucidate the motivation of such oscillatory phenomena.

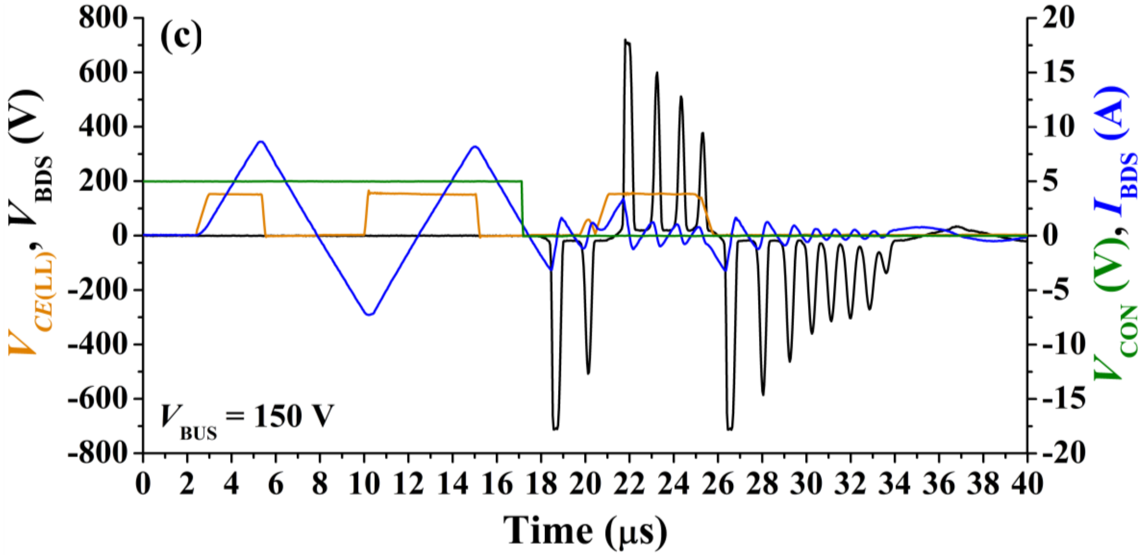


Fig. 3.3-8. Dynamic analysis of (a) SJ MOSFETs V_{BUS} = 150 V. Figure extracted from [1].

3.4. Functional Prototype and Final Application Test

From all the studied solutions, the most promising one (GaN HEMTs based BDS) is fully optimized in terms of its integration characteristics and thermal management issues (Fig. 3.2-1 (c)), implemented into an optimized prototype and tested in an induction cooker application for its characterization under real working conditions, using three heatsinks with different thermal resistances (Fig. 3.4-1). Such tests provided quantitative information related with the thermal management versus level of integration trade-off in this innovative SSR solution. This is one of the more critical aspects to be considered for the practical implantation of this kind of solutions due to the impact of the cooling components on the cost, on the system integration and on the system reliability.

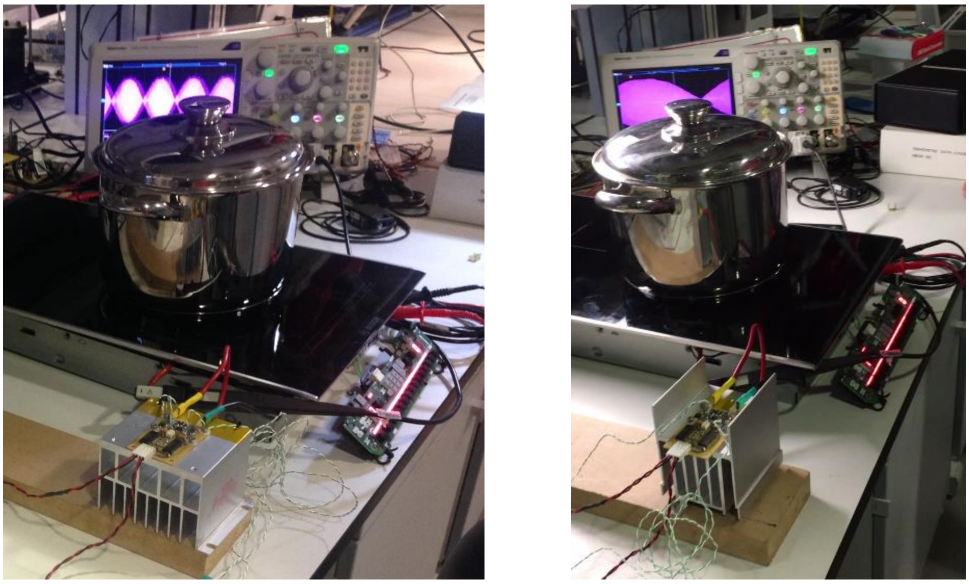


Fig. 3.4-1. GaN HEMT based BDS prototype mounted in two heatsinks.

3.5. Conclusions

This work demonstrates that improved SSR alternatives to the EMRs are possible in home appliances applications. Concerning their static *I-V* characteristics, all considered solutions have demonstrated to be applicable for implementing the BDS function. Those based on bipolar devices highlighted an off-set voltage which may result in slight distortions of the AC currents/voltages at the BDS in the zero-crossing region. This may not represent a remarkable problem in practical applications but an increase of the power losses. Conversely, GaN HEMTs, SiC MOSFETs and SiC JFETs based BDS experienced a symmetrical conduction in the first and third quadrants with the lowest conduction voltage drops.

Concerning the dynamic analysis, several technologies have been identified to suffer from anomalous behaviours (TRIAC, SJ MOSFET and RC-IGBT). Conversely, SiC MOSFETs, SiC JFETs and, to a lesser extent, SiC BJT+diode based BDS highlight excellent dynamic characteristics, with higher driving requirements for JFET and BJT, and a less expected costs drop in the short/medium-term than GaN HEMTs. In addition, GaN HEMTs based BDS presented outstanding static, dynamic and integration characteristics, being the best candidates to replace the EMRs. Moreover, their thermal management issues will become less relevant as the technology maturity will increase.

A more in deep analysis of the benefits and drawbacks of each solution is derived from the experimental results in Publication [1].

Concerning the BDS implementation based on GaN HEMT has been proposed to become patented [5][6].

Chapter 4: RUGGEDNESS AND RELIABILITY STUDIES IN POWER SEMICONDUCTOR DEVICES FOR IH

4.1. Objectives and PhD student's role

In this chapter, the limit in thermal generation under high current conduction based on [34], while the device withstands V_{BUS}, is explored in IGBTs and GaN HEMTs. In order to evaluate the effect of the IGBTs V_{GE} and adapt the test at the final application requirements, SC I tests are conducted setting V_{GE} as:

- V_{GE} = 20 V (which helps to reduce on-state losses) as is conventionally used in IH applications. This can also derive from a conception device point of view, as the main applications set them at 15 V. Moreover, Trench IGBTs with non-rated SC capability could present filamentary behaviour leading to oscillations. This has been observed in high voltage devices, but not in the medium voltage case.
- V_{GE} = 15 V will be also analysed, as semiconductor manufacturers have established this value as the usual one for IGBT conduction, as reference value.
- V_{GE} = 10 V to reproduce the following high dissipation condition: an overcurrent event due to the snubber discharge when the maximum current is passing through the device as a consequence of losing ZVS, as presented in [34].

In the case of GaN HEMTs, an exploratory study is done. Recently, 600-650 V GaN HEMTs have been introduced in the market. Aside for motor drive applications [83][84], they show a promising potential to be used in induction cookers, either for implementing a SSR BDS (as shown in Chapter 3) or for the replacement of the IGBTs at the power inverter [85]. In this framework, they should withstand also such SC condition previously explored for IGBTs to meet with the IH ruggedness requirements. These technologies present a significantly low maturity and it exists a significant lack of knowledge on their SC behaviour. Furthermore, SC tests allow evaluating if, for a given V_{BUS}, t_{on} is long enough so that the SC condition can be detected by a controller or driver, and safely interrupted by switching-off the tested device with no electrical damage for the power converter [37], as previously stated. According to the available drivers, the fault detection time is conservatively estimated to be below 6 µs [38]. However, a certain margin is left: i.e. in the case of IGBTs, it is conventionally used t_{on} = 10 µs. Nevertheless, a remarkable reduction on the gate driver response time has been achieved, which depending on the requirements on the final application may compensate for the difference in costs: e.g., 360-600 ns for SiC based devices [86] or 200 ns for GaN HEMTs [87]. Consequently, both SC I and SC II tests have been performed. Such results regarding GaN HEMTs are covered in the publications of the compendium presented in leading power semiconductor devices conferences and journals: [7]-[9].

In all this work, the PhD student performed the tests and deeply analysed all the experimental results, assisted by TCAD simulations. The set-up for SC tests was already available at IMB-CNM before starting the PhD thesis.

4.2. SC Test Platform Description

In this section, the designed test platform for performing SC I and SC II tests is briefly described. Fig. 4.2-1 (a) depicts the schematic of the SC test bench including the board parasitics (R_{σ}, $L_{\sigma,1}$ and $L_{\sigma,2}$), a DC power supply (V_{BUS}) and a capacitors bank (C_{BUS}) which stores the energy for the SC events. A gate driver, with a driving voltage, V_G, is used for controlling the gate turn-on and -off of the DUT, while customizable gate resistors ($R_{G(\mathrm{on})}$ and $R_{G(\mathrm{off})}$) are used for limiting the gate current (I_G). A coaxial shunt (R_{Shunt}) is used to monitor the drain/collector current (I_D, I_C), while differential voltage probes are used for measuring $I_{G(\mathrm{on})}$ (I_G sensed at $R_{G(\mathrm{on})}$), the drain-source/collector-emitter voltage (V_{DS}, V_{CE}), and the gate-source/gate-emitter voltage (V_{GS}, V_{GE}).

For performing SC II tests, 8 complementary IGBTs connected in parallel are added to the previous design together with a Free Wheeling Diode (FWD), and a 300 µH inductive load (L), as shown by Fig. 4.2-1 (b). Some pictures of the developed platform and detailed views of a DUT and the developed driver are shown in Fig. 4.2-1 (c)-(e), respectively.

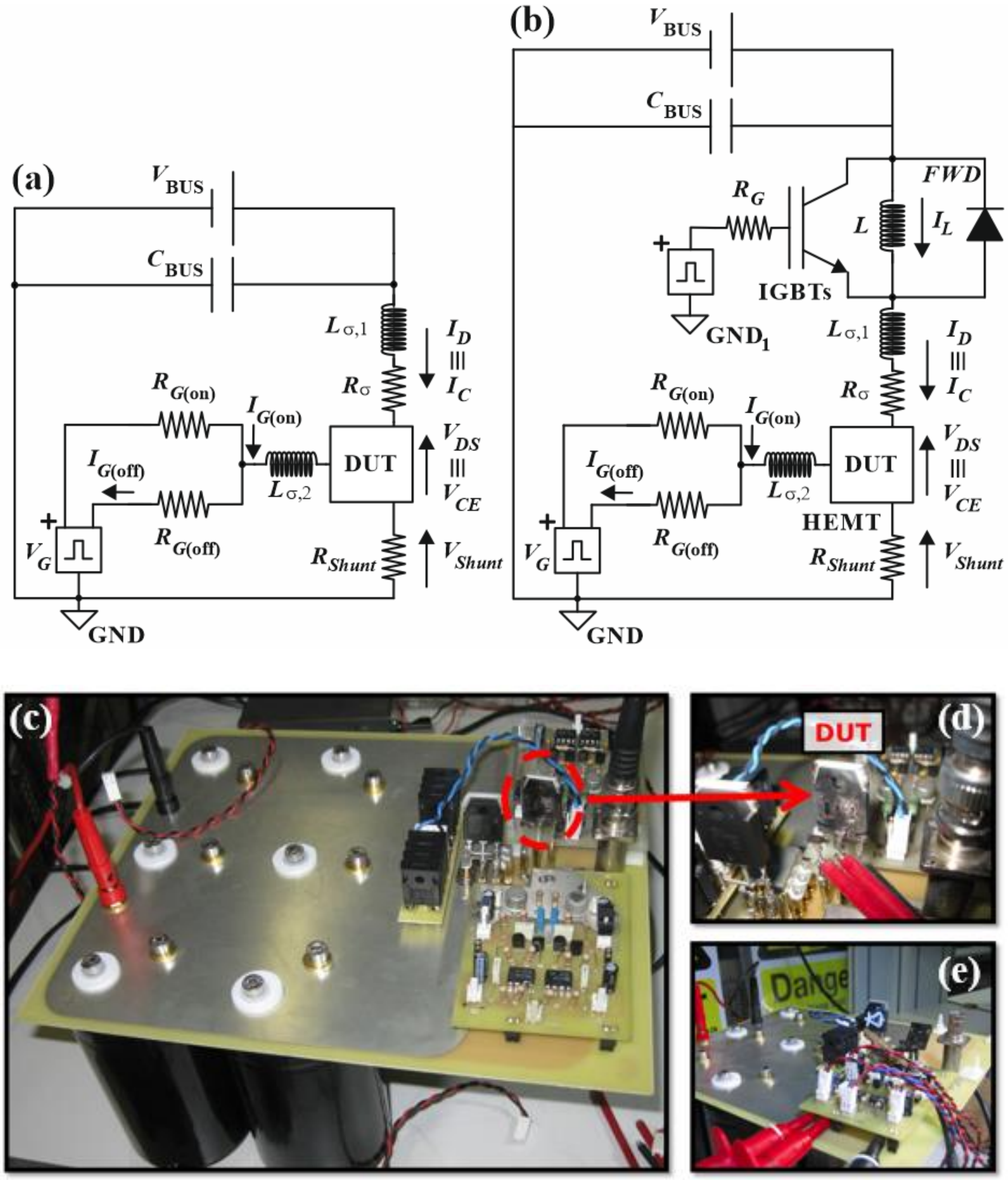


Fig. 4.2-1. Schematic of the designed test setup for (a) SC I and (b) SC II. Illustration of (c) the developed platform and detailed views of (d) a DUT and (e) the used driver.

4.3. Selected IGBTs, Test Conditions and Results

Five different field stop trench IGBT references have been selected for a SC endurance evaluation. Each of them is encapsulated in TO-247 with antiparallel diodes, some in co-pack and, the rest, monolithically. Four of these references are conventionally used for IH appliances, and any of them is SC rated. A fifth SC rugged device (RC-IGBT) has been included for reference. SC tests have been performed at V_{GE}

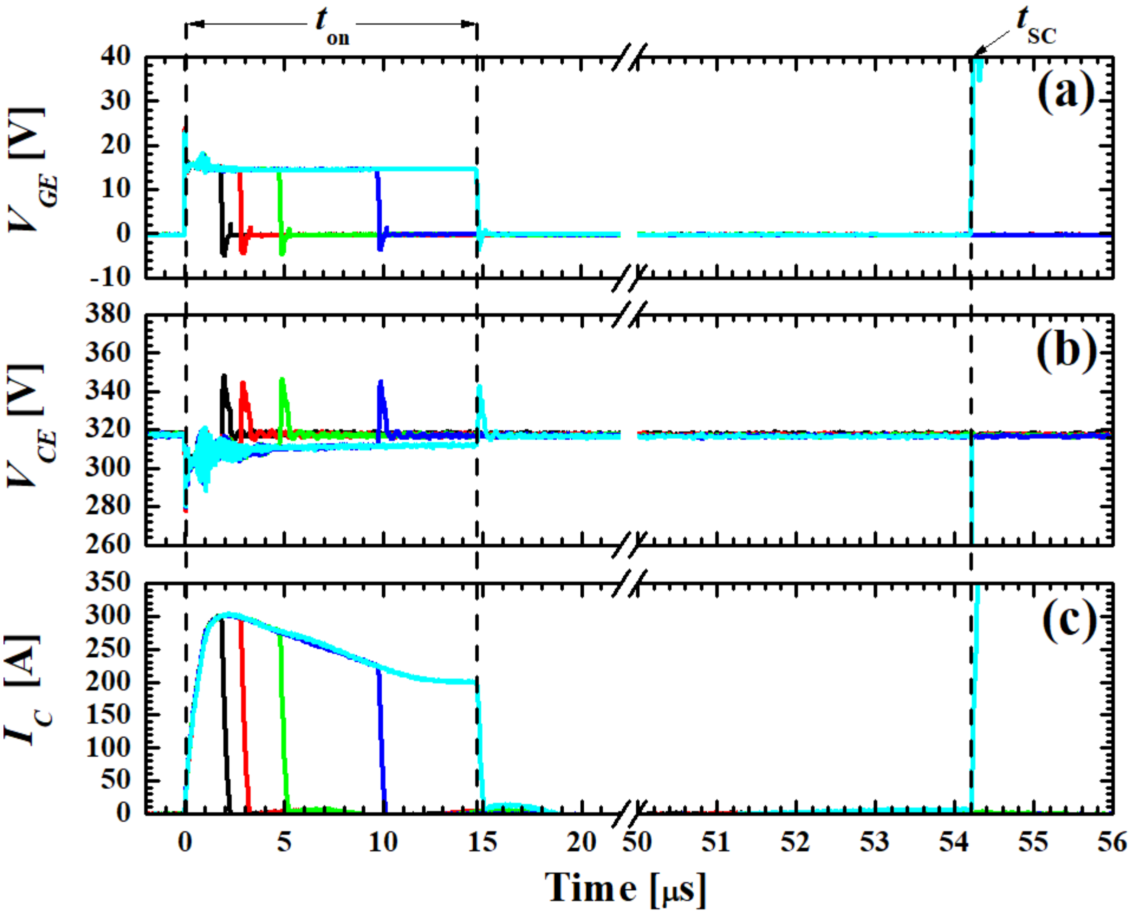


Fig. 4.3-1. Non-destructive (black, red, green and blue solid lines) and destructive (cyan solid line) SC rated RC-IGBT SC experimental waveforms results for V_{BUS} = 320 V, V_G = 0 / 15 V, $R_{G(on)}$ = $R_{G(off)}$ = 10 Ω: (a) V_{GE}, (b) V_{CE} and (c) I_C.

= 10, 15 and 20 V, and the different failure mechanisms are investigated for each case. Moreover, a static parameter, useful for the prediction of SC capability, is identified. A brief summary of the obtained results is presented here. As a testing procedure, V_{BUS} = 320 V while t_{on} is increased in several steps up to the device destruction, as shown by Fig. 4.3-1 for SC rated RC-IGBT tested at V_{GE} = 15 V. In this test, the device is capable of withstanding a SC event for t_{on} = 10 µs. However, it fails 39 µs after a t_{on} = 15 µs SC event had finished (t_{SC} = 54.2 µs), due to the positive feedback of power and heat dissipation with collector-emitter leakage current (thermal runaway).

On the other hand, non SC rugged RC-IGBTs SC test results at V_{GE} = 15 V and 20 V are presented in Fig. 4.3-2 (a)-(c) and (d)-(f), respectively. Due to the higher transconductance (g_{fs}) of these devices, which correlates I_C with V_{GE}, a higher saturation current ($I_{C(sat)}$) is reached than that for the SC rated IGBTs. Moreover, dI_C/dt is

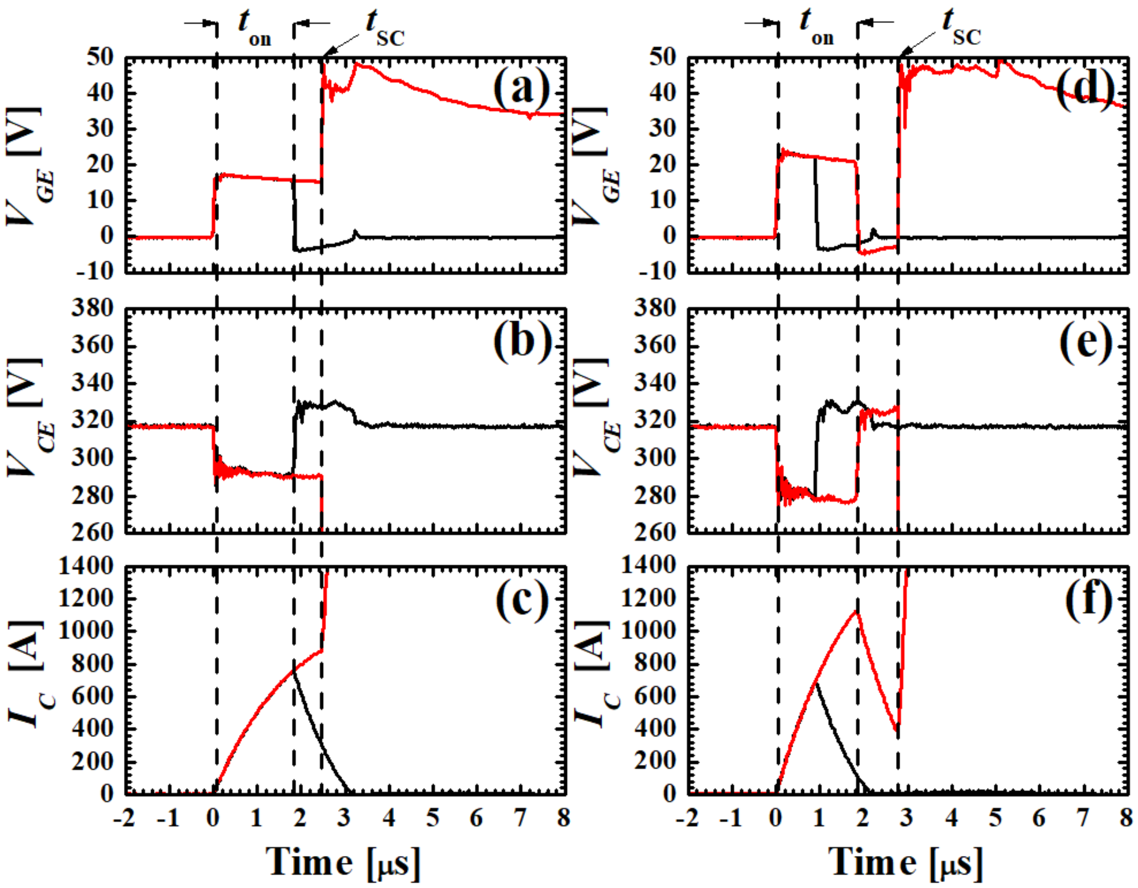


Fig. 4.3-2. Non-destructive (black solid line) and destructive (red solid lune) non SC rated RC-IGBT SC experimental waveforms results for V_{BUS} = 320 V, $R_{G(on)}$ = $R_{G(off)}$ = 10 Ω: (a)-(d) V_{GE}, (b)-(e) V_{CE} and (c)-(f) I_C at V_G = 0 / 15 V and 20 V, respectively.

substantially increased when V_{GE} is changed from 15 V to 20 V. Concerning V_{GE} = 15 V test, destruction is reached during the SC event owing to the high power dissipation. However, at V_{GE} = 20 V, the device is capable of withstanding a 2 μs SC event, but fails during turn-off due to the dissipated power during the SC pulse and the remaining turn-off commutation energy produced by V_{CE} overvoltage in combination with a decreasing, but still high, I_C.

Concerning co-pack IGBTs, Fig. 4.3-3 shows the SC test results at V_{GE} = 20 V. In this case, an oscillatory phenomenon is identified at V_{GE} and vanishes after 2 μs. Since those oscillations occur at the same point for the three performed tests, it is concluded that the device gate dielectric was damaged during the first SC event (black solid line) due to the high V_{CE} turn-off overvoltage. During second SC test (red solid line), where the device is subjected to a longer t_{on}, I_C marks a turning point on its way at the same instant in which the first SC event had been switched-off.

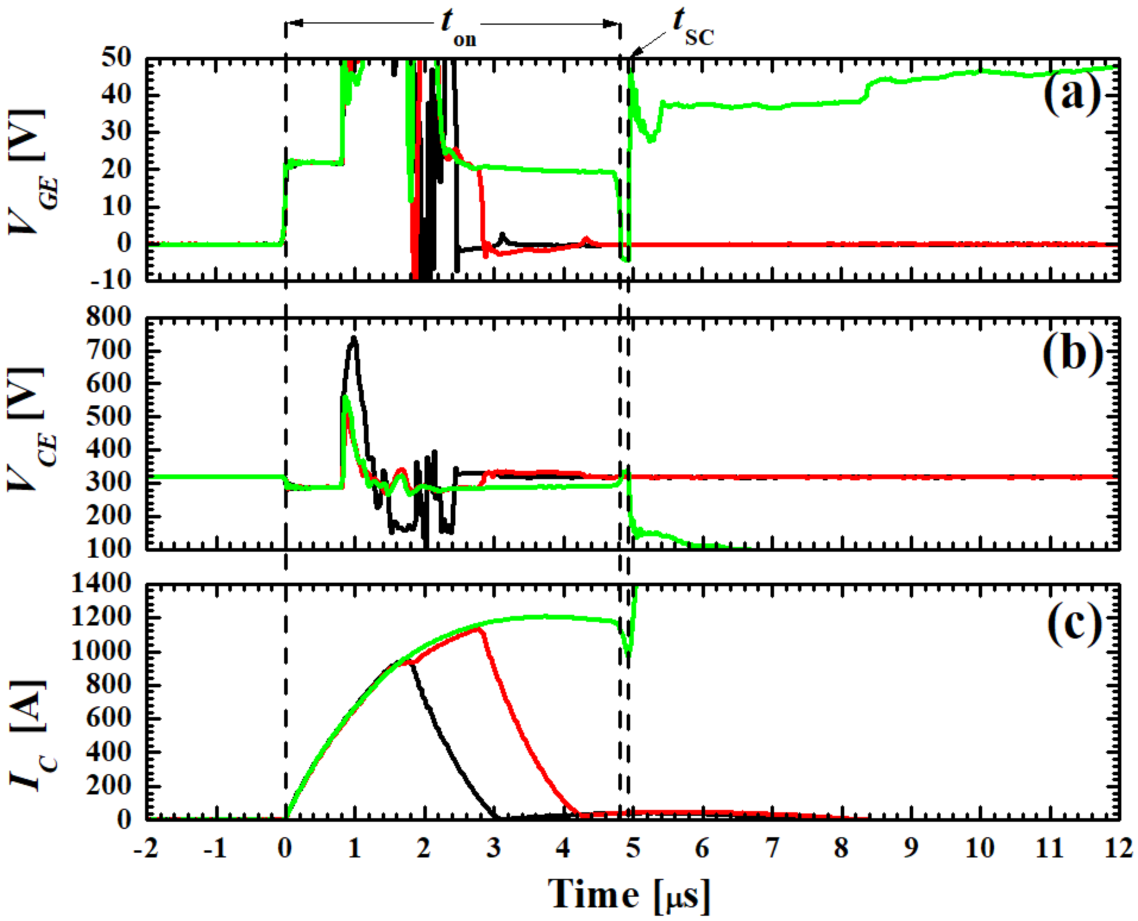


Fig. 4.3-3. Non-destructive (black and red solid lines) and destructive (green solid lune) co-pack IGBT SC experimental waveforms results for V_{BUS} = 320 V, V_G = 0 / 20 V, $R_{G(on)} = R_{G(off)}$ = 10 Ω: (a) V_{GE}, (b) V_{CE} and (c) I_C.

Similar results are obtained when V_{GE} = 15 V, as shown by Fig. 4.3-4, where the device is damaged at the second SC event (red solid line).

Moreover, co-pack device presents an intermediate value of g_{fs} compared to the previous tested references. Considering the SC tests at V_{GE} = 15 V, a midway $I_{C(sat)}$ and t_{SC} is reached for this reference.

Finally, the SC results at V_{GE} = 10 V are presented in Fig. 4.4-1 for a different co-pack reference, whose g_{fs} is close to the lowest value fixed by the first presented RC-IGBT. In this case, the device is capable of withstanding a SC event for 10 µs, and fails due to thermal runaway after a SC event for t_{on} = 15 µs.

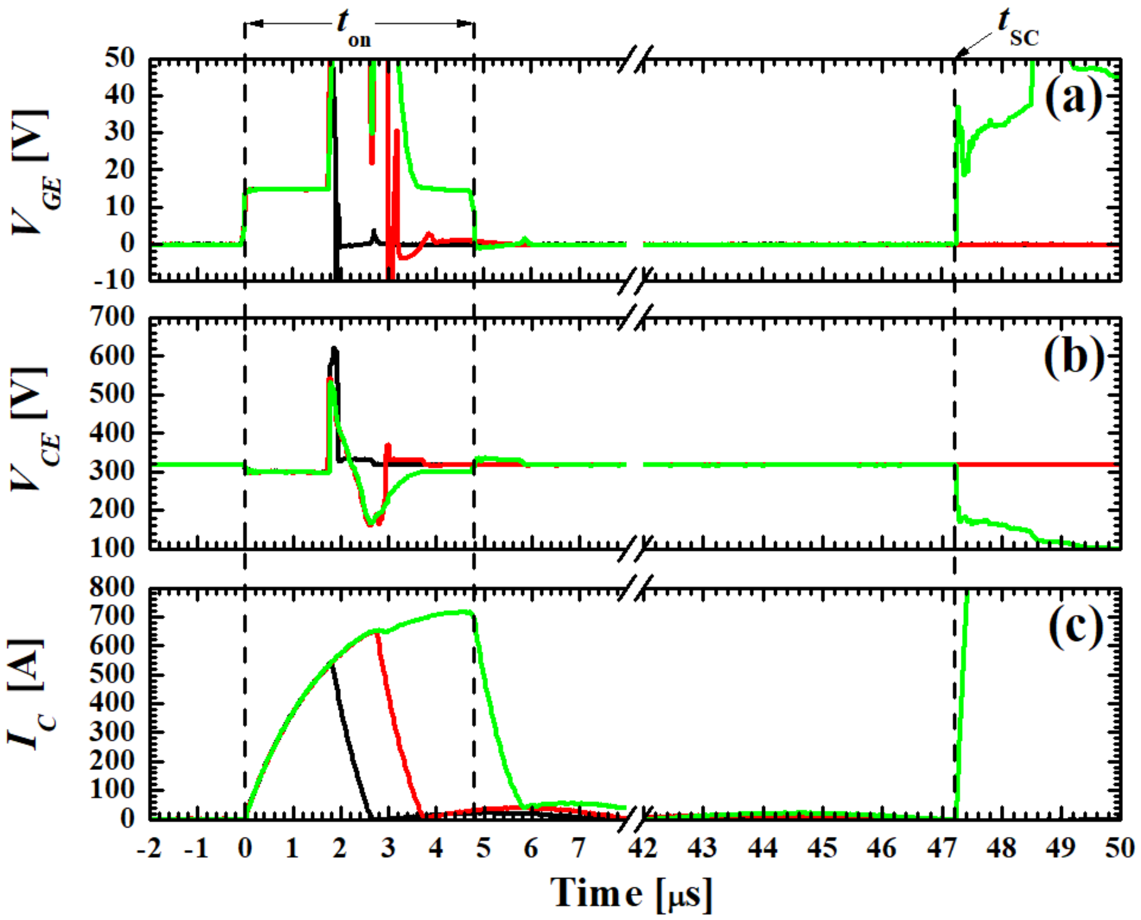


Fig. 4.3-4. Non-destructive (black and red solid lines) and destructive (green solid lune) co-pack IGBT SC experimental waveforms results for V_{BUS} = 320 V, V_G = 0 / 15 V, $R_{G(on)}$ = $R_{G(off)}$ = 10 Ω: (a) V_{GE}, (b) V_{CE} and (c) I_C.

4.4. Selected GaN HEMTs, Tests Conditions, and Results

Since only a few GaN HEMTs are commercially accessible as stated in Chapter 3, all the available normally-off options (p-GaN HEMTs, GaN MISHEMTs and GaN cascodes) are evaluated under SC conditions (SC I and II for p-GaN HEMTs and GaN MISHEMTs, and SC I only for GaN cascodes). GaN cascodes are encapsulated in TO-220, p-GaN HEMTs, in a Dual Flat No-lead (DFN) 8x8 packaging, and GaN MISHEMTs, in a Printed Circuit Board (PCB) embedded die packaging. More detail on their test conditions is provided in Publication [8]. As a testing procedure, V_{BUS} is ramped from 50 V to 400 V in steps of 50 V, while t_{on} is kept at 10 μs.

In Publications [8][9], it is presented a comprehensive analysis of their different performances in terms of the temperature distribution, SC dissipated energy (E_{SC}) and experienced I_D decrease during SC events. In addition, the physics of I_D reduction and an

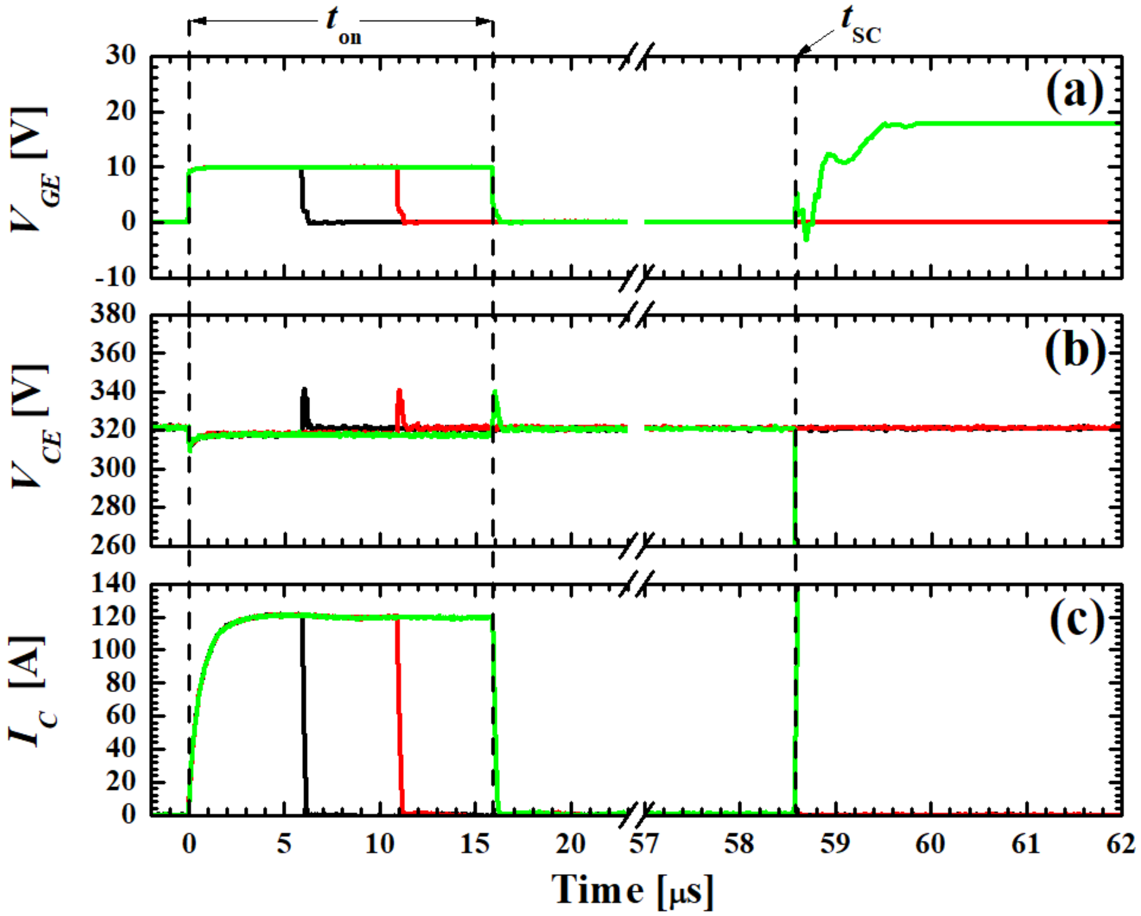


Fig. 4.4-1. Non-destructive (black, red and green solid lines) and destructive (blue solid lune) co-pack IGBT SC experimental waveforms results for V_{BUS} = 320 V, V_G = 0 / 10 V, $R_{G(on)}$ = $R_{G(off)}$ = 10 Ω: (a) V_{GE}, (b) V_{CE} and (c) I_C.

identified $I_{G(on)}$ high leakage during SC events are further analysed in [7]. To do so, experimental results have been compared to physics-based simulations. Fig. 4.4-2 (a)-(b) depict the good agreement between the measured and simulated I_D waveforms for a p-GaN HEMT, together with the time evolution of the simulated gate (T_{Gate}) and maximum temperatures (T_{Max}). In addition, the temperature distribution and absolute electric field ($|E|$) vertical profile at the field plate right edge (indicated by a dashed line through the structures in Fig. 4.4-2 (c) and (e)) are extracted at different times:

- t = 200 ns, when the saturation current ($I_{D(sat)}$) is reached (Fig. 4.4-2 (c)-(d)), and large $|E|$ is located at the Two-Dimensional Electron Gas (2DEG) channel, just beneath the edge of the field plate.
- t = 800 ns, when I_D has already experienced a severe reduction and is almost stabilized (Fig. 4.4-2 (e)-(f)), and the temperature has already reached its maximum.

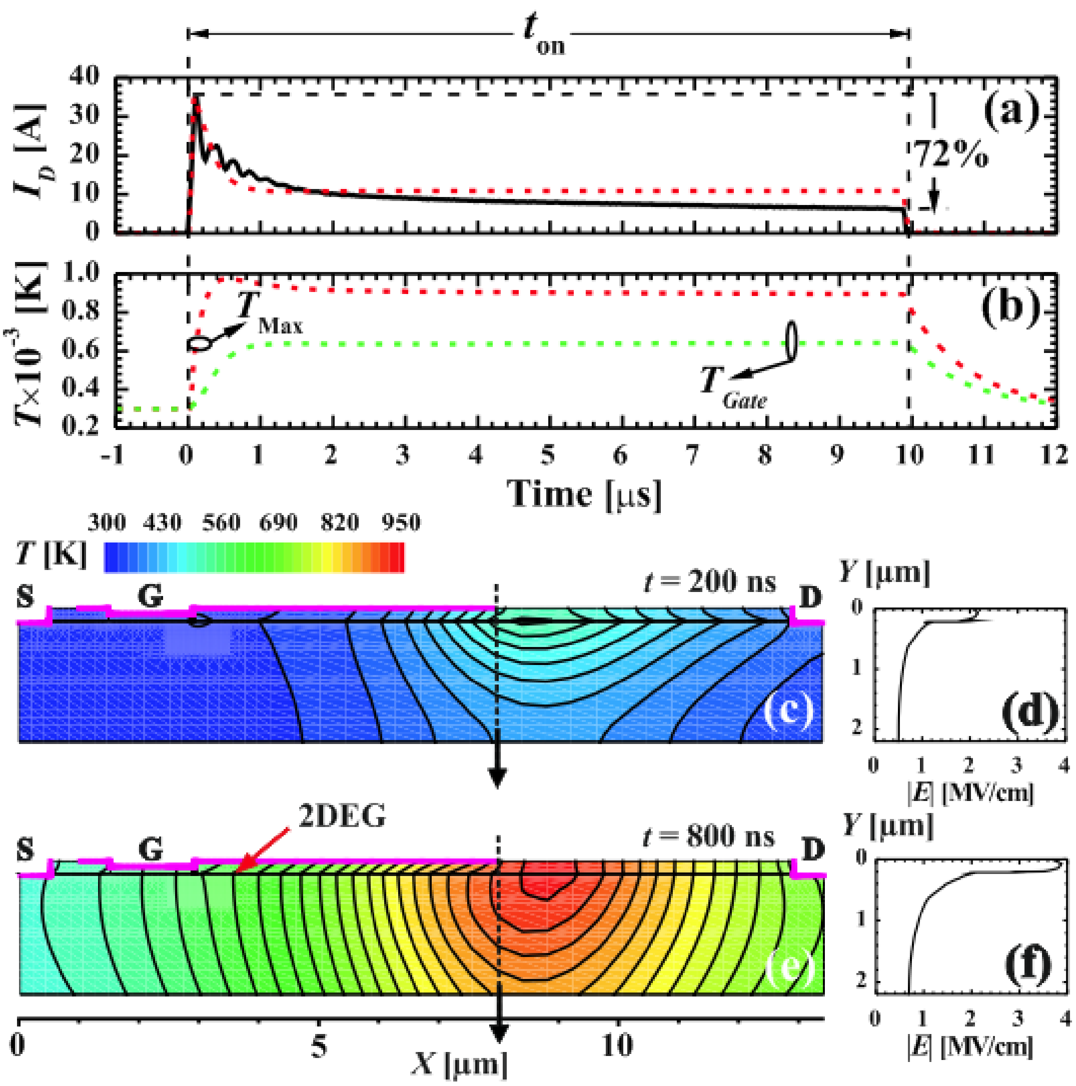


Fig. 4.4-2. Measured (black solid line) and simulated (red and green dashed lines) waveforms for (a) I_D, (b) simulated T_{Gate} (green) and T_{Max} (red), and temperature distribution in the p-GaN HEMT channel after (c) 200 ns and (e) 800 ns, with (d)-(f) absolute electric field (|E|) vertical profile (on the right) (black line) in a SC event for V_{BUS} = 350 V (non-destructive). Figure extracted from [8].

During this time interval, the maximum |E| is reached at the field plate right edge, right in the 2DEG channel. There, a high power density spot appears due to Joule effect, and the generated heat flows to the surrounding areas, leading to an increase of T_{Gate}. Since $I_{G(on)}$ increases with T_{Gate} [88]-[90], this provokes a decrease of V_{GS} due to a higher voltage drop at $R_{G(on)}$. However, as it is further explained in [7], the achieved $I_{G(on)}$ is not enough high to be the main responsible for the I_D decrease during the SC event, while the temperature dependence of the electrons mobility in the 2DEG channel is identified to be the principal cause of this phenomenon [7].

Moreover, the SC results have been compared to other technologies, and some recommendations for improving SC capability are also included [7][8].

4.5. Conclusions

The main conclusions about SC capability for each device concept are summarized here:

- IGBTs: When V_{GE} is increased up to 20 V, higher $I_{C(\mathrm{sat})}$ are reached. Then, the power dissipation at the device is higher and t_{SC} is drastically reduced. Therefore, a t_{on} = 10 µs SC event cannot be guaranteed. Moreover, from all tested devices, the SC rated RC-IGBT is the only one capable of withstanding a SC event for t_{on} = 10 µs at V_{GE} = 15 V, followed by a co-pack IGBT. Finally, the devices g_{fs} have been identified to keep an inverse relationship with t_{SC}.
- GaN HEMTs: None of the studied devices can withstand a SC I event at V_{BUS} = 400 V during t_{on} = 10 µs. EHEMTs have demonstrated to endure a SC I test at V_{BUS} = 300 V (MISHEMTs) and V_{BUS} = 350 V (p-GaN HEMTs), while GaN cascodes did not pass the tests for $V_{\mathrm{BUS}} > 150$ V [7]-[9]. Concerning SC II events p-GaN HEMTs have been capable of withstanding a V_{BUS} = 350 V SC II event for t_{on} = 17 µs, while GaN MISHEMTs only passed the SC II test at V_{BUS} = 250 V [9]. As a result of the performed analysis, it has been determined that the higher I_D decrease during the SC event of EHEMTs is caused by the thermal behaviour of their channel, while cascodes behaviour results from their different structure, driving and thermal characteristics [8].

As for SC failure in GaN HEMTs, an abrupt I_D rise with a null or low $I_{G(\mathrm{on})}$ leakage for cascodes and EHEMTs outlines a purely thermal destruction [7][8]. All devices fail during the SC event. In comparison to other available technologies, SJ and SiC MOSFETs present the best SC capability, mainly due to the low maturity of GaN devices and the lack of knowledge on their behaviour under SC conditions [8]. In this scenario, two main findings useful for SC protection strategies are provided. On the one hand, protection circuits require at least a 300 ns response to safely switch the analysed EHEMTs and GaN cascodes off [8][9] and, on the other hand, $I_{G(\mathrm{on})}$ monitoring under operation by means of a smart gate driver could be a good state indicator for SC prevention in EHEMTs [8].

Chapter 5: T_J EXTRACTION AND DEVICE WEAK SPOTS IDENTIFICATION UNDER REAL CONDITIONS

5.1. Objectives and PhD Student's role

In this chapter, several objectives are talked according to the needs identified in Chapter 1:

- Providing a die-level approach for power losses measurement, decoupling the effect of the snubber in such measurements,
- Inspecting the device surface current distribution at high switching frequencies to identify possible current crowding effects associable to the device weak spots,
- Setting a new approach for validating electro-thermal models under operation.

This activity has required developing a new set-up [10], in which the PhD student has focused his efforts. This set-up has consisted of developing a method to extract T_j of different power devices to obtain:

- Each component of power losses, i.e., conduction and switching, thanks to a specifically designed circuit that decouples them;
- Surface temperature and current distribution map to inspect the effect of driving concepts, such as operating outside ZVS condition or determining the effect of capacitive snubbers.

To this end, several experimental methods have been set up or/and performed by the PhD student: the capability for removing the top molding compound of the devices, the integration in a test platform of a modified half-bridge circuit and an IR camera to measure T_j under operation, and the extraction of the thermal impedance of the system. This work goes beyond the nowadays state-of-the-art and is reported in publication [10]. To complement this information and better explain several methodological aspects, this chapter presents the devices and set-up developed for T_j extraction, as well as some details of how the thermal impedance measurements and electro-thermal model has been performed.

5.2. T_j evaluation with an appropriate calculation of thermal losses

5.2.1 Selected Devices

First, the devices under test are defined. A total of five samples of a conventional IGBT 650 V and 40 A reference encapsulated in TO-247, commonly used in current induction cookers, are studied.

Initially, their conduction and switching dissipation models is revised according to the state-of-the-art. V_{CE}-I_C static characteristic curves are measured at two temperatures (ambient and working temperature) for conduction modelling using a curve tracer.

5.2.2 Test Setup Description I: Power Stage

The conduction and switching losses are decoupled from IR measurements: a new methodology based on measuring T_j of the device is carried out to check its contribution to the power losses. To do this a specifically designed test setup is developed, whose schematic is depicted in Fig. 5.2-1. This setup is based on a modified half-bridge topology with a flexible resistive (R_{eq}) and inductive (L_{eq}) load where an additional auxiliary switch (AUX) is used to separately extract the conduction and switching losses of the DUT, connected in series to AUX. It is necessary that the packaging moulding compound of the DUT is removed, so that both chips (IGBT and Diode) become accessible to perform the IR thermographies, while keeping functional their electrical behaviour. In addition, the DUT is mounted on a heat sink and externally monitored with embedded thermocouples.

To adjust the resonance current and frequency, customizable resonant capacitors (C_{res}) are used. In addition, configurable gate resistances (R_G), gate drivers and snubber capacitors (C_{snub}) allow an accurate commutation of the IGBTs under the specified switching conditions.

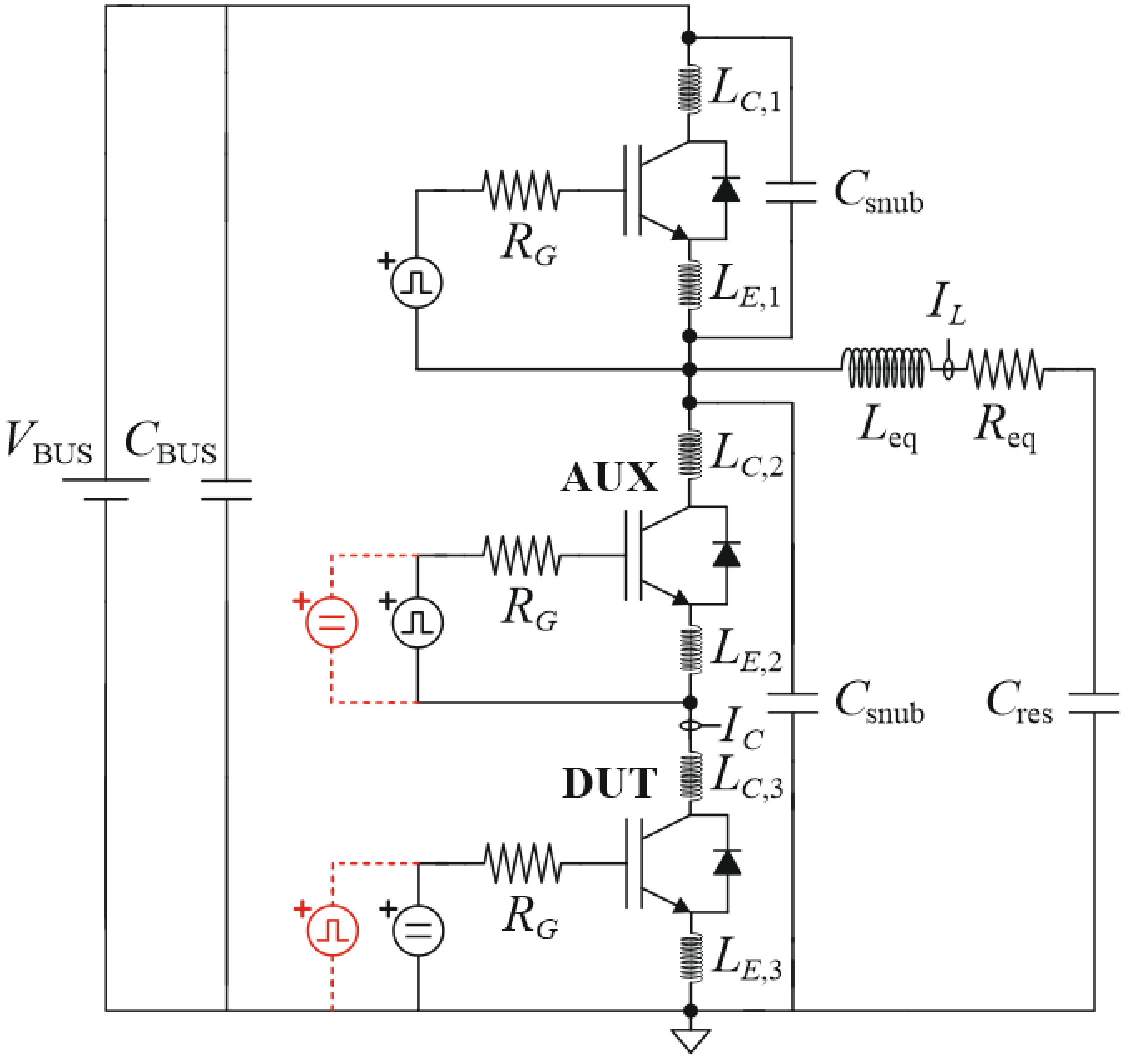


Fig. 5.2-1. Schematic of the designed test platform for the IGBT DUT conduction (black) and switching (red) power losses decoupling.

IGBTs thermal measurements are performed using this resonant circuit with devices under steady state bias, where conduction and switching losses are decoupled from IR measurements. Considering the two IGBTs connected in series on the lower branch:

- Conduction losses are evaluated by electrical or IR measurements in the DUT, kept at V_{GE} = 20 V, while AUX is switched according to a ZVS strategy (induction cooker used), as illustrated by Fig. 5.2-1, in black color.
- Next, the IR inspected device is switched under ZVS driving, while AUX is kept at conduction state. Therefore, both conduction and switching losses are evaluated by IR measurements on the DUT, as shown by Fig. 5.2-1, in red color.

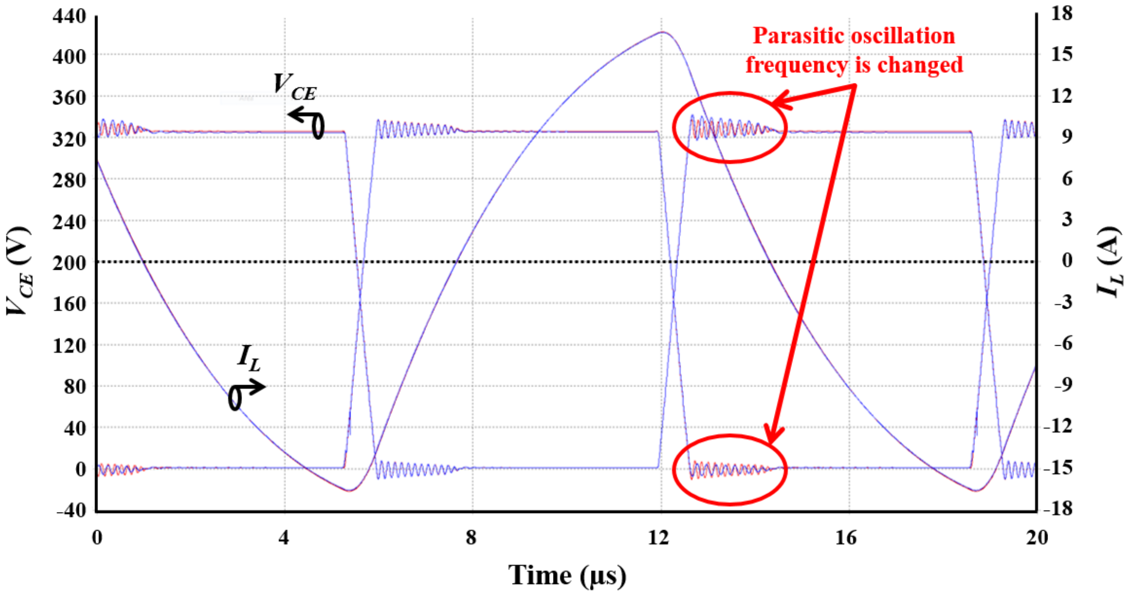


Fig. 5.2-2. SPICE simulation comparing a standard half-bridge (blue solid lines) with the proposed modified half-bridge topology (red solid lines).

From the comparison of both results, information about the contribution to thermal field of each conduction and switching losses can be inferred and decoupled. In addition, this setup provides enough flexibility to analyse the DUT at very different conditions: i.e. operation out of ZVS conditions and with/without a snubber capacitor.

5.2.2.1 Simulation of the Power Stage

To ensure the applicability of a design where two power devices are present at the lower branch with the final application, with a single device only, a SPICE simulation is presented comparing both circuits in Fig. 5.2-2, where the load current (I_L) and V_{CE} at the DUT are depicted for both a standard half-bridge topology, in blue solid lines, and the proposed modified half-bridge topology of Fig. 5.2-1 with its parasitics ($L_{C,1}$, $L_{E,1}$, …), in red solid lines.

No relevant changes are identified at I_L, while V_{CE} oscillating frequency slightly changes during turn-on/off as a consequence of the additional parasitic inductance introduced by the DUT ($L_{C,3}$, $L_{E,3}$).

In addition, the DUT power waveforms have been measured and the total energy losses have been calculated for both a standard half-bridge topology and the proposed modified half-bridge topology. The results are shown in Fig. 5.2-3, where no relevant changes have been detected. Besides, the modified half-bridge topology can also be

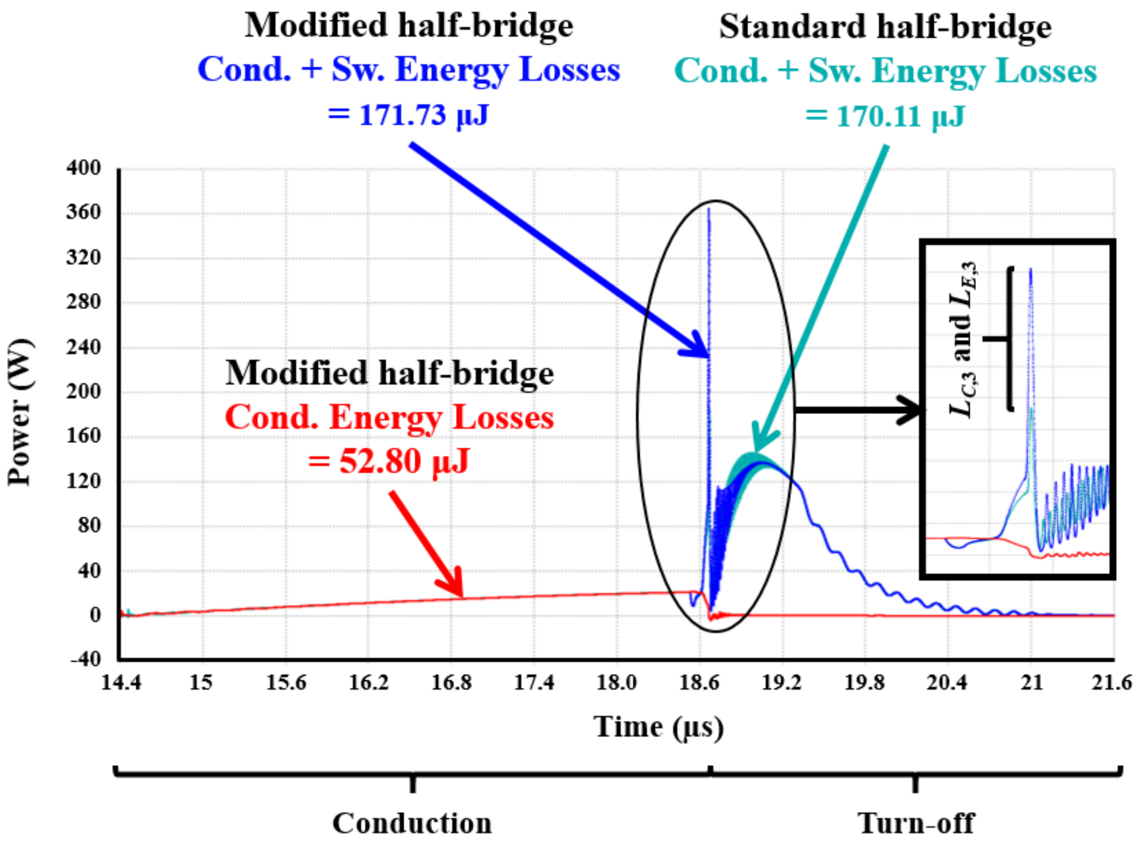


Fig. 5.2-3. SPICE simulation comparing the dissipated power waveforms and the calculated total energy losses for a standard half-bridge (dark cyan solid lines) and the proposed modified half-bridge topology (blue solid lines); together with the calculated conduction energy losses and dissipated power waveforms for the modified half-bridge topology (red solid line).

used for calculating the conduction power losses only, as shown in Fig. 5.2-3. Therefore, it has been demonstrated from simulation the suitability of the designed test platform for studying the power losses distribution.

5.2.3 Test Setup Description II: Peltier Stage and IR Measurements

Fig. 5.2-4 (a)-(b) depict the designed test setup for performing the electrical and IR measurements [91] while Fig. 5.2-4 (c)-(d) illustrate the platform described in Section 5.2.2 mounted on a micropositioning stage to allow its precise focusing and displacement. Fig. 5.2-4 (e) presents a detailed view of the device depicted in Fig. 5.2-4 (d) where both chips have been made visually accessible. Besides, the flexible capacitances, inductors, and resistances, mounted on a heatsink with forced ventilation, are correspondingly illustrated in Fig. 5.2-4 (f)-(h).

IR measurements are performed using a FLIR C5500 IR camera equipped with an internal lock-in module and several microscopic lenses with lateral resolutions up to 5 µm. For each test, the IR images acquisition characteristics are:

- Frame rate f_r = 376 Hz
- Integration time t_{int} = 49 µs
- Number of images: 50.000

IR images are processed at different lock-in frequencies (f_{lock}), limited by the switching frequency at the power inverter (f_{Sw}) (8~10 kHz). Using this technique, thermal variations below the camera Noise Equivalent Temperature Difference (NETD) (below 1 m°C) can be achieved.

Moreover, the visually accessible devices (IGBT and Diode) are positioned over a Peltier thermoregulated stage with its initial temperature set for T_i = 50 °C, which helps to improving the signal-to-noise ratio [92] and is closer to real operating conditions, since induction cooktops are normally positioned over an oven, which imposes environment temperatures even higher, around 75~100 °C. Furthermore, the camera sensitivity is improved by coating both chips with a high emissivity black paint [93].

In addition, a DC voltage source and a waveform generator are used for the heat sources modulation and biasing of the devices, respectively. Concerning the IGBT, its gate is biased with a square wave pulses between V_{GE} = 0 and 20 V.

The main features of the developed test setup are the following:

- V_{BUS} up to 800 V
- I_L up to 50 A
- A flexible load has been designed specifically for this test setup: R_{eq} {3, 6 Ω} and L_{eq} {from 24 to 275 µH}.
- Peltier temperature (T_{P}): from -25 to 125 °C, which is the temperature range that can be imposed at the device.
- Configurable drivers, gate resistances and snubbers.
- Visual access to IGBT and diode, granted from a combination mechanical and chemical processes.

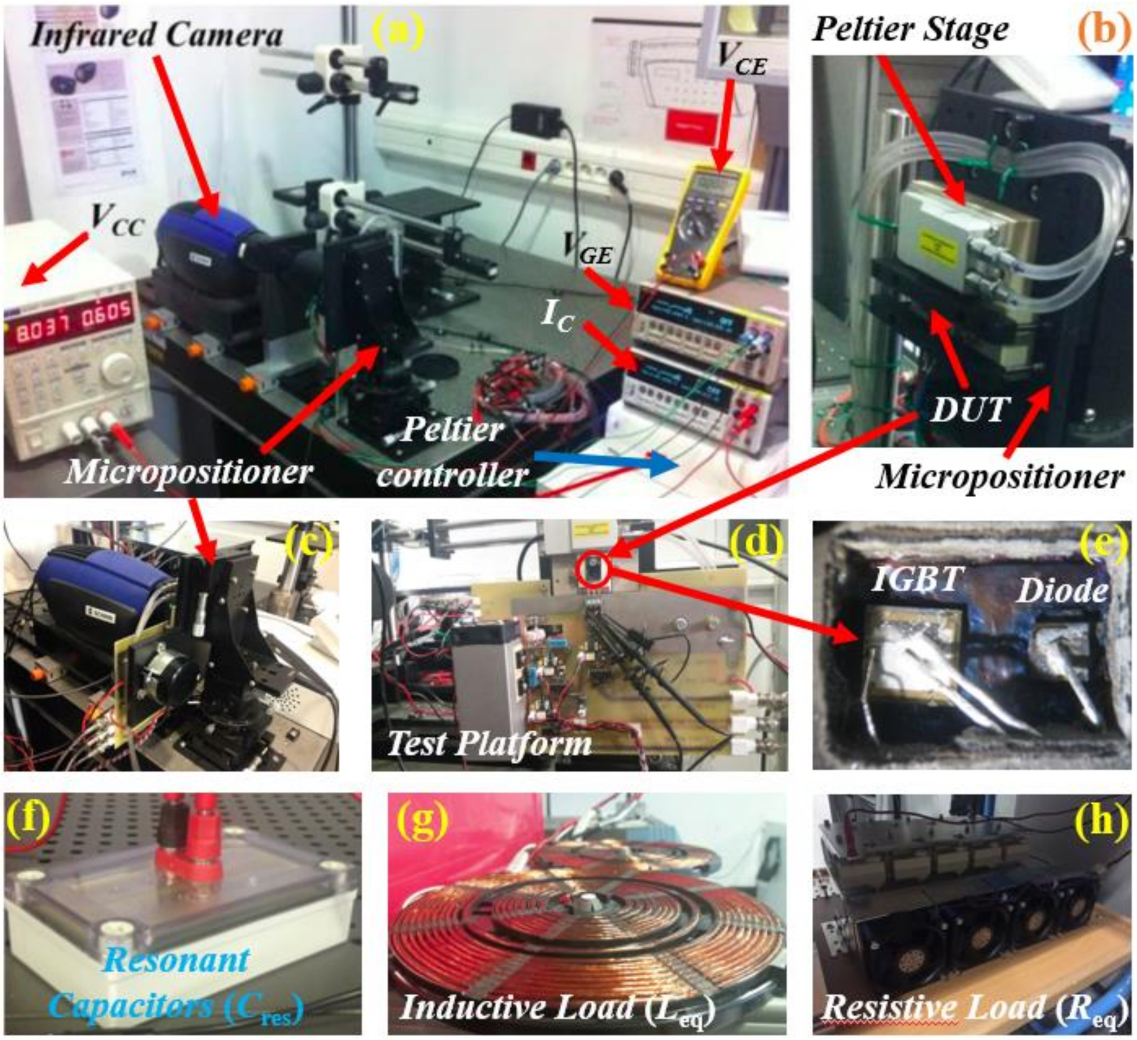


Fig. 5.2-4. (a) Experimental test bench for performing IR Thermographies, (b) Peltier stage, (c) test platform mounted on a micropositioner, (d) test platform and (e) detailed view of the device, and flexible (f) resonant capacitors, (g) inductive load and (h) resistive load. Figure extracted from [10].

In addition, to check the strength of the frequency signal to be measured by the IR camera, the harmonic decomposition of power and temperature waveforms for a few cycles at a 40 kHz sample test at the IGBT and the diode is performed. Fig. 5.2-5 (a) depicts the conduction power waveform harmonic decomposition at the DUT, while Fig. 5.2-5 (b) corresponds to the conduction and switching power waveform harmonic decomposition at the DUT. From those results, it is concluded that there exists a strong signal harmonic at the operating frequency. The same conclusions are obtained from the harmonic decomposition of the diode and the temperature measurements.

5.2.4 CTM and Power Losses Extraction

Prior to start with T_j measurements, the thermal impedance of several power devices encapsulated in a TO-247 package is firstly extracted. Then, a TSEP is selected and calibrated with an oven (Fig. 5.2-6) to be used in thermal impedance measurements: V_{CE} at I_C = 10 mA.

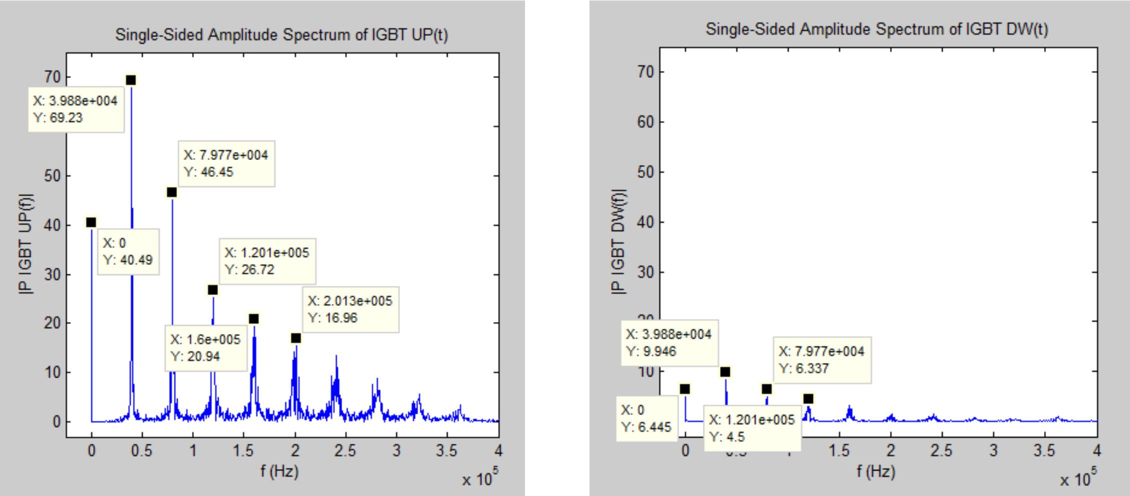


Fig. 5.2-5. Harmonic decomposition of (a) conduction power waveform at the DUT and (b) conduction and switching power waveform at the DUT, at f_{SW} = 40 kHz.

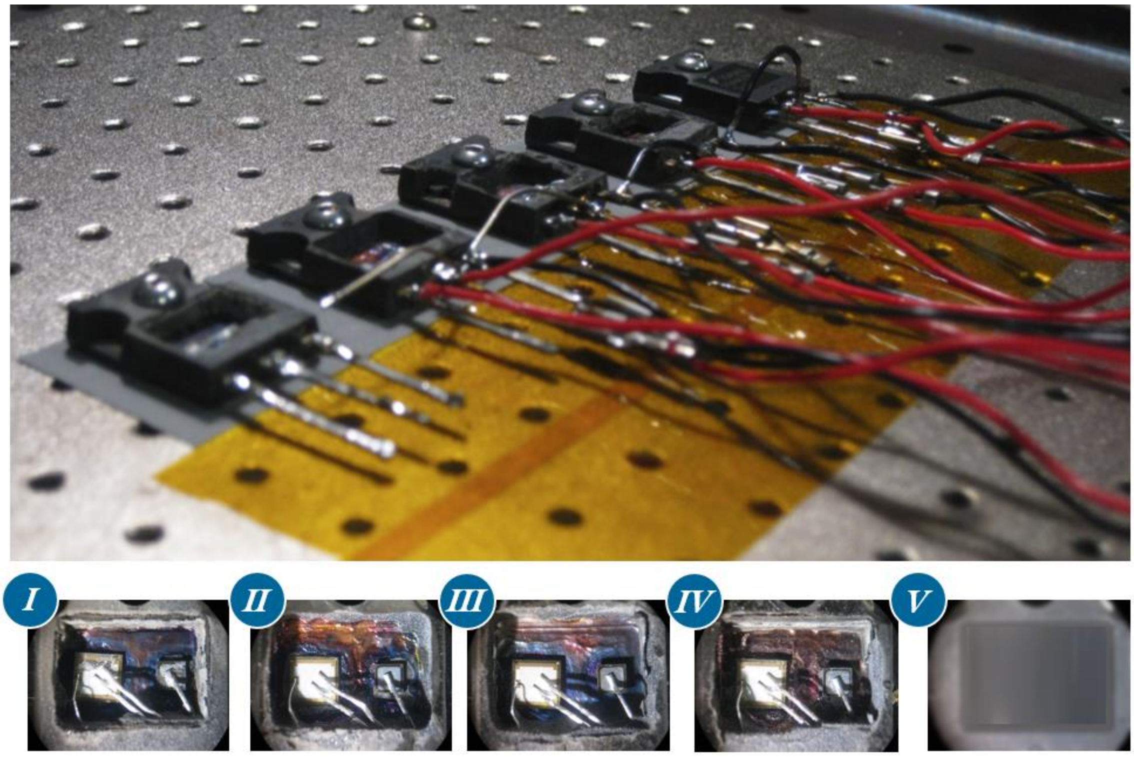


Fig. 5.2-6. Measured devices with the IGBT and diode chips visually accessible (devices I to IV) and a closed device used for reference (device V).

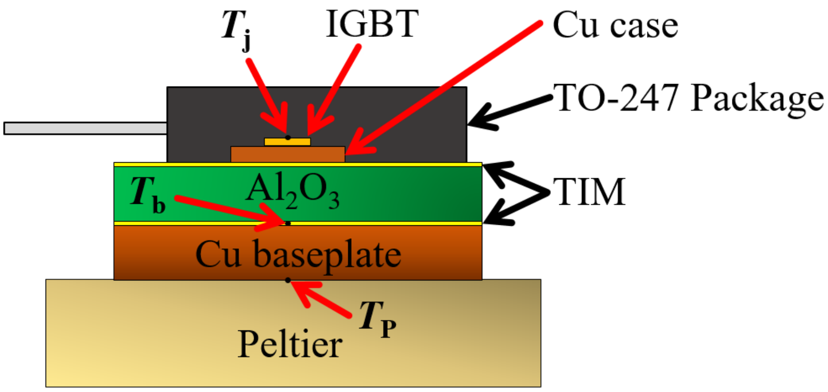


Fig. 5.2-7. Device layers structure including the TO-247 package, the Thermal Interface Materials (TIMs), an Al_2O_3 layer, a Cu baseplate, and a Peltier. Figure extracted from [10].

The total thermal impedance ($Z_{\text{th(j-P)}}$) is obtained for the assembly shown in Fig. 5.2-7, formed by a stack of different materials. They separate the device from the Peltier thermoregulated stage at a given temperature $T_{\text{P}}(t)$ = 50 °C. Thus, $Z_{\text{th(j-P)}}$ is calculated as follows:

$$Z_{\text{th(j}-\text{P)}}(t) = \frac{T_{\text{j}}(t) - T_{\text{P}}(t)}{P} \tag{2}$$

Where P is the dissipated power in the device. P is kept constant along this process. For more details see Publication [10]. With $Z_{\text{th(j-P)}}$, an electro-thermal model of the device is derived from in the form of an RC Cauer network and used for electro-thermal simulation purposes. For more details on the electro-thermal simulation process and the methodology followed, see Publication [10].

By means of the set-up depicted in Fig. 5.2-4, publication [10] presents IR DC measurement results from which P at the DUT is calculated in steady state, according to:

$$P = \frac{T_{\text{j}}(t \rightarrow \infty) - T_{\text{P}}(t \rightarrow \infty)}{R_{\text{th(j}-\text{P)}}} \tag{3}$$

where $R_{\mathrm{th(j-P)}}$is thermal resistance from junction to Peltier, i.e., $Z_{\mathrm{th(j-P)}}(t \rightarrow \infty)$. The obtained results are assessed with electrical measurements and simulation results.

5.3. Conclusions

An experimental approach has been set up to thermally monitor power losses and current distribution at the die-level under switching conditions representative of induction cooking applications. To this end, a half bridge converter has been designed with the following considerations: the studied devices have been prepared visually accessible with an IR camera to acquire its thermal field in DC and under working switching frequency. With DC measurements, T_{j} is determined, which is the main contribution to the thermal field seen by the device. On the other hand, the current distribution within the device has been determined by lock-in acquisition and postprocessing approaches. To tackle such challenges, the packaging moulding compound has been removed, leaving the both dies (IGBT and Diode) accessible to perform IR thermographies. It should be noticed that the semiconductor devices characteristics has not been modified by this process.

With the designed workbench, several aspects related with the reliability of IGBTs have been studied and modelled. The first one has been the temperature working conditions in all components, providing an electrothermal model for its analysis. In addition, the IGBTs and diodes have been studied when working within and out of ZVS condition.

As a main conclusion, it has been observed that the natural frequency of the converter should be lower than the IGBT switching one to be working in more rugged scenarios. The main results of this study are reported in publication [10], where thermal maps are discussed to determine possible failure weak spots in the references considered.

Chapter 6: GENERAL CONCLUSIONS AND FUTURE WORK

6.1. General Conclusions

As stated in Chapters 1 and 2, this thesis focuses on addressing a more flexible, sustainable, efficient and reliable induction cooking approach from a power semiconductor device point of view. In this framework and with this perspective, this PhD thesis has identified the following activities to cover such demands: SSR based on power semiconductor devices, ruggedness study on power semiconductor devices in induction cooking appliances, and power losses calculation at die-level in resonant power converters.

In Chapter 3, SSR solutions are investigated as an alternative to the EMRs. All devices commercially available presenting low conduction losses have been considered. From the performances presented in DC mode, several conclusions have been identified. Those BDS based on bipolar devices (TRIAC, IGBT+diode, RC-IGBT, RB-IGBT and SiC BJTs) have highlighted an off-set voltage. Such an off-set may result in slight distortions of the AC currents/voltages at the BDS in the zero-crossing region. In spite of this, it does not represent a remarkable problem in practical applications but an increase of the conduction power losses. Conversely, GaN HEMTs, SiC MOSFETs and SiC JFETs based BDS experienced a symmetrical conduction in the first and third quadrants with the lowest conduction voltage drops. With regards to their dynamic analysis, several technologies have been identified to suffer from anomalous behaviours (TRIAC, SJ MOSFET and RC-IGBT). Conversely, SiC MOSFETs, SiC JFETs and, to a lesser extent, SiC BJT+diode based BDS highlight excellent dynamic characteristics, with higher driving requirements for JFET and BJT, and a less expected costs drop in the short/medium-term than GaN HEMTs. In addition, GaN HEMTs based BDS presented outstanding static, dynamic and integration characteristics, being the best candidates to replace the EMRs. Moreover, their thermal management issues will become less relevant as the technology maturity will increase. As a main conclusion, the BDS based on GaN HEMTs has been identified as the best solution in terms of its outstanding static and dynamic characteristics.

In Chapter 4, the SC capability is studied for power semiconductor devices employed or with potential to be used in induction cooking. Adapted SC tests have been set in this scenario, analyzing IGBTs and GaN HEMTs. In the latter case, SC capability tests have been performed for the first time. As main conclusions, the following results have been obtained. In IGBTs, the SC withstanding time is drastically reduced when V_{GE} is increased up to 20 V, and t_{on} = 10 µs cannot be guaranteed. This is due to the fact that the power dissipation in the IGBT is higher due to the higher current concentration passing through the IGBT channel. In fact, the SC rated RC-IGBT is the only one capable of withstanding a SC event for t_{on} = 10 µs at V_{GE} = 15 V, but not at V_{GE} = 20 V. As a main result, the transconductance of the IGBT (g_{fs}), which correlates I_C with V_{GE}, has been identified to predict the IGBTs SC endurance, where the SC duration keeps an inverse relationship with g_{fs}.

As for GaN HEMTs, none of the studied devices withstand a SC I event at V_{BUS} = 400 V during t_{on} = 10 µs. EHEMTs have demonstrated to endure a SC I test at V_{BUS} = 300 V (MISHEMTs) and V_{BUS} = 350 V (p-GaN HEMTs), while GaN cascodes did not pass the tests for $V_{\mathrm{BUS}} > 150$ V. Conversely, p-GaN HEMTs have been capable of withstanding a V_{BUS} = 350 V SC II event for t_{on} = 17 µs, while GaN MISHEMTs only passed the SC II test at V_{BUS} = 250 V. As a result, it has been determined that the higher I_D decrease during the SC event of EHEMTs is caused by the thermal behaviour of their channel, while cascodes behaviour results from their different structure, driving and thermal characteristics. In this study, further information has been derived for GaN HEMTs. The abrupt I_D rise with a null or low $I_{G(\mathrm{on})}$ leakage for cascodes and EHEMTs outlines a purely thermal destruction. As a general conclusion, all devices fail during the SC event. In comparison to other available technologies, SJ and SiC MOSFETs present the best SC capability, mainly due to the low maturity of GaN devices and the lack of knowledge on their behaviour under SC conditions. In this scenario, two main findings useful for SC protection strategies are provided. On the one hand, protection circuits require at least a 300 ns response to safely switch the analysed EHEMTs and GaN cascodes off and, on the other hand, $I_{G(\mathrm{on})}$ monitoring under operation by means of a smart gate driver could be a good state indicator for SC prevention in EHEMTs.

Finally, Chapter 5 presents a novel experimental approach to thermally monitor power losses and current distribution at the die-level under switching conditions representative of induction cooking applications. To this end, a half-bridge converter has been designed with the following considerations: the studied devices have been prepared visually accessible with an IR camera to acquire its thermal field in DC and under working switching frequency. With DC measurements, T_j is determined, which is the main contribution to the device thermal field. On the other hand, the current distribution within the device has been determined by lock-in postprocessing approaches. To this end, both dies (IGBT and Diode) have been prepared to be visually accessible (moulding compound removed) without modifying their characteristics. To access to the potential of this technique, several aspects related with the reliability of IGBTs have been also studied and modelled. The first one has been the temperature working conditions in all components, providing an electrothermal model for its analysis. In addition, the IGBTs and diodes have been studied when working within and out of ZVS condition. As a main conclusion, it has been observed that the natural frequency of the converter should be lower than the IGBT switching one to be working in more rugged scenarios.

6.2. Future Work

This PhD thesis can give rise to face several open challenges. On the one hand, it can assist to provide a major understanding on the physics underlying the power semiconductor devices used under constrained operation conditions, which are responsible for the device failure. On the other hand, pre-evaluation tests of new references of power semiconductor devices will be also revised to make them more representative of the final application. Such actions are crucial to addressing reliability issues in induction cookers and improving pre-evaluation tests when they are undetectable during pre-assessment manufacturing stages. In this scenario, die inspection under operation, as well as local ruggedness tests, would be very valuable:

- to perform suitability studies in new references of power devices for BSH induction cookers,
- to identify problems at the device layout level, or
- to modify some of BSH pre-evaluation approaches.

As a matter of fact, a higher knowledge at the die-level in such fields is a clear need of IH manufacturers. Having access to this information will deliver a much better description of the device internal physics (only available to device manufacturers) and bring the opportunity for an invaluable academic study, thanks to IR thermography measurements at the die-level supported by the developed set-up.

In spite of the fact that such data are very useful for preventing semiconductor power devices from eventual failures, electro-thermal physical simulations at the device level are mandatory to go beyond the current knowledge on the device structures. Thus, it is imperative to combine such a set-up with physical modelling, which would give rise to an unprecedented approach. In general, such simulations require having access to the internal structure of the analysed semiconductor power device. The added value of the proposed approach will be the extraction of fundamental information at the die-level, never accessed until now; making the selection of new references/technologies easier, or solving reliability issues with power devices, for instance. Aside from conventional IGBTs, alternative technologies with great potential in induction cookers will be explored aiming at extending the analysis performed to other useful semiconductor devices. Moreover, the proposed study will be a cornerstone to answer and solve other open reliability quests in running projects, i.e.:

- **Noise reduction outside ZVS condition, while power devices work at higher frequencies.** Switching power devices outside of ZVS condition at frequencies of 200 kHz is a promising solution to reduce noise. In such a situation, the snubbers are rapidly loaded following a non-linear behaviour. In this scenario, modelling such losses and identifying how them could affect the final product and power devices is very interesting for cooker designers.
- **Local access to losses in power converters and snubbers.** Accessing to all the information about the power dissipated by each component of the converter (mainly, power devices and snubbers) is an interesting matter to deepen into the

real limits of power devices, especially from the calculation losses point of view. Actions in this way are crucial to accurately modelling the system, observing how this compromise is translated at the chip level, and having access to local temperature calculations to better understanding the real limits at the die-level.

- **Influence of using cheaper IGBTs on the cookers reliability.** Due to the aggressive decrease cost demanded by the induction cooker market, the use of cheaper IGBTs is fundamental to achieving the final price reduction of the product. Thus, defining a procedure to perform this evaluation among multiple references in an accurate way is of paramount importance. This is reduced to determine the safety margin required and how cooker designer could evaluate this design parameter.
- **Reliability change due to current scaling up in induction cookers, while reducing the number of components.** Studies in the scaling up of the same technology to work with higher currents are a final user aim to reduce cost while keeping the reliability levels to meet all requirements imposed by induction cooker’s market.

In this scenario, predictive physics-based simulations will provide die-level information basic to understanding the device issues arisen from their operation (e.g., working outside ZVS condition, unexpected capacitor discharge, bad device driver control).

Aside from the topics directly related with power device operation and analysis, this PhD thesis has demonstrated that SSRs based on new semiconductors are of main technical interest for IH appliances, and GaN HEMT based solutions have been identified as a very promising option. Some aspects related with GaN based SSR implementation require still additional research and development effort, such as low volume thermal management solutions and design optimization in view of system cost reduction. Nevertheless, power devices technology is moving fast and advances (such as commercial monolithic GaN HEMT BDSs, lower cost SiC MOSFETs, etc.) could introduce new breakthroughs in the SSR scenario.

CONCLUSIONES GENERALES

Tal y como se ha indicado en los Capítulos 1 y 2, esta tesis tiene como objetivo alcanzar una mejora en la flexibilidad, sostenibilidad, eficiencia y fiabilidad para aplicaciones de cocina de inducción poniendo el foco en los dispositivos semiconductores de potencia. En el marco de esta tesis se han identificado y desarrollado una serie de actividades que sirven como vehículo para cumplir con los mencionados objetivos: en primer lugar, el desarrollo de interruptores bidireccionales basados en dispositivos de potencia de estado sólido. A continuación, el estudio de robustez y fiabilidad en dispositivos semiconductores de potencia presentes en cocinas de inducción y, por último, el cálculo preciso de las pérdidas de potencia a nivel de chip en convertidores resonantes.

En el Capítulo 3, se investigan las diferentes soluciones de interruptor bidireccional basadas en dispositivos de estado sólido como alternativas a los relés electromecánicos. En esta tarea se han tenido en cuenta todos aquellos dispositivos que se encontraban comercialmente disponibles y que presentaban unas pérdidas de conducción razonablemente bajas. En base a los resultados obtenidos durante una primera etapa de medidas estáticas, se ha concluido que para el caso de aquellos interruptores bidireccionales basados en dispositivos bipolares, existirá una tensión de off-set (por ejemplo, aquellos basados en TRIAC, IGBT + diodo, RC-IGBT, RB-IGBT y SiC BJT) que podrá dar lugar a ligeras distorsiones en las corrientes y tensiones durante el cruce por cero. A pesar de ello, esto no representará un problema en aplicaciones prácticas, sino que tan solo resultará en un aumento de las pérdidas de potencia en conducción. Por el contrario, para el caso de las implementaciones basadas en GaN HEMTs, SiC MOSFETs y SiC JFETs, estos presentarán una conducción simétrica en el primer y tercer cuadrantes con las menores caídas de tensión en conducción. Con respecto a los análisis dinámicos, se han identificado varias tecnologías que sufren comportamientos anómalos (TRIAC, SJ MOSFET y RC-IGBT). Por el contrario, los interruptores bidireccionales basados en SiC MOSFETs, SiC JFETs y, en menor medida, SiC BJTs+diodo destacan por sus excelentes características dinámicas. Sin embargo, precisan de mayores requisitos de control/complejidad y se espera que a corto/medio plazo, presenten una menor caída de los precios de la que se espera que se produzca para el caso de los GaN HEMT.

En cuanto al interruptor bidireccional basado en GaN HEMTs, este presenta excelentes características estáticas, dinámicas y de integración, siendo identificados como los candidatos más prometedores para reemplazar a los EMR. Además, los problemas derivados de los mecanismos de disipación de calor serán cada vez menos relevantes a medida que aumente la madurez de esta tecnología. Como conclusión principal, el interruptor bidireccional basado en GaN HEMTs ha sido identificado como la mejor solución en términos de sus características estáticas y dinámicas.

En el Capítulo 4, se estudia la capacidad en cortocircuito para los dispositivos semiconductores de potencia empleados o con potencial para ser utilizados en calentamiento por inducción. En este escenario se han analizado tanto IGBTs como GaN HEMTs. En el caso de esos últimos, se trata de la primera vez que este tipo de tests había sido llevado a cabo para el estudio de este tipo de componentes. Como conclusiones principales se han obtenido los siguientes resultados.

En cuanto a IGBTs, el tiempo de cortocircuito se reduce drásticamente cuando V_{GE} se incrementa hasta los 20 V, no pudiendo garantizarse un tiempo mínimo de cortocircuito de 10 µs. Esto se debe al hecho de que la disipación de potencia en el IGBT es mayor debido a la mayor concentración de corriente que pasa a través del canal IGBT. De hecho, el RC-IGBT con clasificación de cortocircuito es la única referencia capaz de soportar un evento de cortocircuito superior a t_{on} = 10 µs, a V_{GE} = 15 V, pero no a V_{GE} = 20 V. Como aspecto relevante, la transconductancia del IGBT (g_{fs}), que correlaciona I_C con V_{GE}, ha sido identificada como parámetro para tratar de predecir la robustez un IGBTs durante un corto-circuito, de tal forma que t_{SC} mantiene una relación inversa con gfs.

En cuanto a los GaN HEMT, ninguno de los dispositivos estudiados es capaz de soportar un evento de cortocircuito de tipo I a V_{BUS} = 400 V durante t_{on} = 10 µs. Los EHEMT han demostrado soportar una prueba de cortocircuito tipo I en V_{BUS} = 300 V (MISHEMT) y V_{BUS} = 350 V (p-GaN HEMT), mientras que los cascodos de GaN no pasaron las pruebas para V_{BUS} > 150 V. Por el contrario, los p-GaN HEMTs han sido capaces de soportar un evento V_{BUS} = 350 V SC II para ton = 17 µs, mientras que GaN MISHEMTs solo pasó la prueba de SC II a V_{BUS} = 250 V. Como resultado, se ha determinado que la mayor disminución de I_D durante el evento SC de EHEMTs es causado por el comportamiento térmico de su canal, mientras que el comportamiento de cascodo es el resultado de su diferente estructura, conducción y características térmicas. En este estudio, se ha obtenido más información para los dispositivos GaN HEMTs. El aumento abrupto de I_D con una fuga de corriente de puerta $I_{G(\mathrm{on})}$ nula o baja para cascodes y EHEMT esboza una destrucción puramente térmica. Como conclusión general, todos los dispositivos fallan durante el evento de cortocircuito. En comparación con otras tecnologías disponibles, los MOSFET SJ y SiC presentan la mayor capacidad cortocircuito, principalmente debido a la baja madurez de los dispositivos GaN y la falta de conocimiento sobre su comportamiento en condiciones cortocircuito. En este escenario, se proporcionan dos hallazgos principales útiles para las estrategias de protección en cortocircuito. Por un lado, los circuitos de protección requieren al menos una respuesta de 300 ns para desconectar con seguridad los EHEMT analizados y los cascodes de GaN y, por otro lado, el monitoreo $I_{G(\mathrm{on})}$ bajo operación por medio de un controlador inteligente puede ser un buen estado indicador de prevención de cortocircuito en en HEMTs.

Finalmente, el Capítulo 5 presenta un novedoso enfoque experimental para monitorear térmicamente las pérdidas de potencia y la distribución de corriente a nivel de chip en condiciones de conmutación representativas de las aplicaciones de cocina de inducción. Con este fin, un convertidor de medio puente ha sido diseñado con las siguientes consideraciones: los dispositivos estudiados han sido preparados para ser visualmente accesibles por una cámara IR para adquirir su campo térmico en continua y bajo frecuencia de conmutación de trabajo. Con las mediciones de continua, se determina T_{j}, que es la principal contribución al campo térmico del dispositivo. Por otro lado, la distribución actual dentro del dispositivo ha sido determinada por medio de técnicas e postprocesamiento de bloqueo. Con este fin, ambos chips (IGBT y Diodo) se han preparado para ser accesibles visualmente (se ha eliminado la cápsula que los cubre) de tal forma que sus características eléctricas permaneciesen intactas. Para poder aprovechar el potencial de esta técnica, se han estudiado y modelado varios aspectos relacionados con la fiabilidad en los IGBT. Por ejemplo, la temperatura en las condiciones de trabajo para el IGBT y el diodo bajo test, proporcionando un modelo electro térmico para su análisis. Además, los IGBT y los diodos se han estudiado al trabajar dentro y fuera de la condición de ZVS. Como conclusión principal, se ha observado que la frecuencia natural del convertidor debe ser menor que la frecuencia de conmutación del IGBT para trabajar en escenarios más robustos.

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PUBLICATIONS

In this section, the compendium of publications is included. First, the publications are listed in order of appearance.

1. Development of compact SSR based on advanced power semiconductor devices:
    a. Journal Publication

[1] M. Fernández, X. Perpiñà, J. Rebollo, M. Vellvehi, D. Sánchez, T. Cabeza, S. Llorente, and X. Jordà, "Solid State Relay Solutions for Induction Cooking Applications based on Advanced Power Semiconductor Devices," *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2018.2838093. (In press).
URL: https://ieeexplore.ieee.org/document/8365104/

b. Conference Publications

[2] M. Fernández, X. Perpiñà, M. Vellvehi, X. Jordà, T. Cabeza, and S. Llorente, "Analysis of solid state relay solutions based on different semiconductor technologies," in *Proc. European Conference on Power Electronics and Applications* (EPE), Warsaw, Sept. 2017, pp. P.1-P.9, doi: 10.23919/EPE17ECCEEurope.2017.8099012.
URL: https://ieeexplore.ieee.org/document/8099012/

[3] M. Fernández, X. Perpiñà, M. Vellvehi, D. Sánchez, X. Jordà, J. Millán, T. Cabeza and, S. Llorente, "Analysis of bidirectional switch solutions based on different power devices," in *Proc. Spanish Conference on Electron Devices* (CDE), Barcelona, Feb. 2017, pp. 1-4, doi: 10.1109/CDE.2017.7905220.
URL: https://ieeexplore.ieee.org/document/7905220/

c. In Writing Process

[4] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, S. Llorente, and X. Jordà, "Feedback Oscillations in Super-Junction MOSFET-based Solid State Relays," *IEEE Transactions on Power Electronics* (In writing process).

d. Patent

[5] T. Cabeza, M. Fernández, X. Jordà, S. Llorente, I. Millán, X. Perpiñà, D. Sánchez, and M. Vellvehi, "Dispositivo de aparato doméstico", Application number: P201631613 (19.12.2016), Publication number: ES2673129 A1 (19.06.2018).

[6] T. Cabeza, M. Fernández, X. Jordà, S. Llorente, I. Millán, X. Perpiñà, D. Sánchez, and M. Vellvehi, "Haushaltsgerätevorrichtung", Application number: DE201710222394 (11-12-2017), Priority number: ES20160031613 (19.12.2016).

2. Ruggedness and reliability studies of several power semiconductor devices:

c. Journal Publications

[7] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, X. Jordà, and M. Tack, "P-GaN HEMTs Drain and Gate Current Analysis Under Short-Circuit," *IEEE Electron Device Letters*, vol. 38, no. 4, pp. 505-508, April 2017, doi: 10.1109/LED.2017.2665163.
URL: https://ieeexplore.ieee.org/document/7845577/

[8] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, M. Tack, and X. Jordà, "Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9012-9022, Nov. 2017, doi: 10.1109/TIE.2017.2719599.
URL: https://ieeexplore.ieee.org/document/7956198/

d. Conference Publication

[9] M. Fernández, X. Perpiñà, M. Vellvehi, X. Jordà, J. Roig, F. Bauwens and M. Tack, "Short-circuit capability in p-GaN HEMTs and GaN MISHEMTs," in *Proc. International Symposium on Power Semiconductor Devices and ICs* (ISPSD), Sapporo, May 2017, pp. 455-458. doi: 10.23919/ISPSD.2017.7988916.
URL: https://ieeexplore.ieee.org/document/7988916/

3. Junction temperature extraction and device weak spots identification under real conditions:

b. In Writing Process

[10] M. Fernández, M. Vellvehi, X. Jordà, and Xavier Perpiñà, “Power Losses and Current Distribution Extraction in IGBTs under Resonant Load and ZVS Condition,” *IEEE Transactions on Power Electronics*. (In writing process).

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Solid State Relay Solutions for Induction Cooking Applications based on Advanced Power Semiconductor Devices

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Tomás Cabeza, Sergio Llorente, and Xavier Jordà

***Abstract*—This work focuses on providing an improved and efficient alternative to Electro Mechanical Relays (EMR) in view of the growing demand characteristics for an effective power multiplexing in induction heating applications. A major analytical approach to the design and implementation of Bi-Directional Switches (BDS) based on different power semiconductor technologies is presented, including thorough static and dynamic characterizations. Emerging Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) and Silicon Carbide (SiC) based devices are identified as potential candidates for the mentioned applications.**

***Index Terms*—Bidirectional power flow, Bidirectional Switch, Electro Mechanical Relay, GaN, GaN HEMTs, Induction heating, Multiplexing, Power semiconductor devices, SiC.**

I. INTRODUCTION

THIS paper experimentally analyses Solid State Relay (SSR) solutions based on advanced power semiconductor devices suitable for medium power industrial applications. Specifically, SiC and GaN based semiconductor devices are compared with the most performant Si counterparts. Concretely, this work is framed in the context of induction heating for home appliances, which involves a two-stage power conversion that can be synthesized as follows. First, mains AC voltage is rectified by a diode bridge and filtered. Then, the resulting DC bus voltage (V_{BUS}) is connected to switching inverters to supply the high-frequency current to the induction coils [1].

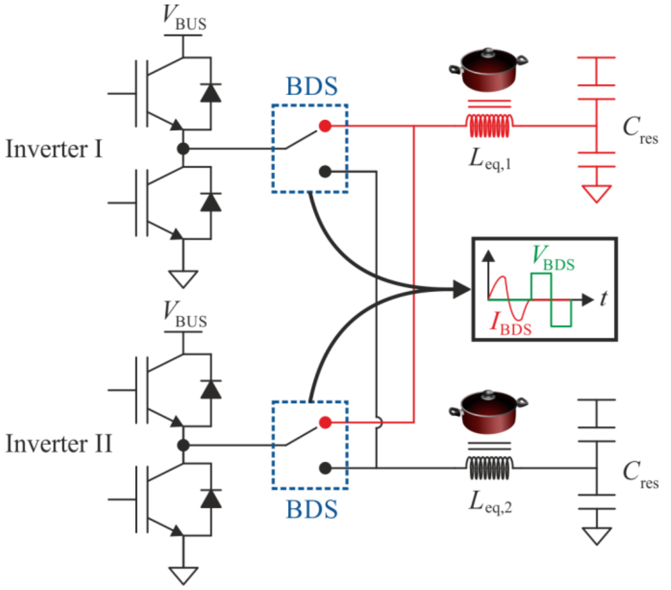

Fig. 1. Simplified schematic of an induction heating system.

The main drawback of conventional multiple loads induction cooking systems is that they involve several independent inverters to provide the nominal power requirements for each inductor. This issue can be solved through the loads-multiplexing technique, based on using several switches to connect and disconnect the loads to the inverters and allow their parallel operation, thereby reducing the whole cost of the system. This method can be implemented using SPDT (Single-Pole, Double-Throw) Bi-Directional Switches (BDS) which are time-multiplexed to enable (bidirectional current conduction flow, I_{BDS}) or disable (bidirectional voltage blocking, V_{BDS}) the different loads ($L_{\mathrm{eq,1}}$, $L_{\mathrm{eq,2}}$, …), which are in resonance with capacitor banks (C_{res}) [2] as highlighted in Fig. 1.

Electro Mechanical Relays (EMRs) constitute the lowest-cost solution for commutating power sub-circuit blocks. They have been in use up to now for implementing BDS in industrial electronics applications [2], with a low on-state resistance (5-10 mΩ). For the studied application framework, conventional PCB mounted relays are usually unable to manage voltages/currents higher than 400 VAC/20~30 A. In addition, their application to power multiplexing evidences a set of limitations which intend to be downsized or removed by semiconductor devices based designs [3]:

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1) Existence of moving parts, which are susceptible to wear (short service life) and be affected by vibration or physical shock.
2) Presence of electric arcs during commutation with consequent risk of terminals welding.
3) Acoustical noise and large electromagnetic interference.
4) High inrush current and input power consumption (350-400 mW).
5) Slow response (5-10 ms), making them incompatible with high frequency applications and limiting the multiplexing rate in the presented induction cooking example.
6) Large size and weight.

This paper performs for the first time an exhaustive comparison among the electric and electronic options available to implement the BDS function for EMR replacement, analyzing their pros and cons and including emerging technologies such as WBG (Wide Band-Gap) power devices.

More specifically, this work focuses on analyzing different static (semiconductor-based) implementations of the Single-Pole, Single-Throw (SPST) BDS switching function as the main step for SPDT implementation, so that all results stemming from this study can be extended to the mentioned SPDT relay. The resulting power switch shall be operated under two different conditions: bidirectional voltage blocking state, with its two terminals disconnected one another (switch opened, high impedance state), and bidirectional current conduction state, with both connected each other (switch closed, low impedance state).

The mentioned application framework involves voltage and current rated levels of 600-1200 V and 20-70 A for the power devices included in the study, with the lowest possible conduction losses as the most demanded characteristic. However, despite the fast switching capability is not a core requirement, the BDS must undertake high-frequency AC currents (30-80 kHz) in the conduction mode, which involve somewhat high dI/dt values (around 7000 A/ms); and high dV/dt in blocking mode (around 500 V/µs). In this sense, a Figure Of Merit (FOM) is defined to allow the quantification of the BDSs electro-thermal behavior taking into account their operation with AC currents. Regarding this topic, it is worth mentioning common applications for BDSs are matrix converters, in which a fast switching capability becomes a must requirement in opposition to our case [4].

This paper starts with a review of the available devices for developing the BDS function. Then, their implementation into test vehicles is described, together with the designed test setup and the characterization methods. Afterwards, the BDS solutions are fully characterized by means of static and dynamic analysis. In this sense, a new dynamic test platform was designed to study the BDSs behavior under different dV/dt and dI/dt conditions. Based on those results, a functional prototype of one of the most performing solutions is tested in the final application. In addition, we described the abnormal behavior of promising semiconductor technologies for implementing the BDS function that have not been reported before. Finally, the whole results are discussed in the last section, together with the conclusions of this work.

II. BDS TECHNOLOGIES

Besides the aforementioned EMRs, a broad range of devices can be in principle considered for implementing a BDS in the framework of the induction heating applications:

1) Dry reed relays, which can operate faster than EMRs with less input power consumption and longer expected service life. Unfortunately, they have a higher contact resistance and are limited to low currents (2-3 A) due to their smaller contacts [5].
2) Mercury Displacement Relays (MDR) [6] are a type of reed relays. The lack of mobile contacts and the absence of heatsinks are the main advantages over EMRs and SSRs respectively [7]. However, they cannot be operated at high frequencies, and owing to the mercury toxicity they became obsolete.
3) Micro-Electro-Mechanical-Switches (MEMS), whose main switch element consists of a freestanding mechanical cantilever. Despite this technology is currently being used for low power, a solution based on MEMS arrays connected in parallel has already been demonstrated to withstand up to 300 V, with a low on-state resistance (100 mΩ) and an arc-free fast switching speed (~µs) [8]. Regrettably, it presents a low current-carrying capability (~5 A) and a very high-voltage driving (~80 V). However, as this technology is currently under development it is expected a performance improvement.
4) Standard SSR solutions, consists on using power semiconductor devices for implementing the aforementioned BDS function. The industrially available SSRs integrate, in a single part, both control and power stages. Their output stages are commonly TRIAC or Thyristor based for AC loads and MOSFET based for AC/DC loads [9]. However, the first ones are widely spread only for low-frequency AC applications (50-60 Hz mains, 0-1.5 kV) and therefore are not suitable for the high-frequency currents involved in this study. SSR solutions based on new semiconductor device technologies will be analyzed in the next sections.
5) Specific hybrid solutions, e.g. a TRIAC based SSR in parallel with an EMR, where a control circuit switches on first the SSR, to handle the load inrush current, and then the EMR (at no load), to handle the load current [7].

As a result, from the characteristics of each technology it can be concluded that the only practical solution for the induction cooking application is based on the use of advanced SSRs.

III. BDS SSR SOLUTIONS

This section describes BDS implementations with the most performing power devices which are commercially available (or under research) in the voltage and current ranges of interest. In the following paragraphs the different solutions are categorized by the number of power devices required in a BDS and their individual characteristics.

A. Single device:

A standard TRIAC stands out for implementing a BDS just by itself, with significantly low on-state losses ~1.15 V @ 30 A for a 800 V device. Unfortunately, both TRIACs and SCRs are limited on their turn-off behavior for the specified rate of decrease of commutating on-state current $(dI/dt)_C$ [10], [11]. Snubberless TRIACs made significant improvements to make this technology compatible with all applications in the 50-60 Hz range [11] and are widely used in nowadays AC low-frequency industrial SSR. However, the TRIAC dynamic limitations are far away from the requirements of the studied application.

B. Multiple power devices:

Multiple devices can be combined to attain the BDS function [12] as depicted in Table I:

1) Anti-parallel arrangement of devices

Reverse-Blocking IGBTs (RB-IGBTs) [13] are the only commercially available devices in this category and involve the monolithical integration of a modified IGBT structure with reverse blocking capability. The BDS function is obtained by the anti-parallel arrangement of two devices, with only a single device conducting current regardless the sense of circulation [14], [15]. All few commercially available RB-IGBTs structures belong to Non-Punch-Through (NPT) technology [16] where a junction isolation region is added to provide the reverse blocking capability like on a P-N diode [13]. Consequently, their dynamic performance is limited [12]. 600 V RB-IGBTs provide saturation voltages ($V_{CE(\mathrm{sat})}$) around ~1.5 V @ 30 A.

2) Anti-series arrangement of devices

These configurations are either possible by a common-emitter/source or a common-collector/drain arrangement of two devices.

Numerous solutions can be implemented from the commercially available IGBT technologies. The most performing generation of 650 V IGBTs for the considered application is based on the trench technology. The bidirectional current capability is either possible by a co-packed integration with an anti-parallel diode (IGBT+Diode) [17], offering a low $V_{CE(\mathrm{sat})} < 1$ V @ 30 A, or by a Reverse-Conducting IGBT (RC-IGBT) with a monolithically embedded diode [18], with slightly higher $V_{CE(\mathrm{sat})}$ (~1.25 V @ 30 A). Solutions based on this approach present higher on-state voltage drops from the series conduction of two devices in both directions: IGBT and diode.

Silicon (Si) based planar MOSFETs have been used in standard SSR for low-voltage/high-current AC/DC applications. Besides, last generation of 650 V Si Super-Junction (SJ) MOSFETs [19] are identified as a promising solution since they enable a significant reduction in the specific on resistance ($R_{\mathrm{on,sp}}$) < 1 $\Omega\cdot\mathrm{mm}^2$, with a consequent lowering of the conduction losses (on-state resistance ($R_{DS(\mathrm{on})}$) ~19 mΩ) for a wide range of currents, compared to IGBTs.

Although Silicon Carbide (SiC) based devices have not been available in the 600 V range [20], few devices have recently emerged. Concretely, SiC MOSFETs with smaller $R_{\mathrm{on,sp}}$ than their Si counterparts are now in the market. This accounts for similar $R_{DS(\mathrm{on})}$ with an order of magnitude smaller chip sizes [21], [22]. Consequently, higher power densities are feasible: i.e. 650 V SiC trench MOSFETs, with $R_{DS(\mathrm{on})}$ ~29 mΩ, or 1.2 kV SiC planar MOSFETs, with $R_{DS(\mathrm{on})}$ ~34 mΩ.

Concerning SiC JFETs, commercially available 1.2 kV normally-on vertical trench structures [23] present low $R_{DS(\mathrm{on})}$ ~45 mΩ, while devices with a lateral channel component [24] present slightly higher $R_{DS(\mathrm{on})}$ ~70 mΩ. The normally-off alternative co-packages vertical normally-on trench JFETs with a normally-off low-voltage Si MOSFET in a cascode configuration, and presents marginally higher $R_{DS(\mathrm{on})}$ ~60 mΩ and ~45 mΩ for 1.2 kV and 650 V devices respectively.

SiC Bipolar-Junction-Transistors (BJT) feature several improvements over Si BJT, being a higher current gain and a smaller on-state voltage drop [25] the most important ones for the studied application (equivalent $R_{DS(\mathrm{on})}$ ~20 mΩ, for 1.2 kV). At present, there is a very low commercial availability of these devices although their potential could increase with the development of new applications.

Together with SiC devices, Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) [20] are quickly emerging and gaining a significant market presence in the < 650 V range [26]. Since these devices are natively normally-on switches, enhancement-mode HEMTs and cascodes have rapidly appeared as normally-off solutions [27]. The most performing devices are 650 V normally-off insulated gate HEMTs with $R_{DS(\mathrm{on})}$ ~32 mΩ, p-GaN gate HEMTs with $R_{DS(\mathrm{on})}$ ~70 mΩ and GaN cascodes, with $R_{DS(\mathrm{on})}$ ~41 mΩ.

3) Other combination of devices

An additional BDS solution results from embedding any of the devices presented in the last section into a diode bridge [28]. Using SiC Schottky diodes will provide the lowest forward voltage drop [22], [29], [30]. However, due to the series voltage drop of three discrete devices (two diodes and the power switch) this solution presents high on-state losses, around 3 V @ 30 A.

Furthermore, hybrid SSR BDSs combine different devices to fulfil specific needs: i.e. the anti-parallel combination of a RB-IGBT with an IGBT with a series diode, to improve the turn-on losses in a two-stage direct power converter topology [31]. Another example is the anti-series combination of a normally-off RC-IGBT and a normally-on JFET to protect matrix converters under specific driving fault conditions [32].

4) Non-commercial devices

In this section, different solutions of interest which are or have been under research are briefly reviewed.

Based on super gain BJTs [33], a first solution considers the anti-serial combination of two 600 V devices, capable of reducing the on-state power losses below the TRIACs (0.29 V @ 30 A) [34]. On the other hand, a monolithic implementation of a bidirectional bipolar device (BTRAN [35] or Double-Side Double-Gate IGBT [36]) comes from a modification of an IGBT structure so that a controlled switch is present in both top and bottom sides of the resulting symmetrical structure. Thus, it implements a BDS just by itself. The estimated conduction losses are extraordinary low: < 0.2 V @ 30 A for a 650 V device.

Finally, single packaged GaN HEMT/Si MOSFET cascodes based BDSs have been recently explored [37]. In addition, GaN HEMTs based BDS power stage can also be

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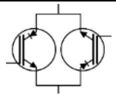
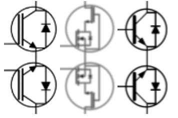
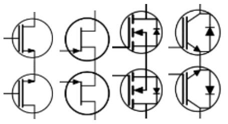
TABLE I
IMPLEMENTED BDS SOLUTIONS

Device Technology	Control Stage	Control: Complexity / Losses / Costs	Power Stage & Integration	Power: Losses / Costs	Dynamic Test
One power device					
Si TRIAC	1 std. opto-driver 1 pwr. source	↓↓ / ↑↑ / ~	 1-chip	↓↓ / ↓↓	Not passed
Multiple power devices					
Si RB-IGBTs	2 std. opto-drivers 4 pwr. sources	↑↑ / ~ / ↑↑	 2-chips / 1 conducting	↑ / ↓↓	Passed
Si IGBT+Diode SiC Cascode	1 std. opto-driver 2 pwr. sources	↓ / ↓ / ~	 4-chips / 2 conducting	↑ / ↓	
GaN Cascode				↑↑ / ↑	
SiC BJT+Diode	1 opto-coupler 1 non-std. driver 2 non-std. pwr. sources	↑ / ↑↑ / ↑↑		↑ / ↑↑	
GaN HEMTs		↑ / ↓↓ / ↑↑	 2-chips / 2 conducting	↓ / ↑↑	
SiC JFETs				↓↓ / ↑	
SiC MOSFETs	1 std. opto-driver 2 non-std. pwr. sources	~ / ↓ / ↑↑			
Si SJ MOSFETs	1 std. opto-driver 2 pwr. sources	↓ / ↓ / ~		↑ / ~	Not passed
Si RC-IGBTs				↑ / ↓↓	

implemented monolithically, as reported in [38], without a relevant increase on the chip size and no effect of the conduction power losses, since this configuration provides the reverse blocking capability without additional series P-N junctions. As GaN technology is progressing fast, monolithic GaN BDS is a very promising option.

IV. BDS IMPLEMENTATIONS

This section describes the implementation of the different analyzed BDS into test vehicles, using the most performing commercially available power devices among the options discussed in the previous section and presents an analysis of their integration, control complexity and costs. Table I shows a list of the implemented BDS solutions, each of them accompanied by their control and power stage characteristics.

The block diagram in Fig. 2 defines the common structure of all the analyzed test vehicles. They require two main inputs: a control signal (V_{IN} = 0 V / 5 V) and an external power supply (V_{AC}). On the other side, their outputs are the BDS power terminals, which are galvanically isolated from the inputs. The operation of the test vehicles is conditioned by the number of required power devices, the way they are arranged in the BDS and their driving requirements: voltage/current control, operating modes (normally-on/normally-off), etc. Therefore, a particular driving circuitry is designed for each solution. A different number of floating voltage power supplies is used for biasing the gate opto-coupled drivers (with levels V_{EE} and/or V_{CC}), which isolate V_{IN} from the power stage with a resulting gate control signal (V_{CON}) that either enables or disables the power stage devices. Moreover, the test vehicles are provided with gate and power stage overvoltage protections, while a zero current detection system ensures commutation at $|I_{\mathrm{BDS}}| \leq$ 50 mA in order to avoid excessive inductive voltage peaks across the BDS. In this work, a total of thirteen implementations based on different device technologies are developed and electrically characterized. An example of two of them is shown in Fig. 3 (a)-(b), where the size of the boards is the same in all cases for best fitting in the characterization setups. As the objective of the present section is to analyze all the feasible solutions based on different semiconductor technologies, the study of the thermal dissipation issues is postponed to the final section, and therefore, any dissipation system is observed in Fig. 3.

TRIACs (which are considered in our study as reference) are commonly driven using opto-DIAC gate drivers, but they introduce large switching delays which make them incompatible with the studied application. Therefore, the TRIAC based BDS is controlled using a standard IGBT driver to ensure the required gate current. When compared to the other solutions, it presents the lowest control complexity at affordable costs, but higher control losses, with a 1 W power supply needed. In addition, it implements the BDS power stage in a single-chip, providing the best integration characteristics.

Cascodes, IGBTs and MOSFETs based BDSs control stages are compatible with standard IGBT/MOSFET gate opto-drivers and highlight very low control losses, with only two 200 mW power supplies needed. However, common-source configuration is not feasible for the RB-IGBT BDS, which requires individual drivers and power sources for each device, with a consequently higher control complexity, losses (four 200 mW power supplies needed) and costs. Likewise, SiC MOSFETs based BDS need non-standard power sources for managing their specific driving voltages, thereby increasing both control complexity and costs but with similar input power consumption to standard MOSFETs. This contrasts with the rest of the mentioned solutions, which highlight low control

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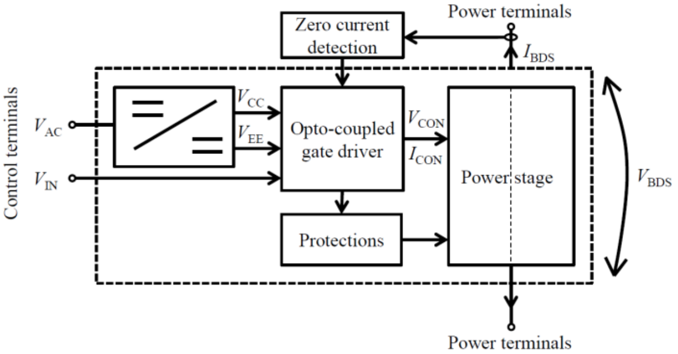

Fig. 2. Test vehicles: block diagram.

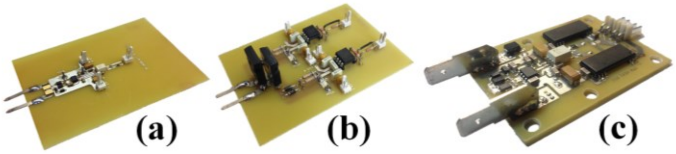

Fig. 3. Test vehicles for implementing a BDS from (a) GaN HEMTs and (b) RB-IGBTs; and (c) GaN HEMT BDS functional prototype.

complexity, losses and affordable costs. The integration characteristics are reliant on the number of involved chips: two chips (RB-IGBTs, RC-IGBTs, MOSFETs) or four chips (IGBTs+Diode, Cascodes).

With regards to GaN HEMTs and SiC JFETs based BDSs, the absence of reasonably priced gate opto-drivers for their particular driving voltages implies separated opto-couplers for providing galvanic isolation, and specific gate drivers, with higher control complexity (especially for normally-on JFETs) and costs, but the lowest control losses (only two 50 and 100 mW power supplies needed respectively). GaN HEMTs and SiC JFETs present Self Commutated Reverse Capability (SCRC), which provides natural "freewheel paths" in case that the transistors do not commutate simultaneously when conducting in the third quadrant. In addition, GaN HEMTs lateral structure makes it possible a monolithical integration of the BDS power stage [38]. However, considering only commercially available devices, both solutions present similar integration characteristics as RC-IGBTs and MOSFETs based BDSs, with two chips required. Besides, GaN HEMTs do not feature avalanche capability. Therefore, their Breakdown Voltage (BV) process is destructive and a higher security margin is required when compared to the other technologies. For that reason, this solution is provided with drain-source overvoltage protection by adding a Transient Voltage Suppressor (TVS) between both of the BDS power terminals.

Lastly, the substantially high continuous gate currents required to keep SiC BJTs on-state result into high control losses, with the requirement of a 10 W power supply, and the need for separated opto-couplers and drivers.

Static and dynamic analyses have been performed so as to study the electrical behavior of these test vehicles.

V. STATIC CHARACTERIZATION

In the studied application framework there is a clear predominance of the conduction losses since the BDSs are commutated at very low switching frequencies. To go deeper into this, the static I-V curves are extracted for each BDS test vehicle in forward and blocking modes using a curve tracer TEK 371A. Given that the active device areas cannot be precisely extracted we considered their bare die areas, which have been measured using a Scanning Acoustic Microscope (SAM) Sonoscan GEN-5. From those areas, the static current densities (J_D) are calculated and J_D-V_{BDS} curves are obtained for each solution, so that the static analysis can be extended from specific references to device technologies. In this calculation, the die areas are totaled when more than one device is simultaneously conducting current. Concerning their static I-V characteristics, all considered solutions have demonstrated to be applicable for implementing the BDS function. Those based on bipolar devices highlighted an off-set voltage which may result in slight distortions of the AC currents/voltages at the BDS in the zero-crossing region. This may not represent a remarkable problem in practical applications but an increase of the power losses. Conversely, HEMTs, MOSFETs and JFETs based BDS experienced a symmetrical conduction in the first and third quadrants.

However, the performance in terms of the conduction losses shall depend on the current waveform amplitude and morphology. In order to perform a comparative evaluation of the different device technologies, a FOM is defined as the dissipated power per semiconductor unit area for a sinusoidal current density ($J_D(t)$) with amplitude (J_D) and period T_p (1):

$$\mathrm{FOM}(J_D) = \frac{1}{T_p}\int_{t=0}^{t=T_p} J_D(t)\cdot V_{\mathrm{BDS}}(J_D(t))\cdot dt \qquad (1)$$

where $J_D(t) = J_D \cdot \sin(2\pi t/T_p)$. This FOM is presented in three categories, depending on the semiconductor material of the device technologies under test: Si, WBG and hybrid (Cascodes based on Si and WBG devices combination). Fig. 4 (a)-(c) depicts the FOMs for each category at a junction temperature (T_j) of 25 ºC. As may be deduced from Fig. 4 (a), the TRIAC presents the lowest (the best) FOM of the many Si based solutions for $J_D \geq 55$ A/cm^2, with Si SJ MOSFETs as the first alternatives to TRIACs. On the other hand, 1200 V trench SiC JFETs stands out from 650 V WBG based BDS, closely followed by trench and planar SiC MOSFETs and GaN HEMTs (Fig. 4 (b)). Furthermore, the 650 V cascoded SiC JFET alternative presents a better performance than that of the cascoded GaN HEMT (Fig. 4 (c)), leading to the expectation of a significant improvement for the BDS application in case that stand-alone 650 V SiC JFETs were commercially accessible. Moreover, this analysis reveals a close proximity between SiC based devices and GaN HEMTs power densities, which may imply that a final decision could depend on other conditioning factors.

Since the operating temperature in a real application will differ from the studied at 25 ºC, further analysis is presented to evaluate how the BDS performances are influenced by the temperature. The FOMs are measured and presented at $T_j = 100$ ºC in Fig. 4 (d)-(f). In this scenario, Si based BDS are hardly affected by the temperature except for SJ MOSFETs, whose power density is dramatically reduced (Fig. 4 (d)). Conversely, WBG devices are affected by the temperature, with a higher derating of GaN devices above SiC Fig. 4 (e)-(f).

With the exception of the TRIAC, all studied devices show positive forward voltage drop coefficient of variation with

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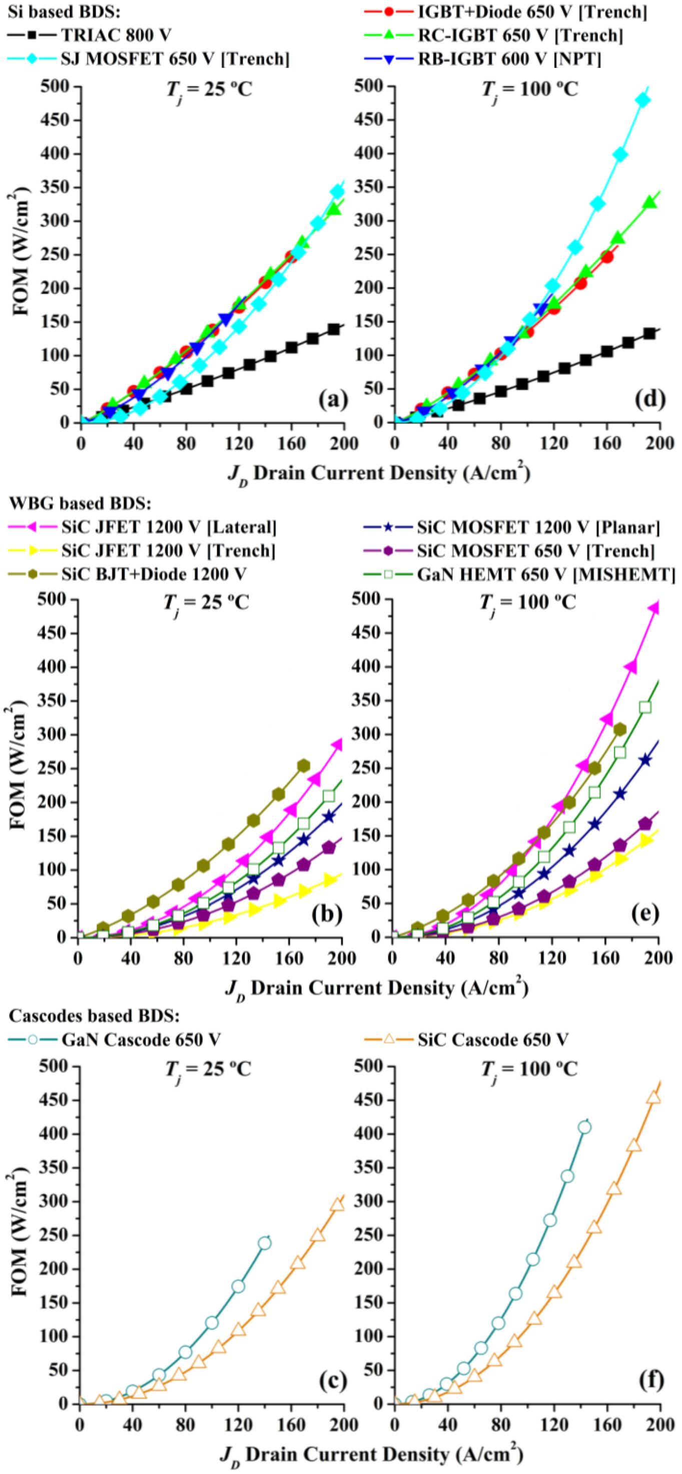

Fig. 4. FOM vs Drain current density (J_D) at 25 ºC and 100 ºC for (a, d) Si, (b, e) WBG and (c, f) Cascodes based BDS respectively.

temperature for practical current levels, making it possible the current scalability of the BDS solutions by the devices parallelization, with special mention to unipolar devices. This allows substantial reductions of the conduction power losses, summarized in Table I for the different analyzed technologies.

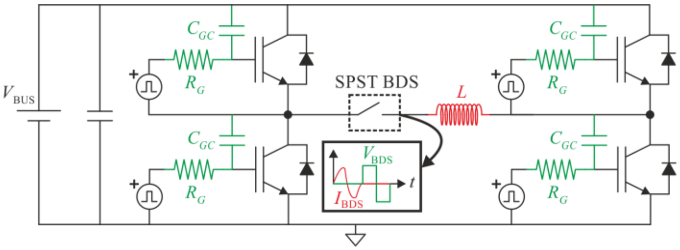

Fig. 5. Schematic of the designed test platform with flexible *dV/dt* (green) and/or *dI/dt* (red) adjustment.

VI. DYNAMIC CHARACTERIZATION

A. Dynamic test platform:

As it was previously mentioned, although the analyzed solid state BDSs will not be controlled at high switching frequencies, they will conduct high-frequency currents and must support high-frequency voltages when blocked. Testing their behavior in a real application converter involves many practical difficulties and, for this reason, a specific test platform has been designed for performing the BDSs dynamic analyses. It is based on a full-bridge converter topology where the BDS under test is connected in series with an inductive load (Fig. 5). This setup makes it possible to identify any BDS malfunction, limitation or performance degradation on a wide range of *dV/dt* and/or *dI/dt* across the BDSs. Concerning its implementation, a control board establishes a set of specific switching conditions (e.g. flexible dead times for the IGBTs, frequency of the output waveforms, etc.). Moreover, a power board applies square shape voltage and triangular shape current waveforms at the load, with flexible and independent *dV/dt* and *dI/dt* values. The different *dV/dt* are achieved through capacitances connected between the gate-collector terminals of the inverter switches (C_{GC}, rough tuning) in combination with different gate resistance values (R_G, fine tuning). Besides, an independent *dI/dt* is possible by changing the load inductance (L) of the bridge. Both capabilities have been experimentally demonstrated for *dV/dt* from 350 V/µs to 5000 V/µs and *dI/dt* from 40 A/ms to 7000 A/ms. A simplified SPICE simulation model of the whole platform is used to calculate the applicable C_{GC}, R_G and L values for a specified *dV/dt* and *dI/dt* test conditions.

The dynamic BDS behavior is analyzed when commutated from conduction to blocking state: first a 15 A current peak triangular AC current (*dI/dt* = 6765 A/ms) flows through the BDS. Then it is switched to blocking state at 300 V V_{BUS} (*dV/dt* = 520 V/µs) and subjected to a bidirectional voltage between its terminals, so that to evaluate its susceptibility to spurious turn-on. Such *dV/dt* and *dI/dt* values are typical of the induction cooking appliances in our working framework.

B. Dynamic test results:

The experimental results for the different BDS are depicted in Fig. 6, where green waveforms represent the BDS control signal, V_{CON}, blue waveforms are the current through the BDS, I_{BDS}, and black waveforms are the voltage drop between the BDS terminals, V_{BDS}. For illustrative purposes, the collector-emitter voltage at the lower left IGBT ($V_{CE(LL)}$) in Fig. 5 is also included in orange color. In a functional BDS it is expected

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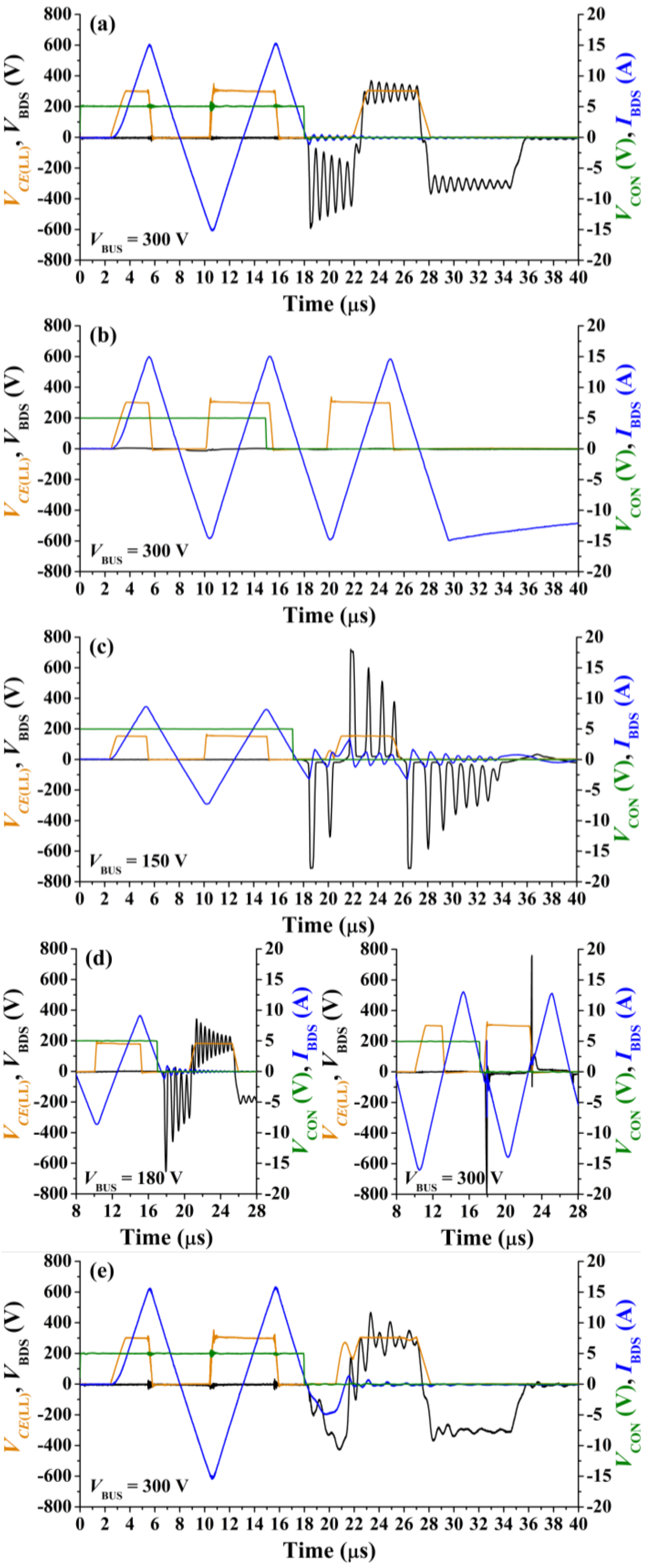

Fig. 6. Dynamic analysis of (a) GaN HEMTs, (b) Si TRIAC, (c) Si SJ MOSFETs, (d) Si RC-IGBTs and (e) SiC BJTs based BDS at different V_{BUS}.

that at the blocking instant I_{BDS} reaches zero, just while the BDS starts to withstand V_{BUS}. At this moment, the parasitic RLC elements of the circuit may provoke oscillations, with different contributions coming from the variation of the devices non-linear parasitic capacitances. As it has been demonstrated from experimental and simulation results, the amplitude and frequency of the current oscillations are linked to the devices output capacitances (C_{oss}). This fact explains the lower oscillation frequencies observed in slower devices. Moreover, once switched-off, the BDS is subjected to a bidirectional voltage, V_{BDS}.

TABLE II
HEATSINK SELECTION

R_{th} [ºC/W]	Weight [g]	Size [mm]	T [ºC]
1	450	110 x 80.5 x 70	59.5
1.63	400	100 x 75 x 100	80
2.8	200	100 x 47 x 51	125

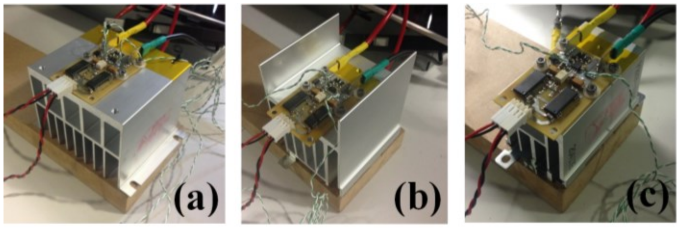

Fig. 7. GaN HEMT based BDS prototype mounted in three heatsinks: (a) R_{th} = 1 ºC/W, (b) R_{th} = 1.63 ºC/W and (c) R_{th} = 2.8 ºC/W.

Most of the studied solutions pass the dynamic tests (Table I) with special mention to GaN HEMTs (Fig. 6 (a)) and SiC based BDSs (similar waveforms than in Fig. 6 (a)). Any spurious switching due to high dV/dt in blocking state was observed for all the implemented BDSs.

The TRIAC fails switching off the AC current due to highly exceeding its maximum rated $(dI/dt)_C$ in the studied application (Fig. 6 (b)), as already mentioned in Section III.

A remarkable result concerns the SJ MOSFET based BDS. As shown in Fig. 6 (c), once this solution is switched to blocking state, two problems are immediately evident: first, an abnormal voltage peak close to the device nominal BV, even at a low 150 V V_{BUS} voltage. Second, the significantly high-current peaks flowing through the devices after turn-off. Those behaviors are linked to the devices internal structure, but further analyses about these issues remain to be undertaken and are out of the scope of this paper. Therefore, it is concluded that SJ MOSFET technology shows dynamic controllability problems for the studied application.

IGBT+Diode and RC-IGBT based solutions were expected to show similar dynamic performances, but the latter presents considerably higher voltage parasitic oscillation peaks, motivated by its lower C_{oss}. Therefore, nominal BV is reached at V_{BUS} = 180 V, leading to the device destruction at V_{BUS} = 300 V (Fig. 6 (d)). Those oscillations can be alleviated by limiting the commutation dV/dt using snubber output capacitances at the RC-IGBTs collector-emitter terminals.

Regarding the SiC BJT+SiC Schottky Diode BDS, the device presents significantly lower voltage oscillations when commutated to blocking state than any other solution, but highlights a current peak after turn-off caused by the BJTs reverse recovery process (Fig. 6 (e)), which might be reduced in case that the SiC BJT and diode were integrated into a single chip solution [39]. RB-IGBTs together with all SiC and

GaN based BDS highlight good dynamic characteristics, and amongst them all, GaN HEMTs present an excellent performance and are established as a promising solution to replace EMRs in the mid-term with lower expected costs.

C. Functional prototype and final application test

Finally, one of the best SSR BDS candidates to replace EMR is implemented into a fully functional prototype (illustrated in Fig. 3 (c)) [40], and successfully tested in an induction heating application. The purpose of this test is to compare the trade-off between integration and thermal management of small-size packaged EMRs with a SSR BDS. Owing to their critical thermal behavior, SMD packaged GaN HEMTs have been selected to implement this functional prototype. The prototype is kept in conduction state and connected in series to the coil of a commercial induction cooking appliance working at an average power level (1-2 kW), at which the measured RMS load current is around 16 A when using a standard cooking pot. The same dV/dt and dI/dt values apply than the used for performing the dynamic tests. The power dissipation becomes a relevant design challenge, particularly considering that the devices are SMD packaged. Therefore, every application needs to be evaluated in light of this situation. Three different heatsinks with different sizes and thermal resistances (R_{th}) have been selected (Fig. 7 (a)-(c)), so that an evaluation can be made regarding the trade-off between volume/weight and device maximum temperature. As it is very difficult measuring the true T_j value under operation, a temperature reference (T) is acquired at the devices package using a thermocouple (T will be slightly lower than T_j). The temperatures reached after 600 s (the time required for starting 3 dm^3 water boiling in the pot) are presented in Table II, which quantifies the trade-off between the BDS level of integration and its thermal limits. It is expected that future improvements on GaN technologies (lower $R_{DS(\mathrm{on})}$, higher operating temperatures, etc.) will account for higher power densities compared to current EMR.

VII. CONCLUSIONS

This work demonstrates that improved alternatives to the EMRs based on advanced commercially available power semiconductor devices are possible in home appliances applications involving high dV/dt and dI/dt values. All the studied solutions provide the required I-V static characteristics for implementing the BDS function, where SiC JFETs, SiC MOSFETs and GaN HEMTs based BDSs performed above the rest with the lowest conduction voltage drops. Furthermore, an even better performance is expected for SiC JFETs in case that 600-650 V switches were commercially available. Regarding the dynamic analysis, several technologies have been identified to suffer from anomalous behaviors (TRIAC, SJ MOSFET and RC-IGBT). Conversely, IGBT+Diode based BDS constitutes a cost-effective solution, but together with RB-IGBTs presents relatively high power losses due to the off-set voltage, but will not be as affected by temperature as stand-alone and cascode WBG-based solutions. Also, SiC MOSFETs, SiC JFETs and, to a lesser extent, SiC BJT+Diode based BDS present excellent dynamic characteristics, although JFET and BJT driving requirements show a higher complexity. Besides, these devices have a less expected costs drop in the short-term than GaN HEMTs, whose superior static and dynamic behaviors, and the further integration improvement from the possibility of implementing the BDS monolithically, revealed them as the best candidates to replace the EMRs. Nevertheless, thermal management of GaN based BDS is critical as inferred from the test results of the prototype developed in this work. This issue will be less relevant as the technology maturity will increase.

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Analysis of Solid State Relay Solutions Based on Different Semiconductor Technologies

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Keywords

«Industrial application», «Induction heating», «Power semiconductor device», «Device application», «Device characterisation».

Abstract

This paper provides an analysis on the design, implementation and operation of Bi-Directional Switches (BDS) based on power semiconductor devices intended to replace Electro Mechanical Relays (EMR) in home appliances. Static and dynamic characterizations of test vehicles developed using different power device semiconductor technologies (TRIAC, Super Junction (SJ) MOSFET, IGBT…) are presented. At this time, emerging Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) seem to be very suitable for the mentioned applications. Actually, GaN HEMTs based BDS has demonstrated to be the best solution to replace EMRs, with a high expectation to a significant cost reduction.

Introduction

EMRs are the cheapest solution for commutating power sub-circuit blocks and have been in use up to now for implementing BDS in industrial electronics applications [1]. However, they present a set of disadvantages (e.g., slow response, presence of moving parts, acoustic noise, high input power consumption, short life, presence of electric arcs during commutation, large size and weight) which intend to be removed by a semiconductor devices based design.

This work focuses on implementing a Single-Pole, Single-Throw (SPST) BDS, which can be operated in two states: blocking state, where its two terminals are disconnected one from each other (high impedance state), and conduction state, where they are both connected together (low impedance state). Furthermore, the BDS has to be capable of blocking voltage between its terminals in both directions while opened, and allowing a bidirectional current flow while closed (AC applications). The most commonly used Single-Pole, Double-Throw (SPDT) function can be considered as an extension of the SPST case and all the results derived from our study can be extended to the SPDT relay.

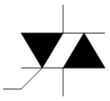
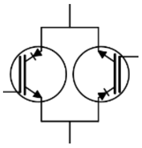
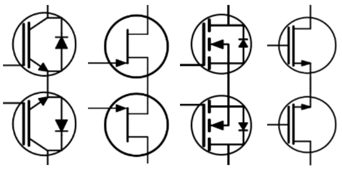
The presented BDSs aim to be used in home appliances, such as induction cookers for inductors multiplexing [1], main power supply connection switches, etc. This framework implies rated voltages and current levels of 600-1200 V and 20-70 A for the power devices involved in the study. Fast switching capability is not a main requirement but the BDS must convey high frequency AC currents (tens of kHz), involving relatively high dV/dt and dI/dt values (in the range of 500 V/µs and 6700 A/ms respectively). The main characteristic demanded to the analyzed BDSs was as low as possible conduction losses.

There exist a wide range of possible implementations for the BDS function based on semiconductor devices, which are conditioned by their individual characteristics. The most relevant implementations are depicted in Table I. The TRIAC [2] solution is in fact the only single device capable of implementing a BDS by itself.

Another possibility consists in a solution based on two RB-IGBTs [4]-[7]. As the RB-IGBTs provide bidirectional voltage blocking and unidirectional current conduction capabilities, two of these devices are arranged in anti-parallel for implementing the BDS function [7] [8].

Furthermore, IGBT+Diode (in Co-Pack package) [9], normally-on Silicon Carbide (SiC) JFETs [10], SJ MOSFETs [11] and normally-off GaN HEMTs [10] [12] provide bidirectional current conduction and unidirectional voltage blocking capabilities, so an anti-series arrangement of two of these devices is required for implementing the BDS function [8] [13]-[15].

Table I: Implemented BDS Solutions Classification

Device	**Device characteristics**	**BDS implementation symbol**	**BDS function**
One power device			
TRIAC	Bidirectional voltage blocking and bidirectional current conduction		One device only
Multiple power devices			
RB-IGBTs	Bidirectional voltage blocking and unidirectional current conduction		Anti-parallel arrangement of two devices
IGBT+Diode SiC JFETs SJ MOSFETs GaN HEMTs	Unidirectional voltage blocking and bidirectional current conduction		Anti-series arrangement of two devices

This paper starts describing the implementations of the different analyzed BDS into test vehicles. These test vehicles have been implemented using the most performing power devices commercially available in the voltage and current ranges of interest, focusing on the 600 V – 40 A rated values. Then, their static and dynamic characterization results are depicted in the following sections. Finally, a discussion of those results is presented in the last section, together with the conclusions of this work.

BDS Implementation

The BDS solutions based on power semiconductor devices introduced in the previous section have been implemented in test vehicles. As it is depicted in the block diagram of Fig. 1, all these test vehicles have two main inputs: an external power supply (V_{AC}) and an input control signal (V_{IN} = 0 V / 5 V); while their outputs are the two power terminals. The implementation of these test vehicles is determined by the driving requirements of each power device: switching characteristics (voltage/current control and levels, parasitic capacitances), operation modes (normally-on or normally-off), number of required power devices and the way they are arranged in the BDS, etc. Therefore, a specific driving circuitry is designed for each solution. One or more floating voltage power supplies are used for biasing an opto-coupled gate-driver (at levels V_{EE} and/or V_{CC}) which isolates the input signal V_{IN} from the power stage, resulting into a gate control signal (V_{CON}) for enabling (bidirectional current conduction, I_{BDS}) or disabling (bidirectional voltage blocking, V_{BDS}) the power stage devices. In addition, each test vehicle has been provided with overvoltage protection devices between gate-source and drain-source terminals. As the objective of the present work was to analyze all the possible solutions based on different semiconductor technologies, in a first step the study of the thermal dissipation issues was postponed for a second phase. For this reason, any heat-sink or dissipation system is observed in Fig. 2. This approach allowed the development and electrical characterization of up to 6 test vehicles, and the selection of the most promising solutions to be fully developed in future works.

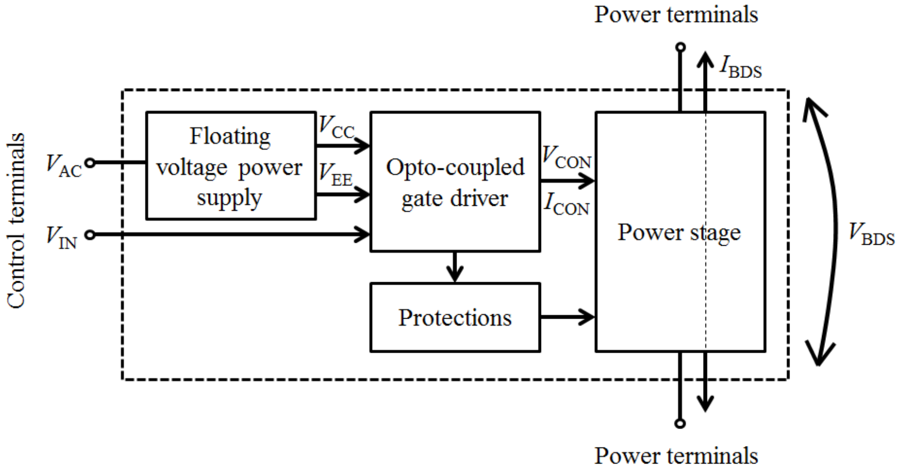


Fig. 1: Block diagram of the test vehicles.

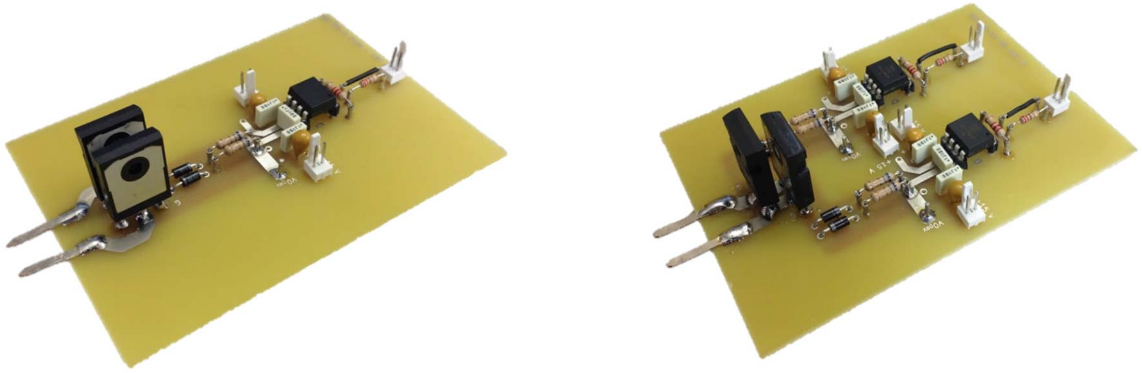


Fig. 2: Test vehicles for implementing a BDS from IGBT+Diode (co-pack) and RB-IGBTs.

The TRIAC based BDS requires just one single-chip device and one opto-DIAC gate driver, thereby presenting the best integration characteristics, the lowest control complexity and costs.

The implementations based on IGBTs, and MOSFETs present a good ease of control as their driving voltages make them compatible with standard IGBT/MOSFET gate drivers including an opto-coupler at the input. However, a common source configuration is not possible for the RB-IGBT BDS, and it requires two separate drivers and four power sources (as it can be derived from the picture in Fig. 2) for implementing the V_{CC} and V_{EE} voltages (see Fig. 1), with a consequently higher control complexity and costs. In addition, together with IGBT+Diode based BDS, they present lower integration characteristics as four individual chips are involved.

Regarding the GaN HEMTs and SiC JFETs based BDSs, due to the unavailability of reasonably priced commercial gate opto-drivers for their specific driving voltages, these solutions require separated opto-couplers for providing galvanic isolation, together with specific gate drivers for managing their individual driving voltages: V_{CON} = 7 V / -2 V for GaN HEMTs, V_{CON} = 2 V / -15 V for SiC JFETs, with an increased control complexity and costs. Furthermore, both implementations result in very robust solutions, as conduction in the third quadrant (SCRC or Self Commutated Reverse Capability) provides natural “freewheel paths” in case that both transistors do not commutate simultaneously. However, thanks to their lateral structure, GaN HEMTs provide additional integration capabilities since a monolithical integration of the BDS power stage is possible as it has already been presented in many publications [16]-[19]. In addition, GaN has an extra advantage compared with SiC as a result of the enhanced mobility of electrons, which translates into a device with a smaller size for a given R_{on} and breakdown voltage (BV). Despite the rest of the considered devices, the selected SiC JFETs are normally-on switches. Therefore, two different versions of the same BDS have been implemented for evaluating the BDS performance when using a non-inverted opto-coupler and the one for enabling a normally-off control of the BDS. In addition, together with SJ MOSFETs BDS, SiC JFETs BDS integration characteristics are in the grey area between GaN HEMTs BDS or TRIACs and IGBTs based BDS, as only two individual chips are required.

In order to study the electrical behavior of the different test vehicles, static and dynamic analysis have been performed.

Static Characterization

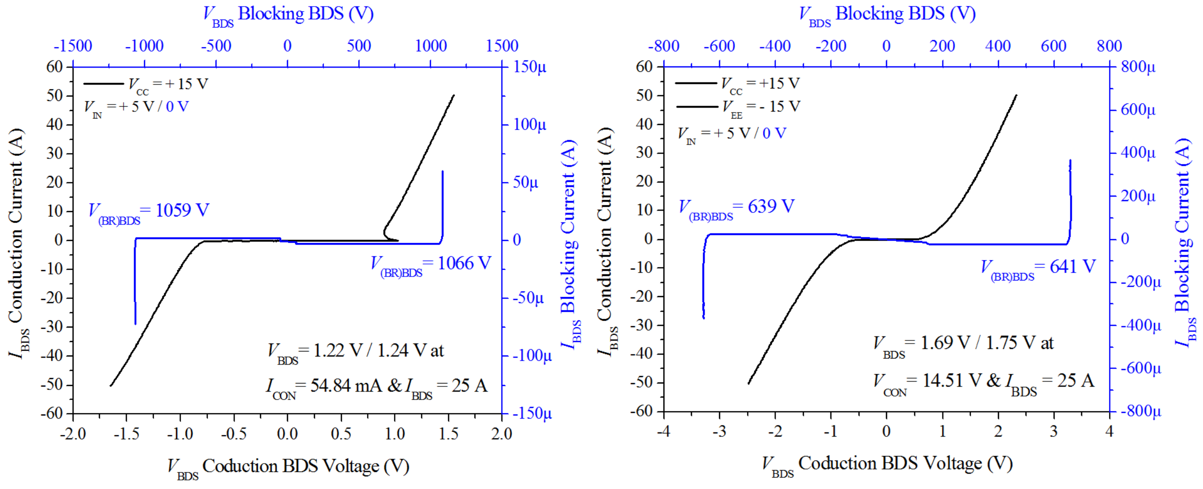
The static analysis includes the extraction of the static I-V curves of the analyzed BDS test vehicles in forward and blocking modes using a curve tracer. From these results, their on-state resistance (R_{on}), on-state voltage drop (V_{BDS}) and conduction losses are extracted.

Fig. 3 shows the static test results and highlights V_{BDS} @ I_{BDS} = 25 A (and at the corresponding gate driving I_{CON} or V_{CON} depending on the involved power devices). Blue curves are representative of BDSs voltage blocking capability (breakdown voltage ($V_{(BR)BDS}$)). Alternatively, black curves are representative of BDSs current conduction capability. Static analyses demonstrate that all the studied solutions are capable of implementing the BDS function. Those based on bipolar devices show an off-set voltage in their I-V curves which translates in slight distortions of the AC currents/voltages flowing through the BDS in the zero-crossing region, while SiC JFETs, SJ MOSFETs and GaN HEMTs BDS have no off-set voltage and experience symmetrical switching. However, this fact does not represent a serious problem in practical applications but increases the conduction power losses.

The best performance in terms of the conduction power losses is achieved by the implementations based on TRIACs and SJ MOSFETs. However, it is noted that as GaN HEMTs are an emerging technology, for the moment when the static tests were performed a brand new device with almost 3 times lower R_{on} was still not available. A BDS implementation based on these new devices would lower V_{BDS} @ I_{BDS} = 25 A close to TRIACs. It is worth to point out that in the framework of the studied applications, conduction losses are predominant as the BDSs are used at very low switching or commutation frequencies. Concerning the SiC JFETs it is also relevant to consider that the devices analyzed in this work are rated for 1200 V BV. Consequently, the availability of 600 V devices (not commercially accessible) could improve significantly their figures of merit for the BDS application.

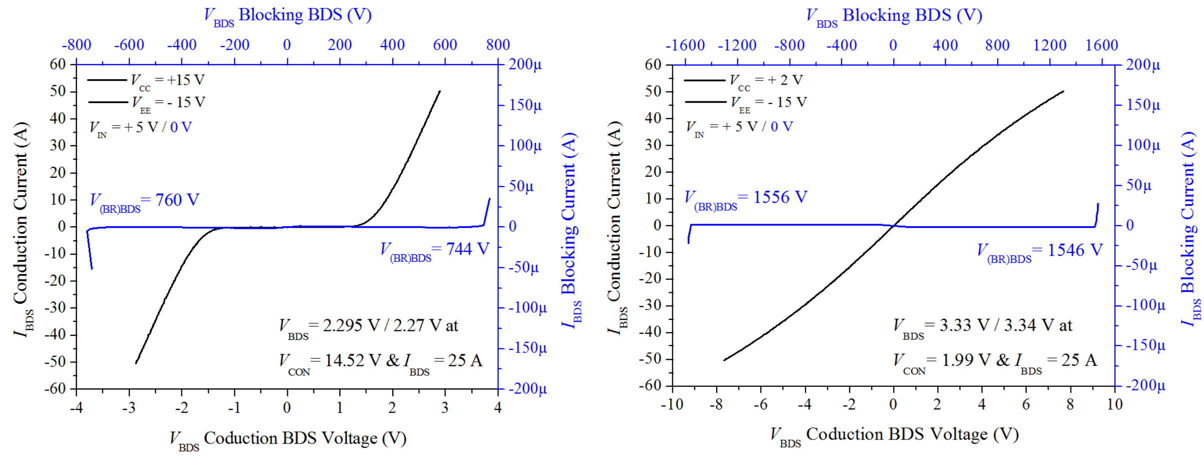
All analyzed devices (except the TRIAC) show positive forward voltage drop coefficient with temperature for practical current levels, meaning that the current scalability of the BDS solutions is possible by parallel interconnection of devices. In this sense, an additional benefit of the unipolar devices is that as they do not show an off-set voltage, their paralleling allows a significant reduction of the conduction power losses.

Finally, it is worth to mention that as GaN HEMTs do not show avalanche capability, their BV process is destructive and higher security margin is required compared with the other devices. Accordingly, drain-source overvoltage protection is provided by placing a transient voltage suppressor (TVS) between the BDS power terminals.



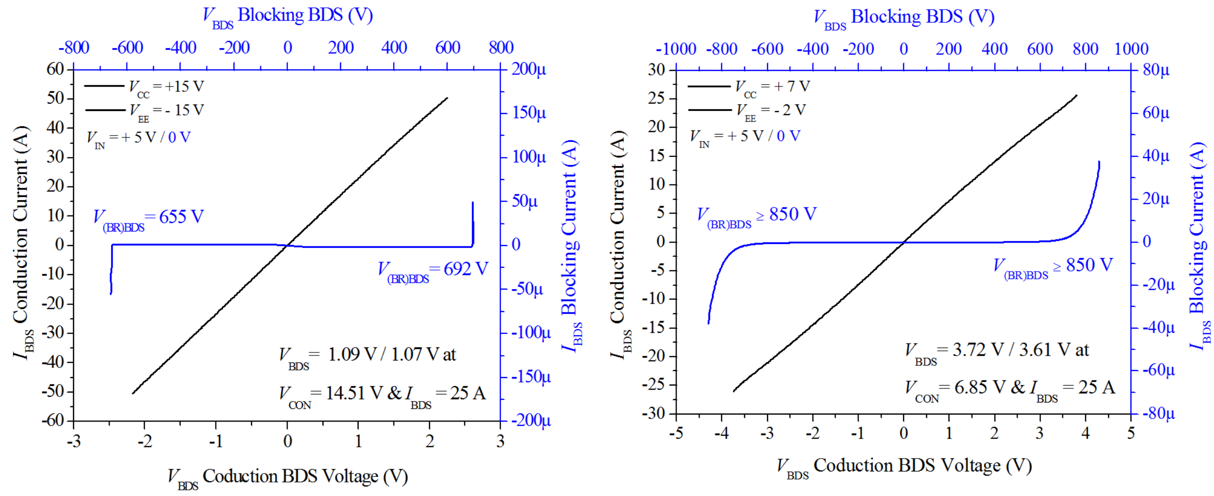
(a) Static analysis of a BDS based on a TRIAC

(b) Static analysis of a BDS based on RB-IGBTs



(c) Static analysis of a BDS based on IGBT+Diode

(d) Static analysis of a BDS based on SiC JFETs



(e) Static analysis of a BDS based on SJ MOSFETs

(f) Static analysis of a BDS based on GaN HEMTs

Fig. 3: Static I-V characteristics obtained for the six analyzed BDS solutions.

Dynamic Characterization

A specific test platform, based on a full-bridge converter topology, was designed for performing the dynamic analysis. It applies for zero crossing current analysis of the proposed BDSs and aims to easily identify any malfunction on a wide range of *dV/dt* and/or *dI/dt* across the BDS under test. The following experimental results are collected using the aforementioned test vehicles.

In these tests, first a triangular AC current flows through the BDSs (15 A current peak, *dI/dt* = 6765 A/ms) and is then switched to blocking state (300 V, *dV/dt* = 520 V/µs). These *dV/dt* and *dI/dt* values are typically found in induction cooking applications. Green waveforms in Fig. 4 represent V_{CON}, black waveforms are the voltage drop between terminals of the BDS, V_{BDS}, and blue waveforms are the current through the switch, I_{BDS}.

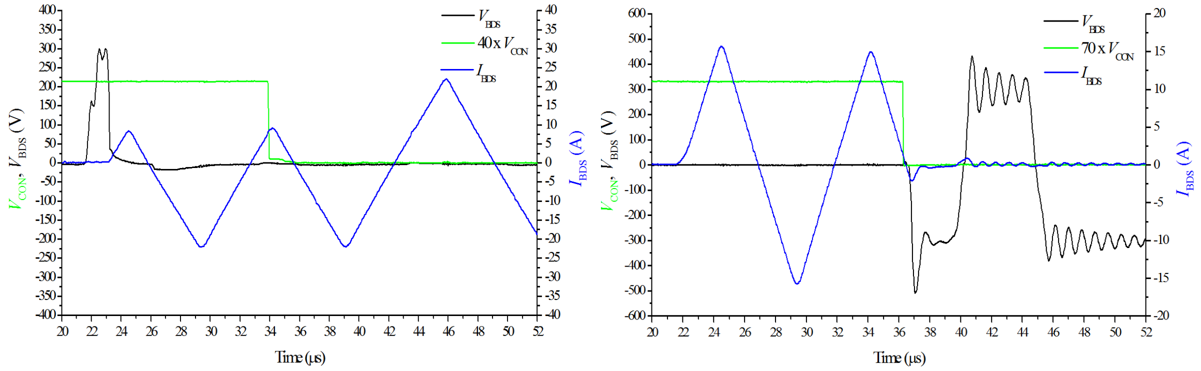
In general, for a functional BDS we expect the following behavior: at the blocking instant, I_{BDS} stops flowing through the BDS after a few parasitic oscillations, while the BDS starts to withstand a bidirectional voltage. The mentioned oscillations are caused by the parasitic RLC elements of the circuit with a different contribution for each device, caused from the diverse variation of their non-linear parasitic capacitances. The amplitude of those oscillations is related to the devices output capacitance, while their frequency is conditioned by the devices BV.

Most solutions pass the dynamic tests with special mention to GaN HEMT and SiC JFET based BDSs. As it can be observed, the TRIAC is not capable of switching off because of highly exceeding its maximum rated *dI/dt* for the specified value in the studied application. Furthermore, the selected opto-DIAC gate driver introduces large delays at the beginning of the test (Fig. 4 (a)), which can be easily fixed by using a standard IGBT driver and correctly dimensioning the gate resistance of the TRIAC for voltage controlling the device.

SiC JFETs present good dynamic characteristics but high conduction power losses. However, extending this analysis to lower BV devices (< 1.2 kV), which are still not available for the moment, will improve the performance of this solution.

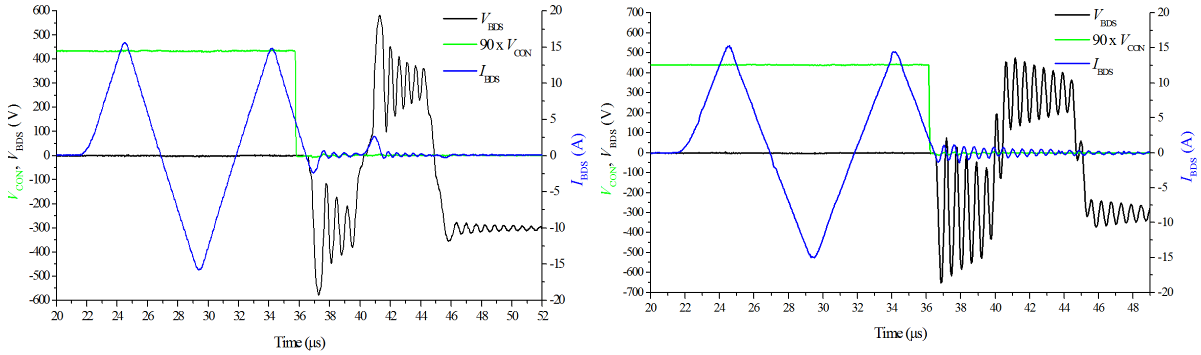
Perhaps one of the most relevant results of our study concerns the SJ MOSFET devices that showed very promising static characteristics. As it can be observed in Fig. 4, once the SJ MOSFET test vehicle is switched from conduction to blocking state, it experiences several problems: first, at a blocking voltage of 150 V it appears an abnormal voltage peak, close to the device nominal BV. In addition, once switched-off, a significant current peak flows through the devices. This issue seems to be related with the devices internal structure, but a complete explanation about this abnormal behaviour is not completely undertaken. From this analysis it is concluded that SJ technology shows controllability problems for the present application.

Finally, GaN HEMTs have been confirmed to be a promising solution to replace EMRs in a medium term from their excellent dynamic behavior.



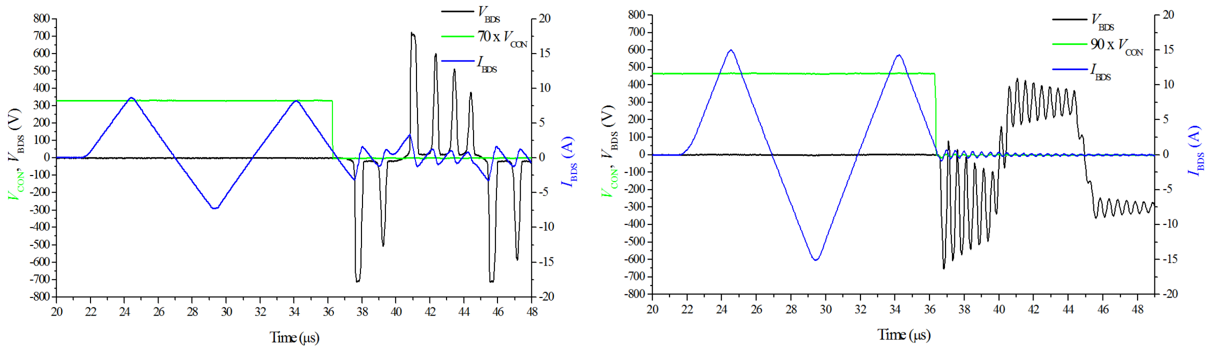
(a) Dynamic analysis of a BDS based on a TRIAC

(b) Dynamic analysis of a BDS based on RB-IGBTs



(c) Dynamic analysis of a BDS based on IGBT+Diode

(d) Dynamic analysis of a BDS based on SiC JFETs



(e) Dynamic analysis of a BDS based on SJ MOSFETs

(f) Dynamic analysis of a BDS based on GaN HEMTs

Fig. 4: Dynamic conduction to blocking state test results.

Conclusion

This work reveals that alternatives to the EMR based on semiconductor devices are possible in home appliances applications, involving high frequency currents and voltages. The studied solutions provide the required I-V static characteristics for implementing the BDS function. However, a significant disparity exists between the best and the worst performance in terms of their control complexity, power losses, costs, etc. TRIAC and SJ MOSFETs appeared initially as very promising since they provided superior static characteristics, performing the lowest conduction voltage drops of all studied implementations. However, as a consequence of their anomalous behaviors (maximum rated *dI/dt* exceeded for the TRIAC and abnormal current peaks for the SJ MOSFET) both technologies have to be discarded for the studied application. Regarding the IGBT based solutions, IGBT+Diode BDS is robust and cost-effective, but together with RB-IGBTs present relatively high power losses due to the off-set voltage. SiC JFET based BDS presents excellent dynamic characteristics regardless the additional opto-driver implementation difficulties, but relatively high conduction power losses, in part due to the lack of commercial devices in the 600 V voltage range. Moreover, these SiC devices have a less expected costs drop in the short term than for GaN HEMTs. Finally, from their superior static and dynamic characteristics and the additional integration improvements from the possibility of implementing the BDS monolithically (lateral device), GaN HEMTs have been revealed as the best solution to replace EMRs in the mid-term. Only their thermal management seems to be critical and will be analyzed in future works.

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Analysis of Bidirectional Switch Solutions Based on Different Power Devices

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***Abstract*—The numerous limitations of Electro Mechanical Relays (EMRs) for implementing Single-Pole, Single-Throw (SPST) Bi-Directional Switches (BDS) lead to new developments based on power semiconductor devices. This work gives an insight into the design and operation of BDSs based on the combination of unidirectional voltage blocking and bidirectional current conduction power devices, which aim to substitute EMRs in home appliances. The developed BDSs are fully characterized.**

***Keywords*—Bidirectional switch, SPST, relay, anti-series, power device.**

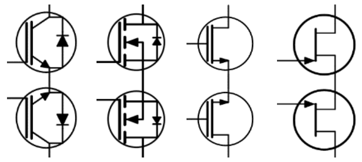
I. INTRODUCTION

The Electro Mechanical Relay (EMR) is one of the most spread components in industrial electronics systems. Although it shows severe limitations in terms of switching speed, acoustic and electronic noise generation, wearing of moving parts, etc. it provides the cheapest solution for connecting or isolating power sub-circuit blocks [1]. Typical EMRs provide the Single-Pole, Double-Throw (SPDT) switch function that can be also implemented from two Single-Pole, Single-Throw (SPST) switches controlled in a complementary way. A SPST Bi-Directional Switch (BDS) is meant to operate in two different states: a blocking state, where its two terminals are disconnected from each other (high impedance) and voltages are blocked between them, and a conduction state, where both terminals are connected together (low impedance) thus allowing a bidirectional current flow (AC applications).

The BDS can be implemented from different power semiconductor devices, whose individualities and characteristics determine the complexity and in some cases limit the performance of the BDS. An example is the TRIAC [2], [3], which is not capable of switching off the high *dI/dt* AC currents present in induction heating appliances [4], which implies rated voltages and current levels of 600-1200 V and 20-70 A for the involved BDS power devices. Furthermore, the use of bidirectional voltage blocking and unidirectional current conduction devices (for example RB-IGBTs) [5]-[7], from which a BDS is made up by the anti-parallel arrangement of two devices [7], [8], is not spread and presents high power losses (relatively high conduction voltage drops) and driving complexity. These drawbacks leave room for using unidirectional voltage blocking and bidirectional current conduction power devices from which a BDS is made up by the anti-serial arrangement of two devices [8]-[11] (Table I). In particular, this work focuses on using normally-off IGBT+Diode (combined together in the so called Co-Pack package style) [12], RC-IGBTs [13], Super-Junction (SJ) MOSFETs [14], Silicon Carbide (SiC) MOSFETs [15], Gallium Nitride High-Electron-Mobility Transistors (GaN HEMTs) [15], [16] and normally-on SiC JFETs [11], [15]. In this work, a set of test vehicles have been experimentally developed for implementing the BDS function from the mentioned devices in order to evaluate their performances and characteristics.

The paper will be divided as follows. First, a description of the implementations based on test vehicles is presented in Section II. Then, their static and dynamic characterization results are described in sections III and IV respectively, and briefly discussed in section V in conjunction with the conclusions of the study.

TABLE I. IMPLEMENTED BDS SOLUTIONS SYMBOLS

Device	Implementation symbol
IGBT+Diode [12] RC-IGBT [13] SJ MOSFETs [14] SiC MOSFETs [15] GaN HEMTs [15][16] SiC JFETs [11][15]	[8] [9] [16] [11] 

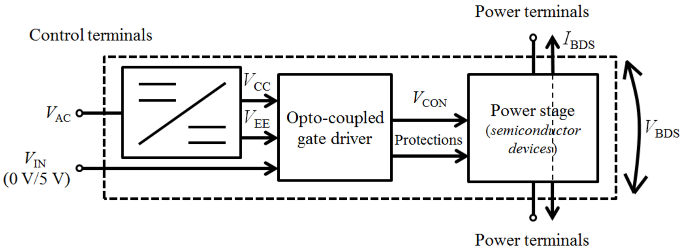


Fig. 1. Block diagram of the test vehicles.

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II. BDS IMPLEMENTATION

The BDS solutions based on the devices mentioned in Table I have been integrated into test vehicles, whose inputs and outputs are depicted in the block diagram of Fig. 1. Two main inputs are needed for controlling the test vehicles: an external power supply (V_{AC}) and an input control signal with two possible states (V_{IN} = 0 V / 5 V). Their outputs are the two power terminals: between which a bidirectional voltage blocking or current conduction is allowed.

With the driving requirements of each power device conditioning the implementation of each test vehicle, like their operating modes (normally-on or normally-off), their switching characteristics (voltage control levels and parasitic capacitances) and the number of required power devices with their corresponding arrangement, a specific driving circuitry is designed for each vehicle. It is composed by one or more floating voltage power supplies which biases a gate opto-driver (galvanic isolation) at different levels V_{EE} and/or V_{CC} and thus decouples V_{IN} from the power stage. This results into a gate control signal (V_{CON}) capable of either enable (bidirectional current conduction, I_{BDS}) or disable (bidirectional voltage blocking, V_{BDS}) the devices located at the power stage. Furthermore, the test vehicles are provided with protections, i.e. gate-source overvoltage protection by placing transient voltage suppressors (TVS) between the gate and the source of the devices. Fig. 2 illustrates an example of one of them.

The implementations based on IGBT+Diode, RC-IGBT and MOSFETs feature a better ease of control as their driving voltages make them compatible with standard IGBT/MOSFET gate drivers including an opto-coupler at the input. The IGBT+Diode BDS shows slightly worse integration characteristics since it requires 4 individual chips instead of the 2 chips required for the rest of the analysed solutions. Concerning the GaN HEMTs and SiC devices based BDSs, as a consequence of the unavailability of affordable commercial gate opto-drivers for their specific gate driving voltages, these solutions precise separated opto-couplers for providing galvanic isolation and specific gate drivers managing these particular driving voltages, different from the typical ±15 V used with standard IGBTs: V_{CON} = 7 V / -2 V for GaN HEMTs, V_{CON} = 2 V / -15 V for SiC JFETs and V_{CON} = 20 V / -5 V for SiC MOSFETs, with a consequently increased control complexity. In addition, thanks to their lateral structure, GaN HEMTs provide additional integration capabilities from the possibility of implementing the BDS monolithically, as demonstrated in many publications [17]-[19].

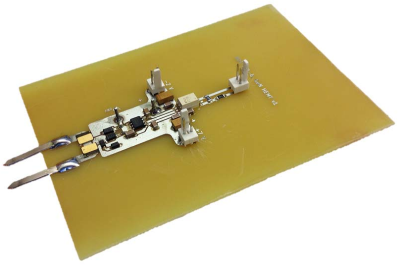

Fig. 2. Test vehicle for implementing a BDS from GaN HEMTs.

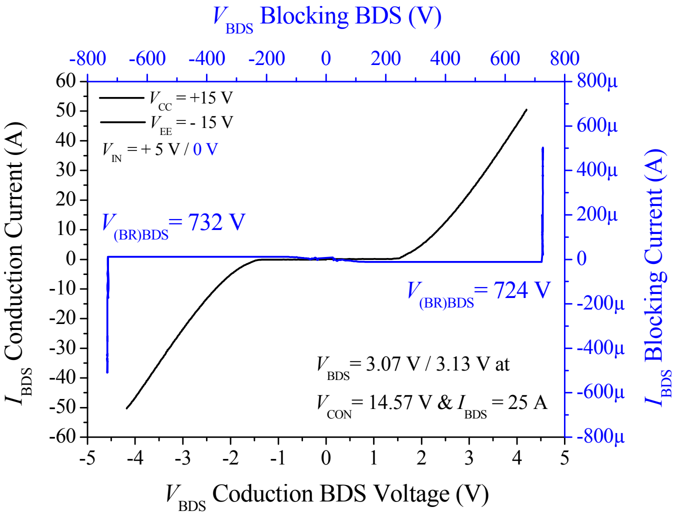

Fig. 3. Static analysis of a BDS based on RC-IGBTs.

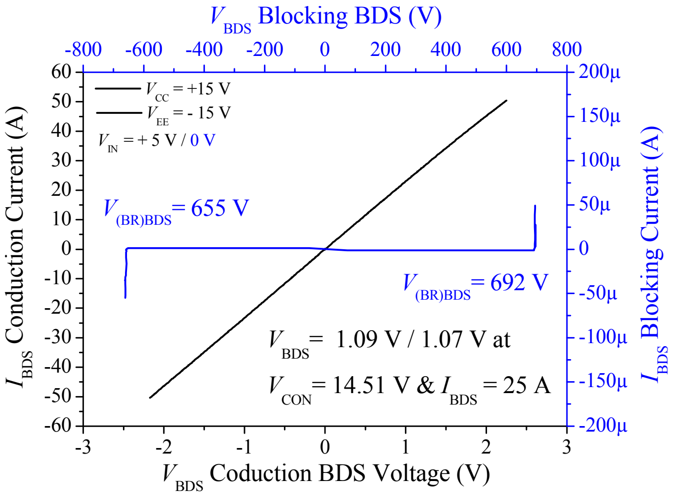

Fig. 4. Static analysis of a BDS based on SJ MOSFETs.

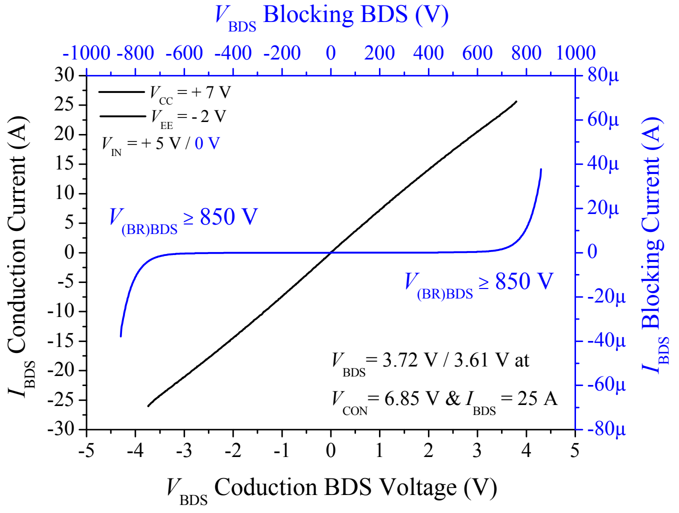

Fig. 5. Static analysis of a BDS based on GaN HEMTs.

III. STATIC CHARACTERIZATION

First, the static I-V curves of all the BDS test vehicles are extracted in forward and blocking states using a Tektronix 371 curve tracer. Conduction losses, on-state resistance (R_{on}) and conduction voltage drop (V_{BDS}) are measured for all test vehicles at the conduction current (I_{BDS}) of 25 A and the corresponding gate control value (V_{CON}). Figs. 3-5 show the results of the static tests for RC-IGBTs, SJ MOSFETs and GaN HEMTs based BDSs. Blue curves describe BDSs voltage blocking capability (breakdown voltage ($V_{(BR)BDS}$)), while black curves describe their current conduction behaviour.

Static analysis validates the designed test vehicles capability to achieve the BDS functionality. The solutions based on bipolar devices present an offset voltage that slightly distorts AC zero-crossing currents/voltages through the BDS, which does not represent a serious problem for the real applications. The lower power losses are achieved by the Si SJ MOSFETs based BDS. When these tests were performed only a GaN HEMT device with three times higher R_{on} than nowadays devices was accessible. Using last generation GaN HEMT references would lower V_{BDS} at I_{BDS} = 25 A close to SJ MOSFETs. Nevertheless, when power losses are evaluated per device area, the superior characteristics of GaN HEMTs and SiC JFETs come to light, resulting into a higher current densities and more cost-effective solutions. Besides, as the BDSs are operated at very low frequencies, the importance of the switching losses remains limited.

IV. DYNAMIC CHARACTERIZATION

Dynamic analysis were performed using a specifically designed test platform which applies for identifying any malfunction on an extensive range of *dV/dt* and/or *dI/dt*, thereby adapting to any operating frequency, and at the zero crossing current for each BDS. This characterization circuit is based on a full-bridge converter topology with the BDS under test connected in series with a load inductance. For performing the tests, first a 15 A peak and 6765 A/ms *dI/dt* triangular AC current flows through the BDSs, and it is then commutated to a blocking state up to 300 V with a *dV/dt* of 520 V/µs, which are the typical values found in induction cooking applications.

Figs. 6-8 show the results of the dynamic tests for the aforementioned selection of devices, where green waveforms describe V_{CON}, black waveforms, V_{BDS}, and blue waveforms, I_{BDS}. Once the BDS is switched to blocking state, and after a few oscillations produced by the circuit parasitic RLC elements, I_{BDS} drops to zero and starts supporting a bidirectional voltage. At that moment, at a blocking voltage of 150~180 V, both SJ MOSFETs and RC-IGBTs based BDSs present an anomalous voltage peak which reaches their rated breakdown voltage and leads to devices destruction at higher blocking voltages. Moreover, significant current peaks flow through the SJ MOSFETs once it is switched off. This phenomenon has not yet been explained in detail and is not present at any of the other test vehicles, but seems to be related with SJ MOSFETs internal structure. The rest of BDS implemented prototypes present analogous dynamic behaviors which are exemplified by the GaN HEMT BDS waveforms of Fig. 8. As it can be observed, the BDS provides ±300 V voltage blocking capability without any relevant current peak at the turn-off. The voltage oscillations are more severe in the two first blocking periods due to the variation of the non-linear parasitic device capacitances.

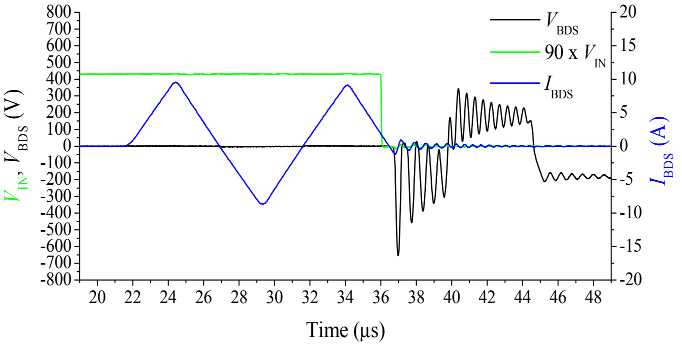

Fig. 6. Dynamic analysis of a BDS based on RC-IGBTs at a bus voltage of 180 V.

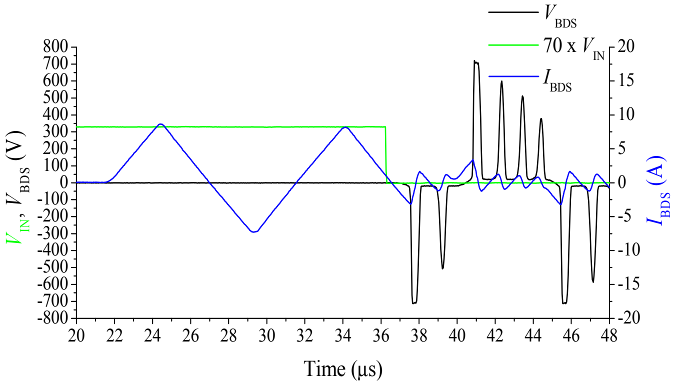

Fig. 7. Dynamic analysis of a BDS based on SJ MOSFETs at a bus voltage of 150 V.

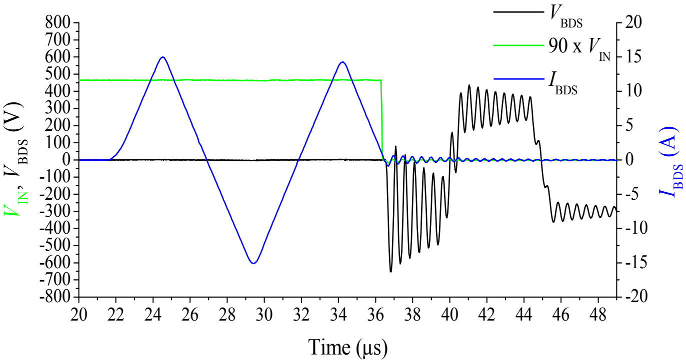

Fig. 8. Dynamic analysis of a BDS based on GaN HEMTs at a bus voltage of 300 V.

V. DISCUSSION AND CONCLUSIONS

All solutions tested have demonstrated to provide the required I-V static characteristics for implementing a BDS. Depending on their specific individualities it exists a significant disparity between the best and the worst performing device in terms of their conduction voltage drop, control complexity, costs, etc.

SJ MOSFETs provide excellent static characteristics, performing the lowest conduction voltage drop of all BDSs implementations. However, as a consequence of the anomalous current peaks experienced at the dynamic tests, it is settled that SJ MOSFET technology presents controllability problems for the studied application and has to be discarded.

Unlike RC-IGBT BDS, which present anomalous voltage peaks, the solution based on standard IGBTs+Diodes demonstrates to be robust and cost-effective, but showing fairly high power losses.

SiC JFETs and MOSFETs present excellent dynamic characteristics, and extending these analysis to lower breakdown voltage (<1.2 kV) devices, which are still not available for the moment, they will improve their static performance and reduce their conduction power losses. Unluckily, these devices present less expected costs drop in the short term than GaN HEMTs.

Finally, GaN HEMTs have demonstrated to be a promising solution to replace EMRs in the mid-term, which also provides additional integration improvements from the possibility of implementing the BDS monolithically (lateral device). Only their thermal management seems to be critical.

In conclusion, this work identifies several alternatives to the EMR based on power semiconductor devices for home appliances applications, which involves high frequency AC currents and voltages. However, some Si power devices based implementations that initially seemed to be very promising, like the SJ MOSFET or the RC-IGBT BDSs revealed critical problems which are pending for further analysis, while efficient solutions like SiC JFETs and MOSFETs are expensive and significant cost decay is not expected in the short term.

At the moment, new devices that seem to be very suitable for this application, like GaN HEMTs, are entering the market. In fact, this solution has demonstrated to be the best candidate to replace EMRs, with higher expectations to a substantial cost reduction.

ACKNOWLEDGMENT

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Feedback Oscillations in Super-Junction MOSFET-based Solid State Relays

M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, S. Llorente, and X. Jordà.

***Abstract*—Super-Junction (SJ) MOSFETs are excellent candidates for implementing Solid-State Relays (SSRs) in medium voltage scenario (300-400 V). Unfortunately, such devices present an electrical oscillatory behavior, which may compromise the power system reliability. Such a phenomenon is studied by experimentation and physics-based simulation. As a conclusion, such a behavior is a response of the inductive load to SJ-MOSFETs carrier dynamics when they switch to off state due to its internal structure based on highly doped pillars.**

***Index Terms*—Bidirectional power flow, Bidirectional Switch, Solid-State Relays, SJ-MOSFETs, Power converter reliability.**

I. INTRODUCTION

COUPLINGS amongst devices and passive elements can originate oscillatory behaviors, which can be responsible for the failure of complex power systems [1] [2]. Several studies have been reported on this [1]-[8], but not on Solid-State Relays (SSRs). SSRs are electronic devices capable of controlling the two-way current path across their terminals with a low voltage signal (Bidirectional Switches, BDS) [9] [10]. They are implemented with low-cost and bidirectional power devices (e.g., TRIACs), but several final applications in the medium voltage range (300-400 V), such as induction heating, claim for a faster response at higher current rise rates [11]. In this scenario, 600/650 V Silicon (Si) Super-Junction (SJ) MOSFETs have been identified as promising devices due to their low specific on resistance and conduction losses [12]. However, dynamic tests revealed an oscillatory phenomenon in the voltage drop (V_{BDS}) and current (I_{BDS}) of SJ MOSFET-based SSRs when commutated from conduction to blocking state [13]. This work studies its physics and proposes a solution to mitigate it on the basis of experimentation and Technology Computer-Aided Design (TCAD) [14] simulation.

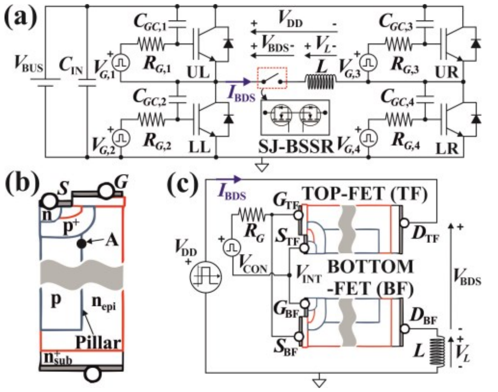

Fig. 1. (a) Schematic of the test platform with flexible dV_{BDS}/dt and dI_{BDS}/dt. (b) SJ-MOSFET basic cell cross section. (c) SSR schematics for simulation.

II. DEVICE, EXPERIMENT AND SIMULATION DESCRIPTION

The SSRs have been carried out with two 19 mΩ-650 V SJ MOSFETs connected in an anti-series common-source configuration and integrated, together with a control stage, into a small PCB board. Fig. 1 (a) depicts the test platform for their dynamic analyses. It consists on a full-bridge converter with an inductive load (L, with a voltage drop V_L) and implemented by IGBTs co-packaged with freewheel diodes, as indicated in Fig. 1 (a). In this circuit, the SSR under test is inserted in series with L, where $V_{\mathrm{DD}} = V_{\mathrm{BDS}}+V_L$. At a given bus voltage (V_{BUS}), the IGBTs are switched in pairs to create a current path from V_{BUS} to ground across L. The test platform is arranged so that I_{BDS} flows with a triangular AC waveform through the SSR, which experiences typical values of V_{BDS}, dV_{BDS}/dt and dI_{BDS}/dt of an induction heating application when $V_{\mathrm{BUS}} = 300$ V [13]. However, the SSR dynamic behavior is analyzed when SJ MOSFETs are switched, according to a control signal (V_{CON}), from on to off state at $V_{\mathrm{BUS}} = 150$ V to avoid the SSR destruction. In on state, $dI_{\mathrm{BDS}}/dt = 3400$ A/ms is set by $L = 63.4$ μH, reaching an I_{BDS} peak of 8 A. When the SSR is switched to off state under proper operation, the IGBTs gate-collector capacitors (C_{GC}) and gate resistors (R_G) fix dV_{BDS}/dt at 520 V/μs.

To reproduce the test results, two TCAD structures based on the device cross section of Fig. 1 (b) have been connected as in Fig. 1 (c), and simulated varying V_{DD} between $\pm$ V_{BUS} and omitting the test bench parasitics. Moreover, the Si default parameters of drift-diffusion model have been considered. As in [15], such structures have been set to show identical static and dynamic electrical characteristics as in measured devices. All physical quantities derived are extracted at point A of Fig. 1 (b), as their maximum values are there achieved.

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Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

III. RESULTS AND DISCUSSION

As for experimental results, Fig. 2 plots the time evolution of V_{CON}, I_{BDS}, V_{BDS}, and for descriptive purposes, the collector-emitter voltage of the low left IGBT of Fig. 1 (a) ($V_{CE,\mathrm{LL}}$). During the SSR switching from conduction to blocking state, I_{BDS} crosses zero while SSR starts to withstand V_{BUS} [9] [10], highlighting the time intervals I, II and III. Depending on the polarity of V_{DD}, Bottom-FET (time intervals I and III, $V_{CE,\mathrm{LL}}$ low) or Top-FET (time interval II, $V_{CE,\mathrm{LL}} = V_{\mathrm{BUS}}$) support V_{BUS}, while the complementary device remains in on state through its inherent diode structure (i.e., p-n$_{\mathrm{epi}}$ junction of Fig. 1 (b)) referred to as integral diode. In all cases, the following periodic spike pattern is observed in V_{BDS}. First, in spite of V_{BUS} = 150 V, a V_{BDS} spike overcomes the device rated breakdown voltage. After, further V_{BDS} spikes occur, generating damped oscillations until the V_{DD} polarity change. Simultaneously, I_{BDS} flow through the devices with a dimmed sawtooth waveform.

Such phenomena rely on the blocking voltage device physics and the inductive load response. As the device internal electric field develops as dV_{BDS}/dt manifests, the dynamics of V_{BDS} periodically changes the V_L sign. This makes the positive and negative slope of I_{BDS}, defined as $(dI_{\mathrm{BDS}}/dt)_{\mathrm{P}}$ and $(dI_{\mathrm{BDS}}/dt)_{\mathrm{N}}$, evolving differently. When Top-FET withstands V_{BUS}, $(dI_{\mathrm{BDS}}/dt)_{\mathrm{P}} = V_{\mathrm{BUS}}/L$ and $(dI_{\mathrm{BDS}}/dt)_{\mathrm{N}} = (V_{DS,\mathrm{BF}} - |V_{\mathrm{BUS}}|)/L$. Conversely, when Bottom-FET blocks V_{BUS}, $(dI_{\mathrm{BDS}}/dt)_{\mathrm{N}} = V_{\mathrm{BUS}}/L$ and $(dI_{\mathrm{BDS}}/dt)_{\mathrm{P}} = (V_{\mathrm{BUS}} - |V_{DS,\mathrm{TF}}|)/L$. As a result, a sawtooth waveform for I_{BDS} appears, which in turn, sets the dV_{BDS}/dt value. In this feedback process, I_{BDS} and V_L gradually reduce, attenuating the observed oscillations. To check this, the carrier generation/recombination rates at point A of Fig. 1 (b) by avalanche (G_{Av}) and SRH (R_{SRH}), the drain to source voltage of Bottom-FET ($V_{DS,\mathrm{BF}}$) and Top-FET ($V_{DS,\mathrm{TF}}$), as well as I_{BDS} and V_{BDS}, have been derived. Fig. 3 depicts them for the time interval I. In this interval, Bottom-FET withstands V_{BDS} while Top-FET conducts through its integral diode. Fig. 3 (a) compares the simulated (solid) and experimental (dashed) curves of I_{BDS} (in red) and V_{BDS} (in black), perfectly matching. Figs. 3 (b) and (c) illustrate G_{Av} (in wine), $|R_{\mathrm{SRH}}|$ when positive (recombination, in green) or negative (generation, in blue), $V_{DS,\mathrm{BF}}$ and $V_{DS,\mathrm{TF}}$ (both, in black). In this figure, four regimes, named A, B, C, and D, are observed according to the physics involved at each time instant t.

In regime A ($t_0 < t \leq t_2$), I_{BDS} decreases at a V_{BUS}/L rate until achieving a minimum at $t = t_2$ (Fig. 3 (a)), while Bottom-FET turns off creating an internal space charge region. Its drift region is depleted, and an internal electric field is built up, setting $dV_{\mathrm{BDS}}/dt = dV_{DS,\mathrm{BF}}/dt$. Fig. 3 (b) depicts that the space charge formation starts at $t = t_1$, when R_{SRH} reaches a negative plateau as the carriers from doping level are totally removed at the p-n$_{\mathrm{epi}}$ junction. Thus, this process takes longer in SJ devices due to their high pillar charge, and L fixes I_{BDS} as $V_L = V_{\mathrm{BUS}}$. For $t_1 \leq t \leq t_2$, $V_{DS,\mathrm{BF}}$ increases until V_{BUS} (Fig. 3 (b)), which limits the I_{BDS} minimum as $V_L = 0$. Meanwhile, the Top-FET integral diode conducts as its R_{SRH} recombination raises with I_{BDS} and $V_{DS,\mathrm{TF}}$ becomes negative (Fig. 3(c)).

For regime B ($t_2 < t \leq t_4$), I_{BDS} rises up to zero at $(dI_{\mathrm{BDS}}/dt)_{\mathrm{P}}$ (Fig. 3 (a)), as $V_{DS,\mathrm{BF}} > |V_{\mathrm{BUS}}|$. When $t_2 < t \leq t_3$, $V_{DS,\mathrm{BF}}$ increases further at $dV_{DS,\mathrm{BF}}/dt \propto |I_{\mathrm{BDS}}|$ until saturating at $\Delta V + V_{\mathrm{BUS}}$ (Fig. 3 (b)), as the drift region is totally depleted. Thus, Bottom-FET enters into dynamic avalanche [16], enhancing G_{Av} and keeping $(dI_{\mathrm{BDS}}/dt)_{\mathrm{P}} = \Delta V/L$. In $t_3 < t \leq t_4$ (Fig. 3 (b)), while $V_{DS,\mathrm{BF}} = \Delta V + V_{\mathrm{BUS}}$, G_{Av} decreases in Bottom-FET with $|I_{\mathrm{BDS}}|$ due to the current space charge modulation [16] [17]. In Top-FET, R_{SRH} recombination augments up to a peak, and after, drops with $|I_{\mathrm{BDS}}|$, as manifested in $V_{DS,\mathrm{TF}}$.

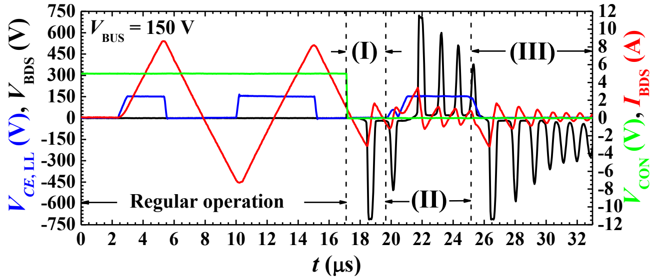

Fig. 2. Measured V_{CON}, I_{BDS} (red), V_{BDS} and $V_{CE,\mathrm{LL}}$ vs. time.

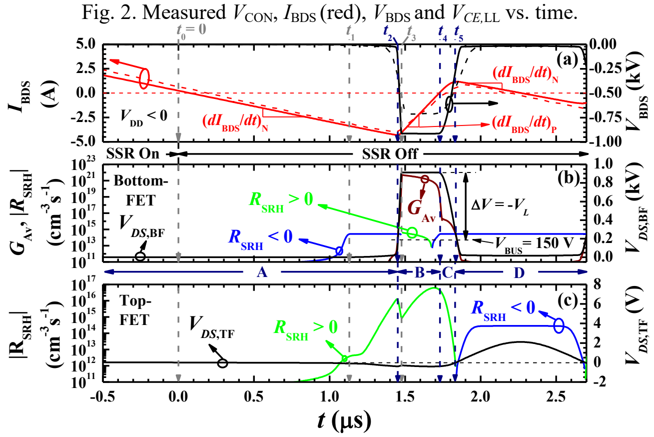

Fig. 3. Time evolution within interval I of (a) measured and simulated waveforms for I_{BDS} and V_{BDS}, (b) Bottom-FET G_{Av} and R_{SRH} at location A, jointly with $V_{DS,\mathrm{BF}}$, and (c) Top-FET R_{SRH} at location A, together with $V_{DS,\mathrm{TF}}$.

In Regime C ($t_4 < t \leq t_5$), I_{BDS} becomes positive and grows at $(dI_{\mathrm{BDS}}/dt)_{\mathrm{P}}$ until achieving a maximum at $t = t_5$, i.e., when $V_{DS,\mathrm{BF}} = |V_{\mathrm{BUS}}|$. This maximum is smaller in absolute value than that observed at $t = t_2$ (see Fig. 3 (a)). In this regime, Bottom-FET is filled in of carriers as $I_{\mathrm{BDS}} > 0$, thinning the device space charge region. $V_{DS,\mathrm{BF}}$ decreases at $dV_{DS,\mathrm{BF}}/dt \propto -|I_{\mathrm{BDS}}|$ to V_{BUS} and below, lowering G_{Av} up to reach the R_{SRH} level, as the electric field reduces. In Top-FET (Fig. 3 (c)), $V_{DS,\mathrm{TF}}$ increases to zero due to the p-n$_{\mathrm{epi}}$ depletion.

Along Regime D ($t > t_5$), I_{BDS} lessens at $(dI_{\mathrm{BDS}}/dt)_{\mathrm{N}}$ until becoming negative (Fig. 3 (a)). In this case, $V_{DS,\mathrm{TF}}$ grows up until reaching a positive maximum when $I_{\mathrm{BDS}} = 0$, dropping again to zero, due to the space charge formation and extinction. This is supported by the evolution of R_{SRH} generation in Fig. 3 (c), which roughly follows the $V_{DS,\mathrm{TF}}$ behavior: it rises up to a plateau and after decreases to zero. Thus, Bottom-FET integral diode restarts the process detailed since t_0. The diode is not supporting voltage, but when $V_{DS,\mathrm{TF}}$ stops rising, Bottom-FET starts to deplete its p-n$_{\mathrm{epi}}$ junction from net doping carriers, as indicated by the $V_{DS,\mathrm{BF}}$ increase.

To extend this analysis to the rest of oscillation cycles, Fig. 4 presents the time evolution of all variables provided in Fig. 3 along time intervals I, II and III. Fig. 4 (a) shows I_{BDS} and V_{BDS}, whereas Figs. 4 (b) and (c) depict G_{Av}, R_{SRH} and V_{DS} for

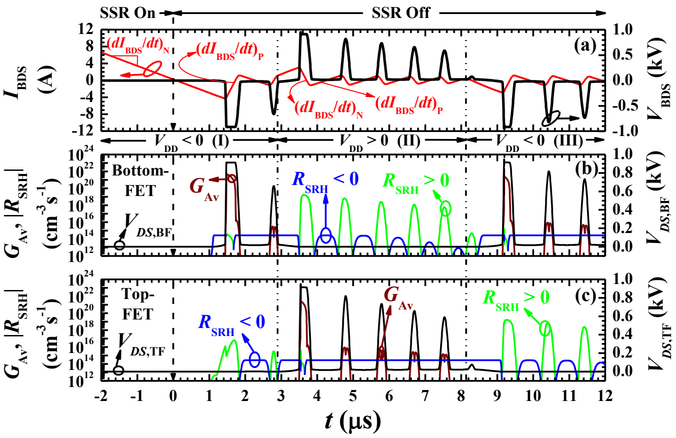

Fig. 4. Time evolution of (a) simulated waveforms for I_{BDS} and V_{BDS}, (b) Bottom-FET G_{Av} and R_{SRH} at location A, jointly with $V_{DS,\mathrm{BF}}$, and (c) Top-FET G_{Av} and R_{SRH} at location A, together with $V_{DS,\mathrm{TF}}$.

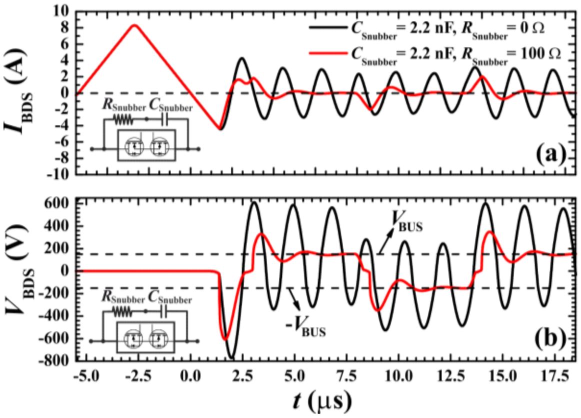

Fig. 5. Simulated waveforms for (a) I_{BDS} and (b) V_{BDS} considering several values for the snubber parameters. In the inset, schematic showing the snubber connection to the SSR.

the Bottom-FET and Top-FET, respectively. Depending on the V_{DD} polarity, the physics of the blocking device p-n$_{\mathrm{epi}}$ junction, jointly with V_L, favors the damped oscillations. In fact, $dV_{DS,i}/dt$ in the blocking device (i refers to TF or BF) and V_L (i.e., dI_{BDS}/dt) fix the oscillation period, as they establish the time to reach the maximum blocking voltage (e.g, $t_{\mathrm{D}} = t_3$-t_2 in Fig. 3 (b)) and I_{BDS} peaks (e.g, t_2 or t_5, in Fig. 3 (a)). In the first V_{BDS} spike after changing the V_{DD} polarity, dynamic avalanche always occurs due to the total depletion of SJ-MOSFET drift region, as $\Delta V < t_{\mathrm{D}}\ (dV_{DS,i}/dt)$, where i refers again to TF or BF. After, each V_{BDS} and I_{BDS} peak is decreased as dynamic avalanche limits the first I_{BDS} minimum, while its ensuing maximum is rapidly reached because a high (dI_{BDS}/dt) is ensured by the ΔV attained during dynamic avalanche. In addition, I_{BDS} modulates G_{Av} because the charge density is current dependent [16]. This modulation is observed along all oscillation cycles: two G_{Av} asymmetric maximums with a minimum between them match with the I_{BDS} maximum, minimum, and null values, respectively. As for the conducting device, R_{SRH} spikes decrease with the observed I_{BDS} peaks.

According to all stated, one solution may be the use of a passive device to rapidly fix V_{BDS} to V_{BUS}, and ensure the SSR blocking capability. This may be exerted with an RC snubber circuit: a capacitor (C_{Snubber}) with a series resistor (R_{Snubber}) connected in parallel to the SSR, whose values can be set according to the application. This is depicted in the inset of Fig. 5. Fig. 5 also presents the simulated waveforms for I_{BDS} (Fig. 5 (a)) and V_{BDS} (Fig. 5 (b)) considering several values for the snubber parameters. The oscillations are rapidly dampened and mitigated when $R_{\mathrm{Snubber}} \neq 0\ \Omega$, as it charges C_{Snubber} with a time constant, which allows C_{Snubber} to fix a constant V_{BDS}.

IV. CONCLUSIONS

The oscillatory phenomenon observed in SJ-MOSFETs-based SSRs when turned off is studied. Such a behavior is induced by the response of the inductive load to SJ-MOSFETs carrier dynamics resulting from their highly doped pillars and drift region. Namely, the SSR blocking device starts to deplete its drift region, while keeping $V_L = V_{\mathrm{BUS}}$. Due to the inductive load discharge, the device still conducts, delaying when it starts to withstand voltage. This situation worsens with the SJ-MOSFETs shrinkage trends, as thinner pillars with a higher doping level are envisaged. As a low-cost solution, the integration of an RC snubber within the SSR is proposed.

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(54) Título: **Dispositivo de aparato de cocción por inducción con al menos una unidad de conexión**

(57) Resumen:

La invención hace referencia a un dispositivo de aparato doméstico, en particular, a un dispositivo de aparato de cocción, con al menos una unidad de conexión (10a; 10d, 24d; 10e, 24e) que comprende al menos un elemento de conexión (12a-e, 14a-e).

Con el fin de mejorar la eficiencia del dispositivo de aparato doméstico, se propone que el elemento de conexión (12a-e, 14a-e) esté realizado como transistor HEMT.

En otro aspecto de la invención, se propone que la unidad de conexión (10a; 10d, 24d; 10e, 24e) comprenda al menos otro elemento de conexión (12a-e, 14a-e), el cual esté realizado de manera aproximada o exactamente equivalente al elemento de conexión (12a-e, 14a-e) y esté conectado con éste eléctricamente en serie de manera inversa.

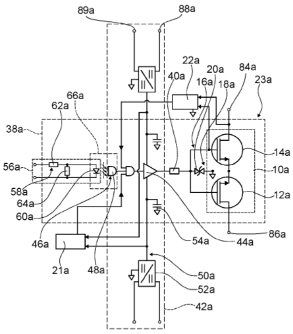

Fig. 3

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REIVINDICACIONES

1. Dispositivo de aparato de cocción por inducción con al menos una unidad de conexión (10a; 10d, 24d; 10e, 24e) que comprende al menos un elemento de conexión (12a-e, 14a-e), caracterizado porque el elemento de conexión (12a-e, 14a-e) está realizado como transistor HEMT.

2. Dispositivo de aparato de cocción según la reivindicación 1, caracterizado porque la unidad de conexión (10a; 10d, 24d; 10e, 24e) comprende al menos otro elemento de conexión (12a-e, 14a-e), el cual está conectado eléctricamente en serie con el elemento de conexión (12a-e, 14a-e).

3. Dispositivo de aparato de cocción según al menos el preámbulo la reivindicación 1 y, en particular, según las reivindicaciones 1 ó 2, caracterizado porque la unidad de conexión (10a; 10d, 24d; 10e, 24e) comprende al menos otro elemento de conexión (12a-e, 14a-e), el cual está realizado de manera equivalente al elemento de conexión (12a-e, 14a-e) y está conectado con éste eléctricamente en serie de manera inversa.

4. Dispositivo de aparato de cocción según una de las reivindicaciones enunciadas anteriormente, caracterizado porque el elemento de conexión (12a-e, 14a-e) comprende nitruro de galio.

5. Dispositivo de aparato de cocción según una de las reivindicaciones enunciadas anteriormente, caracterizado por una unidad de protección (16a-e), la cual está prevista para proteger la unidad de conexión (10a; 10d, 24d; 10e, 24e) frente a daños.

6. Dispositivo de aparato de cocción según la reivindicación 5, caracterizado porque la unidad de protección (16a-e) comprende una unidad de protección frente a la sobretensión (18a-e), la cual está prevista para evitar la sobretensión entre al menos dos terminales de la unidad de conexión (10a; 10d, 24d; 10e, 24e).

7. Dispositivo de aparato de cocción según la reivindicación 6, caracterizado porque la unidad de protección frente a la sobretensión (18a-e) comprende al menos un diodo supresor (20a-e), el cual está conectado con al menos uno de los terminales de la unidad de conexión (10a; 10d, 24d; 10e, 24e).

8. Dispositivo de aparato de cocción según una de las reivindicaciones 5 a 7, caracterizado porque la unidad de protección (16a) comprende al menos una unidad de protección frente a los cortocircuitos (22a), la cual está prevista para evitar los cortocircuitos entre al menos dos terminales de la unidad de conexión (10a).

9. Dispositivo de aparato de cocción según una de las reivindicaciones enunciadas anteriormente, caracterizado porque la unidad de conexión (10a) conforma al menos parcialmente un interruptor de conexión.

10. Dispositivo de aparato de cocción según una de las reivindicaciones enunciadas anteriormente, caracterizado por al menos otra unidad de conexión (10a; 10d, 24d; 10e, 24e), la cual está realizada de manera equivalente a la unidad de conexión (10a; 10d, 24d; 10e, 24e) y está conectada con la unidad de conexión (10a; 10d, 24d; 10e, 24e) eléctricamente en paralelo.

11. Dispositivo de aparato de cocción según la reivindicación 10, caracterizado porque la unidad de conexión (10d, 24d) y la otra unidad de conexión (10d, 24d) conforman conjuntamente al menos un conmutador selector al menos parcialmente.

12. Aparato doméstico (26a), en particular, aparato de cocción por inducción, con al menos un dispositivo de aparato doméstico según una de las reivindicaciones enunciadas anteriormente.

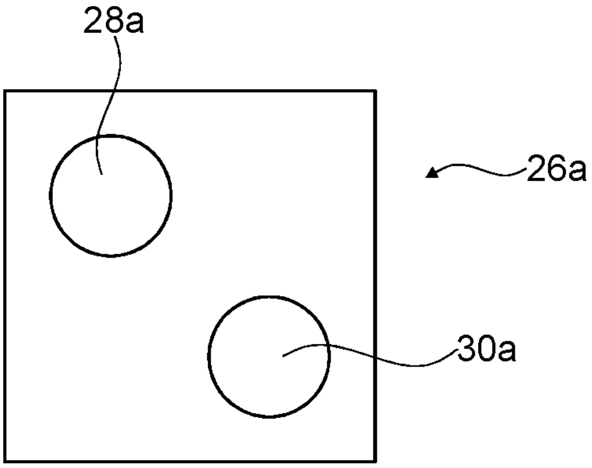

Fig. 1

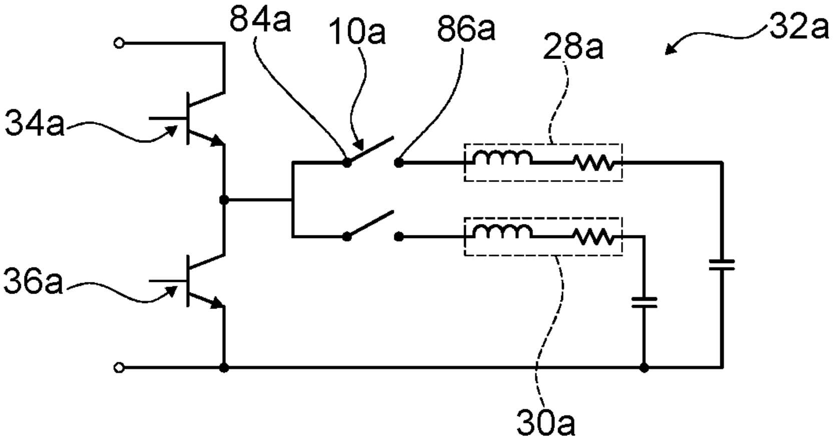

Fig. 2

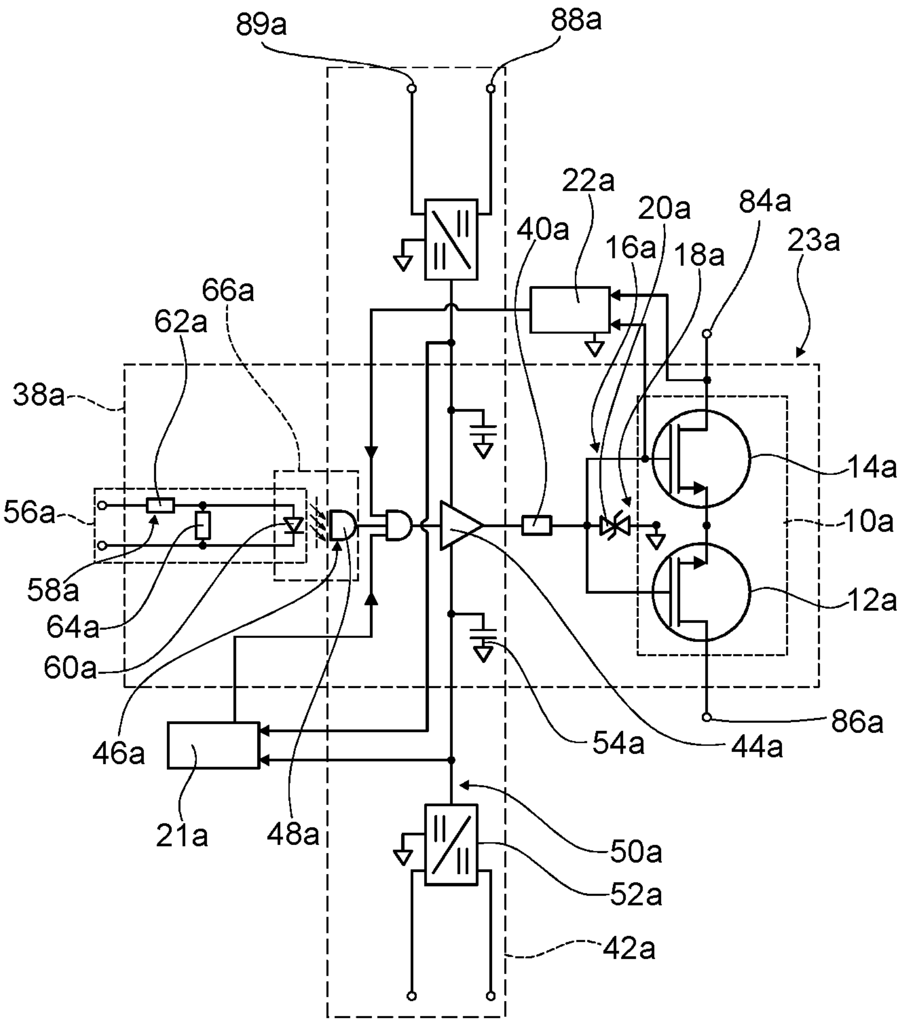
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Fig. 3

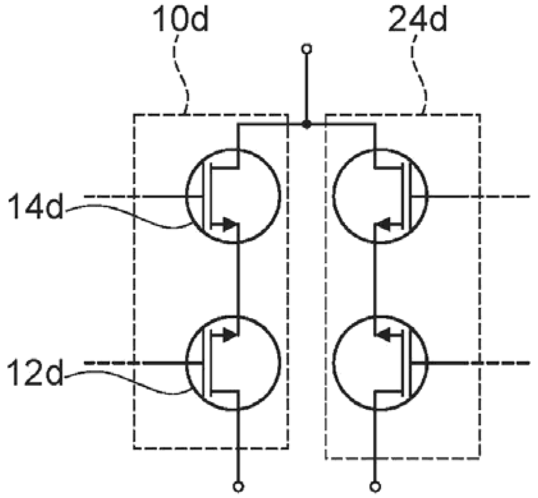

Fig. 4

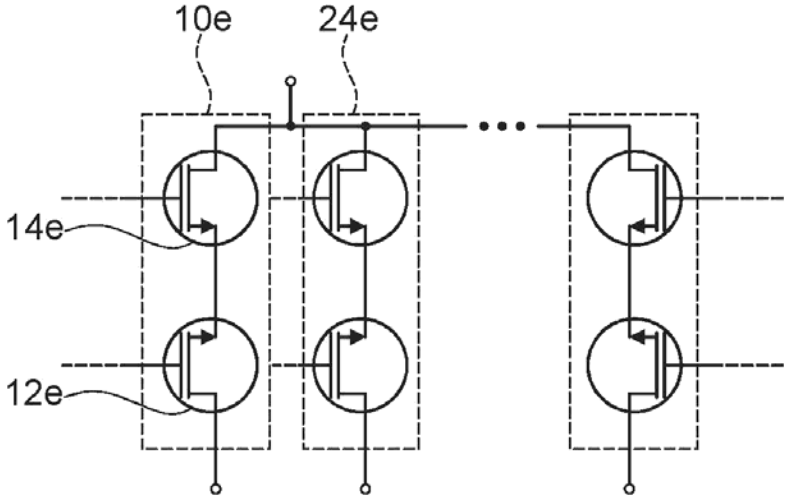

Fig. 5

OFICINA ESPAÑOLA
DE PATENTES Y MARCAS

ESPAÑA

㉑ N.º solicitud: 201631613

㉒ Fecha de presentación de la solicitud: 19.12.2016

㉜ Fecha de prioridad:

INFORME SOBRE EL ESTADO DE LA TECNICA

(51) **Int. Cl. :** Ver Hoja Adicional

DOCUMENTOS RELEVANTES

Categoría	(56) **Documentos citados**	**Reivindicaciones afectadas**
X	US 2015303916 A1 (HERNANDEZ BLASCO PABLO JESUS et al.) 22/10/2015, Todo el documento.	1-12
A	DE 102012211400 A1 (BSH BOSCH SIEMENS HAUSGERAETE) 31/01/2013, Todo el documento.	1-12
A	DE 202013003006U U1 (SIEMENS AG) 25/04/2013, Resumen de la base de datos EPODOC. Recuperado de EPOQUE; resumen.	1-12
A	WO 2015150967 A1 (BSH HAUSGERAETE GMBH) 08/10/2015, Descripción; figuras.	1-12
A	DE 202013003006U U1 (SIEMENS AG) 25/04/2013, Descripción; figuras.	1-12
A	EP 1931177 A1 (BSH BOSCH SIEMENS HAUSGERAETE GMBH) 11/06/2008, Todo el documento.	1-12
A	Yuki Niiyama et al. “Induction Heating System Operation by Soft Switching GaN Heterojunction Field Effect Transistors” Power Semiconductor Devices and ICs 19th International Symposium on, 2007. Jeju Korea. IEEE, Pi. Anonymous, 01/05/2007, Páginas 157 - 160 [en línea][recuperado el 16/10/2017]. ISSN ISBN 978-1-4244-1095-8 ; ISBN 1-4244-1095-9	1-12

Categoría de los documentos citados

X: de particular relevancia
Y: de particular relevancia combinado con otro/s de la misma categoría
A: refleja el estado de la técnica
O: referido a divulgación no escrita
P: publicado entre la fecha de prioridad y la de presentación de la solicitud
E: documento anterior, pero publicado después de la fecha de presentación de la solicitud

El presente informe ha sido realizado
☒ para todas las reivindicaciones
☐ para las reivindicaciones nº:

Fecha de realización del informe	**Examinador**	**Página**
20.10.2017	M. d. López Sábater	1/4

CLASIFICACIÓN OBJETO DE LA SOLICITUD

H03K17/96 (2006.01)
H05B6/12 (2006.01)
F24C7/08 (2006.01)

Documentación mínima buscada (sistema de clasificación seguido de los símbolos de clasificación)

H05B, H02M, H03K, F24C

Bases de datos electrónicas consultadas durante la búsqueda (nombre de la base de datos y, si es posible, términos de búsqueda utilizados)

INVENES, EPODOC, IEEE, Internet

Fecha de Realización de la Opinión Escrita: 20.10.2017

Declaración

Novedad (Art. 6.1 LP 11/1986)	Reivindicaciones	2-4,8-12	**SI**
	Reivindicaciones	1,5-7	**NO**
Actividad inventiva (Art. 8.1 LP11/1986)	Reivindicaciones		**SI**
	Reivindicaciones	1-12	**NO**

Se considera que la solicitud cumple con el requisito de aplicación industrial. Este requisito fue evaluado durante la fase de examen formal y técnico de la solicitud (Artículo 31.2 Ley 11/1986).

Base de la Opinión.-

La presente opinión se ha realizado sobre la base de la solicitud de patente tal y como se publica.

1. Documentos considerados.-

A continuación se relacionan los documentos pertenecientes al estado de la técnica tomados en consideración para la realización de esta opinión.

Documento	Número Publicación o Identificación	Fecha Publicación
D01	US 2015303916 A1 (HERNANDEZ BLASCO PABLO JESUS et al.)	22.10.2015
D02	DE 102012211400 A1 (BSH BOSCH SIEMENS HAUSGERAETE)	31.01.2013
D03	DE 202013003006U U1 (SIEMENS AG)	25.04.2013

2. Declaración motivada según los artículos 29.6 y 29.7 del Reglamento de ejecución de la Ley 11/1986, de 20 de marzo, de Patentes sobre la novedad y la actividad inventiva; citas y explicaciones en apoyo de esta declaración

Reivindicación 1:

El documento del estado de la técnica anterior considerado más cercano a esta primera reivindicación independiente es D01, que divulga un dispositivo de aparato de cocción por inducción con al menos una unidad de conexión que comprende al menos un elemento de conexión (20), caracterizado porque el elemento de conexión (42,30) está realizado como transistor. De entre los tipos de transistor posibles puede emplearse uno tipo HEMT, como se lee en la descripción del documento, párrafo [0005]. Por lo tanto, esta primera reivindicación carece de novedad según el artículo 6 de la Ley de Patentes 11/86.

Reivindicaciones 2 a 4, 9, 10 y 11:

Estas reivindicaciones dependientes carecen de características técnicas que, en combinación con las reivindicaciones de las que dependen, conlleven actividad inventiva según el artículo 8 de la Ley de Patentes 11/86, puesto que consisten en refinamientos en la realización del interruptor que consisten en diseños topológicos o en el empleo de materiales bien conocidos en el estado de la técnica.

Reivindicaciones 5 a 7:

En la reivindicación dependiente número cinco se incluye que el transistor empleado como unidad de conexión ha de constar con una unidad de protección. En la reivindicación seis se especifica que debe tratarse de una protección contra las sobretensiones entre dos terminales de la unidad de conexión y en la siete que esta unidad de protección debe constar con al menos un diodo supresor conectado a los terminales de la unidad de conexión.

El empleo de dos diodos unidireccionales como unidad de protección contra sobretensiones entre los terminales de una unidad de conexión es algo ampliamente conocido en el estado de la técnica. Puede encontrarse en D01 por lo que se anula la novedad de estas tres reivindicaciones. (A modo de ejemplo, también puede encontrarse en D02)

Reivindicación 8:

El empleo de una unidad de protección contra sobrecorrientes y cortocircuitos en los relés de estado sólido es habitual en el estado de la técnica, como puede ilustrar D03. Por lo tanto, esta reivindicación dependiente carece de actividad inventiva.

Reivindicación 12:

El documento D01 refiere a un aparato de cocción por inducción que incorpora al menos un dispositivo como el que se desea proteger en las reivindicaciones anteriores. Por lo tanto, esta reivindicación también carece de actividad inventiva.

(19) Deutsches
Patent- und Markenamt

(10) **DE 10 2017 222 394 A1** 2018.06.21

(12)
Offenlegungsschrift

(21) Aktenzeichen: **10 2017 222 394.4**
(22) Anmeldetag: **11.12.2017**
(43) Offenlegungstag: **21.06.2018**

(51) Int Cl.: ***F24C 7/08*** (2006.01)
H05B 6/06 (2006.01)
H05B 6/66 (2006.01)
H02H 9/04 (2006.01)

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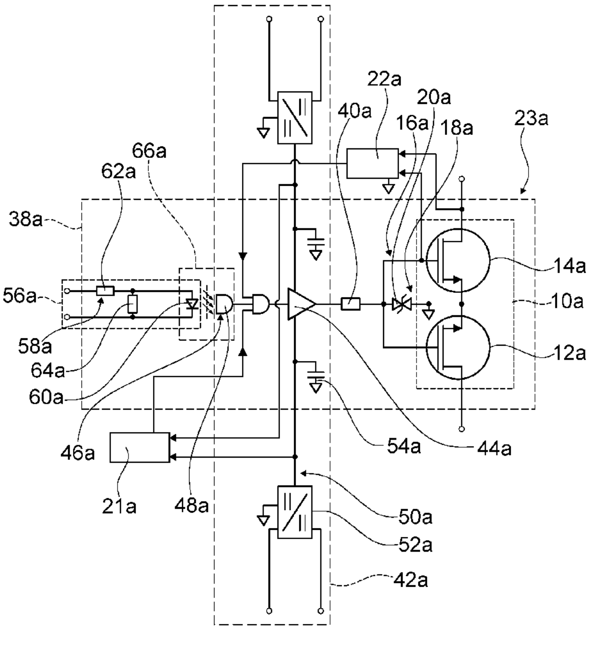
Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen.

(54) Bezeichnung: **Haushaltsgerätevorrichtung**

(57) Zusammenfassung: Die Erfindung geht aus von, einer Haushaltsgerätevorrichtung, insbesondere Gargerätevorrichtung, mit zumindest einer Schalteinheit (10a; 10d, 24d; 10e, 24e), welche zumindest ein Schaltelement (12a-e, 14a-e) umfasst.

Um eine Effizienz der Haushaltsgerätevorrichtung zu verbessern wird vorgeschlagen, dass das Schaltelement (12a-e, 14a-e) als ein HEMT-Transistor ausgebildet ist.

In einem weiteren Aspekt der Erfindung wird vorgeschlagen, dass die Schalteinheit (10a; 10d, 24d; 10e, 24e) zumindest ein weiteres Schaltelement (12a-e, 14a-e) umfasst, welches zumindest im Wesentlichen äquivalent zu dem Schaltelement (12a-e, 14a-e) ausgebildet ist und mit diesem zumindest teilweise elektrisch invers in Reihe verbunden ist.



auf Bauteile mit gleichen Bezugszeichen, grundsätzlich auch auf die Zeichnung und/oder die Beschreibung der anderen Ausführungsbeispiele, insbesondere der **Fig. 1** bis **Fig. 3**, verwiesen werden kann. Zur Unterscheidung der Ausführungsbeispiele ist der Buchstabe a den Bezugszeichen des Ausführungsbeispiels in den **Fig. 1** bis **Fig. 3** nachgestellt. In den Ausführungsbeispielen der **Fig. 4** und **Fig. 5** ist der Buchstabe a durch die Buchstaben d und e ersetzt.

[0040] **Fig. 4** zeigt ein weiteres alternatives Ausführungsbeispiel der Erfindung. Dieses alternative Ausführungsbeispiel unterscheidet sich von dem vorherigen Ausführungsbeispiel zumindest im Wesentlichen hinsichtlich einer Anzahl von Schalteinheiten. Im vorliegenden Fall weist die Haushaltsgerätevorrichtung eine Schalteinheit 10d und eine weitere Schalteinheit 24d auf. Die weitere Schalteinheit 24d ist zumindest im Wesentlichen äquivalent zur Schalteinheit 10d ausgebildet. Die weitere Schalteinheit 24d ist zumindest teilweise elektrisch parallel mit der Schalteinheit 10d verbunden. Ein zweiter Anschluss der Schalteinheit 10d ist mit einem weiteren zweiten Anschluss der weiteren Schalteinheit 24d verbunden. Die Schalteinheit 10d und die weitere Schalteinheit 24d bilden gemeinsam einen Wechselschalter aus.

[0041] **Fig. 5** zeigt ein weiteres alternatives Ausführungsbeispiel der Erfindung. Dieses Ausführungsbeispiel unterscheidet sich von dem vorherigen Ausführungsbeispiel zumindest im Wesentlichen hinsichtlich einer Anzahl von weiteren Schalteinheiten 24e. Im vorliegenden Fall weist die Haushaltsgerätevorrichtung eine Anzahl von N weiteren Schalteinheiten 24e auf. Eine Schalteinheit 10e und die N weiteren Schalteinheiten 24e sind zumindest teilweise elektrisch parallel miteinander verbunden. Die Schalteinheit 10e und die N weiteren Schalteinheiten 24e bilden gemeinsam einen Multiplex-Schalter aus.

Bezugszeichenliste

10	Schalteinheit
12	Schaltelement
14	Schaltelement
16	Schutzeinheit
18	Überspannungsschutzeinheit
20	Suppressordiode
21	Unterspannungsschutzeinheit
22	Kurzschlussschutzeinheit
24	Weitere Schalteinheit
26	Haushaltsgerät
28	Induktor
30	Induktor
32	Wechselrichterschaltkreis
34	Wechselrichter
36	Wechselrichter
38	Relais
40	Basiswiderstand
42	Betriebseinheit
44	Treiber
46	Empfangseinheit
48	photoempfindliches Element
50	Betriebsschaltkreis
52	Betriebsspannungswandler
54	Glättungselement
56	Steuereinheit
58	Steuerschaltkreis
60	Photonenemitter
62	Reihenwiderstand
64	Parallelwiderstand
66	Entkopplungseinheit
68	Widerstand
70	Widerstand
72	Widerstand
74	Operationsverstärker
76	Schaltelement
78	Widerstand
80	Operationsverstärker

Patentansprüche

1. Haushaltsgerätevorrichtung, insbesondere Gargerätevorrichtung, mit zumindest einer Schalteinheit (10a; 10d, 24d; 10e, 24e), welche zumindest ein Schaltelement (12a-e, 14a-e) umfasst, **dadurch gekennzeichnet**, dass das Schaltelement (12a-e, 14a-e) als ein HEMT-Transistor ausgebildet ist.

2. Haushaltsgerätevorrichtung nach Anspruch 1, **dadurch gekennzeichnet**, dass die Schalteinheit (10a; 10d, 24d; 10e, 24e) zumindest ein weiteres Schaltelement (12a-e, 14a-e) umfasst, welches mit dem Schaltelement (12a-e, 14a-e) zumindest teilweise elektrisch in Reihe verbunden ist.

3. Haushaltsgerätevorrichtung zumindest nach dem Oberbegriff des Anspruchs 1 und insbesondere nach Anspruch 1 oder 2, **dadurch gekennzeichnet**, dass die Schalteinheit (10a; 10d, 24d; 10e, 24e) zumindest ein weiteres Schaltelement (12a-e, 14a-e) umfasst, welches zumindest im Wesentlichen äqui-

valent zu dem Schaltelement (12a-e, 14a-e) ausgebildet ist und mit diesem zumindest teilweise elektrisch invers in Reihe verbunden ist.

4. Haushaltsgerätevorrichtung nach einem der vorhergehenden Ansprüche, **dadurch gekennzeichnet**, dass das Schaltelement (12a-e, 14a-e) zumindest teilweise aus Galliumnitrid besteht.

5. Haushaltsgerätevorrichtung nach einem der vorhergehenden Ansprüche, **gekennzeichnet durch** eine Schutzeinheit (16a-e), welche dazu vorgesehen ist, die Schalteinheit (10a; 10d, 24d; 10e, 24e) vor einer Beschädigung zu schützen.

6. Haushaltsgerätevorrichtung nach Anspruch 5, **dadurch gekennzeichnet**, dass die Schutzeinheit (16a-e) eine Überspannungsschutzeinheit (18a-e) umfasst, welche dazu vorgesehen ist, eine Überspannung zwischen zumindest zwei Anschlüssen der Schalteinheit (10a; 10d, 24d; 10e, 24e) zu vermeiden.

7. Haushaltsgerätevorrichtung nach Anspruch 6, **dadurch gekennzeichnet**, dass die Überspannungsschutzeinheit (18a-e) zumindest eine Suppressordiode (20a-e) umfasst, welche mit zumindest einem der Anschlüsse der Schalteinheit (10a; 10d, 24d; 10e, 24e) verbunden ist.

8. Haushaltsgerätevorrichtung nach einem der Ansprüche 5 bis 7, **dadurch gekennzeichnet**, dass die Schutzeinheit (16a) zumindest eine Kurzschlussschutzeinheit (22a) umfasst, welche dazu vorgesehen ist, einen Kurzschluss zwischen zumindest zwei Anschlüssen der Schalteinheit (10a,) zu vermeiden.

9. Haushaltsgerätevorrichtung nach einem der vorhergehenden Ansprüche, **dadurch gekennzeichnet**, dass die Schalteinheit (10a) zumindest teilweise einen Einschalter ausbildet.

10. Haushaltsgerätevorrichtung nach einem der vorhergehenden Ansprüche, **gekennzeichnet durch** zumindest eine weitere Schalteinheit (10a; 10d, 24d; 10e, 24e), welche zumindest im Wesentlichen äquivalent zur Schalteinheit (10a; 10d, 24d; 10e, 24e) ausgebildet ist und welche zumindest teilweise elektrisch parallel mit der Schalteinheit (10a; 10d, 24d; 10e, 24e) verbunden ist.

11. Haushaltsgerätevorrichtung nach Anspruch 10, **dadurch gekennzeichnet**, dass die Schalteinheit (10d, 24d) und die weitere Schalteinheit (10d, 24d) gemeinsam zumindest teilweise wenigstens einen Wechselschalter ausbilden.

12. Haushaltsgerät (26a), insbesondere Gargerät, mit zumindest einer Haushaltsgerätevorrichtung nach einem der vorhergehenden Ansprüche.

Es folgen 3 Seiten Zeichnungen

P-GaN HEMTs Drain and Gate Current Analysis Under Short-Circuit

M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, X. Jordà, and M. Tack

***Abstract*— Gallium Nitride High-Electron-Mobility Transistors (GaN HEMTs) are promising devices for high-frequency and high-power density converters, but some of their applications (e.g., motor drives) require high robustness levels. In this scenario, 600 V normally-off p-GaN gate HEMTs are studied under Short-Circuit (SC) by experiment and physics-based simulations (drift-diffusion and thermodynamic models). A strong drain current reduction (>70% after saturation peak) and high gate leakage current (tens of mA) are observed. All studied devices withstand the SC test at bus voltages up to 350 V, while fail at 400 V. Furthermore, its understanding is crucial to improving SC ruggedness in p-GaN HEMTs.**

***Index Terms*— GaN HEMTs, p-GaN, short-circuit, reliability.**

I. INTRODUCTION

STUDYING Wide Band-Gap (WBG) power devices under Short-Circuit (SC) conditions is essential for making them suitable for motor drive applications (e.g., railway traction or electric vehicle) [1], [2]. In this regard, SC robustness of Silicon Carbide (SiC) devices has been intensively studied in the literature [2]–[5], whereas this analysis on Gallium Nitride High-Electron-Mobility Transistors (GaN HEMTs) is scarcely reported for Depletion-mode (D-mode) HEMTs, cascoded D-mode HEMTs and other GaN technologies [4], [6]–[9]. The growing interest on p-doped gate GaN (p-GaN) HEMTs [10], [11] relies on the fact that, differently from cascoded D-mode HEMTs [7], the normally-off operation is provided free of internal resonances and ensuring gate control of the switching speed. Despite p-GaN HEMTs are commercially available [12], their SC ruggedness has never been addressed. This work analyzes the SC behavior and failure physics of p-GaN HEMTs combining measurements and Technology Computer-Aided Design (TCAD) simulations. The physics of the SC currents observed at drain (I_D) and gate (I_G) are investigated, as their behavior differs to that reported for the currently used Silicon (Si) devices in motor drives. Fig. 1 (a) depicts a higher I_D reduction (>70%) and I_G leakage (tens of mA) during SC in p-GaN HEMTs than in Si Insulated-Gate Bipolar Transistors (IGBTs; collector current I_C) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) [12]–[14].

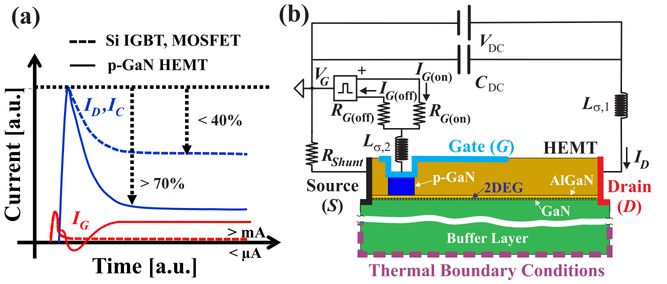


Fig. 1. (a) Illustrative comparison of I_D and I_G SC waveforms for p-GaN HEMTs with Si IGBTs/MOSFETs [12]–[14] at their maximum SC energy capability. (b) Schematic description of test circuit and TCAD structure used in experimental test and simulations, respectively.

II. DEVICE, EXPERIMENT AND SIMULATION DESCRIPTION

Four units of a commercially available 600 V p-GaN HEMT described in [15] with 140 mΩ on-state resistance (R_{on}) are selected as Devices Under Test (DUTs). According to [15], a recessed p-doped GaN layer, on top of an AlGaN/GaN heterostructure, acts as a pn-junction gate (diode-like behavior) [16] and depletes the Two-Dimensional Electron Gas (2DEG) channel beneath it when no gate-source voltage (V_{GS}) is applied (normally-off) [17]. Oppositely, when V_{GS} exceeds the gate threshold voltage ($V_{GS(\text{th})}$), the diode turns on and HEMT conduction starts [18]. Moreover, such devices are current collapse free [15] and successfully passed other reliability tests [19].

Fig. 1 (b) depicts the SC test bench schematic [20] with its parasitic inductances ($L_{\sigma,1}$ and $L_{\sigma,2}$), a DC power supply (V_{DC}), a capacitors bank (C_{DC}), and a gate driver (driving voltage V_G). Gate turn-on and -off driving is performed by two branches with customizable gate resistors ($R_{G(\text{on})}$ and $R_{G(\text{off})}$). For electrical measurements, a coaxial shunt (R_{Shunt}) monitors I_D, while differential voltage probes are used for $I_{G(\text{on})}$ (I_G sensed at $R_{G(\text{on})}$), drain-source voltage (V_{DS}), and V_{GS} acquisition. As fixed test conditions, ambient temperature (T_{A}), SC time (t_{on}), $R_{G(\text{on})}$ and $R_{G(\text{off})}$ are set for 23 °C, 10 μs and 50 Ω. In order to avoid spurious turn-on and to keep $I_{G(\text{on})}$ at 10 mA, V_G is 4 V and -3 V during on- ($V_{G(\text{on})}$) and off-states. As a testing procedure, V_{DC}

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Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

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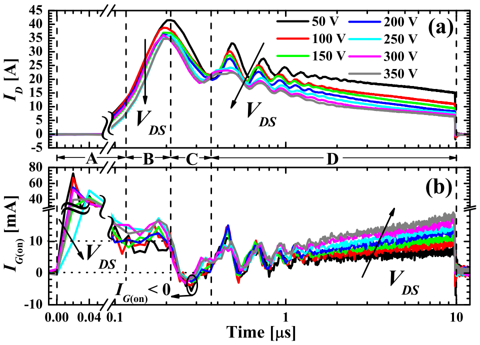

Fig. 2. Time evolution of measured (a) I_D and (b) $I_{G(\mathrm{on})}$ for different V_{DC}.

is ramped from 50 V to 400 V in steps of 50 V. Destruction of all DUTs occurred at $V_{\mathrm{DC}} = 400$ V. Besides, one DUT is cyclically tested at $V_{\mathrm{DC}} = 50$, 100 and 250 V each 60 s.

A 2D finite element structure [21] is used to understand the SC tests. As a first approximation, the HEMT cross section in Fig. 1 (b) is simulated with the default parameters of drift-diffusion and thermodynamic models in [22], as well as omitting the test bench parasitics and the p-drain structure to compensate the current collapse as indicated in [15]. The latter is emulated by considering an ideal device without trapping states. The DUTs and TCAD structure show identical R_{on} and $V_{GS(\mathrm{th})}$ ($\sim$1.2 V) for a 75 mm gate length. A voltage capability higher than 600 V is obtained for 10 μm drift length. Only the boundary conditions of the buffer layer are set to reproduce the destruction at $V_{\mathrm{DC}} = 400$ V.

III. Results and Discussion

A. Non-Destructive SC Measurements

Inspected DUTs have withstood V_{DC} voltages ranging from 50 to 350 V without apparent degradation. The invariability of I_D and $I_{G(\mathrm{on})}$ curves after ten SC tests, at $V_{\mathrm{DC}} = 50$, 100 and 250 V, points to an absence of induced permanent trapped charge or other sort of damage. Fig. 2 summarizes I_D and $I_{G(\mathrm{on})}$ measured in one of the samples. The decrement of I_D with V_{DS} and time is observed in Fig. 2 (a). At $V_{\mathrm{DC}} =$ 350 V, an I_D decay of 72% takes place during 3 μs after its saturation peak ($I_{D(\mathrm{sat})}$), whereas an almost constant I_D is observed during the rest of t_{on}. Actually, this decay improves the device ruggedness, since power dissipation is reduced. The dynamics of $I_{G(\mathrm{on})}$ is presented in Fig. 2 (b) with four time intervals named as regimes A, B, C, and D. During regime A, the DUT input capacitance is charged to enhance the 2DEG channel and, thus, to turn the device on. Afterwards, a plateau region with $I_{G(\mathrm{on})} \sim 10$ mA takes place during regime B to keep the 2DEG channel enhanced. At the beginning of regime C, when I_D reaches $I_{D(\mathrm{sat})}$, $I_{G(\mathrm{on})}$ suddenly drops to negative values. This trend contrasts to that observed at lower V_{DS} values (i.e., conventional conduction operation), where $I_{G(\mathrm{on})}$ is constant and decreases with V_{DS} at a fixed V_{GS}. Finally, despite some initial induced oscillations by $L_{\sigma,1}$ and $L_{\sigma,2}$, regime D presents a relatively high $I_{G(\mathrm{on})}$ that rises with time and V_{DS}. From a ruggedness point of view, high $I_{G(\mathrm{on})}$ in regime D is beneficial due to the consequent lowering in V_{GS} and I_D.

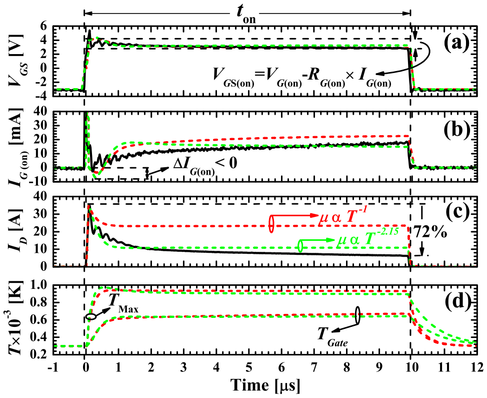

Fig. 3. Measured and simulated waveforms for (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, and (c) I_D, jointly with (d) simulated T_{Gate} and T_{Max}, in non-destructive test. $V_{\mathrm{DC}} = 350$ V.

B. SC Current Trends Analysis by Simulation

To gain insight into the non-destructive SC tests, Fig. 3 compares measured and simulated waveforms of V_{GS}, $I_{G(\mathrm{on})}$, and I_D at $V_{\mathrm{DC}} = 350$ V, and depicts also the simulated maximum and gate temperatures (T_{Max} and T_{Gate}). In this analysis, charge trapping is omitted and I_D decay is mainly attributed to thermal effects. The DUTs have been proved to be current collapse free for regular operation [19]. Besides, they have a rapid thermal response (1 μs; steady-state) and a high thermal resistance due to the buffer layer thermal properties [9]. Therefore, the temperature (T) dependence of the electrons mobility in the 2DEG channel ($\mu(T)$) is set for $\mu(T) \propto T^{-2.15}$ (instead of $\propto T^{-1}$ set by default) to obtain an excellent match with measurements. In literature, $\mu(T) \propto T^{-1.5}$ is typically considered for GaN bulk in accordance to the acoustic phonon electron scattering [22], and is commonly extended to heterojunctions modelling [23]. However, other contributions could lead to a stronger $\mu(T)$ dependence with T as results reported in [23] support. Moreover, the existence of a p-doped GaN layer in the studied DUTs is susceptible to impact $\mu(T)$ if its dopants (e.g., Magnesium) reach the 2DEG, which is still to be demonstrated. By contrast, $I_{G(\mathrm{on})}$ increases with T_{Gate} during regime D. This dependence of $I_{G(\mathrm{on})}$ is fixed by the Schottky and p-GaN contact physics. The gate electro-thermally behaves as a Schottky contact and pn-junction [16], and hence, $V_{GS(\mathrm{th})}$ decreases with T_{Gate} [24]. Besides, a high $I_{G(\mathrm{on})}$ induces a voltage drop in $R_{G(\mathrm{on})}$, which reduces V_{GS} during on-state ($V_{GS(\mathrm{on})}$) in Fig. 3 (a). In any case, T_{Max} does not reach a critical temperature for the device destruction.

Fig. 4 presents at $V_{\mathrm{DC}} = 350$ V, the profiles along the 2DEG channel of several physical magnitudes at different time instants during t_{on}. For $t \leq 0$, the HEMT withstands V_{DS} in off-state and the peaks of lateral and vertical electric fields (E_x and E_y) are located at the edges of the gate and field plate, where the highest value is achieved. When conduction starts for $0 < t \leq t_3$, the density of electrons (ϱ_e^-) enormously increases, with its profile modulated by E_x and E_y. Eventually, when $t = t_2$, E_x and E_y reach their maximum value, but suddenly drop at $t = t_3$. From this moment onwards, E_y is originated by the applied V_{GS}, and both E_x and E_y gradually

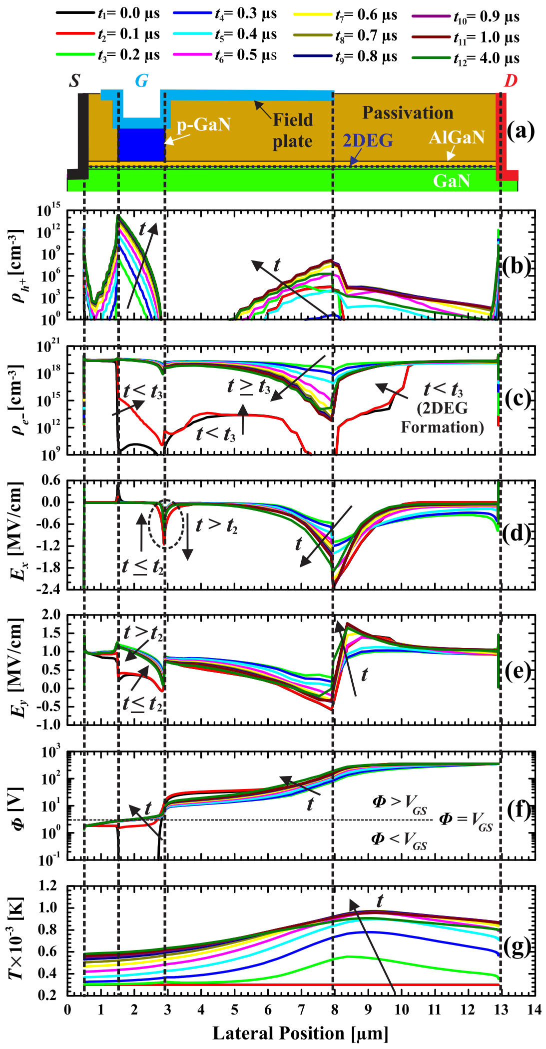

Fig. 4. Profiles extracted along 2DEG layer (see structure in (a)) at 12 time instants (up to 4 μs) corresponding to the following physical variables: (b) ϱ_h^+, (c) ϱ_e^-, (d) E_x, (e) E_y, (f) Φ, and (g) T.

increase below the gate edges. The low density of holes (ϱ_h^+) points to a negligible hole injection prior to t_3. Differently, when $t_3 < t \leq t_6$, a constant $I_{G(\text{on})}$ injects holes into the 2DEG channel, and a noticeable increase of the electric potential (Φ) and its lateral gradient appear below the gate. When $V_{GS(\text{on})}$ - $\Phi < V_{GS(\text{th})}$, the gate stops injecting holes at the surroundings of the gate right edge (lateral position 2.9 μm), producing two synchronized effects on $I_{G(\text{on})}$ and I_D. $I_{G(\text{on})}$ collapses to negative values in regime C, whereas I_D saturates at $I_{D(\text{sat})}$ due to the electron drift conduction by E_x at the gate right edge. Since the carrier velocity is saturated at this location and not at the field plate end, $I_{D(\text{sat})}$ becomes almost independent of V_{DS} when $V_{\text{DC}} > 50$ V. Within the same interval and due to a strong E_x, a large power density is dissipated close to the field plate edge, and eventually, the heat is diffused to the surrounding areas. After the drastic reduction of I_D and the dissipated power for $t > t_6$, T_{Max} remains stagnated, whereas T_{Gate} continues increasing due to the heat flow effect. In turn, $I_{G(\text{on})}$ rises as $V_{GS(\text{th})}$ lowers with T_{Gate}, and ϱ_h^+ has a lateral gradient along the gate contact due to Φ lateral profile.

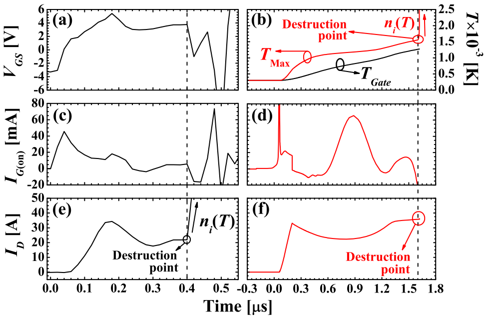

Fig. 5. Measured waveforms for (a) V_{GS}, (c) $I_{G(\text{on})}$ and (e) I_D, and simulated for (b) T_{Gate} and T_{Max}, (d) $I_{G(\text{on})}$ and (f) I_D in a destructive test. $V_{\text{DC}} = 400$ V.

C. Destructive SC Measurements and Simulations

The main measured and simulated waveforms (i.e., V_{GS}, $I_{G(\text{on})}$, and I_D, jointly with T_{Max} and T_{Gate}) for a destructive test at $V_{\text{DC}} = 400$ V are detailed in Fig. 5. Measurements are similar for all DUTs exhibiting a failure after being under SC conditions during several hundreds of nanoseconds. Prior to failure, V_{GS}, $I_{G(\text{on})}$, I_D, T_{Gate} and T_{Max} for regimes A, B and C are equal to those simulated at $V_{\text{DC}} = 350$ V. An electrical signature based on a steep I_D rise and the absence of a high leakage at the gate indicates a purely thermal destruction. This means that the semiconductor becomes intrinsic when T_{Max} locally reaches a critical temperature, as intrinsic carrier concentration $n_i(T)$ locally increases with T. Fig. 5 demonstrates that simulation predicts the thermal destruction for longer times when $T_{\text{Max}} > 1500$ K is achieved within the drift region. A shorter time-to-failure is measured due to current crowding effects, which cannot be reproduced by 2D simulations. In these experimental tests, no conventional current collapse behavior has been observed in terms of an abrupt $I_{D(\text{sat})}$ decay. Thus, the followed simulation approach without trapped charges has allowed qualitatively reproducing the experimental results.

As possible solutions to enhance the SC capability, limiting $I_{D(\text{sat})}$ by drain/source metal contact [25] or with innovative drift region engineering [26], [27], as well as increasing $\mu(T)$ dependence with T [28], are very promising. Moreover, improving heat extraction through the contacts or deposing a high thermal conductivity material on top of the device [29] can assist to overcome local thermal problems.

IV. CONCLUSIONS

The performance of 600 V p-GaN HEMTs is analyzed under SC conditions with experiments and physics-based simulations. All devices passed the SC tests for $V_{\text{DC}} \leq 350$ V and failed at $V_{\text{DC}} = 400$ V. Special attention has been paid to understand the physics of I_D reduction (>70%) and $I_{G(\text{on})}$ high leakage (>10 mA). The self-regulation of I_D under SC is due to a strong thermal dependence of $\mu(T)$. Besides, the high $I_{G(\text{on})}$ is due to a thermal reduction of $V_{GS(\text{th})}$. Added to the efforts for improving the thermal properties of the buffer layer or using thermal management solutions at die level, the precise tuning of I_D and $I_{G(\text{on})}$ waveforms by process engineering becomes a cornerstone to enable the GaN adoption in applications where SC ruggedness is mandatory.

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Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs

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***Abstract*—This paper studies by experimentation and physics-based simulation the Short-Circuit (SC) capability of several normally-off 600–650 V Gallium Nitride High-Electron-Mobility Transistors (GaN HEMTs): cascodes, p-GaN, and GaN Metal–Insulator–Semiconductor HEMTs (MISHEMTs). As a result, cascodes present the worst SC ruggedness. By contrast, p-GaN gate HEMTs and MISHEMTs provide a higher SC capability thanks to their strong drain current reduction. In addition, a valuable state-of-the-art about all commercially available technologies is also provided, which demonstrates that current GaN devices do not allow SC capability.**

***Index Terms*—Enhancement mode, failure analysis, Gallium Nitride (GaN) cascode, GaN High-Electron-Mobility Transistors (GaN HEMTs), GaN Metal–Insulator–Semiconductor HEMTs (MISHEMTs), hard switch fault, reliability, robustness, Short Circuit (SC), simulation, wide band gap semiconductors.**

I. INTRODUCTION

MEDIUM-VOLTAGE (600–650 V breakdown voltage, V_{BR}) Gallium Nitride High-Electron-Mobility Transistors (GaN HEMTs) are an emerging technology with superior switching and thermal characteristics. They are optimal for high-frequency and harsh environment power converters [1] for applications requiring a DC-bus voltage (V_{DC}) in the 400 V range [2] and devices with low on-state resistance ($R_{DS(\mathrm{on})}$). Natively, GaN HEMTs are normally-on switches (Depletion-mode HEMTs, DHEMTs), which result critical for appliances with fail-safe requirements. In response to this, GaN cascodes and Enhancement-mode HEMTs (EHEMTs) have appeared as a normally-off solution [3], [4]. In this scenario, p-GaN and Metal–Insulator–Semiconductor HEMTs (MISHEMTs) are consolidating as the most promising commercially available EHEMTs. Besides, their electrical characteristics are as follows [4].

1) GaN cascodes offer a high threshold voltage ($V_{GS(\mathrm{th})}$) and low specific $R_{DS(\mathrm{on})}$ (on-state resistance per unit area) [3].
2) P-GaN HEMTs [4]–[8] feature lower $V_{GS(\mathrm{th})}$ and specific $R_{DS(\mathrm{on})}$ than GaN cascodes.
3) MISHEMTs [3] provide a higher $V_{GS(\mathrm{th})}$ than p-GaN with a similar specific $R_{DS(\mathrm{on})}$.

As an interesting niche market, 600–650 V HEMTs have a potential applicability for motor drives [5], [9], as working at higher frequencies, the converter weight, volume, cost, and losses can become radically reduced. In such an appliance, HEMTs must be capable of withstanding short-circuit (SC) events at V_{DC} values around 400 V, while providing sufficient time for the gate drive circuit actuation [10]. Among all SC conditions [11]–[13], the hard switch fault (SC type I or SC I) test is the most commonly used by power device manufacturers [12], despite being less demanding for the device than fault under load (SC type II) test. Under a SC I condition, the device under test (DUT) is gated on into a faulty event. Consequently, SC current flows through it while withstanding V_{DC}, eventually giving rise to its destruction in a certain time to failure (t_{SC}). For a given V_{DC}, this test aims at evaluating whether the SC time duration (t_{on}) is long enough to detect the SC condition with a controller or driver, and safely switch the device off without any converter electrical failure [10]. According to the available drivers, the fault detection time is conventionally estimated to be below 6 μs [2], but traditionally, a certain margin is left. For instance, in the case of Insulated-Gate Bipolar Transistors (IGBTs), it is conservatively set for 10 μs. However, current trends aim at achieving a remarkable reduction on the gate driver response time, e.g., 360–600 ns for silicon carbide (SiC)-based devices [14] or 200 ns for GaN HEMTs [15].

Unfortunately, only few works [2], [16]–[20] have analyzed the HEMTs SC capability, as summarized in Table I. This table also provides their driving voltages (V_G) and drain current (I_D) decrease experienced during SC (ΔI_D). In this case, ΔI_D is calculated as $1 - I_{D(t_{\mathrm{on}})}/I_{D(\mathrm{sat})}$, where $I_{D(\mathrm{sat})}$ is the saturation drain current peak and $I_{D(t_{\mathrm{on}})}$ is the value of I_D at t_{on}. In general, no SC capability for all tested GaN HEMTs is reported

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TABLE I
STATE-OF-THE-ART OF SC CAPABILITY

Device technology	$V_{\rm BR}$ (V)$-I_D$ (A)***	$V_{\rm DC}$ (V)	$t_{\rm on}\|\|t_{\rm SC}$ (µs)	ΔI_D (%)	V_G (V)
GaN EHEMT [20]	200–3	50^{*}	10	25	+4/0
		100	2	–	+4/0
GaN cascode [2]	600–20	150^{*}	10	39	+12/0
		200^{*}	10	–	+12/0
		$<280^{*/**}$	10	–	+12/0
GaN cascode [18]	600–5	400	7.8	–	N/A
	600–16	400	7.7	–	N/A
	600–30	400	7	46	N/A
GaN DHEMT [19]	650–N/A	250^{*}	10	40	0/–15
		300	4	–	0/–15
		350	0.9	–	0/–15
		400	<0.5	–	0/–15
		400	30	–	–1.5/–15
GaN cascode [16]	600–18	100^{*}	10	70	+10/0
		100	14	–	+10/0
		200	4	–	+10/0
		300	1.8	–	+10/0
GaN EHEMT [16]	600–16	100^{*}	10	33	+5/–3
		150	4.5	–	+5/–3
		150^{*}	4	–	+5/–3
		200^{*}	2	–	+5/–3
GaN EHEMT [17]	650–60	400^{*}	10	90	+5/0
		400	1.2	–	+5/0
		$400^{*/**}$	500	–	+5/0
	650–30	270^{**}	>800	–	+5/0
		270^{**}	>800	–	+5/0
	650–22	400	~0.2	–	+5/0
		400	~0.2	–	+5/0

*Nondestructive SC results/**only for few parts/***rated values.

when $t_{\rm on} = 10\,\mu$s and $V_{\rm DC} = 400$ V, due to a premature thermal failure [16], [17]. In [18], a 600 V non-commercial GaN cascode has withstood a SC event up to $t_{\rm SC} = 7\,\mu$s thanks to its improved design for better SC ruggedness at the cost of lowering its specific $R_{DS({\rm on})}$. In [19], a 650 V GaN DHEMT has passed a SC event with $t_{\rm on} = 30\,\mu$s thanks to its gate-source voltage (V_{GS}) bias close to $V_{GS({\rm th})}$. In this case, the failure was electrically driven (extremely high local electric field). Finally, in [17], few samples of 650 V EHEMTs have outstayed a SC event for $t_{\rm on}$ ranging from 200 to 500 µs, whereas most of the tested device population failed at $t_{\rm SC} < 1$ µs. Although far from being an avalanche rated technology, the results shown by the last EHEMTs generation open the possibility to commercialize GaN transistors with SC capability in a short term. Besides, the physics limiting the SC capability in cascodes and EHEMTs is not fully known. Thus, the comparison and deep understanding of SC performance between commercially available GaN power technologies is mandatory.

In this scenario, this work not only compares GaN cascode, p-GaN HEMT and MISHEMT devices in terms of their capability and electrical failure signature under SC I, but also comprehends their failure mechanism physics. To this end, this paper is organized as follows. The studied devices and SC test platform are presented in Section II. Next, Section III depicts the SC results for the GaN power devices. Afterward, Section IV analyzes SC behavior with technology computer-aided design (TCAD) physics-based simulations, and contrasts its destruction critical energies with other medium voltage power devices. Finally, Section V draws the conclusions.

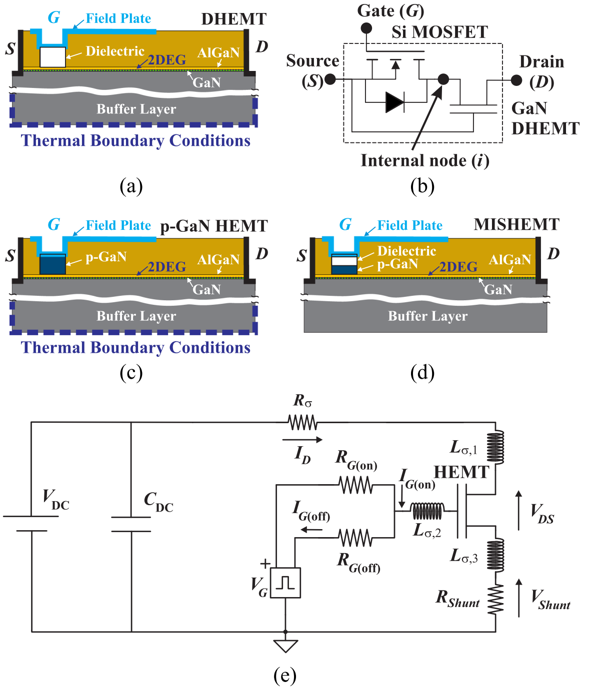


Fig. 1. (a) DHEMT structure, (b) GaN cascode schematic, (c) p-GaN structure, (d) MISHEMT structure, and (e) schematic of the designed test board. Thermal boundary conditions in simulated DHEMT and p-GaN structures are shown.

II. GAN POWER DEVICES AND SC TESTS DESCRIPTION

A. Tested Devices and Their Internal Structure

For the intended tests, several commercially available GaN cascodes and EHEMTs have been selected. As for GaN cascodes, two 600 V devices packaged in standard TO-220 [21] with different active areas, i.e., different nominal current and $R_{DS({\rm on})}$ values, have been studied. The smaller active area device is a 9 A and 290 mΩ switch (referred to as Cascode$_{\rm Small}$), whereas the larger features a 17 A and 150 mΩ (referred to as Cascode$_{\rm Large}$). For p-GaN case, the selected HEMTs are current collapse free 600 V devices with 10 A and 140 mΩ [22], and encapsulated in a dual flat no-lead 8 × 8 packaging [23]. With regards to MISHEMTs, two 650 V devices with different active areas, referred to as MISHEMT$_{\rm Small}$ (7.5 A and 220 mΩ) and MISHEMT$_{\rm Large}$ (15 A and 110 mΩ), and encapsulated with printed circuit board (PCB) embedded die packaging [24] are analyzed. The package influence [21], [23], [24] is restricted to the devices commutation instants due to all parasitic inductances (package and power circuit). Therefore, it does not thermally and electrically affect during $t_{\rm on}$, as it is short enough to confine the thermal phenomena in the die [25] and long enough to stabilize the device in a non-oscillatory on-state.

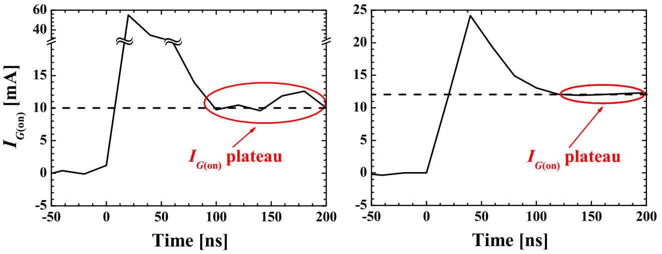
Such devices present the following internal structures. GaN cascodes are a dual-die solution, which packages together a low voltage silicon (Si) MOSFET with a GaN DHEMT. DHEMT structure of the studied cascode is depicted in Fig. 1(a), where the white box below the gate contact is a dielectric. At the aluminum GaN (AlGaN)/GaN heterojunction, a 2-D electron gas (2DEG) channel is permanently formed with a $V_{GS({\rm th})} < 0$ [4].

Consequently, electrons flow from the source to the drain contacts when $V_{GS} > V_{GS(\mathrm{th})}$ and $V_{DS} > 0$ are applied, which constitutes the main current conduction mechanism for all studied devices. According to Fig. 1(b), Si MOSFET acts as a buffer, which allows driving the DHEMT with a $V_{GS(\mathrm{th})} > 0$ at the cascode gate. Si MOSFETs drain terminal is connected to DHEMTs source (internal node, *i*), whereas *S* is wired to DHEMTs gate, so that the voltage drop between nodes *i* and *S* determines the gate-source voltage at the DHEMT $(V_{GS,\mathrm{GaN}})$. Node *i* is floating and not externally accessible, thus being susceptible to generate issues during the driving [26], [27]. Oppositely, p-GaN HEMTs and MISHEMTs are single-die solutions. In p-GaN devices, normally-off operation is provided by depositing on top of an AlGaN/GaN heterostructure a p-doped GaN layer [Fig. 1(c) with p-GaN gate], implementing a diode-like gate [6], [22]. This depletes the 2DEG channel beneath the gate contact [28] and shifts its $V_{GS(\mathrm{th})}$ positively. Similarly, the studied MISHEMTs also have such a p-GaN gate, but incorporate an ultra-thin dielectric layer (<10 nm) between the metal and p-GaN layers [Fig. 1(d) with p-GaN gate and dielectric]. The dielectric layer insulates this terminal, simplifies the device voltage driving, and limits the gate current when V_{GS} is positive.

B. SC Tests Platform and Driving Conditions

Fig. 1(e) depicts the electrical schematic of the designed test platform used for SC I tests [29], [30] (i.e., hard switch fault condition), also indicating the main parasitic resistance R_σ and inductances ($L_{\sigma,1}$, $L_{\sigma,2}$, and $L_{\sigma,3}$) resulting from the power circuit and packaging. It is composed by a DC power supply at V_{DC}, a capacitors bank (C_{DC}), a gate driver, and the DUT. The gate driving is carried out in two separated branches with different gate resistors ($R_{G(\mathrm{on})}$ and $R_{G(\mathrm{off})}$) for turning the DUT on and off. A 10 mΩ coaxial shunt (R_{Shunt}) senses I_D (V_{Shunt}), whereas two differential voltage probes measure V_{GS}, gate current at $R_{G(\mathrm{on})}$ $(I_{G(\mathrm{on})})$, and drain-source voltage (V_{DS}) in the DUT. To carry out the tests, p-GaN and MISHEMT switches are soldered to a small PCB board with optimized stray elements. The driving conditions (i.e., V_{GS}) depend on the device, and customizable $R_{G(\mathrm{on})}$ and $R_{G(\mathrm{off})}$. Ambient temperature is set for 23 °C. In a first experiment, SC tests are run for each power device changing the V_{DC} voltage, while keeping t_{on} at 10 µs. They start from $V_{\mathrm{DC}} = 50$ V and V_{DC} is increased in steps of 50 V until the device destruction. In a second experiment, GaN cascodes, p-GaN HEMTs and GaN MISHEMTs are repeatedly subjected every 60 s to SC tests at the same V_{DC} without cumulative self-heating, considering V_{DC} at 50, 100, and 250 V, as long as they have not failed during the test. After ten cyclical tests at each V_{DC}, all measured curves (V_{GS}, $I_{G(\mathrm{on})}$, V_{DS}, and I_D) remained unaltered, indicating no-structural degradation.

As for the devices driving, the following conditions have been accounted for making possible their comparison. Some devices have been tested using high values for $R_{G(\mathrm{on})}$ and $R_{G(\mathrm{off})}$. Despite such values are unusual for applications where the energy losses have to be minimized, they are realistic in other scenarios where low dI_D/dt and low dV_{GS}/dt are required. For instance, they could be suitable for converters requiring high EMC levels [31] or half-bridge topologies where a dual-channel driver does not withstand $dV_{GS}/\mathrm{dt} > 50$ V/ns [32]. From an experimental point of view, large $R_{G(\mathrm{on})}$ and $R_{G(\mathrm{off})}$ values allow carrying out several actions. In general, they avoid oscillations due to $L_{\sigma,2}$ and $L_{\sigma,3}$. Note that this does not affect the SC test results, as they aim at subjecting the devices to stable and high I_D and V_{DS} levels, simultaneously. In EHEMTs, high $R_{G(\mathrm{on})}$ and $R_{G(\mathrm{off})}$ values also allow setting similar V_{GS} levels and $I_{G(\mathrm{on})}$ plateau values (as highlighted in Fig. 2), which make it possible to compare their SC results for an in-depth analysis. In GaN cascodes, this approach delays the GaN DHEMT switching without affecting their dI_D/dt, though the Si MOSFET response is slowed down. As a result, oscillatory behaviors or eventual accidental turn-on/off processes are also successfully avoided. Taking all this into account, the gate in cascodes is controlled considering $V_G = -12\,\mathrm{V}/+12\,\mathrm{V}$ and $V_G = 0\,\mathrm{V}/+12\,\mathrm{V}$, with $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$. P-GaN HEMTs are driven at $I_{G(\mathrm{on})} = 10$ mA as recommended by the manufacturer, which typically corresponds to $V_{GS} = 3.5$ V. This is ensured with $V_G = -3\,\mathrm{V} + 4\,\mathrm{V}$ and $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 50\,\Omega$. Finally, MISHEMTs are switched with $V_G = -3\,\mathrm{V}/+5\,\mathrm{V}$ and $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$. The used negative gate bias for all GaN devices grants safe operation against voltage spikes over $V_{GS(\mathrm{th})}$. As long as the device is capable of switching off without experiencing any accidental turn-on, the SC performance will be the same for both cases.



(a) (b)

Fig. 2. $I_{G(\mathrm{on})}$ waveforms for nondestructive SC at $V_{\mathrm{DC}} = 200$ V of (a) p-GaN HEMT and (b) GaN MISHEMT.

III. SC TEST RESULTS

A. Nondestructive SC Results

1) GaN Cascodes: Fig. 3 compares measured V_{GS}, $I_{G(\mathrm{on})}$, V_{DS}, and I_D waveforms between $\mathrm{Cascode}_{\mathrm{Small}}$ (in black line) and $\mathrm{Cascode}_{\mathrm{Large}}$ (in red line) for a SC event at $V_{\mathrm{DC}} = 100$ V. Similar $I_{G(\mathrm{on})}$ dynamics is exhibited in both devices, with slight differences in V_{GS}, I_D, and V_{DS}. The identical waveforms observed for $I_{G(\mathrm{on})}$ correspond to that of a typical MOSFET with a large $R_{G(\mathrm{on})}$. This similarity is already expected due to their equal small-signal gate input capacitance (C_{iss}). $I_{G(\mathrm{on})}$ evolves showing an initial current peak that charges C_{iss}, and, afterwards, slowly dropping to zero once C_{iss} is fully charged. In comparison with $\mathrm{Cascode}_{\mathrm{Small}}$, $\mathrm{Cascode}_{\mathrm{Large}}$ has a higher I_D, because of its lower $R_{DS(\mathrm{on})}$. In its turn, the larger dI_D/dt in $\mathrm{Cascode}_{\mathrm{Large}}$ induces a more

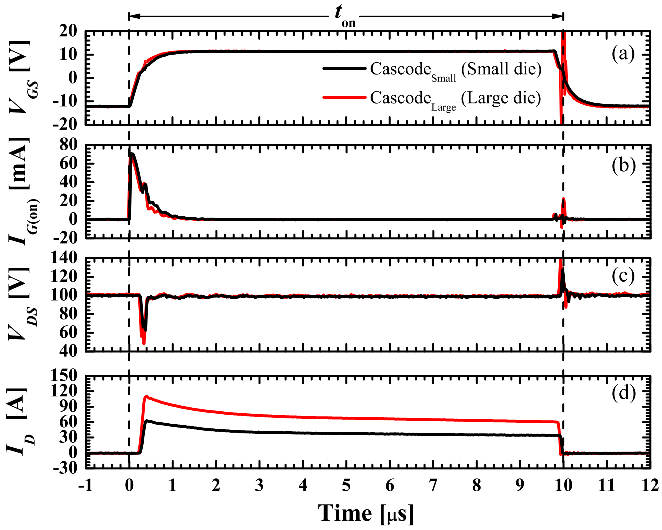


Fig. 3. Cascode$_{\mathrm{Small}}$ (black line) and Cascode$_{\mathrm{Large}}$ (red line) nondestructive SC results for $V_{\mathrm{DC}} = 100\,\mathrm{V}$, $V_G = -12/+12\,\mathrm{V}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

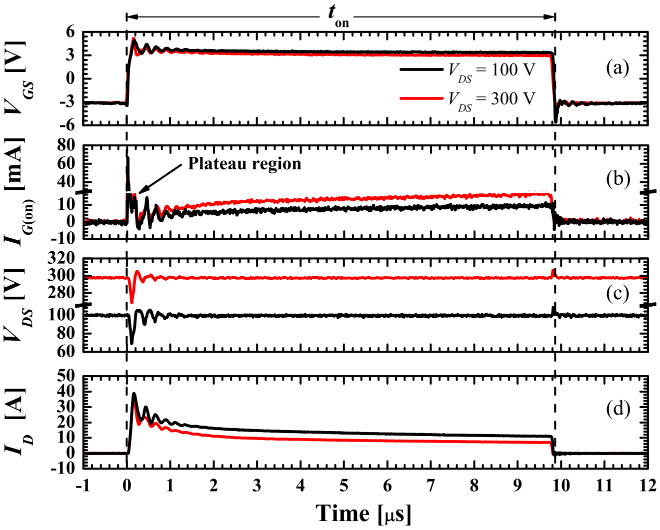


Fig. 5. P-GaN HEMT nondestructive SC results for $V_{\mathrm{DC}} = 100\,\mathrm{V}$ (black line) and 300 V (red line), $I_{G(\mathrm{on})} = 10\,\mathrm{mA}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 50\,\Omega$: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

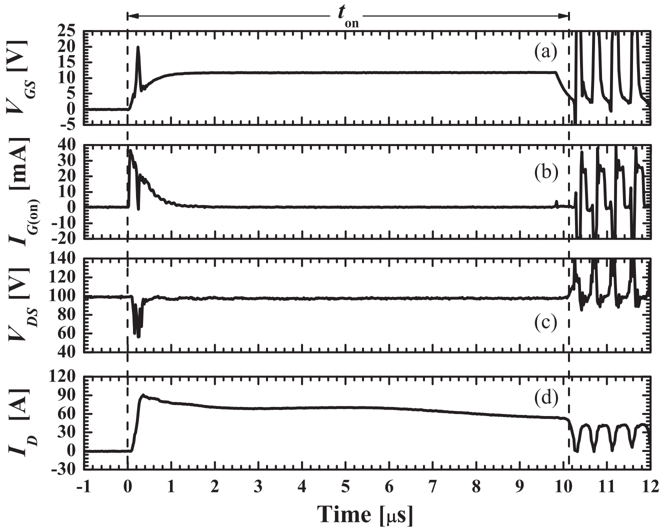


Fig. 4. Cascode$_{\mathrm{Large}}$ nondestructive SC results for $V_{\mathrm{DC}} = 100\,\mathrm{V}$, $V_G = 0/+12\,\mathrm{V}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

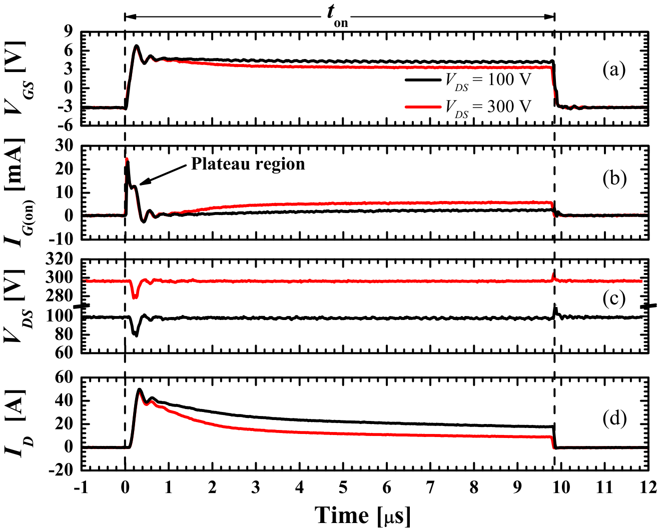


Fig. 6. GaN MISHEMT$_{\mathrm{Large}}$ nondestructive SC results for $V_{\mathrm{DC}} = 100\,\mathrm{V}$ (black line) and 300 V (red line), $V_G = -3/+5\,\mathrm{V}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

prominent V_{DS} notch due to a higher voltage drops in $L_{\sigma,1}$. Besides, Cascode$_{\mathrm{Large}}$ has a slightly lower ΔI_D (45.59%) than Cascode$_{\mathrm{Small}}$ (46.03%).

As for V_{GS} waveforms, in spite that both transistors are driven at similar voltage levels, Cascode$_{\mathrm{Large}}$ presents a noisier turn-off. To gain insight into the origin of these oscillations, Cascode$_{\mathrm{Large}}$ is driven at $V_G = 0\,\mathrm{V}/+12\,\mathrm{V}$. The results obtained under these conditions are depicted in Fig. 4. V_{GS}, $I_{G(\mathrm{on})}$, V_{DS}, and I_D waveforms present a significant oscillation after the device turn-off, while V_{GS} also shows a significant ringing at the device turn-on. The former could be caused by $L_{\sigma,2}$ and $L_{\sigma,3}$ [33], as discussed in Section IV. A. With regards to V_{GS} ringing at Cascode$_{\mathrm{Large}}$ turn-on [see Fig. 4(a)], it is originated by $L_{\sigma,3}$, due mainly to the packaging contribution [27]. Consequently, the driving loop of the final application must be carefully designed to damp down these oscillations, which could increase the switching losses and restrain the device performance [34].

2) P-GaN HEMTs and MISHEMTs: The SC performance of p-GaN HEMTs and MISHEMTs at different values of V_{DC} leads to anomalous behaviors in $I_{G(\mathrm{on})}$ and I_D, as Figs. 5 and 6 demonstrate. Fig. 5 presents for p-GaN case, the V_{GS}, $I_{G(\mathrm{on})}$, V_{DS} and I_D measured waveforms for SC tests at $V_{\mathrm{DC}} = 100\,\mathrm{V}$ (in black line) and $V_{\mathrm{DC}} = 300\,\mathrm{V}$ (in red line). As shown in Fig. 5(b), $I_{G(\mathrm{on})}$ evolves as follows: achieves a peak (C_{iss} charge for 2DEG channel enhancement), decreases to a plateau (channel maintenance current), and after saturation at $I_{D(\mathrm{sat})}$, reaches negative values to increase up to some

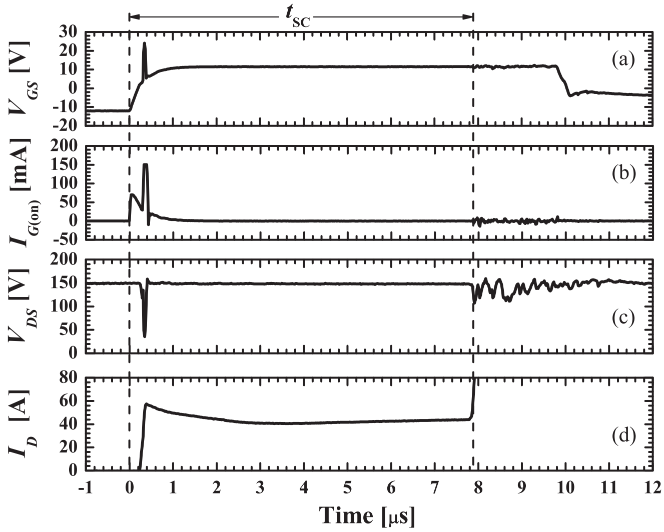


Fig. 7. Cascode$_{\mathrm{Small}}$ destructive SC results for $V_{\mathrm{DC}} = 150\,\mathrm{V}$, $V_G = -12/+12\,\mathrm{V}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$: (a) V_{GS} (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

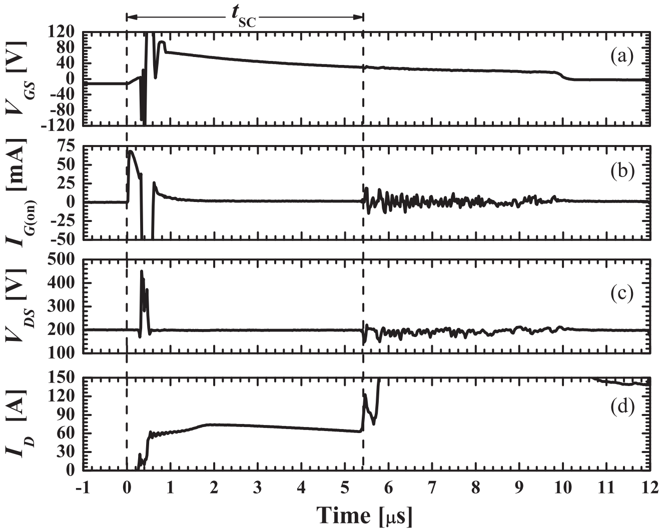


Fig. 8. Cascode$_{\mathrm{Large}}$ destructive SC results for $V_{\mathrm{DC}} = 200\,\mathrm{V}$, $V_G = -12/+12\,\mathrm{V}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

tens of mA depending on V_{DS} value. As the device is voltage controlled, the mentioned variations in $I_{G(\mathrm{on})}$ modify the voltage drop at $R_{G(\mathrm{on})}$, inducing the observed V_{GS} reduction [see Fig. 5(a)]. On the other hand, I_D decreases after reaching its saturation value $I_{D(\mathrm{sat})}$ [see Fig. 5(d)], achieving a larger ΔI_D than that for the cascode case. This trend assists the EHEMTs to be more rugged against SC events, entailing that when the device has been capable of undergoing the first 2–3 µs in SC, then it will likely pass the test. As for MISHEMT$_{\mathrm{Large}}$ case, Fig. 6 plots the V_{GS}, $I_{G(\mathrm{on})}$, V_{DS}, and I_D measured waveforms for a SC test at $V_{\mathrm{DC}} = 100\,\mathrm{V}$ (in black line) and $V_{\mathrm{DC}} = 300\,\mathrm{V}$ (in red line). In general, Fig. 6(b) and (c) portrays the same $I_{G(\mathrm{on})}$ and I_D time evolution than that reported by Fig. 5(b) and (d), also observing a similar ΔI_D. Furthermore, the extracted waveforms for MISHEMTs are quite smoother owing to their lower packaging parasitic inductance [24].

As for the chip area analysis in MISHEMT devices, nondestructive results point to the same conclusions drawn for GaN cascodes in terms of $R_{DS(\mathrm{on})}$, I_D and V_{DS} notch.

B. Destructive SC Results

Figs. 7–10 depict the V_{GS}, $I_{G(\mathrm{on})}$, V_{DS}, and I_D waveforms measured during SC tests performed with Cascode$_{\mathrm{Small}}$, Cascode$_{\mathrm{Large}}$, p-GaN, and MISHEMT$_{\mathrm{Large}}$, respectively. For all cases, the high power dissipation ended up with the device destruction after a certain time to failure t_{SC} ($t_{\mathrm{SC}} \leq t_{\mathrm{on}}$). After few µs, Cascode$_{\mathrm{Small}}$ and Cascode$_{\mathrm{Large}}$ reach destruction in the DHEMT at $V_{\mathrm{DC}} = 150\,\mathrm{V}$ (see Fig. 7) and $V_{\mathrm{DC}} = 200\,\mathrm{V}$ (see Fig. 8), respectively. This is due to the fact that the DHEMT of the Cascode$_{\mathrm{Large}}$ has a larger active area and it presents for the same I_D value, a lower power density than that of Cascode$_{\mathrm{Small}}$. This makes possible to withstand the SC event at a higher V_{DC} value. In the p-GaN case, the destruction is achieved at $V_{\mathrm{DC}} = 400\,\mathrm{V}$ (see Fig. 9) after 400 ns. The waveforms preceding the failure present similar behaviors to those at $V_{\mathrm{DC}} = 350\,\mathrm{V}$. Finally, MISHEMT$_{\mathrm{Large}}$ fails at $V_{\mathrm{DC}} = 350\,\mathrm{V}$ (see Fig. 10) after 700 ns. Likewise, the MISHEMT$_{\mathrm{Large}}$ waveforms before the failure are identical to those at $V_{\mathrm{DC}} = 300\,\mathrm{V}$. At the failure instant, all analyzed devices have the same electrical failure signature: I_D abruptly increases with a null (cascodes) or low (EHEMTs) $I_{G(\mathrm{on})}$ leakage, which is indicative of a thermal destruction. This occurs because of reaching a critical temperature at which the semiconductor becomes intrinsic, due to intrinsic carrier concentration dependence on temperature. However, despite the electrical signatures are similar for all devices, dissimilar mechanisms precede destruction. Thus, the study of the differences observed among devices in terms of their electrical (ΔI_D) and thermal (temperature, dissipated energies) behaviors is deepened in Section IV.

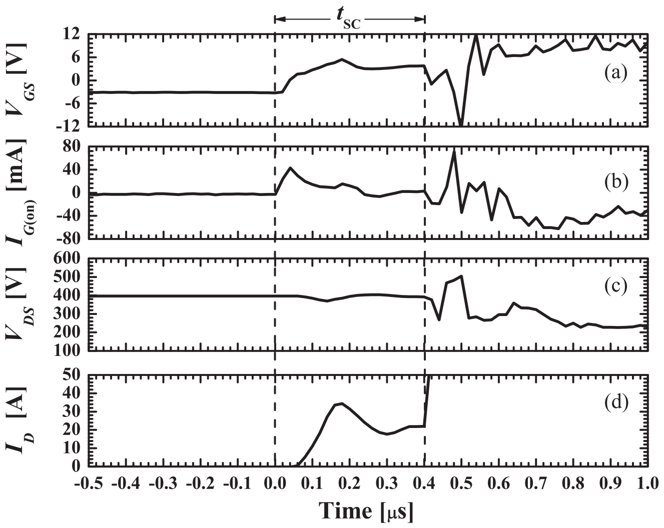


Fig. 9. P-GaN HEMT destructive SC results for $V_{\mathrm{DC}} = 400\,\mathrm{V}$, $I_{G(\mathrm{on})} = 10\,\mathrm{mA}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 50\,\Omega$: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

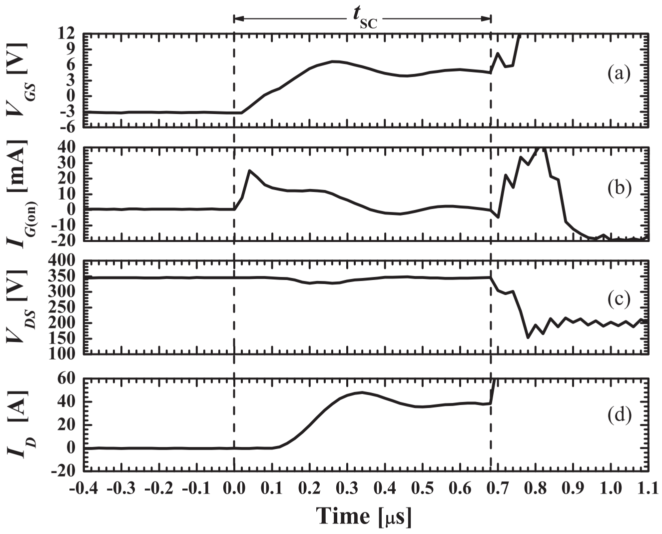


Fig. 10. MISHEMT$_{\mathrm{Large}}$ destructive SC results for $V_{\mathrm{DC}} = 350\,\mathrm{V}$, $V_G = -3/+5\,\mathrm{V}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, (c) V_{DS}, and (d) I_D.

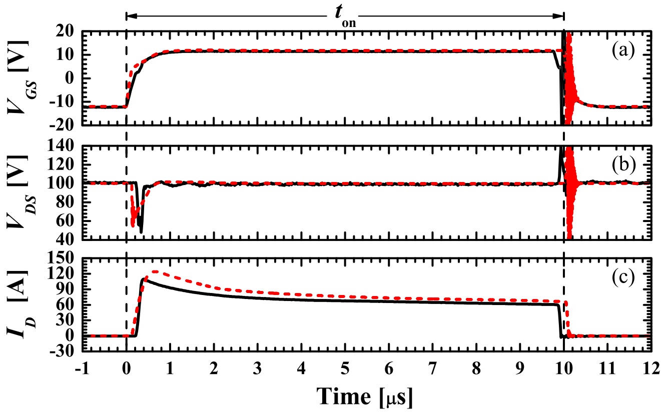


Fig. 11. Cascode$_{\mathrm{Large}}$ nondestructive SC results experimental (black solid line) and simulated (red dashed line) waveforms for $V_{\mathrm{DC}} = 100$ V, $V_G = -12/+12$ V, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\ \Omega$: (a) V_{GS}, (b) V_{DS}, and (c) I_D.

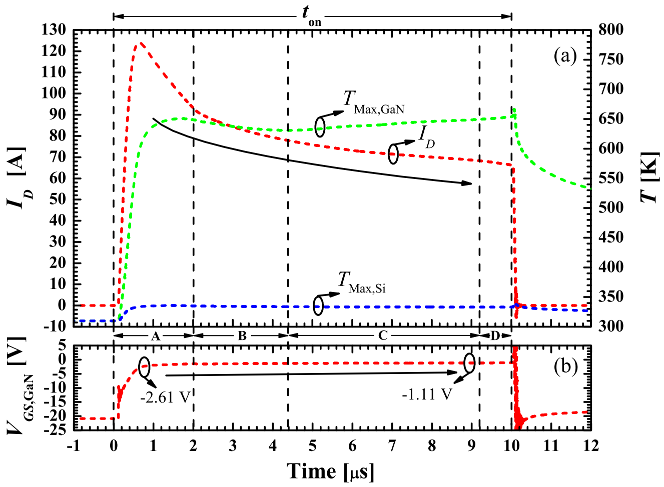


Fig. 12. Cascode$_{\mathrm{Small}}$ non-destructive SC results simulated waveforms for $V_{\mathrm{DC}} = 100\,\mathrm{V}$, $V_G = -12/+12\,\mathrm{V}$, $R_{G(\mathrm{on})} = R_{G(\mathrm{off})} = 270\,\Omega$: (a) I_D (red line), $T_{\mathrm{Max,GaN}}$ (green line) and $T_{\mathrm{Max,Si}}$ (blue line) and (b) $V_{GS,\mathrm{GaN}}$.

IV. SC BEHAVIORAL ANALYSIS AND DISCUSSION

A. GaN Cascodes Turn-off Oscillations and ΔI_{D}

Seeking to explain the issues related to cascode results, generic finite-element structures were set in mixed-mode simulation with TCAD software [35], for both Si MOSFET and GaN DHEMT. This allows gaining qualitative insight into the measured oscillatory phenomena at V_{GS} during turn-off when $V_G = -12\,\mathrm{V}/+12\,\mathrm{V}$ and observed ΔI_D. First, Si MOSFET and GaN DHEMT structures were resized to show similar $R_{DS(\mathrm{on})}$ and small-signal parasitic capacitances (C_{iss}, reverse transfer C_{rss} and output C_{oss}). Besides, more internal parasitic elements were considered as carried out in [36]. The physical models referring to the thermal dependence of electron mobility in the 2DEG channel (μ (T)) were calibrated to qualitatively reproduce the experimental observations in $I_{D(\mathrm{sat})}$ and I_D decay by means of its thermal dependence. As for thermal boundary conditions, a non-adiabatic wall with a thermal series resistance accounting for the substrate thermal contribution is prescribed at the bottom of the DHEMT buffer layer, as indicated in Fig. 1(a).

As for cascodes oscillatory phenomena at turn-off, an accurate definition of the common source inductance ($L_{\sigma,3}$) is crucial to reproduce V_{GS}. Fig. 11 depicts the good agreement between experimental and simulated waveforms corresponding to a SC event in Cascode$_{\mathrm{Large}}$ at $V_{\mathrm{DC}} = 100\,\mathrm{V}$ and $V_G = -12\,\mathrm{V}/+12\,\mathrm{V}$. Conversely, when $V_G = 0\,\mathrm{V}/+12\,\mathrm{V}$ is considered in Cascode$_{\mathrm{Large}}$, the measured V_{DS} ringing after turn-off is strongly impacted by large $L_{\sigma,2}$ and $L_{\sigma,3}$ [33]. This influence is not observed when driven at $V_G = -12\,\mathrm{V}/+12\,\mathrm{V}$, as the device successfully switches off, even after experiencing a strong V_{DS} overshoot. In this respect, driving the device to negative V_G assists to overcome this issue.

With regards to ΔI_D, its main cause is the device self-heating. This hypothesis is supported in Fig. 12 by simulation results of a SC event at $V_{\mathrm{DC}} = 100\,\mathrm{V}$. Fig. 12(a) depicts the waveforms of I_D (red dashed line), the DHEMT maximum temperature ($T_{\mathrm{Max,GaN}}$, green dashed line), the Si MOSFET maximum temperature ($T_{\mathrm{Max,Si}}$, blue dashed line), whereas Fig. 12(b) shows the $V_{GS,\mathrm{GaN}}$ waveform (red dashed line). Additionally, this figure identifies several time intervals named as A, B, C, and D.

In the course of regime A and once $I_{D(\mathrm{sat})}$ is reached, I_D decreases with a specific slope as $T_{\mathrm{Max,GaN}}$ continues increasing. However, from the beginning of regime B, device dissipation mechanisms lead the heat to diffuse along the upper AlGaN/GaN layers until reaching the metallic contacts of the die back-end. This improves the heat extraction and reduces $T_{\mathrm{Max,GaN}}$, which modifies I_D slope. As the temperature at the contacts (die metallization back-end) increase, the efficiency of this extraction worsens, resulting into a new $T_{\mathrm{Max,GaN}}$ rising and the modification observed in the I_D slope during regime C. Finally, during regime D, the I_D slope follows the last steep $T_{\mathrm{Max,GaN}}$ increase.

TABLE II
SC TESTS SUMMARY

Tested devices	$R_{DS(\text{on})}$ (mΩ)	V_{DC} (V)	$I_{D(\text{sat})}$ (A)	ΔI_D (%)	V_G (V)	t_{SC} (μs)||V_{DC} (V)
GaN-Vendor 1:						
Cascode$_{\text{Small}}$	290	100	63	46	–12/+12	7.80||15
Cascode$_{\text{Large}}$	150	150	90	62	–12/+12	5.38||20
GaN-Vendor 2:						
p-GaN HEMT	140	350	35	82	–3/+4	0.40||400
GaN-Vendor 3:						
MISHEMT$_{\text{Small}}$	220	150	31	71	–3/+5	0.68||35
MISHEMT$_{\text{Large}}$	110	300	48	82	–3/+5	01.12||200

In comparison with EHEMTs, the I_D time evolution observed in cascodes differs. Concretely, cascodes experience a lower ΔI_D (see Table II), which justifies their lesser ruggedness against SC. Therefore, the self-regulating effect in EHEMTs consisting in decreasing the power dissipation during SC is less prominent in cascodes. This distinct behavior can be explained by cascodes internal structure. As shown in Fig. 1(b), GaN cascodes have their control stage (low voltage Si MOSFET) electrothermally decoupled from their power stage (GaN DHEMT). Then, $V_{GS,\text{GaN}}$ and I_D in GaN cascodes are correlated through the Si MOSFET on-state resistance ($R_{DS(\text{on,Si})}$) by the following equation [18]:

$$V_{GS,\text{GaN}} = -R_{DS(\text{on,Si})} \cdot I_D \tag{1}$$

and under SC conditions (saturation regime), the I_D thermal dependence is proportional to the product $\mu(T)\,(|V_{GS(\text{th})}| - |V_{GS,\text{GaN}}|)$ at the DHEMT [18]. As shown in Fig. 12(a), temperature mainly rises at the GaN DHEMT during the SC event, practically not affecting $R_{DS(\text{on,Si})}$ [18], though it can be corrected by design. Therefore, once I_D starts decreasing after reaching $I_{D(\text{sat})}$ due to DHEMT self-heating, $|V_{GS,\text{GaN}}|$ decreases and further enhances DHEMT channel. As a result, ΔI_D should lower. However, the $|V_{GS(\text{th})}|$ reduction with temperature should counteract the previous effect [18], increasing ΔI_D. According to simulation results, the former could not be relevant, as DHEMT $|V_{GS(\text{th})}|$ is fairly higher than –3 V [see Fig. 12(b)]. By contrast, $|V_{GS(\text{th})}|$ reduction is not predominant, as supported by the experimental results. Therefore, $|V_{GS,\text{GaN}}|$ must present a stronger thermal dependence than $|V_{GS(\text{th})}|$ to increase the $(|V_{GS(\text{th})}| - |V_{GS,\text{GaN}}|)$ term. Actually, $|V_{GS,\text{GaN}}|$ decreases at a similar rate than $\mu(T)$ with temperature according to (1), inducing a positive feedback.

B. P-GaN HEMTs Temperature Distribution During SC

To better comprehend the role of 2DEG channel in the SC ruggedness, the EHEMT temperature (T) and electric field profile along the 2DEG channel are analyzed using TCAD physics-based simulations [35]. In particular, as p-GaN and MISHEMT devices have a similar internal structure, only a p-GaN HEMT is analyzed. A 2-D finite-element structure [37] is used to understand the SC tests. The cross section depicted in Fig. 1(c) is simulated setting the default physical models parameters of drift-diffusion and thermodynamic models [35], without considering the test bench and packaging parasitics. As for thermal boundary conditions, a non-adiabatic wall with a thermal series resistance accounting for the substrate thermal contribution has been defined at the bottom of the buffer layer as indicated in Fig. 1(c). The DUT and TCAD structure show identical $R_{DS(\text{on})}$ and $V_{GS(\text{th})}$ ($\sim$ 1.2 V) by setting the gate length for 75 mm, whereas $V_{\text{BR}} > 600$ V is ensured for a drift length of 10 μm. The thermal resistance of the buffer layer boundary condition is set to reproduce the destruction at $V_{\text{DC}} = 400$ V.

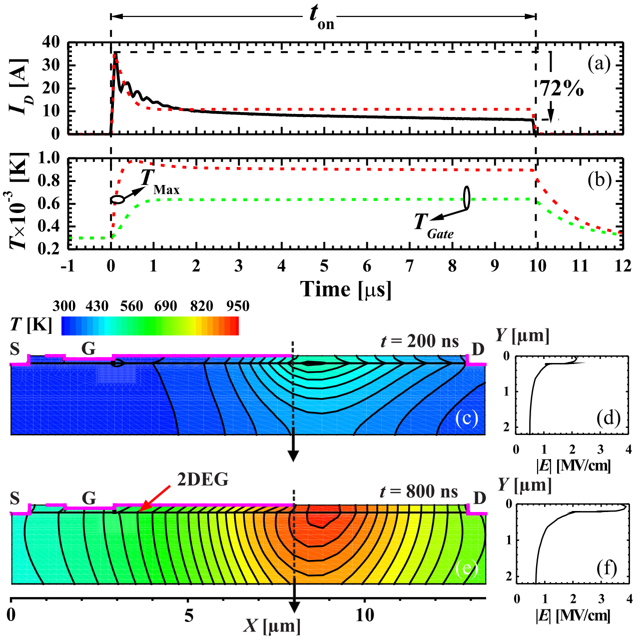


Fig. 13. Measured (black solid line) and simulated (red and green dashed lines) waveforms for (a) I_D, (b) simulated T_{Gate} (green) and T_{Max} (red), and temperature distribution in the p-GaN HEMT channel after (c) 200 ns and (e) 800 ns, with (d)–(f) absolute electric field (|E|) vertical profile (on the right) (black line) in a SC event for $V_{\text{DC}} = 350$ V (nondestructive).

In this regard, Fig. 13(a) and (b) represents the good agreement between the measured and simulated I_D waveforms and the time evolution of simulated gate (T_{Gate}) and maximum temperatures (T_{Max}). Moreover, the temperature distribution and absolute electric field (|E|) vertical profile at the field plate right edge [see Fig. 1(c)] are extracted at different times: $t = 200$ ns when $I_{D(\text{sat})}$ is reached [see Fig. 13(c) and (d)] and $t = 800$ ns when I_D already stabilized [see Fig. 13(e) and (f)]. In Fig. 13(c) and (e), the field plate (gate contact metallization) right edge is also indicated with a dashed line through the structures, pointing out the cut location. At $t = 200$ ns, a large $|E|$ is located at the 2DEG channel, just beneath the edge of the field plate. However, the maximum temperature is not reached until $t = 800$ ns, for when I_D has already experienced a severe reduction according to experimental results. In fact, the field plate fixes $|E|$ spatial distribution, presenting its maximum in the 2DEG channel below the field plate right edge. Then, at this location, a high power density spot appears due to Joule effect. In this time interval, the heat generated there flows to the surrounding areas entailing an increase of T_{Gate}. Since $I_{G(\text{on})}$ increases with T_{Gate} [8], [20], [38], this provokes a decrease of V_{GS}

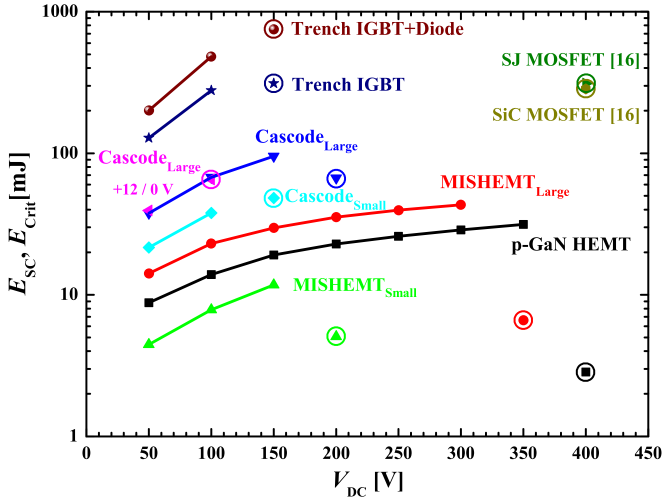


Fig. 14. Dissipated and critical energies comparison with V_{DC} for p-GaN (black line, ■), MISHEMT$_{\text{Large}}$ (red line, ●), MISHEMT$_{\text{Small}}$ (green line, ▲), Cascode$_{\text{Large}}$ (blue line, ▼), Cascode$_{\text{Large}}$ for $V_G = +12/0$ V (◀), Cascode$_{\text{Small}}$ (cyan line, ◆), SJ MOSFET (▶), SiC MOSFET (⬢), Trench IGBT without diode (navy line, ★), Trench IGBT with diode (wine line, ●).

owing to a higher voltage drop at $R_{G(\text{on})}$. However, the reduction of μ (T) due to thermal effects is the main responsible for ΔI_D, as in view of simulation results, $I_{G(\text{on})}$ level is not high enough to induce a V_{GS} decrease to explain the measured ΔI_D values. Therefore, both effects contribute to the 2DEG conductance modulation and results into a larger ΔI_D than for GaN cascodes (82% in experiments for $V_{\text{DC}} = 350$ V). In addition, as the gate electrothermally behaves like a pn-junction [6], $V_{GS(\text{th})}$ also decreases with T_{Gate} [8]. All these phenomena can be also extrapolated to the studied MISHEMTs, which present very thin dielectric layers in their structure in contrast to p-GaN HEMTs [see Fig. 1(c) and (d)]. Under SC conditions, the MISHEMTs $I_{G(\text{on})}$ also rises to the milliamp range due to this thermal behavior combined with dielectric tunneling effects. In conclusion, a SC event with identical electrical conditions is less harsh in EHEMTs than in GaN cascodes thanks to the electrothermal self-regulation.

C. Dissipated and Breakdown Critical Energies

The dependence of SC dissipated (E_{SC}) and breakdown critical (E_{Crit}) energies on V_{DC} during tests are studied and qualitatively compared with other power semiconductor technologies rated for 400 V applications ($V_{\text{BR}} \sim 600$ V), i.e.: super junction (SJ) MOSFET, SiC MOSFET (both from [16]), Trench IGBT and Trench IGBT copackaged with a diode (both measured). E_{SC} and E_{Crit} relate with V_{DS} and I_D as follows:

$$E_{\text{SC}} = \int_0^{t_{\text{on}}} V_{DS} \cdot I_D \tag{2}$$

$$E_{\text{Crit}} = \int_0^{t_{\text{SC}}} V_{DS} \cdot I_D. \tag{3}$$

Fig. 14 summarizes E_{SC} (in lines) and E_{Crit} (circled dots) in function of V_{DC} for all stated technologies. It can be observed that SJ and SiC MOSFETs present extremely high E_{Crit} at $V_{\text{DC}} = 400$ V. These values are far above than those for GaN and allow SJ and SiC MOSFETs to pass SC I tests at $V_{\text{DC}} = 400$ V. Besides, it can be observed for the rest of devices that E_{SC} monotonically increases with V_{DC}. At device failure, E_{Crit} is significantly lower than the expected value for E_{SC} trend, as also observed in [16]. This indicates that the failure occurs for $t_{\text{SC}} < t_{\text{on}}$. Depending on the device and t_{SC} duration at a given V_{DC} (see Table II), this could be pointing to a local failure mechanism driven by current crowding phenomena. As a result, a local thermal destruction occurs. This is the main difference between thermal destruction in cascodes and EHEMTs, where the former presents a longer t_{SC} at a lower V_{DC}. According to simulation results, the shorter t_{SC} at a higher V_{DC} of EHEMTs (< 1 µs) leads to expect such local effects: higher local electric field in the 2DEG channel below the field plate right edge. Furthermore, EHEMTs show a much better SC capability than the rest of failed devices thanks to their ΔI_D, which lowers their dissipated power and thus protects them against destruction at higher V_{DC} values.

D. Discussion: Benefits and Drawbacks of Each Device

Resulting from this study, several conclusions can be drawn about GaN cascodes and EHEMTs suitability for motor drives. The main problems of the available GaN cascodes are related to its packaging, which, in combination with control and power loop inductances, is responsible for the observed gate ringing. Under a SC event in a real application, this ringing could lead to the device destruction or converter failure, even after withstanding such an electrical stress. In this regard, gate bipolar control and reducing loop inductances could assist to improve cascodes SC ruggedness. Moreover, the low thermal self-regulation on their gate control makes them less rugged than EHEMTs to SC events. However, GaN cascodes present an inherent pn-junction structure at the Si MOSFET, which can be used as a free-wheeling diode with a significantly lower forward voltage (integral diode + DHEMT) drop than EHEMTs. This is of interest for synchronous rectification, e.g., power inverters for motor driving. As another benefit, GaN cascodes can be controlled using traditional V_G values.

On the other hand, EHEMTs have the main drawback of overheating under operating conditions, which decrease the $\mu(T)$ and degrades $R_{DS(\text{on})}$. Fortunately, this thermal behavior is beneficial for their SC ruggedness, as a self-regulation process on I_D takes place.

V. CONCLUSION

This paper presented the SC behavior of medium-voltage GaN cascodes, p-GaN HEMTs, and MISHEMTs, and provided a comprehensive analysis of their different performances in terms of ΔI_D, temperature distribution, and E_{SC}. This has been achieved by contrasting experimental results with physics-based simulations. Experimental results revealed that none of the studied devices were capable of withstanding a SC I event at $V_{\text{DC}} = 400$ V during $t_{\text{on}} = 10$ µs. GaN cascodes did not pass the tests for $V_{\text{DC}} > 150$ V, while EHEMTs have demonstrated to endure a SC I test at $V_{\text{DC}} = 300$ V (MISHEMTs) and $V_{\mathrm{DC}} = 350\,\mathrm{V}$ (p-GaN HEMTs). In addition, it has been determined that the higher ΔI_D of EHEMTs is caused by the thermal behavior of their channel. By contrast, the cascodes behavior results from their different structure, driving and thermal characteristics.

As for SC failure, an abrupt I_D rise with a null or low $I_{G(\mathrm{on})}$ leakage for cascodes and EHEMTs outlines a purely thermal destruction. All devices fail during the SC event (i.e., $t_{\mathrm{SC}} < t_{\mathrm{on}}$) and E_{Crit} is similar (cascodes) or much lower (EHEMTs) than the trend followed by E_{SC} when increasing V_{DC}. In comparison to other technologies, SJ and SiC MOSFETs present the best SC capability. This is mainly due to the low maturity of GaN devices and the lack of knowledge on their behavior under SC conditions.

In this scenario, two main findings useful for SC protection strategies are provided. Protection circuits require at least a 300 ns response to safely switch the analyzed EHEMTs and GaN cascodes off. On the other hand, $I_{G(\mathrm{on})}$ monitoring under operation by means of a smart gate driver could be a good state indicator for SC prevention in EHEMTs. Besides, using $V_G < 0$ ensures safe commutation against voltage spikes and avoids accidental turn-off/on, though this increases power loss during dead times in synchronous operation (third quadrant operation).

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Short-Circuit Capability in p-GaN HEMTs and GaN MISHEMTs

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***Abstract*—Gallium Nitride (GaN) Enhancement-mode High-Electron-Mobility Transistors (EHEMTs) are promising devices for motor drives. Hence, ensuring and gaining insight into their ruggedness against Short-Circuit (SC) faults become essential. Thus, SC stresses (types I and II) are studied for the first time in commercial EHEMTs with similar on-state resistance (~ 100 mΩ) and breakdown voltage (~ 600 V). As SC failure mechanisms, thermal (SC I) and dielectric (SC II) breakdown are identified.**

Keywords—Short-circuit, Enhancement mode, Failure analysis, GaN HEMTs, GaN cascodes, GaN MISHEMTs, Hard switch fault, Reliability, Robustness, Simulation, Wide band gap semiconductor.

I. INTRODUCTION

600-650 V Gallium Nitride (GaN) Enhancement-mode High-Electron-Mobility Transistors (EHEMTs) are a potential technology for motor drive applications [1]-[3] (e.g., electrical motorbikes or industrial motors). These applications demand switches efficiently operating at high frequencies and being resilient to harsh working conditions, so as to reduce the converter volume, weight, noise, cost, and losses. Among all ruggedness tests, one of the most severe stresses is the electrical Short-Circuit (SC) during regular operation. Namely, a SC fault in the converter must be withstood by the device without destruction/degradation, and/or detected by its driver to turn it off safely. For this qualification, two electrical tests should be considered depending on whether the device is in off-state (Short-Circuit type I, SC I) or on-state (Short-Circuit type II, SC II) when SC fault occurs. Such studies have started to be frequent in SC I [3]-[5], but have been scarcely addressed in SC II [6]. Thus, there is still a lack of knowledge on their behavior under such conditions. For the first time, this work compares the response to SCs I and II, of two EHEMTs technologies commercially available [7] with similar on-state resistance (R_{on}): 600 V p-doped GaN gate (p-GaN) HEMTs and 650 V GaN Metal-Insulator-Semiconductor HEMTs (MISHEMTs). Besides, their failure mechanisms are qualitatively analyzed with physical Technology Computer Aided Design (TCAD) simulations [8].

II. TESTED DEVICES AND SC TEST BENCH

In this work, 600 V p-GaN HEMTs (R_{on} = 140 mΩ and current collapse free) [9] packaged in a Dual Flat No-lead (DFN) 8x8 and 650 V MISHEMTs (R_{on} = 100 mΩ) encapsulated with Printed Circuit Board (PCB) embedded die packaging are studied. The effect of packaging [10]-[11] on SC results is limited to the switching process without any influence either on the thermal or electrical SC behavior along the SC duration time (t_{on}). For these tests, four units of each type have been selected as Devices Under Test (DUTs).

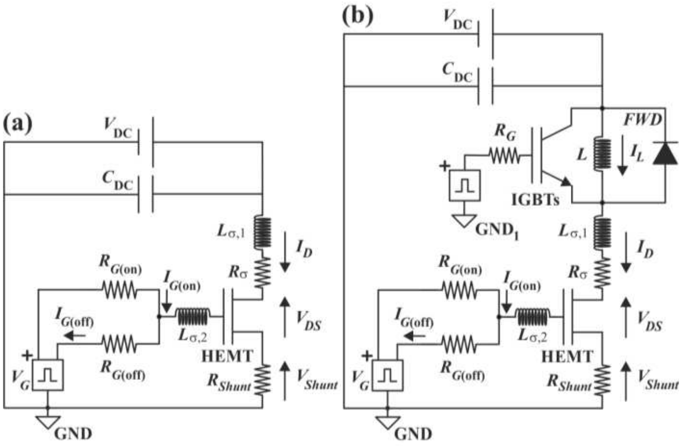

Fig. 1. Schematic of the designed test bench for (a) SC I and (b) SC II.

Fig. 1 (a) depicts the schematic of the SC I test bench [12] with its parasitics (R_σ, $L_{\sigma,1}$ and $L_{\sigma,2}$), a DC power supply (V_{DC}), a capacitors bank (C_{DC}), and a gate driver with a driving voltage V_G. The gate turn-on and -off is performed with two branches with customizable gate resistors ($R_{G(\mathrm{on})}$ and $R_{G(\mathrm{off})}$). A coaxial shunt (R_{Shunt}) monitors the drain current (I_D), while differential voltage probes are used for $I_{G(\mathrm{on})}$ (gate current (I_G) sensed at $R_{G(\mathrm{on})}$), drain-source voltage (V_{DS}), and gate-source voltage (V_{GS}) acquisition. SC II tests are performed by adding 8 complementary IGBTs connected in parallel, a freewheeling diode (FWD), and a 300 μH inductive load (L) to the SC I test circuit, as Fig. 1 (b) shows. As test conditions, ambient temperature (T_{A}) and t_{on} are set for 23 ºC and 10 μs. As a testing procedure, V_{DC} is ramped from 50 V to 400 V in steps of 50 V. To assess no electrical degradation, a single DUT of each type is cyclically tested at V_{DC} = 50, 100 and 250 V with time intervals of 60 s. For the p-GaN case, V_{GS} = 3.5 V is fixed, so that achieving $I_{G(\mathrm{on})}$ = 10 mA as manufacturer recommends. This is attained by V_G = -3 V / +4 V and $R_{G(\mathrm{on})} = R_{G(\mathrm{off})}$ = 50 Ω. By contrast, MISHEMTs are controlled with V_G = -3 V / +5 V and $R_{G(\mathrm{on})} = R_{G(\mathrm{off})}$ = 270 Ω, so that V_{GS} and the $I_{G(\mathrm{on})}$ plateau are comparable for both EHEMTs, as described further on. Besides, $V_G < 0$ avoids accidental turn-on/off in both EHEMTs.

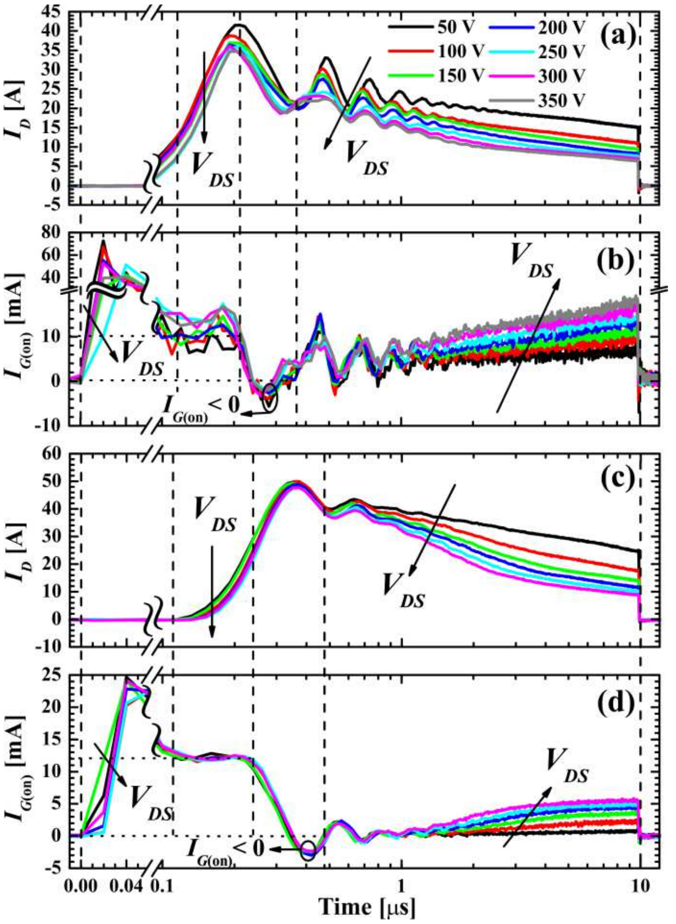

Fig. 2. Time evolution of measured I_D and $I_{G(\mathrm{on})}$ at different V_{DC} for (a, b) p-GaN HEMT and (c, d) GaN MISHEMT.

III. SC I RESULTS

In SC I test, the devices are gated on under high V_{DS} and I_D ratings, as previously stated. Under such conditions, the inspected p-GaN HEMTs and MISHEMTs have withstood without destruction V_{DC} voltages up to 350 V and 300 V. Fig. 2 depicts I_D and $I_{G(\mathrm{on})}$ for a p-GaN HEMT (Figs. 2 (a) and (b)) and MISHEMT (Figs. 2 (c) and (d)). In both devices, I_D decreases after its saturation value $I_{D(\mathrm{sat})}$, while $I_{G(\mathrm{on})}$ dynamics abnormally increases with V_{DC} up to the milliamp range. In p-GaN devices, their turn-on process is observed to be the most demanding in terms of dissipated power, as, for almost similar $I_{G(\mathrm{on})}$ values, $I_{D(\mathrm{sat})}$ decreases with V_{DC}. To comprehend all this, physical TCAD simulations have been performed and set to match the measured electrical behavior [4]. Since p-GaN and MISHEMT devices present similar internal structures, only the p-GaN HEMT has been simulated for a SC I at $V_{\mathrm{DC}} = 350$ V. P-GaN HEMT experimental and simulated V_{GS}, $I_{G(\mathrm{on})}$, and I_D waveforms are depicted in Figs. 3 (a)-(c) together with the simulated maximum and gate temperatures (T_{Max} and T_{Gate}) (Fig. 3 (d)). In this analysis, charge trapping is omitted and I_D decay is mainly attributed to thermal effects, as they have been proved to be current collapse free for regular operation [13]. Besides, they have a rapid thermal response (1 µs; steady-state) and a high thermal resistance due to the buffer layer thermal properties [5]. Therefore, the temperature (T) dependence of the electrons mobility ($\mu(T)$) in the Two- Dimensional Electron Gas (2DEG) channel is set for $\mu(T) \propto T^{-2.15}$ to obtain an excellent agreement with measurements. In literature, $\mu(T) \propto T^{-1.5}$ is typically considered for GaN bulk in accordance to the acoustic phonon electron scattering, and is commonly extended to heterojunctions modelling [14]. However, other effects (e.g., Silicon substrate lattice parameter) could lead to a stronger $\mu(T)$ dependence with T as reported in [14].

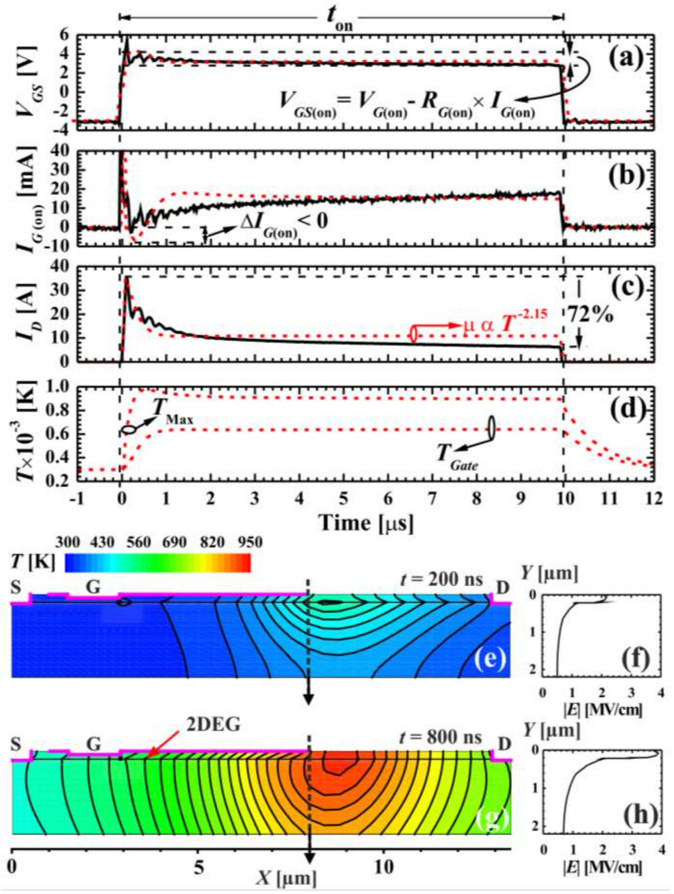

Fig. 3. Measured (black lines) and simulated (red dashed lines) waveforms for p-GaN HEMT at $V_{\mathrm{DC}} = 350$ V: (a) V_{GS}, (b) $I_{G(\mathrm{on})}$, and (c) I_D, jointly with (d) simulated T_{Gate} and T_{Max}. Simulated T distribution in the 2DEG channel and $|E|$ vertical profiles at the field plate right edge (black lines) at (e, f) $t = 200$ ns and (g, h) $t = 800$ ns, respectively.

Fig. 3 also presents the simulation results corresponding to the cross section of a p-GaN HEMT [15] with its internal temperature distribution and a vertical cut of the absolute electric field ($|E|$) at its field plate right edge for different time instants (t): t = 200 ns ($I_{D(\mathrm{sat})}$ reached, Figs. 3 (e)-(f)) and t = 800 ns (Figs. 3 (g)-(h)). Figs. 3 (e)-(g) highlight a hotspot formation (reaching a 950 K peak) beneath the field plate edge, which is the responsible for I_D decrease during SC in p-GaN and MISHEMT devices. $I_{G(\mathrm{on})}$ abnormal dynamics results from the heat diffusion from the hotspot to the p-GaN HEMT gate, and follows the thermal trend expected for a Schottky contact and pn-junction [9]. This indicates that the gate threshold voltage ($V_{GS(\mathrm{th})}$) decreases with T_{Gate} [16], incrementing $I_{G(\mathrm{on})}$, with a similar effect for the case of the MISHEMT. Moreover, the high $I_{G(\mathrm{on})}$ provokes a significant voltage drop in $R_{G(\mathrm{on})}$, thereby reducing $V_{GS(\mathrm{on})}$ during the SC event, as shown in Fig. 3 (a). Besides, T_{Max} does not overcome the critical temperature

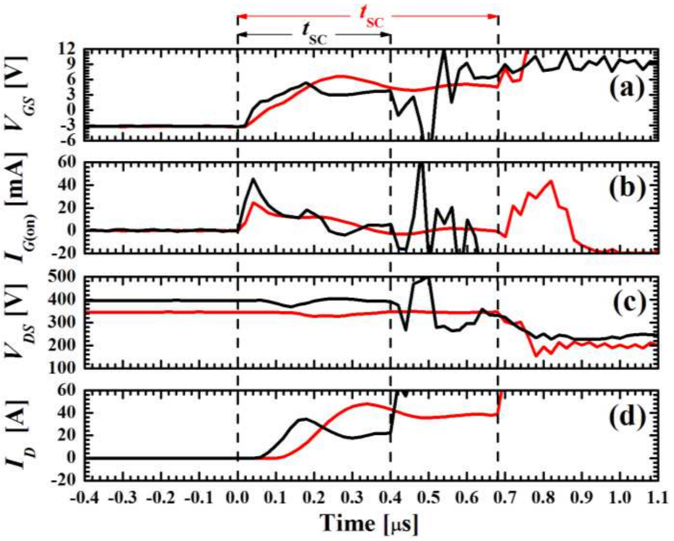

Fig. 4. Results for p-GaN HEMT (black line) and GaN MISHEMT (red line) destructive SC I test during a SC time before failure t_{SC}. Respectively, V_{DC} = 400 V and 350 V, I_G = 10 mA and V_{GS} = -3 / +5 V, $R_{G(on)} = R_{G(off)}$ = 50 Ω and 270 Ω: (a) V_{GS}, (b) $I_{G(on)}$, (c) V_{DS} and (d) I_D.

for the device destruction. Fig. 4 depicts the SC I electrical signature for the p-GaN HEMT and MISHEMT, which after a certain time to failure (t_{SC}) explodes at V_{DC} = 400 V and 350 V, respectively. The p-GaN breaks down at the instant t = 400 ns, after achieving $I_{D(sat)}$ (channel saturation) and I_D significantly decreasing. As simulation supports, a high $|E|$ at the field plate right edge is attained in the 2DEG channel, developing a hotspot. This induces an abrupt I_D rise without a high $I_{G(on)}$, and outlines a purely thermal destruction for both EHEMTs, as experimental results clearly demonstrate.

IV. SC II RESULTS

SC II tests start with the DUT in conduction state, under a low V_{DS} and I_D fixed by the inductive load. Then, at the instant t = 8 µs, the complementary IGBTs are gated on, thereby shorting the load and submitting the DUT to extremely high V_{DS} and I_D levels. Figs. 5 and 6 depict the experimental waveforms of V_{GS}, $I_{G(on)}$, V_{DS} and I_D, of a p-GaN HEMT and MISHEMT without reaching their destruction under SC II stresses. P-GaN HEMTs successfully passed the test at V_{DC} = 350 V for t_{on} = 17 µs. As they presented a high turn-on dissipation in SC I, such devices have been submitted to such a long SC event to discard an eventual thermal breakdown. As for MISHEMTs, they overcame only once a cyclical SC fault at V_{DC} = 250 V during t_{on} = 10 µs. In contrast with SC I, a lower $I_{D(sat)}$ should be expected for both EHEMTs in SC II results, as they are in on-state prior to SC event (i.e., $T > T_A$). However, this trend is not completely reported in Figs. 5 (d) and 6 (d) due to the power circuit and driving loop parasitics. In fact, the IGBTs turn-on induces a high V_{GS} and I_D ringing, which affects $I_{D(sat)}$ in both devices and accidentally turns the p-GaN HEMT off during 1 µs. In this regard, the MISHEMT failed after withstanding a second SC II stress at V_{DC} = 250 V (Fig. 7), due to a gate dielectric damage (see Fig. 7 (a)) induced by parasitics. Thus, the MISHEMTs power dissipation, V_{GS} ringing, and $I_{D(sat)}$ under SC II are higher due to parasitics, extremely limiting the MISHEMTs ruggedness.

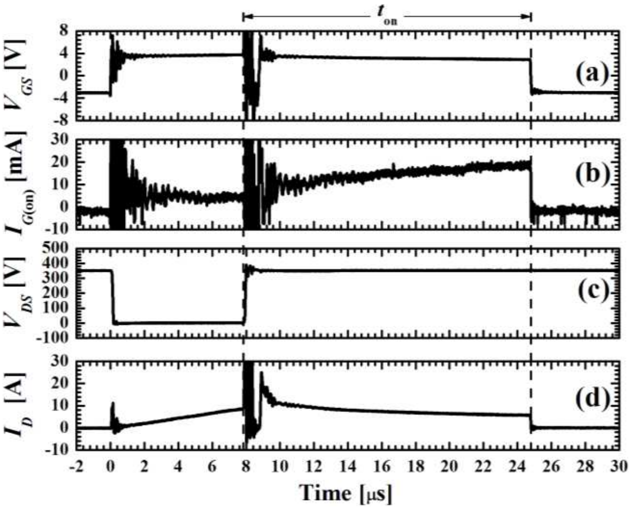

Fig. 5. Results for p-GaN HEMT non-destructive SC II stress. V_{DC} = 350 V, I_G = 10 mA, $R_{G(on)} = R_{G(off)}$ = 50 Ω: (a) V_{GS} , (b) $I_{G(on)}$, (c) V_{DS} and (d) I_D.

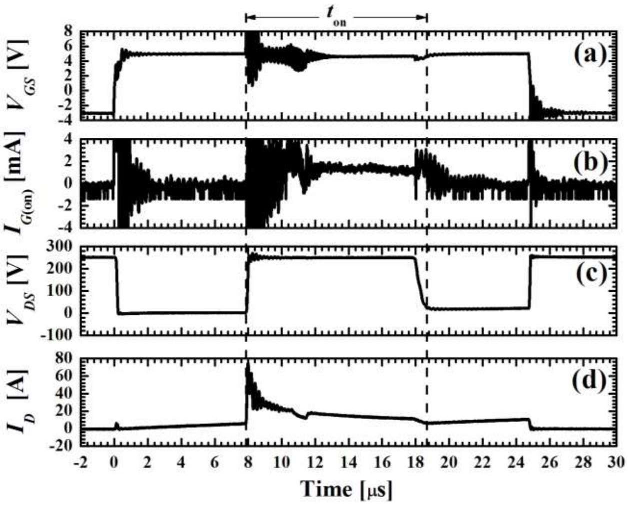

Fig. 6. Results for GaN MISHEMT non-destructive SC II test. V_{DC} = 250 V, V_{GS} = -3 / +5 V, $R_{G(on)} = R_{G(off)}$ = 270 Ω: (a) V_{GS}, (b) $I_{G(on)}$, (c) V_{DS} and (d) I_D.

V. DISSIPATED AND BREAKDOWN CRITICAL ENERGIES

As a results summary, the dissipated (E_{SC}) and breakdown critical (E_{Crit}) energies for all tests are plotted as a function of V_{DS} and calculated as follows:

$$E_{\text{SC}} = \int_0^{t_{\text{on}}} V_{DS} \cdot I_D, \tag{1}$$

$$E_{\text{Crit}} = \int_0^{t\text{SC}} V_{DS} \cdot I_D. \tag{2}$$

Fig. 8 depicts such a dependence of E_{SC} (in lines) and E_{Crit} (circled dots) on V_{DC}. Fig. 8 evidences that p-GaN HEMTs present the highest SC capability, especially under SC II. This behavior results from their similar or lower E_{SC} values due to the thermal self-regulation effect of $\mu(T)$ on I_D. As for failed devices, Fig. 8 shows a higher E_{Crit} at a lower V_{DC} for the MISHEMTs, particularly for SC II. As further factors are involved in SC II events, failure mechanisms can differ from those of SC I and justify this trend. Namely, circuit parasitics are relevant and the dielectric breakdown has been identified

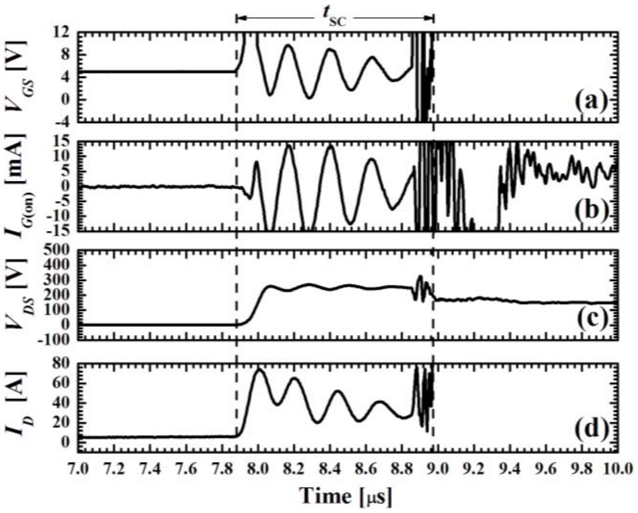

Fig. 7. Results for GaN MISHEMT destructive SC II test during a SC time before failure t_{SC}. V_{DC} = 250 V, V_{GS} = -3 / +5 V, $R_{G(on)} = R_{G(off)}$ = 270 Ω: (a) V_{GS}, (b) $I_{G(on)}$, (c) V_{DS} and (d) I_D.

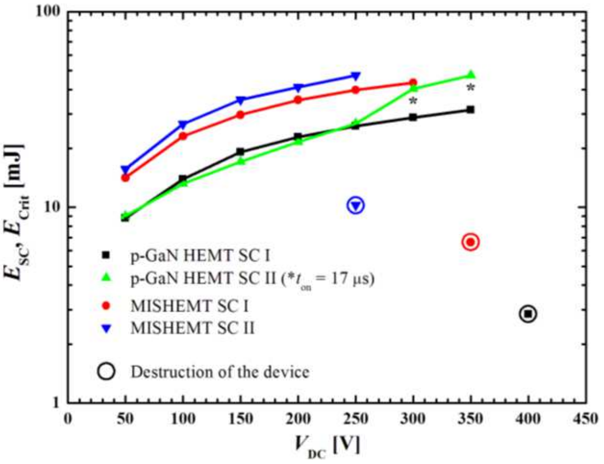

Fig. 8. Dissipated (lines) and critical energies (circled dots, ○) with V_{DC} in p-GaN HEMTs for SC I (black line, ■) and SC II (green line, ▲), and in GaN MISHEMTs for SC I (red line, ●), and SC II (blue line, ▼).

in MISHEMTs. Thus, SC II is more demanding than SC I and closer to the final application scenario, as other limiting application-related aspects can be taken into account.

VI. CONCLUSIONS

The SC I and II capability of 600 V p-GaN HEMTs and 650 V MISHEMTs has been analyzed by comparing experimental and physics-based simulation results. Measurements demonstrated that p-GaN HEMTs have withstood a SC at V_{DC} = 350 V during 10 µs (SC I) and 17 µs (SC II). By contrast, MISHEMTs have endured for 10 µs, a SC I at V_{DC} = 300 V and SC II at V_{DC} = 250 V. The strong dependence of $\mu(T)$ on T has improved the EHEMTs ruggedness, as it exerts a self-regulation effect on I_D. As for the failure in SC I, the sharp I_D rise without a relevant $I_{G(on)}$ leakage points to a thermal breakdown, as also observed in the simulation results for the p-GaN case. During SC II test, MISHEMTs have shown a dielectric breakdown due to the parasitics coming from the test bench, thus being less rugged than p-GaN HEMTs. Both technologies require the use of fast protection circuits (< 400 ns) for being resilient to SC events at the V_{DC} used in their targeted final applications (V_{DC} = 400 V).

ACKNOWLEDGMENT

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Power Losses and Current Distribution Extraction in IGBTs under Resonant Load and ZVS Condition

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***Abstract*—According to the approaches currently followed, power devices junction temperature (T_j) measurements correspond to an average value of the device working temperature and usually having the thermal map can provide additional information that can be related with abnormal working conditions. In view of this, Infrared Lock-in Thermography (IR-LIT) is used to determine at the die level, the power losses and current distribution in IGBTs used in resonant soft-switching power converters when functioning within or outside the Zero Voltage Switching (ZVS) condition. As a result, relevant information is obtained related to decreasing the power losses during commutation in the final application, and a thermal model is extracted for simulation purposes.**

***Index Terms*—IGBTs, Infrared Lock-in Thermography, Simulation, Thermal model, Weak spot detection, ZVS Condition.**

I. INTRODUCTION

INDUSTRIAL power converters are designed to operate under rated conditions of voltage, current, frequency, and temperature. However, they are susceptible to change according to the load and operating environment, as observed in many applications [1] [2]. In this scenario, the power circuit designer should be able to identify the limitations of the power semiconductor devices when functioning out of their nominal conditions to ensure an efficient and safe operation of the power system. In this sense, Failure Mode and Effects Analysis (FMEA) help to identify potential failure modes and provide useful information to evaluate the reliability at system level. In particular, power semiconductor devices are a key part to warrant the converter requirements in terms of performance, efficiency and reliability. Usually, these devices are submitted to a high electro-thermal stress [1], which, in combination to an operation out of their nominal switching conditions, provokes the system failure [2]. Under such situations, the devices reach destruction due to overtemperature or a local high electric field due to current crowding effects [1], which is manifested in both cases, on the die surface with a temperature increase. Therefore, an adequate method to measure not only the power devices local temperature under real operation [3], but also the current distribution, becomes crucial when designing a power converter for reliability. Apart from a selection criterion for the thermal management strategy, this methodology would be extremely useful for determining the most rugged devices for a targeted application.

Unfortunately, solutions directly addressing such demands are not currently available. Nowadays, this problem is tackled gathering simulation and experimental approaches aiming at determining first, the device power losses and after, their associated thermal compact model. Traditionally, the device power losses can be directly measured by electrical means at risk of being invasive or/and unsuitable depending on the application [4]. Furthermore, soft-switching techniques used for reducing losses and electromagnetic emission make difficult the power losses measurements electrically [4]. One of the less invasive solutions is the use of accurate calorimeters [4]-[8], inspired on those employed for power converters efficiency evaluation [9]-[15]. Although their sensitivity and precision have been improved at cost of lengthening the acquisition time, they require to slightly modify the converter geometry without locally accessing to the die. In such cases, the temperature extraction at die level could even be useful for validating the thermal model commonly used for design purposes [16], especially in highly efficient converters using soft-switching driving strategies as in Induction Heating (IH) appliances [6]-[8]. In conclusion, a direct access to the chip surface for temperature monitoring with short acquisition times is mandatory to offer a solution to the aforementioned needs and reduce the design time. Moreover, an approach like this could be very useful for circuit-level simulations to investigate the interaction between the device and circuit parasitics.

In response to this, an experimental approach is proposed to extract at the die level, the power losses and current distribution in IGBTs used in resonant soft-switching power converters. Such circuits connect in parallel the IGBT, its free-wheel diode, and snubber capacitor, making difficult determining the power losses in each component. Besides, the IGBTs have been studied when working within and outside Zero Voltage Switching (ZVS) conditions. From a reliability point of view, the influence of ZVS condition on the current distribution within an IGBT is of concern. Switching when ZVS is not verified can yield to an overheated area resulting

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into a local overstress in the device. When the IGBT loses ZVS condition, the turn-on power losses can be significantly increased [17]. This fact translates into a higher current concentration at the weakest spots of the device (hot-spots). To inspect all these aspects, a half bridge has been designed so that the semiconductor power device under test is visually accessible with an infrared (IR) thermographic system to acquire its thermal field in DC and its spectral component at the switching frequency (f_{Sw}). Among all existing techniques for non-invasive thermal measurements [15][16][18]-[24], IR thermography [25]-[27], combined with a lock-in detection strategy (IR Lock-In Thermography, IR-LIT) [22], has been selected because of its commercial availability, high thermal resolution (below 1 m°C) and high rejection to noise and thermal boundary conditions [28]-[34]. As a result, power losses and current distribution at the die level can be carried out as follows. With DC measurements, the junction temperature (T_{j}) is determined to derive power losses, as they are the main contribution to the device thermal field. In contrast, the current distribution within the device is detected at f_{Sw} by lock-in strategies to identify possible current crowding problems. In comparison to prior works, the proposed approach differs from [35][36] in the used circuit and the tests aim: the device is studied under real working conditions, rather than repetitive stressful switching conditions for safe operating area investigations only oriented to FMEA purposes.

According to all stated, the paper is organized as follows. Section II describes all experimental details of the proposed approach. Section III presents the electro-thermal modelling of the designed test bench. Section IV reports on power losses determination in a IH typical scenario, while current distribution measurements are performed at around 10 kHz. Finally, Section V draws the main conclusions.

II. APPROACH, TEST BENCH AND SAMPLE PREPARATION DESCRIPTION

A. Approach Theoretical Aspects

The methodology proposed to extract power losses (P_{gen}) and current distribution at die level exploits the Joule effect inherent to power devices operation. P_{gen} is the sum of the power dissipated per cycle in on-state (P_{On}) and the transitions from on to off, or viceversa, (P_{Sw}). As a die averaged value, T_{j} and P_{gen} are related, according to a reference temperature (T_{Ref}), through the thermal impedance $Z_{\mathrm{th,(j\text{-}Ref)}}$ [32] as:

$$\Delta T_{(\mathrm{j-Ref})}(t) = \int_0^t P_{\mathrm{gen}}(\tau)\left(\frac{dZ_{\mathrm{th(j-Ref)}}(t-\tau)}{dt}\right)\cdot \mathrm{d}\tau \qquad (1)$$

where $\Delta T_{(\mathrm{j-Ref})}(t) = T_{\mathrm{j}}(t) - T_{\mathrm{Ref}}(t)$. Known $\Delta T_{(\mathrm{j-Ref})}(t)$ and $Z_{th,(\mathrm{j-Ref})}(t)$, P_{gen} (t) is thus inferred by solving (1) in steady state. Besides, P_{On} and P_{Sw} are also derived as detailed in II.B.

This situation changes when current crowding problems occur. Under operation conditions, it is of importance to determine the location where the current density extremely increases at f_{Sw}. There, a weak hot spot appears and superpose to the DC component of the surface thermal field, giving rise to a surface thermal field spectral component at f_{Sw} [33]-[37] as:

$$\Delta T_{\mathrm{surf}}(\vec{r},\vec{r}_n,t,f_{\mathrm{Sw}}) = |P_0(f_{\mathrm{Sw}})| \times \sum_{n=1}^{N} \iint_{S_{HS,n}} dS_{HS,n}\left[a_n \times \frac{C}{|\vec{r}-\vec{r}_n|} \times e^{-\phi_{\tau,n}} \times \cos\left(2\pi f_{\mathrm{Sw}} t - \phi_{\tau,n} - \frac{\pi}{4}\right)\right] \qquad (2)$$

where $|\vec{r}-\vec{r}_n|$ is the distance between each location $\vec{r}$ from the coordinate origin of the thermal field and each hot spot location ($\vec{r}_n$), $dS_{HS,n}$ is the differential of surface of the n^{th} hot spot, and C is a boundary condition constant. $|P_0(f_{\mathrm{Sw}})|$ is the amplitude of the first harmonic spectral component of the total active power dissipated by all hot spots. a_n corresponds to a fraction of $|P_0(f_{\mathrm{Sw}})|$ dissipated in each hot spot. $\phi_{\tau,n}$ is the thermal phase lag related with the heat propagation around a given hot spot n, defined as $\phi_{\tau,n} = |\vec{r}-\vec{r}_n|/\rho$. ρ is the thermal diffusion characteristic length and writes as $\rho = \sqrt{D(\pi f_{\mathrm{Sw}})^{-1}}$, where D is the thermal diffusivity of the media. From its comparison to the die thickness h, ρ establishes when the external boundary conditions do not affect IR-LIT measurements ($\rho < h$, thermally thick condition) [37]-[38], also confining the thermal field around the hot spots (spatial resolution improvement). For their detection, lock-in strategies allow recovering these low thermal signals in the frequency domain. Thus, the thermal amplitude $|\Delta T_{\mathrm{surf}}|$ and phase lag Φ_{surf} maps of $\Delta T_{\mathrm{surf}}(\vec{r},\vec{r}_n,t,f_{\mathrm{Sw}})$ are extracted at f_{Sw}. The used criteria for hot spot location is to determine the position where a local maximum, in $|\Delta T_{\mathrm{surf}}|$, and a local minimum, in Φ_{surf}, are simultaneously observed [22].

B. Test Circuit Presentation and Design

For the intended experiments, the specific test circuit depicted in Fig. 1 has been designed and implemented. This circuit is based on a half-bridge resonant inverter with a flexible resistive (R_{eq}) and inductive (L_{eq}) load, where the Device Under Test (DUT) is connected in series to the IGBT on the lower branch (AUX). The resonant capacitors (C_{res}) can be easily modified to adjust the resonance current and frequency (f_{res}), while configurable capacitors (C_{snub}), gate resistances (R_G) and gate drivers ensure a correct commutation of the IGBTs under the specified switching conditions. Besides, the drivers allow easily tuning the device gate voltage amplitude and polarity. The board has included some monitoring points for electrical measurements in the DUT and load. The DUT's collector current (I_{C}) has been monitored using a Hall probe TCP202 with a current transformer, while for the load current (I_L), a Pearson current monitor model 2877 has been used, also together with a current transformer. Moreover, the DUT collector-emitter and gate-emitter voltages (V_{CE} and V_{GE}, respectively) have been acquired with voltage probes P5050.

Depending on the load characteristics, f_{res} would differ. The designed flexible load allows setting all parameter within these ranges: R_{eq} = {3 to 6 Ω}, L_{eq} = {24 to 275 µH}, and C_{res} = {1 to 4.5 µF}. In an IH application, for instance, R_{eq} and L_{eq} are dependent on the inductor-recipient interaction, resulting into a fixed equivalent power factor (PF) in the range of

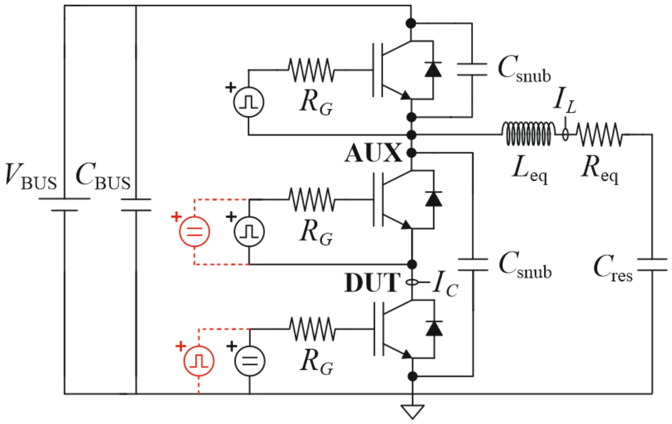

Fig. 1. Schematic of the designed test platform for the IGBT DUT conduction (black) and switching (red) power losses decoupling.

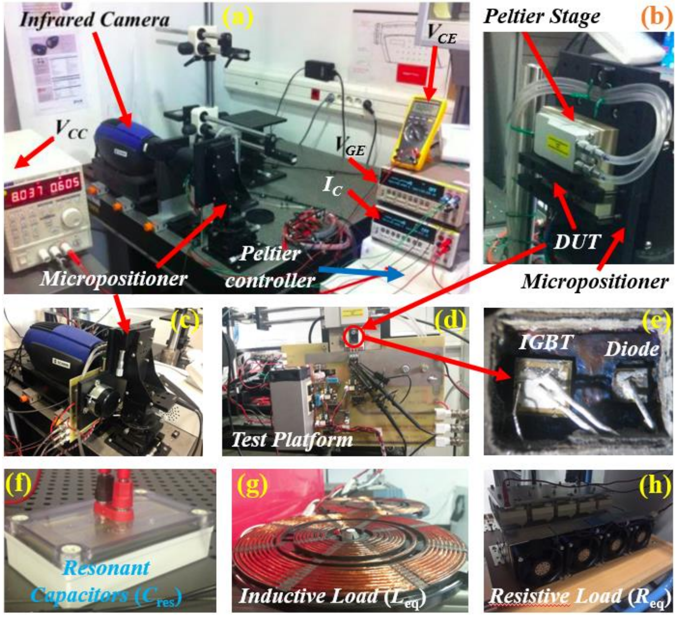

Fig. 2. (a) Experimental test bench for performing IR Thermographies, (b) Peltier stage, (c) test platform mounted on a micropositioner, (d) test platform and (e) detailed view of the device, and flexible (f) resonant capacitors, (g) inductive load and (h) resistive load.

0.43~0.49 for commercially available recipients. Therefore, the power supplied to the load, which comes from a power source at a BUS voltage (V_{BUS}) of 300 V, can be controlled by the modification of f_{Sw}, with respect to f_{res}, in the range of 35-80 kHz for IH.

With this circuit, the DUT when dissipating only P_{On} or both (i.e., $P_{\mathrm{On}} + P_{\mathrm{Sw}}$) can be electrically or thermally evaluated as follows. In P_{On} determination, the DUT is kept at a gate-emitter voltage (V_{GE}) of 20 V, while AUX is commutated according to a Zero Voltage Switching (ZVS) strategy (Fig. 1, black color). Conversely, $P_{\mathrm{On}} + P_{\mathrm{Sw}}$ measurements interchange the role of the devices, i.e., the DUT is switched, while AUX is under conduction state (Fig. 1, red color). From the comparison of both results, P_{Sw} can be inferred.

C. Test Bench Description

To carry out the proposed approach by IR measurements, Figs. 2 (a)-(b) depict the used test bench [39]. Figs. 2 (c)-(d) show the test circuit described in section II.B mounted on a micropositioning stage to allow its precise displacement and focusing. Fig. 2 (e) presents a detailed view of the packaged device shown in Fig. 2 (d), where both chips are visually accessible. Finally, the capacitances, inductors and resistances which constitute the flexible load are presented in Figs. 2 (f)-(h), respectively.

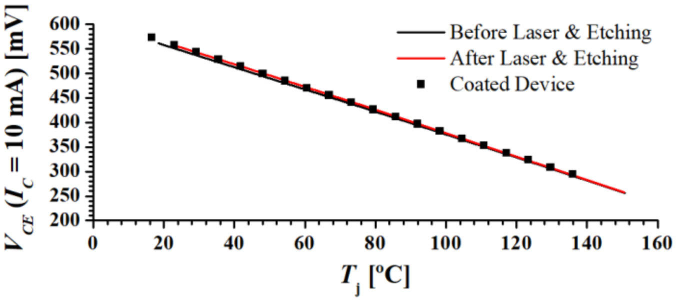

Fig. 3. Sample preparation effects on TSP calibration (Device II).

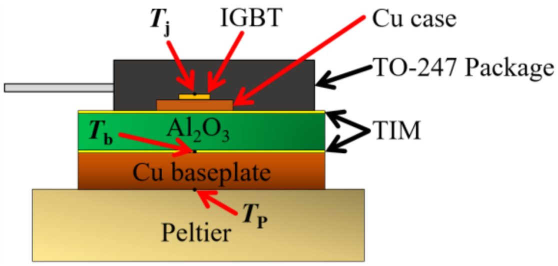

Fig. 4. Device layers structure including the TO-247 package, the TIMs, an Al_2O_3 layer, a Cu baseplate, and a Peltier.

The IR measurements have been performed using a FLIR C5500 camera with an internal lock-in module and a set of microscopic lenses with lateral resolutions up to 5 µm. The IR images have been acquired at a frame rate (f_r) of 376 Hz and an integration time (t_{int}) of 49 µs. A total of 5×10^4 IR images have been acquired at each test and processed at different lock-in frequencies ($f_{\mathrm{lock}} = f_{\mathrm{Sw}}$, 8-10 kHz). The visually accessible packaged chips (IGBT and Diode) have been positioned over a Peltier thermoregulated stage to set its initial temperature (T_{i}) at 50ºC, which helps to improve the signal-to-noise ratio of the camera (S/N) [22] and also fixes an initial representative operating temperature on the device.

D. Devices Preparation and Electrothermal Characterization

For the proposed tests, five samples of a commercially available 650 V-40 A IGBT with a free-wheel diode co-packaged in a TO-247 format have been used and studied as a demonstrator. Several actions have been performed to prepare them for the IR measurements. To have visual access to both dies, the molding compound covering four of them has been removed, leaving one as a reference. This step has been performed combining physical and chemical processes. First, a laser etching is carried out to create a container on top of the package. After, benefiting from this, the container is filled in of acid, which finally removes the rest of molding compound. To increase the IR measurement sensitivity [24], the dies have been covered using a uniform and high emissivity material.

Next to the samples preparation, the thermal impedance junction to case ($Z_{\mathrm{th(j\text{-}c)}}$) of these devices has been extracted to

TABLE I
CAUER NETWORK PARAMETERS FOR $Z_{th(j-c)}$ - R IN [K/W] AND C IN [J/K]

Model	R_1	R_2	R_3	R_4	R_5	C_1	C_2	C_3	C_4	C_5
$Z_{th(j-b)}$	0.053	0.172	0.165	0.300	0.210	$4\cdot10^{-4}$	$2.6\cdot10^{-3}$	0.043	0.313	2.538
$Z_{th(j-P)}$	0.041	0.184	0.235	0.735	0.917	$3\cdot10^{-4}$	$2.4\cdot10^{-3}$	0.561	0.467	17.93

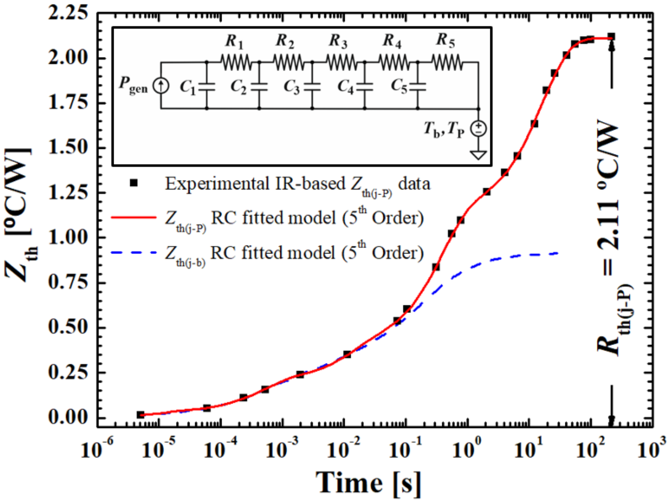

Fig. 5. Experimental IGBT $Z_{th(j-P)}$ (points) including 5th order Foster model fit of $Z_{th(j-P)}$ (red solid line) and the 5th order Foster model fit of $Z_{th(j-b)}$ (blue solid line).

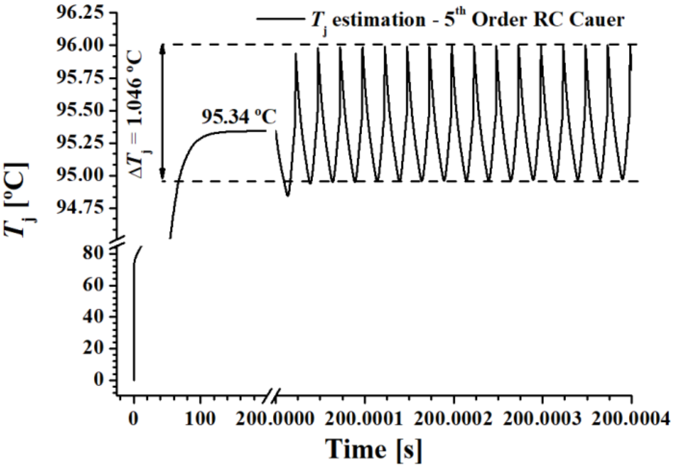

Fig. 6. T_j estimation based on the obtained Foster and Cauer CTM and using superposition principle.

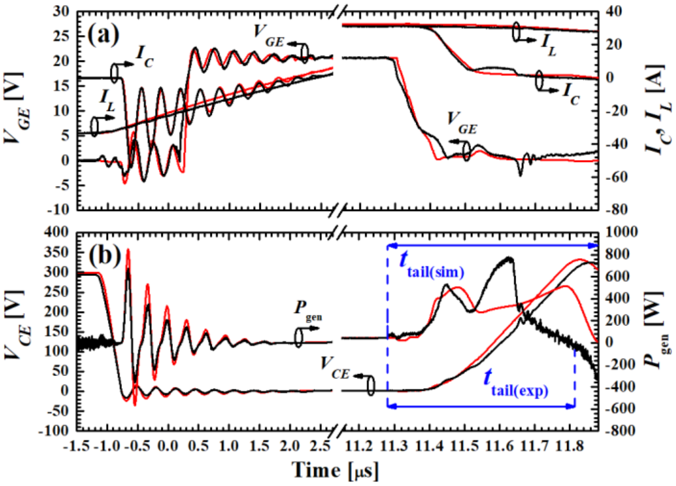

Fig. 7. Detailed view of the (a) turn-on and (b) turn-off commutation electrical waveforms and simulation for $P_{Sw} \neq 0$.

check whether their thermal performance have been modified. To this end, the set-up presented in [40]-[41] was used. The device is first submitted to a step-like pulse (P) of 21 W until reaching its thermal steady state. In that instant, the device dissipation is stopped, and while the device cools down, T_j and its case temperature T_C are captured simultaneously. T_j is directly measured using a thermosensitive parameter (TSP), while T_C is acquired using a spring-loaded K-type thermocouple. With both and considering P as a step-like input, $Z_{th(j-c)}$ is inferred as follows:

$$Z_{\text{th(j−c)}}(t) = \frac{T_j(t) - T_c(t)}{P} \tag{3}$$

As a result, no modification has been introduced due to sample preparation. In this measurement, the TSP selected is V_{CE} at I_C = 10 mA, which has been calibrated from 20 ºC to 135 ºC in an oven. Fig. 3 compares this calibration along the different steps of the sample preparation, demonstrating the independence of data from this process.

III. TEST PLATFORM ELECTRO-THERMAL MODELLING

A. System CTM Extraction by IR and Electrical Means

For the test platform accurate electro-thermal modelling and P_{gen} determination, the total thermal impedance and resistance of the set of elements shown in Fig. 4 ($Z_{th(j-P)}$ and $R_{th(j-P)}$, respectively) is required, i.e.: the encapsulated device, thermal interface materials (TIM, silicone grease), Alumina (Al_2O_3) and copper (Cu) layers, and Peltier stage. Unfortunately, this cannot be performed as in II.D, since the test platform is not compatible. Besides, the IR camera does not present a time resolution to reach timescales below 1 ms to extract T_j. As a solution, electrical and IR measurements have been combined. First, the thermal impedance from junction to Cu baseplate ($Z_{th(j-b)}$, see Fig. 4) has been extracted as performed in II.D. Next, this assembly is mounted on top of the Peltier stage and T_j is monitored by IR means, obtaining the contribution of Peltier heating system. From both results, a final $Z_{th(j-P)}$ is inferred, considering $Z_{th(j-b)}$ as an offset correction to the IR results. Fig. 5 presents $Z_{th(j-b)}$ (blue dashed line) and $Z_{th(j-P)}$ (black squared points) results. Moreover, a CTM based on the 5th order RC Cauer network depicted in the inset of Fig. 5 is fitted in each case (red solid line in $Z_{th(j-P)}$) and their parameters summarized in Table I. From these results, $R_{th(j-P)}$ = 2.11 ºC/W, which is indispensable for P_{gen} determination.

B. Test Circuit Modelling for IR Results Assessment

To assess the IR results, the test circuit shown in Fig. 1 has been simulated electrothermally at circuit level. First, the IGBTs model supplied by the manufacturer has been checked. To this end, the I_C-V_{CE} static characteristic curves of prepared devices at V_{GE} = 20 V have been measured at different temperatures (from 25 ºC to 125 ºC), and compared with the manufacturer model prediction. As a result, a good agreement has been obtained. Moreover, the test circuit parasitics have been fully characterized from electrical measurements and simulation results comparison. Finally, the system CTM derived in III.A is incorporated in the model.

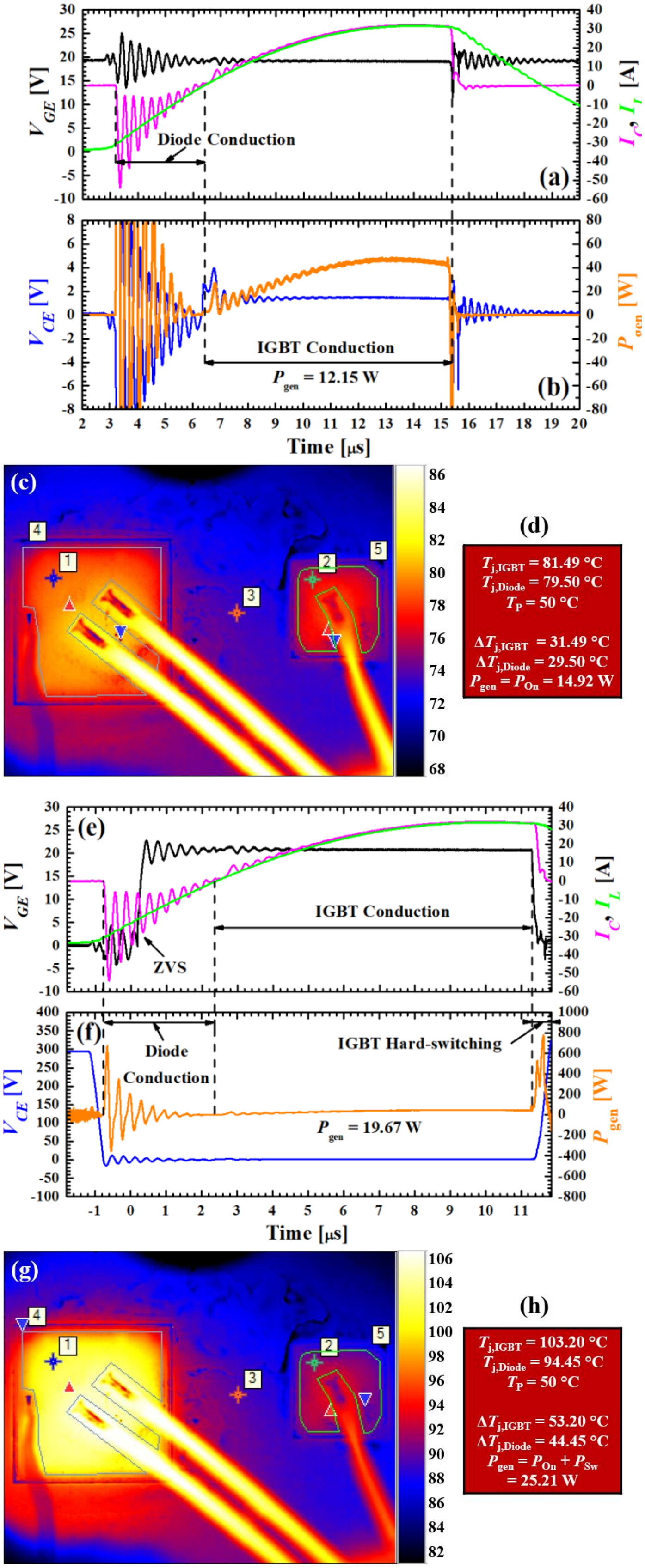

Fig. 8. Electrical waveforms on the DUT for (a)-(b) $P_{Sw} = 0$ and (e)-(f) $P_{Sw} \neq 0$, and IR thermographies, $T_{j,IGBT}$ and $T_{j,Diode}$ measurements as well as their variation ($\Delta T_{j,IGBT}$ and $\Delta T_{j,Diode}$) for (c)-(d) $P_{Sw} = 0$ and (g)-(h) $P_{Sw} \neq 0$.

As for thermal calculation, T_j is computed with the following simplification to reduce simulation time. According to (1), $P_{gen}(\tau)$ can be written with two terms, periodic and slow contributions, depending on τ:

$$P_{gen}(\tau) = P_{AC}(\tau) + P_{Slow}(\tau) \tag{4}$$

where, $P_{AC}(\tau)$ is a fast-varying periodic function of τ and $P_{Slow}(\tau) = P_0 \cdot f(\tau)$ is a slow-varying function of τ. Thus:

$$\Delta T_{(j-Ref)}(t) = \Delta T_{(j-Ref),AC}(t) + \Delta T_{(j-Ref),Slow}(t) \tag{5}$$

which are:

$$\Delta T_{(j-Ref),AC}(t) = \int_0^t P_{AC}(\tau) \cdot \left(\frac{dZ_{th(j-Ref)}(t-\tau)}{dt}\right) d\tau \tag{6}$$

$$\Delta T_{(j-Ref),Slow}(t) = P_0 \int_0^t f(\tau) \cdot \left(\frac{dZ_{th(j-Ref)}(t-\tau)}{dt}\right) d\tau \tag{7}$$

When $t_0 \to \infty$ (steady state) in (7), $\Delta T_{(j-Ref),Slow}(t_0) = P_0 \cdot R_{th(j-Ref)}$, while in (6), $\Delta T_{(j-Ref),AC}(t_0)$ represents the steady state thermal oscillations. Thus, T_j calculation can be addressed in two steps when the goal is to extract the steady state temperature of the device. First, P_{gen} steady state value is considered in CTM, and, after, the periodic component of the power is applied to the CTM. Thanks to this, results are rapidly achieved after a few simulation cycles, as indicated in Fig. 6. This figure shows the thermal simulation results obtained in steady state after following the superposition approach here detailed.

To show the good agreement between the present model and experimental results, a comparison of the electrical measurements and simulation results is addressed in Figs. 7 (a)-(b), where it is shown a detailed view of the device commutations to on and off state (i.e., $P_{Sw} \neq 0$). As test conditions, typical values encountered in IH domestic appliances have been set in the test circuit, i.e.: V_{BUS} = 300 V, f_{Sw}= 40 kHz, f_{res} = 29.6 kHz, R_{eq} = 3 Ω, C_{res} = 1080 nF, and C_{snub} = 15 nF. From these results, it has been obtained a similar behavior to an electrical measurement in terms of the parasitics modelisation. Unfortunately, as Fig. 7 (b) highlights, the IGBT tail current behavior ($t_{tail(sim)}$) when compared to the measured waveform ($t_{tail(exp)}$) does not match. This cannot be fixed by using the model provided by the DUT manufacturer. In such calculations, this introduces a certain error in the power determination of 1.4 W, which signifies an acceptable error of 6% in the prediction. In conclusion, in spite of the IGBT tail current non proper modelling, it is obtained a satisfactory agreement between simulation and electrical approaches, being satisfactory for the assessment of the approach presented.

IV. IR EXPERIMENTAL RESULTS

A. *Power Losses Extraction from IR Measurements*

First, the suitability of IR thermography for measuring P_{gen}

TABLE II
TEST CONDITIONS AND MEASURED TOTAL POWER LOSSES

Nº	V_{BUS} [V]	T_P [ºC]	f_{Sw} [kHz]	f_{res} [kHz]	R_{eq} [Ω]	L_{eq} [H]	C_{res} [nF]	C_{snub} [nF]	Electrical [W]	IR [W]	Sim. [W]
A-I	300	50	40	29.6	3	24.78	1080	15	19.67	25.21	21.48
A-II	250	50	40	29.6	3	24.78	1080	15	15.80	17.21	14.56
A-III	250	50	40	29.6	3	24.78	1080	No	22.93	21.65	24.44
A-IV	200	50	20	29.6	3	24.78	1080	15	18.36	17.46	19.21
A-V	200	50	20	29.6	3	24.78	1080	No	11.94	10.73	9.46

TABLE III
TEST CONDITIONS FOR CURRENT DISTRIBUTION MEASUREMENTS

Nº	V_{BUS} [V]	T_P [ºC]	f_{Sw} [kHz]	f_{res} [kHz]	R_{eq} [Ω]	L_{eq} [H]	C_{res} [nF]	C_{snub} [nF]	ZVS
B-I	300	50	9.31	9.25	6.6	274	1080	15	Yes
B-II	300	50	9.11	9.25	6.6	274	1080	No	Yes
B-III	300	50	9.31	9.25	6.6	274	1080	15	No
B-IV	300	50	9.11	9.25	6.6	274	1080	No	No

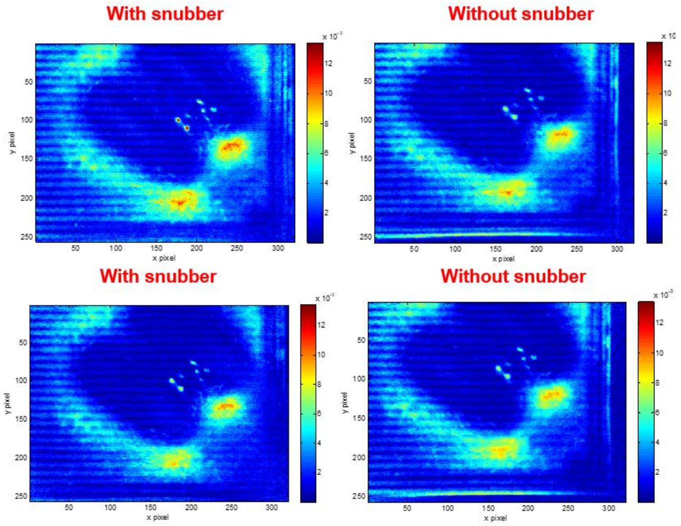

Fig. 9. Current distribution: (a) ZVS condition and snubber capacitor (test B-I), (b) ZVS condition and without snubber capacitor (test B-II), (c) Non-ZVS condition and snubber capacitor (test B-III) and (d) Non-ZVS condition and without snubber capacitor (test B-IV).

has been assessed by experimentation and simulation. To this end, several measuring conditions have been contemplated, leading to 5 different tests. Table II summarizes all them, detailing their conditions and parameters set in circuit of Fig. 1, as well as the power values extracted from electrical measurements and simulations. As a T_{Ref}, the Peltier temperature T_P has been taken into account. In this sense, induction cooktops are conventionally located above an oven, running hot up to ambient temperatures in the range of 75 ºC [42]. T_P has been set for 50 ºC in order to reach close-to-application test conditions, an improvement of the S/N ratio of the camera and ensuring a proper stability of the Peltier cooling system. Tests A-I to A-III are conditions representative of domestic induction cooking appliances ($f_{Sw} > f_{res}$), while Tests A-IV and A-V provide another scenario when $f_{Sw} < f_{res}$. Moreover, the effect of C_{snub} in power losses calculation is also analyzed in both scenarios (see tests A-III and A-V).

As an example, all results corresponding to test A-I are presented when $P_{Sw} = 0$ and $P_{Sw} \neq 0$. Figs. 8 (a)-(b) depict when $P_{Sw} = 0$, the waveforms of V_{GE} (in black), I_C (in magenta), I_L (in green), V_{CE} (in blue) and power dissipated (P_{IGBT}, in orange). In the same conditions, Figs. 8 (c)-(d) present the IR results with the temperature average value at the surface of the IGBT ($T_{j,IGBT}$) and diode ($T_{j,Diode}$). Conversely, Figs. 8 (e)-(d) and Figs. 8 (f)-(g) provide the electrical and IR information for $P_{Sw} \neq 0$, respectively. As expected, the IGBT reach a higher temperature when $P_{Sw} \neq 0$ ($T_{j,IGBT}$ = 103 ºC) than in the case that $P_{Sw} = 0$ is considered ($T_{j,IGBT}$ = 81.49 ºC). Subtracting T_i to $T_{j,IGBT}$ and considering $R_{th(j\text{-}P)}$ previously measured, $P_{On} = 14.92$ W, $P_{On} + P_{Sw} = 25.21$ W, and $P_{Sw} = 10.29$ W are inferred. In comparison to electrical measurements, i.e., $P_{On} = 12.15$ W, $P_{On} + P_{Sw} = 19.67$ W, and $P_{Sw} = 7.52$ W, slight differences are observed.

In general, the results of the power losses calculated from the electrical or IR measurements mainly differ when C_{snub} is considered in the test circuit. This is linked to the oscillations appearing in the DUT I_C waveform, which makes difficult ascertain to which component, i.e., IGBT or C_{snub}, the current is passing through. Moreover, some effects with the probes could also be responsible of such oscillations. Therefore, the proposed approach features a best performance than electrical measurements, as the die-level thermal monitoring is not affected for such electrical effects, showing a higher precision.

B. *Current Distribution Measurement at Die Level by IR-LIT*

In order to achieve a sufficiently high power dissipation, i.e., a high signal level, and a sufficiently low f_{lock}, i.e., strong S/N, the next analysis have been performed at low f_{Sw} = 8~9 kHz, in the range for motor drives or other home appliances, i.e. air conditioners, dishwashers, pumps, fans or washing machines. With regards to the IGBT, its gate is biased (V_{GE}) with a square wave between 0 V and 20 V. The rest of the test conditions are summarized in Table III.Fig. 9 depicts the current distribution obtained for tests B-I to B-IV. Despite a significant part of the chip is covered by the bonding wires, the thermal field is confined in two main zones clearly depicted in Fig.9. Moreover, a temperature increase is observed at the device terminations when no snubber is used, either for ZVS or Non-ZVS test conditions. Thanks to this, it can be identified that the device terminations are potential hotspots when hard switching test conditions are used.

When ZVS condition is applied, the use of C_{snub} does not affect the thermal behavior of the device since the current distribution remains the same in both cases, as shown in Fig. 9 (a)-(b). However, when ZVS condition is lost, the power dissipation is higher when C_{snub} is considered, since the turn-on commutation process of the IGBT is prolonged. This fact translates into a higher current concentration at the weakest parts of the device, that can be identified using lock-in techniques, as shown in Fig. 9 (c)-(d).

V. CONCLUSIONS

A new approach based on thermal measurements is proposed to determine at the die level, the power losses and current distribution in IGBTs driven with a soft-switching technique under a resonant load power, when functioning within and outside the ZVS condition. To this end, a test platform has been designed, which includes an IR camera and a specific test circuit. With the IR camera, the temperature on top the die surface has been averaged on the device surface (power losses determination) or postprocessed to extract the first harmonic of the thermal field by using lock-in detection strategies. The test circuit is based on a half-bridge resonant inverter with a flexible resistive and inductive load. Moreover, it selectively allows measuring $P_{\mathrm{On}} + P_{\mathrm{Sw}}$ or Pon alone. To carry out the IR thermal measurements, the inspected devices have been prepared and fully characterized. The top molding compound has been removed from the DUT without changing its characteristics. Moreover, the DUT has been electrically and thermally evaluated. To assess the IR experimental results, an accurate electro-thermal model of the test platform is presented and validated by electrical measurements.

From IR and electrical measurements comparison, the inclusion of C_{snub} in the test circuit influences in the measurement of the power losses. Furthermore, the first spectral component of the thermal field at f_{Sw} shows current crowding phenomena close to the wire bondings. Moreover, when C_{snub} is not used, a temperature increase is observed at the edge termination of the device either for ZVS or non-ZVS test conditions used. Within ZVS condition, the inclusion of C_{snub} does not affect the thermal behavior of the device, but when outside, the power dissipated is higher leading to the appearance of hot spots.

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APPENDIX

Impact factor

[1] M. Fernández, X. Perpiñà, J. Rebollo, M. Vellvehi, D. Sánchez, T. Cabeza, S. Llorente, and X. Jordà, "Solid State Relay Solutions for Induction Cooking Applications based on Advanced Power Semiconductor Devices," *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2018.2838093. (In press). (Impact Factor: 7.050) URL: https://ieeexplore.ieee.org/document/8365104/

- Journal: IEEE Transactions on Industrial Electronics.
- Status: In press (available online).
- Impact Factor: 7.050.
- Categories:
  - Automation & Control Systems - Q1 - 2/61.
  - Engineering, Electrical & Electronic - Q1 - 13/260.
  - Instruments & Instrumentation - Q1 - 1/61.
- Acceptance Letter: located at the end of this section.

[2] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, X. Jordà, and M. Tack, "P-GaN HEMTs Drain and Gate Current Analysis Under Short-Circuit," *IEEE Electron Device Letters*, vol. 38, no. 4, pp. 505-508, April 2017, doi: 10.1109/LED.2017.2665163.
(Impact Factor: 3.433) URL: https://ieeexplore.ieee.org/document/7845577/

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  - Engineering, Electrical & Electronic - Q1 - 53/260

[3] M. Fernández, X. Perpiñà, J. Roig, M. Vellvehi, F. Bauwens, M. Tack, and X. Jordà, "Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9012-9022, Nov. 2017, doi: 10.1109/TIE.2017.2719599.
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    - Instruments & Instrumentation - Q1 - 1/61.

Co-authored works

The PhD student is the main inventor of the following patents, but the authors were listed in alphabetical order.

[1] T. Cabeza, M. Fernández, X. Jordà, S. Llorente, I. Millán, X. Perpiñà, D. Sánchez, and M. Vellvehi, "Dispositivo de aparato doméstico", Application number: P201631613 (19.12.2016), Publication number: ES2673129 A1 (19.06.2018).

[2] T. Cabeza, M. Fernández, X. Jordà, S. Llorente, I. Millán, X. Perpiñà, D. Sánchez, and M. Vellvehi, "Haushaltsgerätevorrichtung", Application number: DE201710222394 (11-12-2017), Priority number: ES20160031613 (19.12.2016).

Acceptance letters for publications in press

Fecha: 29/04/18 [16:32:22 CEST] **De:** Transactions on Industrial Electronics <onbehalfof@manuscriptcentral.com> **Para:** jacobs.s@ieee.org **Asunto:** IEEE Transactions on Industrial Electronics - Manuscript No. 18-TIE-0489.R1 Christian-Albrechts-Universität zu Kiel, Kiel, Germany, 29-Apr-2018

Dear Authors (CC to Associate Editor, Reviewers),

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Based on the opinions of the reviewers and the Associate Editor in charge, your manuscript has been accepted for publication in the IEEE Transactions on Industrial Electronics. Please accept our congratulations!

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Encl.: Reviewer: 2

Comments to the Author Thank you for your effort! For WBG devices, please add the latest references on bidirectional switches, such as: U. Raheja et al., "Applications and characterization of four quadrant GaN switch," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 1967-1975. As for the snubber, if the solution is to switch at zero current, please give a brief description on the requirements of detection citcuit. For example, how much current will be recognized as zero current by the detection circuit? 1A? 1mA? And, how much delay will the detection cause? 10us? 10ns? An estimation is good enough.

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Escuela de Doctorado
Universidad Zaragoza

RENUNCIA DE LOS COAUTORES DE LOS TRABAJOS PRESENTADOS COMO PARTE DE UNA TESIS DOCTORAL EN LA MODALIDAD DE COMPENDIO DE PUBLICACIONES

1.- Datos personales del coautor

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2.- Tesis Doctoral

Título: TOWARDS A MORE FLEXIBLE, SUSTAINABLE, EFFICIENT AND RELIABLE INDUCTION COOKING: A POWER SEMICONDUCTOR DEVICE PERSPECTIVE

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Programa de doctorado: INGENIERÍA ELECTRÓNICA

3.- Publicaciones que formarán parte de la tesis y de las que el firmante es coautor

1. "Solid State Relay Solutions for Induction Cooking Applications based on Advanced Power Semiconductor Devices", Manuel Fernández, Xavier Perpiñà, José Rebollo, Miquel Vellvehi, David Sánchez, Tomás Cabeza, Sergio Llorente y Xavier Jordà. IEEE Transactions on Industrial Electronics. DOI: 10.1109/TIE.2018.2838093. 24 Mayo 2018. Factor impacto: 7.168 (2016) y 7.829 (5 años). Categorías: {Automation & Control Systems - Q1 - 1/60}, {Engineering, Electrical & Electronic - Q1 - 12/262} y {Instruments & Instrumentation - Q1 - 1/58}.

2. "Analysis of bidirectional switch solutions based on different power devices", Manuel Fernández, Xavier Perpiñà, Miquel Vellvehi, David Sánchez, Xavier Jordà, José Millán, Tomás Cabeza y Sergio Llorente. 2017 Spanish Conference on Electron Devices (CDE). DOI: 10.1109/CDE.2017.7905220. 8-10 Feb. 2017.

3 y 4. Patentes: "Dispositivo de aparato de cocción por inducción con al menos una unidad de conexión", y "Haushaltsgerätevorrichtung", Tomás Cabeza, Manuel Fernández, Xavier Jordà, Sergio Llorente, Ignacio Millán, Xavier Perpiñà, David Sánchez y Miquel Vellvehi. Nºs de publicación: ES2673129 y DE102017222394, respectivamente. Nºs de solicitud: 201631613 y DE201710222394, respectivamente.

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Bellaterra 02/07/2018

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RENUNCIA DE LOS COAUTORES DE LOS TRABAJOS PRESENTADOS COMO PARTE DE UNA TESIS DOCTORAL EN LA MODALIDAD DE COMPENDIO DE PUBLICACIONES

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2.- Tesis Doctoral

Título: TOWARDS A MORE FLEXIBLE, SUSTAINABLE, EFFICIENT AND RELIABLE INDUCTION COOKING: A POWER SEMICONDUCTOR DEVICE PERSPECTIVE

Autor: MANUEL FERNÁNDEZ MARTÍNEZ

Programa de doctorado: INGENIERÍA ELECTRÓNICA

3.- Publicaciones que formarán parte de la tesis y de las que el firmante es coautor

1. "Solid State Relay Solutions for Induction Cooking Applications based on Advanced Power Semiconductor Devices", Manuel Fernández, Xavier Perpiñà, José Rebollo, Miquel Vellvehi, David Sánchez, Tomás Cabeza, Sergio Llorente y Xavier Jordà. IEEE Transactions on Industrial Electronics. DOI: 10.1109/TIE.2018.2838093. 24 Mayo 2018. Factor impacto: 7.168 (2016) y 7.829 (5 años). Categorías: {Automation & Control Systems - Q1 - 1/60}, {Engineering, Electrical & Electronic - Q1 - 12/262} y {Instruments & Instrumentation - Q1 - 1/58}.

2. "Analysis of bidirectional switch solutions based on different power devices", Manuel Fernández, Xavier Perpiñà, Miquel Vellvehi, David Sánchez, Xavier Jordà, José Millán, Tomás Cabeza y Sergio Llorente. 2017 Spanish Conference on Electron Devices (CDE). DOI: 10.1109/CDE.2017.7905220. 8-10 Feb. 2017

3. "Analysis of Solid State Relay Solutions Based on Different Semiconductor Technologies". Autores: Manuel Fernández, Xavier Perpiñà, Miquel Vellvehi, Xavier Jordà, Tomás Cabeza y Sergio Llorente. Conferencia: 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe). DOI: 10.23919/EPE17ECCEEurope.2017.8099012. 11-14 Sept. 2017.

4 y 5. Patentes: "Dispositivo de aparato de cocción por inducción con al menos una unidad de conexión", y "Haushaltsgerätevorrichtung", Tomás Cabeza, Manuel Fernández, Xavier Jordà, Sergio Llorente, Ignacio Millán, Xavier Perpiñà, David Sánchez y Miquel Vellvehi. Nºs de publicación: ES2673129 y DE102017222394, respectivamente. Nºs de solicitud: 201631613 y DE201710222394, respectivamente.

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