Escuela Universitaria Politécnica - La Almunia
Centro adscrito
Universidad Zaragoza

ESCUELA UNIVERSITARIA POLITÉCNICA

DE LA ALMUNIA DE DOÑA GODINA (ZARAGOZA)

ANEXOS

Sistema de seguridad con reconocimiento facial aplicado al acceso a un bloque de apartamentos

Security system based on facial recognition for access to apartment building

424.19.16

Autor: Luis Arbós Gómez

Director: Javier Esteban Escaño

Fecha: 22/09/2020

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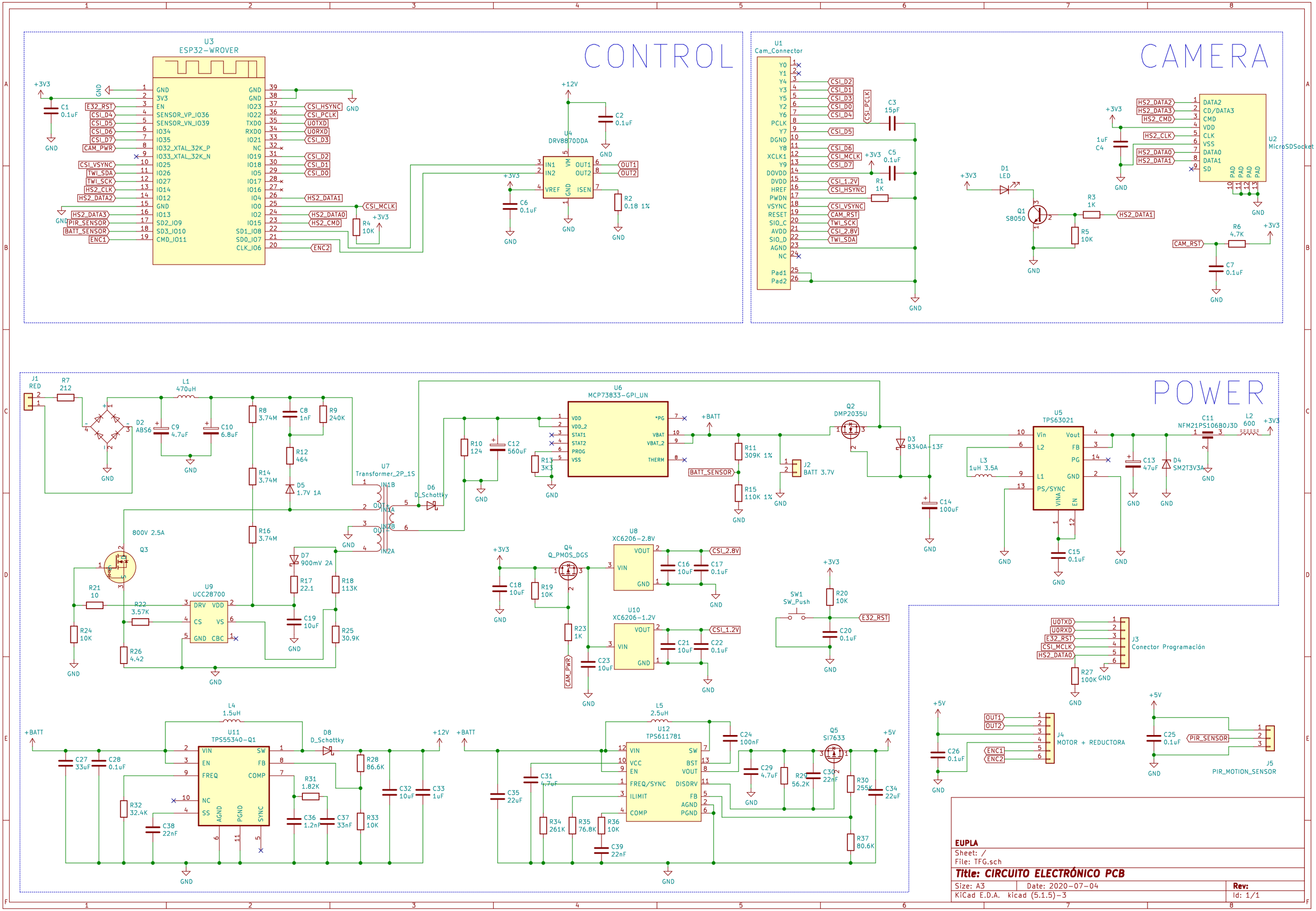
ANEXO 1. PLANOS


CONTROL
U3
ESP32-WROVER
U4
DRV8870DDA
CAMERA
U1
Cam_Connector
U2
MicroSDSocket
D1
LED
Q1
S8050
POWER
J1
RED
D2
ABS6
U7
Transformer_2P_1S
U6
MCP73833-GPI_UN
Q2
DMP2035U
D3
B340A-13F
U5
TPS63021
D4
SM2T3V3A
Q3
U9
UCC28700
D7
900mV 2A
Q4
Q_PMOS_DGS
U8
XC6206-2.8V
U10
XC6206-1.2V
SW1
SW_Push
J3
Conector Programación
J4
MOTOR + REDUCTORA
J5
PIR_MOTION_SENSOR
U11
TPS55340-Q1
U12
TPS611781
Q5
SI7633
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Date: 2020-07-04
Rev:
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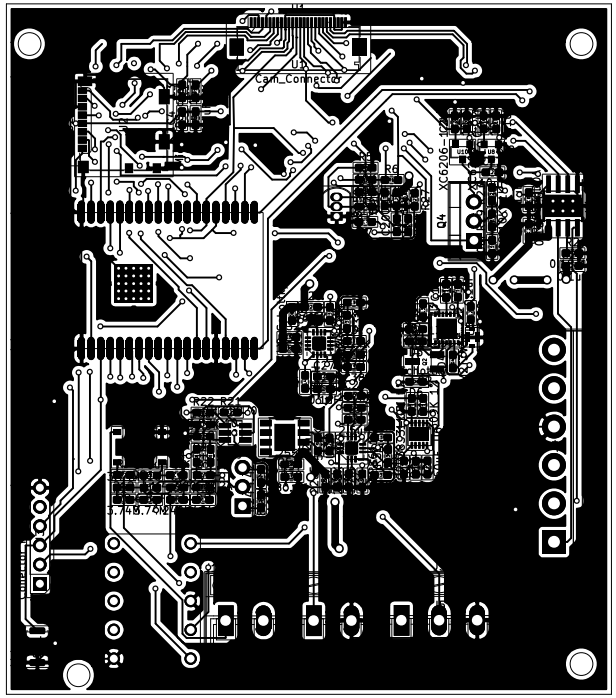

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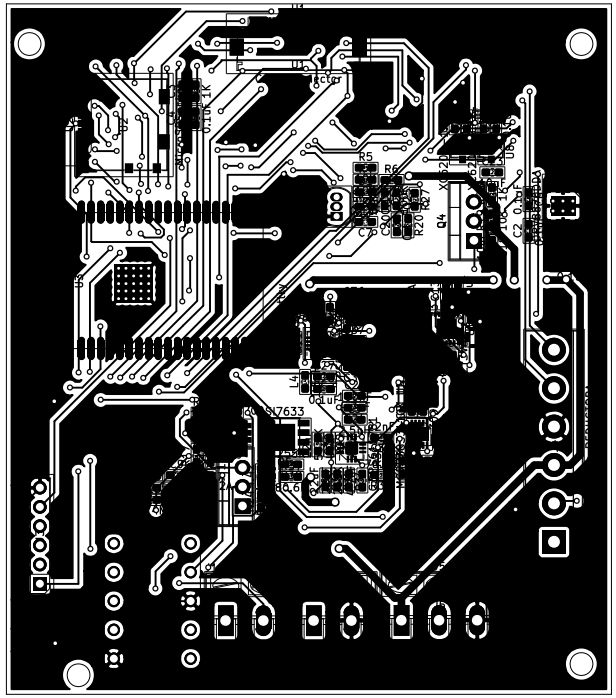

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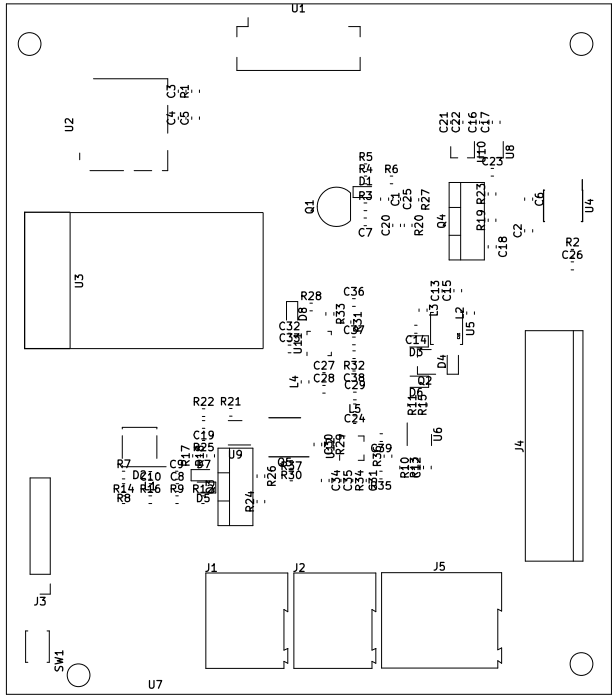

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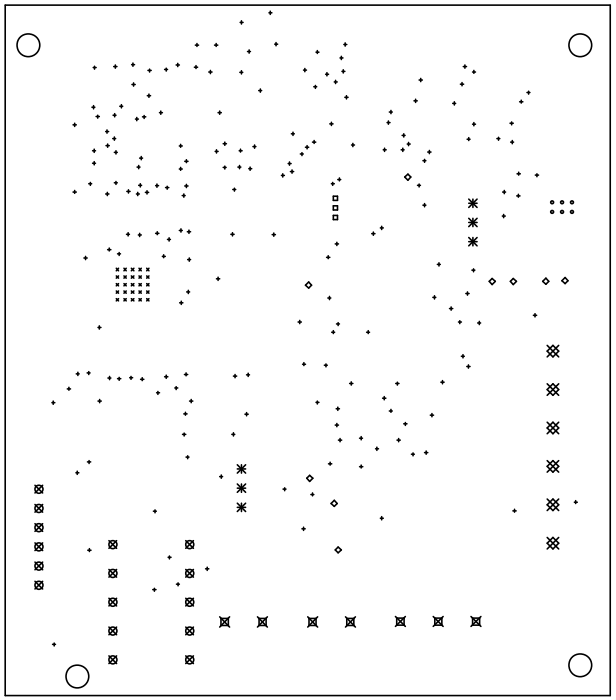

Drill Map:

- 0.30mm / 0.012" (25 holes)
- 0.33mm / 0.013" (6 holes)
- 0.40mm / 0.016" (199 holes)
- 0.75mm / 0.030" (3 holes)
- 0.80mm / 0.031" (9 holes)
- 1.00mm / 0.039" (16 holes)
- 1.10mm / 0.043" (6 holes)
- 1.32mm / 0.052" (7 holes)
- 1.52mm / 0.060" (6 holes)

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Size: A4	Date: 2020-08-28	Rev:
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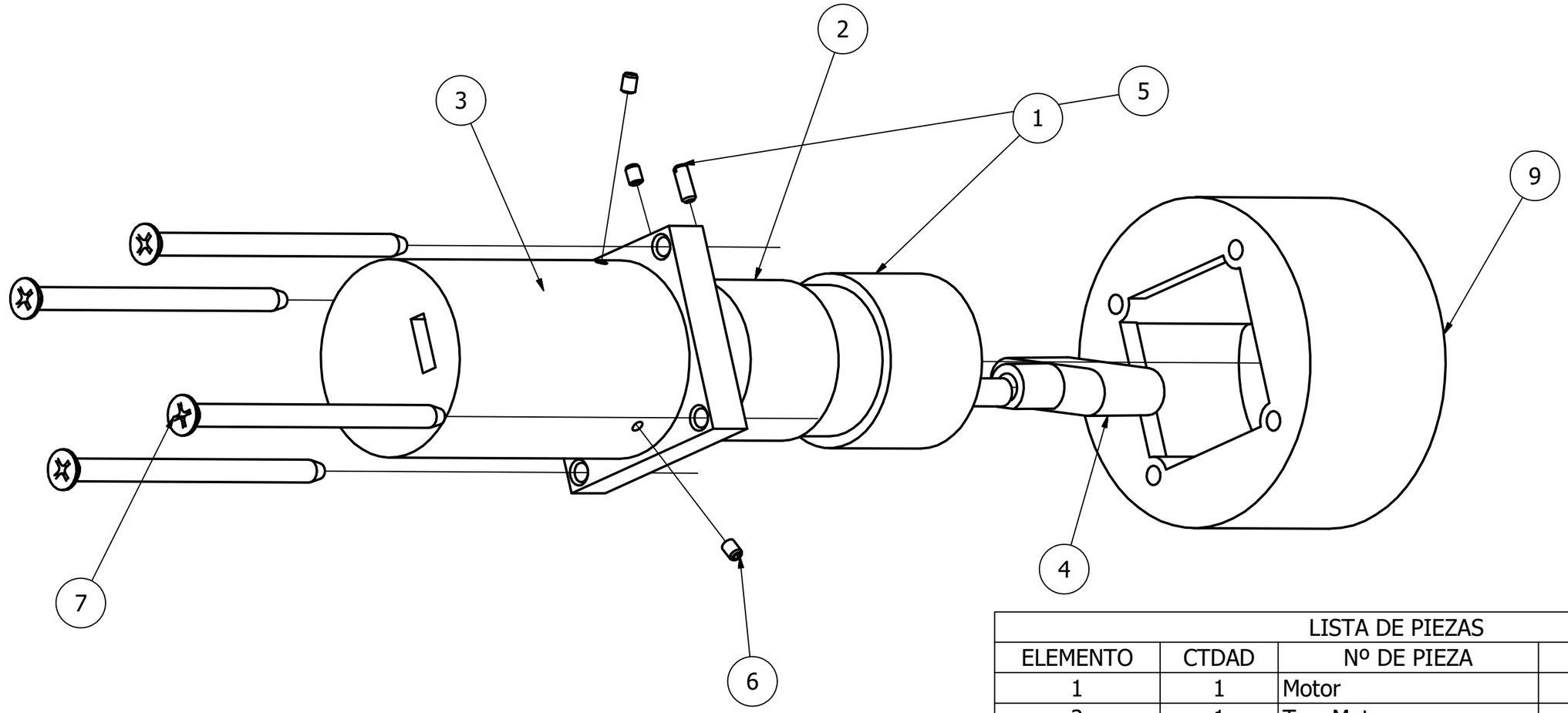


LISTA DE PIEZAS			
ELEMENTO	CTDAD	Nº DE PIEZA	DESCRIPCIÓN
1	1	Motor	
2	1	TapaMotor	
3	1	Cobertura Motor	
4	1	Extremo_Polivalente	
5	1	Screw GB/T 878 M3 x 8	Slotted headless screws with shank
6	4	AS 1421 - M3 x 4 Punta plana	Tornillos ISO métricos sin cabeza con hueco hexagonal
7	4	ANSI B18.6.4 - Nº 10 - 16 - 3	Tornillo de cabeza plana avellanada con hueco cruciforme - Tipo BF - Tipo I
9	1	CoberturtaAuxiliar	

Observaciones Generales

Proyecto: Diseño de un Sistema de Apertura Alternativo
Palabras clave: Sistema de Seguridad
Empresa: Escuela Universitaria Politécnica La Almunia
Estado del proyecto: En curso
Versión: V7

Observaciones de plano

Plano nº: 1 **de:** 1
Formato: A3
Coment:

	Fecha	Nombre
Dibujado	28/08/2020	L. Arbós Gómez
Comprobado		
Idem.s.normas		

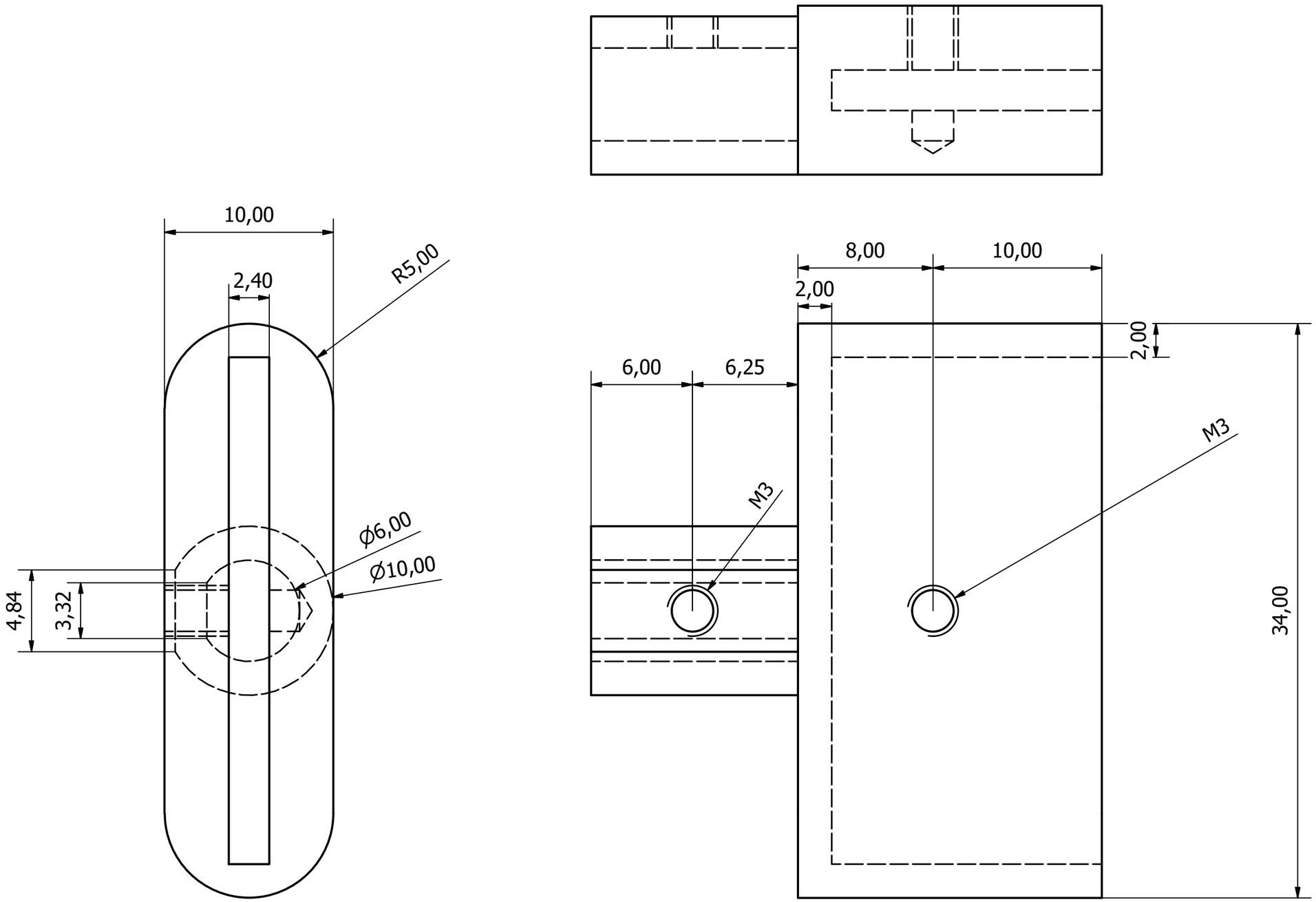
ESCALA 1:1

eupla
ESCUELA UNIVERSITARIA POLITECNICA
La Almunia de Dª Godina -ZARAGOZA-

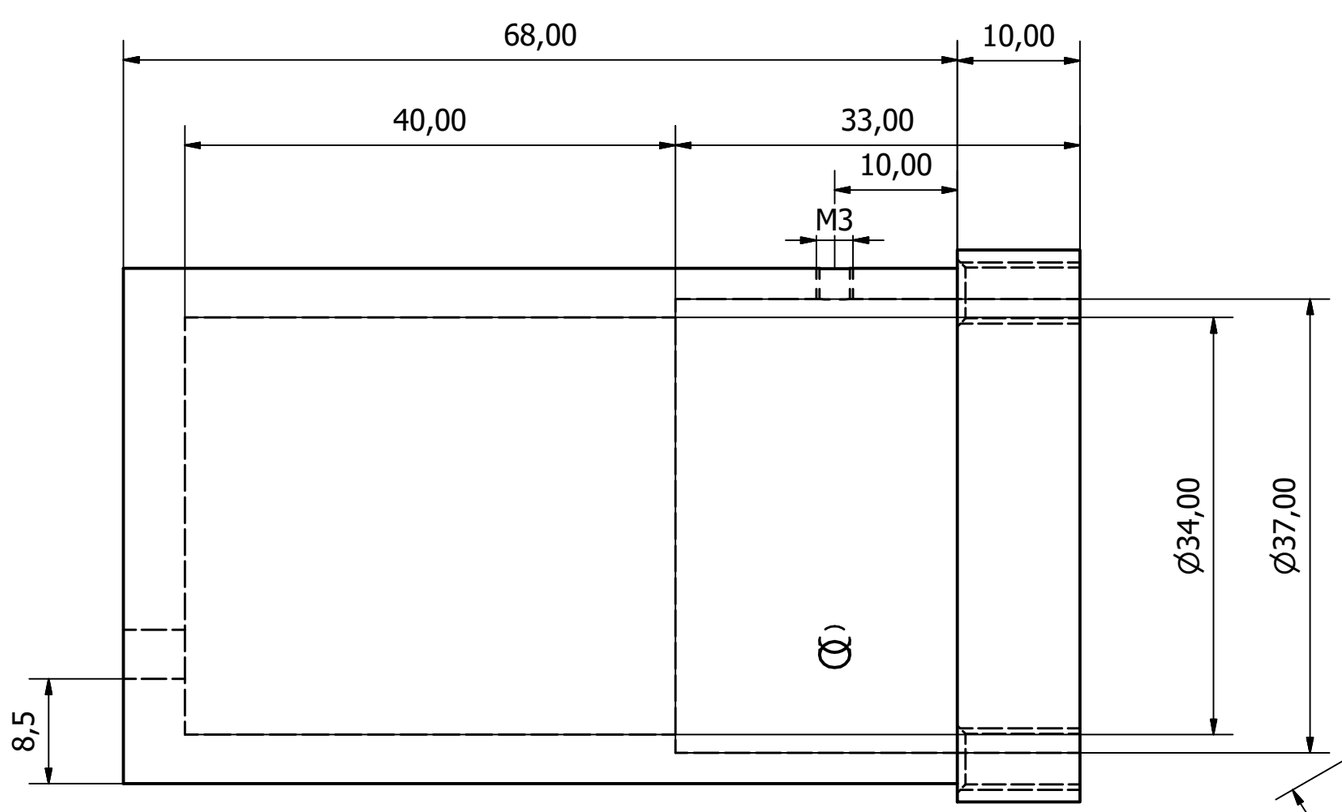
Sistema de Apertura

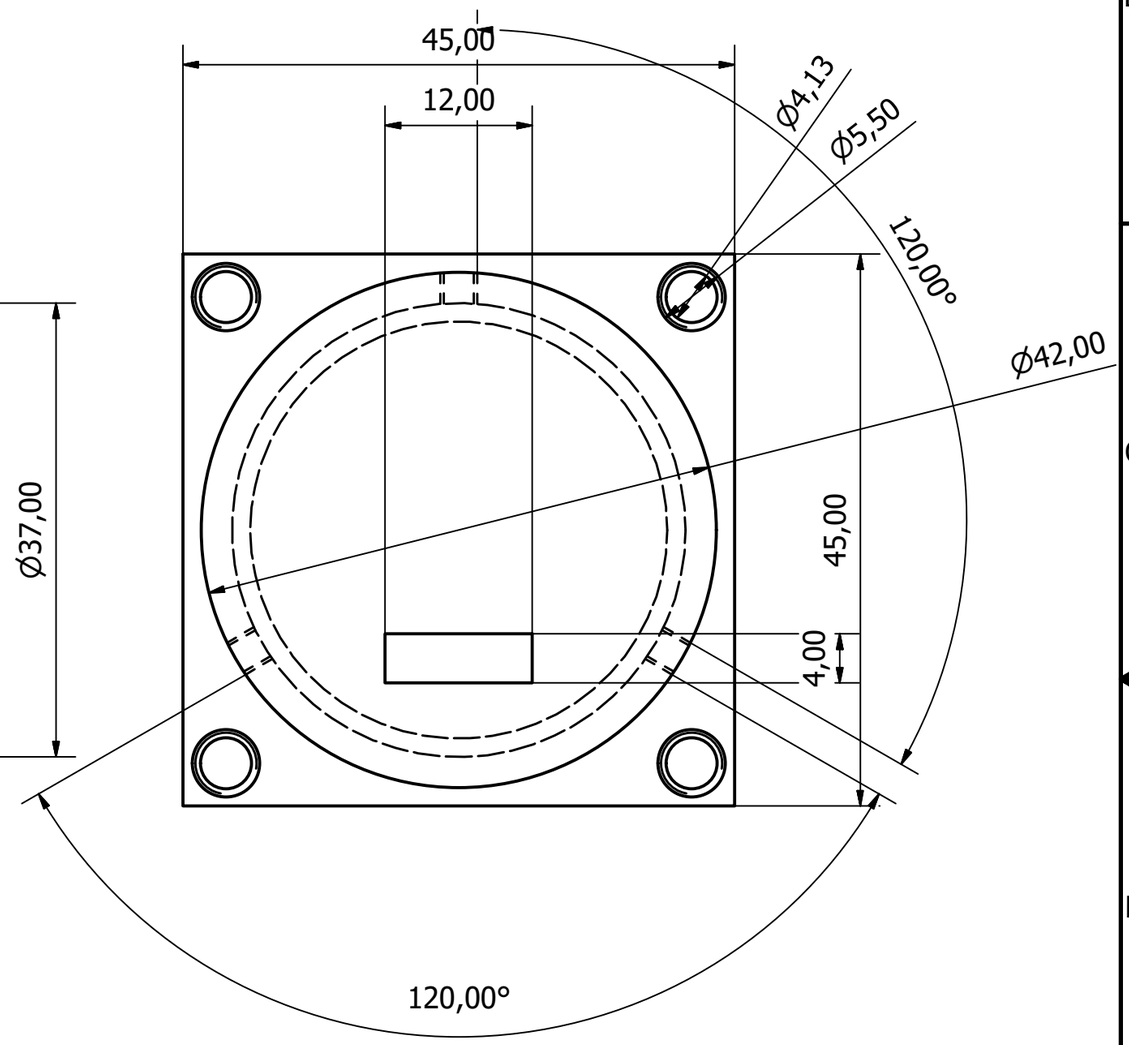
Despiece

Nº P.: 424.19.16.01
Nº O.: 424.19.16
Nom.Ar.: Ensamblaje.idw

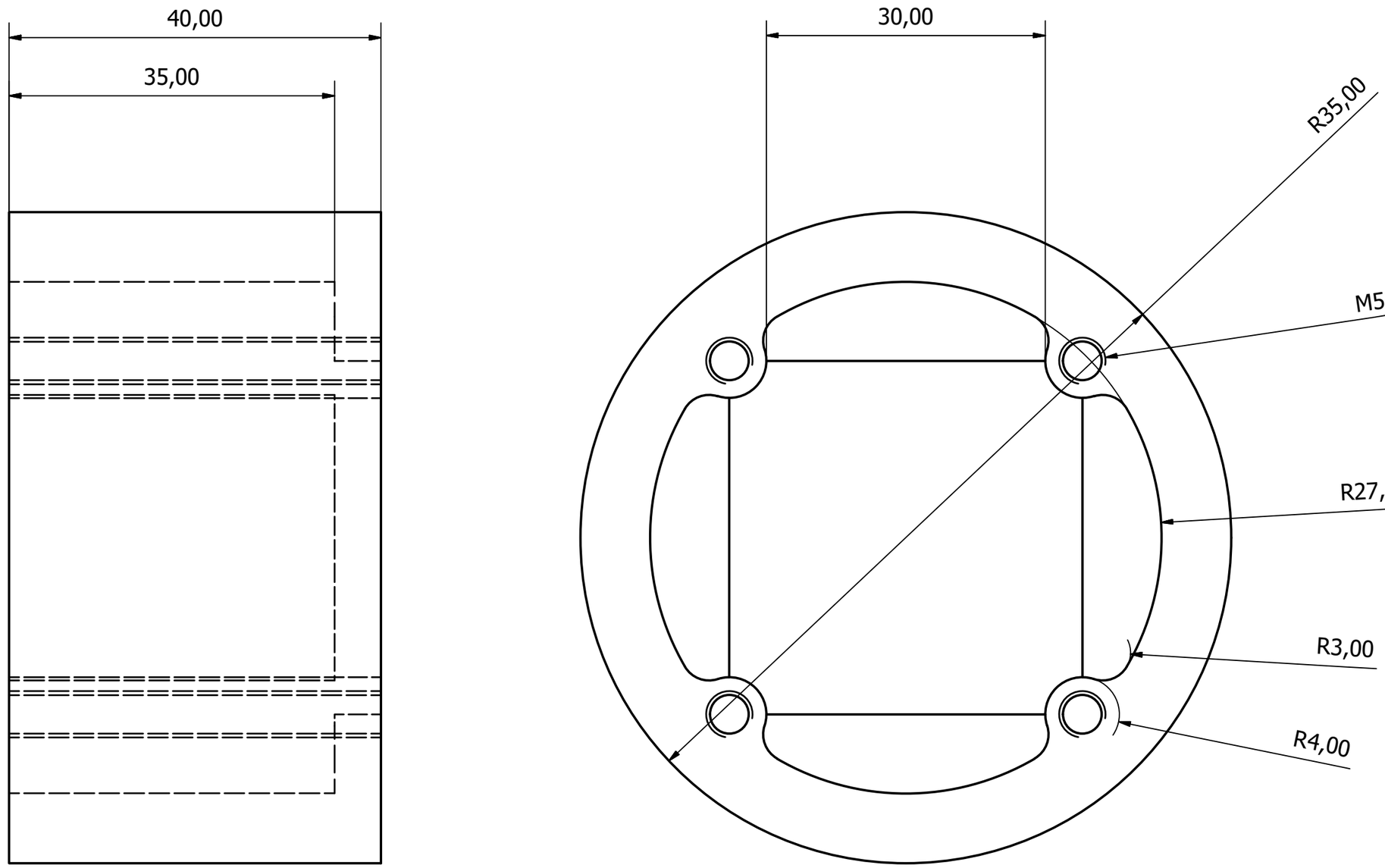


Observaciones Generales	Observaciones de plano		Fecha	Nombre		eupla
Proyecto: Diseño de un Sistema de Apertura Alternativo	**Plano nº:** 1 **de:** 1	**Dibujado**	28/08/2020	L. Arbós Gómez		ESCUELA UNIVERSITARIA POLITECNICA
Palabras clave: Sistema de Seguridad	**Formato:** A3	**Comprobado**				La Almunia de Dª Godina -ZARAGOZA-
Empresa: Escuela Universitaria Politécnica La Almunia	**Coment:**	**Idem.s.normas**				
Estado del proyecto: En curso		**ESCALA** 4:1	**Sistema de Apertura**			**Nº P.:** 424.19.16.02
Versión: V10			Pieza Polivalente de Agarre			**Nº O.:** 424.19.16
						Nom.Ar.: Extremo_Polivalente.dwg

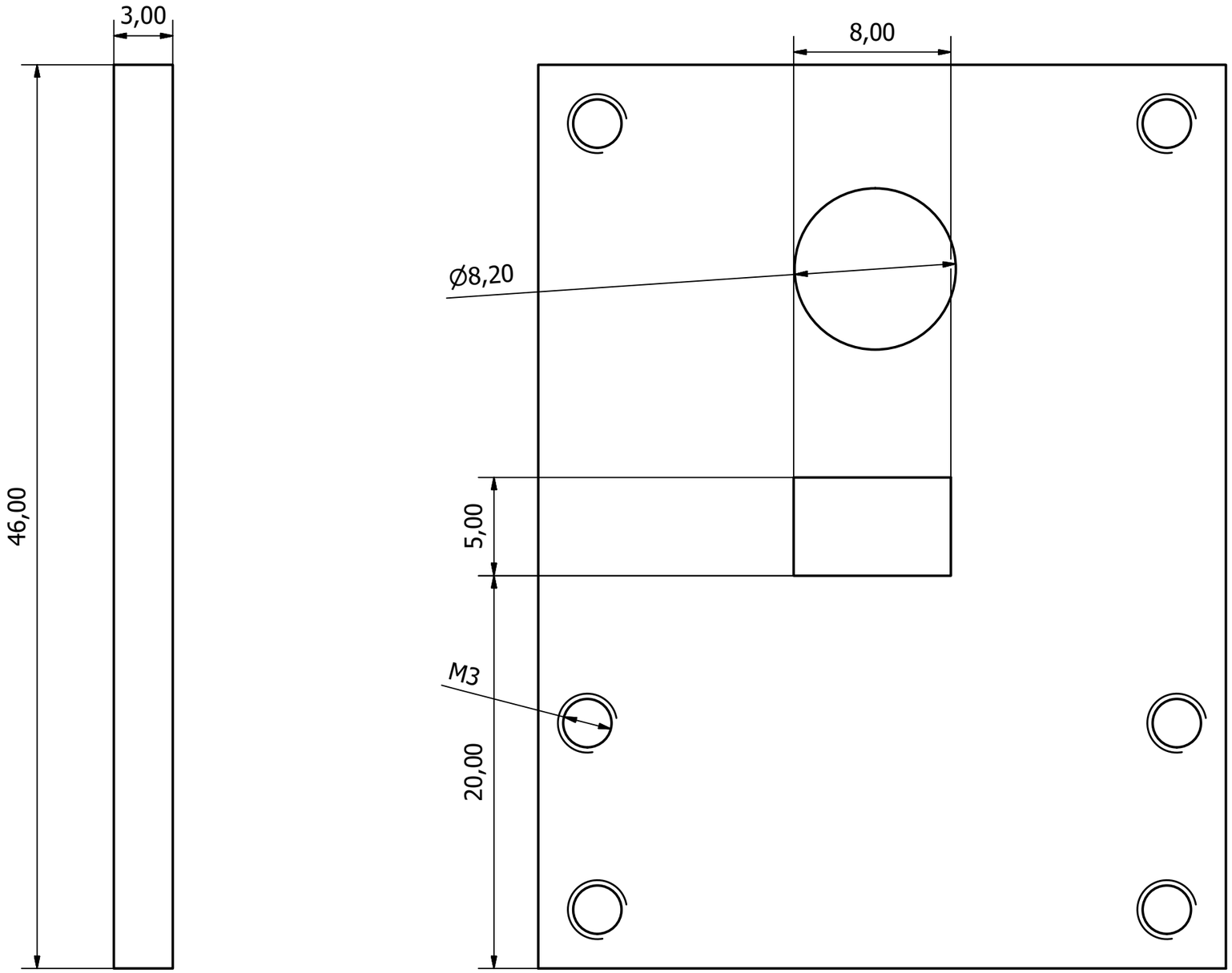




Observaciones Generales	Observaciones de plano		Fecha	Nombre		
Proyecto: Diseño de un Sistema de Apertura Alternativo **Palabras clave:** Sistema de Seguridad **Empresa:** Escuela Universitaria Politécnica La Almunia **Estado del proyecto:** En curso **Versión:** V13	**Plano nº:** 1 **de:** 1 **Formato:** A3 **Coment:**	**Dibujado**	28/08/2020	L. Arbós Gómez		eupla ESCUELA UNIVERSITARIA POLITECNICA La Almunia de Dª Godina -ZARAGOZA-
		Comprobado				
		Idem.s.normas				
		ESCALA 2:1	**Sistema de Apertura** Cobertura Motor			**Nº P.:** 424.19.16.03 **Nº O.:** 424.19.16 **Nom.Ar.:** Cobertura Motor.idw



Observaciones Generales	Observaciones de plano		Fecha	Nombre		
Proyecto: Diseño de un Sistema de Apertura Alternativo **Palabras clave:** Sistema de Seguridad **Empresa:** Escuela Universitaria Politécnica La Almunia **Estado del proyecto:** En curso **Versión:** V2	**Plano nº:** 1 **de:** 1 **Formato:** A3 **Coment:**	**Dibujado**	10/09/2020	L. Arbós Gómez		eupla ESCUELA UNIVERSITARIA POLITECNICA La Almunia de Dª Godina -ZARAGOZA-
		Comprobado				
		Idem.s.normas				
		ESCALA 2:1	**Sistema de Apertura** Cobertura Auxiliar			**Nº P.:** 424.19.16.04 **Nº O.:** 424.19.16 **Nom.Ar.:** CoberturtaAuxiliar.idw



Observaciones Generales	Observaciones de plano		Fecha	Nombre		
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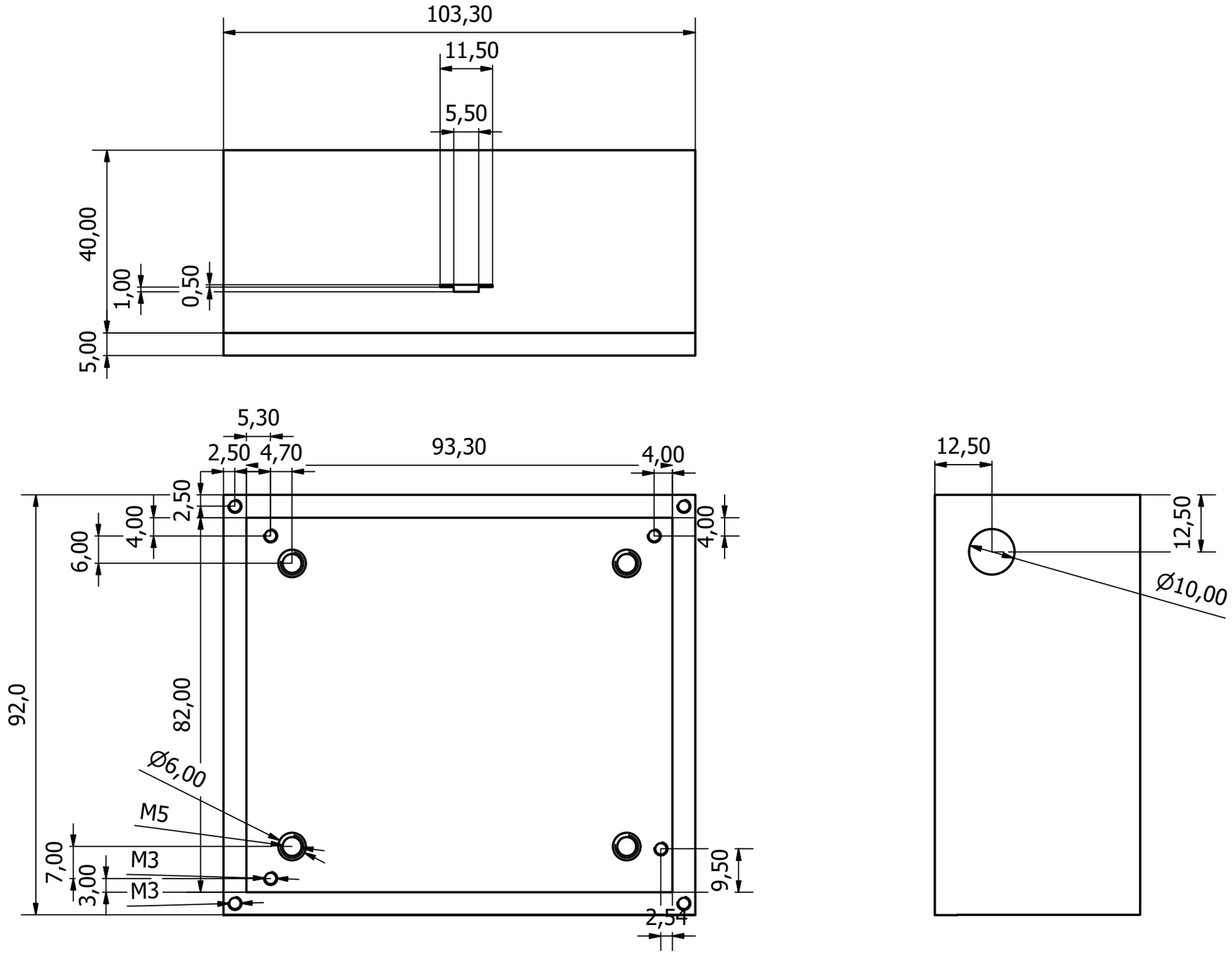
Palabras clave: Sistema de Seguridad	**Formato:** A3	**Comprobado**				ESCUELA UNIVERSITARIA POLITECNICA
Empresa: Escuela Universitaria Politécnica La Almunia	**Coment:**	**Idem.s.normas**				La Almunia de Dª Godina -ZARAGOZA-
Estado del proyecto: En curso		**ESCALA** 4:1	**Sistema de Apertura**			**Nº P.:** 424.19.16.05
Versión: V4			Pletina Soporte para la Cámara y el Sensor PIR			**Nº O.:** 424.19.16
						Nom.Ar.: Pletina Camara.idw



Observaciones Generales	Observaciones de plano		Fecha	Nombre
Proyecto: Diseño de un Sistema de Apertura Alternativo **Palabras clave:** Sistema de Seguridad **Empresa:** Escuela Universitaria Politécnica La Almunia **Estado del proyecto:** En curso **Versión:** V2	**Plano nº:** 1 **de:** 1 **Formato:** A3 **Coment:**	**Dibujado**	13/09/2020	L. Arbós Gómez
		Comprobado		
		Idem.s.normas		
		ESCALA 1:1	**Sistema de Apertura** Carcasa para la PCB	

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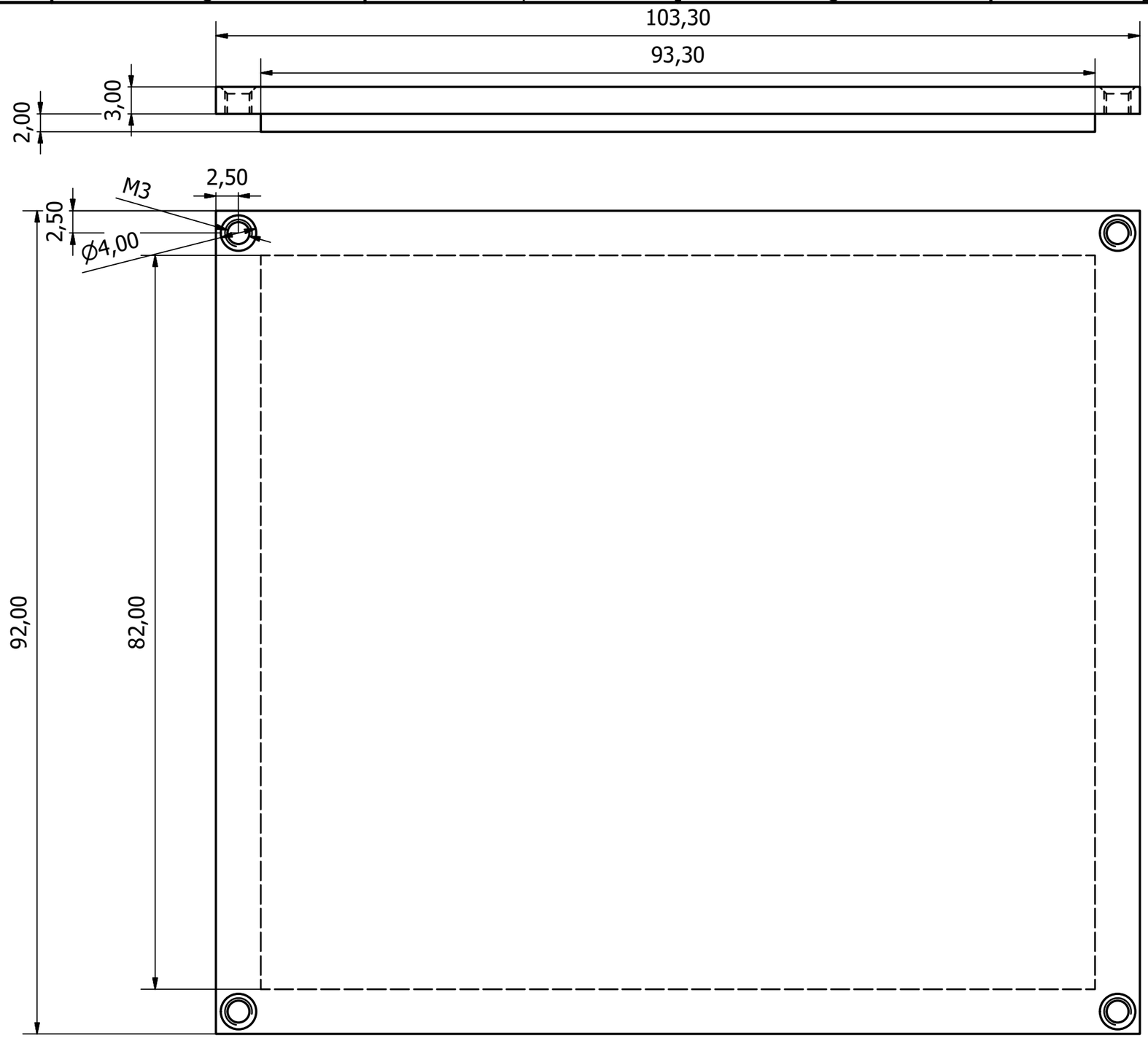
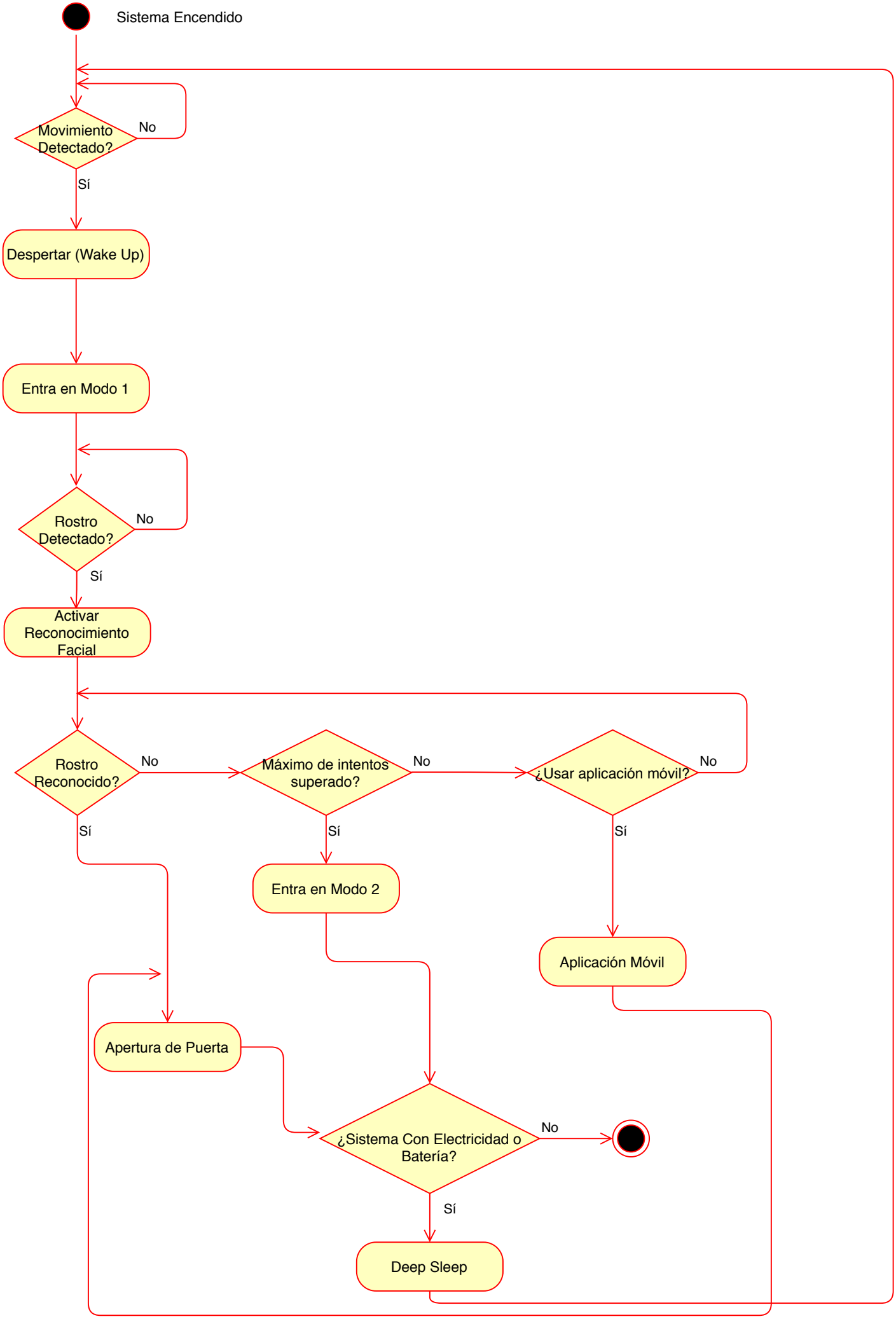
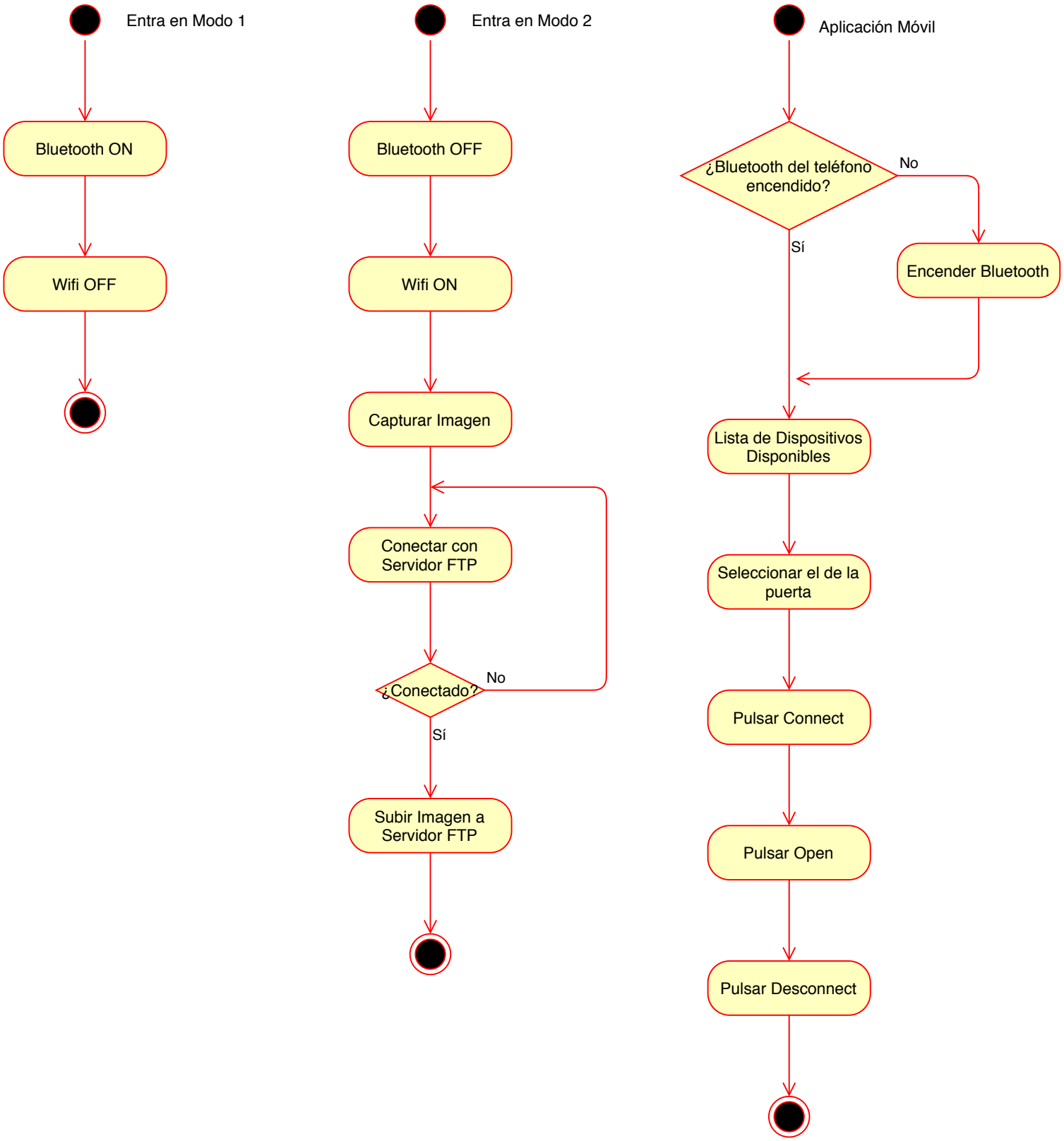
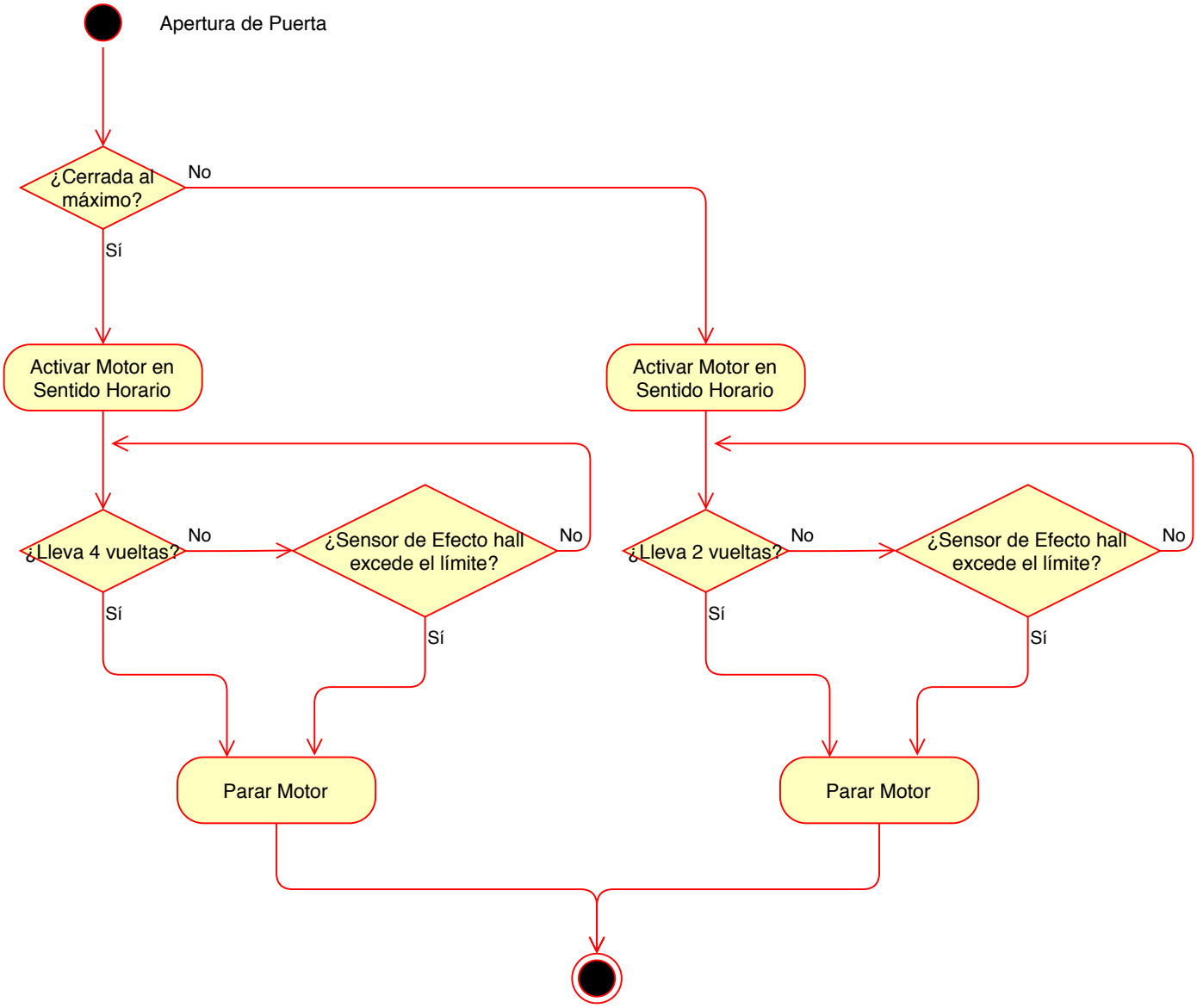
Nº P.: 424.19.16.06
Nº O.: 424.19.16
Nom.Ar.: Carcasa_PCB.idw



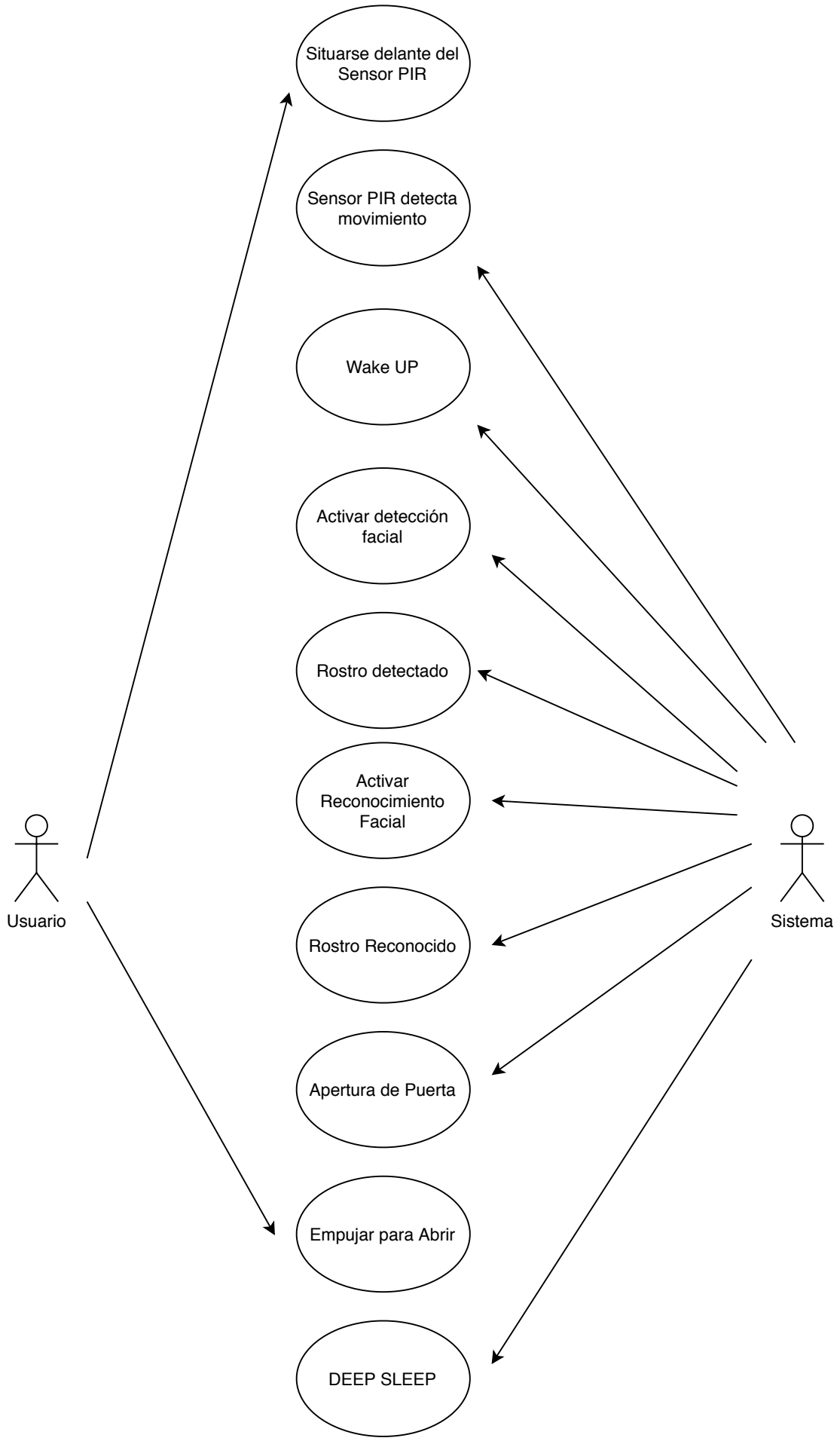
Observaciones Generales	Observaciones de plano		Fecha	Nombre		
Proyecto: Diseño de un Sistema de Apertura Alternativo	**Plano nº:** 1 **de:** 1	**Dibujado**	13/09/2020	L. Arbós Gómez		eupla
Palabras clave: Sistema de Seguriadad	**Formato:** A3	**Comprobado**				ESCUELA UNIVERSITARIA POLITECNICA
Empresa: Escuela Universitaria Politécnica La Almunia	**Coment:**	**Idem.s.normas**				La Almunia de Dª Godina -ZARAGOZA-
Estado del proyecto: En curso		**ESCALA** 2:1	**Sistema de Apertura**			**Nº P.:** 424.19.16.07
Versión: V3			Tapa de la Carcasa para la PCB			**Nº O.:** 424.19.16
						Nom.Ar.: Tapa_Carcasa_PCB.idw


Sistema Encendido
Movimiento Detectado?
No
Sí
Despertar (Wake Up)
Entra en Modo 1
Rostro Detectado?
No
Sí
Activar Reconocimiento Facial
Rostro Reconocido?
No
Máximo de intentos superado?
No
¿Usar aplicación móvil?
No
Sí
Sí
Sí
Entra en Modo 2
Aplicación Móvil
Apertura de Puerta
¿Sistema Con Electricidad o Batería?
No
Sí
Deep Sleep

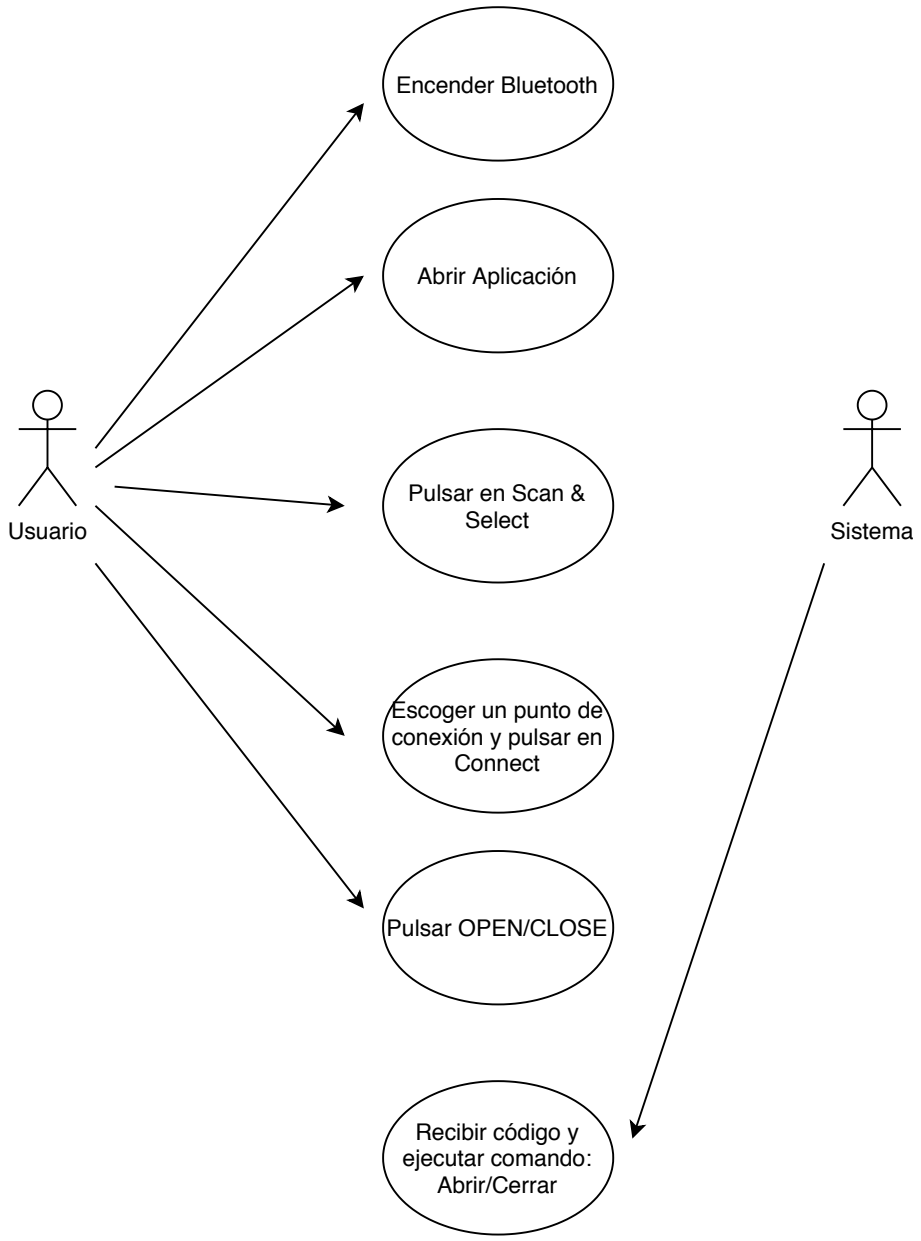

Entra en Modo 1
Bluetooth ON
Wifi OFF
Entra en Modo 2
Bluetooth OFF
Wifi ON
Capturar Imagen
Conectar con Servidor FTP
¿Conectado?
No
Sí
Subir Imagen a Servidor FTP
Aplicación Móvil
¿Bluetooth del teléfono encendido?
No
Sí
Encender Bluetooth
Lista de Dispositivos Disponibles
Seleccionar el de la puerta
Pulsar Connect
Pulsar Open
Pulsar Desconnect


Apertura de Puerta
¿Cerrada al máximo?
No
Sí
Activar Motor en Sentido Horario
Activar Motor en Sentido Horario
¿Lleva 4 vueltas?
No
¿Sensor de Efecto hall excede el límite?
No
Sí
Sí
¿Lleva 2 vueltas?
No
¿Sensor de Efecto hall excede el límite?
No
Sí
Sí
Parar Motor
Parar Motor

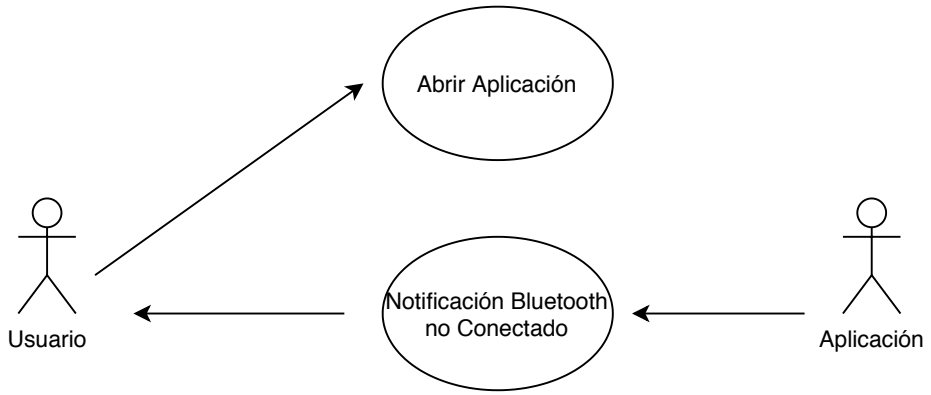
USO HABITUAL DEL SISTEMA



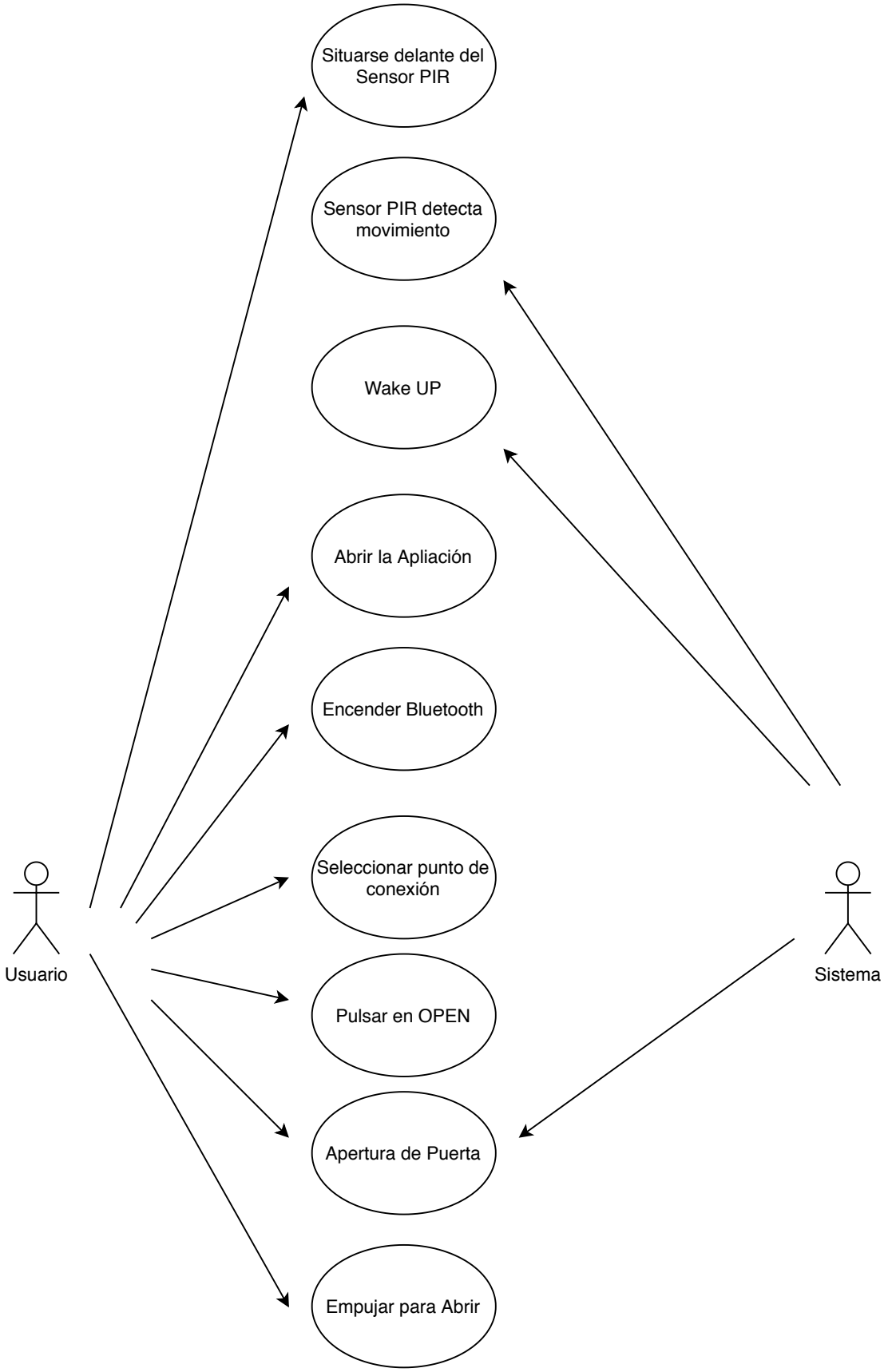
USO HABITUAL DE LA APLICACIÓN



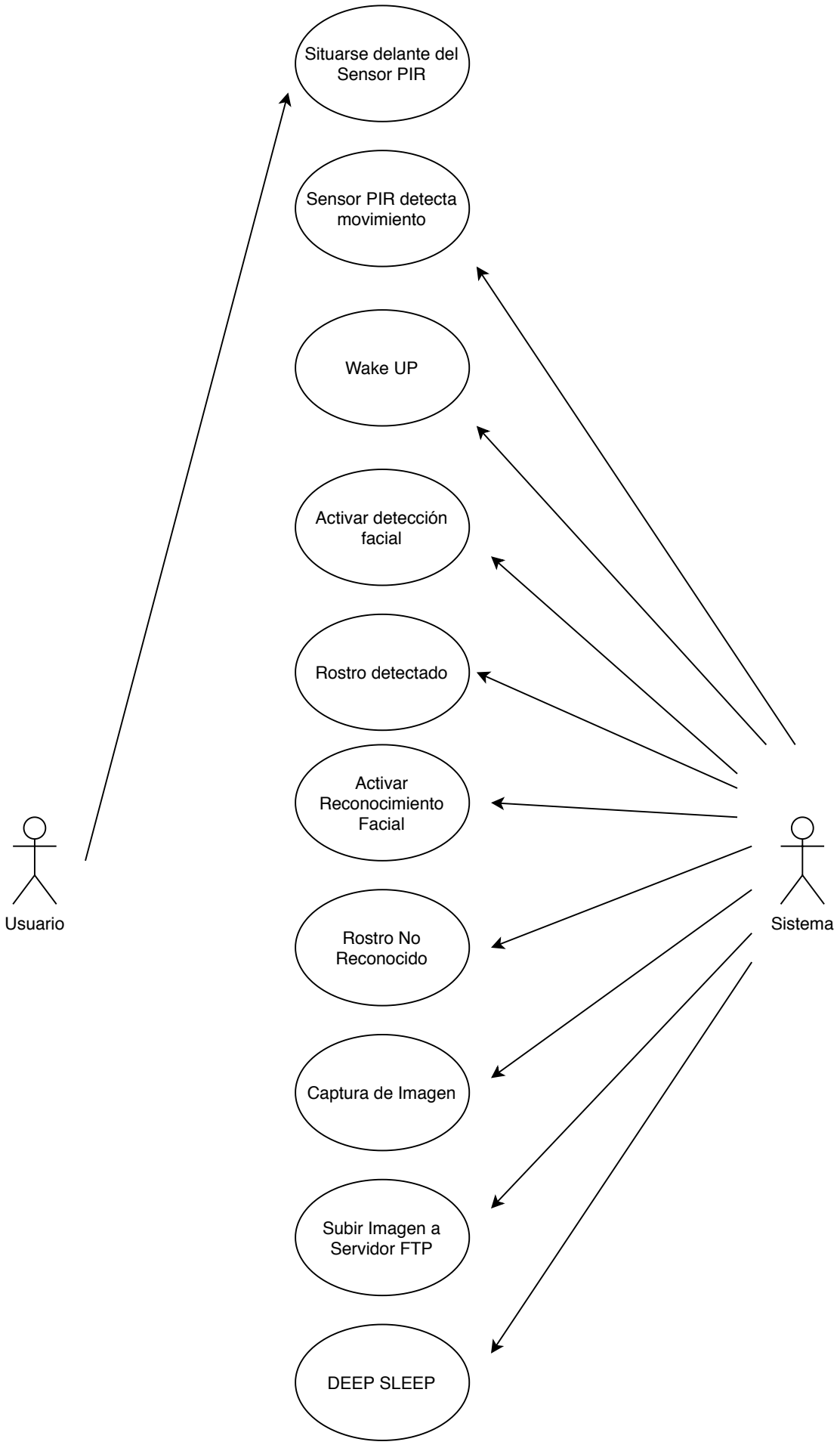
BLUETOOTH NO CONECTADO



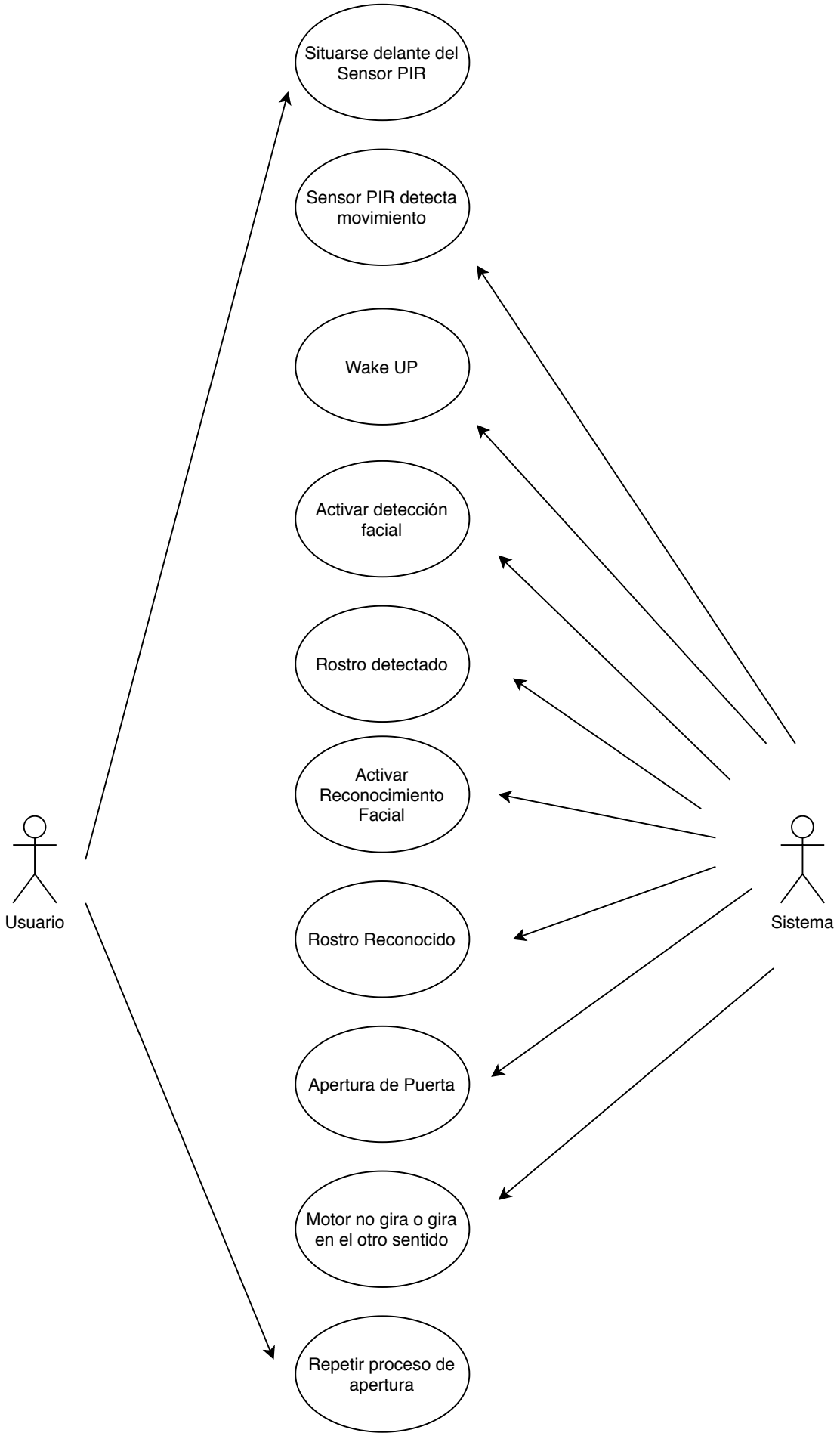
APERTURA CON LA APLICACIÓN



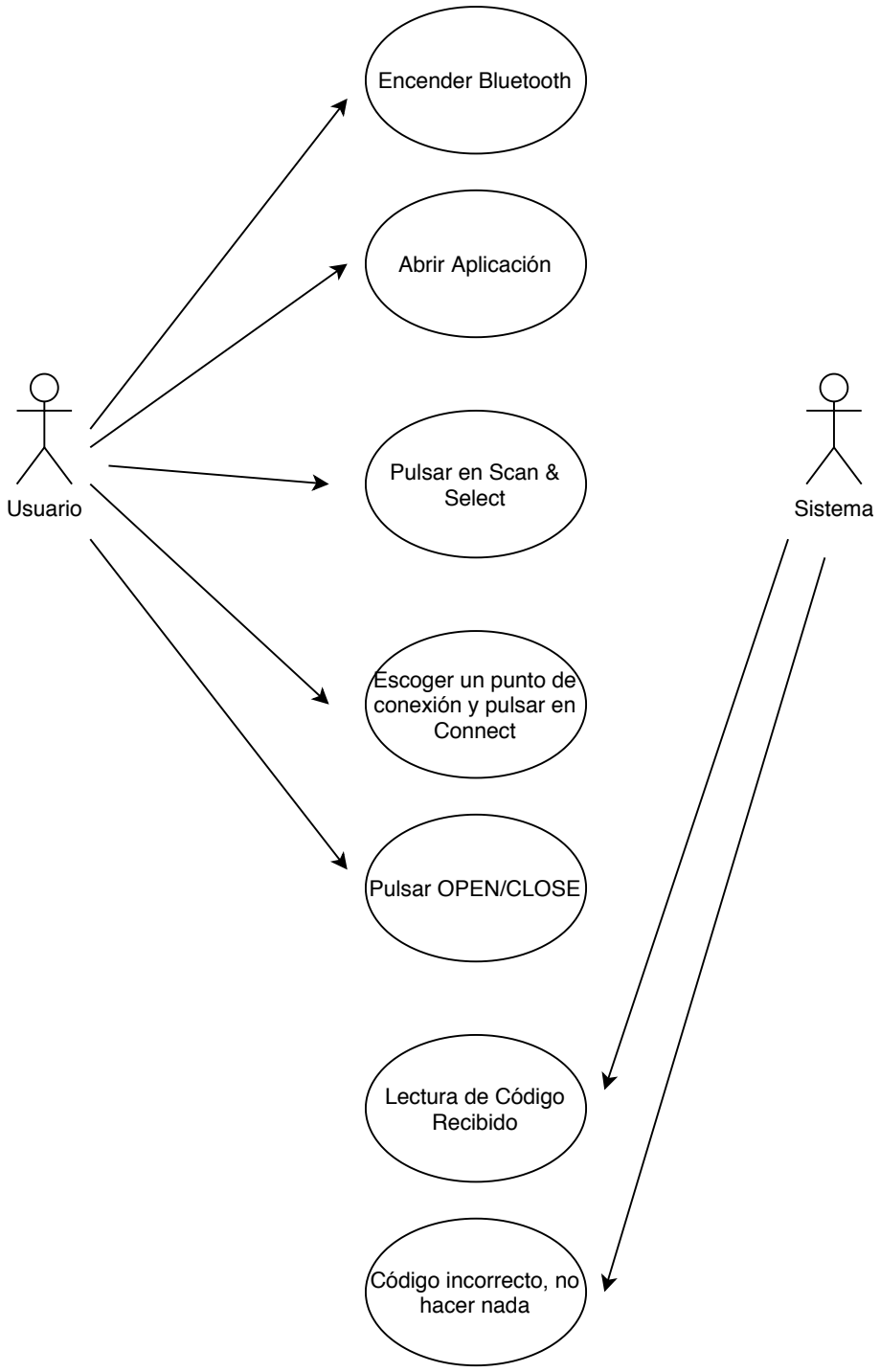
ROSTRO NO RECONOCIDO



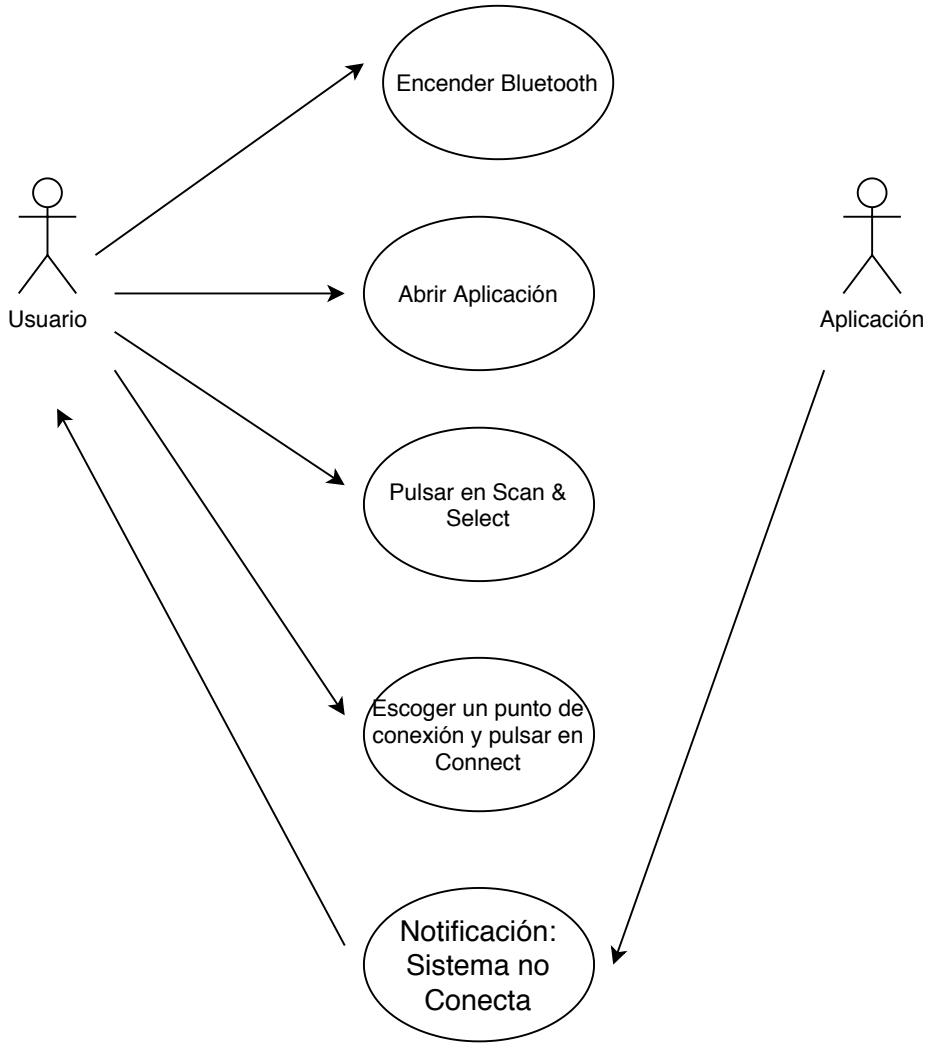
MOTOR GIRA AL REVÉS O NO GIRA



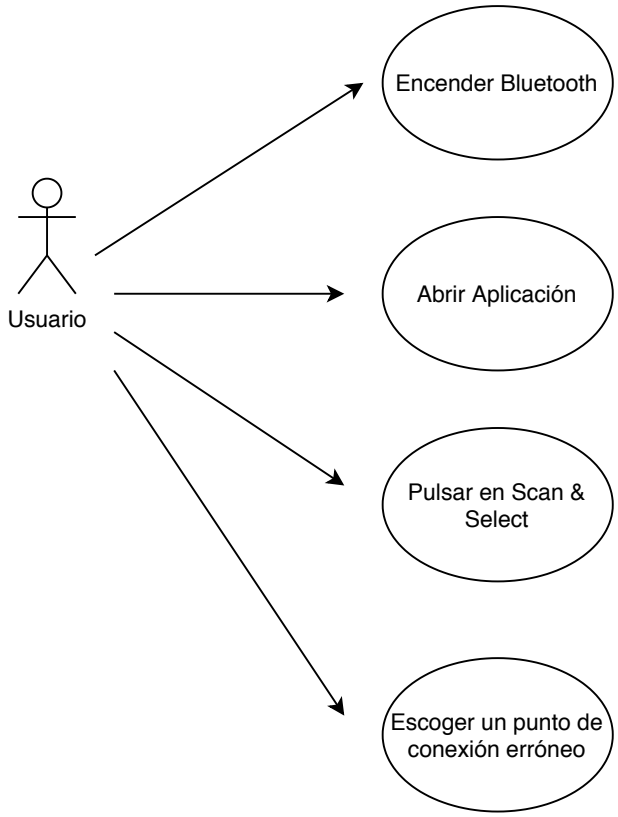
CÓDIGO ALFANUMÉRICO ERRÓNEO



NO CONECTA CON EL SISTEMA



EL USUARIO SE EQUIVOCA DE PUNTO DE CONEXIÓN



ANEXO 2. PRESUPUESTO

2.1. PLACA CIRCUITO IMPRESO (PCB)

En este anexo se recoge el presupuestado de la placa de circuito impreso con todos los componentes, desde condensadores, resistencias y bobinas, hasta el microcontrolador.

PRESUPUESTO DE LA PCB				
Condensadores:	**Cantidad**	**Valor**	**Precio Unitario (€)**	**Precio Total (€)**
C1, C2, C5, C6, C7, C15, C17, C20, C22, C24, C25, C26, C28	13	0.1uF	0.15	1.95
C3	1	15pF	0.29	0.29
C4, C33	2	1uF	0.12	0.24
C8	1	1nF	0.78	0.78
C9, C29, C31	3	4.7uF	0.36	1.08
C10	1	6.8uF	0.46	0.46
C11	1	NFM21PS106B0J3D	0.46	0.46
C12	1	560uF	0.86	0.86
C13	1	47uF	0.268	0.268
C14	1	100uF	0.102	0.102
C16, C18, C19, C21, C23, C32	6	10uF	0.164	0.984
C27	1	33uF	0.26	0.26

C30, C38, C39	3	22nF	0.704	2.112
C34, C35	2	22uF	0.508	1.016
C36	1	1.2nF	0.34	0.34
C37	1	33nF	0.642	0.642
Resistencias:	**Cantidad**	**Valor**	**Precio Unitario**	**Precio Total**
R1, R3, R23	3	1KΩ	0.011	0.033
R2	1	0.18Ω	1.35	1.35
R4, R5, R19, R20, R24, R33, R36	7	10KΩ	0.0239	0.1673
R6	1	4.7KΩ	0.106	0.106
R7	1	212	0.42	0.42
R8, R14, R16	3	3.74MΩ	0.156	0.468
R9	1	240KΩ	0.234	0.234
R10	1	124Ω	0.163	0.163
R11	1	309KΩ	0.124	0.124
R12	1	464Ω	0.178	0.178
R13	1	3.3KΩ	0.09	0.09
R15	1	110KΩ	0.102	0.102
R17	1	22.1Ω	0.13	0.13
R18	1	113KΩ	0.162	0.162
R21	1	10Ω	0.08	0.08

R22	1	3.57KΩ	0.24	0.24
R25	1	30.9KΩ	0.268	0.268
R26	1	4.42Ω	0.34	0.34
R27	1	100KΩ	0.03	0.03
R28	1	86.6KΩ	0.18	0.18
R29	1	56.2KΩ	0.16	0.16
R30	1	255KΩ	0.13	0.13
R31	1	1.82KΩ	0.162	0.162
R32	1	32.4KΩ	0.24	0.24
R34	1	261KΩ	0.125	0.125
R35	1	76.8KΩ	0.16	0.16
R37	1	80.6KΩ	0.192	0.192
Bobinas:	**Cantidad**	**Valor**	**Precio Unitario**	**Precio Total**
L1	1	470uH	1.55	1.55
L2	1	600nH	2.83	2.83
L3	1	1uH	1.45	1.45
L4	1	1.5uH	2.75	2.75
L5	1	2.5uH	1.98	1.98
Diodos:	**Cantidad**	**Valor**	**Precio Unitario**	**Precio Total**
D1	1	LED	0.24	0.24

D2	1	HD06T	0.398	0.398
D3	1	B340A-13F	0.42	0.42
D4	1	SM2Y3V3A	0.47	0.47
D5	1	MBRD835L	0.63	0.63
D6	1	SS24FL	0.18	0.18
D7	1	SK220A	0.1	0.1
D8	1	PR02	0.35	0.35
Transistores:	**Cantidad**	**Valor**	**Precio Unitario**	**Precio Total**
Q1	1	S8050	0.17	0.17
Q2	1	DMP2035U	0.35	0.35
Q3	1	SI7633DP	0.42	0.42
Q4	1	SI7633DP	0.42	0.42
Q5	1	SI7633	0.27	0.27
Botones:	**Cantidad**	**Valor**	**Precio Unitario**	**Precio Total**
SW1	1	-	0.22	0.22
Circuitos Integrados:	**Cantidad**	**Descripción**		**Precio Total**
U1	1	Cam Connector		3.21
U2	1	MicroSD Socket		2.73
U3	1	ESP32-Wrover		2.25
U4	1	DRV8870		0.65

U5	1	TPS63021	1.7
U6	1	MCP73833	0.87
U7	1	Transformador 2P1S	3.87
U8	1	XC6206-2.8V	1.14
U9	1	UCC28700	1.37
U10	1	XC6206-1.2V	1.45
U11	1	TPS55340-Q1	4.08
U12	1	TPS611781	1.8

2.2. MOTOR Y SOPORTE

PIEZA	Cantidad	Precio Unitario	Precio Total
Motor + Reductora + Enconder	1	11.25	11.25

Las piezas diseñadas, el soporte del motor, así como la pieza del extremo, con los tornillos no han sido incluidos en el presupuesto, porque al ser piezas diseñadas especialmente para este proyecto el precio es dependiente del material del que se fabrique.

El total del presupuesto sube hasta 69.30€. Cabe remarcar que este precio no incluye las piezas diseñadas, ni tampoco el montaje en sí de la placa ni del sistema en puerta, solo es un presupuesto de las piezas y componentes que contiene el sistema.

ANEXO 3. PROGRAMACIÓN

```
#include "BluetoothSerial.h"
#include "driver/rtc_io.h"
#include "soc/soc.h"          // Disable brownour problems
#include "soc/rtc_cntl_reg.h"  // Disable brownour problems

#include "Face_Recognition.h"

#if !defined(CONFIG_BT_ENABLED) || !defined(CONFIG_BLUEDROID_ENABLED)
#error Bluetooth is not enabled! Please run `make menuconfig` to and enable it
#endif

//Camera pins
#define PWDN_GPIO_NUM     32
#define RESET_GPIO_NUM    -1
#define XCLK_GPIO_NUM      0
#define SIOD_GPIO_NUM     26
#define SIOC_GPIO_NUM     27

#define Y9_GPIO_NUM       35
#define Y8_GPIO_NUM       34
#define Y7_GPIO_NUM       39
#define Y6_GPIO_NUM       36
#define Y5_GPIO_NUM       21
#define Y4_GPIO_NUM       19
#define Y3_GPIO_NUM       18
#define Y2_GPIO_NUM        5
```

```
#define VSYNC_GPIO_NUM    25
#define HREF_GPIO_NUM     23
#define PCLK_GPIO_NUM     22

//Variables for Bluetooth
BluetoothSerial SerialBT;
char command[9];

//Variables for WIFI
const char *ssid = "EsMiWifi"; //Declare the ssid and password of the wifi
const char  *password = "hola1234567890";

//Variables for time limit and auxiliars
unsigned long currentTime;
byte aux1 = 0, aux2 = 0, aux3 = 0;
//State machine modes
enum State{
    Recon,
    NRecon,
    DeepSleep};
State state = Recon; //First state == Initialization

//Here only appear the Wifi and BLE functions, the other are in Face_Recognition.h

void Wifi_function(bool enable){
 if (enable == true){
  WiFi.begin(ssid,password);
  Serial.println("Connecting Wifi...");
```

```
    Serial.println(ssid);Serial.println(password);
    while (WiFi.status() != WL_CONNECTED) {
        delay(500);
        Serial.print(".");
    }
    Serial.println("");
    Serial.print("IP address: ");
    Serial.println(WiFi.localIP()); }
  else{
    WiFi.mode(WIFI_MODE_NULL); //It should turn wifi off
    Serial.println("Wifi turned off!");
  }
  }

  void BLE_function(bool enable){
    if (enable == true){
      SerialBT.begin("ESP32_CAM");
      Serial.println("The device started, now you can pair it with bluetooth!");
    }
    else{
      SerialBT.end();
      Serial.println("Bluetooth turned off!");
    }
  }

  void setup() {
    WRITE_PERI_REG(RTC_CNTL_BROWN_OUT_REG,  0);  //disable  brownout
detector
```

```
//Deep Sleep Mode
  esp_sleep_enable_ext0_wakeup(GPIO_NUM_12, 1);//Use this pinout as wakeup, for the pir motion sensor
  Serial.begin(115200);
  Serial.setDebugOutput(true);
  pinMode(0, OUTPUT);
//Camera config
camera_config_t config;
  config.ledc_channel = LEDC_CHANNEL_0;
  config.ledc_timer = LEDC_TIMER_0;
  config.pin_d0 = Y2_GPIO_NUM;
  config.pin_d1 = Y3_GPIO_NUM;
  config.pin_d2 = Y4_GPIO_NUM;
  config.pin_d3 = Y5_GPIO_NUM;
  config.pin_d4 = Y6_GPIO_NUM;
  config.pin_d5 = Y7_GPIO_NUM;
  config.pin_d6 = Y8_GPIO_NUM;
  config.pin_d7 = Y9_GPIO_NUM;
  config.pin_xclk = XCLK_GPIO_NUM;
  config.pin_pclk = PCLK_GPIO_NUM;
  config.pin_vsync = VSYNC_GPIO_NUM;
  config.pin_href = HREF_GPIO_NUM;
  config.pin_sscb_sda = SIOD_GPIO_NUM;
  config.pin_sscb_scl = SIOC_GPIO_NUM;
  config.pin_pwdn = PWDN_GPIO_NUM;
  config.pin_reset = RESET_GPIO_NUM;
  config.xclk_freq_hz = 20000000;
  config.pixel_format = PIXFORMAT_JPEG;
```

```
  config.frame_size = FRAMESIZE_UXGA; // Max quality with psram
  config.jpeg_quality = 12;
  config.fb_count = 2;

//Camera Initialization
esp_err_t err = esp_camera_init(&config);
  if (err != ESP_OK) {
    Serial.printf("Camera init failed with error 0x%x", err);
    return;
  }

//Init SD Card Mount
  if(!SD_MMC.begin()){
    Serial.println("SD Card Mount Failed");
    return;
  }

  uint8_t cardType = SD_MMC.cardType();
  if(cardType == CARD_NONE){
    Serial.println("No SD Card attached");
    return;
  }
  //Sensors config for the camera
  sensor_t * s = esp_camera_sensor_get();
    s->set_framesize(s, FRAMESIZE_QVGA);//drop down the quality, I dont need
more than QVGA or CIF
    s->set_vflip(s,1);
    s->set_contrast(s, 2);
```

```
    s->set_saturation(s,-2);
    s->set_gainceiling(s,(gainceiling_t)1);

  //Trying to turn flash off
  ledcSetup(15, 5000, 8);
  ledcAttachPin(4, 15);

  init_everything();
}

void loop() {
currentTime = millis();
switch(state){
  case Recon:
    for(aux2; aux2 < 1; aux2 ++){
    Serial.println("Current state is Recon");
    Wifi_function(false);
    BLE_function(true);}
    fb = NULL;
    godFunction();
    while(SerialBT.available()){
      for(aux1;aux1 < 8;aux1++)
       command[aux1] = SerialBT.read();
      }
    if(strcmp(command,"OpenA101")==0 && currentTime < 20000){
      OpenDoor(0);
      state = DeepSleep;}
```

```
        else if(currentTime >= 20000 ){//I need to add face recog condition here, and
change time to 18 s aprox
          state = NRecon;
          aux2 = 0;
        }
      break;
      case NRecon:
        for(aux3; aux3 < 1; aux3++){
        Serial.println("Current state is No Recon");
        BLE_function(false);
        Wifi_function(true);
        takePic();
        uploadPic();}
        if(currentTime >= 7000 ){ //I'll change the time to 7 or something like that +
the other time
            aux3 = 0;
            state = DeepSleep;
          }
      break;
      case DeepSleep:
        Wifi_function(false);
        BLE_function(false);
        Serial.println("Going to sleep now");
        delay(500);
        esp_deep_sleep_start();
      break;
      default:
      state = Recon;
```

```
  break;
}
}
```

- Página Face_Recognition.h

```
#include "esp_camera.h"
#include "img_converters.h"
#include "Arduino.h"
#include "fb_gfx.h"
#include "fd_forward.h"
#include "fr_forward.h"
#include "FS.h"                // SD Card ESP32
#include "SD_MMC.h"            // SD Card ESP32
#include <WiFi.h>
#include <ESP32_FTPClient.h>

#define ENROLL_CONFIRM_TIMES 5
#define FACE_ID_SAVE_NUMBER 7

//Variables for FTP Server
char ftp_server[] = "files.000webhost.com"; //Declare the variables for ftp server
char ftp_user[]   = "tfgluis";
char ftp_pass[]   = "pw7FDtadGueycl$&YcCu";

ESP32_FTPClient ftp (ftp_server,ftp_user,ftp_pass, 5000, 2);//Call ftp server

#define ENROLL_CONFIRM_TIMES 5
#define FACE_ID_SAVE_NUMBER 7
```

```
#define FACE_COLOR_RED     0x000000FF
#define FACE_COLOR_GREEN  0x0000FF00
#define FACE_COLOR_BLUE   0x00FF0000

void init_everything();

static mtmn_config_t mtmn_config = {0};
static face_id_list id_list = {0};
int enrolling = 1;
camera_fb_t * fb = NULL;
dl_matrix3du_t *aligned_face = NULL;
dl_matrix3du_t *image_matrix = NULL;

void takePic(){
  //Take pic
  fb = esp_camera_fb_get();
  if(!fb) {
    Serial.println("Camera capture failed");
    return;
  }
}

void uploadPic(){
  String PicName = "Pic";
  static int PicNumber;
  PicName.concat(PicNumber);
  PicName.concat(".jpg");
```

```
  PicNumber++;
  ftp.OpenConnection();
    ftp.InitFile("Type I");
    ftp.ChangeWorkDir("/public_html/prueba1/CameraPic");
    const char *Name = PicName.c_str();
    ftp.NewFile(Name);
    ftp.WriteData(fb->buf, fb->len);
    ftp.CloseFile();
    ftp.CloseConnection();
    delay(50);
}

void OpenDoor(int number){
  digitalWrite(number, HIGH);
  delay(500);
  digitalWrite(number, LOW);
}

void SD_Write(face_id_list id_list, String Name){
  String path = "/archive_"+ Name +".txt";

  fs::FS &fs = SD_MMC;
  Serial.printf("File name: %s\n", path.c_str());

  File myFile = fs.open(path.c_str(), FILE_WRITE);
  if(!myFile){
    Serial.println("Failed to open file in writing mode");
  }
```

```
  else {
    myFile.write((const uint8_t*)&id_list, sizeof(id_list));
    Serial.printf("Saved file to path: %s\n", path.c_str());
  }
  myFile.close();
}

void SD_Read(face_id_list id_list, String Name){
  String path = "/archive_"+ Name +".txt";

  fs::FS &fs = SD_MMC;
  Serial.printf("File name: %s\n", path.c_str());

  File myFile = fs.open(path.c_str(), FILE_READ);
  if(!myFile){
    Serial.println("Failed to open file in reading mode");
  }
  else {
    myFile.read((uint8_t*)&id_list, sizeof(id_list));
    Serial.printf("Read file to path: %s\n", path.c_str());
  }
  myFile.close();
}

static inline mtmn_config_t app_mtmn_config(){
  mtmn_config_t mtmn_config = {0};
  mtmn_config.type = FAST;
  mtmn_config.min_face = 80;
```

```
  mtmn_config.pyramid = 0.707;
  mtmn_config.pyramid_times = 4;
  mtmn_config.p_threshold.score = 0.6;
  mtmn_config.p_threshold.nms = 0.7;
  mtmn_config.p_threshold.candidate_number = 20;
  mtmn_config.r_threshold.score = 0.7;
  mtmn_config.r_threshold.nms = 0.7;
  mtmn_config.r_threshold.candidate_number = 10;
  mtmn_config.o_threshold.score = 0.7;
  mtmn_config.o_threshold.nms = 0.7;
  mtmn_config.o_threshold.candidate_number = 1;
  return mtmn_config;
}

typedef struct {
        size_t size; //number of values used for filtering
        size_t index; //current value index
        size_t count; //value count
        int sum;
        int * values; //array to be filled with values
} ra_filter_t;

static ra_filter_t * ra_filter_init(ra_filter_t *filter, size_t sample_size){
    memset(filter, 0, sizeof(ra_filter_t));

    filter->values = (int *)malloc(sample_size * sizeof(int));
    if(!filter->values){
        return NULL;
```

```
    }
    memset(filter->values, 0, sample_size * sizeof(int));

    filter->size = sample_size;
    return filter;
}

static ra_filter_t ra_filter;

static int ra_filter_run(ra_filter_t *filter, int value){
    if(!filter->values){
        return value;
    }
    filter->sum -= filter->values[filter->index];
    filter->values[filter->index] = value;
    filter->sum += filter->values[filter->index];
    filter->index++;
    filter->index = filter->index % filter->size;
    if (filter->count < filter->size) {
        filter->count++;
    }
    return filter->sum / filter->count;
}

static void rgb_print(dl_matrix3du_t *image_matrix, uint32_t color, const char *
str){
    fb_data_t fb;
    fb.width = image_matrix->w;
```

```
    fb.height = image_matrix->h;
    fb.data = image_matrix->item;
    fb.bytes_per_pixel = 3;
    fb.format = FB_BGR888;
    fb_gfx_print(&fb, (fb.width - (strlen(str) * 14)) / 2, 10, color, str);
}

static int rgb_printf(dl_matrix3du_t *image_matrix, uint32_t color, const char *format, ...){
    char loc_buf[64];
    char * temp = loc_buf;
    int len;
    va_list arg;
    va_list copy;
    va_start(arg, format);
    va_copy(copy, arg);
    len = vsnprintf(loc_buf, sizeof(loc_buf), format, arg);
    va_end(copy);
    if(len >= sizeof(loc_buf)){
        temp = (char*)malloc(len+1);
        if(temp == NULL) {
            return 0;
        }
    }
    vsnprintf(temp, len+1, format, arg);
    va_end(arg);
    rgb_print(image_matrix, color, temp);
    if(len > 64){
```

```
            free(temp);
        }
        return len;
    }


    static void draw_face_boxes(dl_matrix3du_t *image_matrix, box_array_t *boxes,
int face_id){
        int x, y, w, h, i;
        uint32_t color = FACE_COLOR_BLUE;
        if(face_id < 0){
            color = FACE_COLOR_RED;
        } else if(face_id > 0){
            color = FACE_COLOR_GREEN;
        }
        fb_data_t fb;
        fb.width = image_matrix->w;
        fb.height = image_matrix->h;
        fb.data = image_matrix->item;
        fb.bytes_per_pixel = 3;
        fb.format = FB_BGR888;
        for (i = 0; i < boxes->len; i++){
            // rectangle box
            x = (int)boxes->box[i].box_p[0];
            y = (int)boxes->box[i].box_p[1];
            w = (int)boxes->box[i].box_p[2] - x + 1;
            h = (int)boxes->box[i].box_p[3] - y + 1;
            fb_gfx_drawFastHLine(&fb, x, y, w, color);
            fb_gfx_drawFastHLine(&fb, x, y+h-1, w, color);
```

```
        fb_gfx_drawFastVLine(&fb, x, y, h, color);
        fb_gfx_drawFastVLine(&fb, x+w-1, y, h, color);
      }
    }

    static int run_face_recognition(dl_matrix3du_t *image_matrix, box_array_t *net_boxes){
      int matched_id = 0;
      aligned_face = dl_matrix3du_alloc(1, FACE_WIDTH, FACE_HEIGHT, 3);
      if(!aligned_face){
        Serial.println("Could not allocate face recognition buffer");
        return matched_id;
      }
      if (align_face(net_boxes, image_matrix, aligned_face) == ESP_OK){
          if(enrolling == 1){
           int8_t left_sample_face = enroll_face(&id_list, aligned_face);

           if(left_sample_face == (ENROLL_CONFIRM_TIMES - 1)){
             Serial.printf("Enrolling Face ID: %d\n", id_list.tail);
           }
           Serial.printf("Enrolling Face ID: %d sample %d\n", id_list.tail, ENROLL_CONFIRM_TIMES - left_sample_face);
           rgb_printf(image_matrix, FACE_COLOR_GREEN, "ID[%u] Sample[%u]", id_list.tail, ENROLL_CONFIRM_TIMES - left_sample_face);
           if (left_sample_face == 0){
             enrolling = 0;
             Serial.printf("Enrolled Face ID: %d\n", id_list.tail);
             SD_Write(id_list, "MyList");
           }
```

```
                esp_camera_fb_return(fb);
               }
               else{
                matched_id = recognize_face(&id_list, aligned_face);
                if (matched_id >= 0) {
                    Serial.printf("Match Face ID: %u\n", matched_id);
                    rgb_printf(image_matrix, FACE_COLOR_GREEN, "Hello Subject %u",
matched_id);
                    OpenDoor(0);
                }
                else {
                    Serial.println("No Match Found");
                    rgb_print(image_matrix, FACE_COLOR_RED, "Intruder Alert!");
                    matched_id = -1;
                    takePic();
                    uploadPic; //Upload the intruder face to the server
                }
               esp_camera_fb_return(fb);
             }
            }
          else {
             Serial.println("Face Not Aligned");
          }

          dl_matrix3du_free(aligned_face);
          return matched_id;
      }
```

```
void godFunction(){
    takePic();
    bool detected = false;
    int face_id = 0;
    image_matrix = dl_matrix3du_alloc(1, 320, 240, 3); //320x240 because of QVGA quality
    if (!image_matrix) {
        Serial.println("dl_matrix3du_alloc failed");
    }
    box_array_t *net_boxes = face_detect(image_matrix, &mtmn_config);

    if (net_boxes){
        detected = true;
        face_id = run_face_recognition(image_matrix, net_boxes);
        draw_face_boxes(image_matrix, net_boxes, face_id);
        free(net_boxes->score);
        free(net_boxes->box);
        free(net_boxes->landmark);
        free(net_boxes);
    }
    esp_camera_fb_return(fb);
    dl_matrix3du_free(image_matrix);
}

void init_everything(){
    face_id_init(&id_list, FACE_ID_SAVE_NUMBER, ENROLL_CONFIRM_TIMES);
    aligned_face = dl_matrix3du_alloc(1, FACE_WIDTH, FACE_HEIGHT, 3);
    if(!aligned_face)
```

```
            Serial.println("Fail Here");
//      SD_Read(id_list, "MyList");
}
```

ANEXO 4. DATASHEETS

ESP32-WROVER-B

Datasheet

Version 1.4

Espressif Systems

About This Document

This document provides the specifications for the ESP32-WROVER-B modules with PCB antenna and IPEX antenna.

Document Updates

Please always refer to the latest version on https://www.espressif.com/en/support/download/documents.

Revision History

For revision history of this document, please refer to the last page.

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1. Overview

ESP32-WROVER-B is a powerful, generic WiFi-BT-BLE MCU module that targets a wide variety of applications, ranging from low-power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding.

This module is provided in two versions: one with a PCB antenna, the other with an IPEX antenna. ESP32-WROVER-B features a 4 MB external SPI flash and an additional 8 MB SPI Pseudo static RAM (PSRAM). **The information in this datasheet is applicable to both modules.**

The ordering information on the two variants of ESP32-WROVER-B is listed as follows:

Table 1: ESP32-WROVER-B Ordering Information

Module	Chip embedded	Flash	PSRAM	Module dimensions (mm)
ESP32-WROVER-B (PCB)	ESP32-D0WD	4 MB [1]	8 MB	(18.00±0.10)×(31.40±0.10)×(3.30±0.10)
ESP32-WROVER-B (IPEX)				

Notes:

1. ESP32-WROVER-B (PCB/IPEX) with 8 MB flash or 16 MB flash is available for custom order.
2. For detailed ordering information, please see *Espressif Product Ordering Information*.
3. For dimensions of the IPEX connector, please see Chapter 10.

At the core of the module is the ESP32-D0WD chip*. The chip embedded is designed to be scalable and adaptive. There are two CPU cores that can be individually controlled, and the CPU clock frequency is adjustable from 80 MHz to 240 MHz. The chip also has a low-power co-processor that can be used instead of the CPU to save power while performing tasks that do not require much computing power, such as monitoring of peripherals. ESP32 integrates a rich set of peripherals, ranging from capacitive touch sensors, Hall sensors, SD card interface, Ethernet, high-speed SPI, UART, I²S and I²C.

Note:

* For details on the part numbers of the ESP32 family of chips, please refer to the document *ESP32 Datasheet*.

The integration of Bluetooth, Bluetooth LE and Wi-Fi ensures that a wide range of applications can be targeted, and that the module is all-around: using Wi-Fi allows a large physical range and direct connection to the Internet through a Wi-Fi router, while using Bluetooth allows the user to conveniently connect to the phone or broadcast low energy beacons for its detection. The sleep current of the ESP32 chip is less than 5 μA, making it suitable for battery powered and wearable electronics applications. The module supports a data rate of up to 150 Mbps, and 20 dBm output power at the antenna to ensure the widest physical range. As such the module does offer industry-leading specifications and the best performance for electronic integration, range, power consumption, and connectivity.

The operating system chosen for ESP32 is freeRTOS with LwIP; TLS 1.2 with hardware acceleration is built in as well. Secure (encrypted) over the air (OTA) upgrade is also supported, so that users can upgrade their products even after their release, at minimum cost and effort.

Table 2 provides the specifications of ESP32-WROVER-B.

Table 2: ESP32-WROVER-B Specifications

Categories	Items	Specifications
Certification	RF certification	FCC/CE-RED/IC/TELEC/KCC/SRRC/NCC
	Bluetooth certification	BQB
	Green certification	RoHS, REACH
Test	Reliablity	HTOL/HTSL/uHAST/TCT/ESD
Wi-Fi	Protocols	802.11 b/g/n (802.11n up to 150 Mbps)
		A-MPDU and A-MSDU aggregation and 0.4 μs guard interval support
	Frequency range	2.4 GHz ~ 2.5 GHz
Bluetooth	Protocols	Bluetooth v4.2 BR/EDR and BLE specification
	Radio	NZIF receiver with –97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC
Hardware	Module interfaces	SD card, UART, SPI, SDIO, I^2C, LED PWM, Motor PWM, I^2S, IR, pulse counter, GPIO, capacitive touch sensor, ADC, DAC
	On-chip sensor	Hall sensor
	Integrated crystal	40 MHz crystal
	Integrated SPI flash	4 MB
	Integrated PSRAM	8 MB
	Operating voltage/Power supply	3.0 V ~ 3.6 V
	Minimum current delivered by power supply	500 mA
	Recommended operating temperature range	–40 °C ~ 85 °C
	Package size	(18.00±0.10) mm × (31.40±0.10) mm × (3.30±0.10) mm
	Moisture sensitivity level (MSL)	Level 3

2. Pin Definitions

2.1 Pin Layout

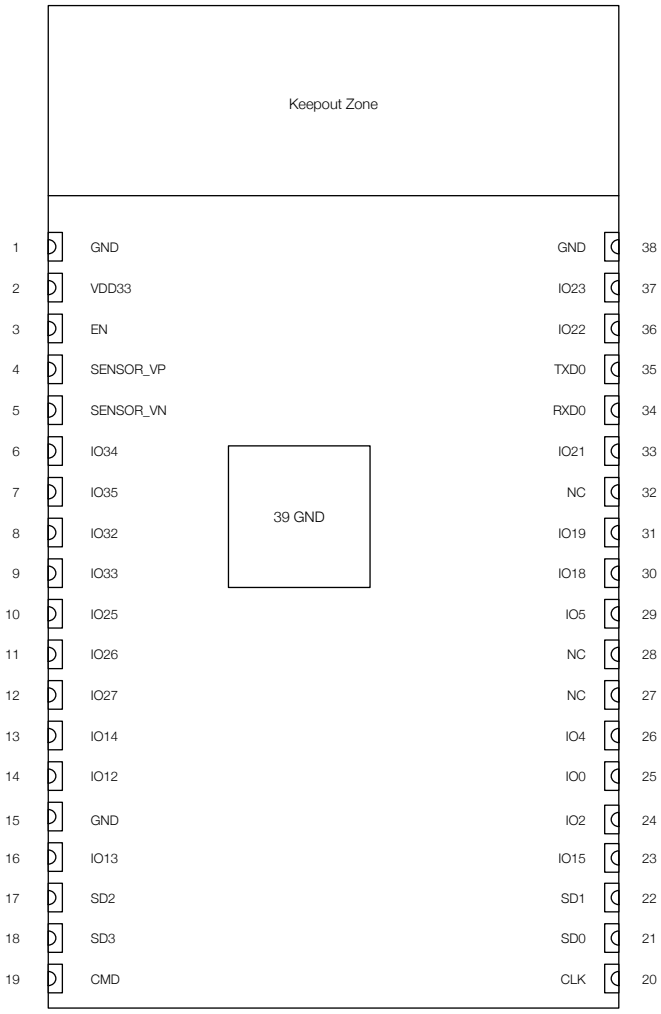


Figure 1: Pin Layout of ESP32-WROVER-B (Top View)

2.2 Pin Description

ESP32-WROVER-B has 38 pins. See pin definitions in Table 3.

Table 3: Pin Definitions

Name	No.	Type	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	Module-enable signal. Active high.
SENSOR_VP	4	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_VN	5	I	GPIO39, ADC1_CH3, RTC_GPIO3
IO34	6	I	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	7	I	GPIO35, ADC1_CH7, RTC_GPIO5
IO32	8	I/O	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	9	I/O	GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	10	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	11	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	12	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	13	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	14	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
GND	15	P	Ground
IO13	16	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
SHD/SD2 *	17	I/O	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
SWP/SD3 *	18	I/O	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
SCS/CMD *	19	I/O	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS
SCK/CLK *	20	I/O	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
SDO/SD0 *	21	I/O	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
SDI/SD1 *	22	I/O	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
IO15	23	I/O	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	24	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	25	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	26	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
NC1	27	-	-
NC2	28	-	-
IO5	29	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK

Name	No.	Type	Function
IO18	30	I/O	GPIO18, VSPICLK, HS1_DATA7
IO19	31	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
NC	32	-	-
IO21	33	I/O	GPIO21, VSPIHD, EMAC_TX_EN
RXD0	34	I/O	GPIO3, U0RXD, CLK_OUT2
TXD0	35	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO22	36	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
IO23	37	I/O	GPIO23, VSPID, HS1_STROBE
GND	38	P	Ground

Notice:

* Pins SCK/CLK, SDO/SD0, SDI/SD1, SHD/SD2, SWP/SD3 and SCS/CMD, namely, GPIO6 to GPIO11 are connected to the SPI flash integrated on the module and are not recommended for other uses.

2.3 Strapping Pins

ESP32 has five strapping pins, which can be seen in Chapter 6 Schematics:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 4 for a detailed boot-mode configuration by strapping pins.

Table 4: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)

Pin	Default	3.3 V	1.8 V
MTDI	Pull-down	0	1
Booting Mode			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO2	Pull-down	Don't-care	0
Enabling/Disabling Debugging Log Print over U0TXD During Booting			
Pin	Default	U0TXD Active	U0TXD Silent
MTDO	Pull-up	1	0

Timing of SDIO Slave					
Pin	Default	Falling-edge Sampling Falling-edge Output	Falling-edge Sampling Rising-edge Output	Rising-edge Sampling Falling-edge Output	Rising-edge Sampling Rising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave" after booting.
- Internal pull-up resistor (R9) for MTDI is not populated in the module, as the flash and SRAM in ESP32-WROVER-B only support a power voltage of 3.3 V (output by VDD_SDIO).

3. Functional Description

This chapter describes the modules and functions integrated in ESP32-WROVER-B.

3.1 CPU and Internal Memory

ESP32-D0WD contains two low-power Xtensa® 32-bit LX6 microprocessors. The internal memory includes:

- 448 KB of ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

3.2 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the *ESP32 Technical Reference Manual*. ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- The external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
  - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
  - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. Up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

ESP32-WROVER-B integrates a 4 MB SPI flash and an 8 MB PSRAM for more memory space.

3.3 Crystal Oscillators

The module uses a 40-MHz crystal oscillator.

3.4 RTC and Low-Power Management

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

For details on ESP32's power consumption in different power modes, please refer to section "RTC and Low-Power Management" in *ESP32 Datasheet*.

4. Peripherals and Sensors

Please refer to Section Peripherals and Sensors in *ESP32 Datasheet*.

Note:
External connections can be made to any GPIO except for GPIOs in the range 6-11, 16, or 17. GPIOs 6-11 are connected to the module's integrated SPI flash and PSRAM. GPIOs 16 and 17 are connected to the module's integrated PSRAM. For details, please see Section 6 Schematics.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
I_{output}[1]	Cumulative IO output current	-	1,100	mA
T_{store}	Storage temperature	–40	150	°C

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground. Please note that pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.
2. Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain.

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	-	-	A
T	Operating temperature	–40	-	85	°C

5.3 DC Characteristics (3.3 V, 25 °C)

Table 7: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		-	2	-	pF
V_{IH}	High-level input voltage		0.75×VDD[1]	-	VDD[1]+0.3	V
V_{IL}	Low-level input voltage		–0.3	-	0.25×VDD[1]	V
I_{IH}	High-level input current		-	-	50	nA
I_{IL}	Low-level input current		-	-	50	nA
V_{OH}	High-level output voltage		0.8×VDD[1]	-	-	V
V_{OL}	Low-level output voltage		-	-	0.1×VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	-	40	-	mA
		VDD3P3_RTC power domain [1, 2]	-	40	-	mA
		VDD_SDIO power domain [1, 3]	-	20	-	mA

Symbol	Parameter	Min	Typ	Max	Unit
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)	-	28	-	mA
R_{PU}	Resistance of internal pull-up resistor	-	45	-	kΩ
R_{PD}	Resistance of internal pull-down resistor	-	45	-	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip	-	-	0.6	V

Notes:

1. Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

5.4 Wi-Fi Radio

Table 8: Wi-Fi Radio Characteristics

Parameter	Condition	Min	Typical	Max	Unit
Operating frequency range ^{note1}	-	2412	-	2484	MHz
Output impedance ^{note2}	-	-	*	-	Ω
TX power ^{note3}	11n, MCS7	12	13	14	dBm
	11b mode	17.5	18.5	20	dBm
Sensitivity	11b, 1 Mbps	-	–98	-	dBm
	11b, 11 Mbps	-	–89	-	dBm
	11g, 6 Mbps	-	–92	-	dBm
	11g, 54 Mbps	-	–74	-	dBm
	11n, HT20, MCS0	-	–91	-	dBm
	11n, HT20, MCS7	-	–71	-	dBm
	11n, HT40, MCS0	-	–89	-	dBm
	11n, HT40, MCS7	-	–69	-	dBm
Adjacent channel rejection	11g, 6 Mbps	-	31	-	dB
	11g, 54 Mbps	-	14	-	dB
	11n, HT20, MCS0	-	31	-	dB
	11n, HT20, MCS7	-	13	-	dB

1. Device should operate in the frequency range allocated by regional regulatory authorities. Target operating frequency range is configurable by software.
2. For the modules that use IPEX antennas, the output impedance is 50 Ω. For other modules without IPEX antennas, users do not need to concern about the output impedance.
3. Target TX power is configurable based on device or certification requirements.

5.5 BLE Radio

5.5.1 Receiver

Table 9: Receiver Characteristics – BLE

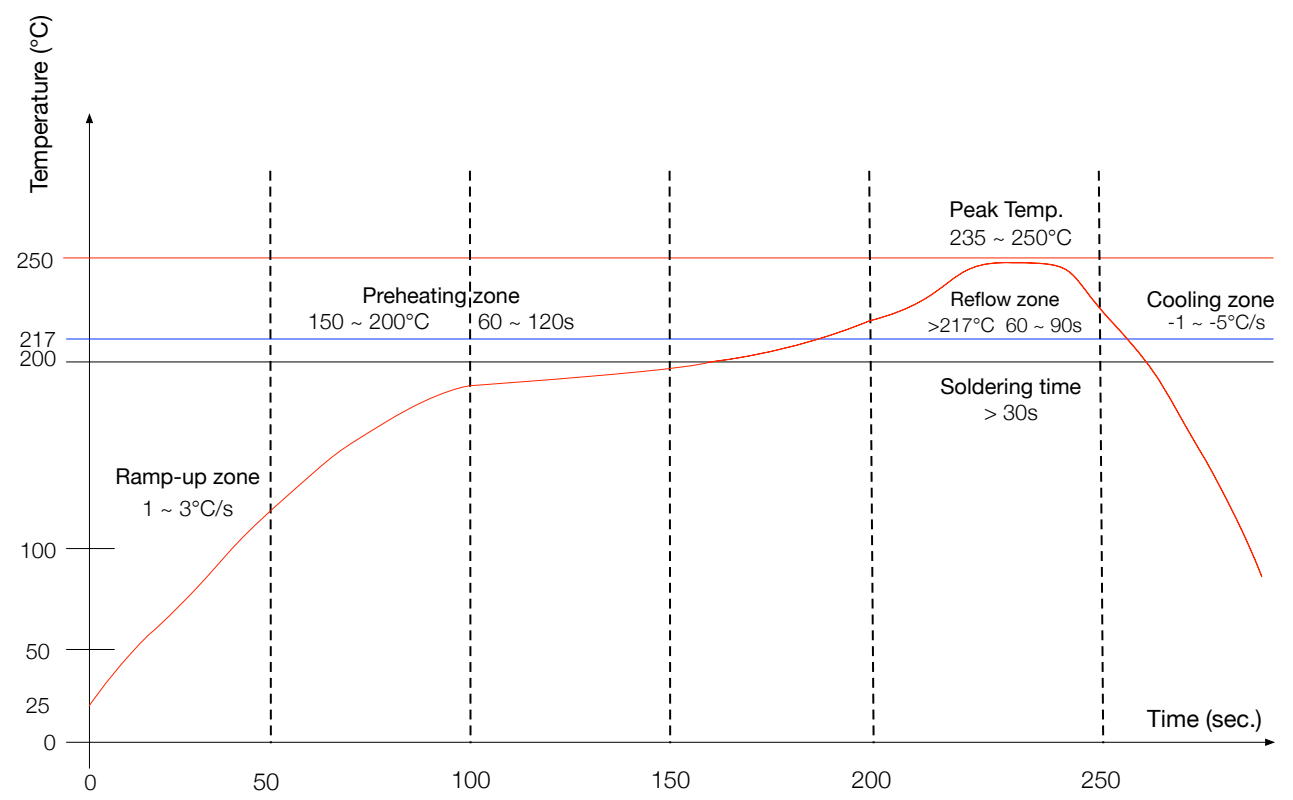
Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	-	-	–97	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	–5	-	dB
	F = F0 – 1 MHz	-	–5	-	dB
	F = F0 + 2 MHz	-	–25	-	dB
	F = F0 – 2 MHz	-	–35	-	dB
	F = F0 + 3 MHz	-	–25	-	dB
	F = F0 – 3 MHz	-	–45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	-	-	dBm
	2000 MHz ~ 2400 MHz	–27	-	-	dBm
	2500 MHz ~ 3000 MHz	–27	-	-	dBm
	3000 MHz ~ 12.5 GHz	–10	-	-	dBm
Intermodulation	-	–36	-	-	dBm

5.5.2 Transmitter

Table 10: Transmitter Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	–12	-	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	-	–52	-	dBm
	F = F0 ± 3 MHz	-	–58	-	dBm
	F = F0 ± > 3 MHz	-	–60	-	dBm
$\Delta f1_{avg}$	-	-	-	265	kHz
$\Delta f2_{max}$	-	247	-	-	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	-	–0.92	-	-
ICFT	-	-	–10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

5.6 Reflow Profile



Ramp-up zone — Temp.: <150°C Time: 60 ~ 90s Ramp-up rate: 1 ~ 3°C/s
Preheating zone — Temp.: 150 ~ 200°C Time: 60 ~ 120s Ramp-up rate: 0.3 ~ 0.8°C/s
Reflow zone — Temp.: >217°C Time: 60 ~ 90s; Peak Temp.: 235 ~ 250°C (<245°C recommended) Time: 30 ~ 70s
Cooling zone — Peak Temp. ~ 180°C Ramp-down rate: -1 ~ -5°C/s
Solder — Sn&Ag&Cu Lead-free solder (SAC305)

Figure 2: Reflow Profile

Note:
Solder the module in a single reflow. If the PCBA requires multiple reflows, place the module on the PCB during the final reflow.

6. Schematics

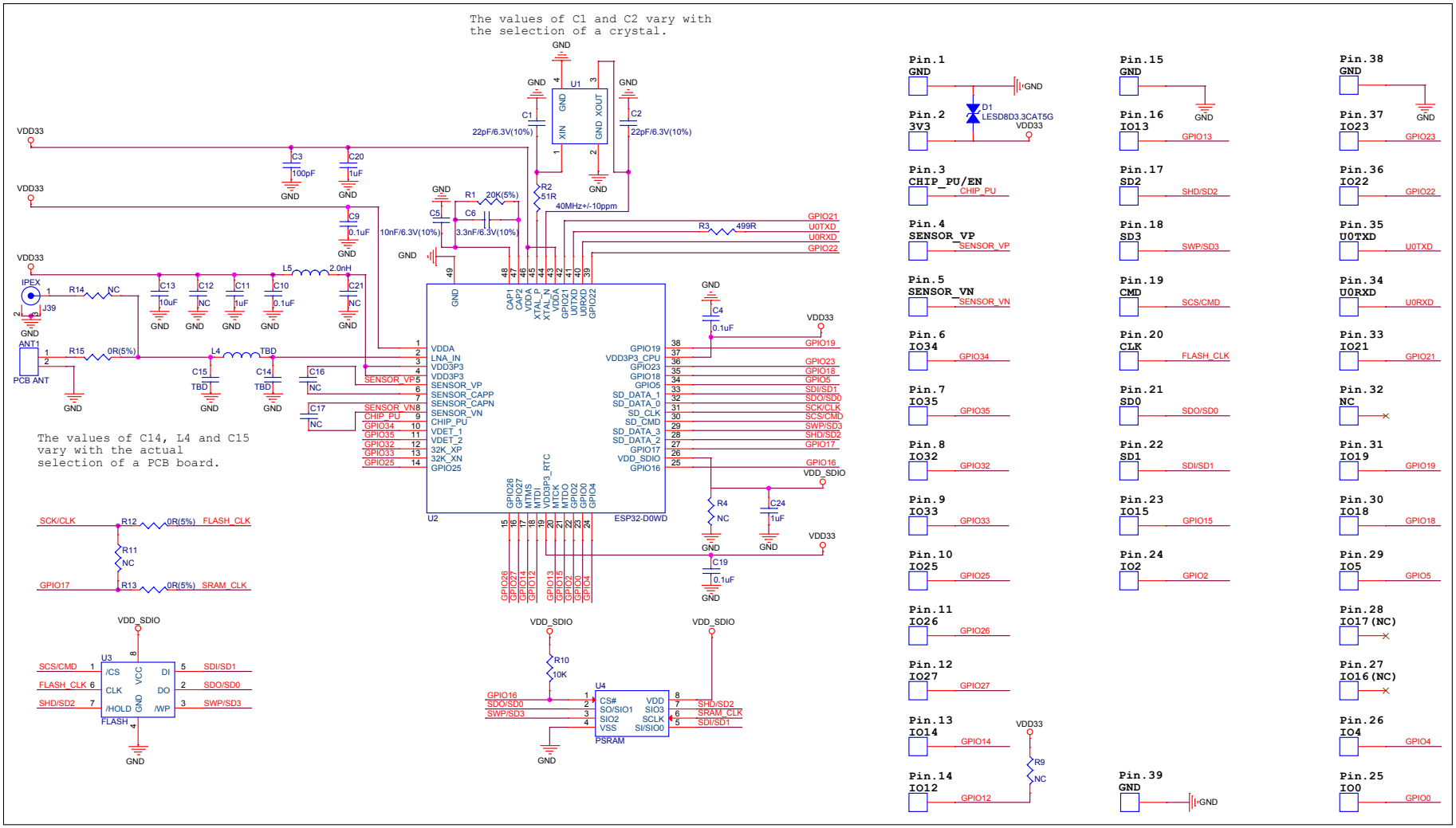


Figure 3: Schematics of ESP32-WROVER-B

7. Peripheral Schematics

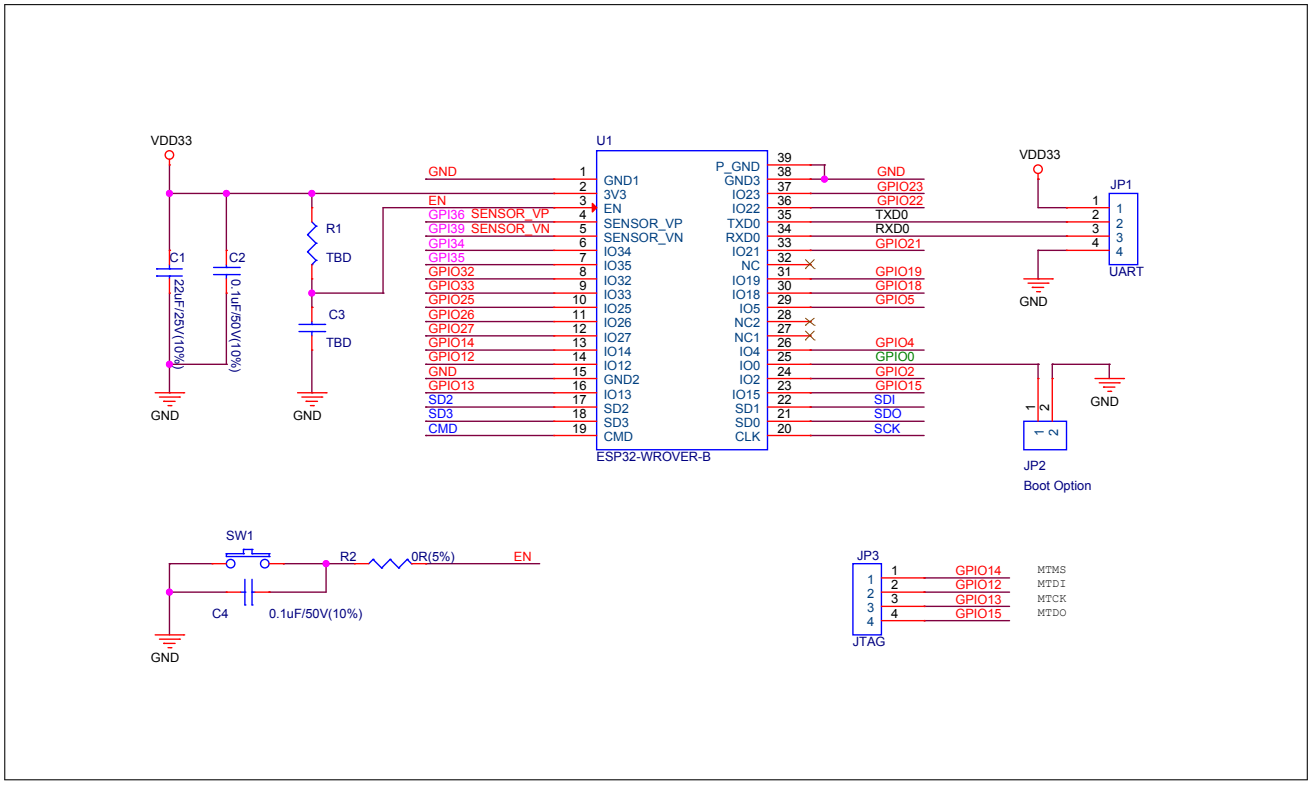


Figure 4: Peripheral Schematics of ESP32-WROVER-B

Note:

- Soldering Pad 39 to the Ground of the base board is not necessary for a satisfactory thermal performance. If users do want to solder it, they need to ensure that the correct quantity of soldering paste is applied.
- To ensure the power supply to the ESP32 chip during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 0.1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32 Datasheet*.

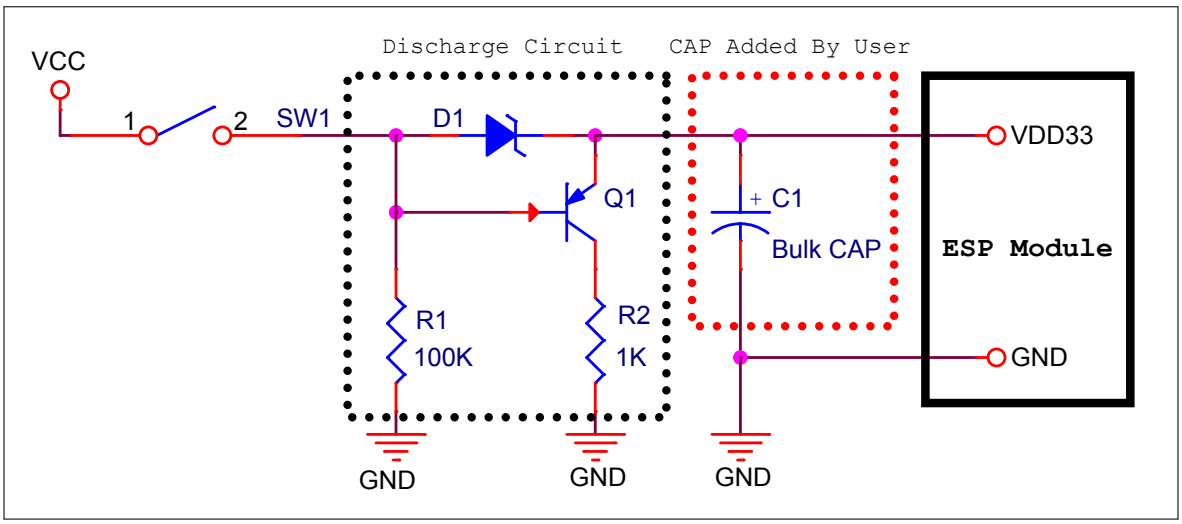


Figure 5: Discharge Circuit for VDD33 Rail

Note:
The discharge circuit can be applied in scenarios where ESP32 is powered on and off repeatedly by switching the power rails, and there is a large capacitor on the VDD33 rail. For details, please refer to Section *Power Scheme* in *ESP32 Datasheet*.

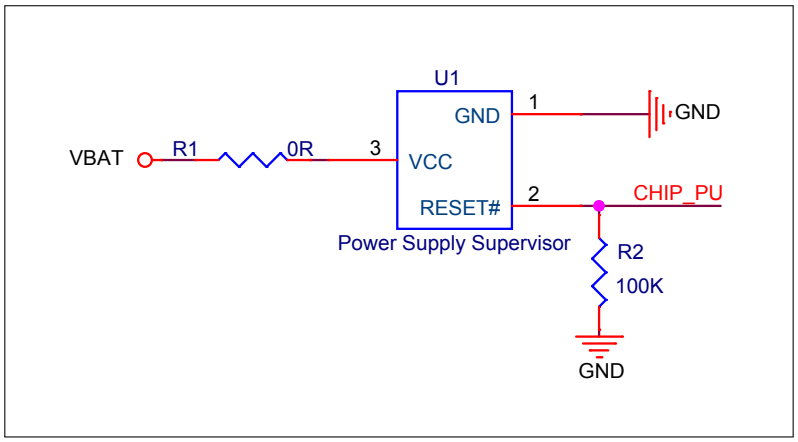


Figure 6: Reset Circuit

Note:
When battery is used as the power supply for ESP32 series of chips and modules, a supply voltage supervisor is recommended to avoid boot failure due to low voltage. Users are recommended to pull CHIP_PU low if the power supply for ESP32 is below 2.3 V.

8. Physical Dimensions

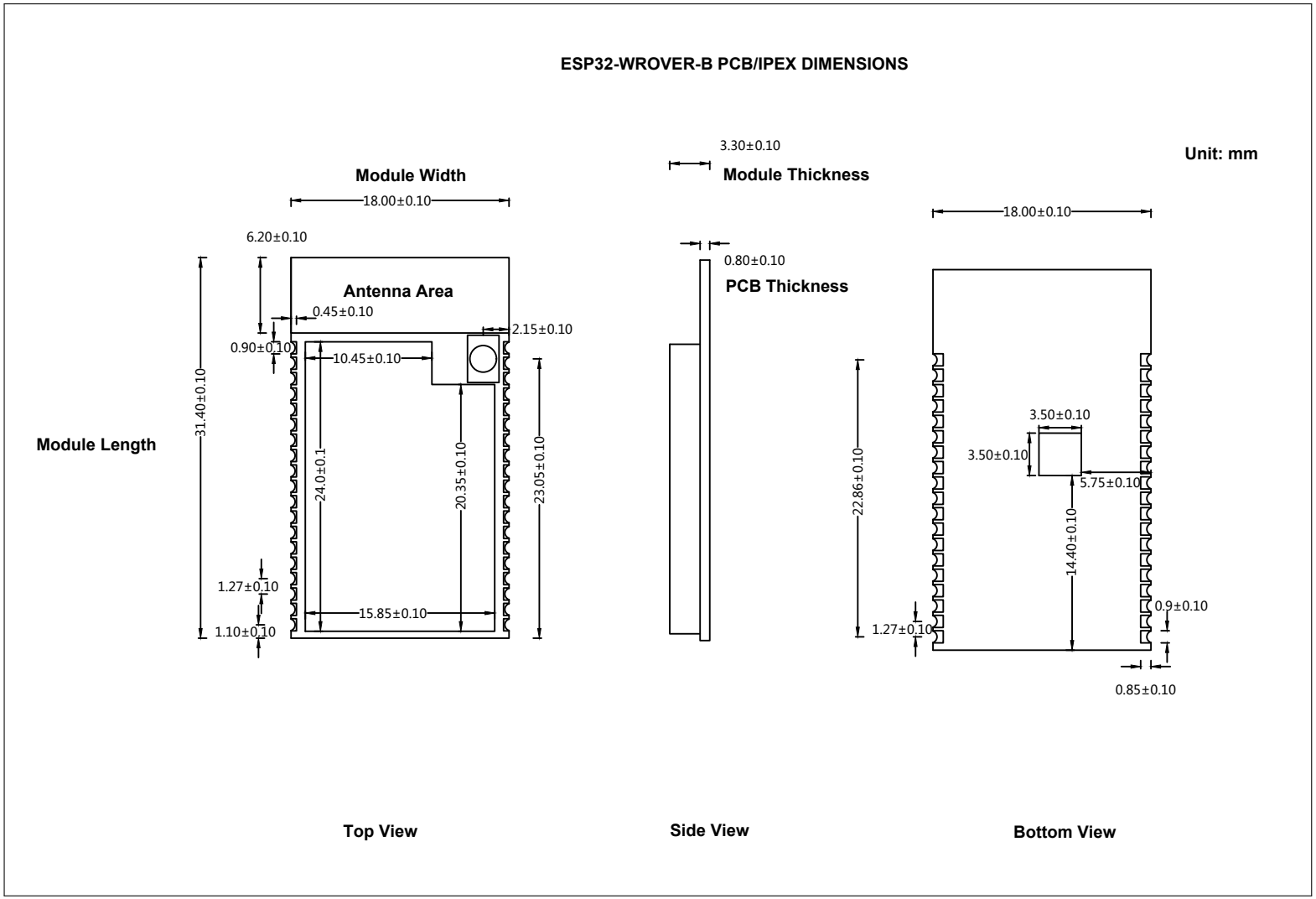


Figure 7: Physical Dimensions of ESP32-WROVER-B (PCB/IPEX)

9. Recommended PCB Land Pattern

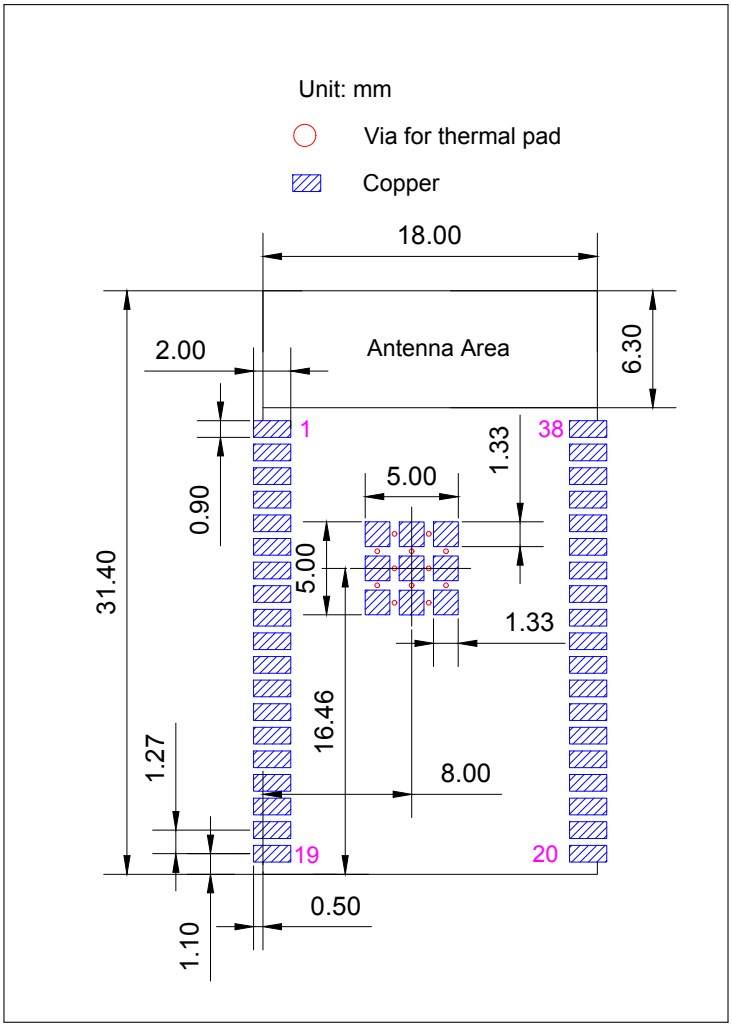


Figure 8: Recommended PCB Land Pattern of ESP32-WROVER-B

10. U.FL Connector Dimensions

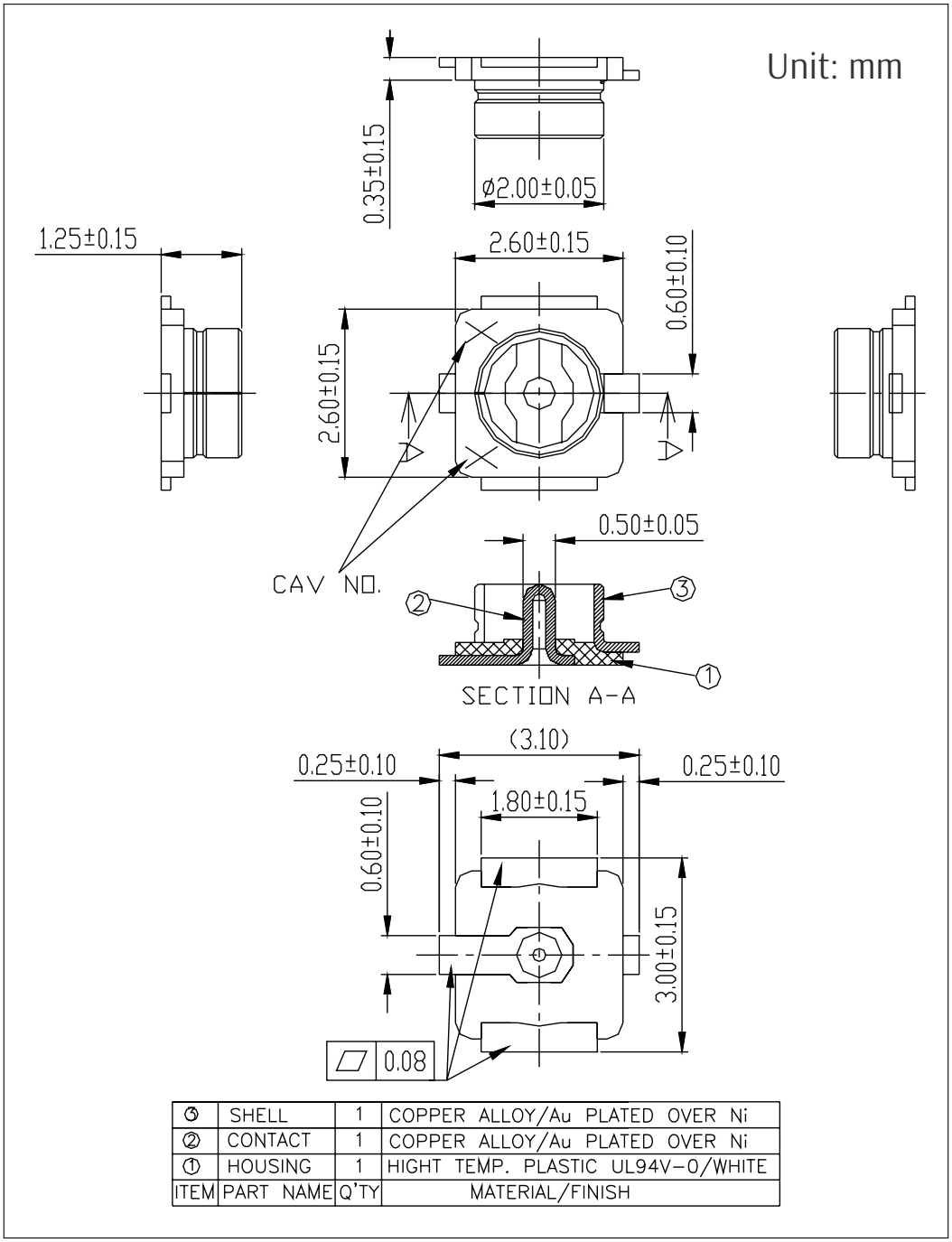


Figure 9: U.FL Connector Dimensions

11. Learning Resources

11.1 Must-Read Documents

The following link provides documents related to ESP32.

- *ESP32 Datasheet*
  This document provides an introduction to the specifications of the ESP32 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.
- *ESP32 ECO V3 User Guide*
  This document describes differences between V3 and previous ESP32 silicon wafer revisions.
- *ECO and Workarounds for Bugs in ESP32*
  This document details hardware errata and workarounds in the ESP32.
- *ESP-IDF Programming Guide*
  It hosts extensive documentation for ESP-IDF ranging from hardware guides to API reference.
- *ESP32 Technical Reference Manual*
  The manual provides detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Resources
  The zip files include the schematics, PCB layout, Gerber and BOM list of ESP32 modules and development boards.
- *ESP32 Hardware Design Guidelines*
  The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32 series of products, including the ESP32 chip, the ESP32 modules and development boards.
- *ESP32 AT Instruction Set and Examples*
  This document introduces the ESP32 AT commands, explains how to use them, and provides examples of several common AT commands.
- *Espressif Products Ordering Information*

11.2 Must-Have Resources

Here are the ESP32-related must-have resources.

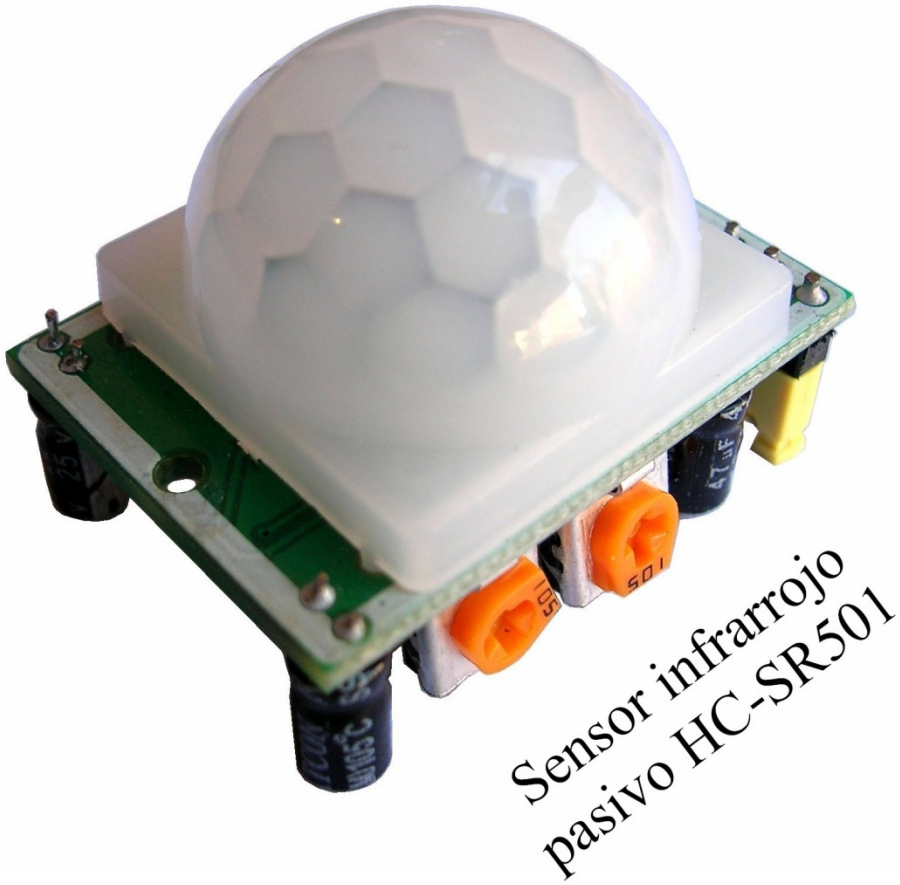
- ESP32 BBS
  This is an Engineer-to-Engineer (E2E) Community for ESP32 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
- ESP32 GitHub
  ESP32 development projects are freely distributed under Espressif's MIT license on GitHub. It is established to help developers get started with ESP32 and foster innovation and the growth of general knowledge about the hardware and software surrounding ESP32 devices.

- ESP32 Tools
  This is a webpage where users can download ESP32 Flash Download Tools and the zip file "ESP32 Certification and Test".
- ESP-IDF
  This webpage links users to the official IoT development framework for ESP32.
- ESP32 Resources
  This webpage provides the links to all available ESP32 documents, SDK and tools.

Revision History

Date	Version	Release notes
2020-03-13	V1.4	• Changed the module's operating temperature range from –40°C ~ 65°C to –40°C ~ 85°C • Added documentation feedback link
2019.09	V1.3	• Changed the supply voltage range from 2.7 V ~ 3.6 V to 3.0 V ~ 3.6 V; • Added Moisture sensitivity level (MSL) 3 in Table 2 *ESP32-WROVER-B Specifications*; • Added notes about "Operating frequency range" and "TX power" under Table 8 *Wi-Fi Radio Characteristics*; • Updated Section 7 *Peripheral Schematics* and added a note about RC delay circuit under it; • Updated Figure 9 *Recommended PCB Land Pattern*.
2019.01	V1.2	Changed the RF power control range in Table 10 from –12 ~ +12 to –12 ~ +9 dBm.
2018.10	V1.1	Added notes on module custom options to Table 1; Added "Cumulative IO output current" entry to Table 5: Absolute Maximum Ratings; Added more parameters to Table 7: DC Characteristics.
2018.07	V1.0	Official release: • Added certifications and reliability test items the module has passed in Table 2: ESP32-WROVER-B Specifications; • Updated the dimensions of the module; • Changed the module's recommended operating temperature from –40°C ~ 85°C to –40°C ~ 65°C; • Updated table 8: Wi-Fi Radio.
2018.06	V0.1	Preliminary release.

Sensor infrarrojo de movimiento PIR HC-SR501



Indice:

1. Principios de funcionamiento:

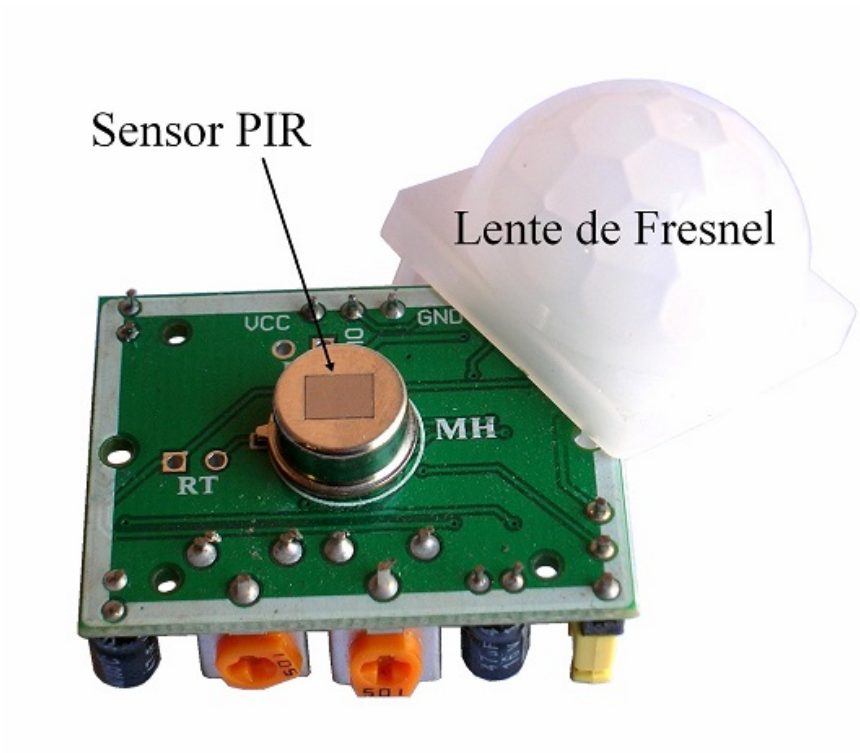
La radiación infrarroja:

Todos los seres vivos e incluso los objetos, emiten radiación electromagnética infrarroja, debido a la temperatura a la que se encuentran. A mayor temperatura, la radiación aumenta. Esta característica ha dado lugar al diseño de sensores de infrarrojo pasivos, en una longitud de onda alrededor de los 9.4 micrones, los cuales permiten la detección de movimiento, típicamente de seres humanos ó animales.

Estos sensores son conocidos como PIR, y toman su nombre de 'Pyroelectric Infrared' ó 'Passive Infrared'.

El lente de Fresnel:

El lente de Fresnel es un encapsulado semiesférico hecho de polietileno de alta densidad cuyo objetivo es permitir el paso de la radiación infrarroja en el rango de los 8 y 14 micrones. El lente detecta radiación en un ángulo con apertura de 110° y, adicionalmente, concentra la energía en la superficie de detección del sensor PIR, permitiendo una mayor sensibilidad del dispositivo.



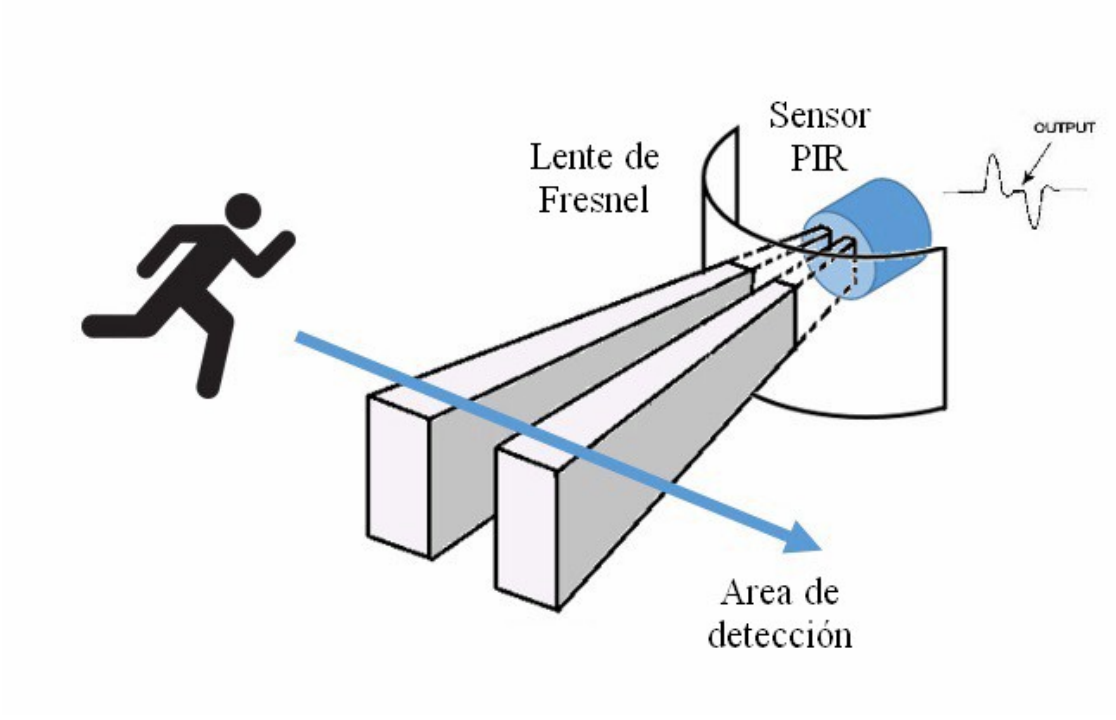
El sensor PIR infrarrojo:

En los sensores de movimiento, el sensor PIR consta en realidad de 2 elementos detectores separados, siendo la señal diferencial entre ambos la que permite activar la alarma de movimiento. En el caso del HC-SR501, la señal generada por el sensor ingresa al circuito integrado BISS0001, el cual contiene amplificadores operacionales e interfaces electrónicas adicionales.

Las funciones y ajustes complementarios del sensor de movimiento son:

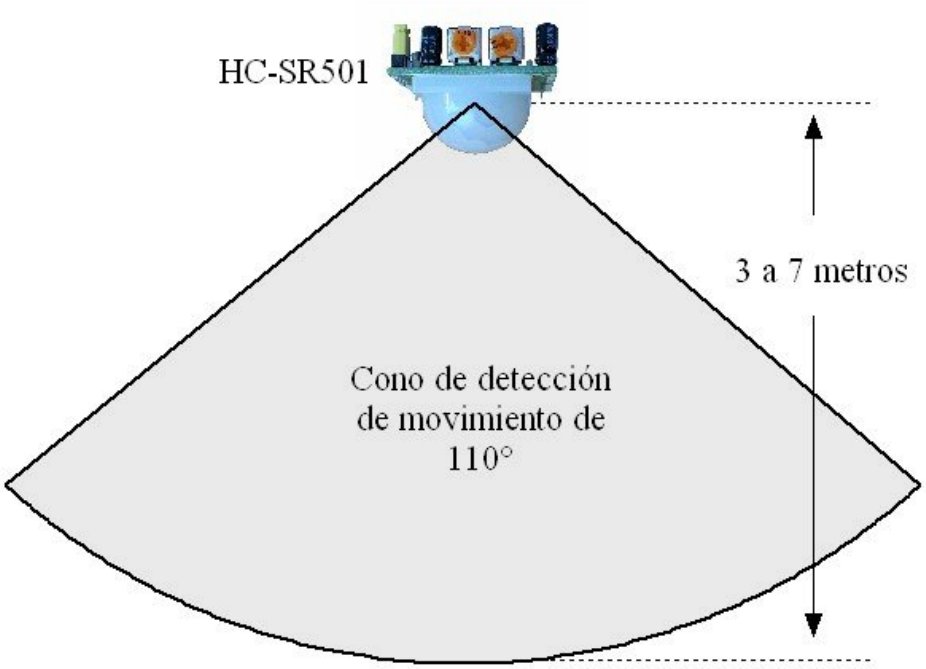
- Ajuste de parámetros: mediante 2 potenciómetros, el usuario puede modificar tanto la sensibilidad como la distancia de detección del PIR.

- Detección automática de luz (esta función no está disponible al adquirir el sensor de fábrica): por medio de una foto resistencia CdS (Sulfuro de Cadmio), se deshabilita la operación del sensor en caso que exista suficiente luz visible en el área. Esta función es utilizada en caso de sensores que enciendan lámparas en lugares poco iluminados durante la noche, y especialmente en corredores ó escaleras.



Rango de detección de los sensores PIR:

Como se indicó anteriormente, el rango de detección de movimiento de los PIR es ajustable y generalmente funcionan con alcances de hasta 7 metros, y con aperturas de 90° a 110°, como se muestra en la figura. El montaje del PIR puede realizarse tanto en piso, muro ó techo, según convenga a la aplicación.



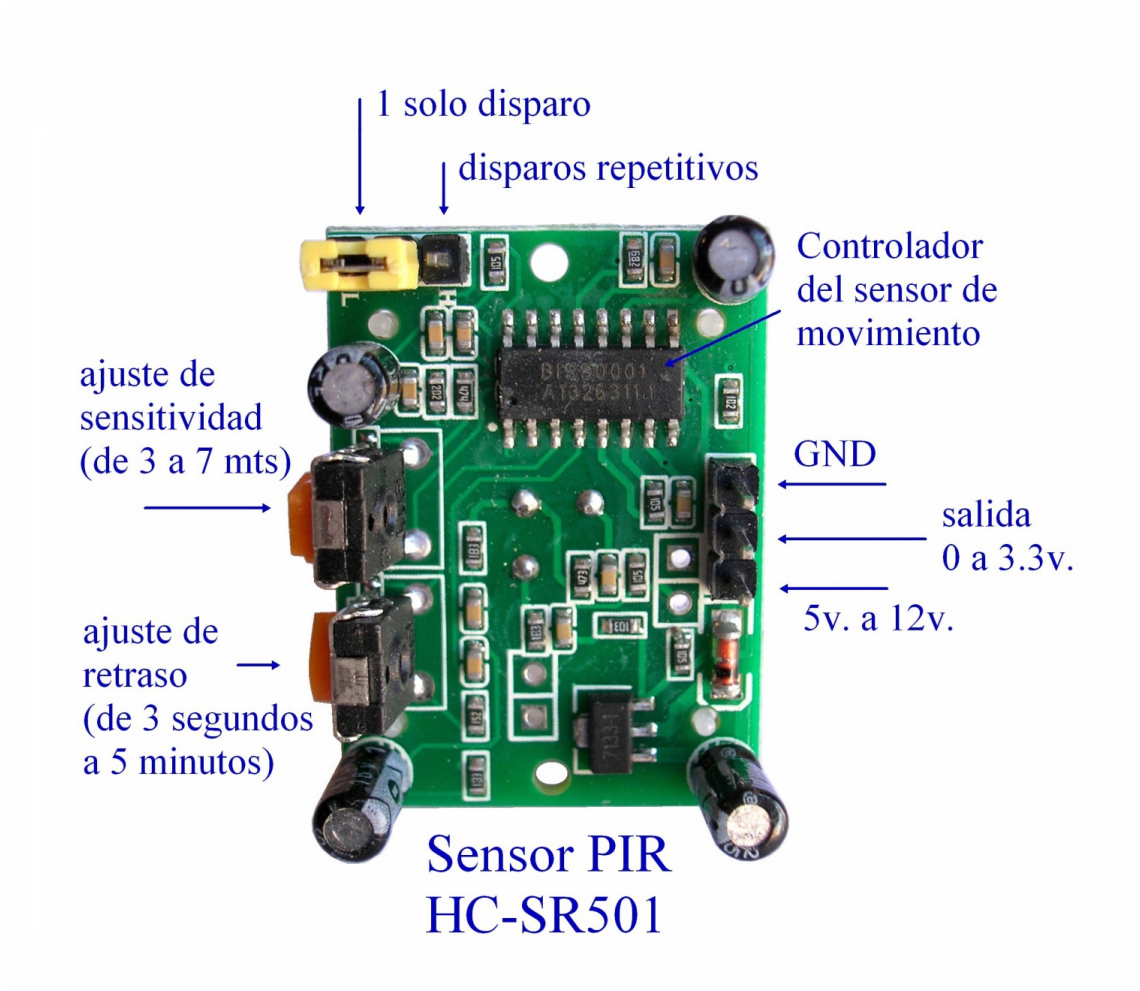
2. Descripción del HC-SR501

El módulo PIR modelo HC-SR501 es de bajo costo, pequeño, e incorpora la tecnología más reciente en sensores de movimiento. El sensor utiliza 2 potenciómetros y un jumper que permiten modificar sus parámetros y adaptarlo a las necesidades de la aplicación: sensitividad de detección, tiempo de activación, y respuesta ante detecciones repetitivas.

Sus especificaciones técnicas son:

- Usa el PIR LHI778 y el controlador BISS0001
- Voltaje de alimentación: de 5 a 12 VDC
- Consumo promedio: <1 miliampere
- Rango de distancia de 3 a 7 metros ajustable.

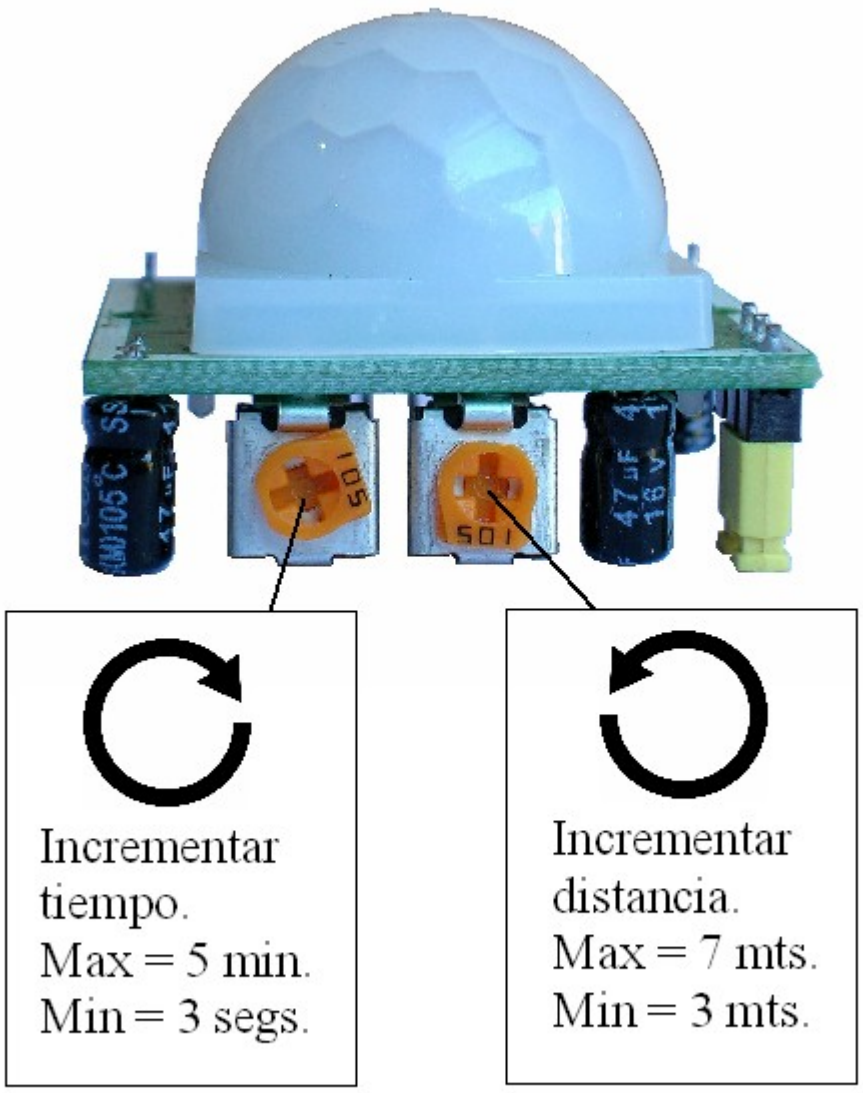
- Angulo de detección: cono de 110°
- Ajustes: 2 potenciómetros para ajuste de rango de detección y tiempo de alarma activa.
- Jumper para configurar la salida de alarma en modo mono-disparo ó disparo repetitivo (‘rettrigerable’)
- Salida de alarma de movimiento con ajuste de tiempo entre 3 segundos a 5 minutos.
- Salida de alarma activa Vo con nivel alto de 3.3 volts y 5 ma source, lista para conexión de un led, ó un transistor y relevador.
- Tiempo de inicialización: después de alimentar el módulo HC-SR05, debe transcurrir 1 minuto antes de que inicie su operación normal. Durante ese tiempo, es posible que el módulo active 2 ó 3 veces su salida.
- Tiempo de salida inactiva: cada vez que la salida pase de activa a inactiva, permanecerá en ese estado los siguientes 3 segundos. Cualquier evento que ocurra durante ese lapso es ignorado.
- Temperatura de operación: -15° a +70° C.
- Dimensiones: 3.2 x 2.4 x 1.8 cms



3. Ajustes y configuración del sensor:

Potenciómetros:

De acuerdo a la figura, el usuario puede ajustar tanto el tiempo de disparo de la señal de alarma de movimiento, como la distancia de detección. Los potenciómetros correspondientes deben girarse en la dirección mostrada para realizar los ajustes.



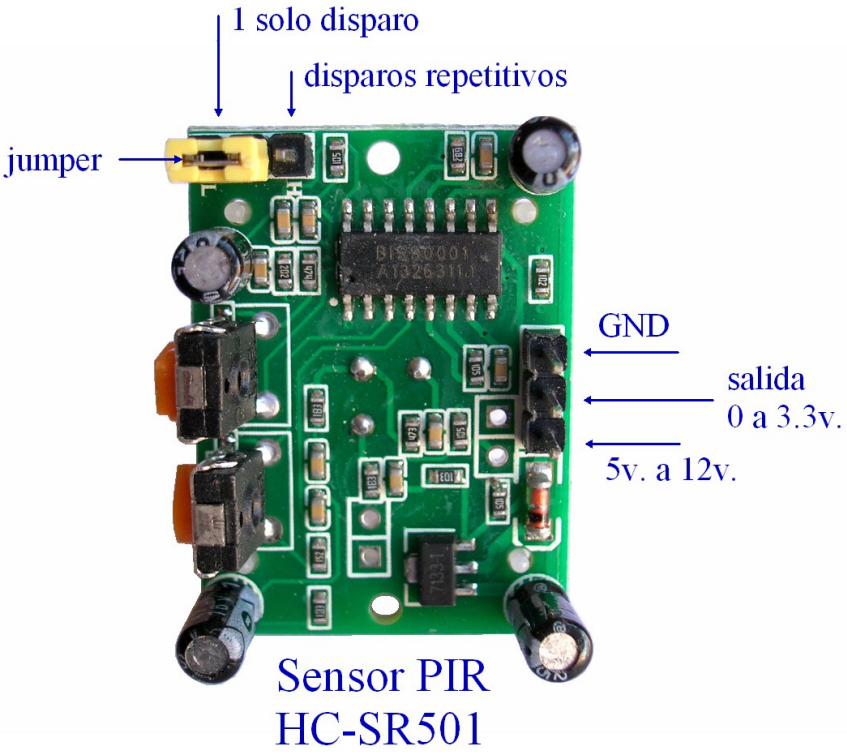
Posición del jumper:

De acuerdo a la imagen, el usuario puede trabajar en 2 modos de operación:

- 1 solo disparo: en este modo, cuando ocurre una detección de movimiento (el cual llamaremos 'evento'), la salida del sensor se activa durante el tiempo que se haya ajustado a través del potenciómetro correspondiente. Para efectos de ejemplo, supongamos que el tiempo de activación es de 60 segundos. Si durante esos 60 segundos ocurre un segundo evento, éste no será considerado.

- Disparos repetitivos: en este modo, cada evento detectado genera un nuevo tiempo de activación. Volviendo al ejemplo de tiempo de 60 segundos. Cuando ocurre el primer evento, la salida se activa. Si transcurridos 30 segundos ocurre un segundo evento, entonces se sumarán 60 segundos al tiempo transcurrido, dando un total de 90 segundos continuos con la salida activa. Y así, cada evento adicional, sumará un tiempo de 60 segundos de activación al tiempo ya transcurrido.

- En cualquier caso, si la salida regresa a su estado inactivo, habrá un lapso de 3 segundos durante los cuales los nuevos eventos no serán considerados. Pasados esos 3 segundos, el dispositivo regresa a su funcionamiento normal.



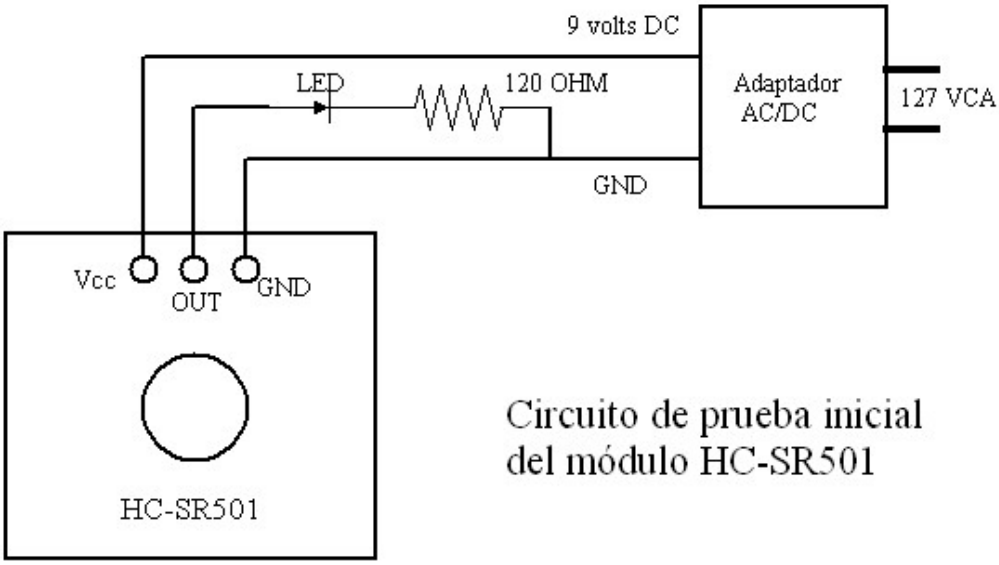
4. Pruebas preliminares del módulo HC-SR501:

En su aplicación más común, el sensor de movimiento es utilizado para activar luces en corredores y escaleras de inmuebles, de tal manera de ahorrar energía.

Para la realización de pruebas preliminares, en su conexión más simple, la salida del HC-SR501 se conecta a un LED, el cual encenderá cuando la alarma del sensor de movimiento esté activa.

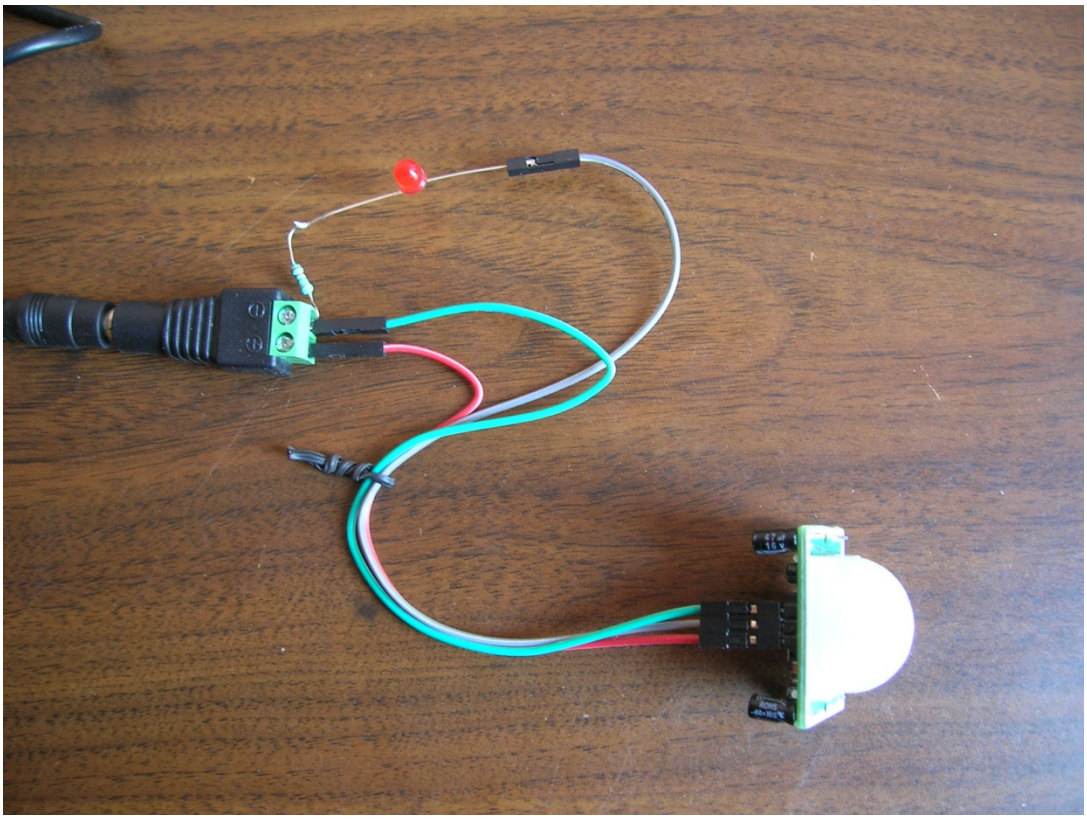
Mediante este sencillo circuito, pueden realizarse pruebas con los ajustes del sensor y comprobar sus parámetros.

El diagrama es el siguiente:



Circuito de prueba inicial
del módulo HC-SR501

En esta foto se muestra el circuito ensamblado. Se utiliza un convertidor de plug a terminal de tornillos para facilitar la conexión del adaptador AC/DC con el HC-SR501, por medio de cables dupont.

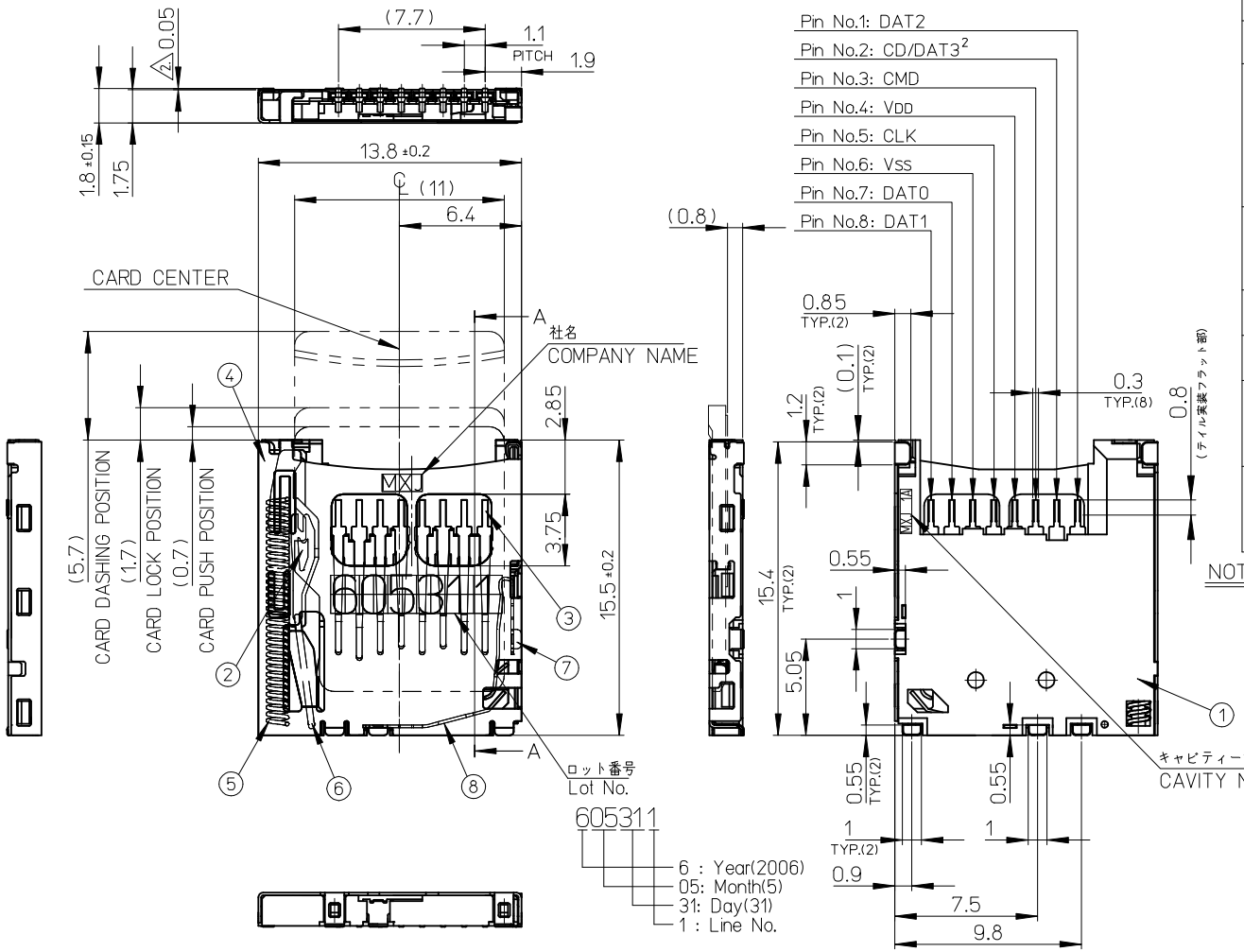


Consideraciones importantes durante las pruebas:

- Se recomienda iniciar las pruebas con los rangos mínimos: 3 segundos de tiempo de activación y 3 metros de distancia de detección (ver punto 3). El jumper posiciónelo de acuerdo a la imagen mostrada en el propio punto 3.

- Recuerde que una vez que transcurre el tiempo de activación de la alarma de movimiento, el led estará apagado durante 3 segundos. Durante ese lapso no será considerado ningún nuevo evento.

- Al alimentar por primera vez el módulo HC-SR501, durante el primer minuto, el módulo entra en modo de inicialización. Durante ese lapso no es considerado ningún evento.



番号 NO.	名 称 NAME	材 料 MATERIAL
①	ハウジング HOUSING	液晶ポリマー(LCP) UL94V-0 LIQUID CRYSTAL POLYMER (LCP) UL94V-0
②	カムスライダー CAM SLIDER	液晶ポリマー(LCP) UL94V-0 LIQUID CRYSTAL POLYMER (LCP) UL94V-0
③	ターミナル TERMINAL	銅合金 接触部：金めっき 0.5μm MIN. (t=0.2) 封孔処理済 テール部：錫めっき 2μm MIN. 下地：ニッケルめっき 1μm MIN. COPPER ALLOY, CONTACT AREA：Au(0.5μm MIN.) SEALING DISPOSITION TAIL AREA：Sn (2μm MIN.) UNDER：Ni(1μm MIN.)
④	シェル SHELL	ステンレス鋼 基板実装部：金めっき0.02μm MIN. (t=0.15) 下地：ニッケルめっき0.5μm MIN. STAINLESS STEEL, NAIL AREA：(0.02μm MIN.), UNDER：Ni(0.5μm MIN.)
⑤	スプリング SPRING	ピアノ線 SWP
⑥	ピン PIN	ステンレス鋼 STAINLESS STEEL
⑦	ディテクトレバー DETECT LEVER	銅合金 接触部、テール部：金めっき 0.2μm MIN. (t=0.15)下地：ニッケルめっき1μm MIN. COPPER ALLOY, CONTACT,TAIL AREA：Au(0.2μm MIN.) UNDER：Ni(1μm MIN.)
⑧	ディテクトスイッチ DETECT SWITCH	銅合金 接触部、テール部：金めっき 0.2μm MIN. (t=0.15)下地：ニッケルめっき1μm MIN. COPPER ALLOY, CONTACT,TAIL AREA：Au(0.2μm MIN.) UNDER：Ni(1μm MIN.)

NOTES
1. ターミナル及びネイルの平坦度は 0.1 MAX.
TERMINAL AND NAIL COPLANARITY TO BE 0.1 MAX.
2. スタンドオフ寸法 STAND OFF
3. パターン禁止エリア
PATTERN PROHIBITION AREA
4. カード検知スイッチ
DETECT SWITCH

カード挿入時 CARD INSERTING POSITION	クローズ CLOSE
カード未挿入時 NO CARD	オープン OPEN

5. 肉抜き位置は任意とする。CAVITY IS TO BE OPTIONAL.
6. ロット印字は任意とする。LOT NUMBERING IS TO BE OPTIONAL.
7. GND 推奨パターン GND RECOMMENDED PATTERN.
8. ELV 及び RoHS 適合品 ELV AND RoHS COMPLIANT

502570-0893	502570-0831	502570-08**
EMBOSSED TAPE	CONNECTOR ONLY	MODEL NO.
ORDER No. オーダー番号	MATERIAL NO.	

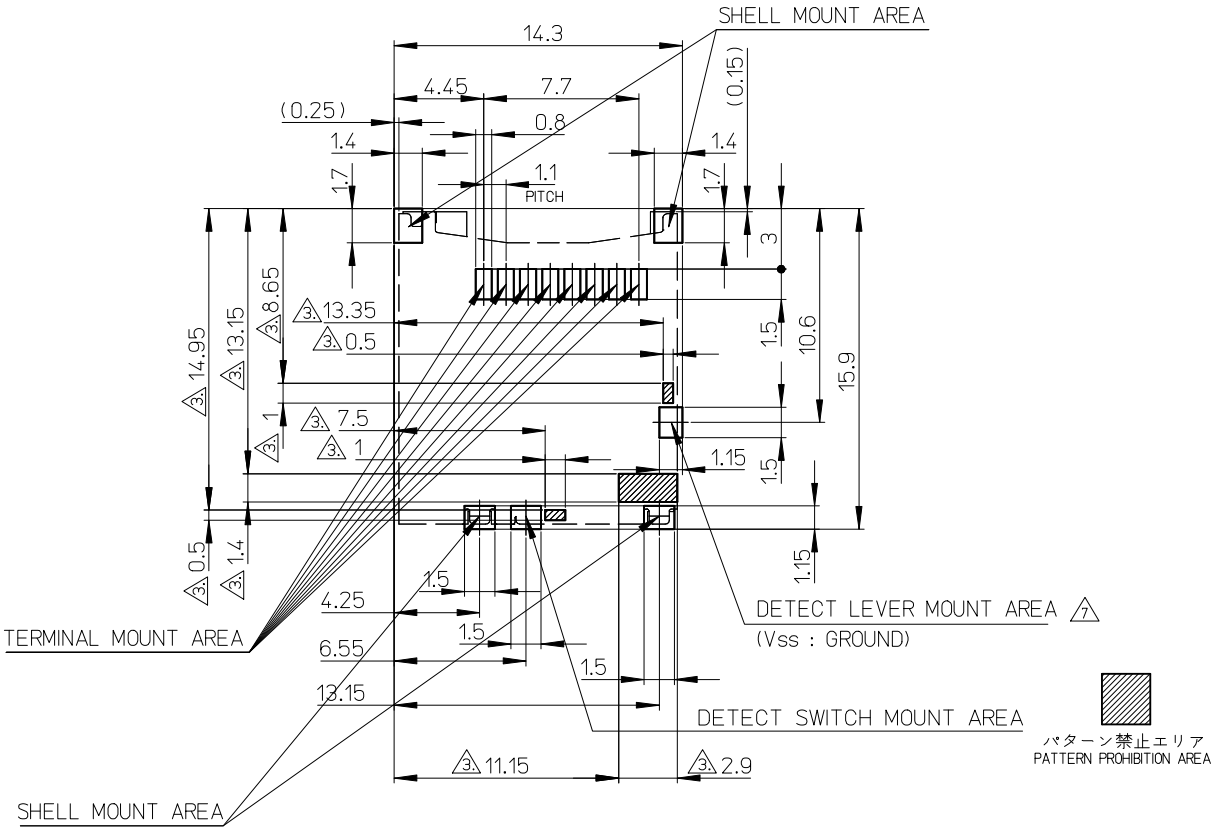
REVISED
EC NO: J2009-2308
DRWN:CARIZONO 2009/04/17
CHKD:T. HARUYAMA 2009/04/17
APPR:NUKITA 2009/04/20
REV: A
DESCRIPTION

GENERAL TOLERANCES (UNLESS SPECIFIED)

10 UNDER	±0.2
10 OVER 30 UNDER	±0.25
30 OVER	±0.3
ANGULAR	±1 °

DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS

DIMENSION STYLE: MM ONLY	SCALE: 4:1	DESIGN UNITS: METRIC	THIRD ANGLE PROJECTION
DRAWN BY: YMATSUMOTO	DATE: 07/09/10	TITLE: MICROSD CARD CONN. (P/P & NORMALSMALL TYPE)	
CHECKED BY: MTOMITA	DATE: 07/09/10		
APPROVED BY: MSASAO	DATE: 07/09/10	molex MOLEX INCORPORATED	
MATERIAL NO.: SEE TABLE	DOCUMENT NO.: SD-502570-001		SHEET NO.: 1 OF 2
SIZE: A3	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		



RECOMMENDED
PCB PATTERN LAYOUT

(GENERAL TOLERANCE : ±0.05)

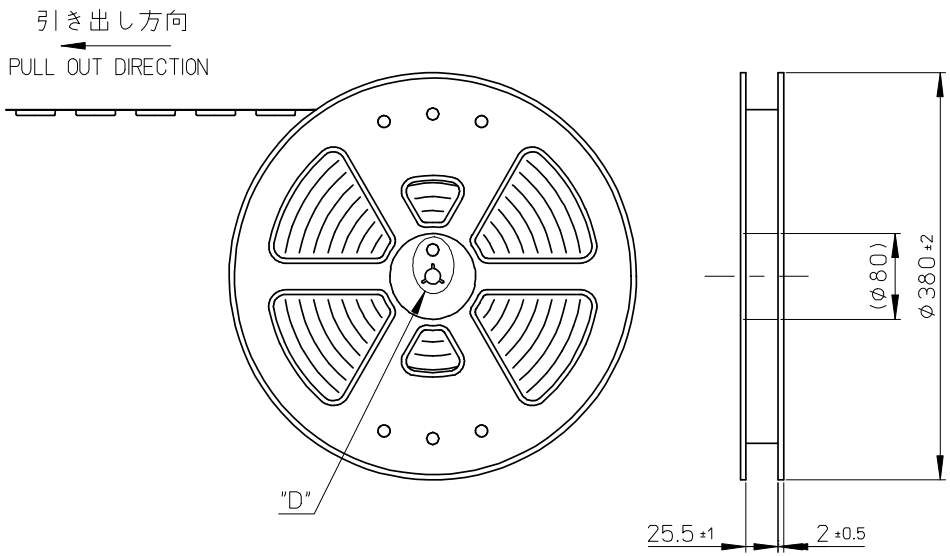
REVISED			
EC NO: J2009-2308			
DRWN:CARIZONO	2009/04/17		
CH'KD:T. HARUYAMA	2009/04/17		
APPR:NUKITA	2009/04/20		
A		DESCRIPTION	REV

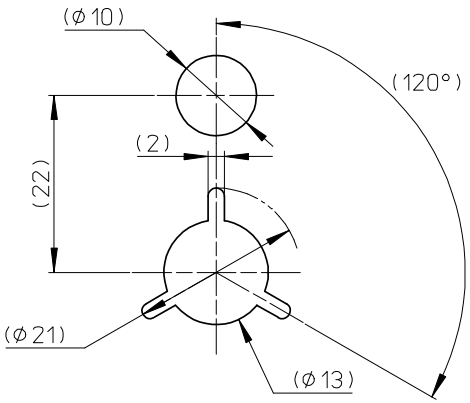
GENERAL TOLERANCES (UNLESS SPECIFIED)

10 UNDER	±0.2
10 OVER 30 UNDER	±0.25
30 OVER	±0.3
ANGULAR ±1 °	

DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS

DIMENSION STYLE: MM ONLY	SCALE: 4:1	DESIGN UNITS: METRIC	THIRD ANGLE PROJECTION
DRAWN BY: YMATSUMOTO	DATE: 07/09/10	TITLE: MICROSD CARD CONN. (P/P & NORMALSMALL TYPE)	
CHECKED BY: MTOMITA	DATE: 07/09/10		
APPROVED BY: MSASAO	DATE: 07/09/10	molex MOLEX INCORPORATED	
MATERIAL NO.: SEE SHEET 1		DOCUMENT NO.: SD-502570-001	SHEET NO.: 2 OF 2
SIZE: A3	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		

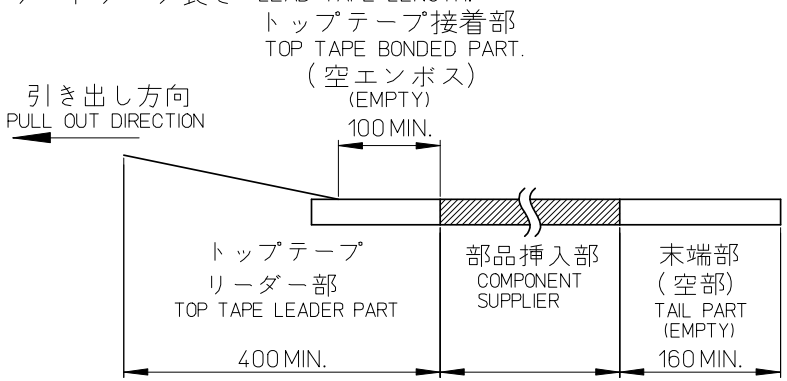




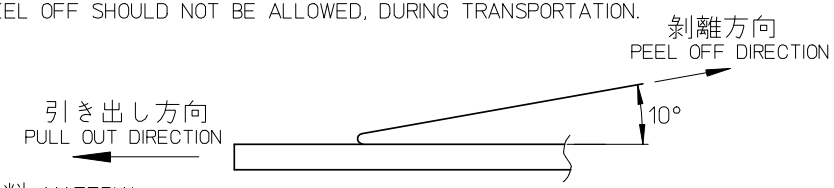
DETAIL "D"

NOTES

1. 製品詳細寸法については、SD 図面を参照下さい。
   RE DETAILED DIMENSION, SEE SALES DRAWING.
2. 梱包数量：1300 個／リール
   NUMBER OF CONNECTORS : 1300 PCS/REEL.
3. リードテープ長さ LEAD TAPE LENGTH.



4. トップテープの剥離強度： JIS C0806-3に準拠(剥離方向は下図参照)
   尚、本規格値は出荷時に適用。(但し、輸送時に剥離が発生しないこと。)
   PEELING OFF FORCE OF TOP TAPE . BASED UPON JIS C0806-3
   (PEELING DIRECTION AS SHOWN IN FOLLOWING FIG.)
   THIS REQUIREMENT SHOULD BE APPLIED AT SHIPMENT.
   PEEL OFF SHOULD NOT BE ALLOWED, DURING TRANSPORTATION.



5. 材料 MATERIAL
   キャリアテープ (CARRIER TAPE)：ポリスチレン (POLYSTYRENE)
   トップテープ (TOP TAPE) : PET, PE, PEF
   リール (REEL) : ポリスチレン(PS) ＜リサイクル材含む＞
   POLYSTYRENE (PS)<RECYCLE MATERIAL CONTAINED>

8. ELV及びRoHS適合品 ELV AND RoHS COMPLIANT

502570-0831	502570-0893	502570-08**
CONNECTOR	MATERIAL NO.	MODEL NO.

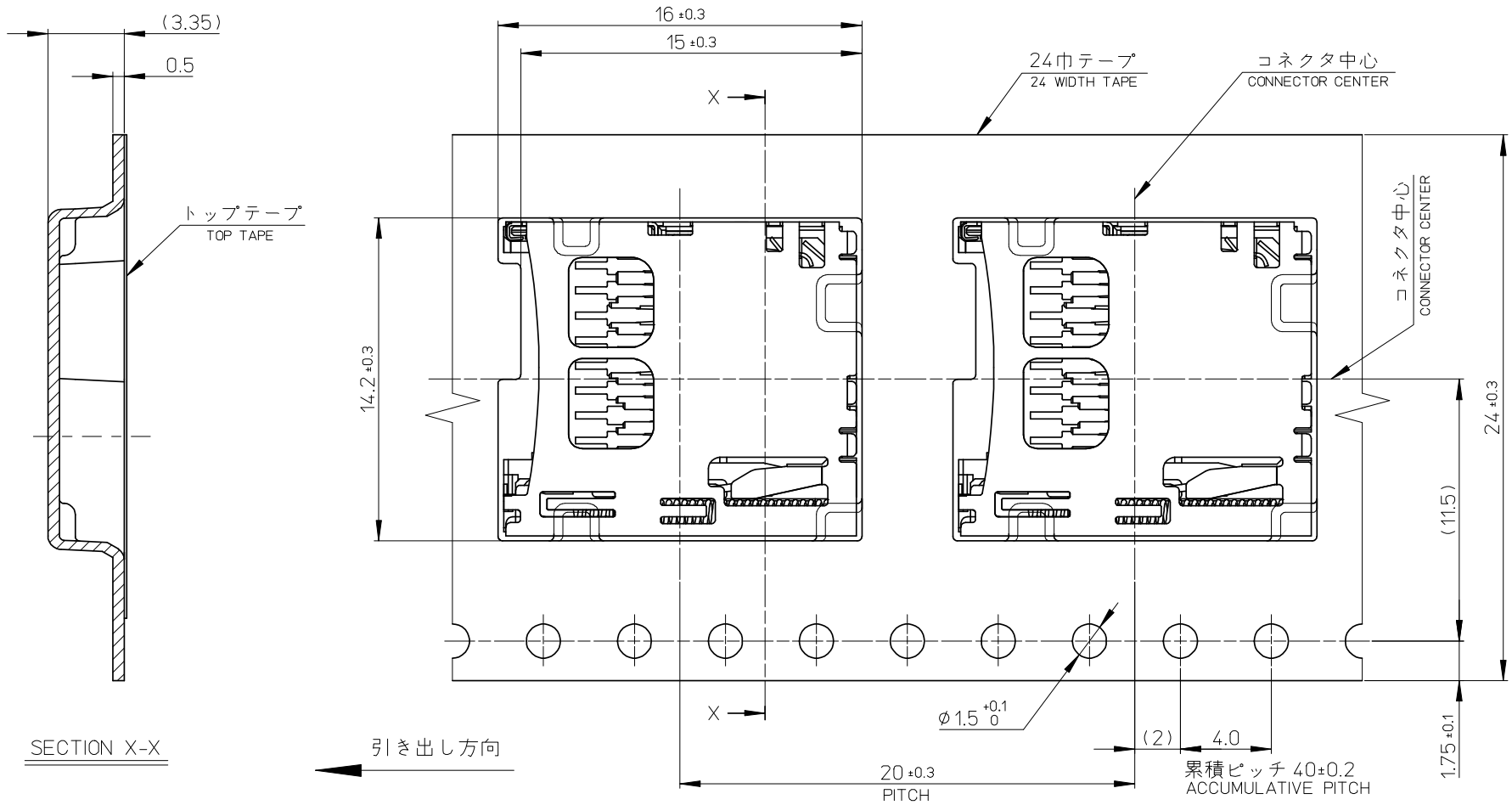
RELEASED
EC NO: J2008-3223
DRWN:HYAJIMA 2008/03/10
CH'KD:THARUYAMA 2008/03/11
APPR:NUKITA 2008/03/11
DESCRIPTION
REV 0

GENERAL TOLERANCES (UNLESS SPECIFIED)

10 UNDER	±0.2
10 OVER 30 UNDER	±0.25
30 OVER	±0.3
ANGULAR ±1 °	

DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS

DIMENSION STYLE: MM ONLY	SCALE: 4:1	DESIGN UNITS: METRIC	THIRD ANGLE PROJECTION
DRAWN BY: YMATSUMOTO	DATE: 07/09/10	TITLE: MICROSD CARD CONN. EMBOSSED TYPE PACKAGE FOR 502570-08**	
CHECKED BY: MTOMITA	DATE: 07/09/10		
APPROVED BY: MSASAO	DATE: 07/09/10	molex MOLEX INCORPORATED	
MATERIAL NO.: SEE TABLE		DOCUMENT NO.: SD-502570-002	SHEET NO.: 1 OF 2
SIZE: A3	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		



RELEASED			
EC NO: J2008-3223			
DRWN:HYAJIMA	2008/03/10		
CH'KD:THARUYAMA	2008/03/11		
APPR:NUKITA	2008/03/11		
0	REV	DESCRIPTION	

GENERAL TOLERANCES (UNLESS SPECIFIED)

10 UNDER	±0.2
10 OVER 30 UNDER	±0.25
30 OVER	±0.3
ANGULAR ±1 °	

DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS

DIMENSION STYLE: MM ONLY	SCALE: 4:1	DESIGN UNITS: METRIC	THIRD ANGLE PROJECTION
DRAWN BY: YMATSUMOTO	DATE: 07/09/10	TITLE: MICROSD CARD CONN. EMBOSSED TYPE PACKAGE FOR 502570-08**	
CHECKED BY: MTOMITA	DATE: 07/09/10		
APPROVED BY: MSASAO	DATE: 07/09/10	molex MOLEX INCORPORATED	
MATERIAL NO.: SEE SHEET 1		DOCUMENT NO.: SD-502570-002	SHEET NO.: 2 OF 2
SIZE: A3	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		

OV2640 Color CMOS UXGA (2.0 MegaPixel) CAMERACHIP™ with OmniPixel2™ Technology

General Description

The OV2640 CAMERACHIP™ is a low voltage CMOS image sensor that provides the full functionality of a single-chip UXGA (1632x1232) camera and image processor in a small footprint package. The OV2640 provides full-frame, sub-sampled, scaled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 15 frames per second (fps) in UXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, white pixel canceling, noise canceling, and more, are also programmable through the SCCB interface. The OV2640 also includes a compression engine for increased processing power. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable color image.

Note: The OV2640 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable apps
- Standard SCCB interface
- Output support for Raw RGB, RGB (RGB565/555), GRB422, YUV (422/420) and YCbCr (4:2:2) formats
- Supports image sizes: UXGA, SXGA, SVGA, and any size scaling down from SXGA to 40x30
- VarioPixel® method for sub-sampling
- Automatic image control functions including Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, gamma, sharpness (edge enhancement), lens correction, white pixel canceling, noise canceling, and 50/60 Hz luminance detection
- Line optical black level output capability
- Video or snapshot operation
- Zooming, panning, and windowing functions
- Internal/external frame synchronization
- Variable frame rate control
- Supports LED and flash strobe mode
- Supports scaling
- Supports compression
- Embedded microcontroller

Ordering Information

Product	Package
OV02640-VL9A (Color, lead-free)	38-pin CSP2

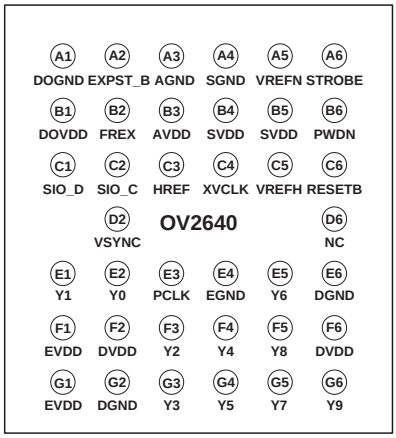
Applications

- Cellular and Camera Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Array Size	**UXGA**	1600 x 1200
Power Supply	**Core**	1.2VDC ± 5%
	Analog	2.5 ~ 3.0VDC
	I/O	1.7V to 3.3V
Power Requirements	**Active**	125 mW (for 15 fps, UXGA YUV mode)
		140 mW (for 15 fps, UXGA compressed mode)
	Standby	600 µA
Temperature Range	**Operation**	-30°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV(422/420)/YCbCr422 • RGB565/555 • 8-bit compressed data • 8-/10-bit Raw RGB data
Lens Size		1/4"
Chief Ray Angle		25° non-linear
Maximum Image Transfer Rate	**UXGA/SXGA**	15 fps
	SVGA	30 fps
	CIF	60 fps
Sensitivity		0.6 V/Lux-sec
S/N Ratio		40 dB
Dynamic Range		50 dB
Scan Mode		Progressive
Maximum Exposure Interval		1247 x t_{ROW}
Gamma Correction		Programmable
Pixel Size		2.2 µm x 2.2 µm
Dark Current		15 mV/s at 60°C
Well Capacity		12 Ke
Fixed Pattern Noise		<1% of $V_{PEAK-TO-PEAK}$
Image Area		3590 µm x 2684 µm
Package Dimensions		5725 µm x 6285 µm

Figure 1 OV2640 Pin Diagram (Top View)



Functional Description

Figure 2 shows the functional block diagram of the OV2640 image sensor. The OV2640 includes:

- Image Sensor Array (1632 x 1232 total image array)
- Analog Signal Processor
- 10-Bit A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Compression Engine
- Microcontroller
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram

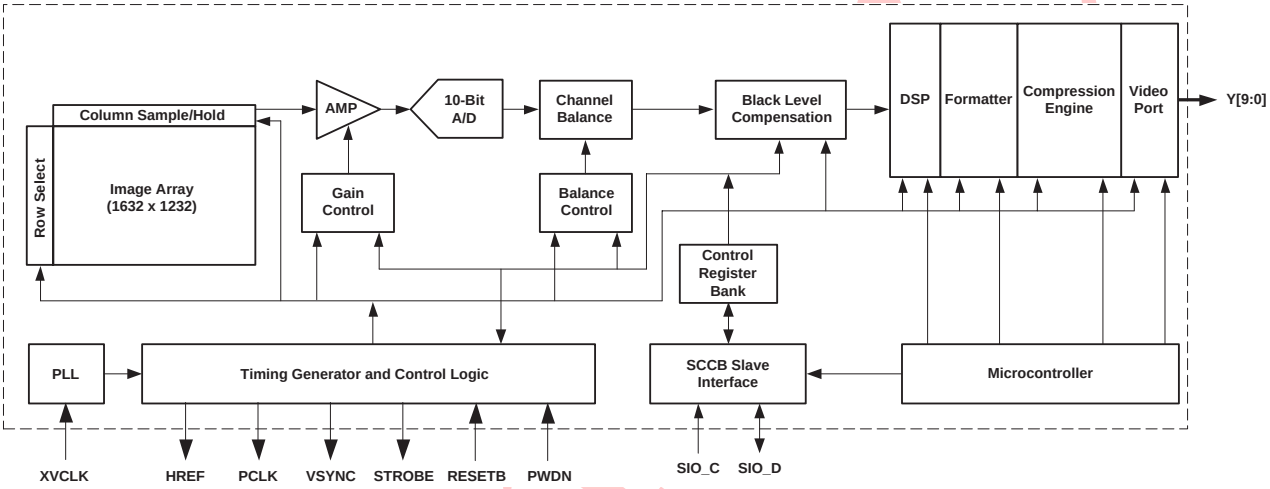
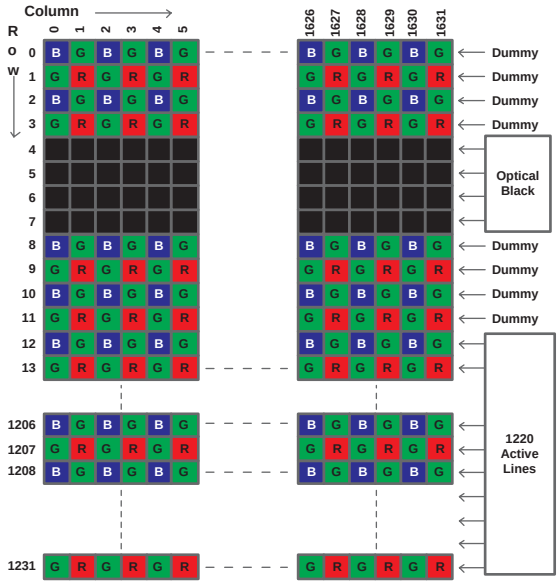


Image Sensor Array

The OV2640 sensor has an image array of 1632 columns by 1232 rows (2,010,624 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Sensor Array Region Color Filter Layout



The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 2,010,624 pixels, 1,991,040 (1632x1220) are active. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

Analog Amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain Control

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC).

10-Bit A/D Converters

After the analog amplifier, the bayer pattern Raw signal is fed to two 10-bit analog-to-digital (A/D) converters, one for G channel and one shared by the BR channels. These A/D converters operate at speeds up to 20 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

Channel Balance

The amplified signals are then balanced with a channel balance block. In this block, the Red/Blue channel gain is increased or decreased to match Green channel luminance level.

Balance Control

Channel Balance can be done manually by the user or by the internal automatic white balance (AWB) controller.

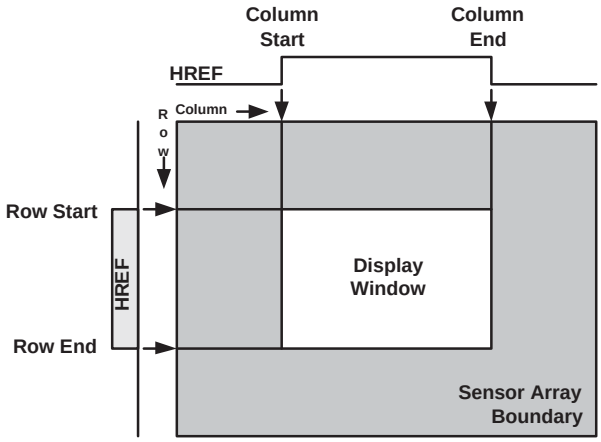
Black Level Compensation

After the pixel data has been digitized, black level calibration can be applied before the data is output. The black level calibration block subtracts the average signal level of optical black pixels to compensate for the dark current in the pixel output. The user can disable black level calibration.

Windowing

The OV2640 allows the user to define window size or region of interest (ROI), as required by the application. Window size setting (in pixels) ranges from 2 x 4 to 1632 x 1220 (UXGA) or 2 x 2 to 818 x 610 (SVGA), and 408 x 304 (CIF), and can be anywhere inside the 1632 x 1220 boundary. Note that modifying window size or window position does not alter the frame or pixel rate. The windowing control merely alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical ROI. The default window size is 1600 x 1200. Refer to Figure 4 and registers HREFST, HREFEND, REG32, VSTRT, VEND, and COM1 for details.

Figure 4 Windowing



Zooming and Panning Mode

The OV2640 provides zooming and panning modes. The user can select this mode under SVGA/CIF mode timing. The related zoom ratios will be 2:1 of UXGA for SVGA and 4:1 of UXGA for CIF. Registers ZOOMS[7:0] (0x49) and COM19[1:0] (0x48) define the vertical line start point. Register ARCOM2[2] (0x34) defines the horizontal start point.

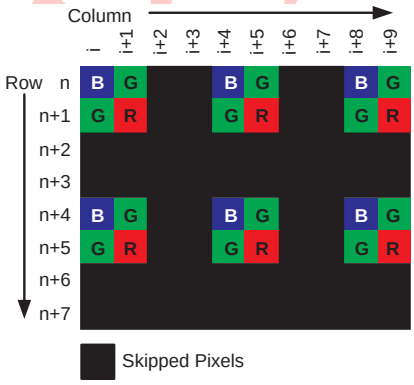
Sub-sampling Mode

The OV2640 supports two sub-sampling modes. Each sub-sampling mode has different resolution and maximum frame rate. These modes are described in the following sections.

SVGA mode

The OV2640 can be programmed to output 800 x 600 (SVGA) sized images for applications where higher resolution image capture is not required. In this mode, both horizontal and vertical pixels will be sub-sampled with an aspect ratio of 4:2 as shown in Figure 5.

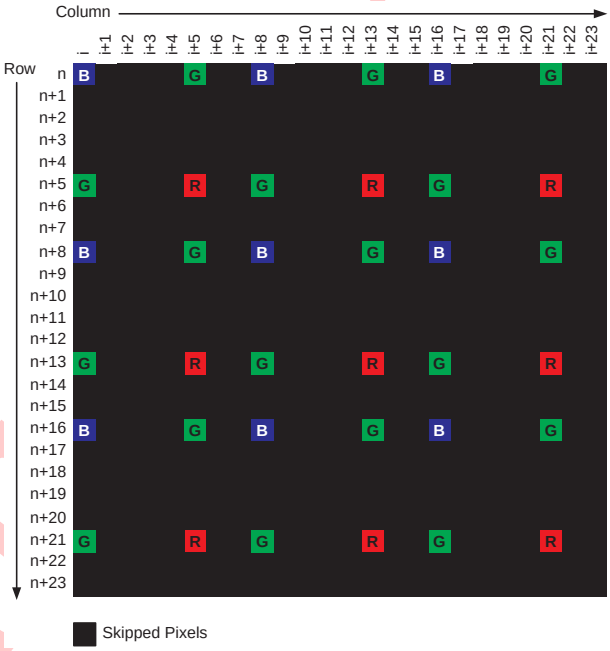
Figure 5 SVGA Sub-Sampling Mode



CIF Mode

The OV2640 can also operate at a higher frame rate to output 400 x 296 sized images. Figure 6 shows the sub-sampling diagram in both horizontal and vertical directions for CIF mode.

Figure 6 CIF Sub-Sampling Mode



Timing Generator and Control Logic

In general, the timing generator controls the following:

- Frame Exposure Mode Timing
- Frame Rate Adjust
- Frame Rate Timing

Frame Exposure Mode Timing

The OV2640 supports frame exposure mode. Typically, the frame exposure mode must work with the aid of an external shutter.

The frame exposure pin, FREX (pin B2), is the frame exposure mode enable pin and the EXPST_B pin (pin A2) serves as the sensor's exposure start trigger. When the external master device asserts the FREX pin high, the sensor array is quickly pre-charged and stays in reset mode until the EXPST_B pin goes low (sensor exposure time can be defined as the period between EXPST_B low and shutter close). After the FREX pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data

output, the OV2640 will output continuous live video data unless in single frame transfer mode. Figure 18 and Figure 19 show the detailed timing and Table 11 shows the timing specifications for this mode.

Frame Rate Adjust

The OV2640 offers three methods for frame rate adjustment:

- Clock prescaler: (see "CLKRC" on page 23)
  By changing the system clock divide ratio and PLL, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 … 1/64 of the input clock rate.
- Line adjustment: (see "REG2A" on page 26 and "FRARL" on page 26)
  By adding a dummy pixel timing in each line (between HSYNC and pixel data out), the frame rate can be changed while leaving the pixel rate as is.
- Vertical sync adjustment:
  By adding dummy line periods to the vertical sync period (see "ADDVSL" on page 26 and "ADDVSH" on page 26 or see "FLL" on page 27 and "FLH" on page 27), the frame rate can be altered while the pixel rate remains the same.

Frame Rate Timing

Default frame timing is illustrated in Figure 15, Figure 16, and Figure 17. Refer to Table 1 for the actual pixel rate at different frame rates.

Table 1 Frame/Pixel Rates in UXGA Mode

Frame Rate (fps)	15	7.5	2.5	1.25
PCLK (MHz)	36	18	6	3

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit
- White pixel canceling
- De-noise

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Scaling Image Output

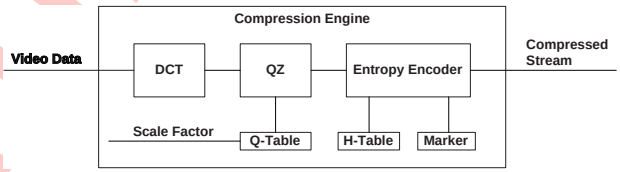
The OV2640 is capable of scaling down the image size from CIF to 40x30. By using SCCB registers, the user can output the desired image size. At certain image sizes, HREF is not consistent in a frame.

Compression Engine

As shown in Figure 7, the Compression Engine consists of three major blocks:

- DCT
- QZ
- Entropy Encoder

Figure 7 Compression Engine Block Diagram



Microcontroller

The OV2640 embeds an 8-bit microcontroller with 512-byte data memory and 4 KB program memory. It provides the flexibility of decoding protocol commands from the host for controlling the system, as well as the ability to fine tune image quality.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Slave Operation Mode

The OV2640 can be programmed to operate in slave mode (default is master mode).

When used as a slave device, COM7[3] (0x12), CLKRC[6] (0x11), and COM2[2] (0x09) register bits should be set to

"1" and the OV2640 will use PWDN and RESETB pins as vertical and horizontal synchronization triggers supplied by a master device. The master device must provide the following signals:

1. System clock MCLK to XVCLK pin
2. Horizontal sync MHSYNC to RESETB pin
3. Vertical frame sync MVSYNC to PWDN pin

See Figure 8 for slave mode connections and Figure 9 for detailed timing considerations.

Figure 8 Slave Mode Connection

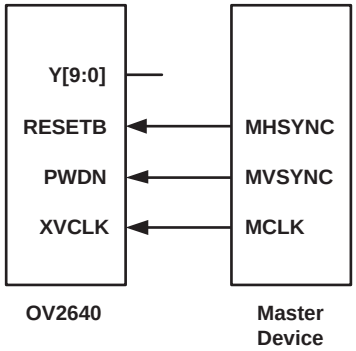
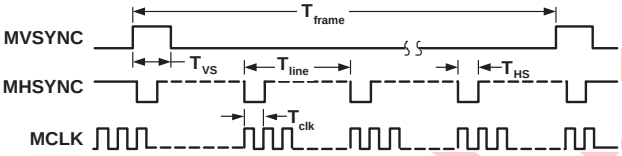


Figure 9 Slave Mode Timing



NOTE:

1) $T_{HS} > 6\ T_{clk}$, $Tvs > T_{line}$
2) $T_{line} = 1922 \times T_{clk}$ (UXGA); $T_{line} = 1190 \times T_{clk}$ (SVGA); $T_{line} = 595 \times T_{clk}$ (CIF)
3) $T_{frame} = 1248 \times T_{line}$ (UXGA); $T_{frame} = 672 \times T_{line}$ (SVGA); $T_{frame} = 336 \times T_{line}$ (CIF)

Strobe Mode

The OV2640 has a Strobe mode that allows it to work with an external flash and LED.

Reset

The OV2640 includes a RESETB pin (pin C6) that forces a complete hardware reset when it is pulled low (GND). The OV2640 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface.

Power Down Mode

Two methods are available to place the OV2640 into power-down mode: hardware power-down and SCCB software power-down.

To initiate hardware power-down, the PWDN pin (pin B6) must be tied to high. When this occurs, the OV2640 internal device clock is halted and all internal counters are reset. The current draw is less than 15 µA in this standby mode.

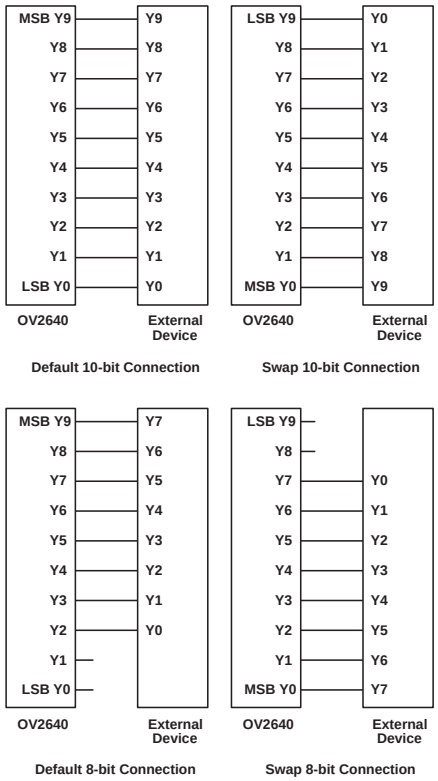
Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. The current requirements drop to less than 1 mA in this mode. All register content is maintained in standby mode.

Digital Video Port

MSB/LSB Swap

The OV2640 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 10 shows some examples of connections with external devices.

Figure 10 Connection Examples



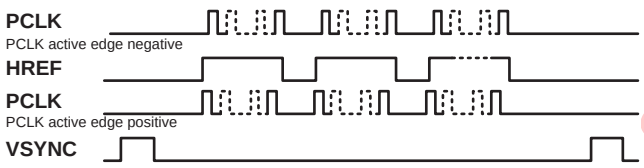
Line/Pixel Timing

The OV2640 digital video port can be programmed to work in either master or slave mode.

In both master and slave modes, pixel data output is synchronous with PCLK (or MCLK if port is a slave), HREF, and VSYNC. The default PCLK edge for valid data is the negative edge but may be programmed using register COM10[4] for the positive edge. Basic line/pixel output timing and pixel timing specifications are shown in Figure 14 and Table 10.

Also, using register COM10[5], PCLK output can be gated by the active video period defined by the HREF signal. See Figure 11 for details.

Figure 11 PCLK Output Only at Valid Pixels



The specifications shown in Table 10 apply for DVDD = +1.2 V, DOVDD = +2.8 V, T_A = 25°C, sensor working at 15 fps, external loading = 20 pF.

Pixel Output Pattern

Table 2 shows the output data order from the OV2640. The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$… $B_{0,1598}$ $G_{0,1599}$. After the second HREF the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$… $G_{1,1598}$ $R_{1,1599}$…, etc. If the OV2640 is programmed to output SVGA resolution data, horizontal and vertical sub-sampling will occur. The default output sequence for the first line of output will be: $B_{0,0}$ $G_{0,1}$ $B_{0,4}$ $G_{0,5}$… $B_{0,1596}$ $G_{0,1597}$. The second line of output will be: $G_{1,0}$ $R_{1,1}$ $G_{1,4}$ $R_{1,5}$… $G_{1,1596}$ $R_{1,1597}$.

Table 2 Data Pattern

R/C	0	1	2	3	. . .	1598	1599
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,1598}$	$G_{0,1599}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,1598}$	$R_{1,1599}$
2	$B_{2,0}$	$G_{2,1}$	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,1598}$	$G_{2,1599}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,1598}$	$R_{3,1599}$
. .					. .		
1198	$B_{1198,0}$	$G_{1198,1}$	$B_{1198,2}$	$G_{1198,3}$	. . .	$B_{1198,1598}$	$G_{1198,1599}$
1199	$G_{1199,0}$	$R_{1199,1}$	$G_{1199,2}$	$R_{1199,3}$	. . .	$G_{1199,1598}$	$R_{1199,1599}$

Pin Description

Table 3 Pin Description

Pin Location	Name	Pin Type	Function/Description
A1	DOGND	Ground	Ground for digital video port
A2	EXPST_B	Input	Snapshot Exposure Start Trigger 0: Sensor starts exposure (only effective in snapshot mode) 1: Sensor stays in reset mode Note: There is no internal pull-up/pull-down resistor.
A3	AGND	Ground	Ground for analog circuit
A4	SGND	Ground	Ground for sensor array
A5	VREFN	Reference	Internal analog reference - connect to ground using a 0.1 µF capacitor
A6	STROBE	I/O	Flash control output Default: Input Note: There is no internal pull-up/pull-down resistor.
B1	DOVDD	Power	Power for digital video port
B2	FREX	Input	Snapshot trigger - use to activate a snapshot sequence Note: There is no internal pull-up/pull-down resistor.
B3	AVDD	Power	Power for analog circuit
B4	SVDD	Power	Power for sensor array
B5	SVDD	Power	Power for sensor array
B6	PWDN	Input	Power-down mode enable, active high Note: There is an internal pull-down resistor.
C1	SIO_D	I/O	SCCB serial interface data I/O
C2	SIO_C	Input	SCCB serial interface clock input Note: There is no internal pull-up/pull-down resistor.
C3	HREF	I/O	Horizontal reference output Default: Input Note: There is no internal pull-up/pull-down resistor.
C4	XVCLK	Input	System clock input Note: There is no internal pull-up/pull-down resistor.
C5	VREFH	Reference	Internal analog reference - connect to ground using a 0.1 µF capacitor
C6	RESETB	Input	Reset mode, active low Note: There is an internal pull-up resistor.
D2	VSYNC	I/O	Vertical synchronization output Default: Input Note: There is no internal pull-up/pull-down resistor.
D6	NC	–	No connection
E1	Y1	I/O	Video port output bit[1] Default: Input Note: There is no internal pull-up/pull-down resistor.

Table 3 Pin Description

Pin Location	Name	Pin Type	Function/Description
E2	Y0	I/O	Video port output bit[0] Default: Input Note: There is no internal pull-up/pull-down resistor.
E3	PCLK	I/O	Pixel clock output Default: Input Note: There is no internal pull-up/pull-down resistor.
E4	EGND	Ground	Ground for internal regulator
E5	Y6	I/O	Video port output bit[6] Default: Input Note: There is no internal pull-up/pull-down resistor.
E6	DGND	Ground	Ground for digital core
F1	EVDD	Power	Power for internal regulator
F2	DVDD	Power	Sensor digital power (Core)
F3	Y2	I/O	Video port output bit[2] Default: Input Note: There is no internal pull-up/pull-down resistor.
F4	Y4	I/O	Video port output bit[4] Default: Input Note: There is no internal pull-up/pull-down resistor.
F5	Y8	I/O	Video port output bit[8] Default: Input Note: There is no internal pull-up/pull-down resistor.
F6	DVDD	Power	Sensor digital power (Core)
G1	EVDD	Power	Power for internal regulator
G2	DGND	Ground	Ground for digital core
G3	Y3	I/O	Video port output bit[3] Default: Input Note: There is no internal pull-up/pull-down resistor.
G4	Y5	I/O	Video port output bit[5] Default: Input Note: There is no internal pull-up/pull-down resistor.
G5	Y7	I/O	Video port output bit[7] Default: Input Note: There is no internal pull-up/pull-down resistor.
G6	Y9	I/O	Video port output bit[9] Default: Input Note: There is no internal pull-up/pull-down resistor.

Figure 12 Pinout Diagram

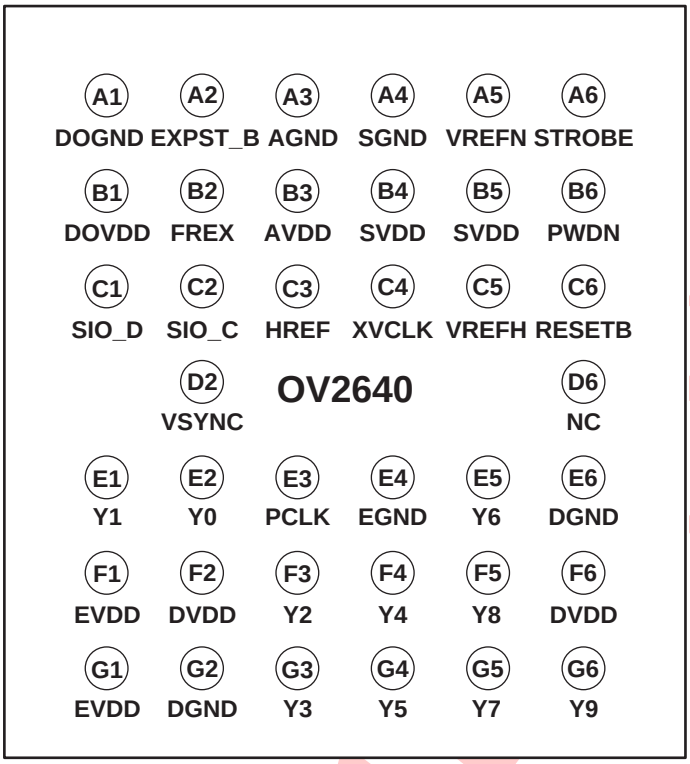


Table 4 Ball Matrix

	1	2	3	4	5	6
A	DOGND	EXPST_B	AGND	SGND	VREFN	STROBE
B	DOVDD	FREX	AVDD	SVDD	SVDD	PWDN
C	SIO_D	SIO_C	HREF	XVCLK	VREFN	RESETB
D		VSYNC				NC
E	Y1	Y0	PCLK	EGND	Y6	DGND
F	EVDD	DVDD	Y2	Y4	Y8	DVDD
G	EVDD	DGND	Y3	75	Y7	Y9

Electrical Characteristics

Table 5 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+1V
Lead-free Temperature, Surface-mount process		245ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 6 DC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD-A}	Supply voltage	2.5	2.8	3.0	V
V_{DD-D}	Supply voltage	1.14	1.2	1.26	V
V_{DD-IO}	Supply voltage[a]	1.71	2.8	3.3	V
I_{DDA-A}	Active (Operating) Current[b]		30	40	mA
I_{DDA-D}	Active (Operating) Current[b]		25 (YUV) 35 (Compressed)	35 (YUV) 50 (Compressed)	mA
I_{DDA-IO}	Active (Operating) Current[b]		6	10	mA
$I_{DDS-SCCB}$	Standby Current[b]		1	2	mA
$I_{DDS-PWDN}$			600	1200	µA
Digital Inputs					
V_{IL}	Input voltage LOW			0.54	V
V_{IH}	Input voltage HIGH	1.26			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF)					
V_{OH}	Output voltage HIGH	1.62			V
V_{OL}	Output voltage LOW			0.18	V
Serial Interface Inputs					
V_{IL}	SIO_C and SIO_D	-0.5	0	0.54	V
V_{IH}	SIO_C and SIO_D	1.26	1.8	2.3	V

a. 1.8V I/O is supported. Contact your local OmniVision FAE for further details.

b. V_{DD-A} = 2.8V, V_{DD-D} = 1.2V, and V_{DD-IO} = 1.8V for 15 fps in UXGA mode
$I_{DDS-SCCB}$ refers to SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to PWDN pad-initiated Standby

Table 7 AC Characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		20		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for UXGA/SVGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 8 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XVCLK)	6	24		MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%

Timing Specifications

Figure 13 SCCB Interface Timing Diagram

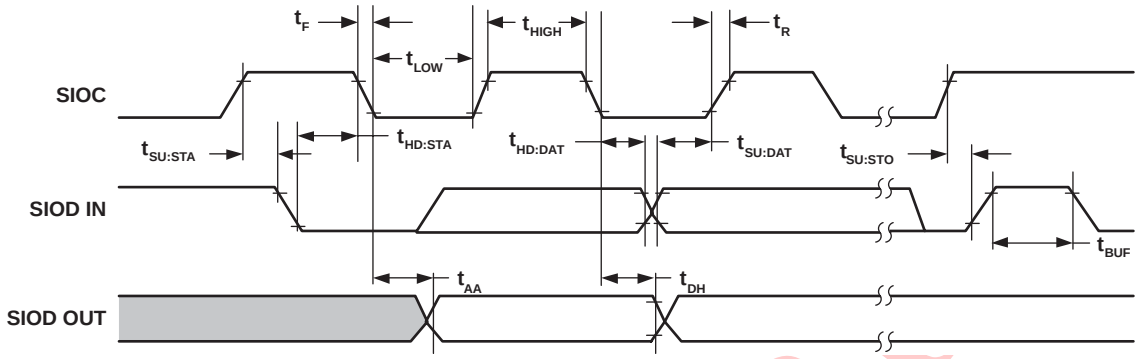


Table 9 SCCB InterfaceTiming Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIOC low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 14 UXGA, SVGA, and CIF Line/Pixel Output Timing

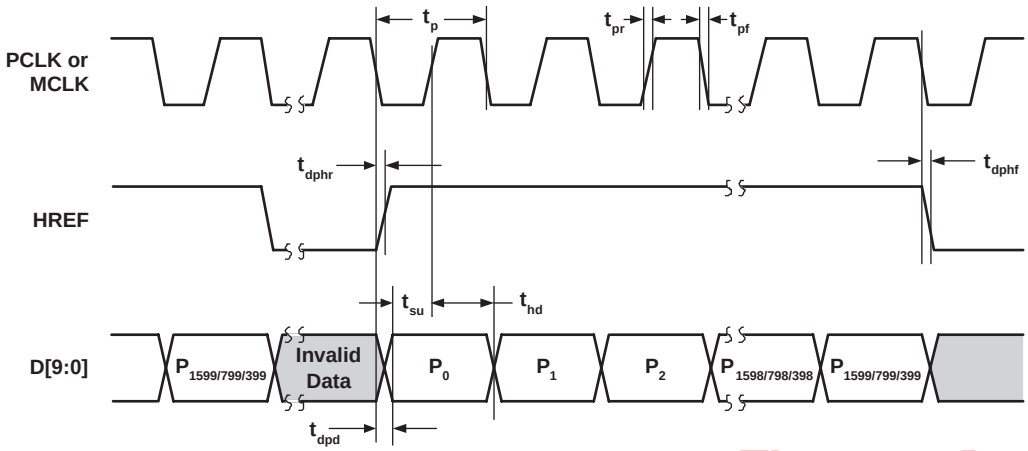


Table 10 Pixel Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		27.78		ns
t_{pr}	PCLK rising time		3.5		ns
t_{pf}	PCLK falling time		2.2		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 15 UXGA Frame Timing

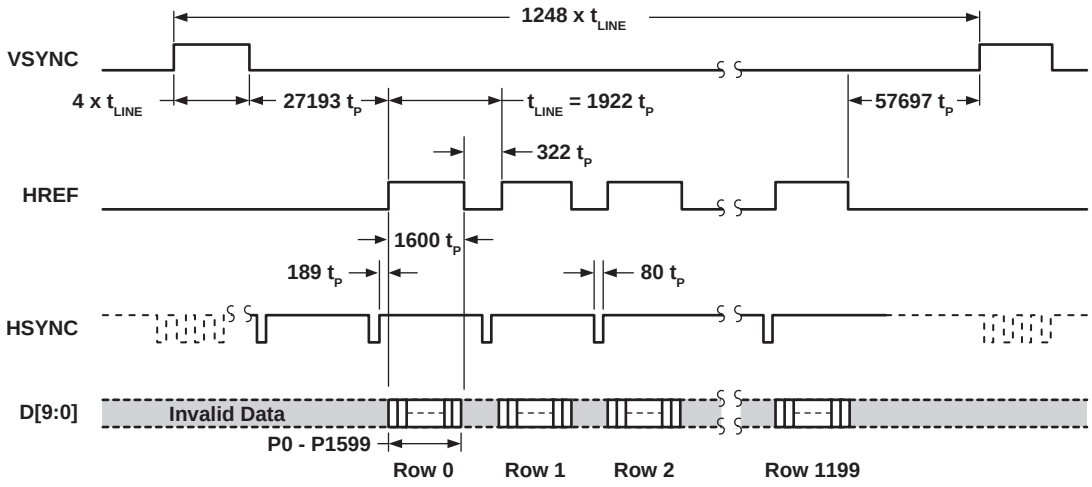


Figure 16 SVGA Frame Timing

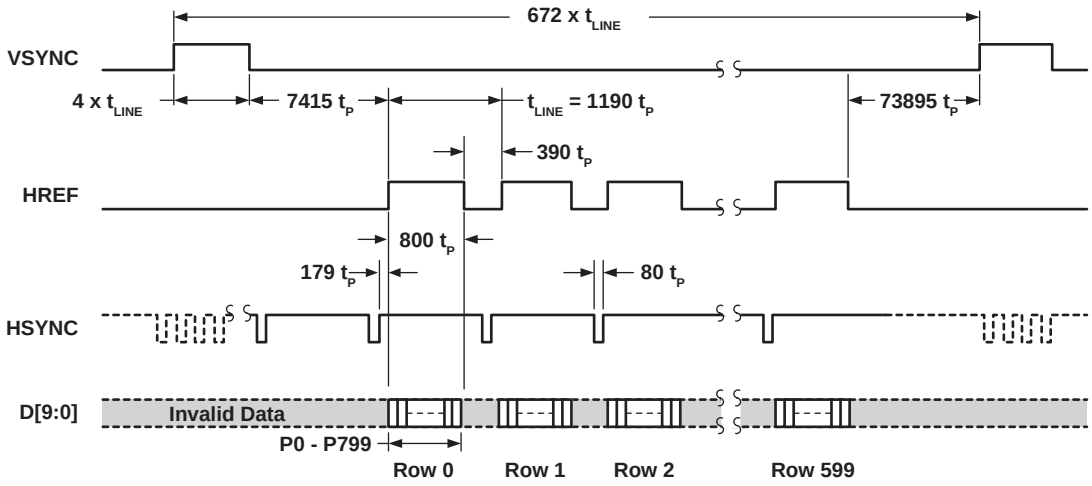


Figure 17 CIF Mode Frame Timing

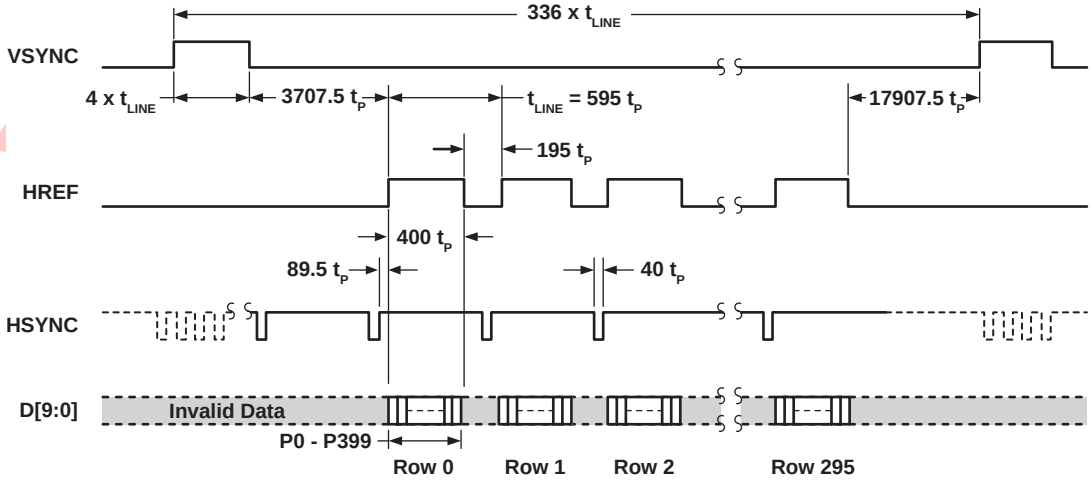


Figure 18 Frame Exposure Mode Timing with EXPST_B Staying Low

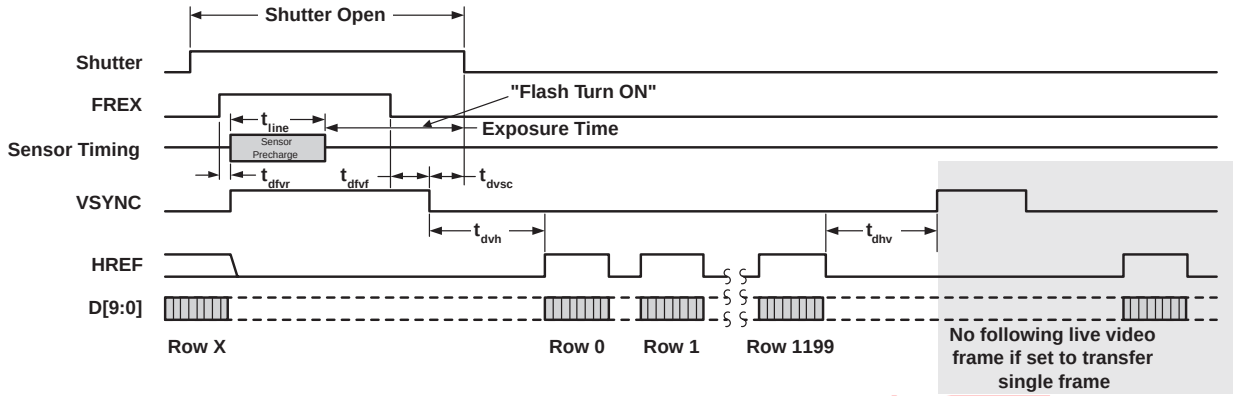


Figure 19 Frame Exposure Mode Timing with EXPST_B Asserted

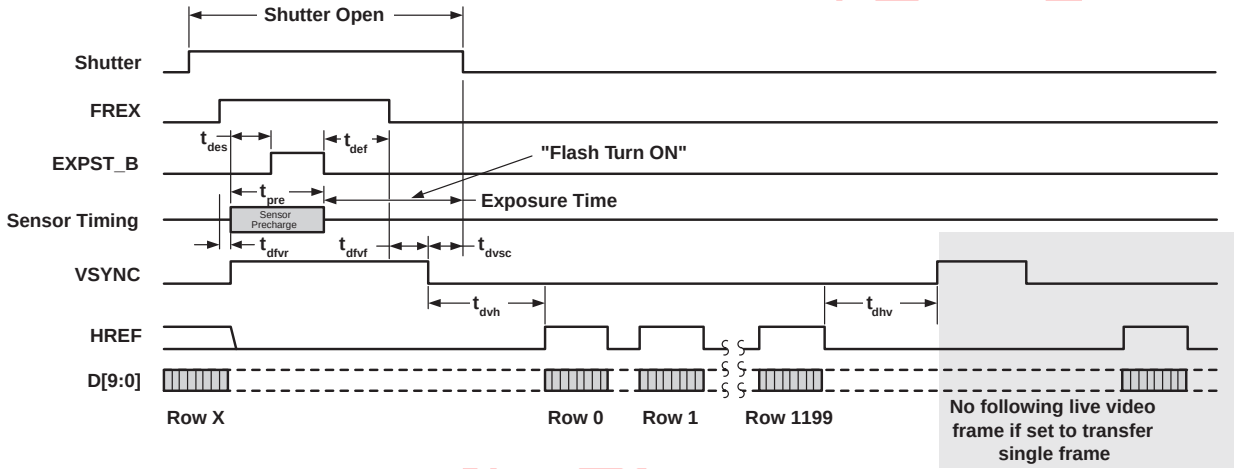


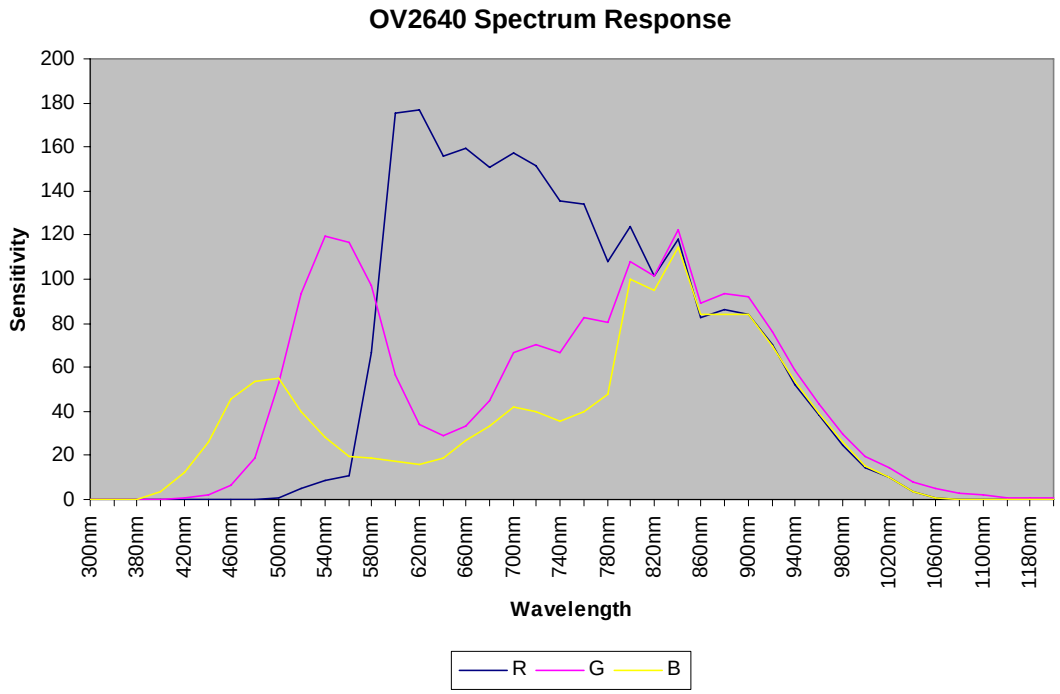
Table 11 Frame Exposure Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		1922 (UXGA)		tp
tvs		4		tline
tdfvr	8		9	tp
tdfvf			4	tline
tdvsc			2	tline
tdhv		38964 (UXGA)		tp
tdvh		15928 (UXGA)		tp
tdhso	0			ns
tdef	20			tp
tdes	8		1900 (UXGA)	tp

NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
2) Shutter must be closed no later then 3896 tp after VSYNC falling edge.

OV2640 Light Response

Figure 20 OV2640 Light Response



Register Set

Table 12 and Table 13 provides a list and description of the Device Control registers contained in the OV2640. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 60 for write and 61 for read.

There are two different sets of register banks. Register 0xFF controls which set is accessible. When register 0xFF=00, Table 12 is effective. When register 0xFF=01, Table 13 is effective.

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 1 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00-04	RSVD	XX	–	Reserved
05	R_BYPASS	0x1	RW	Bypass DSP Bit[7:1]: Reserved Bit[0]: Bypass DSP select 0: DSP 1: Bypass DSP, sensor out directly
06-43	RSVD	XX	–	Reserved
44	Qs	0C	RW	Quantization Scale Factor
45-4F	RSVD	XX	–	Reserved
50	CTRLl[7:0]	00	RW	Bit[7]: LP_DP Bit[6]: Round Bit[5:3]: V_DIVIDER Bit[2:0]: H_DIVIDER
51	HSIZE[7:0]	40	RW	H_SIZE[7:0] (real/4)
52	VSIZE[7:0]	F0	RW	V_SIZE[7:0] (real/4)
53	XOFFL[7:0]	00	RW	OFFSET_X[7:0]
54	YOFFL[7:0]	00	RW	OFFSET_Y[7:0]
55	VHYX[7:0]	08	RW	Bit[7]: V_SIZE[8] Bit[6:4]: OFFSET_Y[10:8] Bit[3]: H_SIZE[8] Bit[2:0]: OFFSET_X[10:8]
56	DPRP[7:0]	00	RW	Bit[7:4]: DP_SELY Bit[3:0]: DP_SELX
57	TEST[3:0]	00	RW	Bit[7]: H_SIZE[9] Bit[6:0]: Reserved
5A	ZMOW[7:0]	58	RW	OUTW[7:0] (real/4)
5B	ZMOH[7:0]	48	RW	OUTH[7:0] (real/4)
5C	ZMHH[1:0]	00	RW	Bit[7:4]: ZMSPD (zoom speed) Bit[2]: OUTH[8] Bit[1:0]: OUTW[9:8]
5D-7B	RSVD	XX	–	Reserved
7C	BPADDR[3:0]	00	RW	SDE Indirect Register Access: Address

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 2 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
7D	BPDATA[7:0]	00	RW	SDE Indirect Register Access: Data
7E-85	RSVD	XX	–	Reserved
86	CTRL2	0D	RW	Module Enable Bit[7:6]: Reserved Bit[5]: DCW Bit[4]: SDE Bit[3]: UV_ADJ Bit[2]: UV_AVG Bit[1]: Reserved Bit[0]: CMX
87	CTRL3	50	RW	Module Enable Bit[7]: BPC Bit[6]: WPC Bit[5:0]: Reserved
88-8B	RSVD	XX	–	Reserved
8C	SIZEL[5:0]	00	RW	{HSIZE[11], HSIZE[2:0], VSIZE[2:0]}
8D-BF	RSVD	XX	–	Reserved
C0	HSIZE8[7:0]	80	RW	Image Horizontal Size HSIZE[10:3]
C1	VSIZE8[7:0]	60	RW	Image Vertical Size VSIZE[10:3]
C2	CTRL0	0C	RW	Module Enable Bit[7]: AEC_EN Bit[6]: AEC_SEL Bit[5]: STAT_SEL Bit[4]: VFIRST Bit[3]: YUV422 Bit[2]: YUV_EN Bit[1]: RGB_EN Bit[0]: RAW_EN
C3	CTRL1	FF	RW	Module Enable Bit[7]: CIP Bit[6]: DMY Bit[5]: RAW_GMA Bit[4]: DG Bit[3]: AWB Bit[2]: AWB_GAIN Bit[1]: LENC Bit[0]: PRE
C4-D2	RSVD	XX	–	Reserved

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 3 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
D3	R_DVP_SP	82	RW	Bit[7]: Auto mode Bit[6:0]: DVP output speed control DVP PCLK = sysclk (48)/[6:0] (YUV0); = sysclk (48)/(2*[6:0]) (RAW)
D4-D9	RSVD	XX	–	Reserved
DA	IMAGE_MODE	00		Image Output Format Select Bit[7]: Reserved Bit[6]: Y8 enable for DVP Bit[5]: Reserved Bit[4]: JPEG output enable 0: Non-compressed 1: JPEG output Bit[3:2]: DVP output format 00: YUV422 01: RAW10 (DVP) 10: RGB565 11: Reserved Bit[1]: HREF timing select in DVP JPEG output mode 0: HREF is same as sensor 1: HREF = VSYNC Bit[0]: Byte swap enable for DVP 0: High byte first YUYV (C2[4]=0) YVYU (C2[4] = 1) 1: Low byte first UYVY (C2[4] =0) VYUY (C2[4] =1)
DB-DF	RSVD	XX	–	Reserved
E0	RESET	04	RW	Reset Bit[7]: Reserved Bit[6]: Microcontroller Bit[5]: SCCB Bit[4]: JPEG Bit[3]: Reserved Bit[2]: DVP Bit[1]: IPU Bit[0]: CIF
E1-EF	RSVD	XX	–	Reserved
F0	MS_SP	04	RW	SCCB Master Speed
F1-F6	RSVD	XX	–	Reserved
F7	SS_ID		RW	SCCB Slave ID

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 4 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
F8	SS_CTRL	01	RW	SCCB Slave Control Bit[7:6]: Reserved Bit[5]: Address auto-increase enable Bit[4]: Reserved Bit[3]: SCCB enable Bit[2]: Delay SCCB master clock Bit[1]: Enable SCCB master access Bit[0]: Enable sensor pass through access
F9	MC_BIST		RW	Bit[7]: Microcontroller Reset Bit[6]: Boot ROM select Bit[5]: R/W 1 error for 12K-byte memory Bit[4]: R/W 0 error for 12K-byte memory Bit[3]: R/W 1 error for 512-byte memory Bit[2]: R/W 0 error for 512-byte memory Bit[1]: BIST busy bit for read; One-shot reset of microcontroller for write Bit[0]: Launch BIST
FA	MC_AL		RW	Program Memory Pointer Address Low Byte
FB	MC_AH		RW	Program Memory Pointer Address High Byte
FC	MC_D	80	RW	Program Memory Pointer Access Address Boundary of register address to separate DSP and sensor register
FD	P_CMD	00	RW	SCCB Protocol Command Register
FE	P_STATUS	00	RW	SCCB Protocol Status Register
FF	RA_DLMT	7F	RW	Register Bank Select Bit[7:1]: Reserved Bit[0]: Register bank select 0: DSP address 1: Sensor address
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 1 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control LSBs Bit[7:0]: Gain setting • Range: 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) ***Note:*** *Set COM8[2] = 0 to disable AGC.*
01-02	RSVD	XX	–	Reserved
03	COM1	0F (UXGA) 0A (SVGA), 06 (CIF)	RW	Common Control 1 Bit[7:6]: Dummy frame control 00: Reserved 01: Allow 1 dummy frame 10: Allow 3 dummy frames 11: Allow 7 dummy frames Bit[5:4]: Reserved Bit[3:2]: Vertical window end line control 2 LSBs (8 MSBs in VEND[7:0] (0x1A)) Bit[1:0]: Vertical window start line control 2 LSBs (8 MSBs in VSTRT[7:0] (0x19))
04	REG04	20	RW	Register 04 Bit[7]: Horizontal mirror Bit[6]: Vertical flip Bit[4]: VREF bit[0] Bit[3]: HREF bit[0] Bit[2]: Reserved Bit[1:0]: AEC[1:0] (AEC[15:10] is in register REG45[5:0] (0x45), AEC[9:2] is in register AEC[7:0] (0x10))
05-07	RSVD	XX	–	Reserved
08	REG08	40	RW	Frame Exposure One-pin Control Pre-charge Row Number
09	COM2	00	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Standby mode enable 0: Normal mode 1: Standby mode Bit[3]: Reserved Bit[2]: Pin PWDN/RESETB used as SLVS/SLHS Bit[1:0]: Output drive select 00: 1x capability 01: 3x capability 10: 2x capability 11: 4x capability
0A	PIDH	26	R	Product ID Number MSB (Read only)
0B	PIDL	41	R	Product ID Number LSB (Read only)

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 2 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	COM3	38	RW	Common Control 3 Bit[7:3]: Reserved Bit[2]: Set banding manually 0: 60 Hz 1: 50 Hz Bit[1]: Auto set banding Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D	COM4	07	RW	Common Control 4 Bit[7:3]: Reserved Bit[2]: Clock output power-down pin status 0: Tri-state data output pin upon power-down 1: Data output pin hold at last state before power-down Bit[1:0]: Reserved
0E-0F	RSVD	XX	–	Reserved
10	AEC	33	RW	Automatic Exposure Control 8 bits for AEC[9:2] (AEC[15:10] is in register REG45[5:0] (0x45), AEC[1:0] is in register REG04[1:0] (0x04)) AEC[15:0]: Exposure time $T_{EX} = t_{LINE} \times AEC[15:0]$ ***Note:*** *The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period.*
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Internal frequency doublers ON/OFF selection 0: OFF 1: ON Bit[6]: Reserved Bit[5:0]: Clock divider CLK = XVCLK/(decimal value of CLKRC[5:0] + 1)

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 3 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COM7	00	RW	Common Control 7 Bit[7]: SRST 1: Initiates system reset. All registers are set to factory default values after which the chip resumes normal operation Bit[6:4]: Resolution selection 000: UXGA (full size) mode 001: CIF mode 100: SVGA mode Bit[3]: Reserved Bit[2]: Zoom mode Bit[1]: Color bar test pattern 0: OFF 1: ON Bit[0]: Reserved
13	COM8	C7	RW	Common Control 8 Bit[7:6]: Reserved Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure time to 1/120s Bit[4:3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: Reserved Bit[0]: Exposure control 0: Manual 1: Auto
14	COM9	50	RW	Common Control 9 Bit[7:5]: AGC gain ceiling, GH[2:0] 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 11x: 128x Bit[4:0]: Reserved

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 4 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COM10	00	RW	Common Control 10 (if Bypass DSP is selected) Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK edge selection 0: Data is updated at the falling edge of PCLK (user can latch data at the next rising edge of PCLK) 1: Data is updated at the rising edge of PCLK (user can latch data at the next falling edge of PCLK) Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
16	RSVD	XX	–	Reserved
17	HREFST	11	RW	Horizontal Window Start MSB 8 bits (3 LSBs in REG32[2:0] (0x32)) Bit[10:0]: Selects the start of the horizontal window, each LSB represents two pixels
18	HREFEND	75 (UXGA), 43 (SVGA, CIF)	RW	Horizontal Window End MSB 8 bits (3 LSBs in REG32[5:3] (0x32)) Bit[10:0]: Selects the end of the horizontal window, each LSB represents two pixels
19	VSTRT	01 (UXGA), 00 (SVGA, CIF)	RW	Vertical Window Line Start MSB 8 bits (2 LSBs in COM1[1:0] (0x03)) Bit[9:0]: Selects the start of the vertical window, each LSB represents two scan lines.
1A	VEND	97	RW	Vertical Window Line End MSB 8 bits (2 LSBs in COM1[3:2] (0x03)) Bit[9:0]: Selects the end of the vertical window, each LSB represents two scan lines.
1B	RSVD	XX	–	Reserved
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-23	RSVD	XX	–	Reserved

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 5 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC Operation AEC/AGC values will decrease in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC Operation AEC/AGC values will increase in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Threshold - effective only in AEC/AGC fast mode (COM8[7] = 1) Bit[7:4]: High threshold Bit[3:0]:Low threshold ***Note:*** *AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0].*
27-29	RSVD	XX	–	Reserved
2A	REG2A	00	RW	Register 2A Bit[7:4]: Line interval adjust value 4 MSBs (LSBs in FRARL[7:0] (0x2B)) Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits (LSBs in register HEDY[7:0] (0x31)) Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits (LSBs in register HSDY[7:0] (0x30))
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits (MSBs in REG2A[7:4] (0x2A)) The frame rate will be adjusted by changing the line interval. Each LSB will add 1/1922 T_{frame} in UXGA and 1/1190 T_{frame} in SVGA mode to te frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse Width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average (this register will auto update) Average Luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + (2 x GbAVG[7:0]) + RAVG[7:0]) x 0.25
30	HSDY	08	RW	HSYNC Position and Width, Start Point LSB 8 bits This register and REG2A[1:0] (0x2A) define HSYNC start position, each LSB will shift HSYNC start by 2 pixel period

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 6 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
31	HEDY	30	RW	HSYNC Position and Width, End Point LSB 8 bits This register and REG2A[3:2] (0x2A) define HSYNC end position, each LSB will shift HSYNC end by 2 pixel period
32	REG32	36 (UXGA), 09 (SVGA, CIF)	RW	Common Control 32 Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position 3 LSBs (8 MSBs in register HREFEND[7:0] (0x18)) Bit[2:0]: Horizontal window start position 3 LSBs (8 MSBs in register HREFST[7:0] (0x17))
33	RSVD	XX	–	Reserved
34	ARCOM2	20	RW	Bit[7:3]: Reserved Bit[2]: Zoom window horizontal start point Bit[1:0]: Reserved
35-44	RSVD	XX	–	Reserved
45	REG45	00	RW	Register 45 Bit[7:6]: AGC[9:8], AGC highest gain control Bit[5:0]: AEC[15:10], AEC MSBs
46	FLL	00	RW	Frame Length Adjustment LSBs Each bit will add 1 horizontal line timing in frame
47	FLH	00	RW	Frame Length Adjustment MSBs Each bit will add 256 horizontal lines timing in frame
48	COM19	00	RW	Common Control 19 Bit[7:2]: Reserved Bit[1:0]: Zoom mode vertical window start point 2 LSBs
49	ZOOMS	00	RW	Zoom Mode Vertical Window Start Point 8 MSBs
4A	RSVD	XX	–	Reserved
4B	COM22	20	RW	Common Control 22 Bit[7:0]: Flash light control
4C-4D	RSVD	XX	–	Reserved
4E	COM25	00	RW	Common Control 25 - reserved for banding Bit[7:6]: 50Hz Banding AEC 2 MSBs Bit[5:4]: 60HZ Banding AEC 2 MSBs Bit[3:0]: Reserved
4F	BD50	CA	RW	50Hz Banding AEC 8 LSBs
50	BD60	A8	RW	60Hz Banding AEC 8 LSBs
51-5C	RSVD	XX	–	Reserved

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 7 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
5D	REG5D	00	RW	Register 5D Bit[7:0]: AVGsel[7:0], 16-zone average weight option
5E	REG5E	00	RW	Register 5E Bit[7:0]: AVGsel[15:8], 16-zone average weight option
5F	REG5F	00	RW	Register 5F Bit[7:0]: AVGsel[23:16], 16-zone average weight option
60	REG60	00	RW	Register 60 Bit[7:0]: AVGsel[31:24], 16-zone average weight option
61	HISTO_LOW	80	RW	Histogram Algorithm Low Level
62	HISTO_HIGH	90	RW	Histogram Algorithm High Level
63-7E	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV2640 uses a 38-ball Chip Scale Package 2 (CSP2). Refer to Figure 11 for package information, Table 9 for package dimensions and Figure 12 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 21 OV2640 Package Specifications

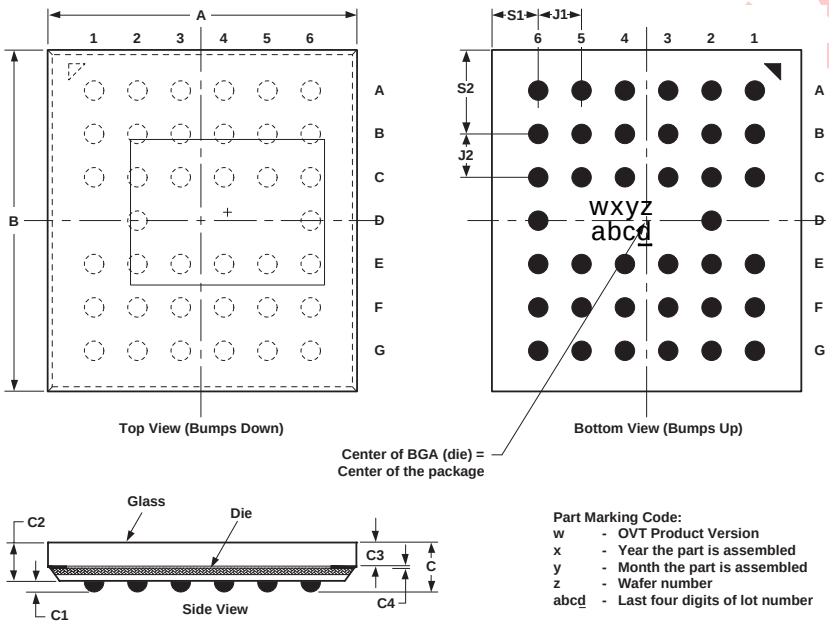
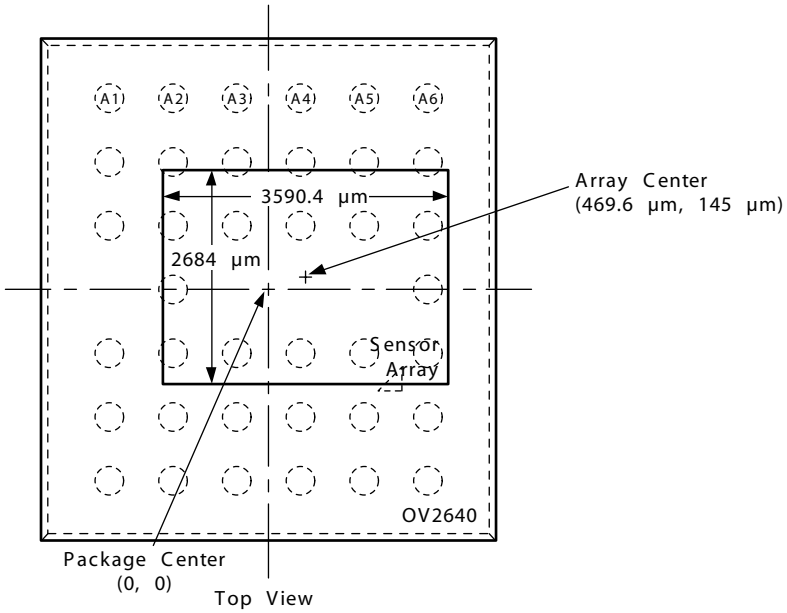


Table 14 OV2640 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package Body Dimension X	A	5700	5725	5750	µm
Package Body Dimension Y	B	6260	6285	6310	µm
Package Height	C	845	905	965	µm
Ball Height	C1	150	180	210	µm
Package Body Thickness	C2	680	725	770	µm
Cover Glass Thickness	C3	375	400	425	µm
Airgap Between Cover Glass and Sensor	C4	30	45	60	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		38 (1 NC)		
Pin Count X-axis	N1		6		
Pin Count Y-axis	N2		7		
Pins Pitch X-axis	J1		800		µm
Pins Pitch Y-axis	J2		800		µm
Edge-to-Pin Center Distance Analog X	S1	833	863	893	µm
Edge-to-Pin Center Distance Analog Y	S2	713	743	773	µm

Sensor Array Center

Figure 22 OV2640 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

IR Reflow Ramp Rate Requirements

OV2640 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 23 IR Reflow Ramp Rate Requirements

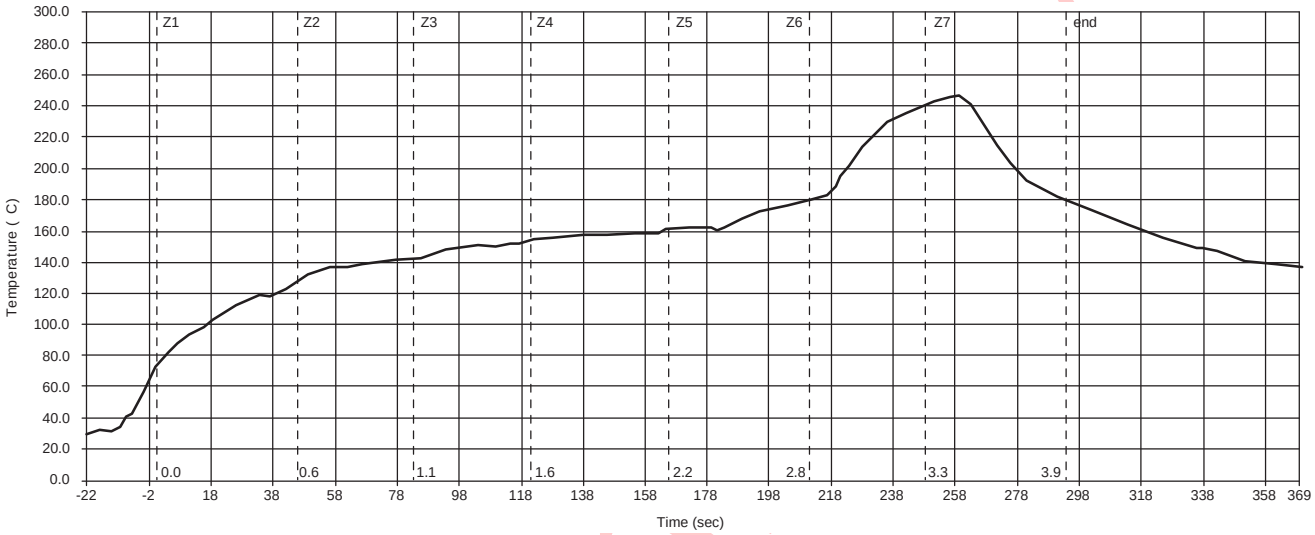


Table 15 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

Initial Release

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.01

DESCRIPTION OF CHANGES

The following changes were made to version 1.0:

- Under Key Specifications on page 1, changed specification for Core Power Supply from "1.2VDC ± 10%" to "1.2VDC ± 5%"
- Under Key Specifications on page 1, changed specification for Analog Power Supply from "2.8VDC ± 10%" to "2.5 ~ 3.0VDC"
- Under Key Specifications on page 1, changed specification for I/O Power Supply from "1.8V to 3.3V" to "1.7V to 3.3V"
- On pages 17 to 20, changed title of Table 12 from "Device Control Register (for 0x00 ~ 0xFF at 0xF8 = 00 and 0xFF = 00)" to "Device Control Register (when 0xFF = 00)"
- On pages 21 to 27, changed title of Table 13 from "Device Control Register (for 0x00 ~ 0x7E at 0xF8 = 01 and 0xFF = 7F)" to "Device Control Register (when 0xFF = 01)"
- In Table 12 on pages 18, changed description of register CTRL3 (0x87) from:

  Module Enable

Bit[7:6]:	Reserved
Bit[5]:	DCW
Bit[4]:	SDE
Bit[3]:	UV_ADJ
Bit[2]:	UV_AVG
Bit[1]:	Reserved
Bit[0]:	CMX

  to

  Module Enable

Bit[7]:	BPC
Bit[6]:	WPC
Bit[5:0]:	Reserved

- In Table 15 on page 30, changed specification for Peak Temperature from "Greater than 245°C" to "245°C"

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.01:

- Under Features on page 1, changed bulleted item from “Supports image sizes: UXGA, SVGA, and any size scaling down from SVGA to 40x30” to “Supports image sizes: UXGA, SXGA, SVGA, and any size scaling down from SXGA to 40x30”
- Under Key Specifications on page 1, deleted specifications for SVGA and CIF Array Size
- Under Key Specifications on page 1, changed Standby Power Requirements specification to “TBD”
- Under Key Specifications on page 1, changed specification for Chief Ray Angle from “TBD” to “25° non-linear”
- Under Key Specifications on page 1, changed specification for Well Capacity from “TBD” to “12 Ke”
- Under Electrical Characteristics on page 10, changed title of Table 6 from “DC Characteristics (-20°C < T_A < 70°C)” to “DC Characteristics (-30°C < T_A < 70°C)”
- In Table 6 on page 10, changed specification for Typ Standby Current from “10” to “TBD”
- In Table 6 on page 10, changed specification for Max Input voltage LOW (V_{IL}) from “0.8” to “0.54”
- In Table 6 on page 10, changed specification for Min Input voltage HIGH (V_{IH}) from “2” to “1.26”
- In Table 6 on page 10, changed subtitle “Digital Outputs (standard loading 25 pF, 1.2 KΩ to 2.8V)” to “Digital Outputs (standard loading 25 pF)”
- In Table 6 on page 10, changed specification for Min Output voltage HIGH (V_{OH}) from “2.2” to “1.62”
- In Table 6 on page 10, changed specification for Max Output voltage LOW (V_{OL}) from “0.6” to “0.18”
- In Table 6 on page 10, changed specification for Serial Interface Inputs Max SIO_C and SIO_D (V_{IL}) from “1” to “0.54”
- In Table 6 on page 10, changed specification for Serial Interface Inputs Min, Typ, and Max SIO_C and SIO_D (V_{IH}) from “2.5, 2.8, and VDD-IO + 0.5” to “1.26, 1.8, and 2.3”, respectively
- In Table 6 on page 10, changed table footnote b from “...$V_{DD\text{-}IO}$ = 2.8V” to “...$V_{DD\text{-}IO}$ = 1.8V”

DESCRIPTION OF CHANGES (CONTINUED)

- In Figure 21 on page 28, changed callout C3 to measure from thickness of glass and added callout C4 to measure airgap from glass to die.
- In Table 14 on page 28, changed C3 parameter name from “Thickness of Glass Surface to Wafer” to “Cover Glass Thickness”
- In Table 14 on page 28, changed C3 Minimum, Nominal, and Maximum specifications from “425, 445, and 465” to “375, 400, and 425”
- In Table 14 on page 28, added C4 parameter, Airgap Between Cover Glass and Sensor, and Minimum, Nominal, and Maximum specifications “30, 45, and 60”, respectively

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.2

DESCRIPTION OF CHANGES

The following changes were made to version 1.1:

- Under Key Specifications on page 1, changed Active Power Requirements specification to "TBD" to "125 mW (for 15 fps, UXGA YUV mode)" and "140 mW (for 15 fps, UXGA compressed mode)"
- Under Key Specifications on page 1, changed Standby Power Requirements specification to "TBD" to "600 µA"
- Under Key Specifications on page 1, deleted Preview (CIF) Power Requirements specification
- In Table 6 on page 10, changed specification for Typ Active (Operating) Current (I_{DDA-A}) from "TBD" to "30"
- In Table 6 on page 10, changed specification for Typ Active (Operating) Current (I_{DDA-D}) from "TBD" to "25 (YUV)" and "35 (Compressed)"
- In Table 6 on page 10, changed specification for Typ Active (Operating) Current (I_{DDA-IO}) from "TBD" to "6"
- IIn Table 6 on page 10, changed specification for Typ Standby Current from "10" to "600"
- In Table 6 on page 10, changed table footnote b from "...V_{DD-IO} = 1.8V" to "...V_{DD-IO} = 1.8V for 15 fps in UXGA mode"

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.21

DESCRIPTION OF CHANGES

The following changes were made to version 1.2:

- In Figure 1 on page 21, corrected the bottom view of the package by correcting the column numbers corresponding to the ball locations from (left to right) “1”, “2”, “3”, “4”, “5”, and “6” to (left to right) “6”, “5”, “4”, “3”, “2”, and “1”, respectively

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.3

DESCRIPTION OF CHANGES

The following changes were made to version 1.21:

- In Table 1 on page 8, made the following changes/corrections:
  - Corrected pin type of pin A1 from Power to Ground
  - Corrected pin type of pin A2 from I/O to Input and added “Note: There is no internal pull-up/pull-down resistor”
  - Corrected pin type of pin A3 from Power to Ground
  - Corrected pin type of pin A4 from Power to Ground
  - Corrected pin type of pin A5 from I/O to Reference
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin A6
  - Corrected pin type of pin B2 from Power to Input and added “Note: There is no internal pull-up/pull-down resistor”
  - Corrected pin type of pin B3 from Input to Power
  - Corrected pin type of pin B4 from I/O to Power
  - Corrected pin type of pin B5 from Input to Power
  - Corrected pin type of pin B6 from I/O to Input and “Note: There is an internal pull-down resistor”
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin C3
  - Added “Note: There is no internal pull-up/pull-down resistor” to description of pin C4
  - Added “Note: There is an internal pull-up resistor” to description of pin C6
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin D2
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E1
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E2
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E3
  - Corrected pin type of pin E4 from Power to Ground
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E5
  - Corrected pin type of pin E6 from Power to Ground

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 1 on page 8, made the following changes/corrections:
  - Corrected pin type of pin F2 from Analog to Power and changed description to “Sensor digital power (Core)”
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pins F3, F4, and F5
  - Corrected pin type of pin F6 from Analog to Power and changed description to be the same as pin F2
  - Corrected pin type of pin G2 from Power to Ground
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pins G3, G4, G5, and G6

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.4

DESCRIPTION OF CHANGES

The following changes were made to version 1.3:

- In Table 6 on page 11, made the following changes:
  - Added “40 mA” for Maximum specification of I_{DDA-A}
  - Added “35 mA (YUV)” and “50 mA (Compressed)” for Maximum specification of I_{DDA-D}
  - Added “10 mA” for Maximum specification of I_{DDA-IO}
  - Added “2 mA” for Maximum specification of $I_{DDS-SCCB}$
  - Added “1200 µA” for Maximum specification of $I_{DDS-PWDN}$

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.5

DESCRIPTION OF CHANGES

The following changes were made to version 1.4:

- Under Register Set section on page 18, changed the second paragraph from
  "There are two different sets for register address from 0x00 to 0x7E. Both register 0xF8 and register 0xFF control which set is accessible. When 0xF8=00 and 0xFF=00, Table 12 is effective. When 0xF8=01, 0xFF=7F, Table 13 is effective."
  to
  "There are two different sets of register banks. Register 0xFF controls which set is accessible. When register 0xFF=00, Table 12 is effective. When register 0xFF=01, Table 13 is effective."

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.6

DESCRIPTION OF CHANGES

The following changes were made to version 1.5:

- In Table 12 on page 18, changed name, default, R/W, and description of register 0x44 from “RSVD”, “XX”, “–”, and “Reserved” to “Qs”, “0C”, “RW”, and “Quantization Scale Factor”
- In Table 12 on page 21, changed description of register RA_DLMT (0xFF) from:

  Sensor/Device Register Address Delimiter
  <(value of register 0xFF): Sensor address
  (value of register 0xFF): DSP address

  to:

  Register Bank Select
  Bit[7:1]: Reserved
  Bit[0]: Register bank select
  0: DSP address
  1: Sensor address
- In Table 13 on page 22, changed default value for register REG08 (0x08) from “00” to “40”
- In Table 13 on page 22, changed description of register bits COM2[1:0] (0x09) from:

  00: Weakest
  01: Double capability
  10: Double capability
  11: Triple drive capability

  to:

  00: 1x capability
  01: 3x capability
  10: 2x capability
  11: 4x capability
- In Table 13 on page 22, changed default value for register PIDL (0x0B) from “40” to “41”
- In Table 13 on page 23, changed description of register bit CLKRC[6] (0x11) to “Reserved”
- In Table 13 on page 25, added “(if Bypass DSP is selected)” to description of register COM10 (0x15)

SPG30 Series

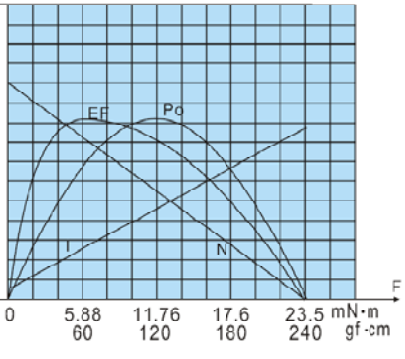
Cytron Technologies

Output Power: 1.1W **Weight: ~160g**

Typical applications: Labal printers、auto shutter、welding machines、water meter IC card、grill、oven、cleaning machine、garbage disposers、household appliances、slot machines、money detector、automatic actuator、coffee machine、towel disposal、lighting、coin refund devices、peristaltic pump.

MOTOR CHARACTERISTICS

Po	EF	I	N
6	60	3.0	7500
4	40	2.0	5000
2	20	1.0	2500
W	%	A	r/min

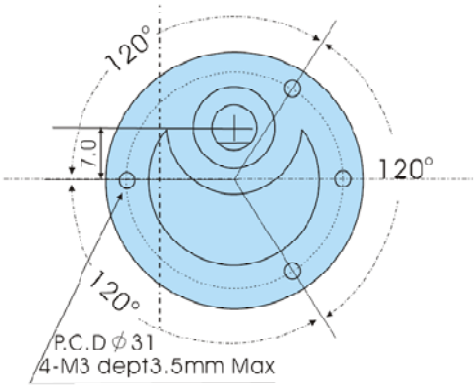


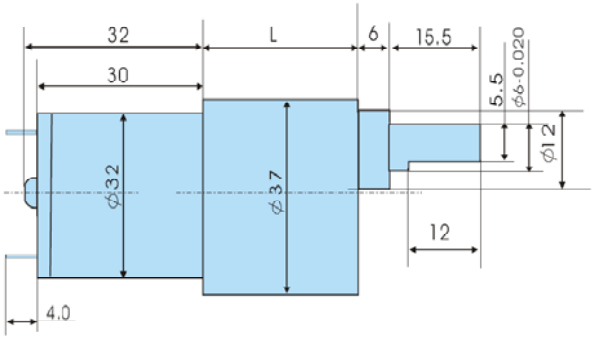
I:current N:speed
Po:output power F:Torque
EF:efficiency

MOTOR TORQUE/SPEED/CURRENT

Rated voltage	12VDC
No load speed	7000r/min
No load current	70mA
Rated torque	60gf・cm 5.88mN・m
Rated current	410mA
Rated speed	5200r/min
Stall torque	240gf・cm 23.5mN・m
Stall current	1.8A

APPEARANCE SIZE





Order Option							
Order Code	Input Voltage	Rated		Weight (g)	Power (w)	Diameter (mm)	L (mm)
		Speed (RPM)	Torque (mN.m)				
SPG10-30K	6	440	29.4	10	-	12	24
SPG10-150K	6	85	107.9	10	-	12	24
SPG10-298K	6	45	176.5	10	-	12	24
SPG20-50K	12	130	58.8	60	0.6	27.2	-
SPG30-20K	12	185	78.4	160	1.1	37	22
SPG30-30K	12	103	127.4	160	1.1	37	22
SPG30-60K	12	58	254.8	160	1.1	37	25
SPG30-150K	12	26	588	160	1.1	37	27
SPG30-200K	12	17	784	160	1.1	37	27
SPG30-300K	12	12	1176	160	1.1	37	27
SPG50-20K	12	170	196	300	3.4	37	23
SPG50-60K	12	56	588	300	3.4	37	26
SPG50-100K	12	34	980	300	3.4	37	26
SPG50-180K	12	17	1960	300	3.4	37	28

DC Geared Motor with Encoder
MO-SPG-30E-XXXK

USER'S MANUAL

V1.1

May 2011

Index

1. Introduction and Overview

Figure 1.0 DC geared motor with encoder and its removable cover

This document explains the general method to use the encoder for MO-SPG-30E-XXXK. "XXX" is referring to the gear ratio of Cytron's SPG-30 Geared Motor series which is either 20, 30, 60, 150, 200 or 300. This DC Geared Motor with Encoder is formed by a quadrature hall effect encoder board which is designed to fit on the rear shaft of Cytron's SPG-30 Geared Motor series. Two hall effect sensor are placed 90 degree apart to sense and produce two output A and B which is 90 degree out of phase and allowing the direction of rotation to be determined. This encoder provides 3 counts per revolution of the rear shaft. Please note that the encoder is mounted at the rear shaft, the minimum resolution is depends on the motor's gear ratio.

Features of Quadrature Hall Effect Encoder:

- Operating voltage : 4.5 V to 5.5 V
- Two digital outputs (Quadrature waveform)
- Small in size and light in weight
- Resolution : 3 pulses per rear shaft revolution, single channel output.
    - 60 counts per main shaft revolution for 1:20 geared motor

- 90 counts per main shaft revolution for 1:30 geared motor
- 180 counts per main shaft revolution for 1:60 geared motor
- 450 count per main shaft revolution for 1:150 geared motor
- 600 count per main shaft revolution for 1:200 geared motor
- 900 count per main shaft revolution for 1:300 geared motor

1.1. State Diagrams and Waveform

State Diagram

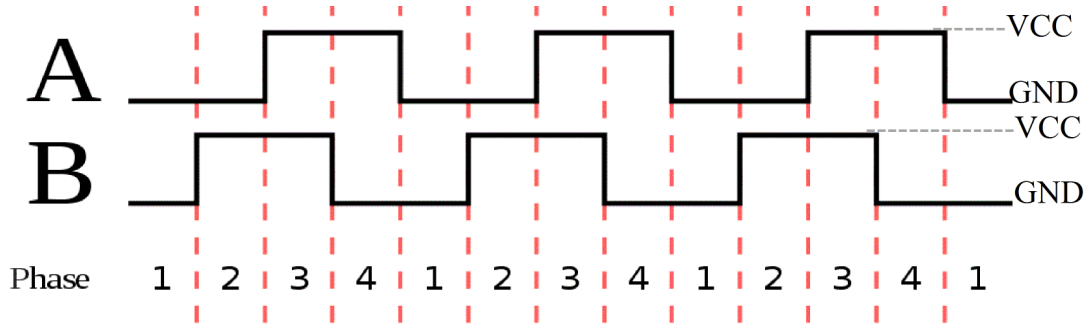
Clockwise Rotation

Phase	A	B
1	0	0
2	0	1
3	1	1
4	1	0

Counter Clockwise Rotation

Phase	A	B
1	1	0
2	1	1
3	0	1
4	0	0

Square quadrature waveform for Channel A and B (Clockwise)



2. Pin Descriptions

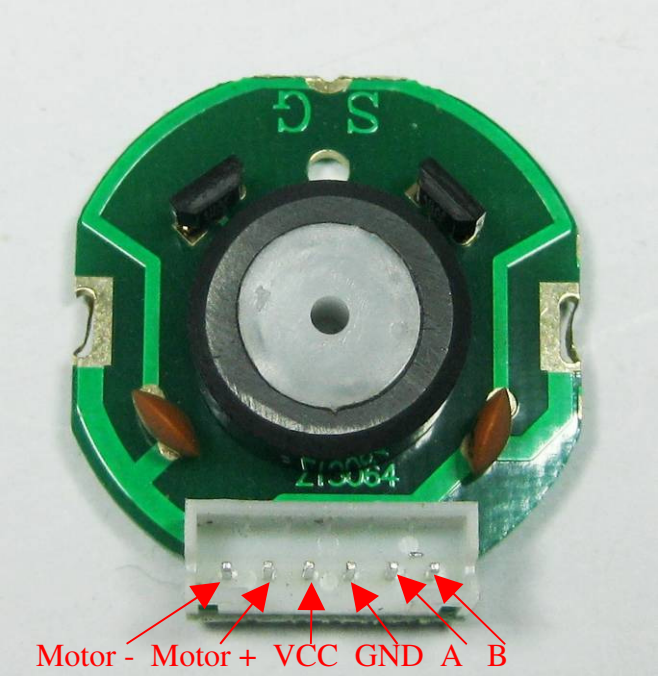


Figure 2.0 2020-06 connector pin descriptions

Pin	Name	Description
1	Motor -	Output of motor driver
2	Motor +	Output of motor driver
3	Hall effect sensor VCC	Supply voltage for sensor circuit (4.5V-5.5V)
4	Hall effect sensor GND	Ground
5	Channel A	Output of the encoder
6	Channel B	Output of the encoder

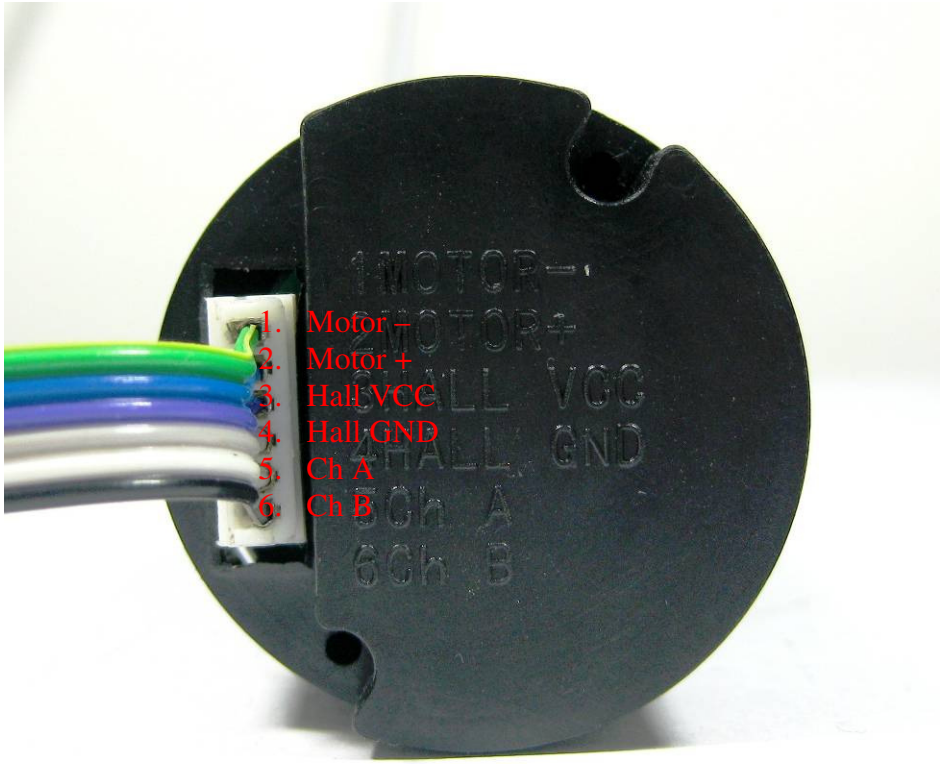


Figure 2.1 Rear view of the motor with encoder and cover

3. Sample Schematic

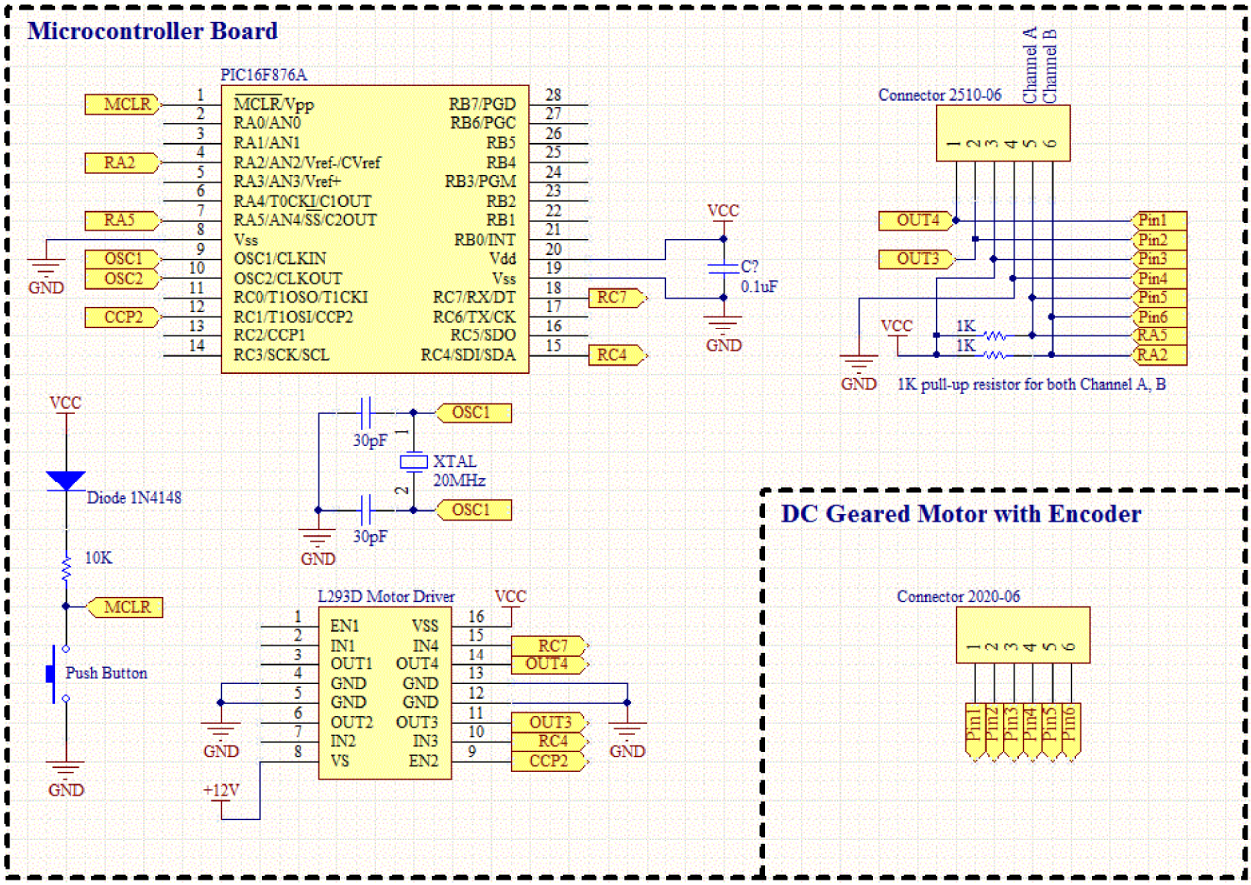


Figure 3.0 Sample schematic diagram with respect to sample source code**

**Schematic above is an example with respect to the sample source code provided. RC4, RC7, RA2, and RA5 can be replaced by any other digital I/O pins. Besides, for PWM control, user can also use CCP1 instead of CCP2. For Channel A and channel B, this sample (schematic and source code) shows continuous monitoring of quadrature signals which can be done by any digital I/O pin. Users are encouraged to modify the schematic and source code to allow use of external interrupt to count the rising or falling edge of either channel to reduce the processing power used by monitoring both channel A and B.

4. Warranty

- Product warranty is valid for 6 months
- Warranty only applies to manufacturing defect.
- Damage caused by misuse is not covered under warranty.
- Warranty does not cover freight cost for both ways.

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DRV88703.6-A Brushed DC Motor Driver (PWM Control)

1 Features

- H-Bridge Motor Driver
  - Drives One DC Motor, One Winding of a Stepper Motor, or Other Loads
- Wide 6.5-V to 45-V Operating Voltage
- 565-mΩ Typical $R_{DS(on)}$ (HS + LS)
- 3.6-A Peak Current Drive
- PWM Control Interface
- Integrated Current Regulation
- Low-Power Sleep Mode
- Small Package and Footprint
  - 8-Pin HSOP With PowerPAD™
  - 4.9 × 6.0 mm
- **Integrated Protection Features**
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Automatic Fault Recovery

2 Applications

- Printers
- Appliances
- Industrial Equipment
- Other Mechatronic Applications

3 Description

The DRV8870 device is a brushed-DC motor driver for printers, appliances, industrial equipment, and other small machines. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that can control motors bidirectionally with up to 3.6-A peak current. The inputs can be pulse-width modulated (PWM) to control motor speed, using a choice of current-decay modes. Setting both inputs low enters a low-power sleep mode.

The DRV8870 device features integrated current regulation, based on the analog input VREF and the voltage on the ISEN pin, which is proportional to motor current through an external sense resistor. The ability to limit current to a known level can significantly reduce the system power requirements and bulk capacitance needed to maintain stable voltage, especially for motor startup and stall conditions.

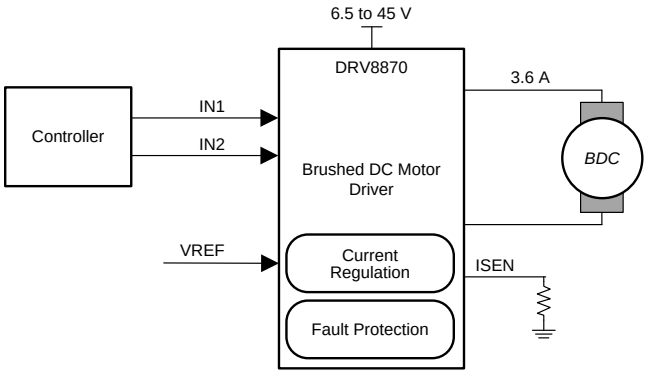
The device is fully protected from faults and short circuits, including undervoltage (UVLO), overcurrent (OCP), and overtemperature (TSD). When the fault condition is removed, the device automatically resumes normal operation.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8870	HSOP (8)	4.90 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



H-Bridge States

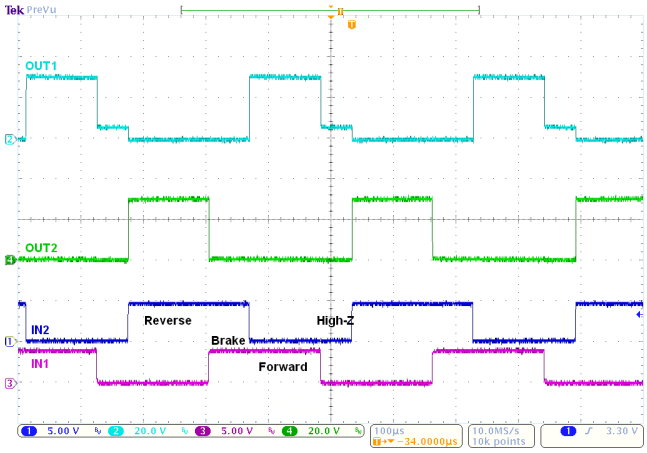


Table of Contents

4 Revision History

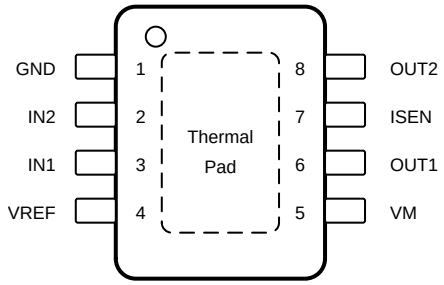
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2016) to Revision B	Page
• Deleted the power supply voltage ramp rate (VM) parameter from the *Absolute Maximum Ratings* table	3
• Added the output current parameter to the *Absolute Maximum Ratings* table	3
• Added the *Receiving Notification of Documentation Updates* section	17

Changes from Original (August 2015) to Revision A	Page
• Updated the f_{PWM} max value and added a note	4
• Removed the redundant T_A condition and added f_{PWM} = 24 kHz	5
• Added more information to clarify how the max RMS current varies for different applications	12

5 Pin Configuration and Functions

DDA Package
8-Pin HSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1	PWR	Logic ground. Connect to board ground
IN1	3	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns. See Table 1.
IN2	2	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns. See Table 1.
ISEN	7	PWR	High-current ground path. If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground.
OUT1	6	O	H-bridge output. Connect directly to the motor or other inductive load.
OUT2	8	O	H-bridge output. Connect directly to the motor or other inductive load.
VM	5	PWR	6.5-V to 45-V power supply. Connect a 0.1-µF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
VREF	4	I	Analog input. Apply a voltage between 0.3 to 5 V. For information on current regulation, see the *Current Regulation* section.
PAD		—	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Logic input voltage (IN1, IN2)	–0.3	7	V
Reference input pin voltage (VREF)	–0.3	6	V
Continuous phase node pin voltage (OUT1, OUT2)	–0.7	VM + 0.7	V
Current sense input pin voltage (ISEN)[(2)]	–0.5	1	V
Output current (100% duty cycle)	0	3.5	A
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VM	Power supply voltage	6.5		45	V
VREF	VREF input voltage	0.3 (1)		5	V
V_I	Logic input voltage (IN1, IN2)	0		5.5	V
f_{PWM}	Logic input PWM frequency (IN1, IN2)	0		200 (2)	kHz
I_{peak}	Peak output current (3)	0		3.6	A
T_A	Operating ambient temperature (3)	–40		125	°C

(1) Operational at VREF = 0 to 0.3 V, but accuracy is degraded
(2) The voltages applied to the inputs should have at least 800 ns of pulse width to ensure detection. Typical devices require at least 400 ns. If the PWM frequency is 200 kHz, the usable duty cycle range is 16% to 84%.
(3) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV8870 DDA (HSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM	VM operating voltage		6.5		45	V
I_{VM}	VM operating supply current	VM = 12 V		3	10	mA
$I_{VMSLEEP}$	VM sleep current	VM = 12 V			10	µA
t_{ON} (1)	Turn-on time	VM > V_{UVLO} with IN1 or IN2 high		40	50	µs
LOGIC-LEVEL INPUTS (IN1, IN2)						
V_{IL}	Input logic low voltage				0.5	V
V_{IH}	Input logic high voltage		1.5			V
V_{HYS}	Input logic hysteresis			0.5		V
I_{IL}	Input logic low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic high current	V_{IN} = 3.3 V		33	100	µA
R_{PD}	Pulldown resistance	to GND		100		kΩ
t_{PD}	Propagation delay	INx to OUTx change (see Figure 6)		0.7	1	µs
t_{sleep}	Time to sleep	Inputs low to sleep		1	1.5	ms
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		307	360	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		258	320	mΩ
t_{DEAD}	Output dead time			220		ns
V_d	Body diode forward voltage	I_{OUT} = 1 A		0.8	1	V
CURRENT REGULATION						
A_V	ISEN gain	VREF = 2.5 V	9.4	10	10.4	V/V
t_{OFF}	PWM off-time			25		µs
t_{BLANK}	PWM blanking time			2		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falls until UVLO triggers		6.1	6.4	V
		VM rises until operation recovers		6.3	6.5	
$V_{UV,HYS}$	VM undervoltage hysteresis	Rising to falling threshold	100	180		mV
I_{OCP}	Overcurrent protection trip level		3.7	4.5	6.4	A
t_{OCP}	Overcurrent deglitch time			1.5		µs
t_{RETRY}	Overcurrent retry time			3		ms
T_{SD}	Thermal shutdown temperature		150	175		°C
T_{HYS}	Thermal shutdown hysteresis			40		°C

(1) t_{ON} applies when the device initially powers up, and when it exits sleep mode.

6.6 Typical Characteristics

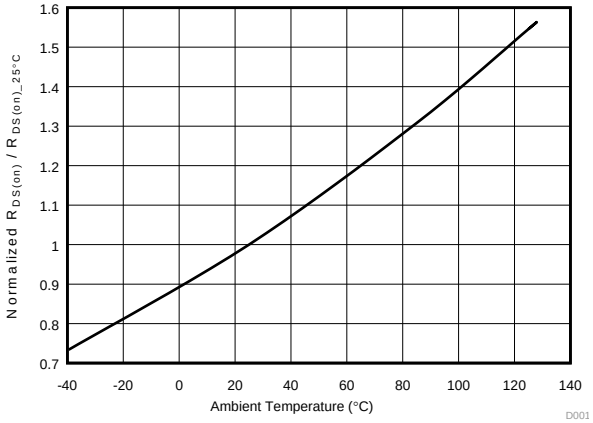


Figure 1. $R_{DS(on)}$ vs Temperature

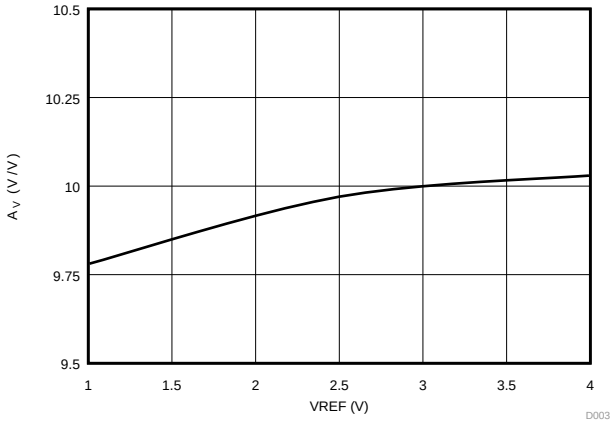


Figure 2. A_V vs VREF

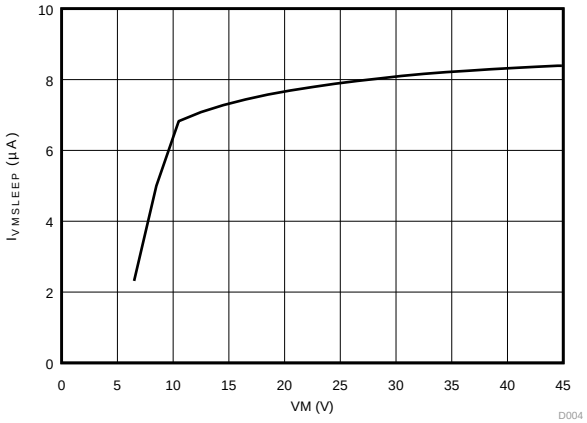


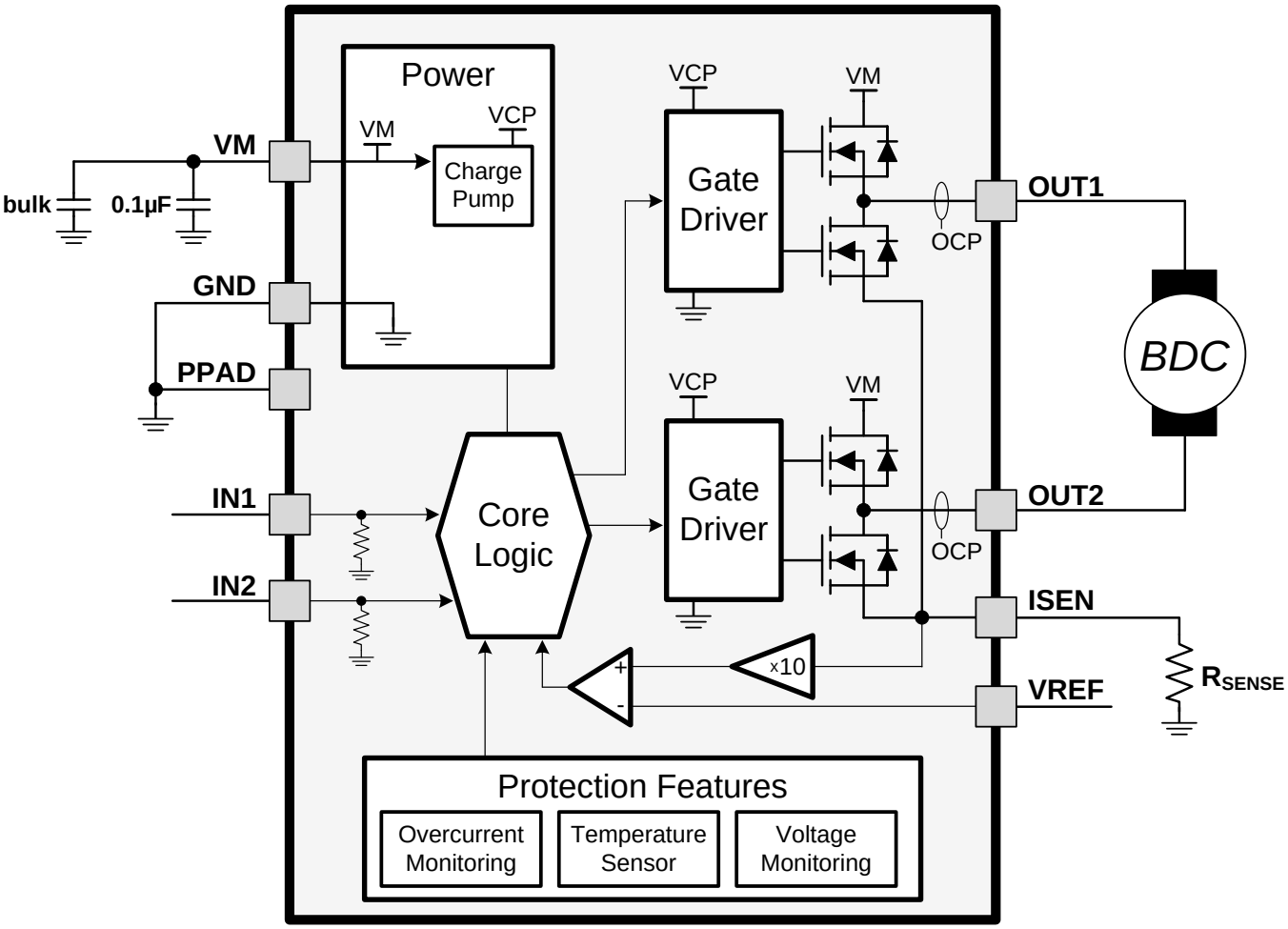
Figure 3. $I_{VMSLEEP}$ vs VM at 25°C

7 Detailed Description

7.1 Overview

The DRV8870 device is an optimized 8-pin device for driving brushed DC motors with 6.5 to 45 V and up to 3.6-A peak current. The integrated current regulation restricts motor current to a predefined maximum. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{ds(on)}$ of 565 mΩ (including one high-side and one low-side FET). A single-power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation, at frequencies between 0 to 100 kHz. The device has an integrated sleep mode that is entered by bringing both inputs low. An assortment of protection features prevent the device from being damaged if a system fault occurs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bridge Control

The DRV8870 output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 1.

Table 1. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available. The input pins can be powered before VM is applied.

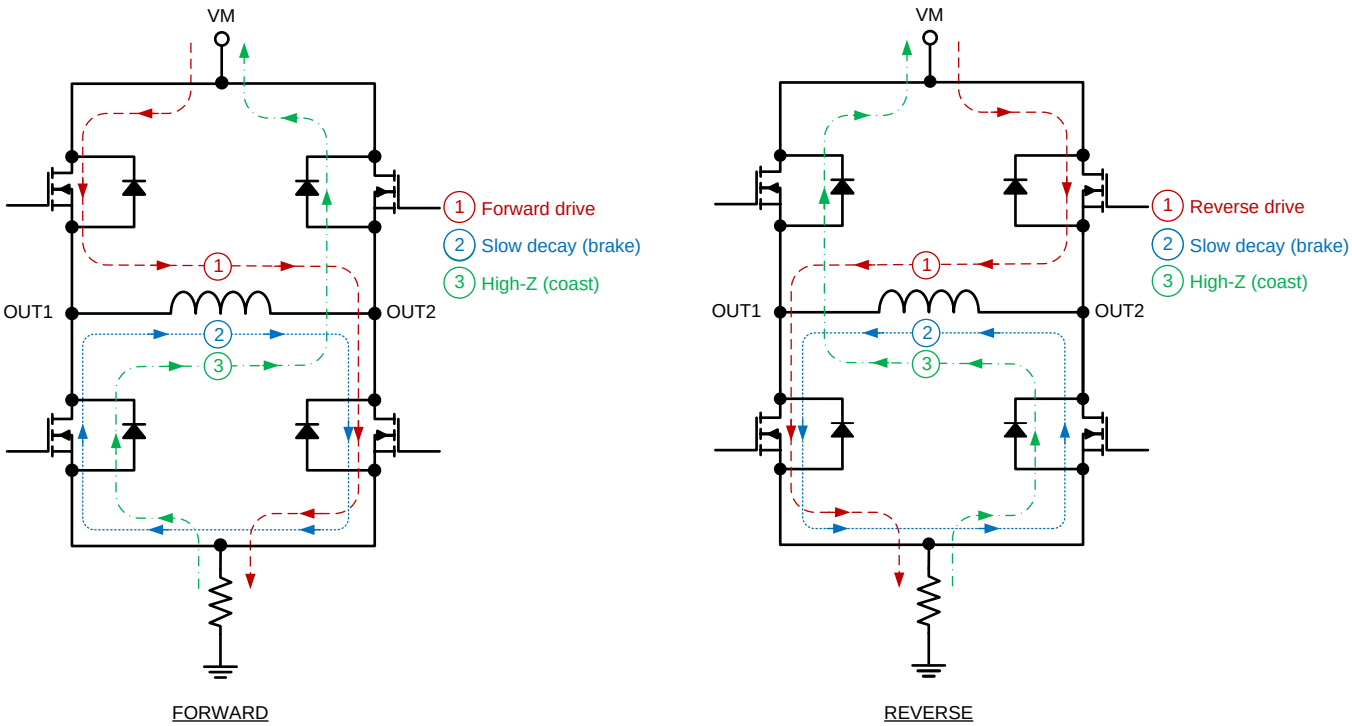


Figure 4. H-Bridge Current Paths

7.3.2 Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP} (typically 1 ms), the DRV8870 device enters a low-power sleep mode, where the outputs remain High-Z and the device uses $I_{VMSLEEP}$ (µA) of current. If the device is powered up while both inputs are low, it immediately enters sleep mode. After the IN1 or IN2 pins are high for at least 5 µs, the device is operational 50 µs (t_{ON}) later.

7.3.3 Current Regulation

The DRV8870 device limits the output current based on the analog input, VREF, and the resistance of an external sense resistor on the ISEN pin according to Equation 1:

$$I_{TRIP}\ (A) = \frac{VREF\ (V)}{A_V \times R_{ISEN}\ (\Omega)} = \frac{VREF\ (V)}{10 \times R_{ISEN}\ (\Omega)} \quad (1)$$

For example, if VREF = 3.3 V and a R_{ISEN} = 0.15 Ω, the DRV8870 device limits motor current to 2.2 A no matter how much load torque is applied. For guidelines on selecting a sense resistor, see the *Sense Resistor* section.

When I_{TRIP} is reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for a time of t_{OFF} (typically 25 µs).

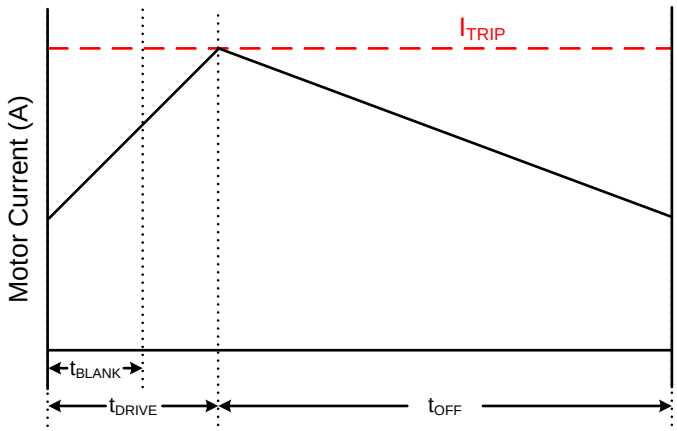


Figure 5. Current-Regulation Time Periods

After t_{OFF} elapses, the output is re-enabled according to the two inputs, INx. The drive time (t_{DRIVE}) until reaching another I_{TRIP} event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

7.3.4 Dead Time

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

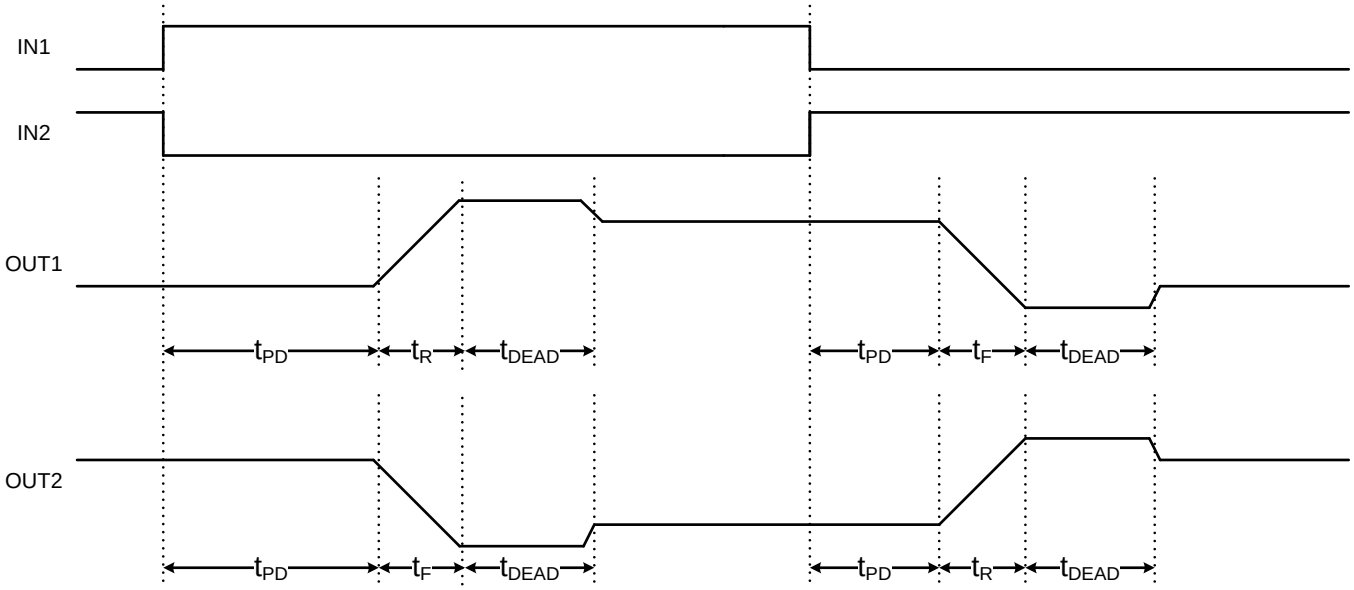


Figure 6. Propagation Delay Time

7.3.5 Protection Circuits

The DRV8870 device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

7.3.5.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage-lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VM rises above the UVLO threshold.

7.3.5.2 Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold, I_{OCP}, for longer than t_{OCP}, all FETs in the H-bridge are disabled for a duration of t_{RETRY}. After that, the H-bridge is re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

7.3.5.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

Table 2. Protection Functionality

FAULT	CONDITION	H-BRIDGE BECOMES	RECOVERY
VM undervoltage lockout (UVLO)	$VM < V_{UVLO}$	Disabled	$VM > V_{UVLO}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	t_{RETRY}
Thermal Shutdown (TSD)	$T_J > 150°C$	Disabled	$T_J < T_{SD} – T_{HYS}$

7.4 Device Functional Modes

The DRV8870 device can be used in multiple ways to drive a brushed DC motor.

7.4.1 PWM With Current Regulation

This scheme uses all of the capabilities of the device. The I_{TRIP} current is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake or slow decay is typically used during the off-time.

7.4.2 PWM Without Current Regulation

If current regulation is not required, the ISEN pin should be directly connected to the PCB ground plane. The VREF voltage must still be 0.3 to 5 V, and larger voltages provide greater noise margin. This mode provides the highest-possible peak current which is up to 3.6 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.6 A, the device might reach overcurrent protection (OCP) or overtemperature shutdown (TSD). If that happens, the device disables and protects itself for about 3 ms (t_{RETRY}) and then resumes normal operation.

7.4.3 Static Inputs With Current Regulation

The IN1 and IN2 pins can be set high and low for 100% duty cycle drive, and I_{TRIP} can be used to control the current of the motor, speed, and torque capability.

7.4.4 VM Control

In some systems, varying VM as a means of changing motor speed is desirable. See the *Motor Voltage* section for more information.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8870 device is typically used to drive one brushed DC motor.

8.2 Typical Application

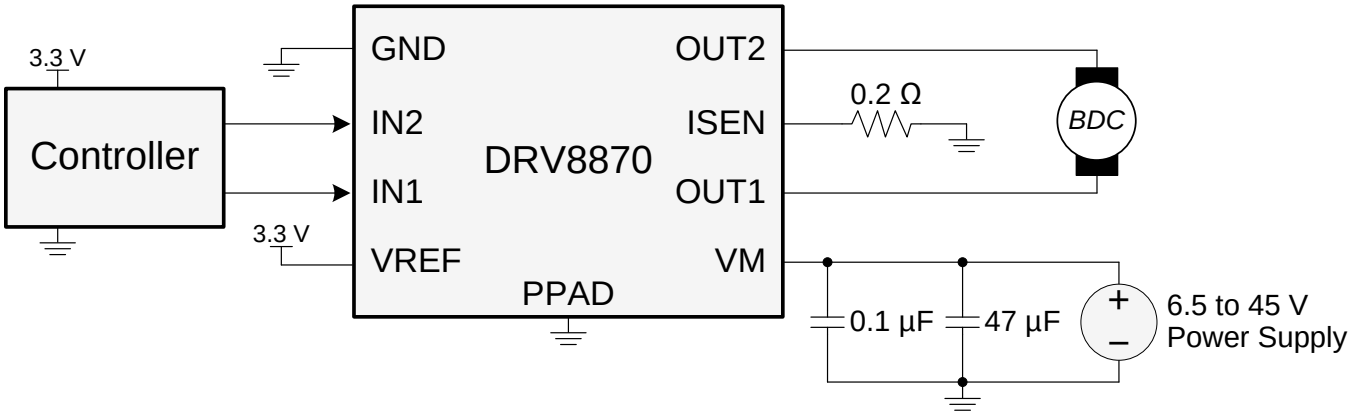


Figure 7. Typical Connections

8.2.1 Design Requirements

Table 3 lists the design parameters.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_M	24 V
Motor RMS current	I_{RMS}	0.8 A
Motor startup current	I_{START}	2 A
Motor current trip point	I_{TRIP}	2.2 A
VREF voltage	VREF	3.3 V
Sense resistance	R_{ISEN}	0.15 Ω
PWM frequency	f_{PWM}	5 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Drive Current

The current path is through the high-side sourcing DMOS power driver, motor winding, and low-side sinking DMOS power driver. Power dissipation losses in one source and sink DMOS power driver are shown in Equation 2.

$$P_D = I^2 \left(R_{DS(on)Source} + R_{DS(on)Sink}\right) \quad (2)$$

The DRV8870 device has been measured to be capable of 2-A RMS current at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on the PCB design, ambient temperature, and PWM frequency. Typically, switching the inputs at 200 kHz compared to 20 kHz causes 20% more power loss in heat.

8.2.2.3 Sense Resistor

For optimal performance, the sense resistor must have the following characteristics:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 1.5 A, and a 0.2-Ω sense resistor is used, the resistor dissipates 1.5 A^2 × 0.2 Ω = 0.45 W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, the system designer should add margin. Measuring the actual sense resistor temperature in a final system is always best.

Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel, between the sense node and ground, is common and distributes the current and heat dissipation.

8.2.3 Application Curves

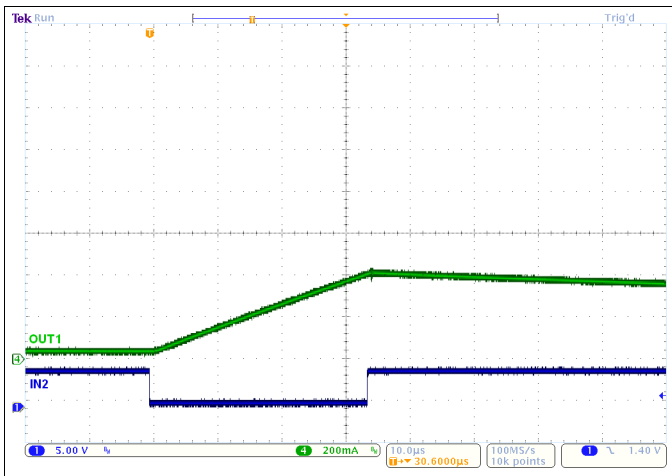


Figure 8. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 12 V

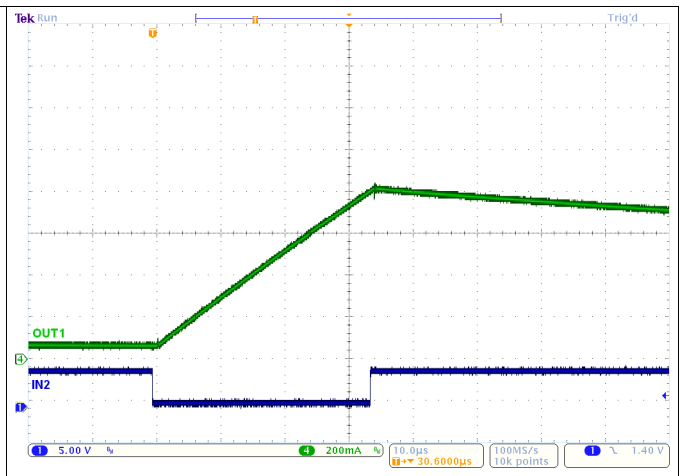


Figure 9. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 24 V

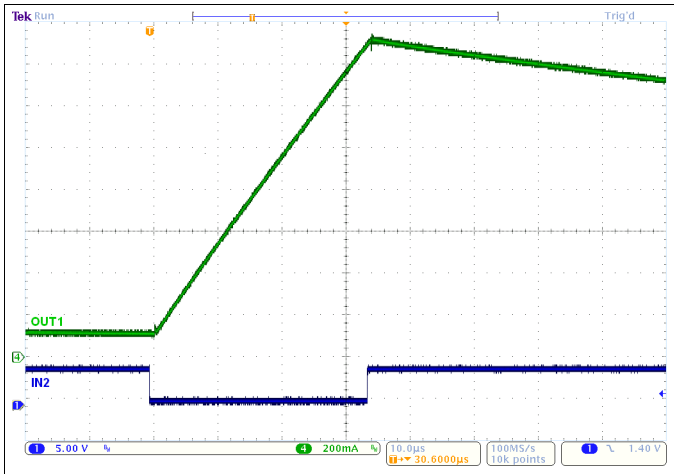


Figure 10. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 45 V

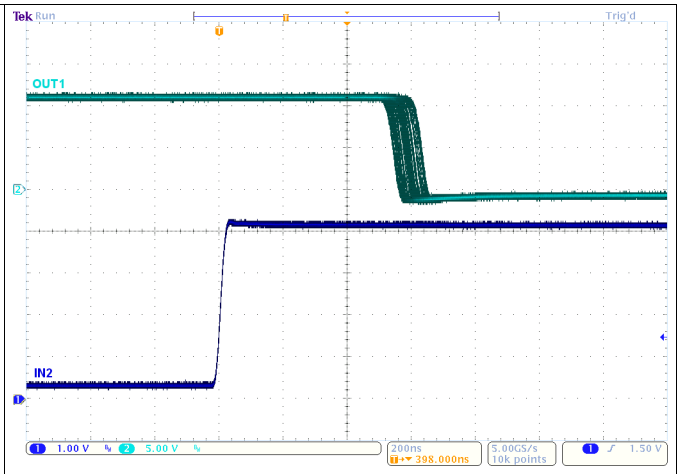


Figure 11. t_{PD}

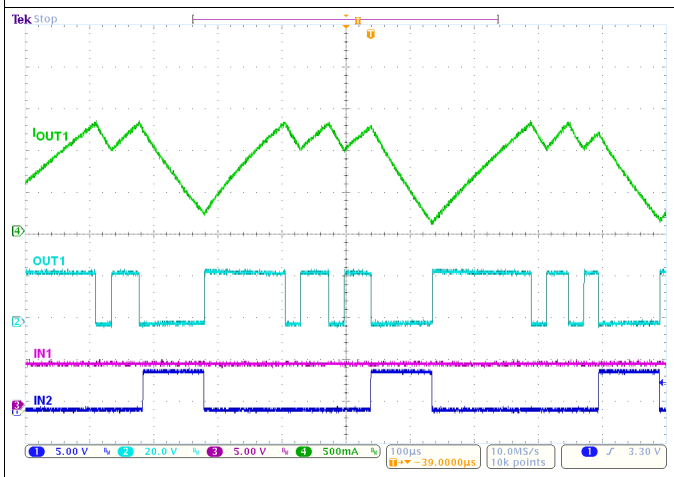


Figure 12. Current Regulation With VREF = 2 V and 150 mΩ

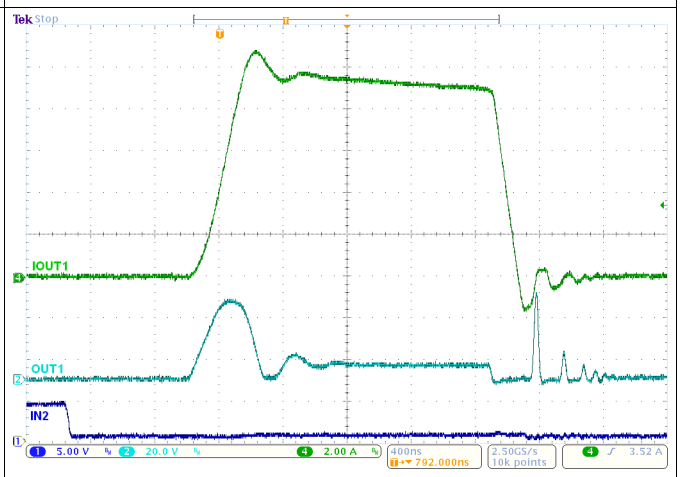


Figure 13. OCP With 45 V and the Outputs Shorted Together

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

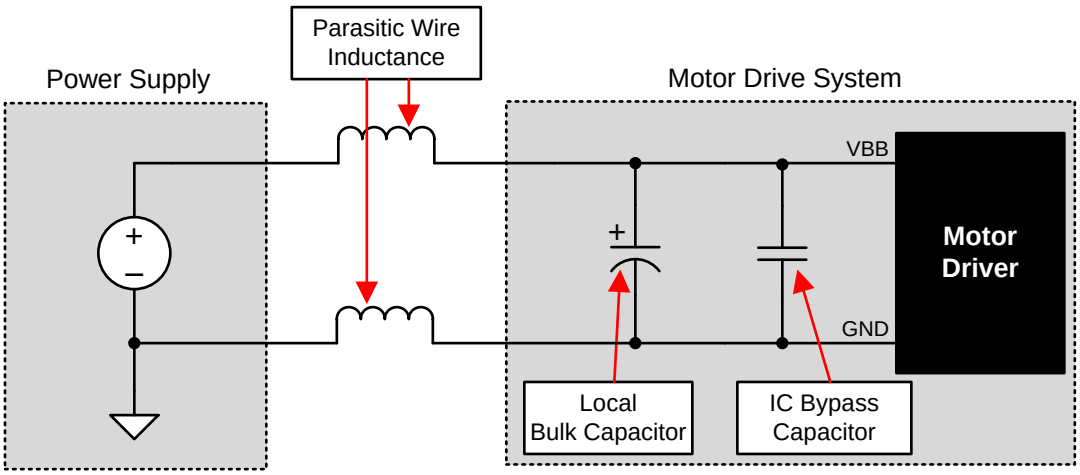


Figure 14. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

Figure 15 shows the recommended layout and component placement.

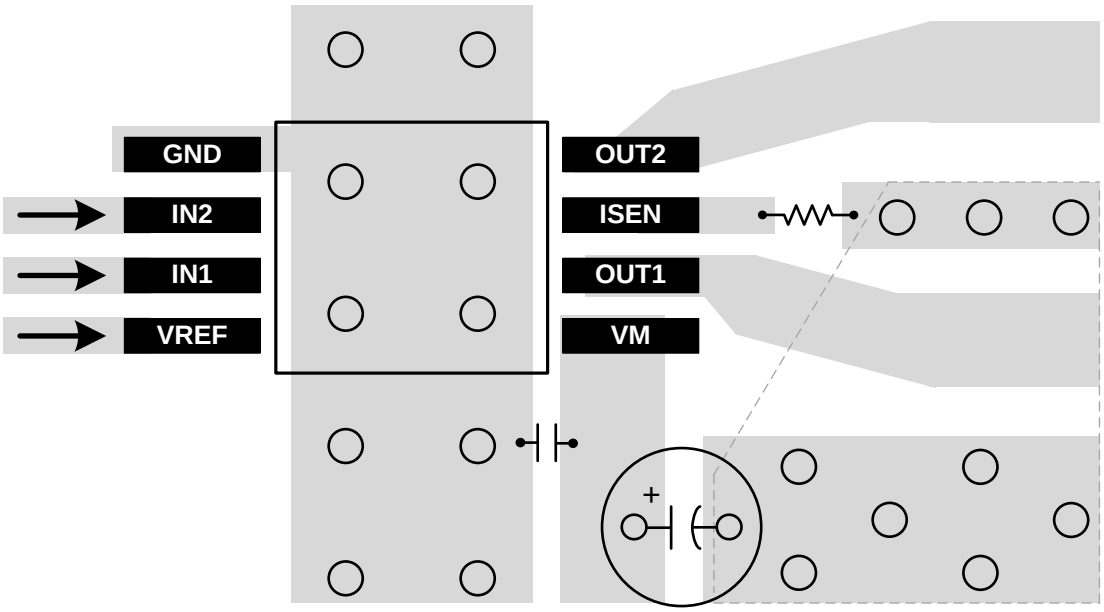


Figure 15. Layout Recommendation

10.3 Thermal Considerations

The DRV8870 device has thermal shutdown (TSD) as described in the *Thermal Shutdown (TSD)* section. If the die temperature exceeds approximately 175°C, the device is disabled until the temperature drops below the temperature hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8870 device is dominated by the power dissipated in the output FET resistance, $R_{DS(on)}$. Use the equation in the *Drive Current* section to calculate the estimated average power dissipation when driving a load.

Note that at startup, the current is much higher than normal running current; this peak current and its duration must be also be considered.

Power Dissipation (continued)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

$R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

The power dissipation of the DRV8870 device is a function of RMS motor current and the FET resistance ($R_{DS(ON)}$) of each output.

$$\text{Power} \approx I_{RMS}^2 \times \left(\text{High-side } R_{DS(ON)} + \text{ Low-side } R_{DS(ON)}\right) \tag{3}$$

For this example, the ambient temperature is 58°C, and the junction temperature reaches 80°C. At 58°C, the sum of $R_{DS(ON)}$ is about 0.72 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat is 0.8 A^2 × 0.72 Ω = 0.46 W.

The temperature that the DRV8870 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, in order dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8870 device had an effective thermal resistance $R_{\theta JA}$ of 48°C/W, and:

$$T_J = T_A + (P_D \times R_{\theta JA}) = 58°C + (0.46\ W \times 48°C/W) = 80°C \tag{4}$$

10.4.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to *PowerPAD™ Thermally Enhanced Package* and *PowerPAD Made Easy™*, available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Calculating Motor Driver Power Dissipation*
- *Current Recirculation and Decay Modes*
- *PowerPAD™ Made Easy*
- *PowerPAD™ Thermally Enhanced Package*
- *Understanding Motor Driver Current Ratings*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8870DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	8870	Samples
DRV8870DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	8870	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

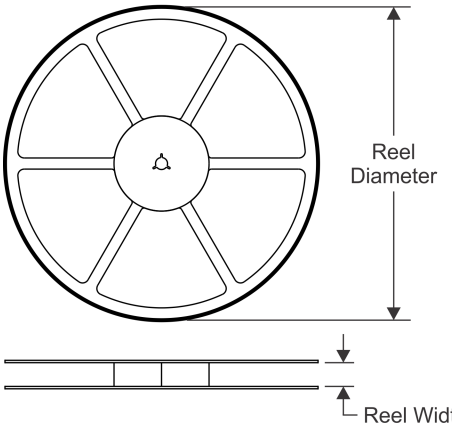
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

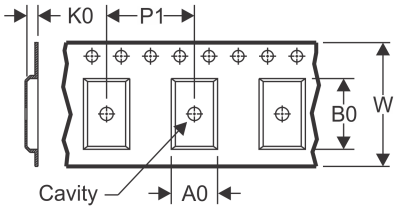
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

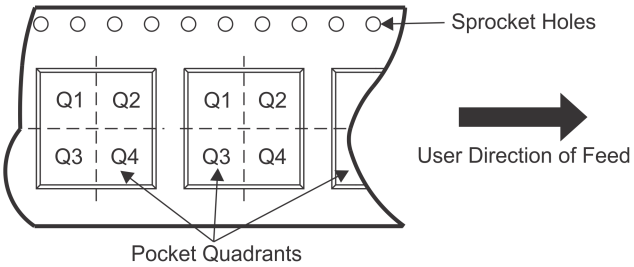


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

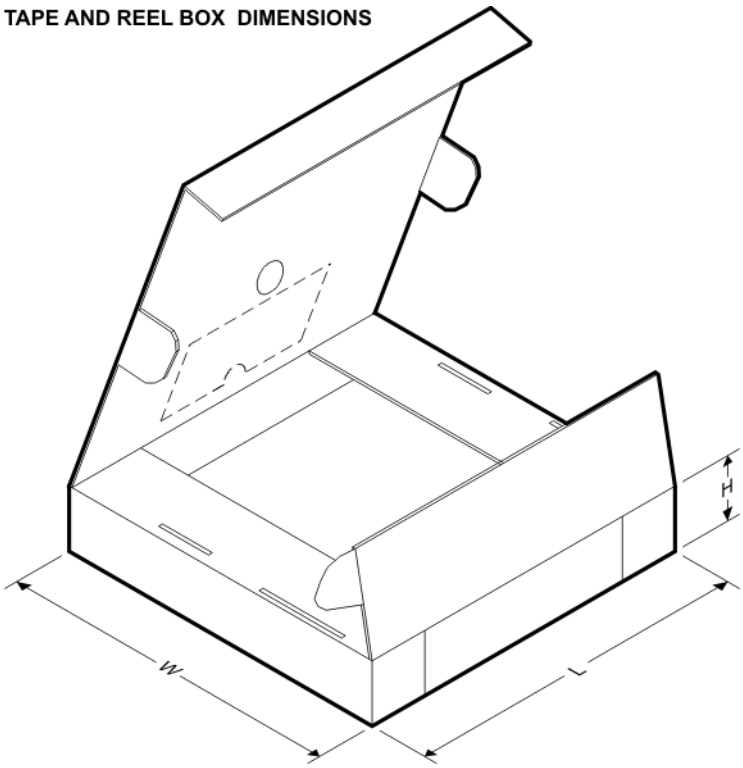
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8870DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

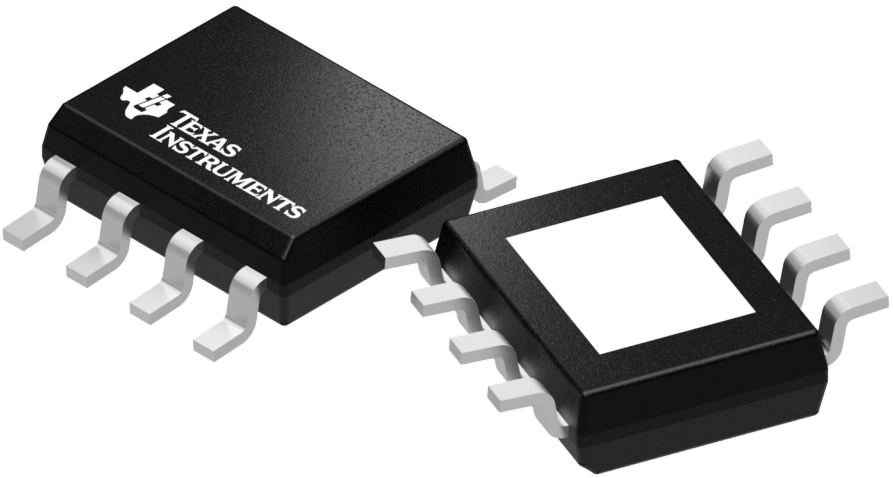


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8870DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

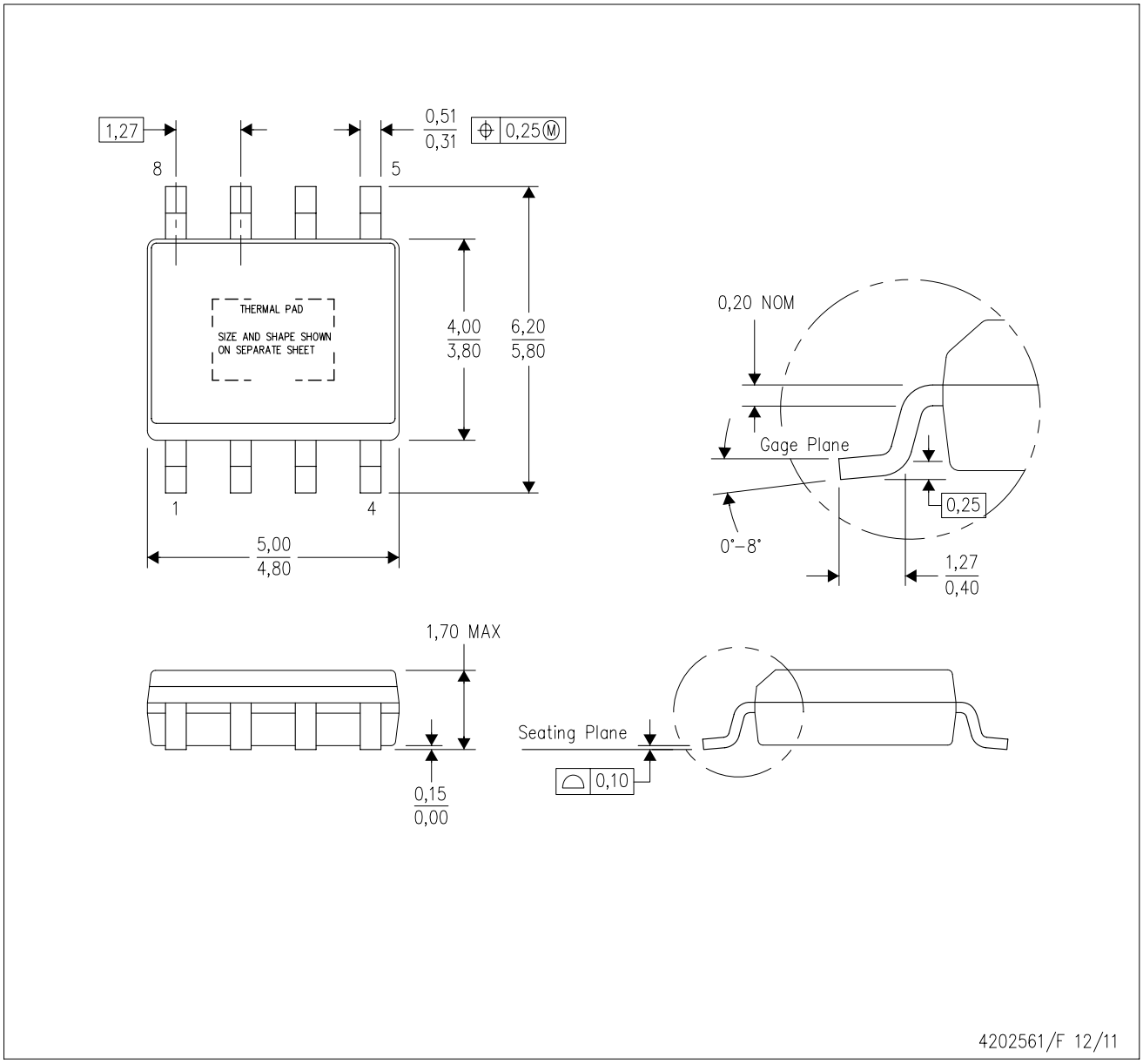
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

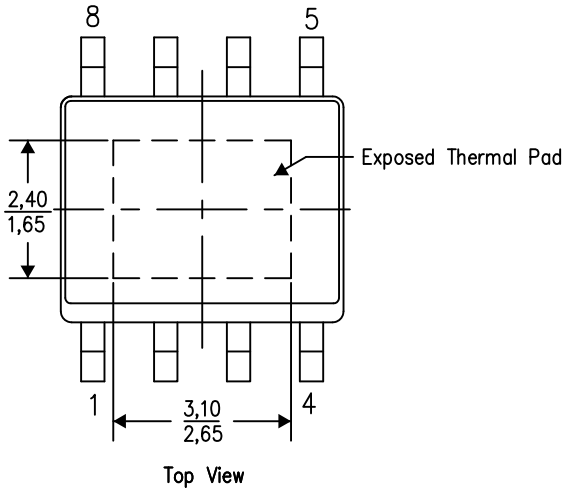
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



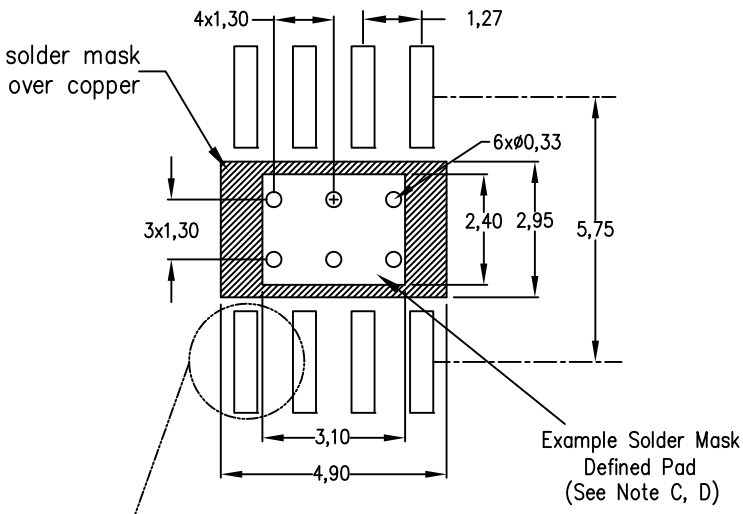
Exposed Thermal Pad Dimensions

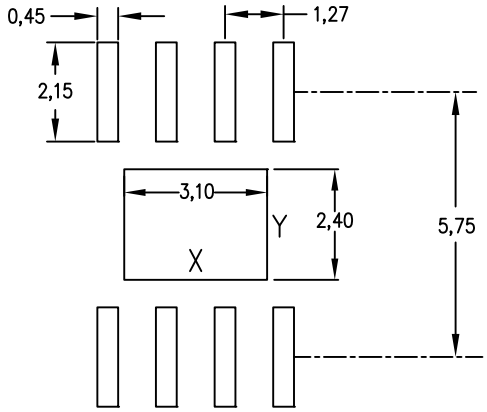
4206322-6/L 05/12

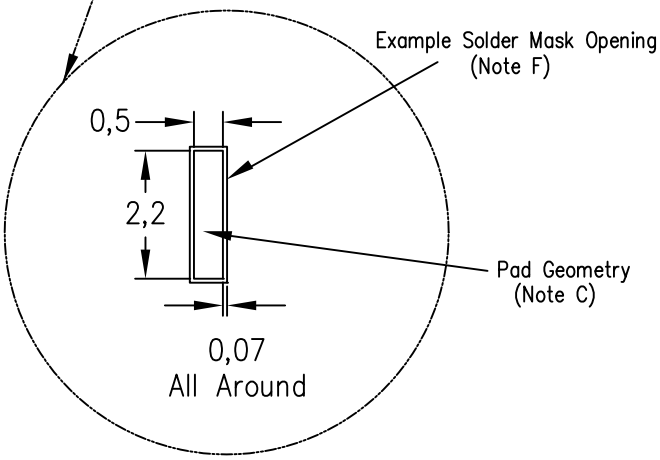
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE







Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951–6/D 04/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TPS6302x High Efficiency Single Inductor Buck-boost Converter with 4-A Switches

1 Features

- Input voltage range: 1.8 V to 5.5 V
- Adjustable output voltage: 1.2 V to 5.5 V
- Output current for V_{IN} > 2.5 V, V_{OUT} = 3.3 V: 2 A
- High efficiency over the entire load range
  - Operating quiescent current: 25 µA
  - Power save mode with mode selection
- Average current mode buck-boost architecture
  - Automatic transition between modes
  - Fixed frequency operation at 2.4 MHz
  - Synchronization possible
- Power good output
- Safety and robust operation features
  - Overtemperature, overvoltage protection
  - Load disconnect during shutdown
- Create a custom design using the
  - TPS63020 with WEBENCH Power Designer
  - TPS63021 with WEBENCH Power Designer

2 Applications

- Pre-regulation in battery-powered devices: EPOS (portable data terminal, barcode scanner), e-cigarette, single board computer, IP network camera, video doorbell, land mobile radios
- Voltage stabilizer: wired communication, wireless communication, PLC, optical module
- Backup supercapacitor supply: electricity meter, solid state drive (SSD) - enterprise

3 Description

The TPS6302x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, a one-cell Li-ion or Li-polymer battery, supercapacitors or other supply rails. Output currents up to 3 A are supported. When using batteries, they can be discharged down to below 2 V. The buck-boost converter is based on a fixed frequency, pulse width modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters power save mode to maintain high efficiency over a wide load current range. The power save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 4 A. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery.

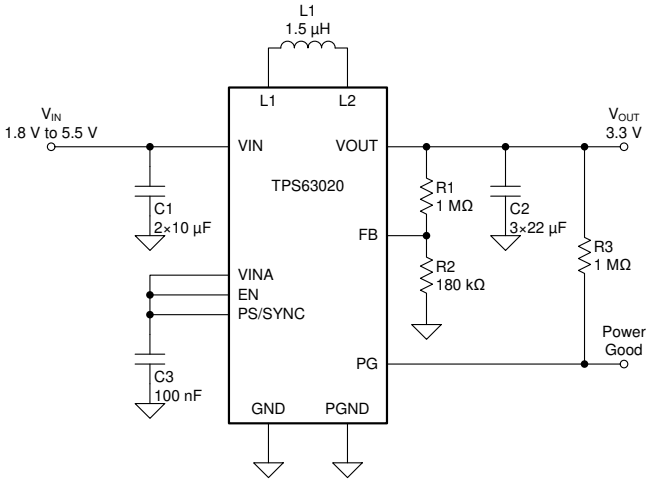
The TPS6302x devices operate over a free air temperature range of –40°C to 85°C. The devices are packaged in a 14-pin VSON package measuring 3 mm × 4 mm (DSJ).

Device Information(1)

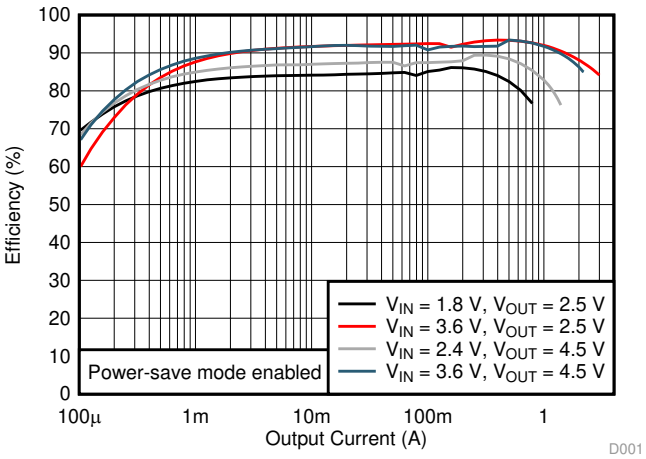
PART NUMBER	OUTPUT VOLTAGE	PACKAGE
TPS63020	Adjustable	VSON (14)
TPS63021	3.3 V	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs Output Current



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4 Revision History

Changes from Revision H (August 2019) to Revision I — **Page**

- Changed ESD numbers to reflect latest test insights ... 5
- Changed Footnotes in order to reflect wording of latest JEP155 and JEP157 specifications ... 5
- Changed V_{FB} naming and description for better readability ... 6

Changes from Revision G (March 2019) to Revision H — **Page**

- Changed R3 68 kΩ To: R4 68 kΩ in Figure 28 ... 21

Changes from Revision F (March 2019) to Revision G — **Page**

- Changed the Simplified Schematic, removed the connection from VINA to VIN ... 1
- Changed Figure 7, removed the connection from VINA to VIN ... 13
- Changed Figure 28, removed the connection from VINA to VIN ... 21

Changes from Revision E (May 2017) to Revision F — **Page**

- Updated Features and Applications on the 1st page ... 1
- Changed the Body Size column To: Output Voltage in the *Device Information* table ... 1
- Changed the *Pin Configuration* image ... 4
- Changed Chapter order in Application Information 13
- Updated output capacitor selection section ... 15
- Added Table of *Typical Characteristics Curves*. ... 17
- Changed Figure 24 and Figure 25 ... 19
- Added Figure 26 and Figure 27 ... 20
- Changed Figure 28 ... 21
- Added system examples *Supercapacitor Backup Power Supply With Active Cell Balancing* and *Low-Power TEC Driver* 22

Changes from Revision D (October 2015) to Revision E — **Page**

- Added Voltage AC-spec to *Absolute Maximum Ratings* table for L1, L2. 5

Changes from Revision C (February 2013) to Revision D — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision B (August 2012) to Revision C — **Page**

- Changed Figure 7 schematic to show correct component values. 13
- Changed Figure 28 schematic to show correct component values. 21

Changes from Revision A (December 2011) to Revision B — **Page**

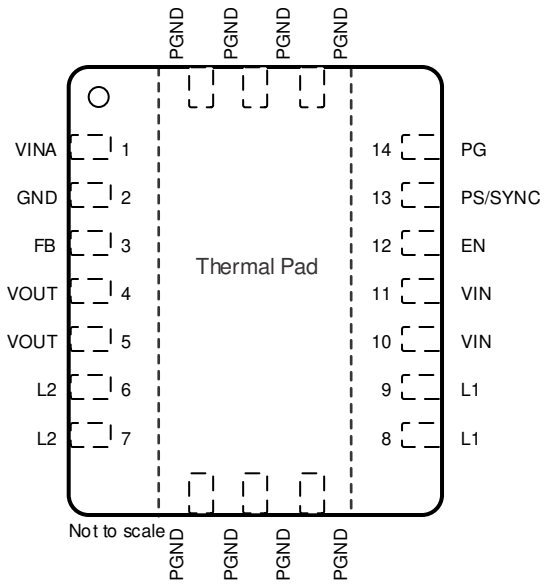
- Changed the Duty cycle in step down conversion values, added MIN = 20%, deleted TYP = 30% and MAX = 40% 6

Changes from Original (April 2010) to Revision A — **Page**

- Updated Figure 31 - PCB Layout Suggestion 23

5 Pin Configuration and Functions

DSJ Package
14-Pin VSON with Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	12	I	Enable input (1 enabled, 0 disabled), must not be left open
FB	3	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	2	–	Control / logic ground
L1	8, 9	I	Connection for inductor
L2	6, 7	I	Connection for inductor
PG	14	O	Output power good (1 good, 0 failure; open-drain), can be left open
PGND		–	Power ground
PS/SYNC	13	I	Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization), must not be left open
VIN	10, 11	I	Supply voltage for power stage
VINA	1	I	Supply voltage for control stage
VOUT	4, 5	O	Buck-boost converter output
Exposed Thermal Pad		–	The exposed thermal pad is connected to PGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage[2]	VIN, VINA, VOUT, PS/SYNC, EN, FB, PG	–0.3	7	V
	L1, L2 (DC)	–0.3	7	V
	L1, L2 (AC, less than 10 ns)[3]	–3	10	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Normal switching operation

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pins VIN, VINA, L1[1]	±500	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins[1]	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	

(1) JEDEC document JEP155 states that, with basic ESD control methods applied, 500 V HBM allows a safe manufacturing with proven margin.
(2) JEDEC document JEP157 states that, with basic ESD control methods applied, 250 V CDM allows a safe manufacturing.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage at VIN, VINA	1.8		5.5	V
Operating free air temperature, T_A	–40		85	°C
Operating junction temperature, T_J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS6302x DSJ (VSON) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage			1.8		5.5	V
	Minimum input voltage for start-up		0°C ≤ T_A ≤ 85°C	1.5	1.8	1.9	V
	Minimum input voltage for start-up			1.5	1.8	2.0	V
V_{OUT}	TPS63020 output voltage			1.2		5.5	V
	Duty cycle in step down conversion			20%			
V_{FB_PWM}	TPS63020 feedback voltage		PS/SYNC = V_{IN}	495	500	505	mV
	TPS63021 output voltage			3.267	3.3	3.333	V
V_{FB_PS}	TPS63020 feedback voltage / TPS63021 output voltage regulation in PS mode		PS/SYNC = GND; referenced to V_{FB_PWM}	0.6%		5%	
	Maximum line regulation				0.5%		
	Maximum load regulation				0.5%		
f	Oscillator frequency			2200	2400	2600	kHz
	Frequency range for synchronization			2200	2400	2600	kHz
I_{SW}	Average switch current limit		V_{IN} = V_{INA} = 3.6 V, T_A = 25°C	3500	4000	4500	mA
	High side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
	Low side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
I_q	Quiescent current	VIN and VINA	I_{OUT} = 0 mA, V_{EN} = V_{IN} = V_{INA} = 3.6 V, V_{OUT} = 3.3 V		25	50	µA
		VOUT			5	10	µA
	TPS63021 FB input impedance		V_{EN} = HIGH		1		MΩ
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = V_{INA} = 3.6 V		0.1	1	µA
CONTROL STAGE							
UVLO	Under voltage lockout threshold		V_{INA} voltage decreasing	1.4	1.5	1.6	V
	Under voltage lockout hysteresis				200		mV
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped to GND or VINA		0.01	0.1	µA
	PG output low voltage		V_{OUT} = 3.3 V, I_{PGL} = 10 µA		0.04	0.4	V
	PG output leakage current				0.01	0.1	µA
	Output overvoltage protection			5.5		7	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

6.6 Typical Characteristics

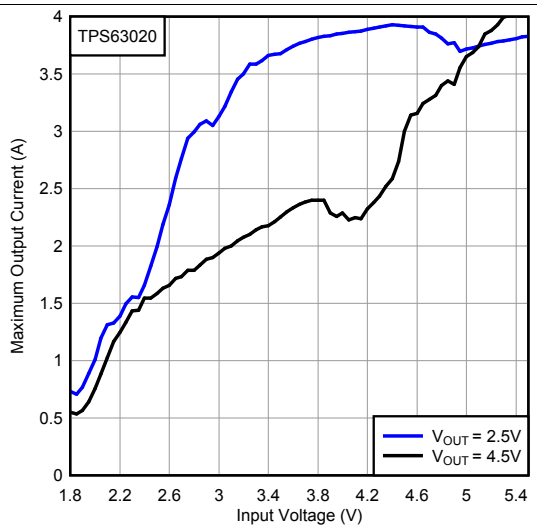


Figure 1. Maximum Output Current Versus Input Voltage, TPS63020, V_{OUT} = 2.5 V/4.5 V

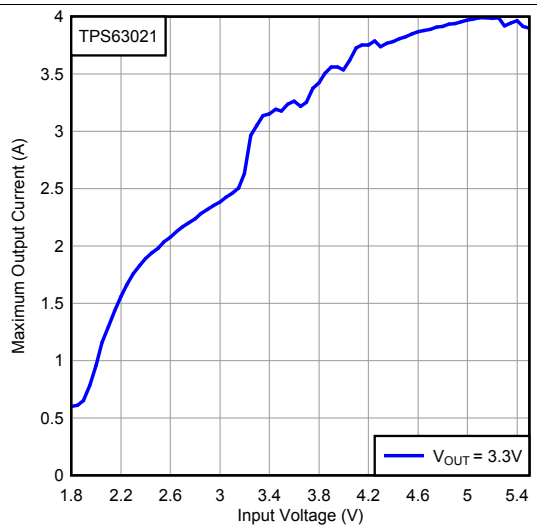


Figure 2. Maximum Output Current Versus Input Voltage, TPS63021, V_{OUT} = 3.3V

7 Detailed Description

7.1 Overview

The control circuit of the device is based on an average current mode topology. The controller also uses input and output voltage feed forward. Changes of input and output voltage are monitored and can immediately change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages, a resistive voltage divider must be connected to that pin. At fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The device uses four internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter. To protect the device from overheating an internal temperature sensor is implemented.

7.2 Functional Block Diagram

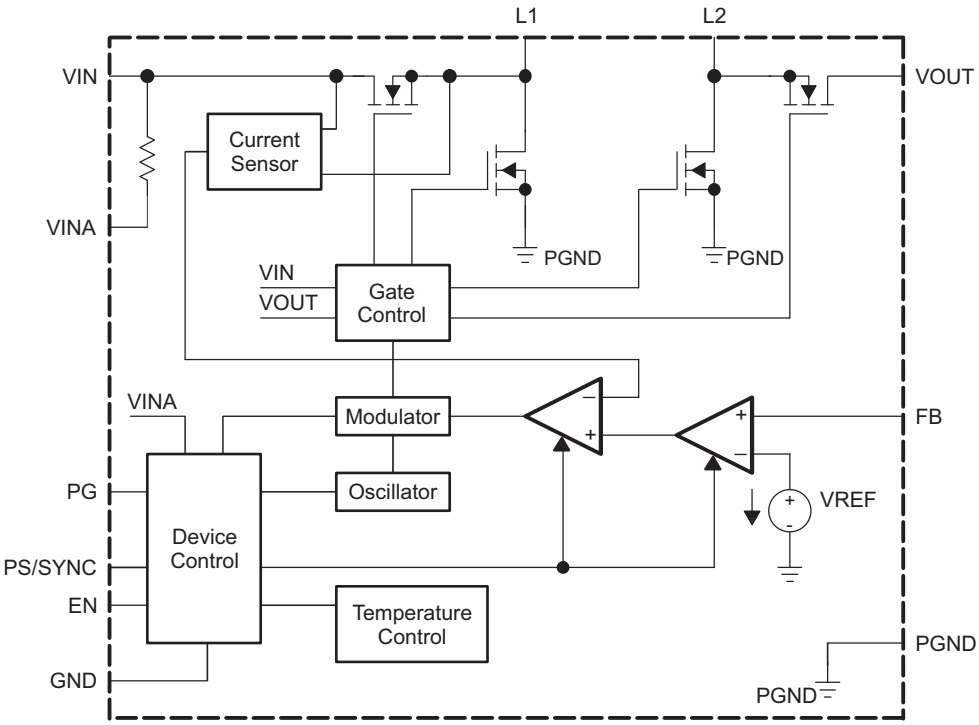


Figure 3. Functional Block Diagram (TPS63020)

Functional Block Diagram (continued)

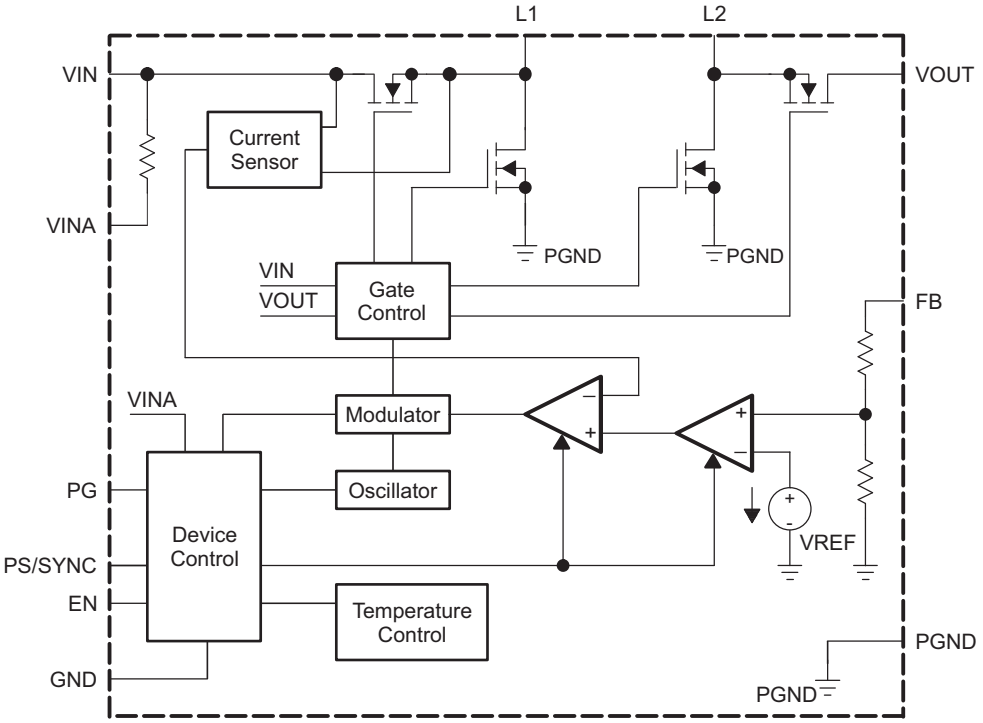


Figure 4. Functional Block Diagram (TPS63021)

7.3 Feature Description

7.3.1 Dynamic Voltage Positioning

As detailed in Figure 6, the output voltage is typically 3% above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. This allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transient changes.

7.3.2 Dynamic Current Limit

To protect the device and the application, the average inductor current is limited internally on the IC. At nominal operating conditions, this current limit is constant. The current limit value can be found in the electrical characteristics table. If the supply voltage at VIN drops below 2.3 V, the current limit is reduced. This can happen when the input power source becomes weak. Increasing output impedance, when the batteries are almost discharged, or an additional heavy pulse load is connected to the battery, can cause the VIN voltage to drop. The dynamic current limit has its lowest value when reaching the minimum recommended supply voltage at VIN. At this voltage, the device is forced into burst mode operation, trying to stay active as long as possible even with a weak input power source.

If the die temperature increases above the recommended maximum temperature, the dynamic current limit becomes active. Similar to the behavior when the input voltage at VIN drops, the current limit is reduced with temperature increasing.

7.3.3 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

Feature Description (continued)

7.3.4 Power Good

The device has a built-in power-good function to indicate whether the output voltage is regulated properly. As soon as the average inductor current limit is reached, the power-good output gets low impedance. The output is open-drain and can be left open if not needed. By connecting a pullup resistor to the supply voltage of the externally connected logic, it is possible to adjust the voltage level within the absolute maximum ratings.

Because it is monitoring the status of the current control loop, the power-good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react.

7.3.5 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore, overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. In case it reaches the overvoltage threshold, the voltage amplifier regulates the output voltage to this value.

7.3.6 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VINA is lower than approximately its threshold (see *Electrical Characteristics*). When in operation, the device automatically enters the shutdown mode if the voltage at VINA drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

7.3.7 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see *Electrical Characteristics*), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

7.4 Device Functional Modes

7.4.1 Soft-start and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial 400 mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit does not increase. There is no timer implemented. Thus, the output voltage overshoot at start-up, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. At a short on the output during operation, the current limit also is decreased accordingly.

7.4.2 Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from step-down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all four switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. For the remaining two switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

Device Functional Modes (continued)

7.4.3 Control Loop

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 5 shows the control loop.

The non-inverting input of the transconductance amplifier, gmv, is assumed to be constant. The output of gmv defines the average inductor current. The inductor current is reconstructed by measuring the current through the high-side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode, the current is measured during the on-time of the same MOSFET. During the off-time, the current is reconstructed internally starting from the peak value at the end of the on-time cycle. The average current and the feedback from the error amplifier gmv forms the correction signal gmc. This correction signal is compared to the buck and the boost sawtooth ramp giving the PWM signal. Depending on which of the two ramps, the gmc output crosses either the buck or the boost stage is initiated. When the input voltage is close to the output voltage, one buck cycle is always followed by a boost cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

The buck-boost overlap control makes sure that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Thanks to this block, whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other. On the other hand, when there is no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result, the number of classical buck-boost cycles or no switching is reduced to a minimum and high efficiency values has been achieved.

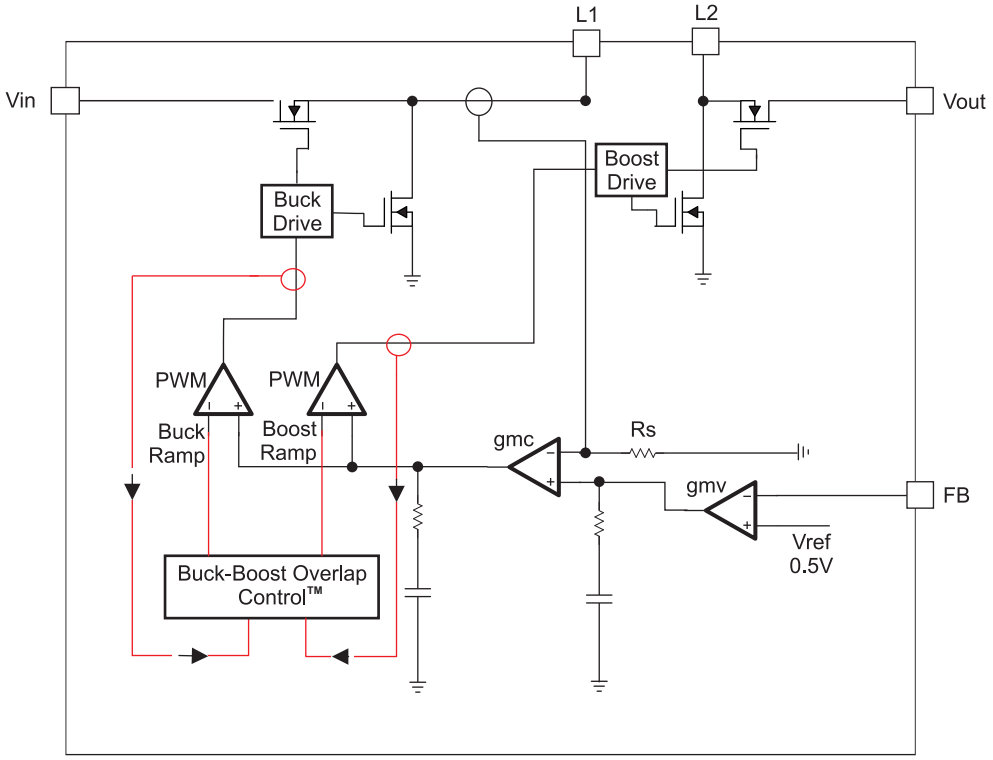


Figure 5. Average Current Mode Control

Device Functional Modes (continued)

7.4.4 Power Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. Power save mode is used to improve efficiency at light load. To enable power save mode, PS/SYNC must be set low. If PS/SYNC is set low, then power save mode is entered when the average inductor current gets lower than about 100 mA. At this point, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. See Figure 6 for detailed operation of the power save mode.

During the power save mode, the output voltage is monitored with a comparator by the threshold comp low and comp high. When the device enters power save mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comp low threshold set to 2.5% typical above V_{OUT}, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last one or several pulses. The converter continues these pulses until the comp high threshold, set to typically 3.5% above V_{OUT} nominal, is reached and the average inductance current gets lower than about 100 mA. When the load increases above the minimum forced inductor current of about 100 mA, the device automatically switches to pulse width modulation (PWM) mode.

The power save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a phase-locked loop (PLL), so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

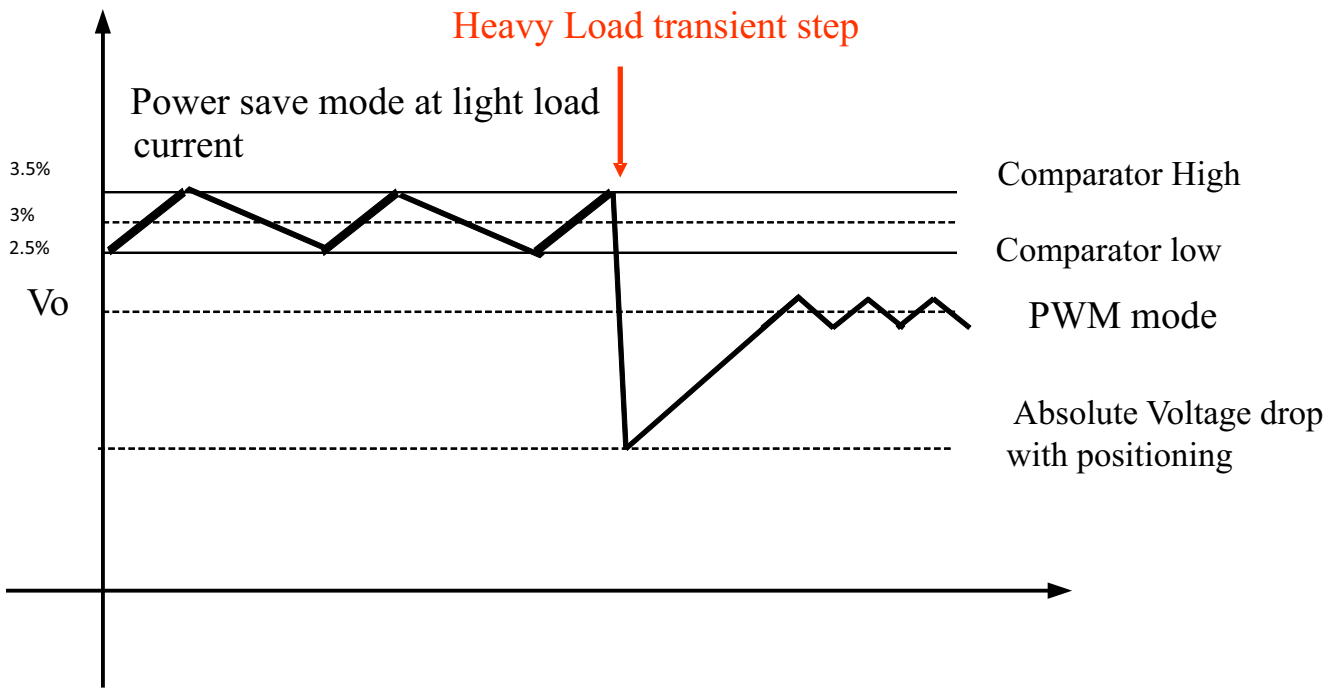


Figure 6. Power Save Mode Thresholds and Dynamic Voltage Positioning

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS6302x are high efficiency, low quiescent current, non-inverting buck-boost converters suitable for applications that need a regulated output voltage from an input supply that can be higher, lower, or equal to the output voltage. Output currents can go as high as 2 A in boost mode and as high as 4 A in buck mode. The average current in the switches is limited to a typical value of 4 A.

8.2 Typical Application

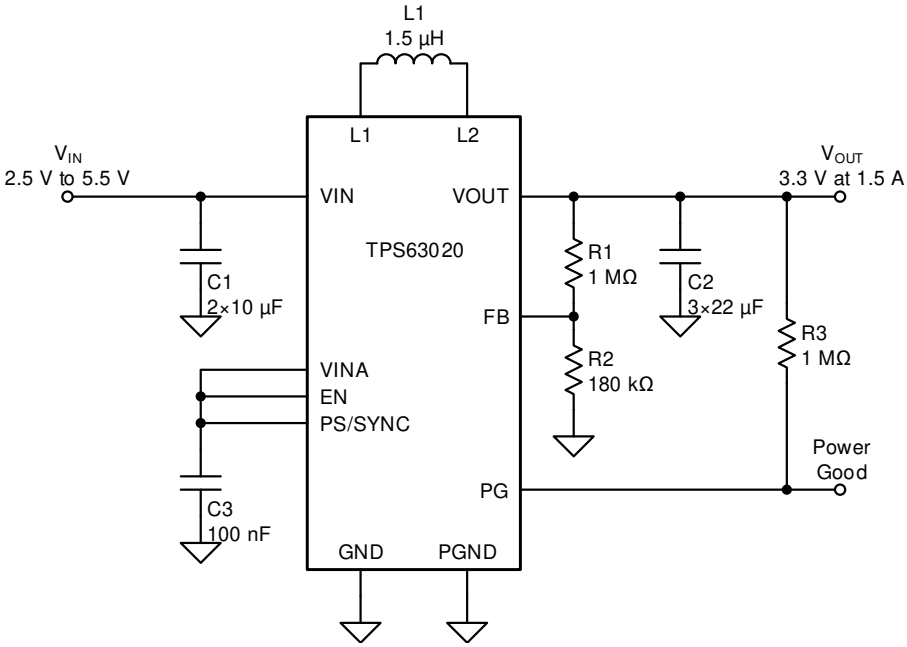


Figure 7. Application Circuit

8.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. See Table 1 for possible inductor and capacitor combinations.

For the fixed output voltage option, the feedback pin needs to be connected to the VOUT pin.

Table 1. Matrix of Output Capacitor and Inductor Combinations

NOMINAL INDUCTOR VALUE [µH] (1)	NOMINAL OUTPUT CAPACITOR VALUE [µF] (2)			
	2×22	3×22	4×22	≥ 100
1.0		+	+	+
1.5	+	+ (3)	+	+
2.2			+	+

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check marks indicate possible filter combinations.

8.2.2 Detailed Design Procedure

The TPS6302x series of buck-boost converter has internal loop compensation. Therefore, the external inductor and output capacitors have to be selected to work with the internal compensation. When selecting the external components, a low limit for the inductor value exists to avoid subharmonic oscillation which can be caused by a far too fast ramp up of the inductor current. For the TPS6302x series, the inductor value must be kept at or above 1 µH.

In particular, either 1 µH or 1.5 µH is recommended working at an output current between 1.5 A and 2 A. If operating with a lower load current, it is also possible to use 2.2 µH.

Selecting a larger output capacitor value is less critical because the corner frequency moves to lower frequencies.

8.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS63020 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.2.2 Inductor Selection

The inductor selection is affected by several parameters such as the following:

- Inductor ripple current
- Output voltage ripple
- Transition point into Power Save Mode
- Efficiency

See Table 2 for a list of typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. Use Equation 2 to avoid saturation of the inductor when calculating the peak current for the inductor in steady state operation. Only the equation which defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L}$$

where

- D = duty cycle in boost mode
- f = converter switching frequency (typical 2.5 MHz)
- L = inductor value
- η = estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption) (2)

NOTE

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 2. Table 2 lists the possible inductors.

Table 2. List of Recommended Inductors (1)

INDUCTOR VALUE [µH]	SATURATION CURRENT [A]	DCR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (LxWxH mm)
1.5	5.1	15	XFL4020-152ME	Coilcraft	4 x 4 x 2.1
1.5	5.4	24	FDV0530S-H-1R5M	muRata	5 x 5 x 3

(1) See *Third-party Products Disclaimer.*

8.2.2.3 Output Capacitor Selection

For the output capacitor, it is recommended to use of small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended nominal output capacitors are three times 22 µF. If, for any reason, the application requires the use of large capacitors that cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. Place the small capacitor as close as possible to the VOUT and PGND pins of the IC.

There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

8.2.2.4 Input Capacitor Selection

A 10 µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS6302x converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

8.2.2.5 Bypass Capacitor

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VINA and GND. Using a ceramic capacitor with a value of 0.1 µF is recommended. The value of this capacitor must not be higher than 0.22 µF.

8.2.3 Setting The Output Voltage

When the adjustable output voltage version TPS63020 is used, the output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 500 mV nominal. The low-side resistor R2 (between FB and GND) must be kept in the range of 200 kΩ. Use Equation 3 to calculate the high-side resistor R1 (between VOUT and FB).

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where

- V_{FB}= 500 mV (3)

Table 3. Resistor Selection For Typical Output Voltages

V_{OUT}	R1	R2
2.5 V	750 kΩ	180 kΩ
3.3 V	1 MΩ	180 kΩ
3.6 V	1.1 MΩ	180 kΩ

Table 3. Resistor Selection For Typical Output Voltages (continued)

V_{OUT}	R1	R2
4.5 V	1.43 MΩ	180 kΩ
5 V	1.6 MΩ	180 kΩ

8.2.4 Application Curves

Table 4. Components for Application Characteristic Curves for V_{OUT} = 3.3 V(1)(2)

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER
U1	High Efficiency Single Inductor Buck-Boost Converter With 4-A Switches	TPS63020 or TPS63021	Texas Instruments
L1	1.5 µH, 4 mm x 4 mm x 2 mm	XFL4020-152ML	Coilcraft
C1	2 × 10 µF 6.3 V, 0603, X5R ceramic	GRM188R60J106ME84D	muRata
C2	3 × 22 µF 6.3 V, 0603, X5R ceramic	GRM188R60J226MEAOL	muRata
C3	0.1 µF, X5R or X7R ceramic	Standard	Standard
R1	1 MΩ at TPS63020, 0 Ω at TPS63021	Standard	Standard
R2	180 kΩ at TPS63020, not used at TPS63021	Standard	Standard
R3	1 MΩ	Standard	Standard

(1) See *Third-Party Products Discalimer.*
(2) For other output voltages, refer to Table 3 for resistor values.

Table 5. Typical Characteristics Curves

PARAMETER	CONDITIONS	FIGURE
EFFICIENCY		
Efficiency vs Output Current, TPS63020 (Power save mode enabled)	V_{IN} = 1.8 V, 2.4 V, 3.6 V, V_{OUT} = 2.5 V, 4.5 V, PS/SYNC = Low	Figure 8
Efficiency vs Output Current, TPS63020 (PWM only)	V_{IN} = 1.8 V, 2.4 V, 3.6 V, V_{OUT} = 2.5 V, 4.5 V, PS/SYNC = High	Figure 9
Efficiency vs Output Current, TPS63021 (Power save mode enabled)	V_{IN} = 2.4 V, 3.6 V, V_{OUT} = 3.3 V, PS/SYNC = Low	Figure 10
Efficiency vs Output Current, TPS63021 (PWM only)	V_{IN} = 2.4 V, 3.6 V, V_{OUT} = 3.3 V, PS/SYNC = High	Figure 11
Efficiency vs Input Voltage, TPS63020 (Power save mode enabled)	V_{OUT} = 2.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low	Figure 12
Efficiency vs Input Voltage, TPS63020 (Power save mode enabled)	V_{OUT} = 4.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low	Figure 13
Efficiency vs Input Voltage, TPS63020 (PWM only)	V_{OUT} = 2.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low	Figure 14
Efficiency vs Input Voltage, TPS63020 (PWM only)	V_{OUT} = 2.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low	Figure 15
Efficiency vs Input Voltage, TPS63021 (Power save mode enabled)	V_{OUT} = 3.3 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low	Figure 16
Efficiency vs Input Voltage, TPS63021 (PWM only)	V_{OUT} = 3.3 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low	Figure 17
REGULATION ACCURACY		
Load Regulation, PWM Boost Operation, TPS63020	V_{IN} = 3.6 V , V_{OUT} = 4.5 V, PS/SYNC = High	Figure 18
Load Regulation, PWM Buck Operation, TPS63020	V_{IN} = 3.6 V, V_{OUT} = 2.5 V, PS/SYNC = High	Figure 19
Load Regulation, PWM Operation, TPS63021	V_{IN} = 3.6 V, V_{OUT} = 3.3 V, PS/SYNC = High	Figure 20
Load Transient, TPS63021	V_{IN} = 2.4 V, V_{OUT} = 3.3 V, Load = 500 mA to 1.5 A	Figure 21
Load Transient, TPS63021	V_{IN} = 4.2 V, V_{OUT} = 3.3 V, Load = 500 mA to 1.5 A	Figure 22
Line Transient, TPS63021	V_{IN} = 3.0 V to 3.7 V, V_{OUT} = 3.3 V, Load = 1.5 A	Figure 23
START-UP		
Start-up Behavior from Rising Enable, TPS63021	V_{IN} = 2.4 V, V_{OUT} = 3.3 V, Load = 2.2 Ω	Figure 24
Start-up Behavior from Rising Enable, TPS63021	V_{IN} = 4.2 V, V_{OUT} = 3.3 V, Load = 2.2 Ω	Figure 25
Start-up Behavior from Rising Enable, TPS63021	V_{IN} = 2.4 V, V_{OUT} = 3.3 V, Load = 2.2 Ω	Figure 26
Start-up Behavior from Rising Enable, TPS63021	V_{IN} = 4.2 V, V_{OUT} = 3.3 V, Load = 2.2 Ω	Figure 27

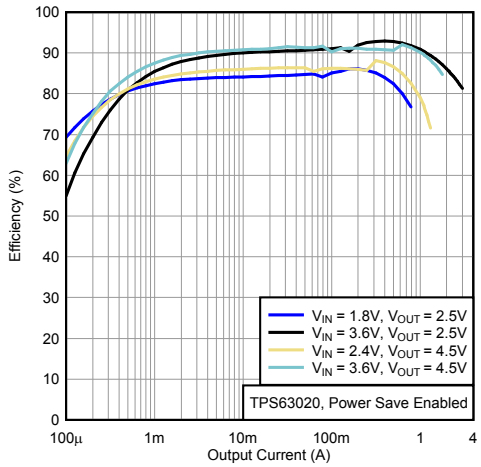


Figure 8. Efficiency Versus Output Current, TPS63020, Power Save Enabled

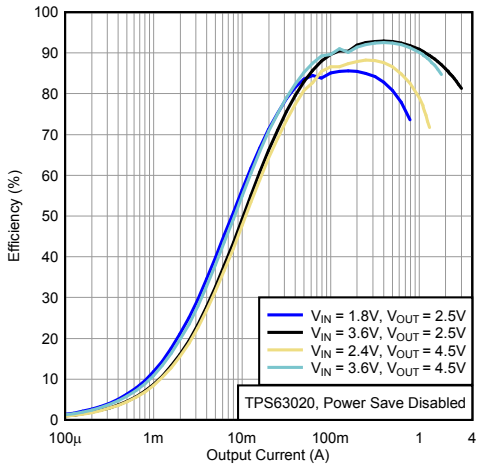


Figure 9. Efficiency Versus Output Current, TPS63020, Power Save Disabled

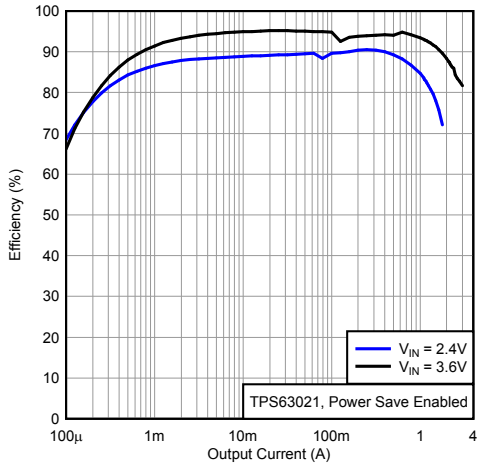


Figure 10. Efficiency Versus Output Current, TPS63021, Power Save Enabled

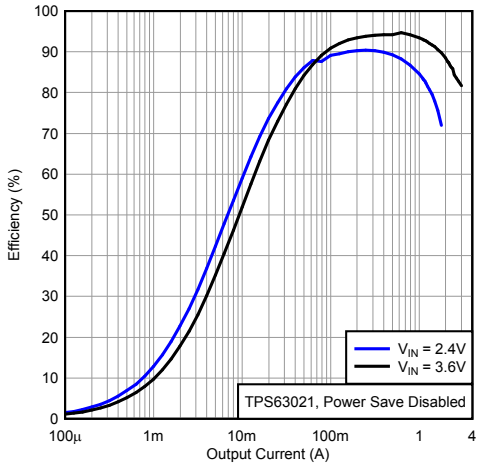


Figure 11. Efficiency Versus Output Current, TPS63021, Power Save Disabled

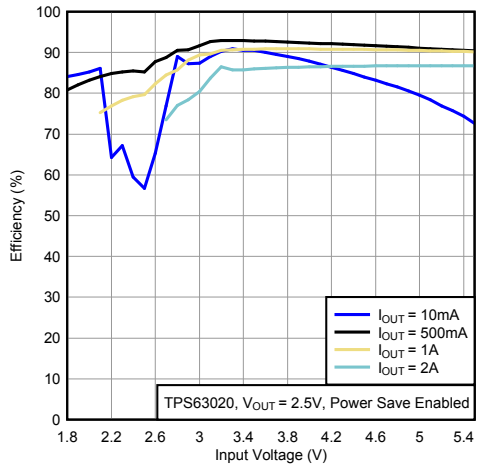


Figure 12. Efficiency Versus Input Voltage, TPS63020, V_{OUT} = 2.5 V, Power Save Enabled

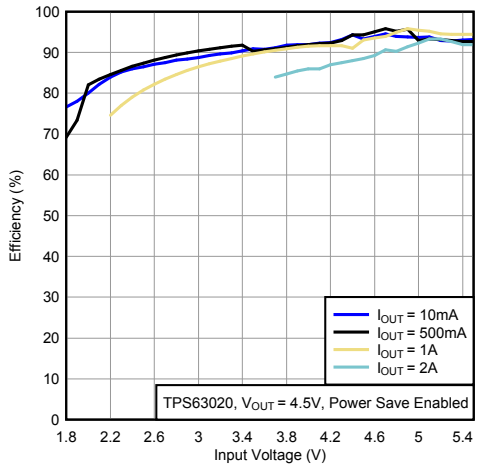


Figure 13. Efficiency Versus Input Voltage, TPS63020, V_{OUT} = 4.5 V, Power Save Enabled

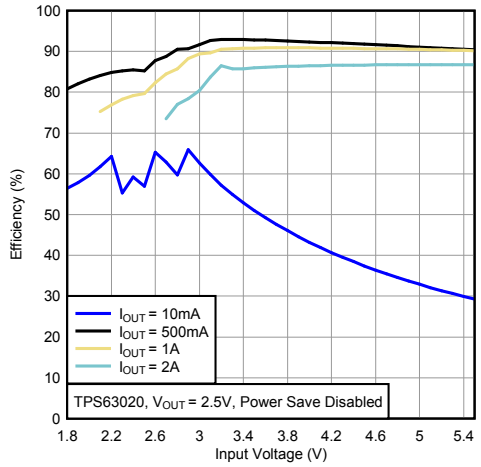


Figure 14. Efficiency Versus Input Voltage, TPS63020, V_{OUT} = 2.5 V, Power Save Disabled

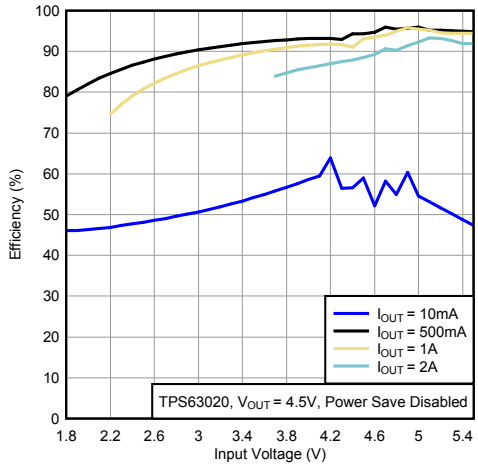


Figure 15. Efficiency Versus Input Voltage, TPS63020, V_{OUT} = 4.5 V, Power Save Disabled

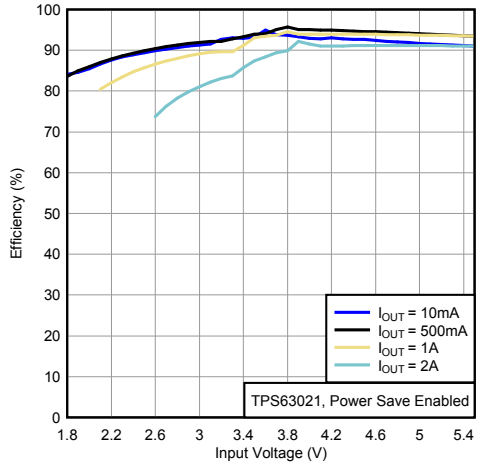


Figure 16. Efficiency Versus Input Voltage, TPS63021, Power Save Enabled

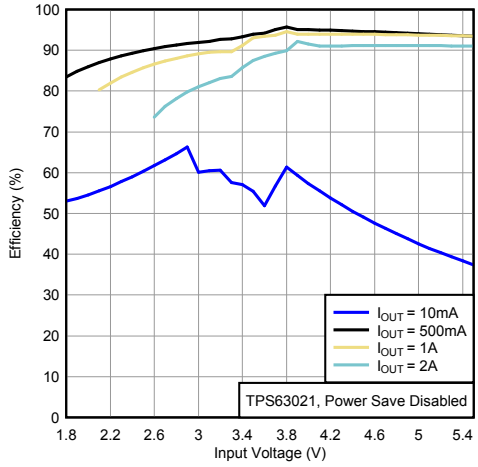


Figure 17. Efficiency Versus Input Voltage, TPS63021, Power Save Disabled

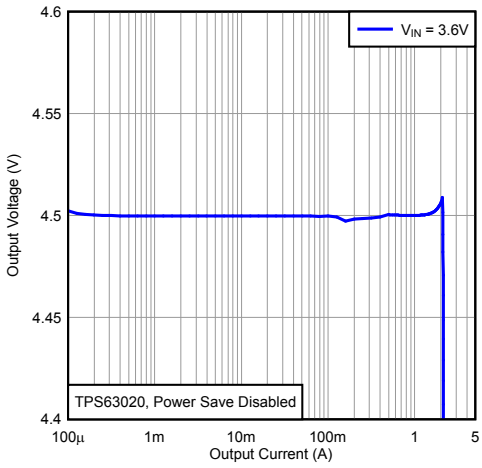


Figure 18. Output Voltage Versus Output Current, TPS63020, Power Save Disabled

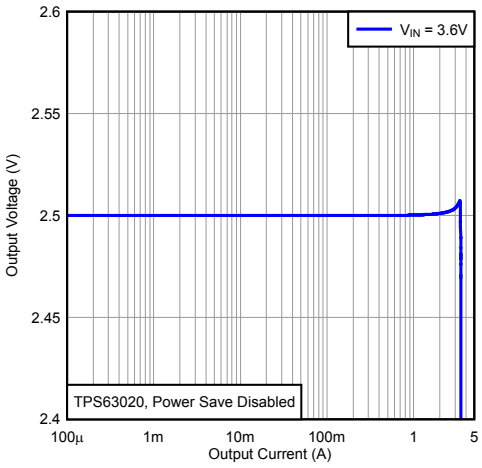


Figure 19. Output Voltage Versus Output Current, TPS63020, Power Save Enabled

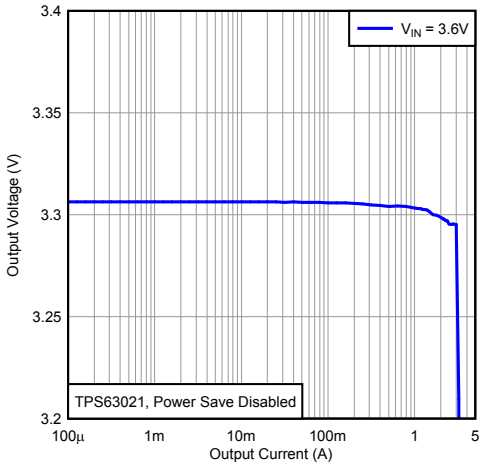
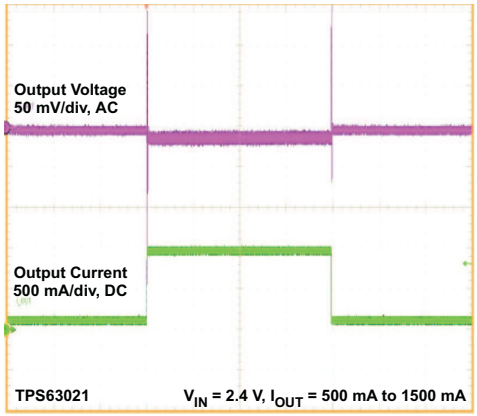
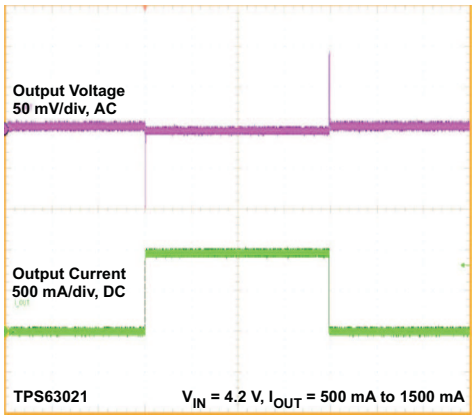


Figure 20. Output Voltage Versus Output Current, TPS63021, Power Save Disabled



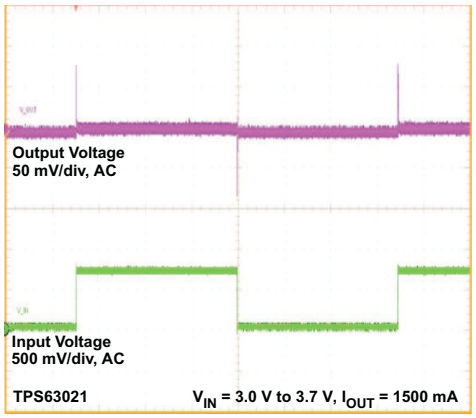
Time 2 ms/div

Figure 21. Load Transient Response, TPS63021



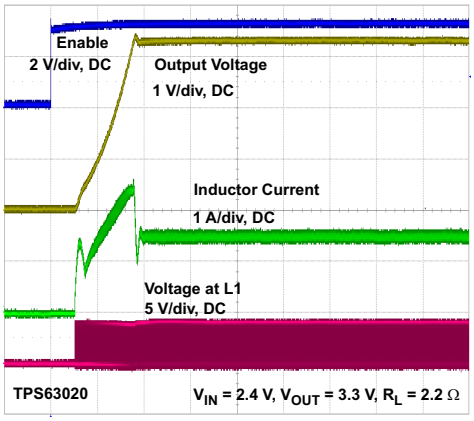
Time 2 ms/div

Figure 22. Load Transient Response, TPS63021



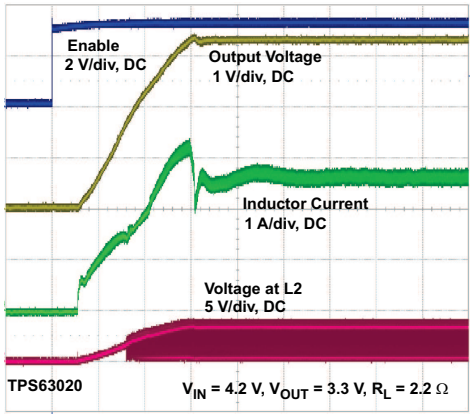
Time 2 ms/div

Figure 23. Line Transient Response, TPS63021



Time 100 µs/div

Figure 24. Start-up Behavior from Rising Enable, TPS63020



Time 100 µs/div

Figure 25. Start-up Behavior from Rising Enable, TPS63020

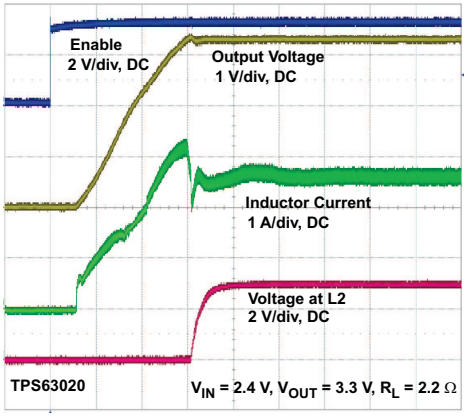


Figure 26. Start-up Behavior from Rising Enable, TPS63020

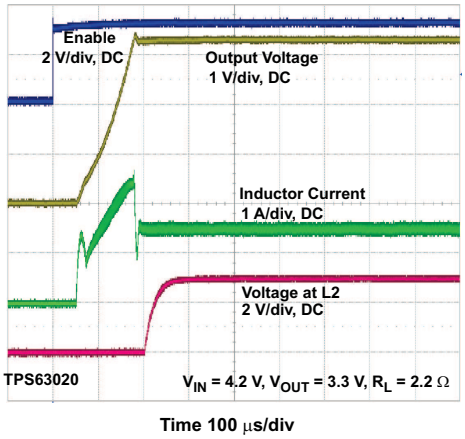


Figure 27. Start-up Behavior from Rising Enable, TPS63020

8.3 System Examples

8.3.1 Improved Transient Response for 2 A Load Current

Capacitor C4 and resistor R4 are added for improved load transient performance.

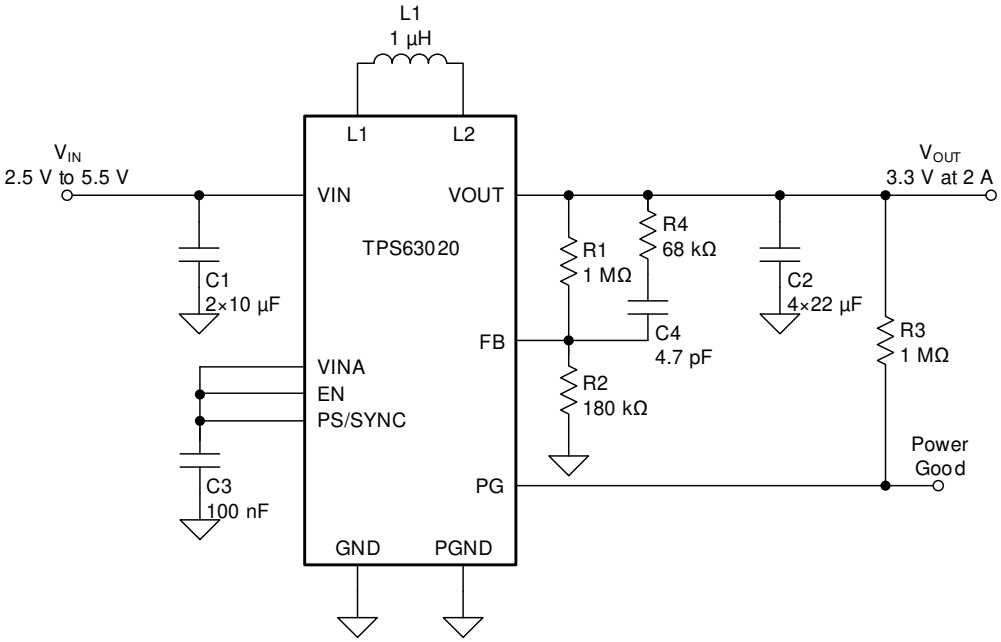


Figure 28. Application Circuit for 2 A Load Current

System Examples (continued)

8.3.2 Supercapacitor Backup Power Supply With Active Cell Balancing

The TPS63020 can be used to charge backup capacitors to a user-defined voltage level while the main power supply is supplying a system, and discharges these capacitors into the system when the main power supply is interrupted. With this design, the system voltage during backup operation keeps constant independent of the voltage reduction on the backup capacitors. Refer to the *PMP9766 Test Results Application Report* for more details.

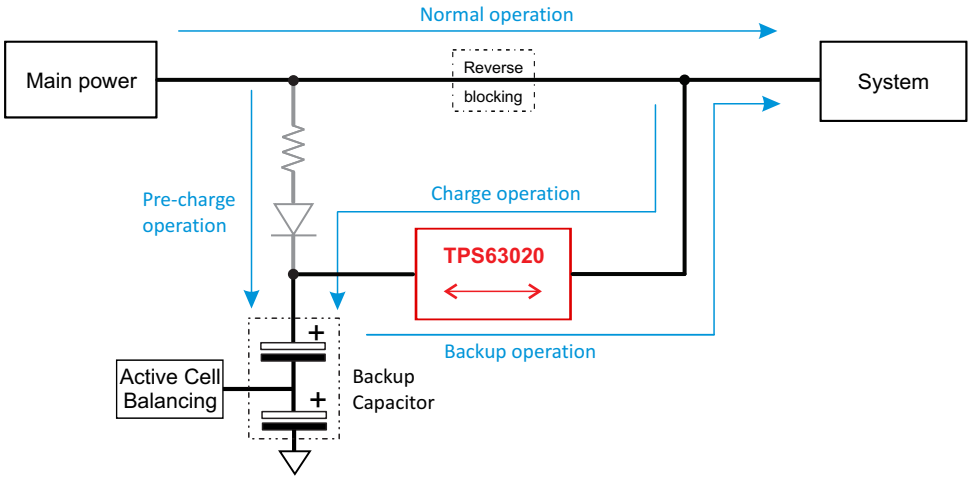


Figure 29. Simplified Block Diagram of a Backup Power System

8.3.3 Low-Power TEC Driver

Controlling the operating temperature of electronic circuits helps attain the best system performance. For passive control, that is, when heat sinks is not giving the right performance, active cooling using a thermoelectric cooler (TEC) might be able to solve the thermal issue. Figure 30 shows an example driving such a TEC element with the TPS63020. Refer to the *Low-power TEC Driver Application Report*.

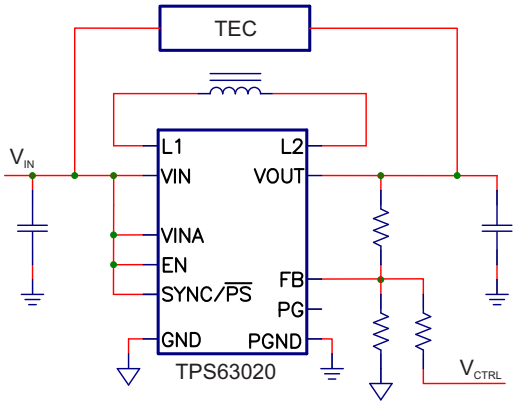


Figure 30. Low-Power TEC Driver Schematic

9 Power Supply Recommendations

The TPS6302x devices have no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS6302x.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. Place the input capacitor, output capacitor, and the inductor as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider must be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

10.2 Layout Example

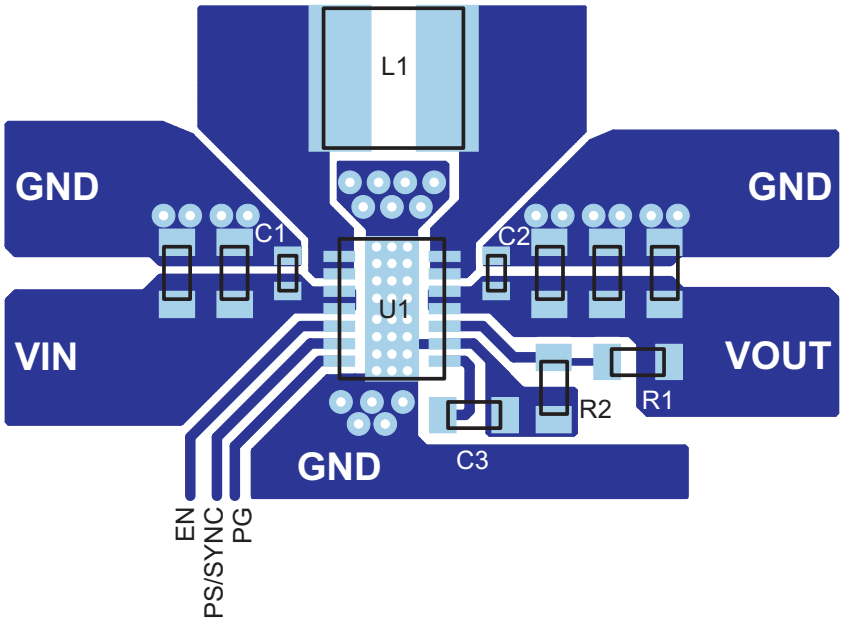


Figure 31. PCB Layout Suggestion

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

Refer to the *Thermal Characteristics Application Note* and the *Semiconductor and IC Package Thermal Metrics Application Note* for more details on how to use the thermal parameters.

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Device Support

11.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS63021 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance,
   – Run thermal simulations to understand the thermal performance of your board,
   – Export your customized schematic and layout into popular CAD formats,
   – Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

11.2.2 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.3 Documentation Support

11.3.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Characteristics Application Note*
- Texas Instruments, *IC Package Thermal Metrics Application Note*

11.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS63020	Click here	Click here	Click here	Click here	Click here
TPS63021	Click here	Click here	Click here	Click here	Click here

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63020DSJR	ACTIVE	VSON	DSJ	14	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63020	Samples
TPS63020DSJT	ACTIVE	VSON	DSJ	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63020	Samples
TPS63021DSJR	ACTIVE	VSON	DSJ	14	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63021	Samples
TPS63021DSJT	ACTIVE	VSON	DSJ	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63021	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS63020 :

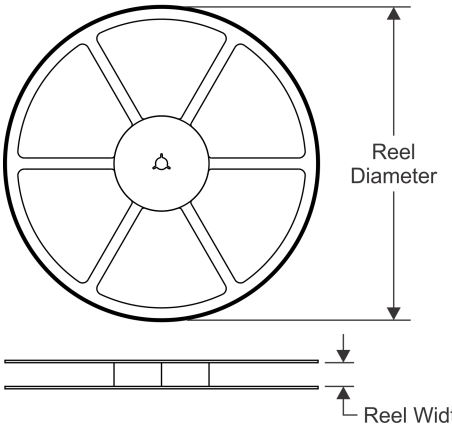
- Automotive: TPS63020-Q1

NOTE: Qualified Version Definitions:

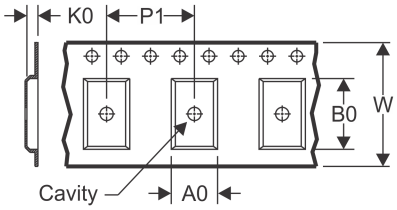
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

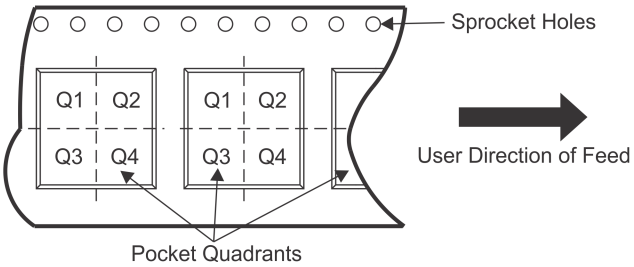


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

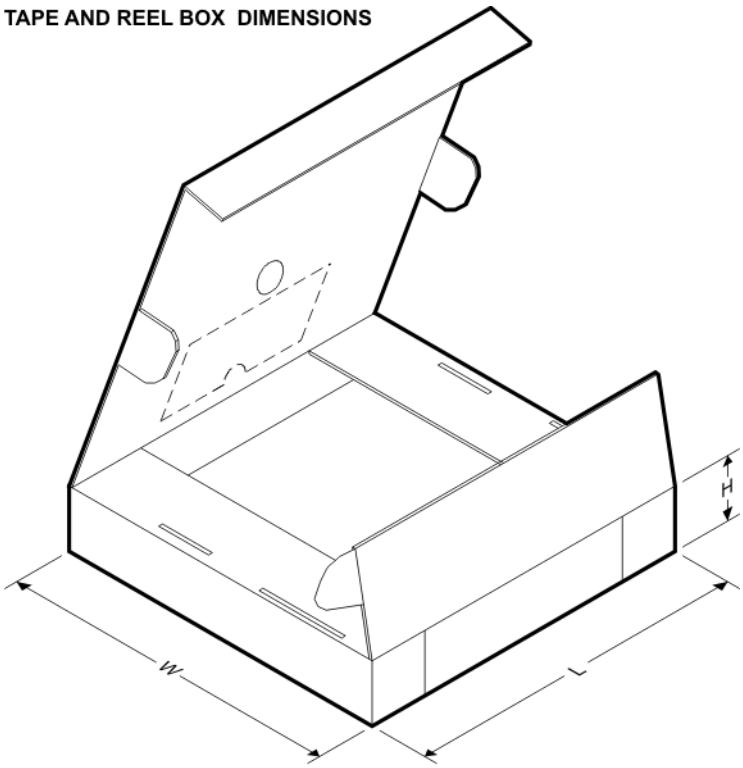
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63020DSJR	VSON	DSJ	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS63020DSJR	VSON	DSJ	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS63020DSJT	VSON	DSJ	14	250	180.0	12.5	3.3	4.3	1.1	8.0	12.0	Q1
TPS63021DSJR	VSON	DSJ	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS63021DSJR	VSON	DSJ	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS63021DSJT	VSON	DSJ	14	250	180.0	12.5	3.3	4.3	1.1	8.0	12.0	Q1
TPS63021DSJT	VSON	DSJ	14	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

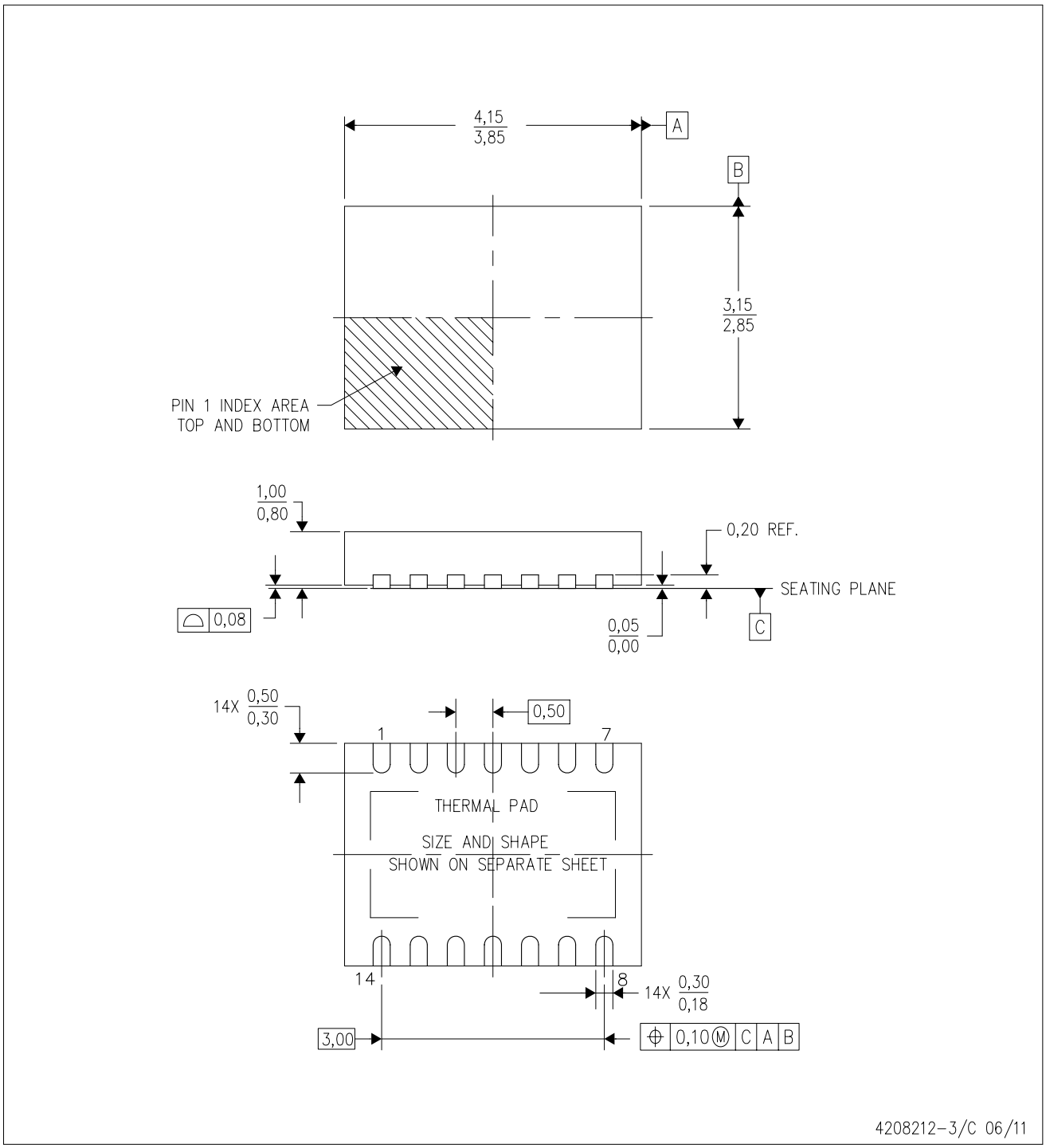
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63020DSJR	VSON	DSJ	14	3000	338.0	355.0	50.0
TPS63020DSJR	VSON	DSJ	14	3000	367.0	367.0	35.0
TPS63020DSJT	VSON	DSJ	14	250	205.0	200.0	33.0
TPS63021DSJR	VSON	DSJ	14	3000	338.0	355.0	50.0
TPS63021DSJR	VSON	DSJ	14	3000	367.0	367.0	35.0
TPS63021DSJT	VSON	DSJ	14	250	205.0	200.0	33.0
TPS63021DSJT	VSON	DSJ	14	250	210.0	185.0	35.0

DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

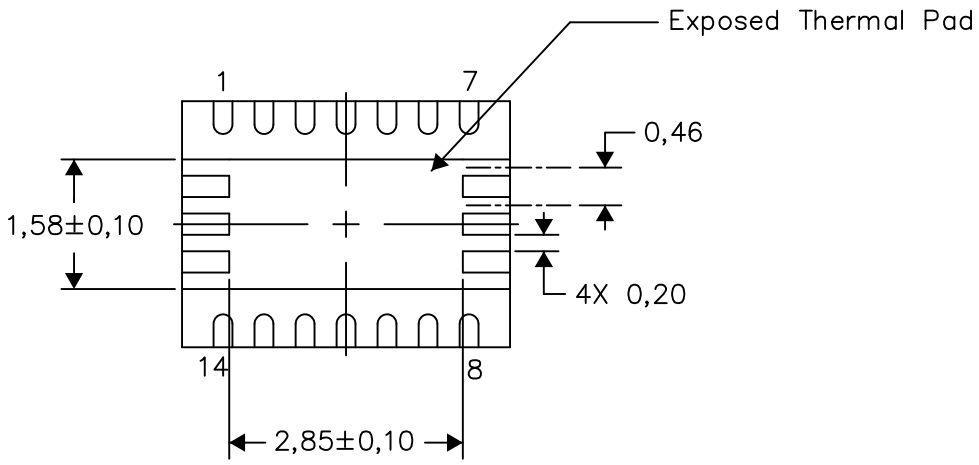
DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



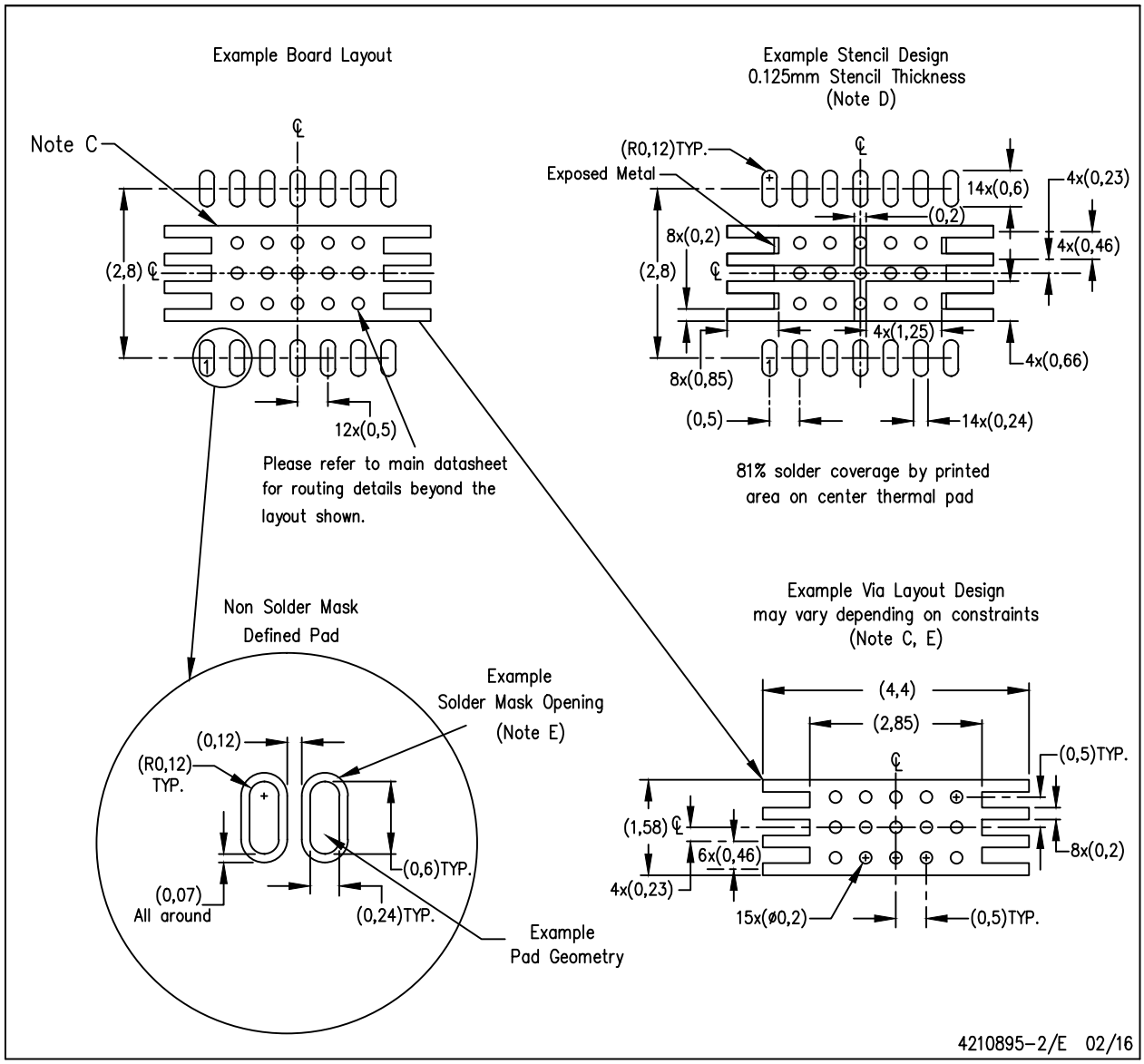
Bottom View

Exposed Thermal Pad Dimensions

4208549–3/G 04/15

NOTE: All linear dimensions are in millimeters

DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

Ferrites and accessories

E 20/10/6 (EF 20)
Cores and accessories

Series/Type: **B66311, B66206**

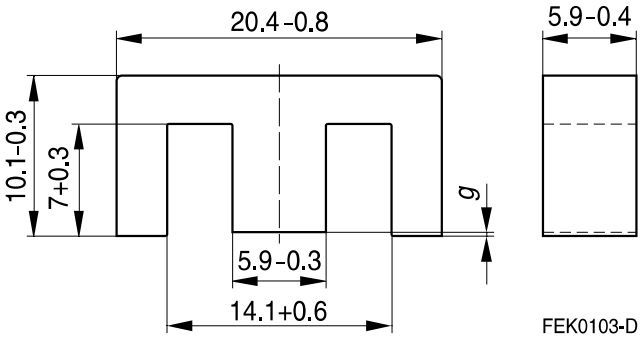
Date: May 2017

EPCOS AG is a TDK Group Company.

E 20/10/6 (EF 20)

Core **B66311**

- To IEC 62317-8
- Delivery mode: single units



Magnetic characteristics (per set)

$\Sigma l/A$ = 1.44 mm^{-1}
l_e = 46.3 mm
A_e = 32.1 mm^2
A_{min} = 31.9 mm^2
V_e = 1490 mm^3

Approx. weight 7.3 g/set

Ungapped

Material	A_L value nH	μ_e	P_V W/set	Ordering code
N30	2150 +30/–20%	2460		B66311G0000X130
T46	7500 ±30%	8610		B66311F0000X146
N27	1300 +30/–20%	1490	< 0.27 (200 mT, 25 kHz, 100 °C)	B66311G0000X127
N87	1470 +30/–20%	1680	< 0.75 (200 mT, 100 kHz, 100 °C)	B66311G0000X187
N97	1500 +30/–20%	1720	< 0.70 (200 mT, 100 kHz, 100 °C)	B66311G0000X197

Gapped (A_L values/air gaps examples)

Material	g mm	A_L value approx. nH	μ_e	Ordering code ** = 27 (N27) = 87 (N87)
N27,	0.09 ±0.01	363	415	B66311G0090X1**
N87	0.10 ±0.02	345	395	B66311G0100X1**
	0.15 ±0.02	250	290	B66311G0150X1**
	0.17 ±0.02	227	259	B66311G0170X1**
	0.25 ±0.02	171	195	B66311G0250X1**
	0.50 ±0.05	103	118	B66311G0500X1**
	1.00 ±0.05	60	70	B66311G1000X1**

The A_L value in the table applies to a core set comprising one ungapped core (dimension g = 0 mm) and one gapped core (dimension g > 0 mm).

Other A_L values/air gaps and materials available on request — see Processing remarks on page 8.

Calculation factors (for formulas, see *"E cores: general information"*)

Material	Relationship between air gap – A_L value		Calculation of saturation current			
	K1 (25 °C)	K2 (25 °C)	K3 (25 °C)	K4 (25 °C)	K3 (100 °C)	K4 (100 °C)
N27	61.6	–0.737	88.1	–0.847	80.9	–0.865
N87	61.6	–0.737	88.5	–0.796	78.4	–0.873

Validity range: K1, K2: 0.05 mm < s < 1.50 mm
K3, K4: 50 nH < A_L < 430 nH

Coil former (magnetic axis horizontal or vertical)

Material: GFR polyterephthalate (UL 94 V-0, insulation class to IEC 60085: F ≙ max. operating temperature 155 °C), color code black Valox 420-SE0 [E207780 (M)] SABIC JAPAN L L C

Solderability: to IEC 60068-2-20, test Ta, method 1 (aging 3): 235 °C, 2 s

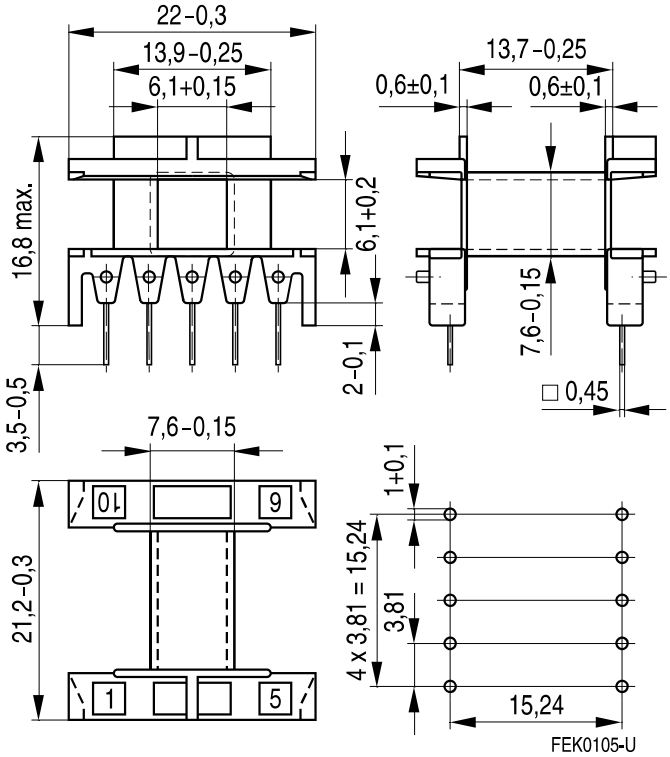
Resistance to soldering heat: to IEC 60068-2-20, test Tb, method 1B: 350 °C, 3.5 s

Winding: see Processing notes, 2.1

Pins: Squared pins. For matching yoke see next page.

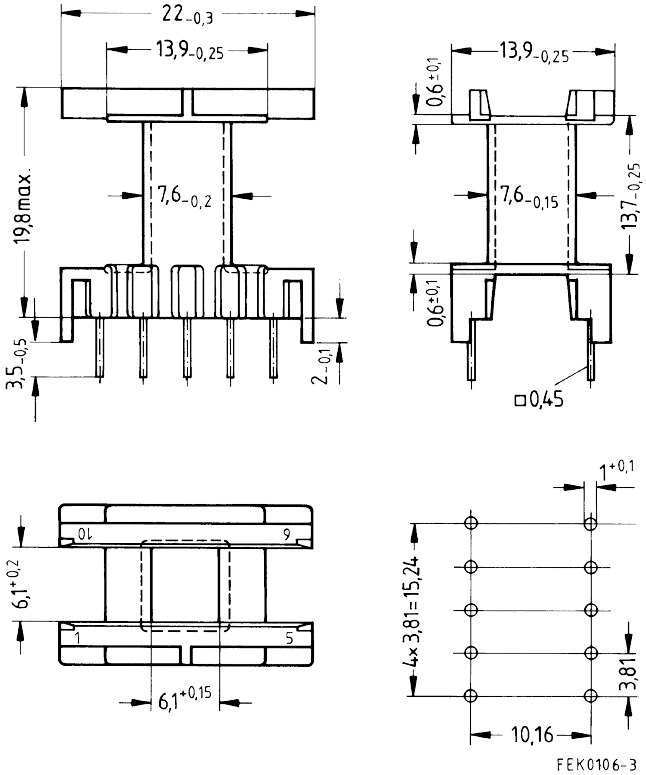
Version	Sections	A_N mm²	l_N mm	A_R value μΩ	Pins	Ordering code
Horizontal	1	34	41.2	42	10	B66206B1110T001
Vertical	1	34	41.2	42	10	B66206W1110T001

Horizontal version



Hole arrangement
View in mounting direction

Vertical version



Hole arrangement
View in mounting direction

Coil former (with right-angle pins)

Material: GFR polyterephthalate (UL 94 V-0, insulation class to IEC 60085: F ≙ max. operating temperature 155 °C), color code black Pocan B4235® [E245249 (M)], LANXESS AG

Solderability: to IEC 60068-2-20, test Ta, method 1 (aging 3): 235 °C, 2 s

Resistance to soldering heat: to IEC 60068-2-20, test Tb, method 1B: 350 °C, 3.5 s

Winding: see Processing notes, 2.1

Pins: Squared pins

Yoke

Material: Stainless spring steel (0.2 mm)

Coil former						Ordering code
Figure	Sections	A_N mm²	l_N mm	A_R value μΩ	Pins	
1	1	34	41.2	42	12	B66206C1012T001
2	1	34	41.2	42	14	B66206C1014T001
3	Yoke (ordering code per piece, 2 are required)					B66206A2010X000

Figure 1, coil former (12 pins)

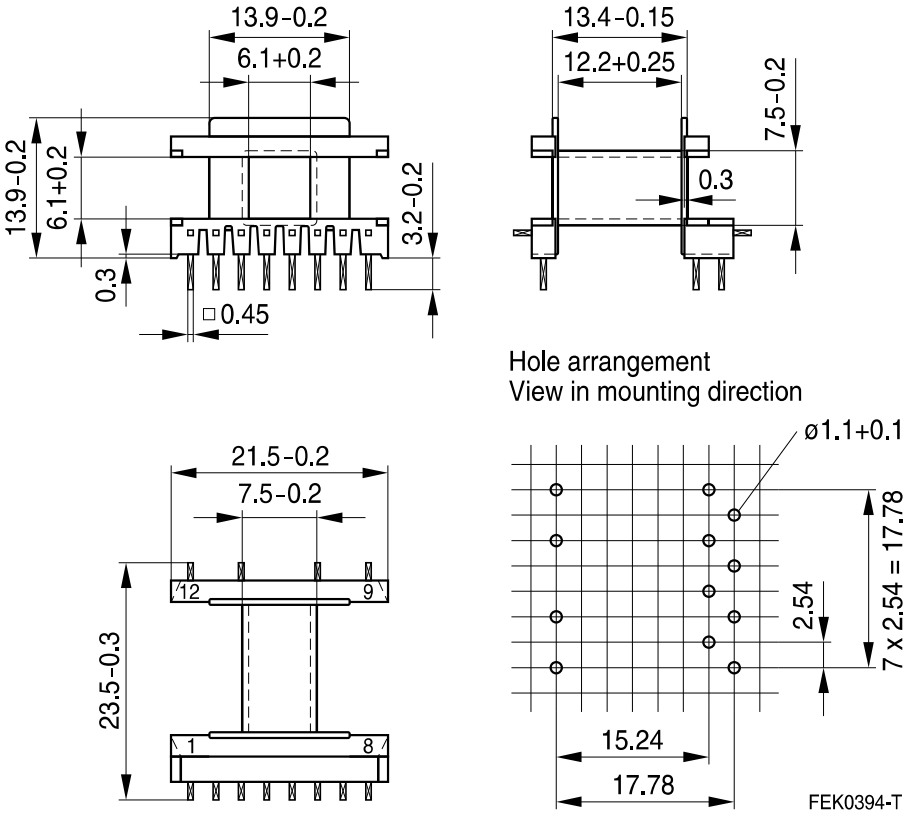


Figure 2, coil former (14 pins)

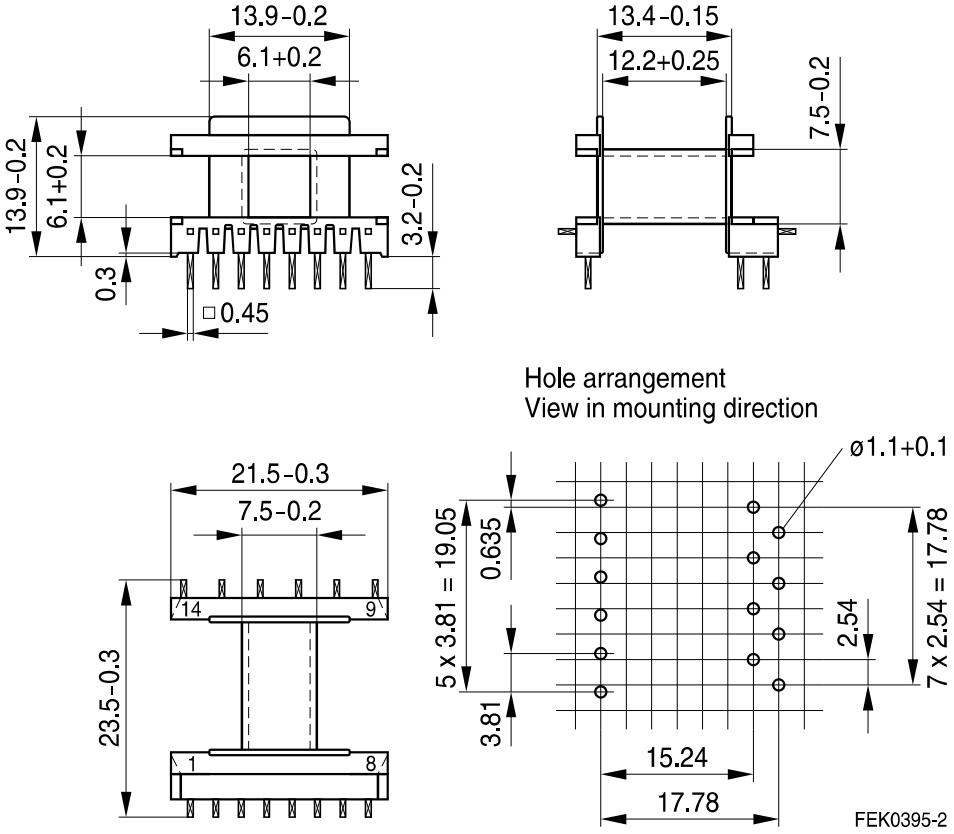
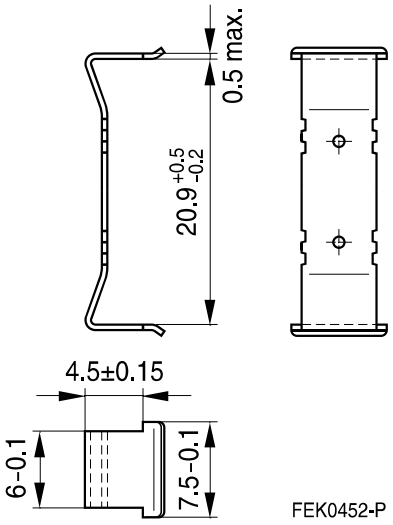


Figure 3, Yoke



Coil former for luminaires

■ Also to be used without clamps

Material: GFR polyterephthalate (UL 94 V-0, insulation class to IEC 60085: H ≙ max. operating temperature 180 °C), color code black Rynite FR 530® [E41938 (M)], E I DUPONT DE NEMOURS & CO INC

Solderability: to IEC 60068-2-20, test Ta, method 1 (aging 3): 235 °C, 2 s

Resistance to soldering heat: to IEC 60068-2-20, test Tb, method 1B: 350 °C, 3.5 s

Winding: see Processing notes, 2.1

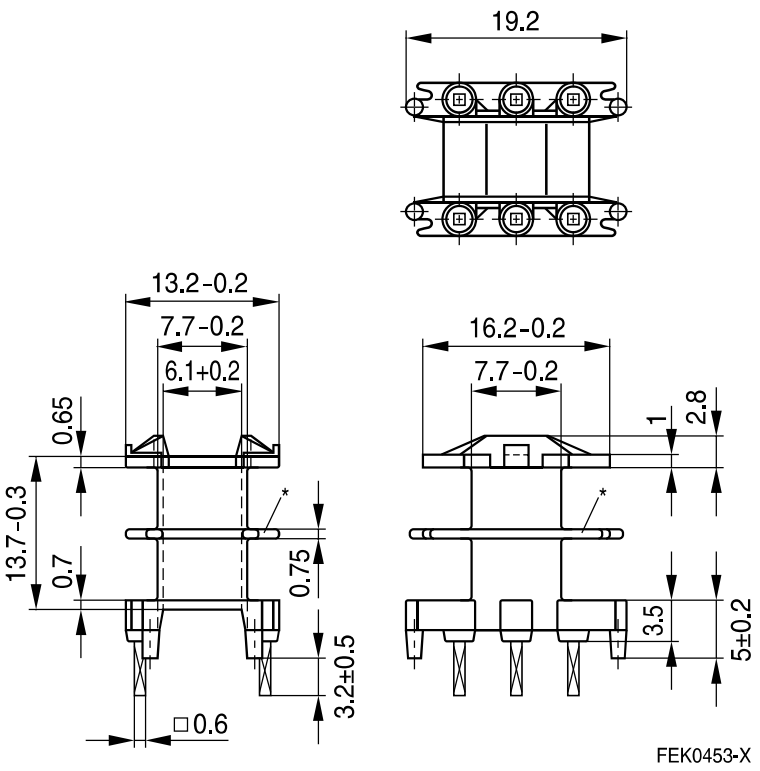
Pins: Squared pins

Yoke

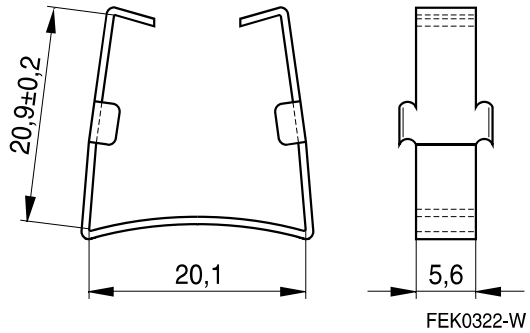
Material: Nickel silver (0.3 mm)

Sections	A_N mm²	l_N mm	A_R value μΩ	Pins	Ordering code
1	32.7	42.3	44.5	6	B66206J1106T001
2	30.7	42.3	34.4	6	B66206K1106T002
Yoke					B66206A2001X000

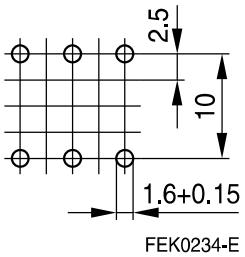
Coil former



Yoke



Hole arrangement
View in mounting direction



* Omitted for one-section version.

Mechanical stress and mounting

Ferrite cores have to meet mechanical requirements during assembling and for a growing number of applications. Since ferrites are ceramic materials one has to be aware of the special behavior under mechanical load.

As valid for any ceramic material, ferrite cores are brittle and sensitive to any shock, fast temperature changing or tensile load. Especially high cooling rates under ultrasonic cleaning and high static or cyclic loads can cause cracks or failure of the ferrite cores.

For detailed information see data book, chapter *"General - Definitions, 8.1"*.

Effects of core combination on A_L value

Stresses in the core affect not only the mechanical but also the magnetic properties. It is apparent that the initial permeability is dependent on the stress state of the core. The higher the stresses are in the core, the lower is the value for the initial permeability. Thus the embedding medium should have the greatest possible elasticity.

For detailed information see data book, chapter *"General - Definitions, 8.1"*.

Heating up

Ferrites can run hot during operation at higher flux densities and higher frequencies.

NiZn-materials

The magnetic properties of NiZn-materials can change irreversible in high magnetic fields.

Ferrite Accessories

EPCOS ferrite accessories have been designed and evaluated only in combination with EPCOS ferrite cores. EPCOS explicitly points out that EPCOS ferrite accessories or EPCOS ferrite cores may not be compatible with those of other manufacturers. Any such combination requires prior testing by the customer and will be at the customer‘s own risk.

EPCOS assumes no warranty or reliability for the combination of EPCOS ferrite accessories with cores and other accessories from any other manufacturer.

Processing remarks

The start of the winding process should be soft. Else the flanges may be destroyed.

- Too strong winding forces may blast the flanges or squeeze the tube that the cores can not be mounted any more.
- Too long soldering time at high temperature (>300 °C) may effect coplanarity or pin arrangement.
- Not following the processing notes for soldering of the J-leg terminals may cause solderability problems at the transformer because of pollution with Sn oxyde of the tin bath or burned insulation of the wire. For detailed information see chapter *"Processing notes"*, section 2.2.
- The dimensions of the hole arrangement have fixed values and should be understood as a recommendation for drilling the printed circuit board. For dimensioning the pins, the group of holes can only be seen under certain conditions, as they fit into the given hole arrangement. To avoid problems when mounting the transformer, the manufacturing tolerances for positioning the customers' drilling process must be considered by increasing the hole diameter.

Display of ordering codes for EPCOS products

The ordering code for one and the same product can be represented differently in data sheets, data books, other publications and the website of EPCOS, or in order-related documents such as shipping notes, order confirmations and product labels. **The varying representations of the ordering codes are due to different processes employed and do not affect the specifications of the respective products**. Detailed information can be found on the Internet under www.epcos.com/orderingcodes.

Symbols and terms

Symbol	Meaning	Unit
A	Cross section of coil	mm^2
A_e	Effective magnetic cross section	mm^2
A_L	Inductance factor; $A_L = L/N^2$	nH
A_{L1}	Minimum inductance at defined high saturation ($\triangleq \mu_a$)	nH
A_{min}	Minimum core cross section	mm^2
A_N	Winding cross section	mm^2
A_R	Resistance factor; $A_R = R_{Cu}/N^2$	$\mu\Omega = 10^{-6}\ \Omega$
B	RMS value of magnetic flux density	Vs/m^2, mT
ΔB	Flux density deviation	Vs/m^2, mT
$\hat{B}$	Peak value of magnetic flux density	Vs/m^2, mT
$\Delta\hat{B}$	Peak value of flux density deviation	Vs/m^2, mT
B_{DC}	DC magnetic flux density	Vs/m^2, mT
B_R	Remanent flux density	Vs/m^2, mT
B_S	Saturation magnetization	Vs/m^2, mT
C_0	Winding capacitance	F = As/V
CDF	Core distortion factor	$mm^{-4.5}$
DF	Relative disaccommodation coefficient $DF = d/\mu_i$	
d	Disaccommodation coefficient	
E_a	Activation energy	J
f	Frequency	s^{-1}, Hz
f_{cutoff}	Cut-off frequency	s^{-1}, Hz
f_{max}	Upper frequency limit	s^{-1}, Hz
f_{min}	Lower frequency limit	s^{-1}, Hz
f_r	Resonance frequency	s^{-1}, Hz
f_{Cu}	Copper filling factor	
g	Air gap	mm
H	RMS value of magnetic field strength	A/m
$\hat{H}$	Peak value of magnetic field strength	A/m
H_{DC}	DC field strength	A/m
H_c	Coercive field strength	A/m
h	Hysteresis coefficient of material	10^{-6} cm/A
h/μ_i^2	Relative hysteresis coefficient	10^{-6} cm/A
I	RMS value of current	A
I_{DC}	Direct current	A
$\hat{I}$	Peak value of current	A
J	Polarization	Vs/m^2
k	Boltzmann constant	J/K
k_3	Third harmonic distortion	
k_{3c}	Circuit third harmonic distortion	
L	Inductance	H = Vs/A

Symbols and terms

Symbol	Meaning	Unit
$\Delta L/L$	Relative inductance change	H
L_0	Inductance of coil without core	H
L_H	Main inductance	H
L_p	Parallel inductance	H
L_{rev}	Reversible inductance	H
L_s	Series inductance	H
l_e	Effective magnetic path length	mm
l_N	Average length of turn	mm
N	Number of turns	
P_{Cu}	Copper (winding) losses	W
P_{trans}	Transferrable power	W
P_V	Relative core losses	mW/g
PF	Performance factor	
Q	Quality factor ($Q = \omega L/R_s = 1/\tan \delta_L$)	
R	Resistance	Ω
R_{Cu}	Copper (winding) resistance (f = 0)	Ω
R_h	Hysteresis loss resistance of a core	Ω
ΔR_h	R_h change	Ω
R_i	Internal resistance	Ω
R_p	Parallel loss resistance of a core	Ω
R_s	Series loss resistance of a core	Ω
R_{th}	Thermal resistance	K/W
R_V	Effective loss resistance of a core	Ω
s	Total air gap	mm
T	Temperature	°C
ΔT	Temperature difference	K
T_C	Curie temperature	°C
t	Time	s
t_v	Pulse duty factor	
$\tan \delta$	Loss factor	
$\tan \delta_L$	Loss factor of coil	
$\tan \delta_r$	(Residual) loss factor at $H \rightarrow 0$	
$\tan \delta_e$	Relative loss factor	
$\tan \delta_h$	Hysteresis loss factor	
$\tan \delta/\mu_i$	Relative loss factor of material at $H \rightarrow 0$	
U	RMS value of voltage	V
Û	Peak value of voltage	V
V_e	Effective magnetic volume	mm^3
Z	Complex impedance	Ω
Z_n	Normalized impedance $\lvert Z\rvert_n = \lvert Z\rvert / N^2 \times \varepsilon\ (l_e/A_e)$	Ω/mm

Symbols and terms

Symbol	Meaning	Unit
α	Temperature coefficient (TK)	1/K
α_F	Relative temperature coefficient of material	1/K
α_e	Temperature coefficient of effective permeability	1/K
ε_r	Relative permittivity	
Φ	Magnetic flux	Vs
η	Efficiency of a transformer	
η_B	Hysteresis material constant	mT^{-1}
η_i	Hysteresis core constant	$A^{-1}H^{-1/2}$
λ_s	Magnetostriction at saturation magnetization	
μ	Relative complex permeability	
μ_0	Magnetic field constant	Vs/Am
μ_a	Relative amplitude permeability	
μ_{app}	Relative apparent permeability	
μ_e	Relative effective permeability	
μ_i	Relative initial permeability	
μ_p'	Relative real (inductive) component of $\bar{\mu}$ (for parallel components)	
μ_p''	Relative imaginary (loss) component of $\bar{\mu}$ (for parallel components)	
μ_r	Relative permeability	
μ_{rev}	Relative reversible permeability	
μ_s'	Relative real (inductive) component of $\bar{\mu}$ (for series components)	
μ_s''	Relative imaginary (loss) component of $\bar{\mu}$ (for series components)	
μ_{tot}	Relative total permeability derived from the static magnetization curve	
ρ	Resistivity	Ωm^{-1}
$\Sigma l/A$	Magnetic form factor	mm^{-1}
τ_{Cu}	DC time constant $\tau_{Cu} = L/R_{Cu} = A_L/A_R$	s
ω	Angular frequency; $\omega = 2\,\Pi f$	s^{-1}

All dimensions are given in mm.

SMD Surface-mount device

Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule we are either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether a product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet (www.tdk-electronics.tdk.com/material). Should you have any more detailed questions, please contact our sales offices.
5. We constantly strive to improve our products. Consequently, **the products described in this publication may change from time to time**. The same is true of the corresponding product specifications. Please check therefore to what extent product descriptions and specifications contained in this publication are still applicable before or when you place an order.

   We also **reserve the right to discontinue production and delivery of products**. Consequently, we cannot guarantee that all products named in this publication will always be available. The aforementioned does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.
6. Unless otherwise agreed in individual contracts, **all orders are subject to our General Terms and Conditions of Supply.**
7. **Our manufacturing sites serving the automotive business apply the IATF 16949 standard.** The IATF certifications confirm our compliance with requirements regarding the quality management system in the automotive industry. Referring to customer requirements and customer specific requirements ("CSR") TDK always has and will continue to have the policy of respecting individual agreements. Even if IATF 16949 may appear to support the acceptance of unilateral requirements, we hereby like to emphasize that **only requirements mutually agreed upon can and will be implemented in our Quality Management System.** For clarification purposes we like to point out that obligations from IATF 16949 shall only become legally binding if individually agreed upon.
8. The trade names EPCOS, CeraCharge, CeraDiode, CeraLink, CeraPad, CeraPlas, CSMP, CTVS, DeltaCap, DigiSiMic, ExoCore, FilterCap, FormFit, LeaXield, MiniBlue, MiniCell, MKD, MKK, MotorCap, PCC, PhaseCap, PhaseCube, PhaseMod, PhiCap, PowerHap, PQSine, PQvar, SIFERRIT, SIFI, SIKOREL, SilverCap, SIMDAD, SiMic, SIMID, SineFormer, SIOV, ThermoFuse, WindCap are **trademarks registered or pending** in Europe and in other countries. Further information will be found on the Internet at www.tdk-electronics.tdk.com/trademarks.

Release 2018-10

MCP73833/4

Stand-Alone Linear Li-Ion / Li-Polymer Charge Management Controller

Features

- Complete Linear Charge Management Controller
  - Integrated Pass Transistor
  - Integrated Current Sense
  - Integrated Reverse Discharge Protection
- Constant Current / Constant Voltage Operation with Thermal Regulation
- High Accuracy Preset Voltage Regulation:
  - 4.2V, 4.35V, 4.4V, or 4.5V, ± 0.75%
- Programmable Charge Current: 1A Maximum
- Preconditioning of Deeply Depleted Cells
  - Selectable Current Ratio
  - Selectable Voltage Threshold
- Automatic End-of-Charge Control
  - Selectable Current Threshold
  - Selectable Safety Time Period
- Automatic Recharge
  - Selectable Voltage Threshold
- Two Charge Status Outputs
- Cell Temperature Monitor
- Low-Dropout Linear Regulator Mode
- Automatic Power-Down when Input Power Removed
- Under Voltage Lockout
- Numerous Selectable Options Available for a Variety of Applications:
  - Refer to **Section 1.0 "Electrical Characteristics"** for Selectable Options
  - Refer to the Product Identification System for Standard Options
- Available Packages:
  - DFN-10 (3 mm x 3 mm)
  - MSOP-10

Applications

- Lithium-Ion / Lithium-Polymer Battery Chargers
- Personal Data Assistants
- Cellular Telephones
- Digital Cameras
- MP3 Players
- Bluetooth Headsets
- USB Chargers

Description

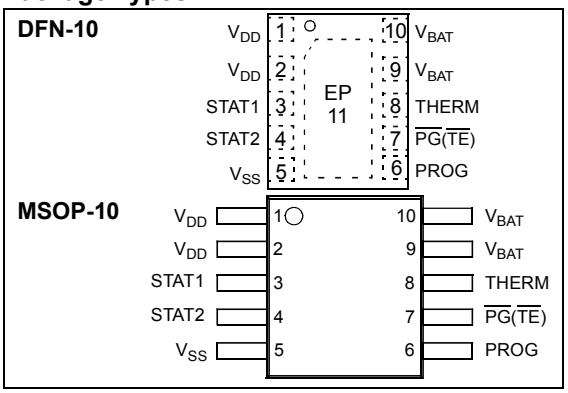
The MCP73833/4 is a highly advanced linear charge management controller for use in space-limited, cost sensitive applications. The MCP73833/4 is available in a 10-Lead, 3 mm x 3 mm DFN package or a 10-Lead, MSOP package. Along with its small physical size, the low number of external components required makes the MCP73833/4 ideally suited for portable applications. For applications charging from a USB port, the MCP73833/4 can adhere to all the specifications governing the USB power bus.

The MCP73833/4 employs a constant current/constant voltage charge algorithm with selectable preconditioning and charge termination. The constant voltage regulation is fixed with four available options: 4.20V, 4.35V, 4.40V, or 4.50V, to accomodate new, emerging battery charging requirements. The constant current value is set with one external resistor. The MCP73833/4 limits the charge current based on die temperature during high power or high ambient conditions. This thermal regulation optimizes the charge cycle time while maintaining device reliability.

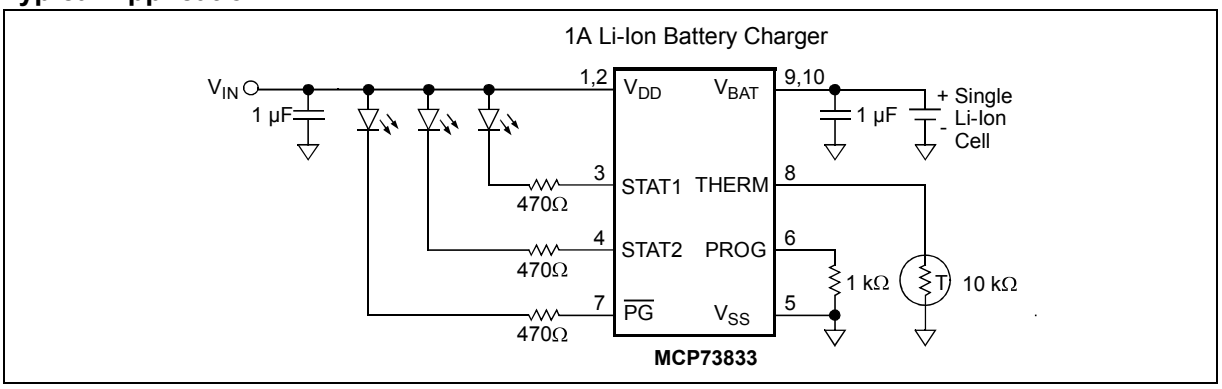
Several options are available for the preconditioning threshold, preconditioning current value, charge termination value, and automatic recharge threshold. The preconditioning value and charge termination value are set as a ratio, or percentage, of the programmed constant current value. Preconditioning can be set to 100%. Refer to **Section 1.0 "Electrical Characteristics"** for available options and the **"Product Indentification System"** for standard options.

The MCP73833/4 is fully specified over the ambient temperature range of -40°C to +85°C.

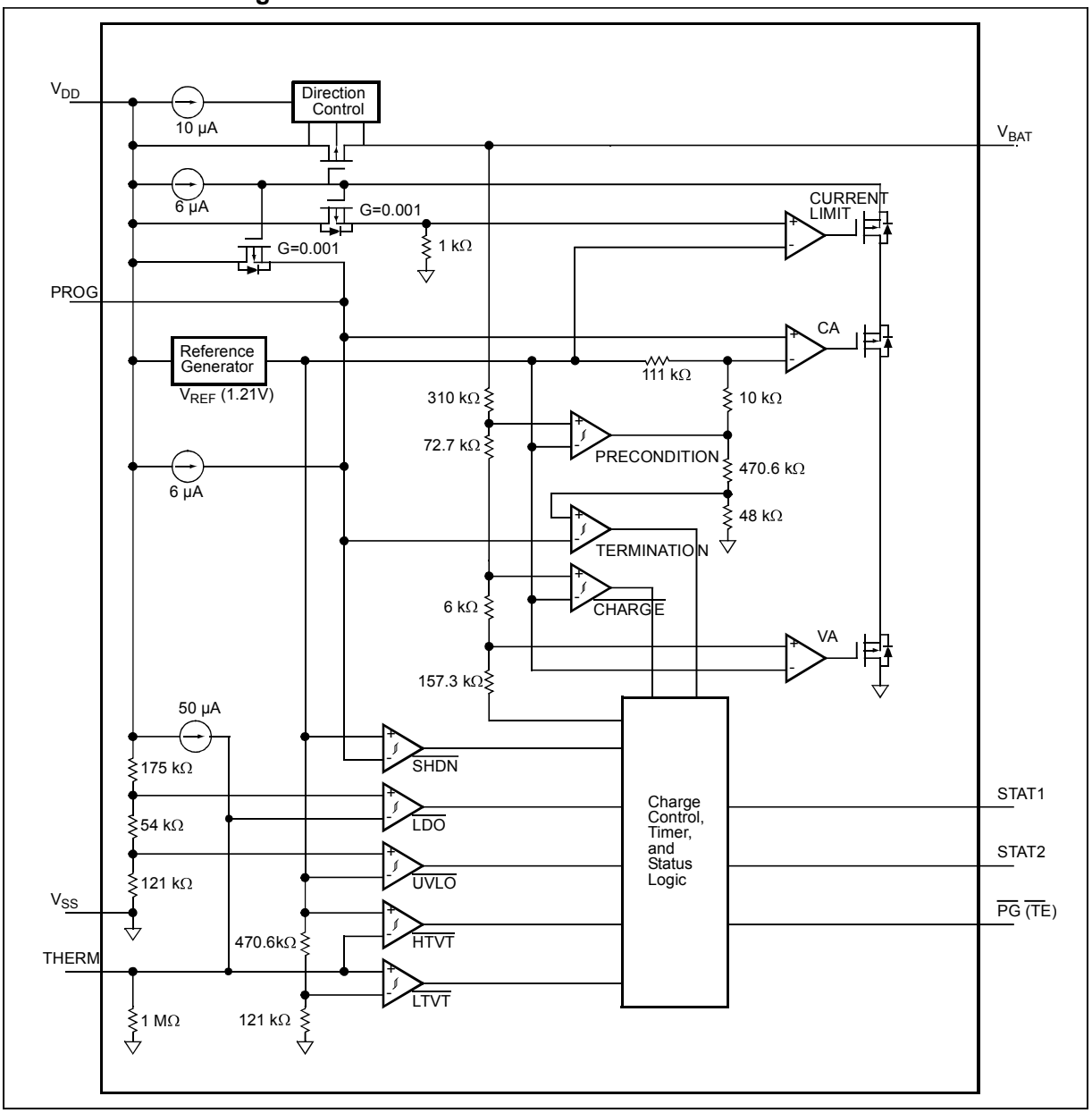
Package Types



Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{DD}.....7.0V

All Inputs and Outputs w.r.t. V_{SS} .....-0.3 to (V_{DD}+0.3)V

Maximum Junction Temperature, T_J . Internally Limited

Storage temperature ..... -65°C to +150°C

ESD protection on all pins:

Human Body Model (HBM)
(1.5 kΩ in Series with 100 pF)..... ≥ 4 kV

Machine Model (MM)
(200 pF, No Series Resistance) 300V

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Input						
Supply Voltage	V_{DD}	3.75	—	6	V	Charging
		V_{REG}(Typical)+0.3V	—	6	V	Charge Complete, Standby
Supply Current	I_{SS}	—	2000	3000	µA	Charging
		—	150	300	µA	Charge Complete
		—	100	300	µA	Standby (No Battery or PROG Floating)
		—	50	100	µA	Shutdown ($V_{DD} \le V_{BAT}$, or $V_{DD} < V_{STOP}$)
UVLO Start Threshold	V_{START}	3.4	3.55	3.7	V	V_{DD} Low-to-High
UVLO Stop Threshold	V_{STOP}	3.3	3.45	3.6	V	V_{DD} High-to-Low
UVLO Hysteresis	V_{HYS}	—	100	—	mV	
Voltage Regulation (Constant Voltage Mode, System Test Mode)						
Regulated Output Voltage	V_{REG}	4.168	4.20	4.232	V	V_{DD}=[V_{REG}(Typical)+1V]
		4.318	4.35	4.382	V	I_{OUT}=10 mA
		4.367	4.40	4.433	V	T_A=-5°C to +55°C
		4.467	4.50	4.533	V	
Line Regulation	$\lvert(\Delta V_{BAT}/V_{BAT})/\Delta V_{DD}\rvert$	—	0.10	0.30	%/V	V_{DD}=[V_{REG}(Typical)+1V] to 6V, I_{OUT}=10 mA
Load Regulation	$\lvert\Delta V_{BAT}/ V_{BAT}\rvert$	—	0.10	0.30	%	I_{OUT}=10 mA to 100 mA V_{DD}=[V_{REG}(Typical)+1V]
Supply Ripple Attenuation	PSRR	—	58	—	dB	I_{OUT}=10 mA, 10Hz to 1 kHz
		—	47	—	dB	I_{OUT}=10 mA, 10Hz to 10 kHz
		—	25	—	dB	I_{OUT}=10 mA, 10Hz to 1 MHz
Current Regulation (Fast Charge Constant Current Mode)						
Fast Charge Current Regulation	I_{REG}	90	100	110	mA	PROG = 10 kΩ
		900	1000	1100	mA	PROG = 1.0 kΩ
						T_A=-5°C to +55°C
Maximum Output Current Limit	I_{MAX}	—	1200	—	mA	PROG < 833Ω

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
Preconditioning Current Regulation (Trickle Charge Constant Current Mode)						
Precondition Current Ratio	I_{PREG} / I_{REG}	7.5	10	12.5	%	PROG = 1.0 kΩ to 10 kΩ
		15	20	25	%	T_A=-5°C to +55°C
		30	40	50	%	
		—	100	—	%	
Precondition Voltage Threshold Ratio	V_{PTH} / V_{REG}	64	66.5	70	%	V_{BAT} Low-to-High
		69	71.5	75	%	
Precondition Hysteresis	V_{PHYS}	—	100	—	mV	V_{BAT} High-to-Low
Charge Termination						
Charge Termination Current Ratio	I_{TERM} / I_{REG}	3.75	5	6.25	%	PROG = 1.0 kΩ to 10 kΩ
		5.6	7.5	9.4	%	T_A=-5°C to +55°C
		7.5	10	12.5	%	
		15	20	25	%	
Automatic Recharge						
Recharge Voltage Threshold Ratio	V_{RTH} / V_{REG}	—	94.0	—	%	V_{BAT} High-to-Low
		—	96.5	—	%	
Pass Transistor ON-Resistance						
ON-Resistance	R_{DSON}	—	300	—	mΩ	V_{DD} = 3.75V T_J = 105°C
Battery Discharge Current						
Output Reverse Leakage Current	$I_{DISCHARGE}$	—	0.15	2	µA	PROG Floating
		—	0.25	2	µA	$V_{DD} \leq V_{BAT}$
		—	0.15	2	µA	$V_{DD} < V_{STOP}$
		—	-5.5	-15	µA	Charge Complete
Status Indicators - STAT1, STAT2, $\overline{PG}$						
Sink Current	I_{SINK}	—	15	25	mA	
Low Output Voltage	V_{OL}	—	0.4	1	V	I_{SINK} = 4 mA
Input Leakage Current	I_{LK}	—	0.01	1	µA	High Impedance, 6V on pin
PROG Input						
Charge Impedance Range	R_{PROG}	1	—	20	kΩ	
Standy Impedance	R_{PROG}	70	—	200	kΩ	Minimum Impedance for Standby
Thermistor Bias						
Thermistor Current Source	I_{THERM}	47	50	53	µA	2 kΩ < R_{THERM} < 50 kΩ
Thermistor Comparator						
Upper Trip Threshold	V_{T1}	1.20	1.23	1.26	V	V_{THERM} Low-to-High
Upper Trip Point Hysteresis	V_{T1HYS}	—	-50	—	mV	
Lower Trip Threshold	V_{T2}	0.235	0.25	0.265	V	V_{THERM} High-to-Low
Lower Trip Point Hysteresis	V_{T2HYS}	—	50	—	mV	
System Test (LDO) Mode						
Input High Voltage Level	V_{IH}	(V_{DD}-0.1)	—	—	V	
THERM Input Sink Current	I_{SINK}	3	6	20	µA	Stand-by or system test mode
Bypass Capacitance	C_{BAT}	1	—	—	µF	I_{OUT} < 250 mA
		4.7	—	—	µF	I_{OUT} > 250 mA

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
Automatic Power Down						
Automatic Power Down Entry Threshold	V_{PD}	—	V_{BAT} + 50 mV	—	V	2.3V ≤ V_{BAT} ≤ V_{REG} V_{DD} Falling
Automatic Power Down Exit Threshold	V_{PDEXIT}	—	V_{BAT} + 150 mV	—	V	2.3V ≤ V_{BAT} ≤ V_{REG} V_{DD} Rising
Timer Enable Input ($\overline{TE}$)						
Input High Voltage Level	V_{IH}	2.0	—	—	V	
Input Low Voltage Level	V_{IL}	—	—	0.6	V	
Input Leakage Current	I_{LK}	—	0.01	1	µA	V_{TE} = 6V
Thermal Shutdown						
Die Temperature	T_{SD}	—	150	—	°C	
Die Temperature Hysteresis	T_{SDHYS}	—	10	—	°C	

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
UVLO Start Delay	t_{START}	—	—	5	ms	V_{DD} Low-to-High
Current Regulation						
Transition Time Out of Preconditioning	t_{DELAY}	—	—	1	ms	V_{BAT}<V_{PTH} to V_{BAT}>V_{PTH}
Current Rise Time Out of Preconditioning	t_{RISE}	—	—	1	ms	I_{OUT} Rising to 90% of I_{REG}
Preconditioning Comparator Filter Time	t_{PRECON}	0.4	1.3	3.2	ms	Average V_{BAT} Rise/Fall
Termination Comparator Filter Time	t_{TERM}	0.4	1.3	3.2	ms	Average I_{OUT} Falling
$\overline{\text{Charge}}$ Comparator Filter Time	t_{CHARGE}	0.4	1.3	3.2	ms	Average V_{BAT} Falling
Thermistor Comparator Filter Time	t_{THERM}	0.4	1.3	3.2	ms	Average THERM Rise/Fall
Elapsed Timer						
Elapsed Timer Period	$t_{ELAPSED}$	0	0	0	Hours	Timer Disabled
		3.6	4.0	4.4	Hours	
		5.4	6.0	6.6	Hours	
		7.2	8.0	8.8	Hours	
Status Indicators						
Status Output turn-off	t_{OFF}	—	—	200	µs	I_{SINK} = 1 mA to 0 mA
Status Output turn-on	t_{ON}	—	—	200	µs	I_{SINK} = 0 mA to 1 mA

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, MSOP-10	θ_{JA}	—	113	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection
Thermal Resistance, DFN-10, 3 mm x 3 mm	θ_{JA}	—	41	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 5.2V, V_{REG} = 4.20V, I_{OUT} = 10 mA and T_A= +25°C, Constant-voltage mode.

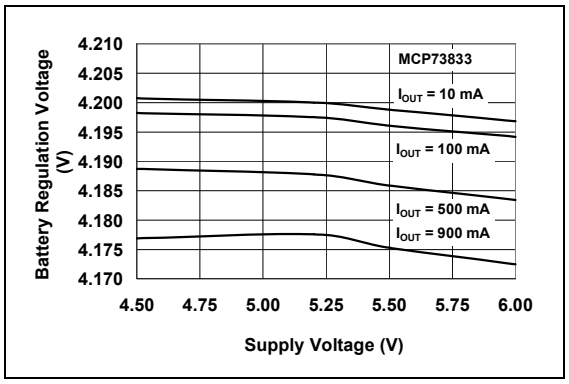


FIGURE 2-1: *Battery Regulation Voltage (V_{BAT}) vs. Supply Voltage (V_{DD}).*

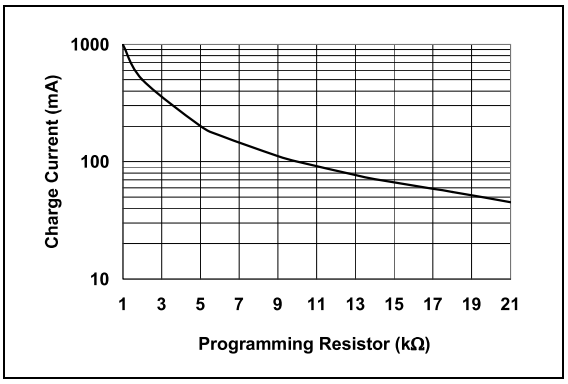


FIGURE 2-4: *Charge Current (I_{OUT}) vs. Programming Resistor (R_{PROG}).*

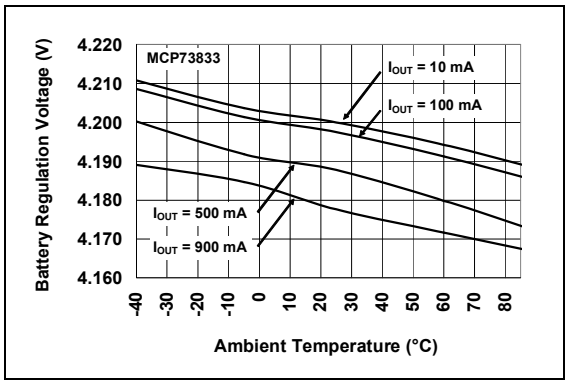


FIGURE 2-2: *Battery Regulation Voltage (V_{BAT}) vs. Ambient Temperature (T_A).*

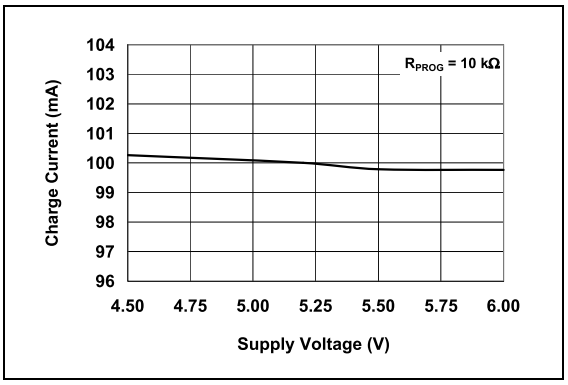


FIGURE 2-5: *Charge Current (I_{OUT}) vs. Supply Voltage (V_{DD}).*

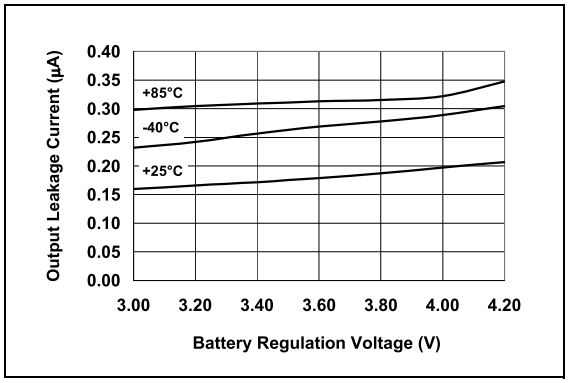


FIGURE 2-3: *Output Leakage Current ($I_{DISCHARGE}$) vs. Battery Regulation Voltage (V_{BAT}).*

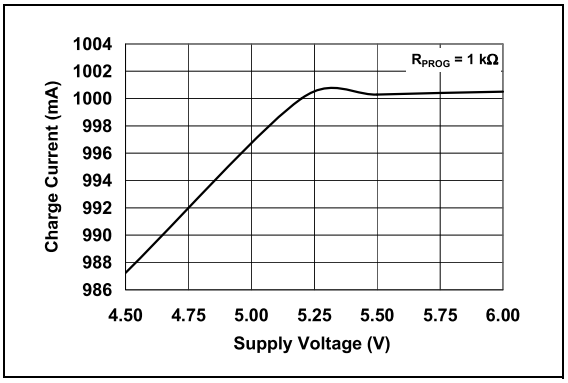


FIGURE 2-6: *Charge Current (I_{OUT}) vs. Supply Voltage (V_{DD}).*

TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, V_{DD} = 5.2V, V_{REG} = 4.20V, I_{OUT} = 10 mA and T_A= +25°C, Constant-voltage mode.

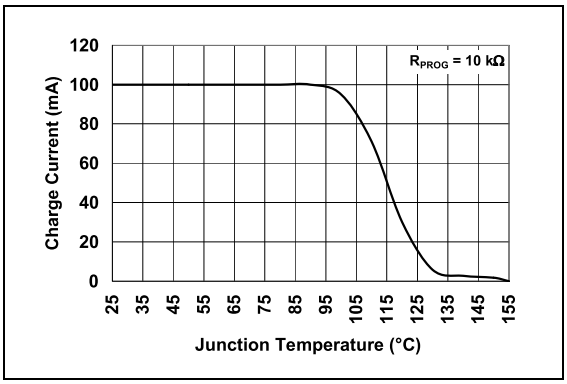


FIGURE 2-7: *Charge Current (I_{OUT}) vs. Junction Temperature (T_J).*

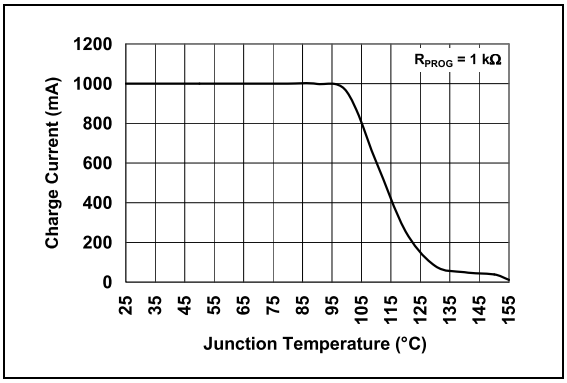


FIGURE 2-8: *Charge Current (I_{OUT}) vs. Junction Temperature (T_J).*

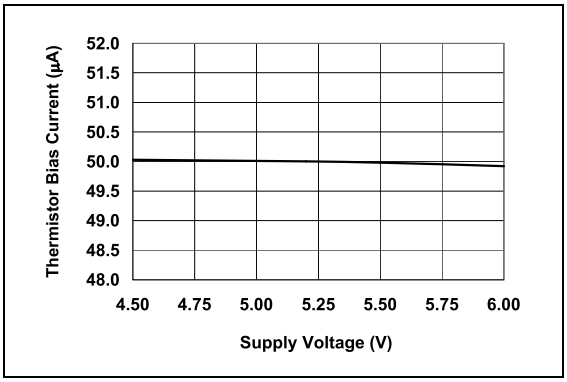


FIGURE 2-9: *Thermistor Bias Current (I_{THRERM}) vs. Supply Voltage (V_{DD}).*

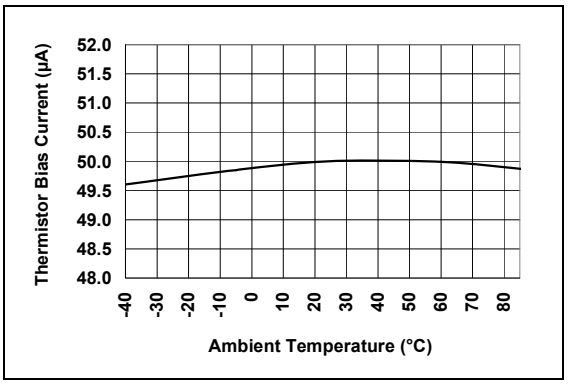


FIGURE 2-10: *Thermistor Bias Current (I_{THRERM}) vs. Ambient Temperature (T_A).*

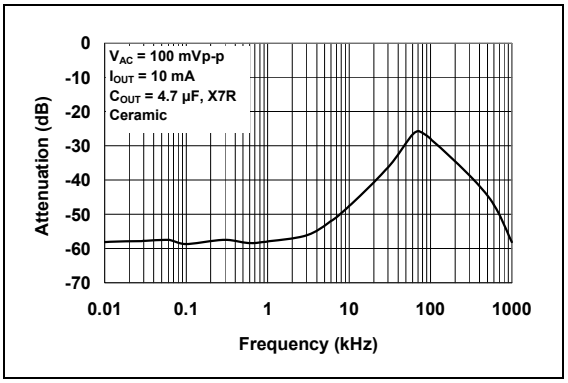


FIGURE 2-11: *Power Supply Ripple Rejection (PSRR).*

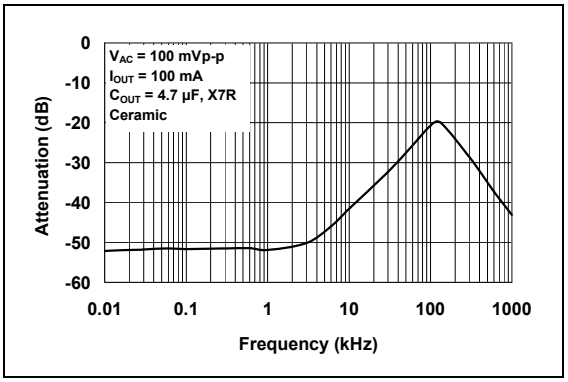


FIGURE 2-12: *Power Supply Ripple Rejection (PSRR).*

TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, V_{DD} = 5.2V, V_{REG} = 4.20V, I_{OUT} = 10 mA and T_A= +25°C, Constant-voltage mode.

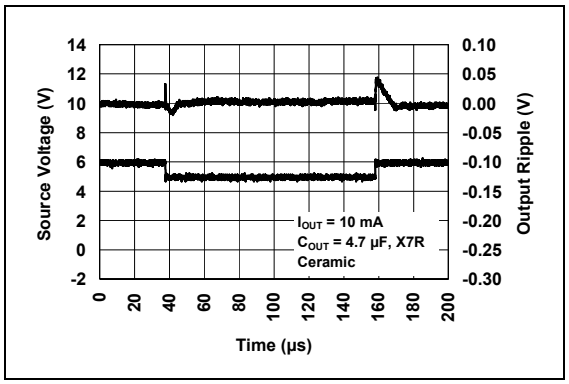


FIGURE 2-13: *Line Transient Response.*

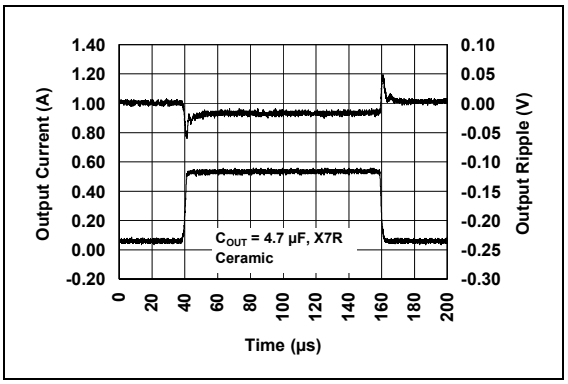


FIGURE 2-16: *Load Transient Response.*

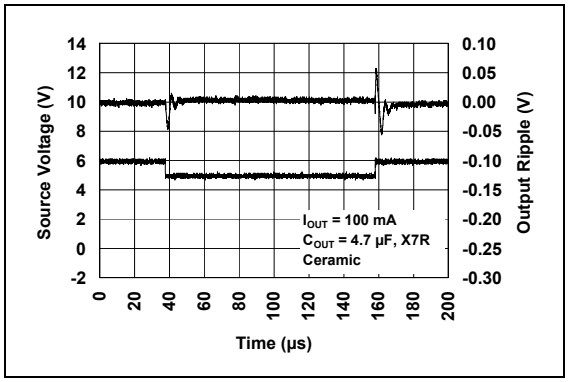


FIGURE 2-14: *Line Transient Response.*

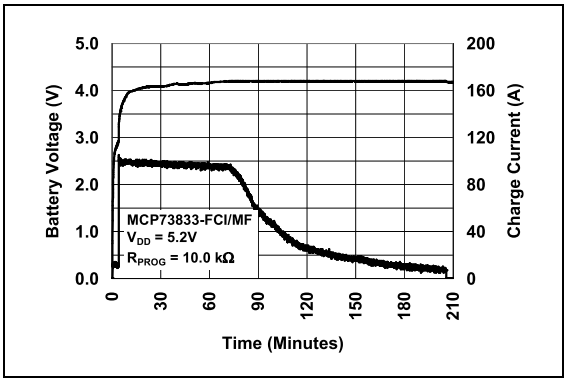


FIGURE 2-17: *Complete Charge Cycle (180 mA Li-Ion Battery).*

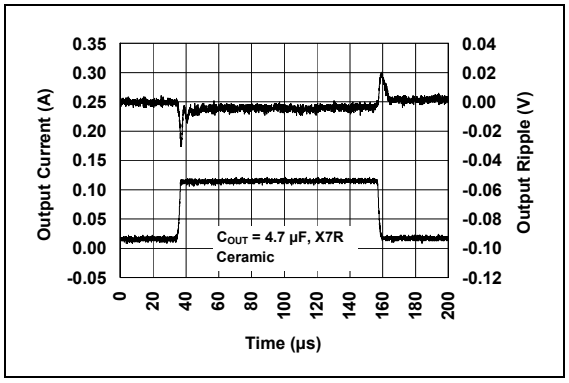


FIGURE 2-15: *Load Transient Response.*

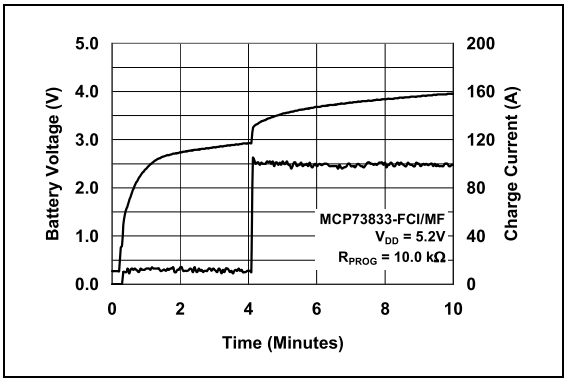


FIGURE 2-18: *Charge Cycle Start - Preconditioning (180 mAh Li-Ion Battery).*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.		Symbol	Function
DFN-10	MSOP-10		
1	1	V_{DD}	Battery Management Input Supply
2	2	V_{DD}	Battery Management Input Supply
3	3	STAT1	Charge Status Output
4	4	STAT2	Charge Status Output
5	5	V_{SS}	Battery Management 0V Reference
6	6	PROG	Current Regulation Set and Charge Control Enable
7	7	$\overline{PG}$, $\overline{TE}$	**MCP73833:** Power Good output, **MCP73834**: Timer Enable input
8	8	THERM	Thermistor input
9	9	V_{BAT}	Battery Charge Control Output
10	10	V_{BAT}	Battery Charge Control Output
11	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

3.1 Battery Management Input Supply (V_{DD})

A supply voltage of [V_{REG} (typical) + 0.3V] to 6V is recommended. Bypass to V_{SS} with a minimum of 1 µF.

3.2 Charge Status Outputs (STAT1, STAT2)

STAT1 and STAT2 are open-drain logic outputs for connection to a LED for charge status indication. Alternatively, a pull-up resistor can be applied for interfacing to a host microcontroller.

3.3 Battery Management 0V Reference (V_{SS})

Connect to negative terminal of battery and input supply.

3.4 Current Regulation Set (PROG)

Preconditioning, fast charge, and termination currents are scaled by placing a resistor from PROG to V_{SS}.

The charge management controller can be disabled by allowing the PROG input to float.

3.5 Power Good Indication ($\overline{PG}$) MCP73833 Only

The power good ($\overline{PG}$) option is a pseudo open-drain output. The $\overline{PG}$ output can sink current, but not source current. However, there is a diode path back to the input, and, as such, the $\overline{PG}$ output should only be pulled up to the input. The $\overline{PG}$ output is low whenever the input to the MCP73833 is above the UVLO threshold and greater than the battery voltage.

3.6 Timer Enable Input ($\overline{TE}$) MCP73834 Only

The timer enable ($\overline{TE}$) input option is used to enable or disable the internal timer. A low signal on this pin enables the internal timer and a high signal disables the internal timer. The $\overline{TE}$ input can be used to disable the timer when the charger is supplying current to charge the battery and power the system load. The $\overline{TE}$ input is compatible with 1.8V logic.

3.7 Thermistor Input (THERM)

An internal 50 µA current source provides the bias for most common 10 kΩ negative-temperature coefficient thermistors (NTC). The MCP73833/4 compares the voltage at the THERM pin to factory set thersholds of 1.20V and 0.25V, typically.

3.8 Battery Charge Control Output (V_{BAT})

Connect to positive terminal of battery. Drain terminal of internal P-channel MOSFET pass transistor. Bypass to V_{SS} with a minimum of 1 µF to ensure loop stability when the battery is disconnected.

3.9 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential.

NOTES:

4.0 FUNCTIONAL DESCRIPTION

The MCP73833/4 is a highly advanced linear charge management controller. Refer to the functional block diagram and Figure 4-1 that depicts the operational flow algorithm from charge initiation to completion and automatic recharge.

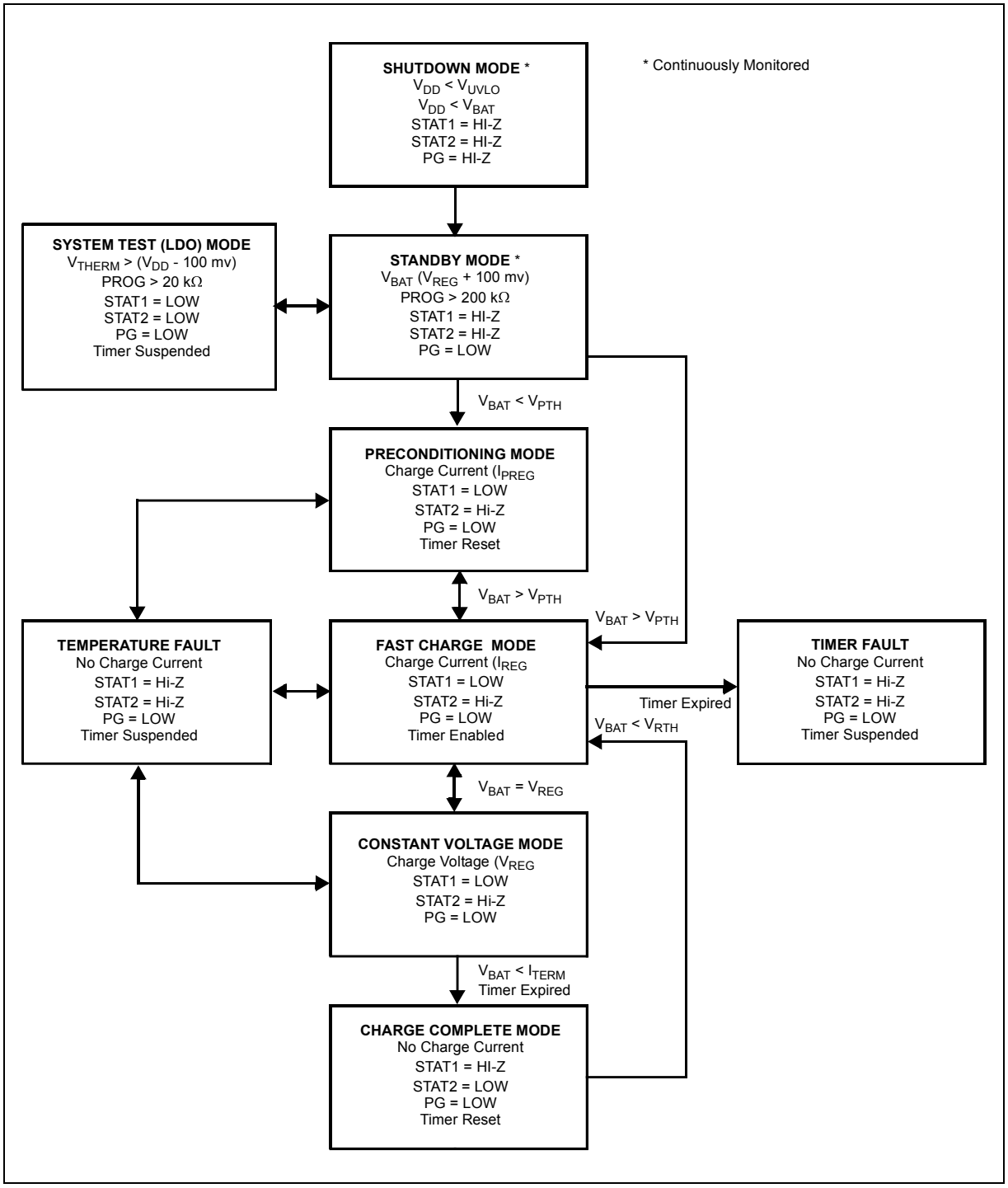


FIGURE 4-1: *Flow Chart.*

4.1 Under Voltage Lockout (UVLO)

An internal under voltage lockout (UVLO) circuit monitors the input voltage and keeps the charger in shutdown mode until the input supply rises above the UVLO threshold. The UVLO circuitry has a built-in hysteresis of 100 mV.

In the event a battery is present when the input power is applied, the input supply must rise +150 mV above the battery voltage before the MCP73833/4 becomes operational.

The UVLO circuit places the device in shutdown mode if the input supply falls to within +50 mV of the battery voltage.

The UVLO circuit is always active. At any time the input supply is below the UVLO threshold or within +50 mV of the voltage at the V_{BAT} pin, the MCP73833/4 is placed in a shutdown mode.

During any UVLO condition, the battery reverse discharge current shall be less than 2 µA.

4.2 Charge Qualification

For a charge cycle to begin, all UVLO conditions must be met and a battery or output load must be present.

A charge current programming resistor must be connected from PROG to V_{SS}. If the PROG pin is open or floating, the MCP73833/4 is disabled and the battery reverse discharge current is less than 2 µA. In this manner, the PROG pin acts as a charge enable and can be used as a manual shutdown.

If the input supply voltage is above the UVLO threshold, but below V_{REG}(Typical)+0.3V, the MCP73833/4 will pulse the STAT1 and PG outputs as the device determines if a battery is present.

4.3 Preconditioning

If the voltage at the V_{BAT} pin is less than the preconditioning threshold, the MCP73833/4 enters a preconditioning or trickle charge mode. The preconditioning threshold is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for preconditioning threshold options.

In this mode, the MCP73833/4 supplies a percentage of the charge current (established with the value of the resistor connected to the PROG pin) to the battery. The percentage or ratio of the current is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for preconditioning current options.

When the voltage at the V_{BAT} pin rises above the pre-conditioning threshold, the MCP73833/4 enters the constant current or fast charge mode.

4.4 Constant Current - Fast Charge Mode

During the constant current mode, the programmed charge current is supplied to the battery or load. The charge current is established using a single resistor from PROG to V_{SS}. The program resistor and the charge current are calculated using Equation 4-1:

EQUATION 4-1:

$$I_{REG} = \frac{1000V}{R_{PROG}}$$

Where:

R_{PROG} = kilo-ohms

I_{REG} = milliampere

Constant current mode is maintained until the voltage at the V_{BAT} pin reaches the regulation voltage, V_{REG}.

When constant current mode is invoked, the internal timer is reset.

4.4.1 TIMER EXPIRED DURING CONSTANT CURRENT - FAST CHARGE MODE

If the internal timer expires before the recharge voltage threshold is reached, a timer fault is indicated and the charge cycle terminates. The MCP73833/4 remains in this condition until the battery is removed, the input power is removed, or the PROG pin is opened. If the battery is removed or the PROG pin is opened, the MCP73833/4 enters the Standby mode where it remains until a battery is reinserted or the PROG pin is reconnected. If the input power is removed, the MCP73833/4 is in Shutdown. When the input power is reapplied, a normal start-up sequence ensues.

4.5 Constant Voltage Mode

When the voltage at the V_{BAT} pin reaches the regulation voltage, V_{REG}, constant voltage regulation begins. The regulation voltage is factory set to 4.20V, 4.35V, 4.40V, or 4.50V with a tolerance of ± 0.75%.

4.6 Charge Termination

The charge cycle is terminated when, during constant voltage mode, the average charge current diminishes below a percentage of the programmed charge current (established with the value of the resistor connected to the PROG pin) or the internal timer has expired. A 1 ms filter time on the termination comparator ensures that transient load conditions do not result in premature charge cycle termination. The percentage or ratio of the current is factory set. The timer period is factory set and can be disabled. Refer to **Section 1.0 "Electrical Characteristics"** for charge termination current ratio and timer period options.

The charge current is latched off and the MCP73833/4 enters a charge complete mode.

4.7 Automatic Recharge

The MCP73833/4 continuously monitors the voltage at the V_{BAT} pin in the charge complete mode. If the voltage drops below the recharge threshold, another charge cycle begins and current is once again supplied to the battery or load. The recharge threshold is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for recharge threshold options.

4.8 Thermal Regulation

The MCP73833/4 limits the charge current based on the die temperature. The thermal regulation optimizes the charge cycle time while maintaining device reliability. Figure 4-2 depicts the thermal regulation for the MCP73833/4.

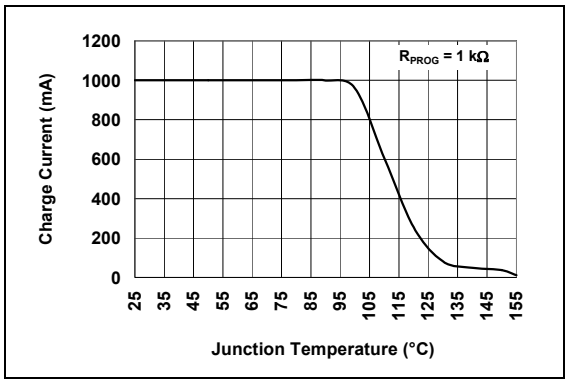


FIGURE 4-2: *Thermal Regulation.*

4.9 Thermal Shutdown

The MCP73833/4 suspends charge if the die temperature exceeds +150°C. Charging will resume when the die temperature has cooled by approximately +10°C. The thermal shutdown is a secondary safety feature in the event that there is a failure within the thermal regulation circuitry.

NOTES:

5.0 DETAILED DESCRIPTION

5.1 Analog Circuitry

5.1.1 BATTERY MANAGEMENT INPUT SUPPLY (V_{DD})

The V_{DD} input is the input supply to the MCP73833/4. The MCP73833/4 automatically enters a Power-down mode if the voltage on the V_{DD} input falls below the UVLO voltage (V_{STOP}). This feature prevents draining the battery pack when the V_{DD} supply is not present.

5.1.2 CURRENT REGULATION SET (PROG)

Fast charge current regulation can be scaled by placing a programming resistor (R_{PROG}) from the PROG input to V_{SS}. The program resistor and the charge current are calculated using the Equation 5-1:

EQUATION 5-1:

$$I_{REG} = \frac{1000V}{R_{PROG}}$$

Where:

R_{PROG} = kilo-ohms

I_{REG} = milliampere

The preconditioning trickle-charge current and the charge termination current are ratiometric to the fast charge current based on the selected device options.

5.1.3 BATTERY CHARGE CONTROL OUTPUT (V_{BAT})

The battery charge control output is the drain terminal of an internal P-channel MOSFET. The MCP73833/4 provides constant current and voltage regulation to the battery pack by controlling this MOSFET in the linear region. The battery charge control output should be connected to the positive terminal of the battery pack.

5.1.4 TEMPERATURE QUALIFICATION (THERM)

The MCP73833/4 continuously monitors battery temperature during a charge cycle by measuring the voltage between the THERM and V_{SS} pins. An internal 50 µA current source provides the bias for most common 10 kΩ negative-temperature coefficient (NTC) or positive-temperature coefficient (PTC) thermistors.The current source is controlled, avoiding measurement sensitivity to fluctuations in the supply voltage (V_{DD}). The MCP73833/4 compares the voltage at the THERM pin to factory set thersholds of 1.20V and 0.25V, typically. Once a volage outside the thresholds is detected during a charge cycle, the MCP73833/4 immediately suspends the charge cycle. The MCP73833/4 suspends charge by turning off the pass transistor and holding the timer value. The charge cycle resumes when the voltage at the THERM pin returns to the normal range.

If temperature monitoring is not required, place a standard 10 kΩ resistor from THERM to V_{SS}.

5.1.4.1 System Test (LDO) Mode

The MCP73833/4 can be placed in a system test mode. In this mode, the MCP73833/4 operates as a low dropout linear regulator (LDO). The output voltage is regulated to the factory set voltage regulation option. The available output current is limitted to the programmed fast charge current. For stability, the V_{BAT} output must be bypassed to V_{SS} with a minimum capacitance of 1 µF for output currents up to 250 mA. A minimum capacitance of 4.7 µF is required for output currents above 250 mA.

The system test mode is entered by driving the THERM input greater than (V_{DD}-100 mV) with no battery connected to the output. In this mode, the MCP73833/4 can be used to power the system without a battery present.

Note 1: I_{THERM} is disabled during shutdown, stand-by, and system test modes.

2: A pull-down current source on the THERM input is active only in stand-by and system test modes.

3: During system test mode, the PROG input sets the available output current limit.

4: System test mode shall be exited by releasing the THERM input or cycling input power.

5.2 Digital Circuitry

5.2.1 STATUS INDICATORS AND POWER GOOD ($\overline{PG}$ - OPTION)

The charge status outputs have two different states: Low (L), and High Impedance (Hi-Z). The charge status outputs can be used to illuminate LEDs. Optionally, the charge status outputs can be used as an interface to a host microcontroller. Table 5-1 summarize the state of the status outputs during a charge cycle.

TABLE 5-1: STATUS OUTPUTS

Charge Cycle State	STAT1	STAT2	PG
Shutdown	Hi-Z	Hi-Z	Hi-Z
Standby	Hi-Z	Hi-Z	L
Charge in Progress	L	Hi-Z	L
Charge Complete (EOC)	Hi-Z	L	L
Temperature Fault	Hi-Z	Hi-Z	L
Timer Fault	Hi-Z	Hi-Z	L
System Test Mode	L	L	L

5.2.2 POWER GOOD ($\overline{PG}$) OPTION

The power good ($\overline{PG}$) option is a pseudo open-drain output. The $\overline{PG}$ output can sink current, but not source current. However, there is a diode path back to the input, and as such, the $\overline{PG}$ output should only be pulled up to the input. The $\overline{PG}$ output is low whenever the input to the MCP73833 is above the UVLO threshold and greater than the battery voltage. If the supply voltage is above the UVLO, but below V_{REG}(Typical)+0.3V, the MCP73833 will pulse the PG output as the device determines if a battery is present.

5.2.3 TIMER ENABLE ($\overline{TE}$) OPTION

The timer enable ($\overline{TE}$) input option is used to enable or disable the internal timer. A low signal on this pin enables the internal timer and a high signal disables the internal timer. The $\overline{TE}$ input can be used to disable the timer when the charger is supplying current to charge the battery and power the system load. The $\overline{TE}$ input is compatible with 1.8V logic.

5.2.4 DEVICE DISABLE (PROG)

The current regulation set input pin (PROG) can be used to terminate a charge at any time during the charge cycle, as well as to initiate a charge cycle or initiate a recharge cycle.

Placing a programming resistor from the PROG input to V_{SS} enables the device. Allowing the PROG input to float or by applying a logic-high input signal, disables the device and terminates a charge cycle. When disabled, the device's supply current is reduced to 100 µA, typically.

6.0 APPLICATIONS

The MCP73833/4 is designed to operate in conjunction with a host microcontroller or in stand-alone applications. The MCP73833/4 provides the preferred charge algorithm for Lithium-Ion and Lithium-Polymer cells Constant-current followed by Constant-voltage. Figure 6-1 depicts a typical stand-alone application circuit, while Figures 6-2 and 6-3 depict the accompanying charge profile.

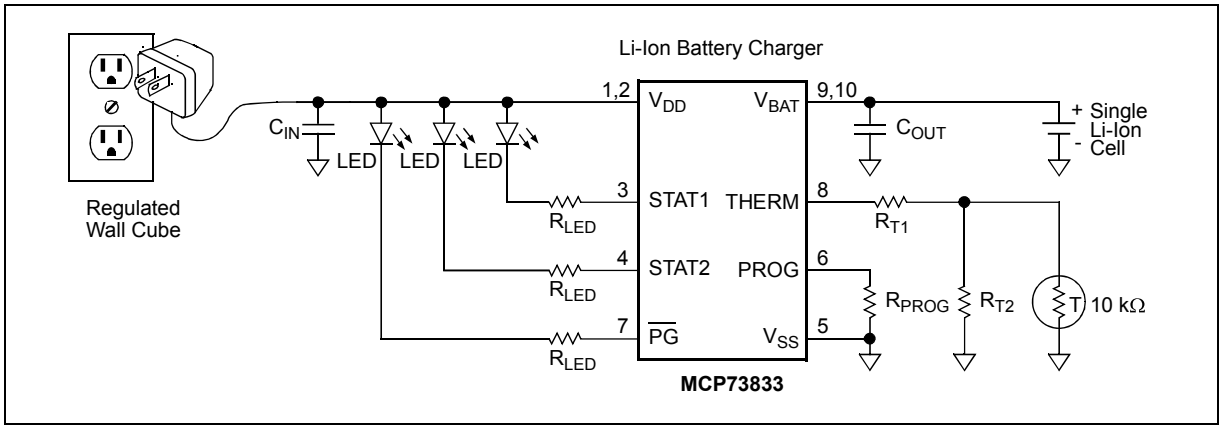


FIGURE 6-1: *Typical Application Circuit.*

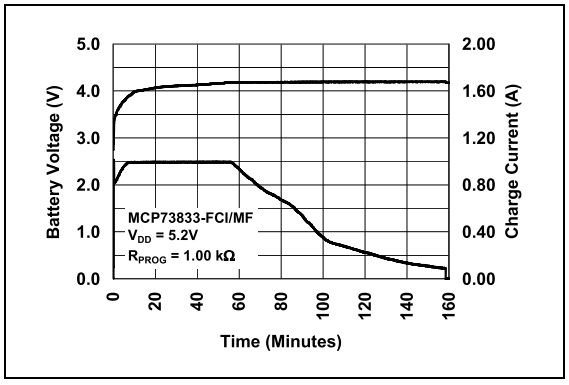


FIGURE 6-2: *Typical Charge Profile with Thermal Regulation (1700 mAh Li-Ion Battery).*

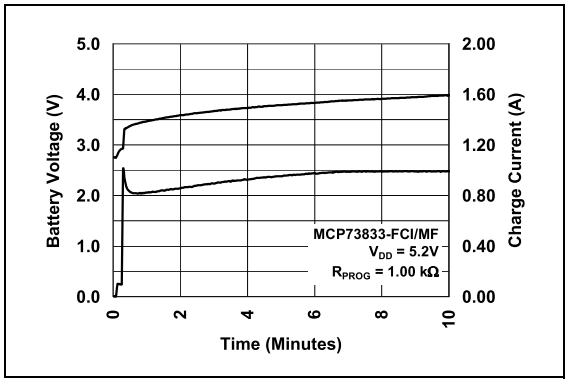


FIGURE 6-3: *Typical Charge Cycle Start with Thermal Regulation (1700 mAh Li-Ion Battery).*

6.1 Application Circuit Design

Due to the low efficiency of linear charging, the most important factors are thermal design and cost, which are a direct function of the input voltage, output current and thermal impedance between the battery charger and the ambient cooling air. The worst-case scenario is when the device has transitioned from the Preconditioning mode to the Constant-current mode. In this situation, the battery charger has to dissipate the maximum power. A trade-off must be made between the charge current, cost and thermal requirements of the charger.

6.1.1 COMPONENT SELECTION

Selection of the external components in Figure 6-1 is crucial to the integrity and reliability of the charging system. The following discussion is intended as a guide for the component selection process.

6.1.1.1 Current Programming Resistor (R_{PROG})

The preferred fast charge current for Lithium-Ion cells is at the 1C rate, with an absolute maximum current at the 2C rate. For example, a 500 mAh battery pack has a preferred fast charge current of 500 mA. Charging at this rate provides the shortest charge cycle times without degradation to the battery pack performance or life.

6.1.1.2 Thermal Considerations

The worst-case power dissipation in the battery charger occurs when the input voltage is at the maximum and the device has transitioned from the Preconditioning mode to the Constant-current mode. In this case, the power dissipation is:

$$PowerDissipation = (V_{DDMAX} - V_{PTHMIN}) \times I_{REGMAX}$$

Where:

V_{DDMAX}	=	the maximum input voltage
I_{REGMAX}	=	the maximum fast charge current
V_{PTHMIN}	=	the minimum transition threshold voltage

Power dissipation with a 5V, ±10% input voltage source is:

$$PowerDissipation = (5.5V - 2.7V) \times 550mA = 1.54W$$

This power dissipation with the battery charger in the MSOP-10 package will cause thermal regulation to be entered as depicted in Figure 6-3. Alternatively, the DFN-10 (3 mm x 3 mm) package could be utilized to reduce charge cycle times.

6.1.1.3 External Capacitors

The MCP73833/4 is stable with or without a battery load. In order to maintain good AC stability in the Constant-voltage mode, a minimum capacitance of 4.7 µF is recommended to bypass the V_{BAT} pin to V_{SS}. This capacitance provides compensation when there is no battery load. In addition, the battery and interconnections appear inductive at high frequencies. These elements are in the control feedback loop during Constant-voltage mode. Therefore, the bypass capacitance may be necessary to compensate for the inductive nature of the battery pack.

Virtually any good quality output filter capacitor can be used, independent of the capacitor's minimum Effective Series Resistance (ESR) value. The actual value of the capacitor (and its associated ESR) depends on the output load current. A 4.7 µF ceramic, tantalum or aluminum electrolytic capacitor at the output is usually sufficient to ensure stability for output currents up to a 500 mA.

6.1.1.4 Reverse-Blocking Protection

The MCP73833/4 provides protection from a faulted or shorted input. Without the protection, a faulted or shorted input would discharge the battery pack through the body diode of the internal pass transistor.

6.1.1.5 Charge Inhibit

The current regulation set input pin (PROG) can be used to terminate a charge at any time during the charge cycle, as well as to initiate a charge cycle or initiate a recharge cycle.

Placing a programming resistor from the PROG input to V_{SS} enables the device. Allowing the PROG input to float or by applying a logic-high input signal, disables the device and terminates a charge cycle. When disabled, the device's supply current is reduced to 100 µA, typically.

6.1.1.6 Temperature Monitoring

The charge temperature window can be set by placing fixed value resistors in series-parallel with a thermistor. The resistance values of R_{T1} and R_{T2} can be calculated with the following equations in order to set the temperature window of interest.

For NTC thermistors:

$$24k\Omega = R_{T1} + \frac{R_{T2} \times R_{COLD}}{R_{T2} + R_{COLD}}$$

$$5k\Omega = R_{T1} + \frac{R_{T2} \times R_{HOT}}{R_{T2} + R_{HOT}}$$

Where:

R_{T1}	=	the fixed series resistance
R_{T2}	=	the fixed parallel resistance
R_{COLD}	=	the thermistor resistance at the lower temperature of interest
R_{HOT}	=	the thermistor resistance at the upper temperature of interest

For example, by utilizing a 10 kΩ at 25C NTC thermistor with a sensitivity index, β, of 3892, the charge temperature range can be set to 0C - 50C by placing a 1.54 kΩ resistor in series (R_{T1}), and a 69.8 kΩ resistor in parallel (R_{T2}) with the thermistor as depicted in Figure 6-1.

6.1.1.7 Charge Status Interface

A status output provides information on the state of charge. The output can be used to illuminate external LEDs or interface to a host microcontroller. Refer to Table 5-1 for a summary of the state of the status output during a charge cycle.

6.2 PCB Layout Issues

For optimum voltage regulation, place the battery pack as close as possible to the device's V_{BAT} and V_{SS} pins, recommended to minimize voltage drops along the high current-carrying PCB traces.

If the PCB layout is used as a heatsink, adding many vias in the heatsink pad can help conduct more heat to the backplane of the PCB, thus reducing the maximum junction temperature. Figures 6-4 and 6-5 depict a typical layout with PCB heatsinking.

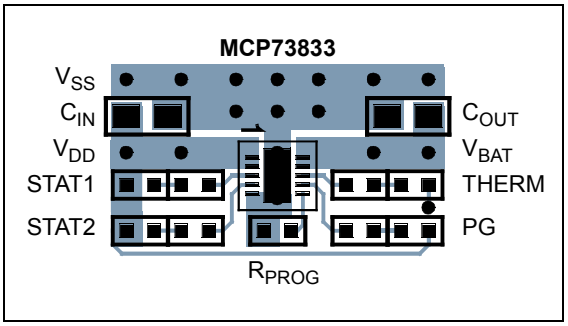


FIGURE 6-4: *Typical Layout (Top).*

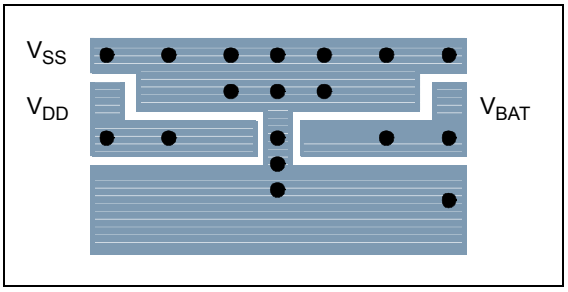


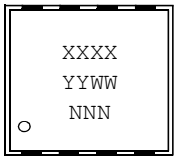
FIGURE 6-5: *Typical Layout (Bottom).*

NOTES:

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

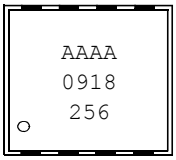
10-Lead DFN (3x3)



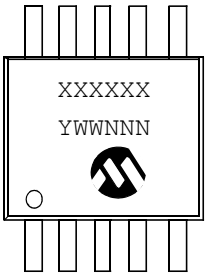
Part Number *	Marking Code	Part Number *	Marking Code
MCP73833-AMI/MF	AAAA		
MCP73833-BZI/MF	AAAB		
MCP73833-FCI/MF	AAAC	MCP73834-FCI/MF	BAAC
MCP73833-GPI/MF	AAAD	MCP73834-GPI/MF	BAAD
MCP73833-NVI/MF	AAAF	MCP73834-NVI/MF	BAAF
MCP73833-6SI/MF	AAAH	MCP73834-6SI/MF	BAAH
MCP73833-CNI/MF	AAAK	MCP73834-CNI/MF	BAAK

* Consult Factory for Alternative Device Options.

Example:



10-Lead MSOP



Part Number *	Marking Code	Part Number *	Marking Code
MCP73833-AMI/UN	833AMI		
MCP73833-BZI/UN	833BZI		
MCP73833-FCI/UN	833FCI	MCP73834-FCI/UN	834FCI
MCP73833-GPI/UN	833GPI	MCP73834-GPI/UN	834GPI
MCP73833-NVI/UN	833NVI	MCP73834-NVI/UN	834NVI
MCP73833-CNI/UN	833CNI	MCP73834-CNI/UN	834CNI

* Consult Factory for Alternative Device Options.

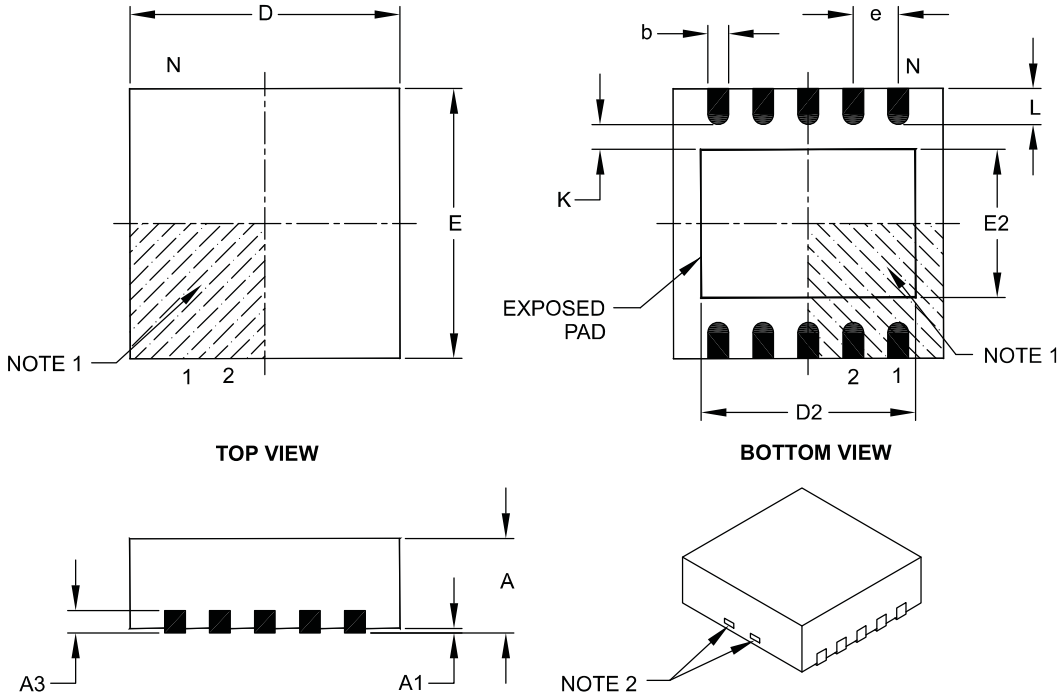
Example:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.20	2.35	2.48
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.40	1.58	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

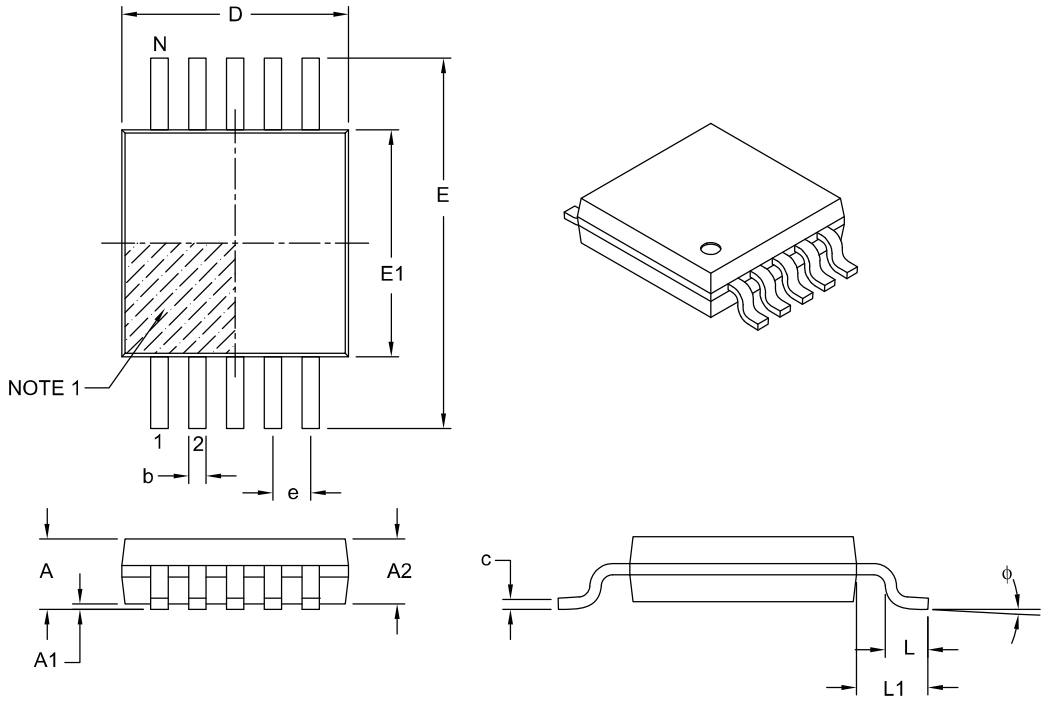
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-063B

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.15	–	0.33

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (May 2009)

The following is the list of modifications:

1. Added the MCP73833-6SI/MF and MCP73834-6SI/MF10-lead DFN packages.
2. Updated DFN pinout.
3. Updated Package Outline Drawings.
4. Updated Appendix A Revision History.

Revision A (September 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. **XX** **X/** **XX**

Device **Output Options*** **Temp.** **Package**

Device:
- MCP73833: 1A Fully Integrated Charger, PG function on pin 7
- MCP73833T: 1A Fully Integrated Charger, PG function on pin 7 (Tape and Reel)
- MCP73834: 1A Fully Integrated Charger, TE function on pin 7
- MCP73834T: 1A Fully Integrated Charger, TE function on pin 7 (Tape and Reel)

Output Options * * — * Refer to table below for different operational options.

* * Consult Factory for Alternative Device Options.

Temperature: I = -40°C to +85°C

Package Type:
- MF = Plastic Dual Flat No Lead (DFN) (3x3x0.9 mm Body), 10-lead
- UN = Plastic Micro Small Outline Package (MSOP), 10-lead

Examples: * *

a) MCP73833-AMI/UN: 10-lead MSOP pkg.
b) MCP73833-BZI/UN: 10-lead MSOP pkg.
c) MCP73833-CNI/MF: 10-lead DFN pkg.
d) MCP73833-FCI/UN: 10-lead MSOP pkg.
e) MCP73833-GPI/UN: 10-lead MSOP pkg.
f) MCP73833-NVI/MF: 10-lead DFN pkg.
g) MCP73833-6SI/MF: 10-lead DFN pkg.

a) MCP73834-CNI/MF: 10-lead DFN pkg.
b) MCP73834-FCI/UN: 10-lead MSOP pkg.
c) MCP73834-GPI/UN: 10-lead MSOP pkg.
d) MCP73834-NVI/MF: 10-lead DFN pkg.
e) MCP73834-6SI/MF: 10-lead DFN pkg.

* * Consult Factory for Alternative Device Options

Part Number	V_{REG}	I_{PREG}/I_{REG}	V_{PTH}/V_{REG}	I_{TERM}/I_{REG}	V_{RTH}/V_{REG}	Timer Period
MCP73833-AMI/MF	4.20V	10%	71.5%	7.5%	96.5%	0 hours
MCP73833-BZI/MF	4.20V	100%	N/A	7.5%	96.5%	0 hours
MCP73833-CNI/MF	4.20V	10%	71.5%	20%	94%	4 hours
MCP73833-FCI/MF	4.20V	10%	71.5%	7.5%	96.5%	6 hours
MCP73833-GPI/MF	4.20V	100%	N/A	7.5%	96.5%	6 hours
MCP73833-NVI/MF	4.35V	10%	71.5%	7.5%	96.5%	6 hours
MCP73833-6SI/MF	4.50V	10%	71.5%	7.5%	96.5%	6 hours
MCP73833-AMI/UN	4.20V	10%	71.5%	7.5%	96.5%	0 hours
MCP73833-FCI/UN	4.20V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-BZI/MF	4.20V	100%	N/A	7.5%	96.5%	0 hours
MCP73834-CNI/MF	4.20V	10%	71.5%	20%	94%	4 hours
MCP73834-FCI/MF	4.20V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-NVI/MF	4.35V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-6SI/MF	4.50V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-FCI/UN	4.20V	10%	71.5%	7.5%	96.5%	6 hours

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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03/26/09

UCC2870x Constant-Voltage, Constant-Current Controller With Primary-Side Regulation

1 Features

- < 30-mW No-Load Power for 5-Star Rating
- Primary-Side Regulation (PSR) Eliminates Opto-Coupler
- ±5% Voltage and Current Regulation
- 130-kHz Maximum Switching Frequency Enables High-Power Density Charger Designs
- Quasi-Resonant Valley-Switching Operation for Highest Overall Efficiency
- Patent-Pending Frequency-Jitter Scheme to Ease EMI Compliance
- Wide VDD Range Allows Small Bias Capacitor
- Clamped Gate-Drive Output for MOSFET
- Protection Functions: Overvoltage, Low-Line, and Overcurrent
- Programmable Cable Compensation (UCC28700 Only)
- NTC Resistor Interface (UCC28701, UCC28702 and UCC28703 Only) With Fixed Cable Compensation Options
- SOT-23 Package

2 Applications

- USB-Compliant Adapters and Chargers for Consumer Electronics (Cell Phones, Tablets and Cameras)
- AC and DC Power Supplies

3 Description

The UCC28700 family of flyback power supply controllers provides Constant-Voltage (CV) and Constant-Current (CC) output regulation without the use of an optical coupler. The devices process information from the primary power switch and an auxiliary flyback winding for precise control of output voltage and current. Low start-up current, dynamically controlled operating states and a tailored modulation profile support very low standby power without sacrificing start-up time or output transient response.

Control algorithms in the UCC28700 family allow operating efficiencies to meet or exceed applicable standards. The output drive interfaces to a MOSFET power switch. Discontinuous Conduction Mode (DCM) with valley switching reduces switching losses. Modulation of switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

The controllers have a maximum switching frequency of 130 kHz and always maintain control of the peak-primary current in the transformer. Protection features help keep primary and secondary component stresses in check. The UCC28700 allows the level of cable compensation to be programmed. The UCC28701, UCC28702, and UCC28703 devices allow remote temperature sensing using a Negative Temperature Coefficient (NTC) resistor while providing fixed cable-compensation levels.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28700	SOT-23 (6)	2.90 mm × 1.60 mm
UCC28701		
UCC28702		
UCC28703		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic

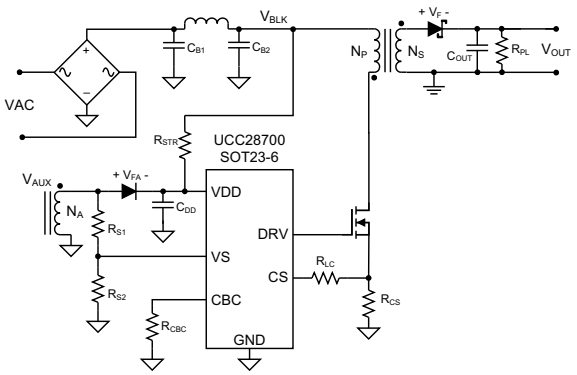


Table of Contents

4 Revision History

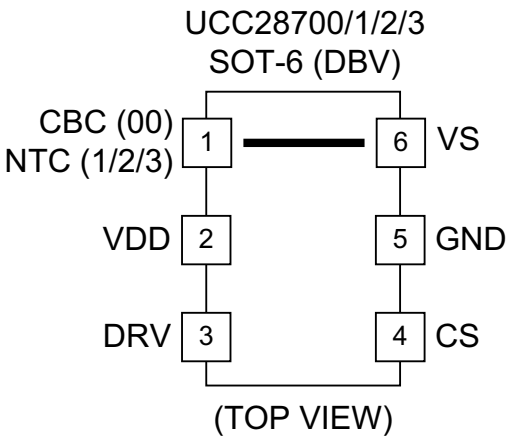
Changes from Original (July 2012) to Revision A	Page
• Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Device Comparison Table[(1)(2)]

PART NUMBER	VERSION
UCC28700	Programmable cable compensation
UCC28701	NTC, 0 mV (at 5-V output) cable compensation option
UCC28702	NTC, 150 mV (at 5-V output) cable compensation option
UCC28703	NTC, 300 mV (at 5-V output) cable compensation option

(1) See Addendum for specific device ordering information.
(2) For other fixed cable compensation options, please consult the factory.

6 Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	UCC28700 NO.	UCC28701/2/3 NO.		
CBC	1	—	I	Cable Compensation (CBC) is a programming pin for compensation of cable voltage drop. Cable compensation is programmed with a resistor to GND.
CS	4	4	I	Current Sense (CS) input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the AC-mains input varies.
DRV	3	3	O	Drive (DRV) is an output used to drive the gate of an external high voltage MOSFET switching transistor.
GND	5	5	—	The Ground (GND) pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
NTC	—	1	I	NTC is an interface to an external NTC (negative temperature coefficient) resistor for remote temperature sensing. Pulling this pin low shuts down PWM action.
VDD	2	2	—	VDD is the bias supply input pin to the controller. A carefully-placed bypass capacitor to GND is required on this pin.
VS	6	6	I	Voltage Sense (VS) is an input used to provide voltage and timing feedback to the controller. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program the AC-mains run and stop thresholds and line compensation at the CS pin.

7 Specifications

7.1 Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Bias supply voltage	V_{VDD}		38	V
Continuous gate current sink	I_{DRV}		50	mA
Continuous gate current source	I_{DRV}		Self-limiting	
Peak VS pin current	I_{VS}		−1.2	
Gate-drive voltage at DRV	V_{DRV}	−0.5	Self-limiting	V
Voltage range	VS	−0.75	7	
	CS, CBC (UCC28700), NTC (UCC28701/2/3)	−0.5	5	
Operating junction temperature range	T_J	−55	150	°C
Lead temperature 0.6 mm from case for 10 seconds			260	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VDD	Bias supply operating voltage	9	35	V
C_{VDD}	VDD bypass capacitor	0.047	1	µF
R_{CBC}	Cable-compensation resistance	10		kΩ
I_{VS}	VS pin current	−1		mA
T_J	Operating junction temperature	−20	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		UCC2870x DBV 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[2]	180	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	71.2	
θ_{JB}	Junction-to-board thermal resistance[4]	44.4	
ψ_{JT}	Junction-to-top characterization parameter[5]	5.1	
ψ_{JB}	Junction-to-board characterization parameter[6]	43.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

over operating free-air temperature range, VDD = 25 V, R_{CBC} = R_{NTC} = open, –20°C ≤ T_A ≤ 125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2.1	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		85	110	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state		1	1.5	
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		2.1	2.8	mA
UNDER-VOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	7.7	8.1	8.45	
VS INPUT						
V_{VSR}	Regulating level	Measured at no-load condition, T_J = 25°C	4.01	4.05	4.09	V
V_{VSNC}	Negative clamp level	I_{VS} = -300 µA, volts below ground	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
CS INPUT						
$V_{CST(max)}$	Max CS threshold voltage	V_{VS} = 3.7 V[1]	715	750	775	mV
$V_{CST(min)}$	Min CS threshold voltage	V_{VS} = 4.35 V[1]	230	250	270	
K_{AM}	AM control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	2.75	3.0	3.15	V/V
V_{CCR}	constant-current regulating level	CC regulation constant	310	319	329	mV
K_{LC}	Line compensating current ratio	I_{VSLS} = -300 µA, I_{VSLS} / current out of CS pin	23	25	28	A/A
T_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	195	235	275	ns
DRV						
I_{DRS}	DRV source current	V_{DRV} = 8 V, V_{VDD} = 9 V	20	25		mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		6	12	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V		14	16	V
R_{DRVSS}	DRV pull-down in start state		150	200	230	kΩ

(1) These devices automatically vary the control frequency and current sense thresholds to improve EMI performance, these threshold voltages and frequency limits represent average levels.

Electrical Characteristics (continued)

over operating free-air temperature range, VDD = 25 V, R_{CBC} = R_{NTC} = open, –20°C ≤ T_A ≤ 125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PROTECTION						
V_{OVP}	Over-voltage threshold	At VS input, T_J = 25°C	4.52	4.6	4.68	V
V_{OCP}	Over-current threshold	At CS input	1.4	1.5	1.6	
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin – increasing	190	220	260	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin – decreasing	70	80	95	
K_{VSL}	VS line-sense ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$	2.5	2.8	3.05	A/A
$T_{J(stop)}$	Thermal shut-down temperature	Internal junction temperature		165		°C
CABLE COMPENSATION (UCC28700 ONLY)						
$V_{CBC(max)}$	Cable compensation maximum voltage	Voltage at CBC at full load	2.8	3.0	3.4	V
$V_{CVS(min)}$	Compensation at VS	V_{CBC} = open, change in VS regulating level at full load	–45	–15	25	mV
$V_{CVS(max)}$	Maximum compensation at VS	V_{CBC} = 0 V, change in VS regulating level at full load	275	320	365	
CABLE COMPENSATION (UCC28701, UCC28702, AND UCC28703 ONLY)						
V_{CVS}	Compensation at VS (UCC28701)	Change in VS regulating level at full load	–45	–15	25	mV
V_{CVS}	Compensation at VS (UCC28702)	Change in VS regulating level at full load		100		
V_{CVS}	Compensation at VS (UCC28703)	Change in VS regulating level at full load		200		
NTC INPUT (UCC28701, UCC28702, AND UCC28703 ONLY)						
V_{NTCTH}	NTC shut-down threshold	Fault UVLO cycle when below this threshold		0.95		V
I_{NTC}	NTC pull-up current	Current out of pin		105		µA

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SW(max)}$	Maximum switching frequency	V_{VS} = 3.7 V(1)	120	130	140	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{VS} = 4.35 V(1)	875	1000	1100	Hz
T_{ZTO}	Zero-crossing timeout delay		1.8	2.1	2.45	µs

(1) These devices automatically vary the control frequency and current sense thresholds to improve EMI performance, these threshold voltages and frequency limits represent average levels.

7.7 Typical Characteristics

At VDD = 25 V, unless otherwise noted.

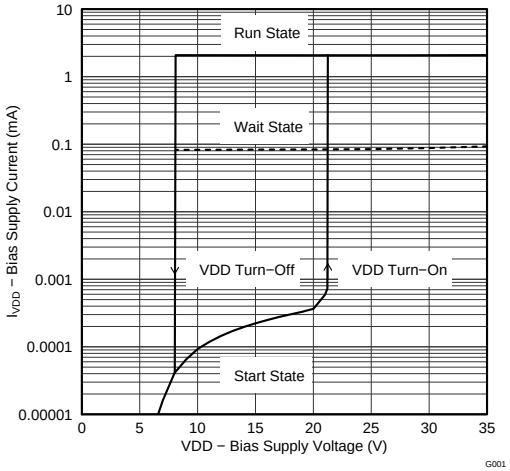


Figure 1. Bias Supply Current vs. Bias Supply Voltage

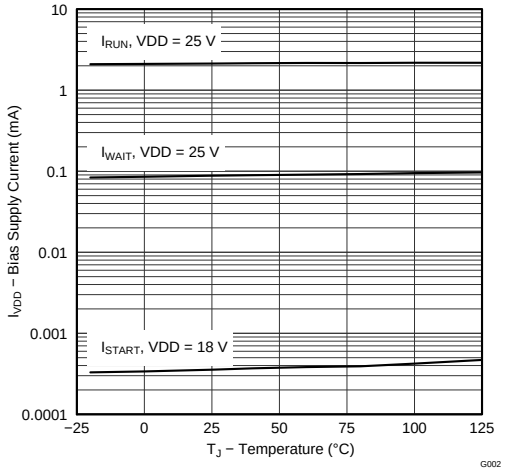


Figure 2. Bias Supply Current vs. Temperature

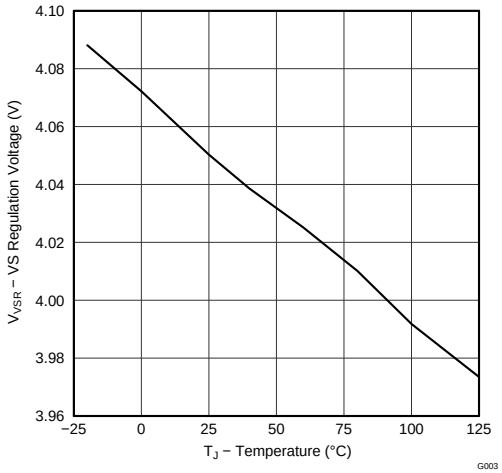


Figure 3. VS Regulation Voltage vs. Temperature

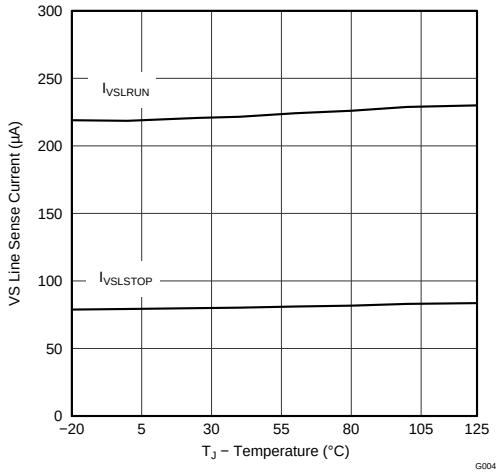


Figure 4. Line-Sense Current vs. Temperature

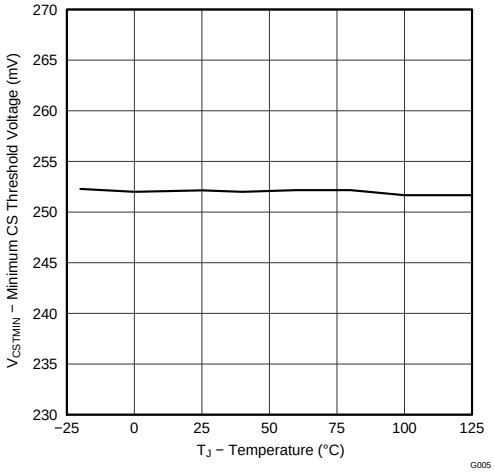


Figure 5. Minimum CS Threshold Voltage vs. Temperature

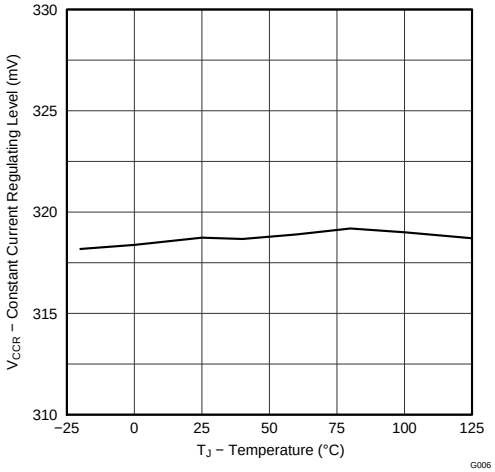


Figure 6. Constant-Current Regulating Level vs. Temperature

Typical Characteristics (continued)

At VDD = 25 V, unless otherwise noted.

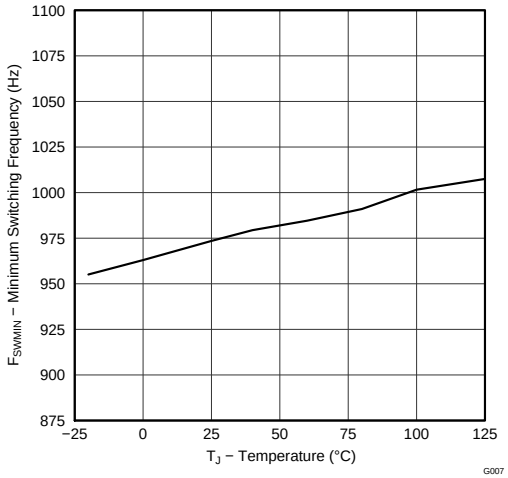
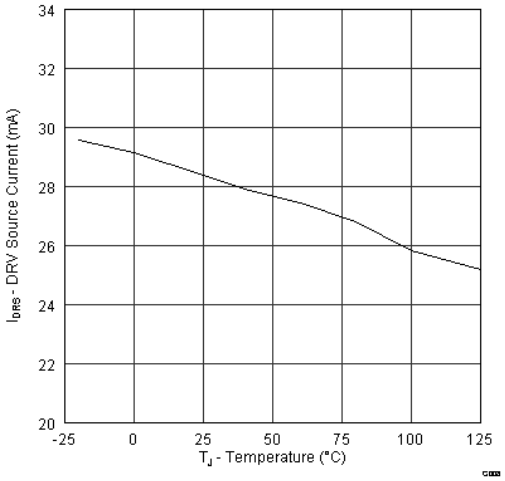


Figure 7. Minimum Switching Frequency vs. Temperature



V_{DRV} = 8 V, V_{VDD} = 9 V

Figure 8. DRV Source Current vs. Temperature

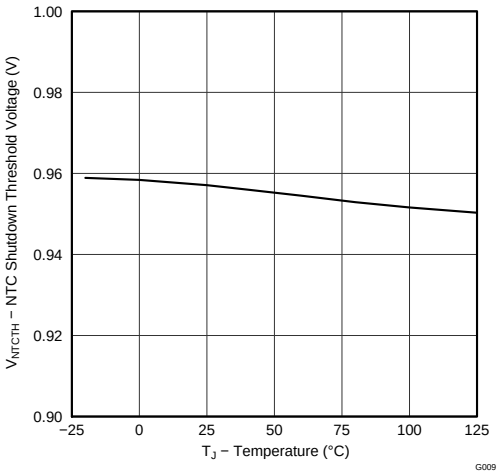


Figure 9. NTC Shutdown Threshold Voltage vs. Temperature

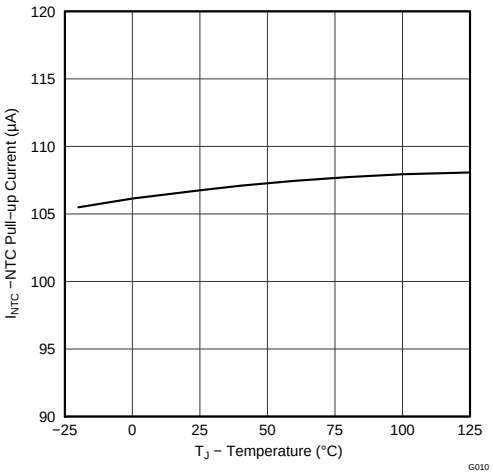


Figure 10. NTC Pullup Current vs. Temperature

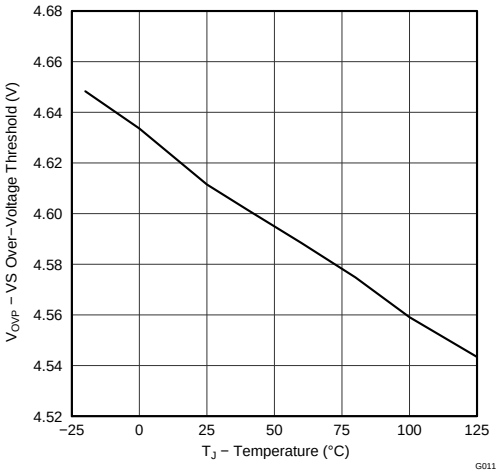


Figure 11. Overvoltage Threshold vs. Temperature

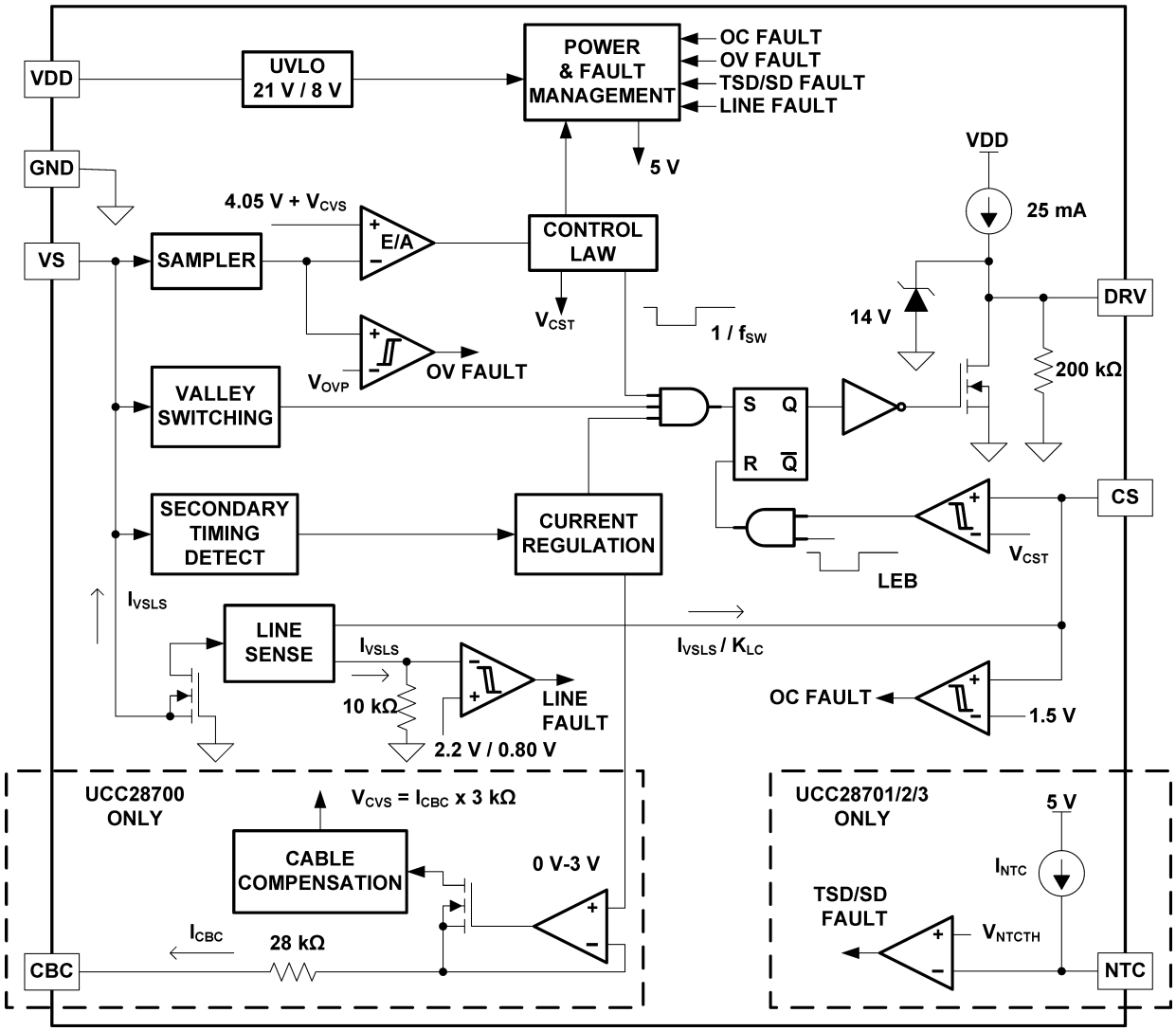
8 Detailed Description

8.1 Overview

The UCC28700 is a flyback power supply controller which provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley-switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range. The control law provides a wide-dynamic operating range of output power to achieve the <30-mW stand-by power requirement.

Another feature beneficial to achieve low stand-by power without excessive start-up time is a wide operating VDD range to allow a high-value VDD start-up resistance and low-value VDD capacitance. During low-power operating ranges the device has power management features to reduce the device operating current at operating frequencies below 44 kHz. The UCC28700 controller includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete charger solution can be realized with a straightforward design process, low cost and low component count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Detailed Pin Description

8.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor (+) terminal. The VDD turn-on UVLO threshold is 21 V and turn-off UVLO threshold is 8.1 V, with an available operating range up to 35 V. The USB charging specification requires the output current to operate in constant-current mode from 5 V to a minimum of 2 V; this is easily achieved with a nominal VDD of approximately 25 V. The additional VDD headroom up to 35 V allows for VDD to rise due to the leakage energy delivered to the VDD capacitor in high-load conditions. Also, the wide VDD range provides the advantage of selecting a relatively small VDD capacitor and high-value start-up resistance to minimize no-load stand-by power loss in the start-up resistor.

8.3.1.2 GND (Ground)

This is a single ground reference external to the device for the gate drive current and analog signal reference. Place the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

8.3.1.3 VS (Voltage-Sense)

The VS pin is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Avoid placing a filter capacitor on this input which would interfere with accurate sensing of this waveform.

The VS pin also senses the bulk capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. This information is sensed during the MOSFET on-time. For the AC-input run/stop function, the run threshold on VS is 220 µA and the stop threshold is 80 µA. The values for the auxilliary voltage divider upper-resistor R_{S1} and lower-resistor R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}}$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$ is the AC RMS voltage to enable turn-on of the controller (run),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the MOSFET on-time. (see the *Electrical Characteristics* table) (1)

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}}$$

where

- V_{OCV} is the converter regulated output voltage,
- V_F is the output rectifier forward drop at near-zero current,
- N_{AS} is the transformer auxiliary to secondary turns ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{VSR} is the CV regulating level at the VS input (see the *Electrical Characteristics* table). (2)

Feature Description (continued)

8.3.1.4 DRV (Gate Drive)

The DRV pin is connected to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turn-on characteristic of the driver is a 25-mA current source which limits the turn-on dv/dt of the MOSFET drain and reduces the leading-edge current spike, but still provides gate-drive current to overcome the Miller plateau. The gate-drive turn-off current is determined by the low-side driver $R_{DS(on)}$ and any external gate-drive resistance. The user can reduce the turn-off MOSFET drain dv/dt by adding external gate resistance.

8.3.1.5 CS (Current Sense)

The current-sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The current-sense threshold is 0.75 V for $I_{PP(max)}$ and 0.25 V for $I_{PP(min)}$. The series resistor R_{LC} provides the function of feed-forward line compensation to eliminate change in I_{PP} due to change in di/dt and the propagation delay of the internal comparator and MOSFET turn-off time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turn-on current spike. It should not be necessary to place a bypass capacitor on the CS pin. The value of R_{CS} is determined by the target output current in constant-current (CC) regulation. The values of R_{CS} and R_{LC} can be determined by the equations below. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example: With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 1.5%. The η_{XFMR} value is approximately: 1 - 0.05 - 0.035 - 0.015 = 0.9.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 I_{OCC}} \times \eta_{XFMR}$$

where

- V_{CCR} is a current regulation constant (see the *Electrical Characteristics* table),
- N_{PS} is the transformer primary-to-secondary turns ratio (a ratio of 13 to 15 is recommended for 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency. (3)

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P}$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- T_D is the current-sense delay including MOSFET turn-off delay, add ~50 ns to MOSFET delay,
- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant (see the *Electrical Characteristics* table). (4)

8.3.1.6 CBC (Cable Compensation), Pin 1 UCC28700

The cable compensation pin is connected to a resistor to ground to program the amount of output voltage compensation to offset cable resistance. The cable compensation block provides a 0-V to 3-V voltage level on the CBC pin corresponding to 0 to I_{OCC} output current. The resistance selected on the CBC pin programs a current mirror that is summed into the VS feedback divider therefore increasing the output voltage as I_{OUT} increases. There is an internal series resistance of 28 kΩ to the CBC pin which sets a maximum cable compensation of a 5-V output to 400 mV when CBC is shorted to ground. The CBC resistance value can be determined by the equation below.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\ k\Omega \times (V_{OCV} + V_F)}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega$$

Feature Description (continued)

where

- V_O is the output voltage,
- V_F is the diode forward voltage,
- V_{OCBC} is the target cable compensation voltage at the output terminals,
- $V_{CBC(max)}$ is the maximum voltage at the cable compensation pin at the maximum converter output current (see the *Electrical Characteristics* table),
- V_{VSR} is the CV regulating level at the VS input (see the *Electrical Characteristics* table). (5)

8.3.1.7 NTC (NTC Thermistor Shut-down), Pin 1 UCC28701/2/3

These versions of the UCC28700 family utilize pin 1 for an external NTC thermistor to allow user-programmable external thermal shut-down. The shut-down threshold is 0.95 V with an internal 105-µA current source which results in a 9.05-kΩ thermistor shut-down threshold. These controllers have either zero or fixed internal cable compensation.

8.3.2 Fault Protection

There is comprehensive fault protection incorporated into the UCC28700. Protection functions include:

- Output overvoltage
- Input undervoltage
- Internal overtemperature
- Primary overcurrent fault
- CS pin fault
- VS pin fault

A UVLO reset and restart sequence applies for all fault protection events.

The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 115% of the nominal V_{OUT}, the device stops switching and keeps the internal circuitry enabled to discharge the VDD capacitor to the UVLO turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

The UCC28700 always operates with cycle-by-cycle primary peak current control. The normal operating range of the CS pin is 0.75 V to 0.25 V. There is additional protection if the CS pin reaches 1.5 V. This results in a UVLO reset and restart sequence. There is no leading-edge blanking on the 1.5-V threshold on CS.

The line input run and stop thresholds are determined by current information at the VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through R_{S1} is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. The run current threshold is 220 µA and the stop current threshold is 80 µA.

The internal overtemperature protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

8.4 Device Functional Modes

8.4.1 Primary-Side Voltage Regulation

Figure 12 shows a simplified flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control.

Device Functional Modes (continued)

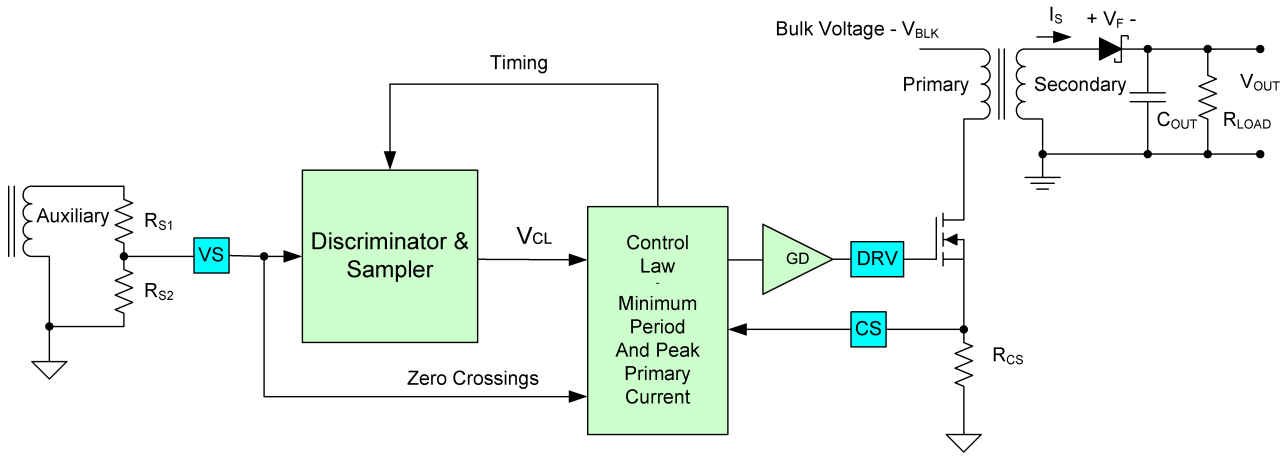


Figure 12. Simplified Flyback Convertor (with the main voltage regulation blocks)

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in Figure 13 it is clear there is a down slope representing a decreasing total rectifier V_F and resistance voltage drop ($I_S R_S$) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V; the resistor divider is selected as outlined in the VS pin description.

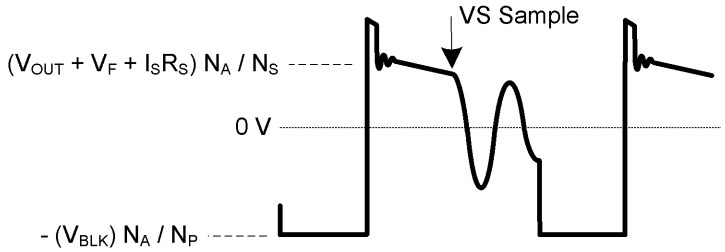


Figure 13. Auxiliary Winding Voltage

The UCC28700 VS signal sampler includes signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 14 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, T_{LK_RESET} in Figure 14. Because this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time less than 500 ns for I_{PRI} minimum, and less than 1.5 µs for I_{PRI} maximum. The second detail is the amplitude of ringing on the V_{AUX} waveform following T_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 100 mV_{p-p} at least 200 ns before the end of the demagnetization time, t_{DM}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary winding voltage by R_{S1} and R_{S2}, and is equal to 100 mV x (R_{S1} + R_{S2}) / R_{S2}.

Device Functional Modes (continued)

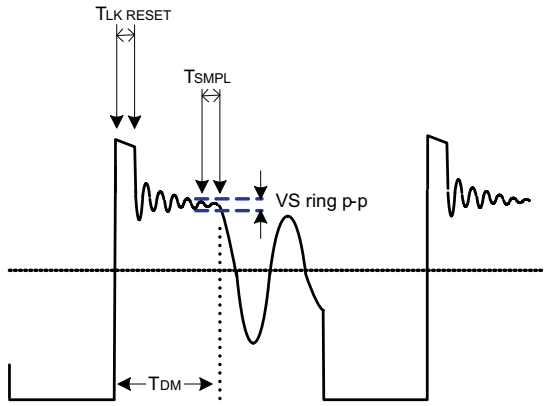


Figure 14. Auxiliary Waveform Details

During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode as illustrated in Figure 15 below. The internal operating frequency limits of the device are 130 kHz maximum and 1 kHz minimum. The transformer primary inductance and primary peak current chosen sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no stability compensation required for the UCC28700 controller.

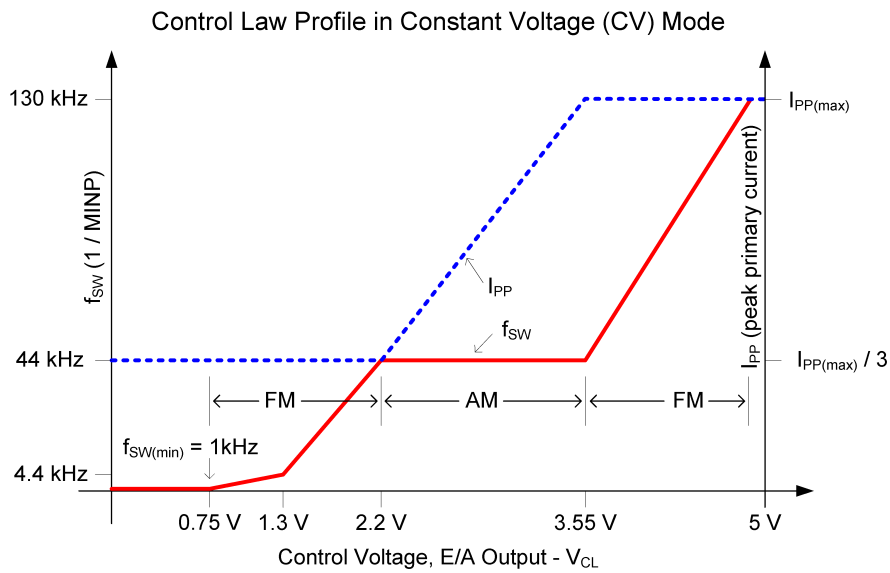


Figure 15. Frequency and Amplitude Modulation Modes (during voltage regulation)

8.4.2 Primary-Side Current Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at $I_{PP(max)}$. Referring to Figure 16 below, the primary-peak current, turns ratio, secondary demagnetization time (t_{DM}), and switching period (T_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by Equation 6. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

Device Functional Modes (continued)

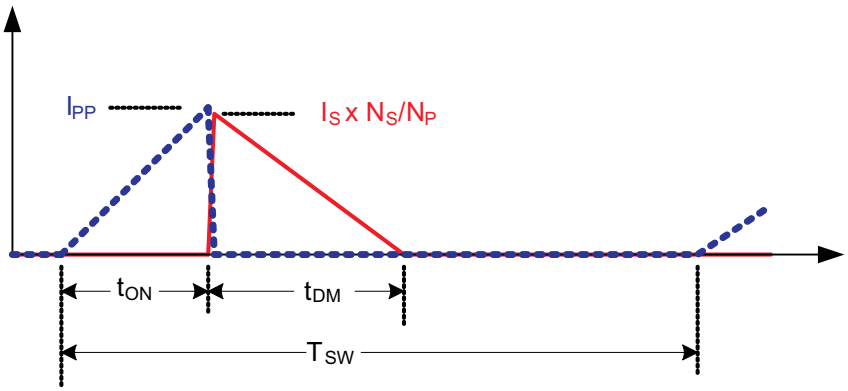


Figure 16. Transformer Currents

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{T_{SW}} \tag{6}$$

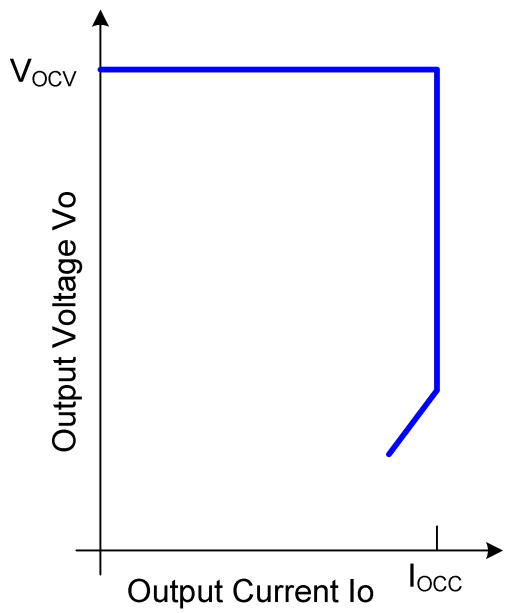


Figure 17. Typical Target Output V-I Characteristic

8.4.3 Valley-Switching

The UCC28700 utilizes valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turn-on current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing has diminished.

Referring to Figure 18 below, the UCC28700 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

Device Functional Modes (continued)

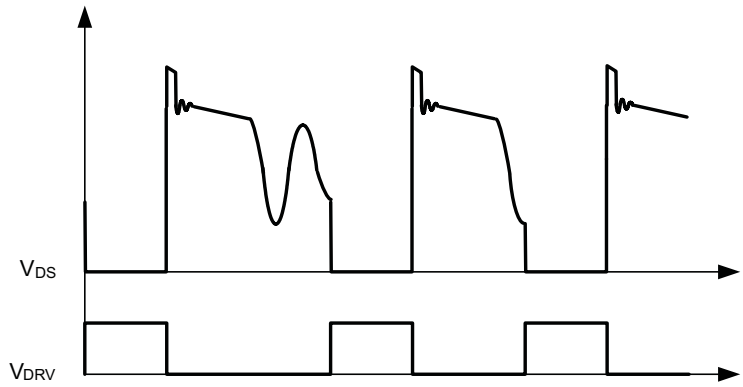


Figure 18. Valley-Skipping Mode

8.4.4 Start-Up Operation

Upon application of input voltage to the converter, the start-up resistor connected to VDD from the bulk capacitor voltage (V_{BLK}) charges the VDD capacitor. During charging of the VDD capacitor the device bias supply current is less than 1.5 µA. When VDD reaches the 21-V UVLO turn-on threshold, the controller is enabled and the converter starts switching. The initial three cycles are limited to $I_{PP(min)}$. This allows sensing any initial input or output faults with minimal power delivery. After the initial three cycles at minimum $I_{PP(min)}$, the controller responds to the condition dictated by the control law. The converter remains in discontinuous mode during charging of the output capacitor(s), maintaining a constant output current until the output voltage is in regulation.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC2870x family of flyback power supply controllers provides constant voltage (CV) and constant current (CC) output regulation to help meet USB-compliant adaptors and charger requirements. These devices use the information obtained from auxiliary winding sensing (VS) to control the output voltage and do not require optocoupler/TL431 feedback circuitry. Not requiring optocoupler feedback reduces the component count and makes the design more cost effective.

9.2 Typical Application

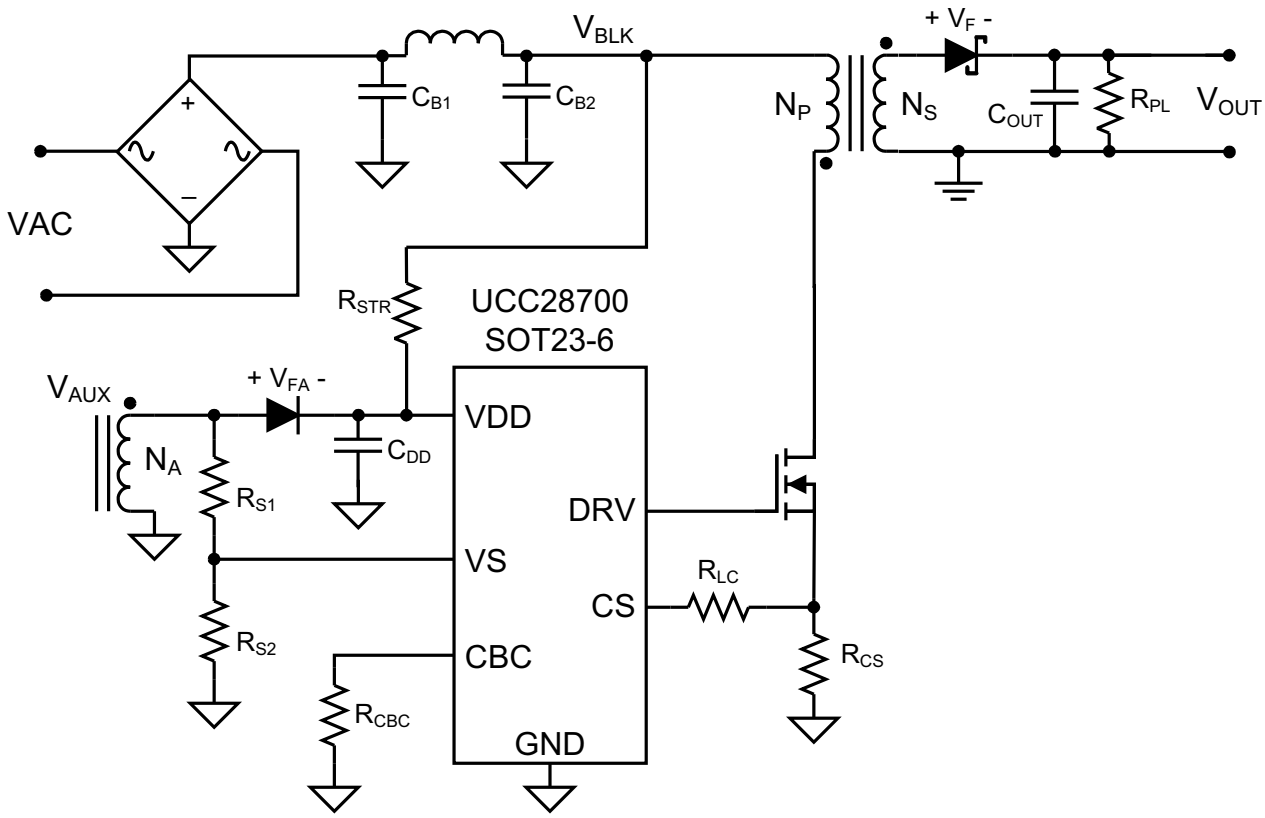


Figure 19. Typical Application Circuit

9.2.1 Design Requirements

Table 1. Design Parameters

PARAMETER	SYMBOL	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
Input Voltage	V_{IN}		100	115/230	240	V
Line Frequency	f_{LINE}		47	50/60	64	Hz
No Load Input Power	P_{SB_CONV}	V_{IN} = Nom, I_O = 0A			30	mW

Typical Application (continued)

Table 1. Design Parameters (continued)

PARAMETER	SYMBOL	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
Brownout Voltage	$V_{IN(RUN)}$	I_O = Nom		70		V
OUTPUT CHARACTERISTICS						
Output Voltage	V_O	V_{IN} = Nom, I_O = Nom	4.75	5	5.25	V
Output Voltage Ripple	V_{RIPPLE}	V_{IN} = Nom, I_O = Max			0.1	V
Output Current	I_O	V_{IN} = Min to Max		1	1.05	A
Output OVP	V_{OVP}	I_{OUT} = Min to Max		5.75		V
Transient Response						
Load Step (V_O = 4.1 V to 6 V)	$V_{O\Delta}$	(0.1 to 0.6 A) or (0.6 to 0.1 A) $V_{O\Delta}$ = 0.9 V for C_{OUT} calculation in applications section	4.1	5	6	A
SYSTEMS CHARACTERISTICS						
Switching Frequency					105	kHz
Full Load Efficiency (115/230 V RMS Input)	η	I_O = 1 A	74%		76%	

9.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28700 family of controllers. Please refer to the Figure 19 for circuit details and section *Device Nomenclature* for variable definitions used in the applications equations below.

9.2.2.1 Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage so these should be reviewed. The UCC28700 controller requires a minimum on time of the MOSFET (T_{ON}) and minimum D_{MAG} time (T_{DMAG}) of the secondary rectifier in the high line, minimum load condition. The selection of F_{MAX}, L_P and R_{CS} affects the minimum T_{ON} and T_{DMAG}.

The secondary rectifier and MOSFET voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \tag{7}$$

For the MOSFET V_{DS} voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \tag{8}$$

The following equations are used to determine if the minimum T_{ON} target of 300 ns and minimum T_{DMAG} target of 1.1 µs is achieved.

$$T_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)} \times V_{CST(min)}}{V_{CST(max)}} \tag{9}$$

$$T_{DMAG(min)} = \frac{T_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \tag{10}$$

9.2.2.2 Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no-load. For example, in some USB charger applications there is a requirement to maintain a minimum V_O of 4.1 V with a load-step transient of 0 mA to 500 mA . The equation below assumes that the switching frequency can be at the UCC28700 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN}\left(\frac{1}{f_{SW(min)}} + 150\ \mu s\right)}{V_{O\Delta}} \tag{11}$$

Another consideration of the output capacitor(s) is the ripple voltage requirement which is reviewed based on secondary peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in the equation below.

$$R_{ESR} = \frac{V_{RIPPLE} \times 0.8}{I_{PP(max)} \times N_{PS}} \tag{12}$$

9.2.2.3 VDD Capacitance, C_{DD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the voltage to the UCC28700. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. There is an estimated 1 mA of gate-drive current in the equation and 1 V of margin added to VDD.

$$C_{DD} = \frac{\left(I_{RUN} + 1\,mA\right) \times \frac{C_{OUT} \times V_{OCC}}{I_O}}{\left(V_{DD(on)} - V_{DD(off)}\right) - 1\,V} \tag{13}$$

9.2.2.4 VDD Start-Up Resistance, R_{STR}

Once the VDD capacitance is known, the start-up resistance from V_{BULK} to achieve the turn-on time target can be determined.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{T_{STR}}} \tag{14}$$

9.2.2.5 VS Resistor Divider, Line Compensation, and Cable Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary to primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \tag{15}$$

The low-side VS pin resistor is selected based on desired V_O regulation voltage.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times \left(V_{OCV} + V_F\right) - V_{VSR}} \tag{16}$$

The UCC28700 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and expected gate drive and MOSFET turn-off delay. Assume a 50-ns internal delay in the UCC28700.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} \tag{17}$$

On the UCC28700 which has adjustable cable compensation, the resistance for the desired compensation level at the output terminals can be determined using the equation below.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\ k\Omega \times (V_{OCV} + V_F)}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega \tag{18}$$

9.2.2.6 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np to Ns turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV}, I_{OCC}, and the full-load efficiency target.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \tag{19}$$

The below equation provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^{\ 2} - V_{BULK(min)}^{\ 2}\right) \times f_{LINE}} \tag{20}$$

9.2.2.7 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period, or 1 µs assuming 500-kHz resonant frequency. D_{MAX} can be determined using the equation below.

$$D_{MAX} = 1 - \left(\frac{T_R}{2} \times f_{MAX}\right) - D_{MAGCC} \tag{21}$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current, CC, operation. It is set internally by the UCC28700 at 0.425. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV}, the secondary rectifier V_F, and the cable compensation voltage (V_{OCBC}). For the 5-V USB charger applications, a turns ratio range of 13 to 15 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \tag{22}$$

Once an optimum turns ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28700 controller constant-current regulation is achieved by maintaining a maximum D_{MAG} duty cycle of 0.425 at the maximum primary current setting. The transformer turns ratio and constant-current regulating voltage determine the current sense resistor for a target constant current.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. For a 5-V, 1-A charger example, bias power of 1.5% is a good estimate. An overall transformer efficiency of 0.9 is a good estimate to include 3.5% leakage inductance, 5% core and winding loss, and 1.5% bias power.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \eta_{XFMR} \tag{23}$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output and transformer power losses are included in the equation below. Initially determine transformer primary current.

Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{24}$$

$$L_P = \frac{2(V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \tag{25}$$

The secondary winding to auxiliary winding transformer turns ratio (N_{AS}) is determined by the lowest target operating output voltage in constant-current regulation and the VDD UVLO of the UCC28700. There is additional energy supplied to VDD from the transformer leakage inductance energy which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \tag{26}$$

9.2.2.8 Standby Power Estimate

Assuming no-load standby power is a critical design parameter, determine estimated no-load power based on target converter maximum switching frequency and output power rating.

The following equation estimates the stand-by power of the converter.

$$P_{SB\_CONV} = \frac{P_{OUT} \times f_{MIN}}{\eta_{SB} \times K_{AM}^2 \times f_{MAX}} \tag{27}$$

For a typical USB charger application, the bias power during no-load is approximately 2.5 mW. This is based on 25-V VDD and 100-µA bias current. The output preload resistor can be estimated by V_{OCV} and the difference in the converter stand-by power and the bias power. The equation for output preload resistance accounts for bias power estimated at 2.5 mW.

$$R_{PL} = \frac{V_{OCV}^2}{P_{SB\_CONV} - 2.5\,mW} \tag{28}$$

Typical start-up resistance values for R_{STR} range from 13 MΩ to 20 MΩ to achieve 1-s start-up time. The capacitor bulk voltage for the loss estimation is the highest voltage for the stand-by power measurement, typically 325 V_{DC}.

$$P_{RSTR} = \frac{V_{BLK}^2}{R_{STR}} \tag{29}$$

For the total stand-by power estimation add an estimated 2.5 mW for snubber loss to the start-up resistance and converter stand-by power loss.

$$P_{SB} = P_{SB\_CONV} + P_{RSTR} + 2.5\,mW \tag{30}$$

9.2.3 Application Curves

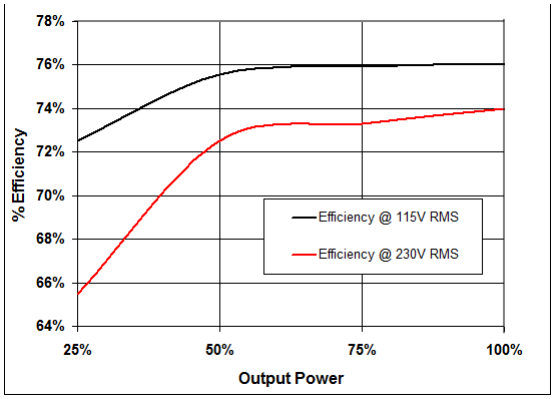


Figure 20. Efficiency

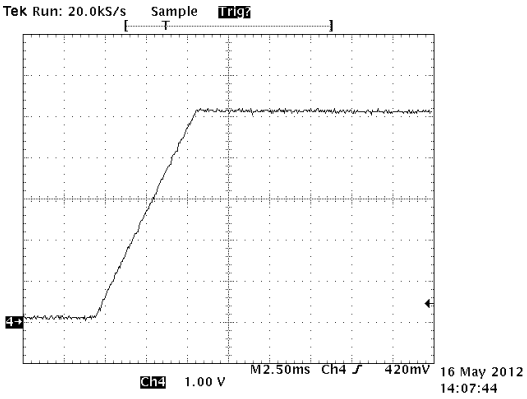


Figure 21. Output at Startup at 115-V RMS (No Load)

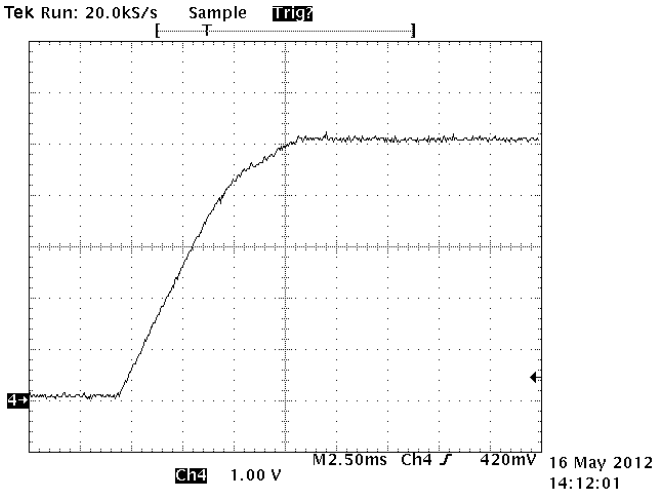


Figure 22. Output at Startup at 115-V RMS (5-Ω Load)

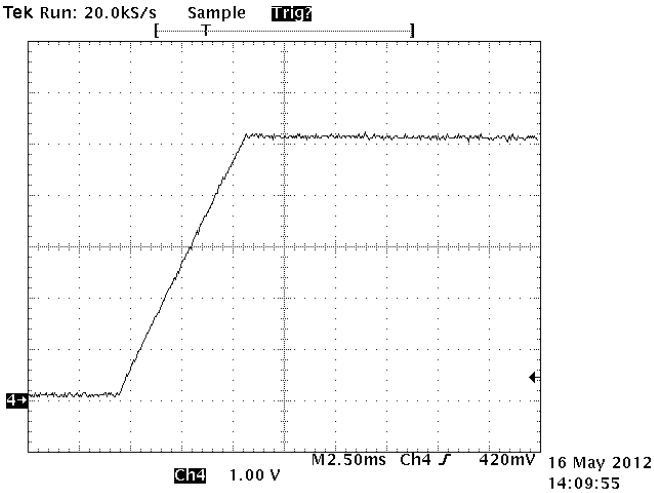


Figure 23. Output at Startup at 230-V RMS (No Load)

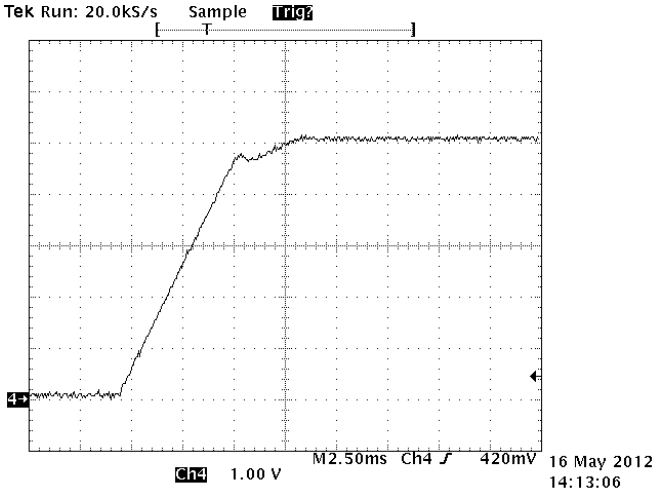
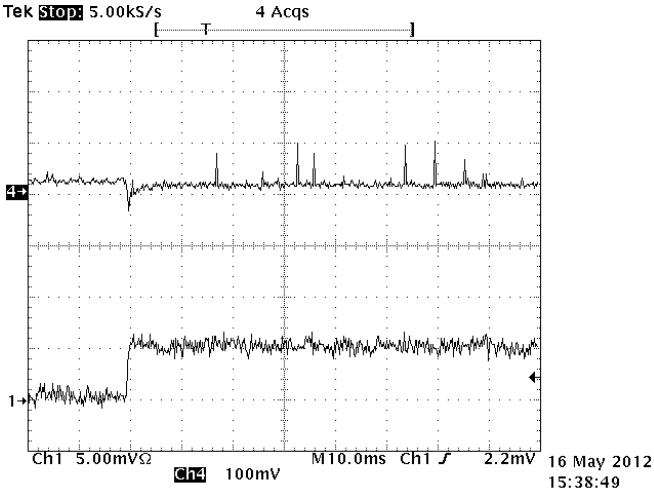
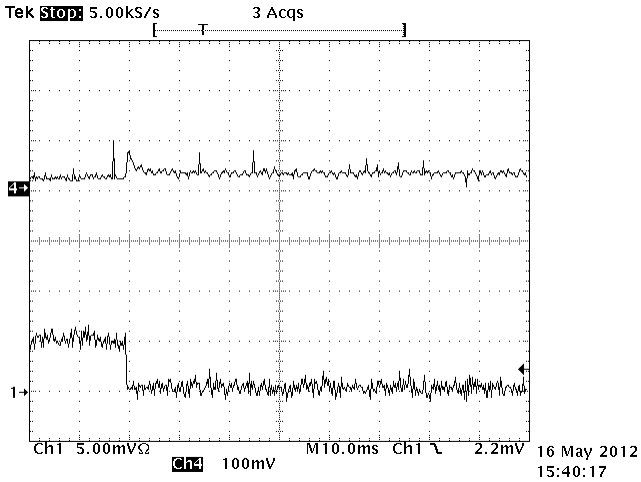


Figure 24. Output at Startup at 230-V RMS (5-Ω Load)



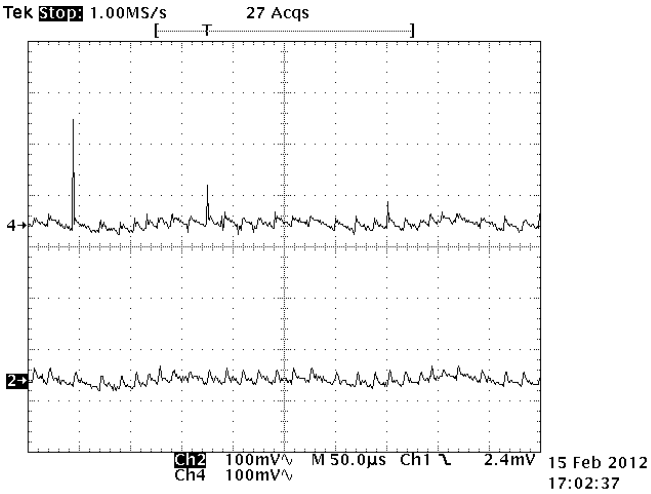
CH1 = I_O, CH4 = V_O With a 5-V Offset

Figure 25. Load Transients: (0.1-A to 0.6-A Load Step)



CH1 = I_O, CH4 = V_O With a 5-V Offset

Figure 26. Load Transients: (0.6-A to 0.1-A Load Step)



CH4 = V_O, Output voltage at EVM output

CH2 = V_O, Output voltage measured at the end of the 3M of cable in parallel with a 1-uF capacitor. The output voltage has less than 50 mV of output ripple at the end of the cable.

Figure 27. Output Ripple Voltage at Full Load

10 Power Supply Recommendations

The UCC2870X family is intended for AC/DC adapters and chargers with input voltage range of 85 $V_{AC(rms)}$ to 265 $V_{AC(rms)}$ using Flyback topology. It can be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

To maintain output current regulation over the entire input voltage range, design the converter to operate close to f_{MAX} when in full-load conditions.

To improve thermal performance increase the copper area connected to GND pins.

11 Layout

11.1 Layout Guidelines

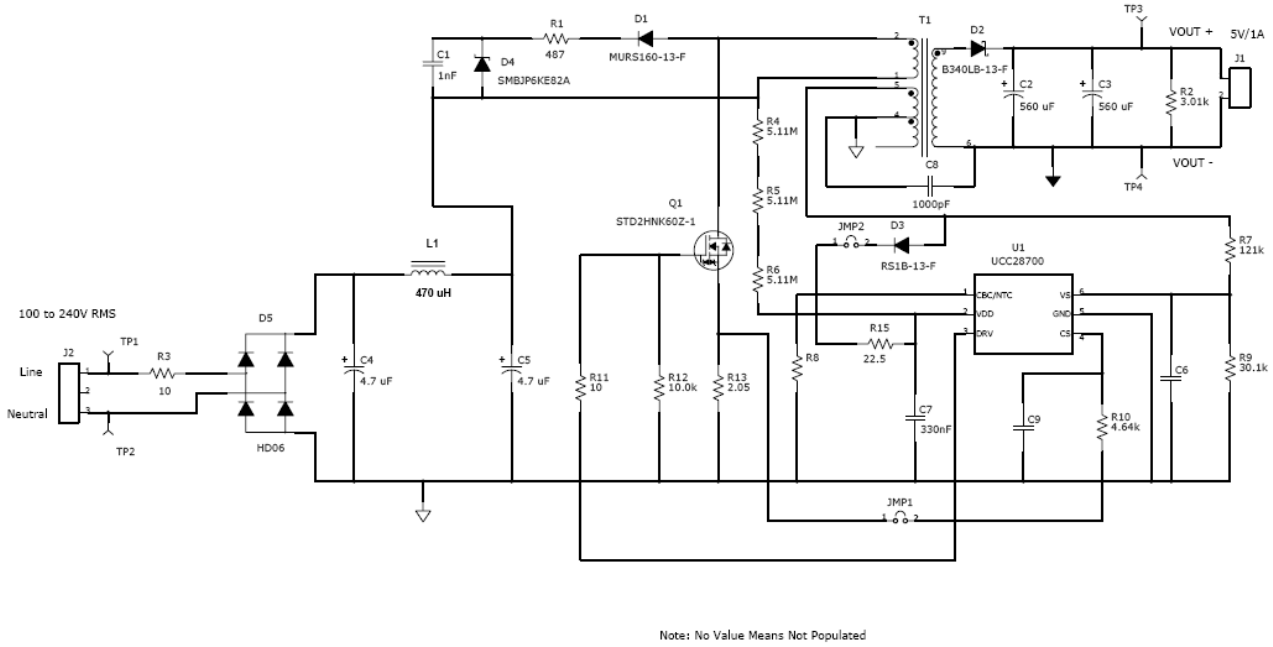


Figure 28. 5W USB Adapter Schematic

- High frequency bypass Capacitor C7 should be placed arcos Pin 2 and 5 as close as you can get it to the pins.
- Resistor R15 and C7 form a low pass filter and the connection of R15 and C7 should be as close to the VDD pin as possible.
- C9 should be put as close to CS pin and R10 as possible. This forms a low pass filter with R10.
- The connection for C9 and R10 should be as close to the CS pin as possible.
- Please note that C9 may not be required in all designs. However, it is wise to put a place holder for it in your design.
- The VS pin controls the output voltage through the transformer turns ratio and the voltage divider of R7 and R9. Note the trace with between the R7, R9 and VS pin should be; as short as; possible to reduce/eliminate possible EMI coupling.
- Note the IC ground and power ground should meet at the bulk capacitor's (C4 and C5) return. Tri to ensure that high frequency/high current from the power stage does not go through the signal ground.
  - The high frequency/high current path that you need to be cautious of on the primary is C4, C5 +, T1 (P1,P2), Q1d, Q1s, R13 to the return of C4 and C5.

Layout Guidelines (continued)

- Try to keep all high current loops as short as possible.
- Keep all high current/high frequency traces away from or perpendicular to other traces in the design.
- Traces on the voltage clamp formed by D1, R1, D4 and C4 as short as possible.
- C4 return needs to be as close to the bulk capacitor supply as possible. This reduces the magnitude of dv/dt caused by large di/dt.
- Avoid mounting semiconductors under magnetics.

11.2 Layout Example

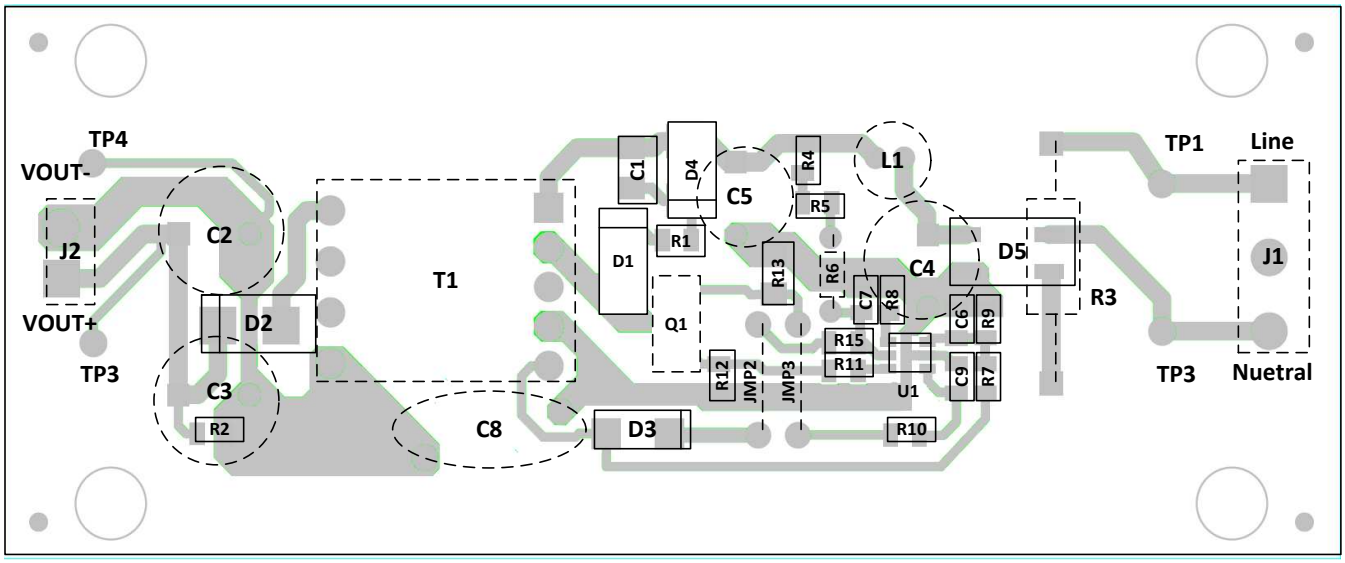


Figure 29. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

12.1.1.1 Capacitance Terms in Farads

C_{BULK} total input capacitance of C_{B1} and C_{B2}.

C_{DD} minimum required capacitance on the VDD pin.

C_{OUT} minimum output capacitance required.

12.1.1.2 Duty Cycle Terms

D_{MAGCC} secondary diode conduction duty cycle in CC, 0.425.

D_{MAX} MOSFET on-time duty cycle.

12.1.1.3 Frequency Terms in Hertz

f_{LINE} minimum line frequency.

f_{MAX} target full-load maximum switching frequency of the converter.

f_{MIN} minimum switching frequency of the converter, add 15% margin over the $f_{SW(min)}$ limit of the device.

$f_{SW(min)}$ minimum switching frequency (see the *Electrical Characteristics* table)

Device Support (continued)

12.1.1.4 Current Terms in Amperes

I_{OCC} converter output constant-current target.

$I_{PP(max)}$ maximum transformer primary current.

I_{START} start-up bias supply current (see the *Electrical Characteristics* table).

I_{TRAN} required positive load-step current.

$I_{VSL(run)}$ VS pin run current (see the *Electrical Characteristics* table).

12.1.1.5 Current and Voltage Scaling Terms

K_{AM} maximum-to-minimum peak primary current ratio (see the *Electrical Characteristics* table).

K_{LC} current-scaling constant (see the *Electrical Characteristics* table).

12.1.1.6 Transformer Terms

L_P transformer primary inductance.

N_{AS} transformer auxiliary-to-secondary turns ratio.

N_{PA} transformer primary-to-auxiliary turns ratio.

N_{PS} transformer primary-to-secondary turns ratio.

12.1.1.7 Power Terms in Watts

P_{IN} converter maximum input power.

P_{OUT} full-load output power of the converter.

P_{RSTR} VDD start-up resistor power dissipation.

P_{SB} total stand-by power.

P_{SB_CONV} P_{SB} minus start-up resistor and snubber losses.

12.1.1.8 Resistance Terms in Ω

R_{CS} primary current programming resistance

R_{ESR} total ESR of the output capacitor(s).

R_{PL} preload resistance on the output of the converter.

R_{S1} high-side VS pin resistance.

R_{S2} low-side VS pin resistance.

R_{STR} maximum start-up resistance to achieve the turn-on time target.

R_{STR} V_{DD} start-up resistance.

12.1.1.9 Timing Terms in Seconds

T_D current-sense delay including MOSFET turn-off delay; add 50 ns to MOSFET delay.

$T_{DMAG(min)}$ minimum secondary rectifier conduction time.

$T_{ON(min)}$ minimum MOSFET on time.

T_R resonant frequency during the DCM (discontinuous conduction mode) time.

T_{STR} converter start-up time requirement.

12.1.1.10 Voltage Terms in Volts

V_{BLK} highest bulk capacitor voltage for stand-by power measurement.

Device Support (continued)

$V_{BULK(min)}$ minimum voltage on C_{B1} and C_{B2} at full power.

V_{OCBC} target cable compensation voltage at the output terminals.

$V_{CBC(max)}$ maximum voltage at the CBC pin at the maximum converter output current (see the *Electrical Characteristics* table).

V_{CCR} constant-current regulating voltage (see the *Electrical Characteristics* table).

$V_{CST(max)}$ CS pin maximum current-sense threshold (see the *Electrical Characteristics* table).

$V_{CST(min)}$ CS pin minimum current-sense threshold (see the *Electrical Characteristics* table).

$V_{DD(off)}$ UVLO turn-off voltage (see the *Electrical Characteristics* table).

$V_{DD(on)}$ UVLO turn-on voltage (see the *Electrical Characteristics* table).

$V_{O\Delta}$ output voltage drop allowed during the load-step transient.

V_{DSPK} peak MOSFET drain-to-source voltage at high line.

V_F secondary rectifier forward voltage drop at near-zero current.

V_{FA} auxiliary rectifier forward voltage drop.

V_{LK} estimated leakage inductance energy reset voltage.

V_{OCV} regulated output voltage of the converter.

V_{OCC} target lowest converter output voltage in constant-current regulation.

V_{REV} peak reverse voltage on the secondary rectifier.

V_{RIPPLE} output peak-to-peak ripple voltage at full-load.

V_{VSR} CV regulating level at the VS input (see the *Electrical Characteristics* table).

12.1.1.11 AC Voltage Terms in V_{RMS}

$V_{IN(max)}$ maximum input voltage to the converter.

$V_{IN(min)}$ minimum input voltage to the converter.

$V_{IN(run)}$ converter input start-up (run) voltage.

12.1.1.12 Efficiency Terms

η_{SB} estimated efficiency of the converter at no-load condition, not including start-up resistance or bias losses. For a 5-V USB charger application, 60% to 65% is a good initial estimate.

η converter overall efficiency.

η_{XFMR} transformer primary-to-secondary power transfer efficiency.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Using the UCC28700EVM-068, Evaluation Module, SLUU968

12.2.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Documentation Support (continued)

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC28700	Click here	Click here	Click here	Click here	Click here
UCC28701	Click here	Click here	Click here	Click here	Click here
UCC28702	Click here	Click here	Click here	Click here	Click here
UCC28703	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28700DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U700	Samples
UCC28700DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U700	Samples
UCC28701DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U701	Samples
UCC28701DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U701	Samples
UCC28702DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U702	Samples
UCC28702DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U702	Samples
UCC28703DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U703	Samples
UCC28703DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 125	U703	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC28700 :

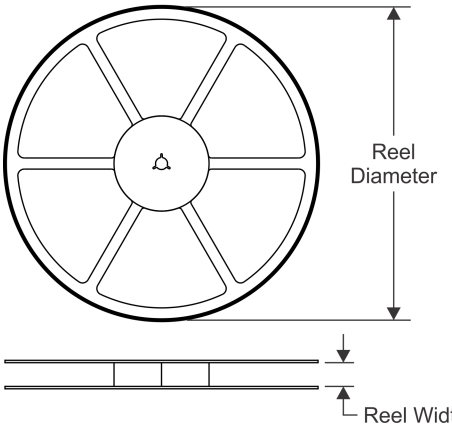
- Automotive: UCC28700-Q1

NOTE: Qualified Version Definitions:

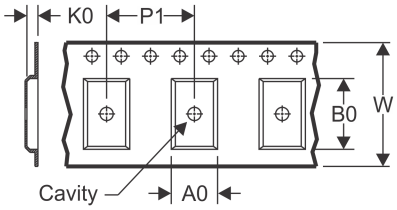
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

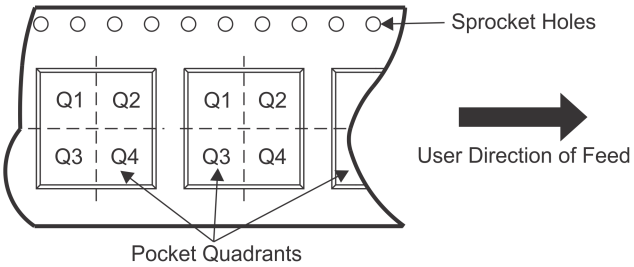


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

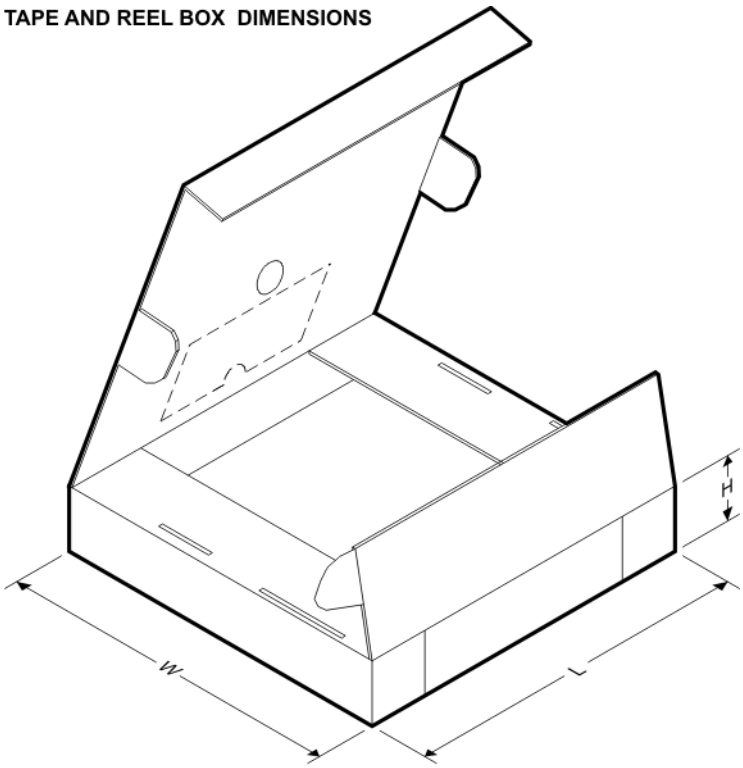
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

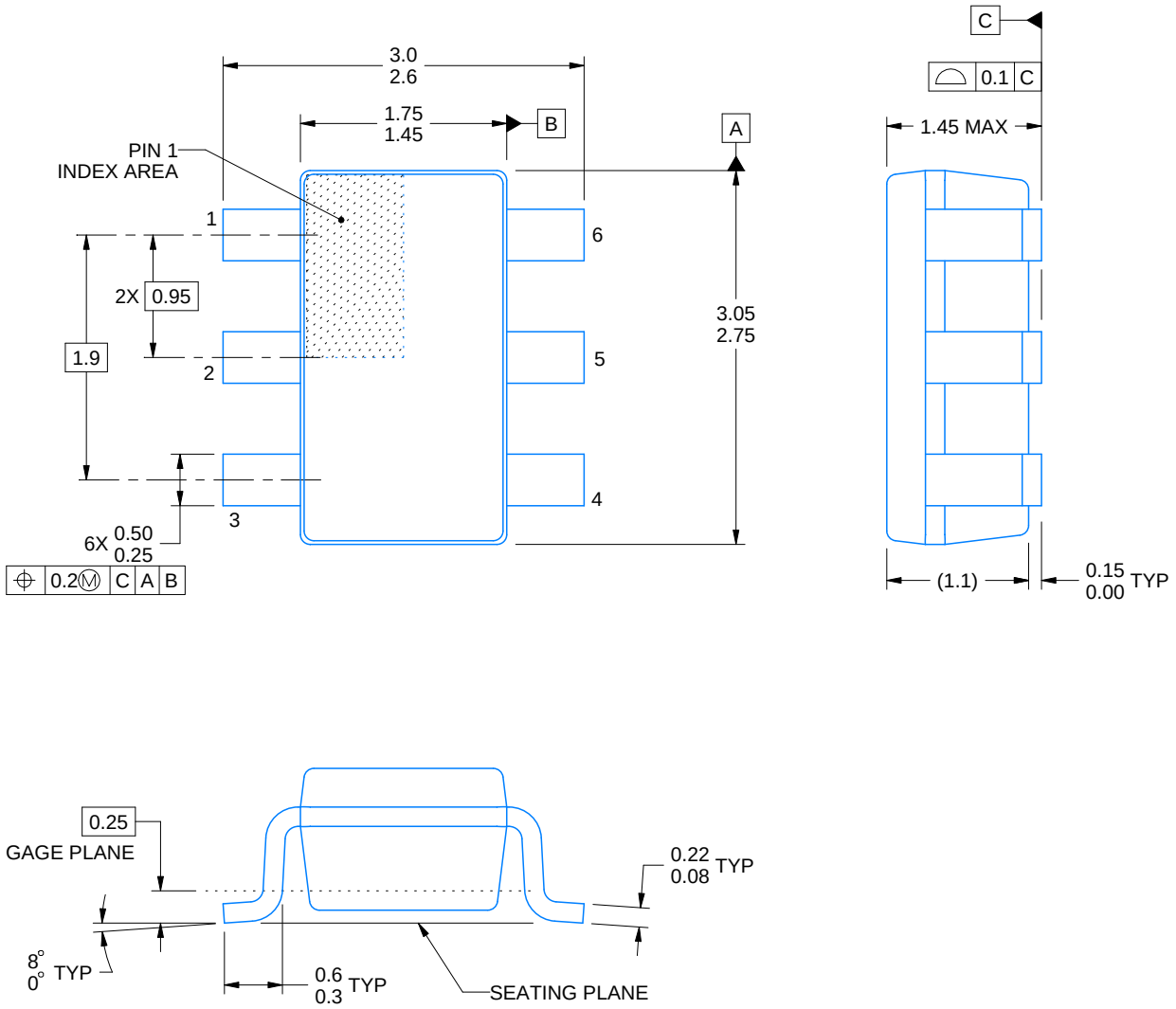
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28700DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28700DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28701DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28701DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28702DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28702DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28703DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28703DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

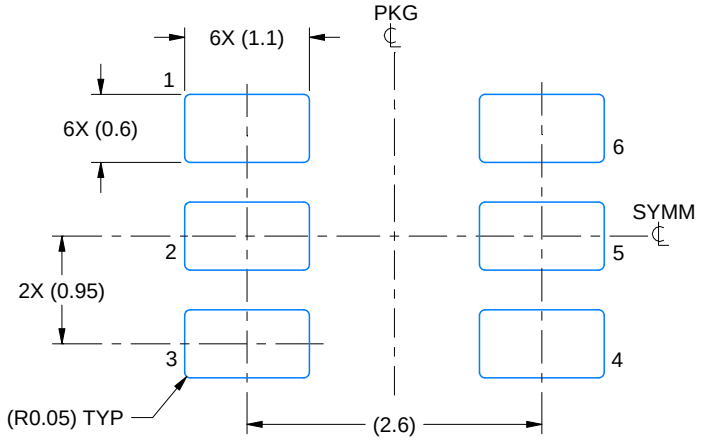
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28700DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28700DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC28701DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28701DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC28702DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28702DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC28703DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28703DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0



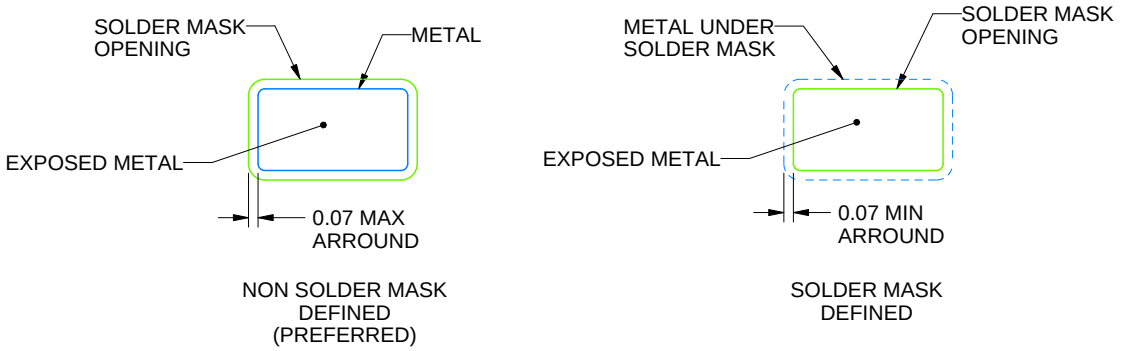
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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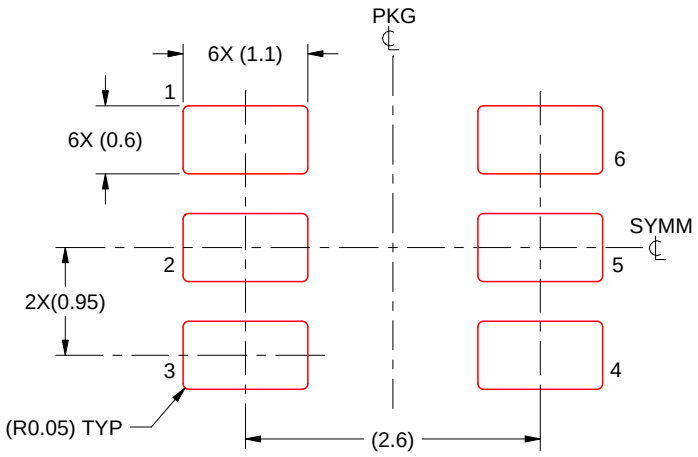
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

XC6206 Series

ETR0305_008

Low ESR Cap.Compatible Positive Voltage Regulators

■GENERAL DESCRIPTION

The XC6206 series are highly precise, low power consumption, 3 terminal, positive voltage regulators manufactured using CMOS and laser trimming technologies. The series provides large currents with a significantly small dropout voltage.
The XC6206 consists of a current limiter circuit, a driver transistor, a precision reference voltage and an error correction circuit. The series is compatible with low ESR ceramic capacitors. The current limiter's foldback circuit operates as a short circuit protection as well as the output current limiter for the output pin.
Output voltages are internally by laser trimming technologies. It is selectable in 0.1V increments within a range of 1.2V to 5.0V. SOT-23, SOT-89 and USP-6B packages are available.

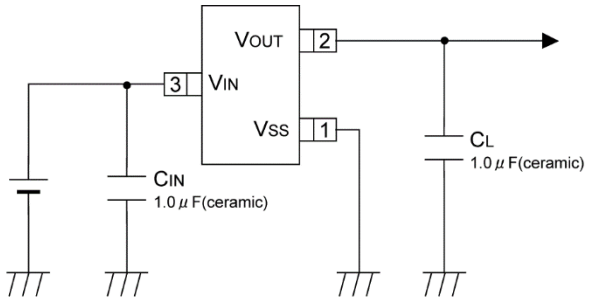
■APPLICATIONS

- Smart phones / Mobile phones
- Portable game consoles
- Digital still cameras / Camcorders
- Digital audio equipments
- Reference voltage sources
- Multi-function power supplies

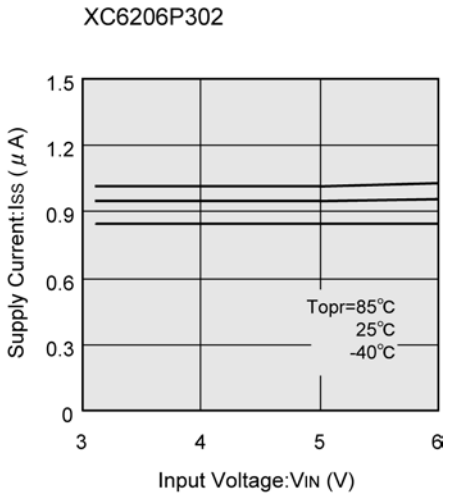
■FEATURES

Maximum Output Current	: 200mA (3.0V type)
Dropout Voltage	: 250mV @ 100mA (3.0V type)
Maximum Operating Voltage	: 6.0V
Output Voltage Range	: 1.2V ~ 5.0V (0.1V increments)
Highly Accurate	: ±2%@V_{OUT}≧1.5V ±30mV@V_{OUT}<1.5V (±1% @V_{OUT}≧2.0V)
Low Power Consumption	: 1.0μA (TYP.)
Low ESR Capacitor	: Ceramic capacitor compatible
Protection	: Current Limit Circuit Built-in
Operating Ambient Temperature	: -40℃~ +85℃
Packages	: SOT-23 SOT-89 USP-6B
Environmentally Friendly	: EU RoHS Compliant, Pb Free

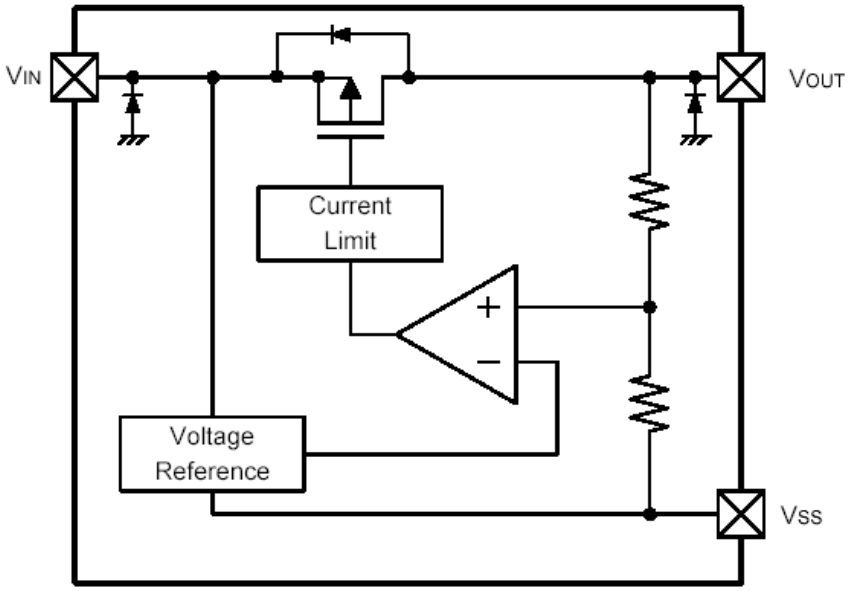
■TYPICAL APPLICATION CIRCUIT



■TYPICAL PERFORMANCE CHARACTERISTICS



■BLOCK DIAGRAM



*Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■PRODUCT CLASSIFICATION

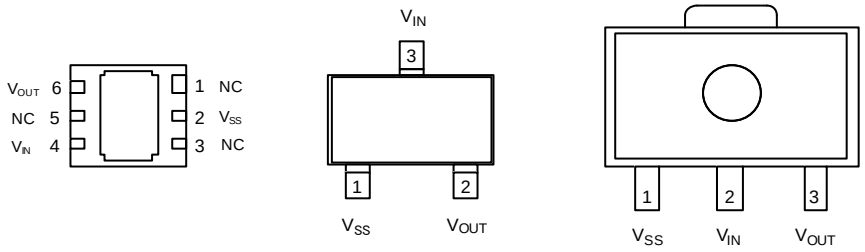
●Ordering Information

XC6206P①②③④⑤−⑥ (*1)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①②	Output Voltage	12~50	e.g. VOUT: 3.0V→①=3, ②=0
③	Accuracy	2	±2% (VOUT≧1.5V), ±30mV (VOUT<1.5V)
		1	±1% (VOUT≧2.0V)
④⑤−⑥	Packages (Order Unit)	MR	SOT-23 (3,000pcs/Reel)
		MR-G	SOT-23 (3,000pcs/Reel)
		PR	SOT-89 (1,000pcs/Reel)
		PR-G	SOT-89 (1,000pcs/Reel)
		DR	USP-6B (3,000pcs/Reel)
		DR-G	USP-6B (3,000pcs/Reel)

(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

■PIN CONFIGURATION



USP-6B
(BOTTOM VIEW)

SOT-23
(TOP VIEW)

SOT-89
(TOP VIEW)

*The dissipation pad for the USP-6B package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release.
If the pad needs to be connected to other pins, it should be connected to the pin number 4 (V_{IN}).

■PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTIONS
SOT-23	SOT-89	USP-6B		
1	1	2	VSS	Ground
3	2	4	VIN	Power Input
2	3	6	VOUT	Output
-	-	1, 3, 5	NC	No Connection

■ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		VIN	-0.3～+7.0	V
Output Current		IOUT	500 (*1)	mA
Output Voltage		VOUT	-0.3 ~ V_{IN} + 0.3	V
Power Dissipation	SOT-23	Pd	250	mW
			500(40mm x 40mm Standard board) (*2)	
	SOT-89		500	
			1000(40mm x 40mm Standard board) (*2)	
	USP-6B		120	
			1000(40mm x 40mm Standard board) (*2)	
Operating Ambient Temperature		Topr	- 40 ~ + 85	°C
Storage Temperature		Tstg	- 55 ~ + 125	°C

(*1) $I_{OUT} \leqq Pd / (V_{IN}-V_{OUT})$
(*2) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

■ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage (Standard)(*2)	$V_{OUT(E)}$(*3)	I_{OUT}=30mA	$V_{OUT(T)}$<1.5V	-0.03	$V_{OUT(T)}$(*4)	+0.03	V	②
			$V_{OUT(T)}$≧1.5V	×0.98		×1.02		
Output Voltage (High Accuracy)(*2)		I_{OUT}=30mA	$V_{OUT(T)}$≧2.0V	×0.99		×1.01		
Supply Current	I_{DD}			-	1.0	3.0	μA	①
Load Regulation	ΔV_{OUT}	$V_{OUT(T)}$≦1.8V, 1mA≦I_{OUT}≦50mA		-	-	E-1(*5)	mV	②
		$V_{OUT(T)}$>1.8V, 1mA≦I_{OUT}≦100mA						
Dropout Voltage 1	Vdif1(*6)	I_{OUT}=30mA		-	E-2(*5)		mV	②
Dropout Voltage 2	Vdif2(*6)	$V_{OUT(T)}$≦1.8V, I_{OUT}=60mA		-	E-3(*5)			
		$V_{OUT(T)}$>1.8V, I_{OUT}=100mA						
Line Regulation	ΔV_{OUT}/ (ΔV_{IN}・V_{OUT})	$V_{OUT(T)}$<4.5V, $V_{OUT(T)}$+1.0V≦V_{IN}≦6.0V, I_{OUT}=30mA		-	0.05	0.25	%/V	②
		$V_{OUT(T)}$≧4.5V, 5.5V≦V_{IN}≦6.0V, I_{OUT}=30mA						
Maximum Output Current	I_{OUTMAX}	V_{OUT}≧$V_{OUT(E)}$× 0.9		E-4(*5)	-	-	mA	②
Short Circuit Current	I_{SHORT}	V_{OUT}=V_{SS}		-	E-5(*5)	-	mA	②
Input Voltage	V_{IN}			1.8	-	6.0	V	②
Output Voltage Temperature Characteristics	ΔV_{OUT}/ (ΔTopr・V_{OUT})	I_{OUT}=30mA, -40℃≦Topr≦85℃		-	±100	-	ppm/℃	②

*1: Unless otherwise stated, V_{IN} = $V_{OUT(T)}$ + 1.0V
*2: (Standard):±2% (1.5V≦$V_{OUT(T)}$) , ±0.03V (1.5V>$V_{OUT(T)}$)
(High Accuracy):±1% (2.0V≦$V_{OUT(T)}$)
*3: $V_{OUT(E)}$:Effective output voltage.
*4: $V_{OUT(T)}$:Nominal voltage
*5: For E-1,E-2,E-3,E-4,E-5, Please refer to Electrical Characteristics Chart.
*6: Vdif =V_{IN1} -V_{OUT1}
V_{OUT1} :A voltage equal to 98% of the output voltage whenever an amply stabilized {$V_{OUT(T)}$ + 1.0V} is input with each I_{OUT}.
V_{IN1} :The input voltage when V_{OUT1} appears as input voltage is gradually decreased.
*7: The low ESR capacitors use that is more than 1.0μF as C_L is possible.

■ELECTRICAL CHARACTERISTICS (Continued)

●Electrical Characteristics Chart

<table>
<tr><th rowspan="4">NOMINAL VOLTAGE</th><th>E-1</th><th colspan="2">E-2</th><th colspan="2">E-3</th><th>E-4</th><th>E-5</th></tr>
<tr><th>LOAD REGULATION</th><th colspan="2">DROPOUT VOLTAGE1</th><th colspan="2">DROPOUT VOLTAGE2</th><th>MAX. OUTPUT CURRENT</th><th>SHORT CURRENT</th></tr>
<tr><th>ΔV_{OUT} (mV)</th><th colspan="2">V_{dif1} (mV)</th><th colspan="2">V_{dif2} (mV)</th><th>I_{OUTMAX} (mA)</th><th>I_{SHORT} (mA)</th></tr>
<tr><th>$V_{OUT(T)}$</th><th>MAX.</th><th>TYP.</th><th>MAX.</th><th>TYP.</th><th>MAX.</th><th>MIN.</th><th>TYP.</th></tr>
<tr><td>1.2</td><td rowspan="3">40</td><td>460</td><td>760</td><td rowspan="2">700</td><td rowspan="2">960</td><td rowspan="4">60</td><td rowspan="3">180</td></tr>
<tr><td>1.3</td><td>400</td><td>650</td></tr>
<tr><td>1.4</td><td>350</td><td>590</td><td rowspan="2">580</td><td rowspan="2">860</td></tr>
<tr><td>1.5</td><td rowspan="5">45</td><td>300</td><td>510</td><td rowspan="3">155</td></tr>
<tr><td>1.6</td><td>250</td><td>450</td><td rowspan="2">450</td><td rowspan="2">810</td><td rowspan="4">80</td></tr>
<tr><td>1.7</td><td>200</td><td>410</td></tr>
<tr><td>1.8</td><td>150</td><td>390</td><td rowspan="6">350</td><td rowspan="2">780</td><td rowspan="5">130</td></tr>
<tr><td>1.9</td><td rowspan="9">100</td><td rowspan="9">370</td></tr>
<tr><td>2.0</td><td rowspan="5">50</td><td rowspan="4">120</td></tr>
<tr><td>2.1</td><td rowspan="8">710</td></tr>
<tr><td>2.2</td></tr>
<tr><td>2.3</td><td rowspan="9">100</td></tr>
<tr><td>2.4</td></tr>
<tr><td>2.5</td><td rowspan="5">55</td><td rowspan="5">150</td></tr>
<tr><td>2.6</td></tr>
<tr><td>2.7</td></tr>
<tr><td>2.8</td></tr>
<tr><td>2.9</td></tr>
<tr><td>3.0</td><td rowspan="5">60</td><td rowspan="9">75</td><td rowspan="9">350</td><td rowspan="9">250</td><td rowspan="9">680</td><td rowspan="9">200</td></tr>
<tr><td>3.1</td></tr>
<tr><td>3.2</td></tr>
<tr><td>3.3</td></tr>
<tr><td>3.4</td></tr>
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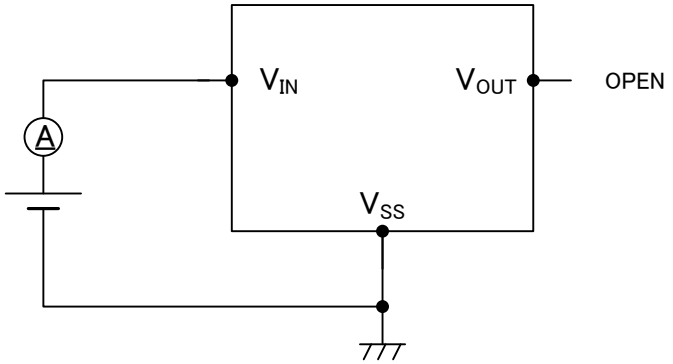
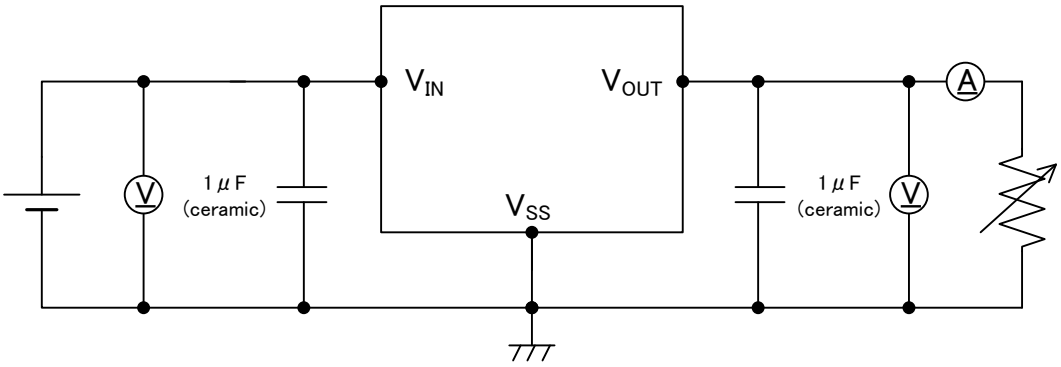
<tr><td>3.6</td></tr>
<tr><td>3.7</td></tr>
<tr><td>3.8</td></tr>
<tr><td>3.9</td></tr>
<tr><td>4.0</td><td rowspan="5">70</td><td rowspan="10">60</td><td rowspan="10">320</td><td rowspan="10">200</td><td rowspan="10">630</td><td rowspan="10">250</td></tr>
<tr><td>4.1</td></tr>
<tr><td>4.2</td></tr>
<tr><td>4.3</td></tr>
<tr><td>4.4</td></tr>
<tr><td>4.5</td><td rowspan="5">75</td></tr>
<tr><td>4.6</td></tr>
<tr><td>4.7</td></tr>
<tr><td>4.8</td></tr>
<tr><td>4.9</td></tr>
<tr><td>5.0</td><td>80</td><td>50</td><td>290</td><td>175</td><td>600</td></tr>
</table>

■TEST CIRCUITS

Circuit ①



Circuit ②



■NOTES ON USE

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please strengthen V_{IN} and V_{SS} wiring in particular

3. Please wire the input capacitor (C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

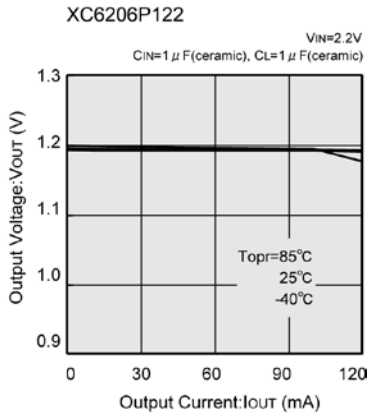
4. Capacitances of these capacitors (C_{IN}, C_L) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.

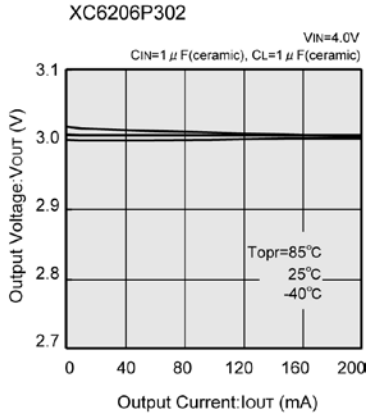
5. When it is used in a quite small input / output dropout voltage, output may go into unstable operation. Please test it thoroughly before using it in production.

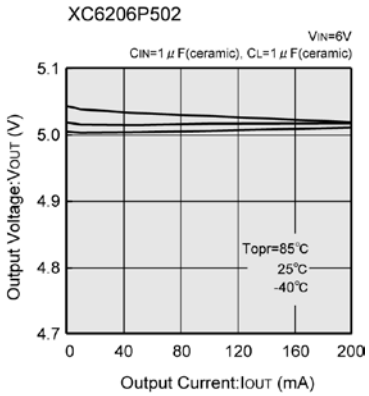
6. Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

■TYPICAL PERFORMANCE CHARACTERISTICS

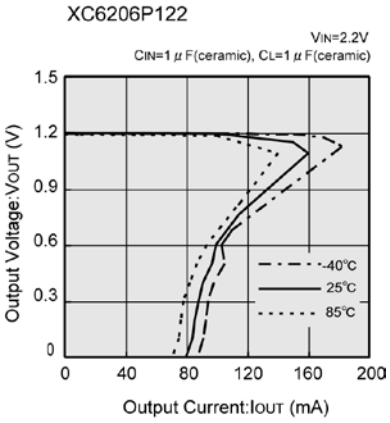
(1) Output Voltage vs. Output Current

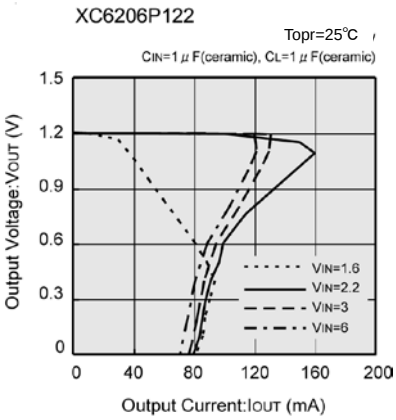


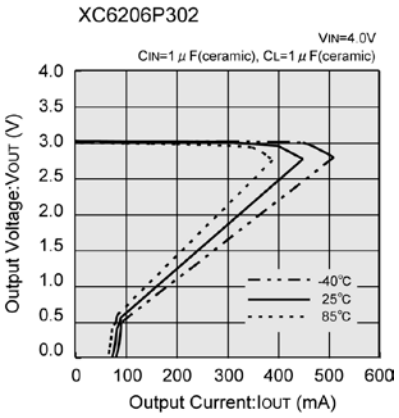


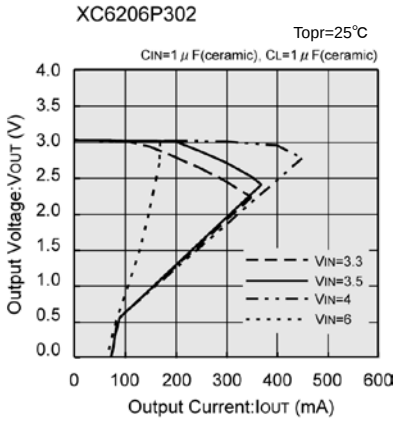


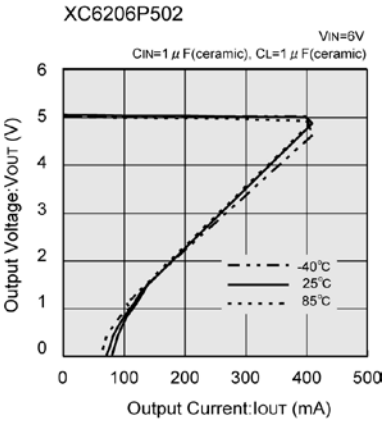
(2) Current Limit

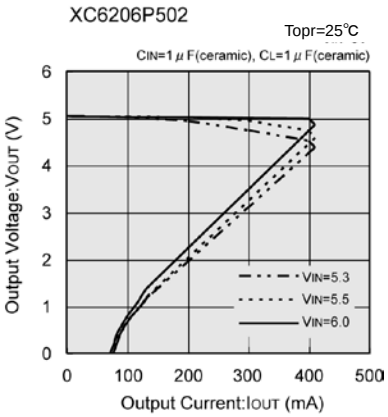






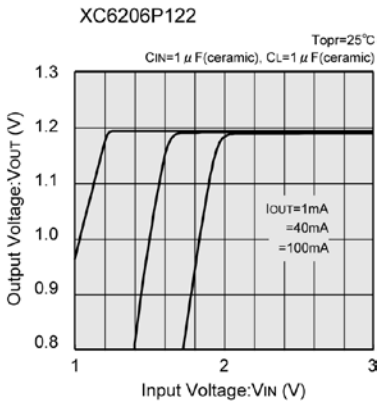


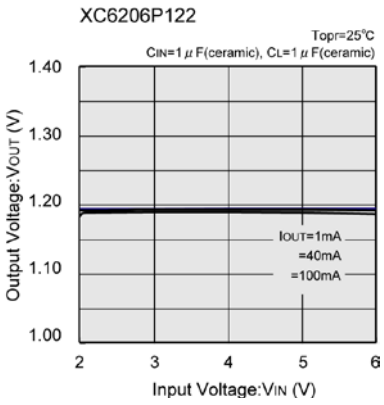


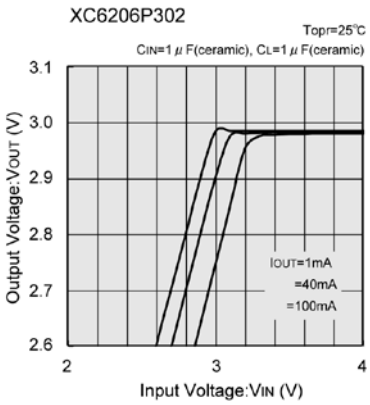


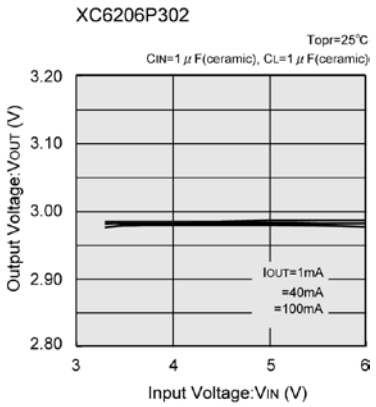
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

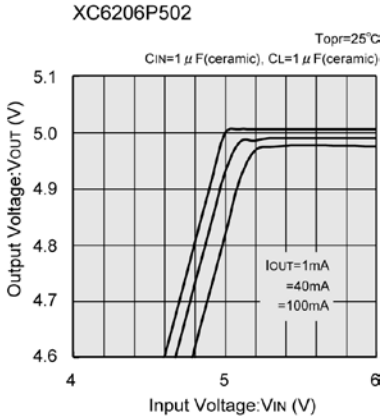
(3) Output Voltage vs. Input Voltage

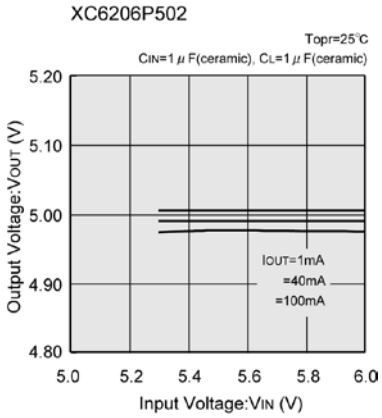




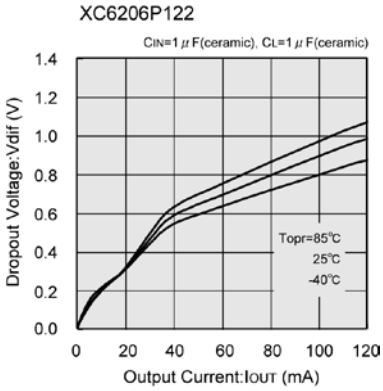


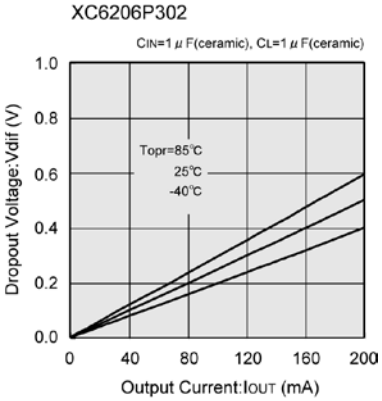


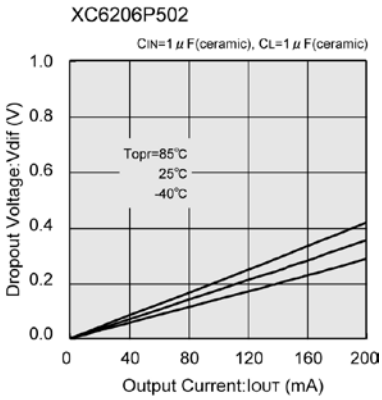




(4) Dropout Voltage vs. Output Current



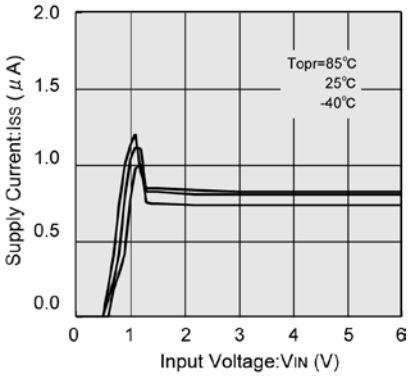




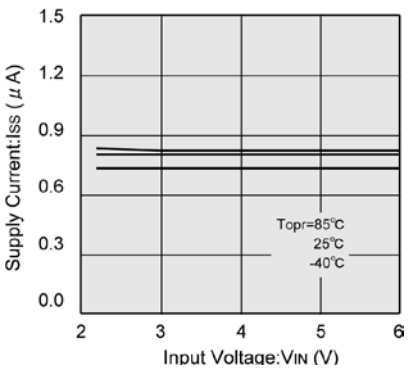
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(5) Supply Current vs. Input Voltage

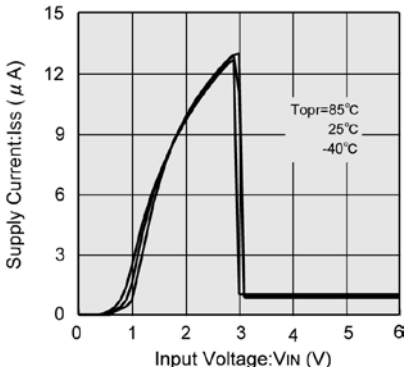
XC6206P122



XC6206P122



XC6206P302



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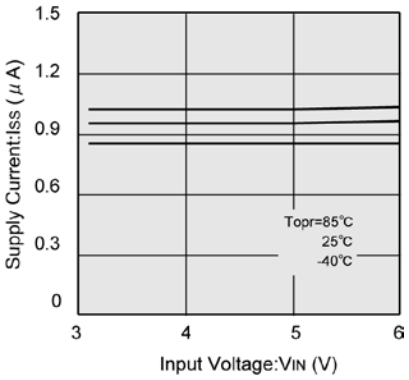
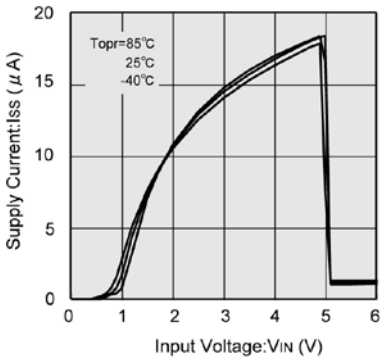


XC6206P502



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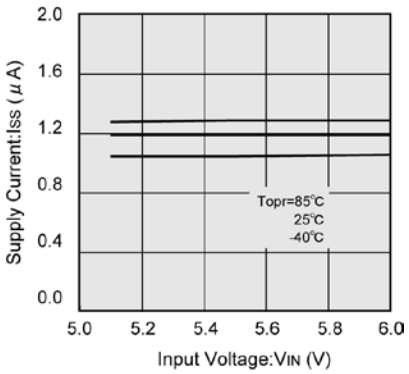
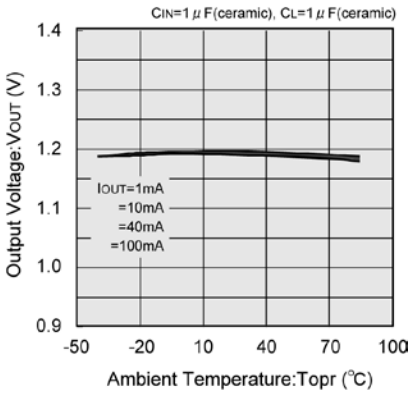


(6) Output Voltage vs. Ambient Temperature

XC6206P122



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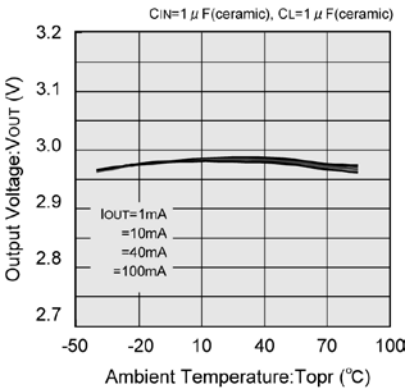

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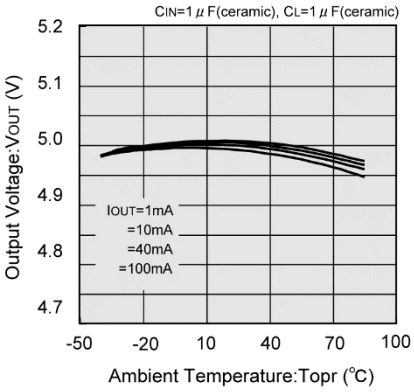
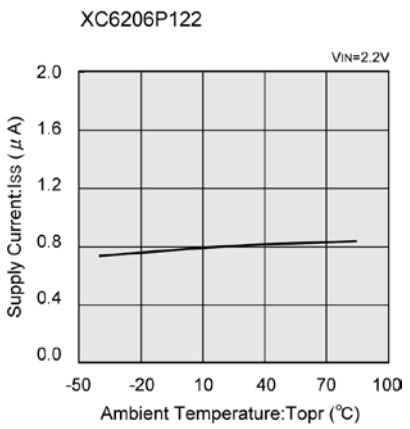
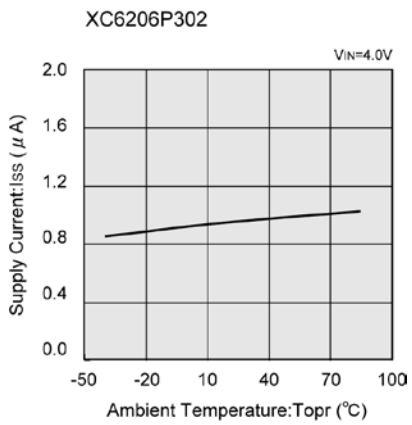
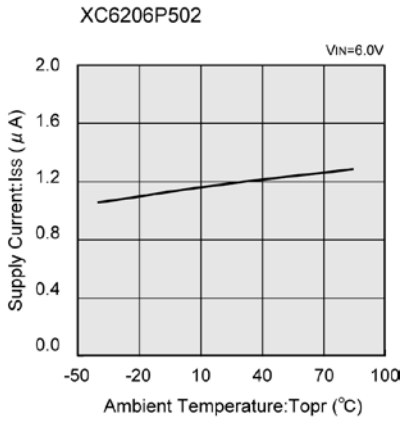


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

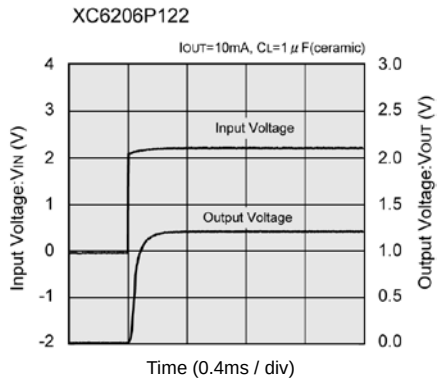
(7) Output Voltage vs. Ambient Temperature

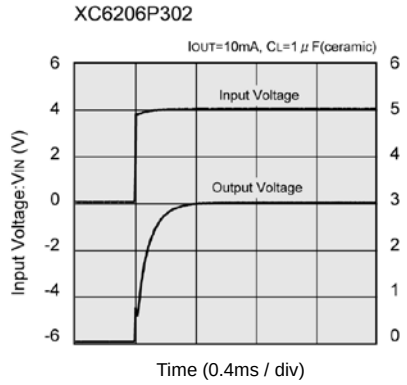


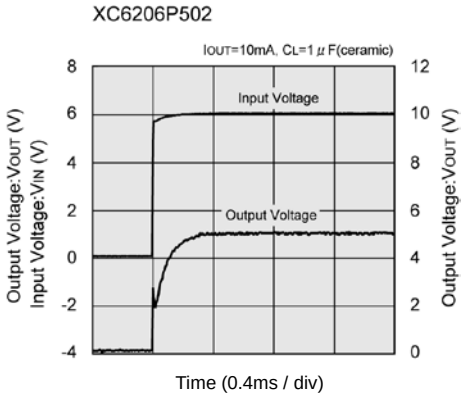




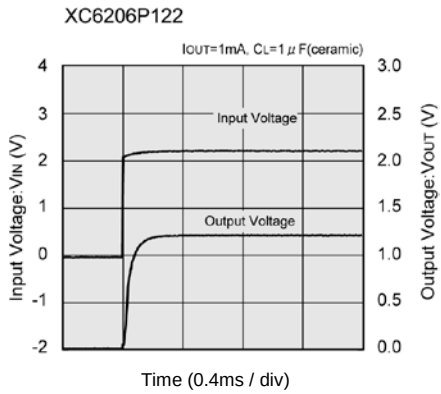
(8) Input Transient Response 1

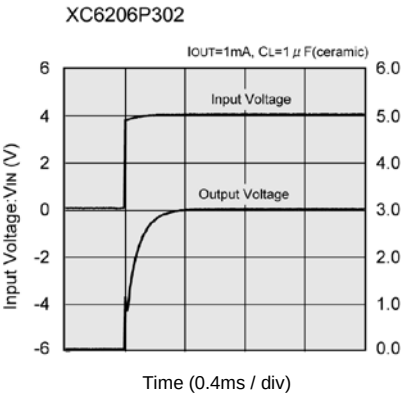


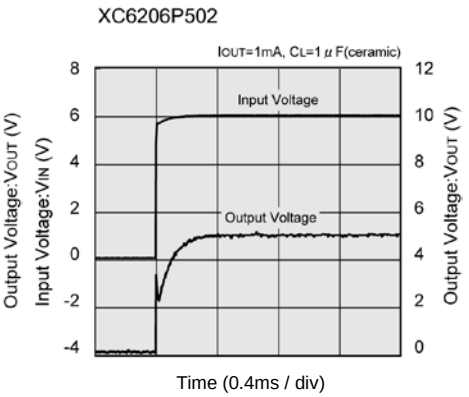




XC6206P122

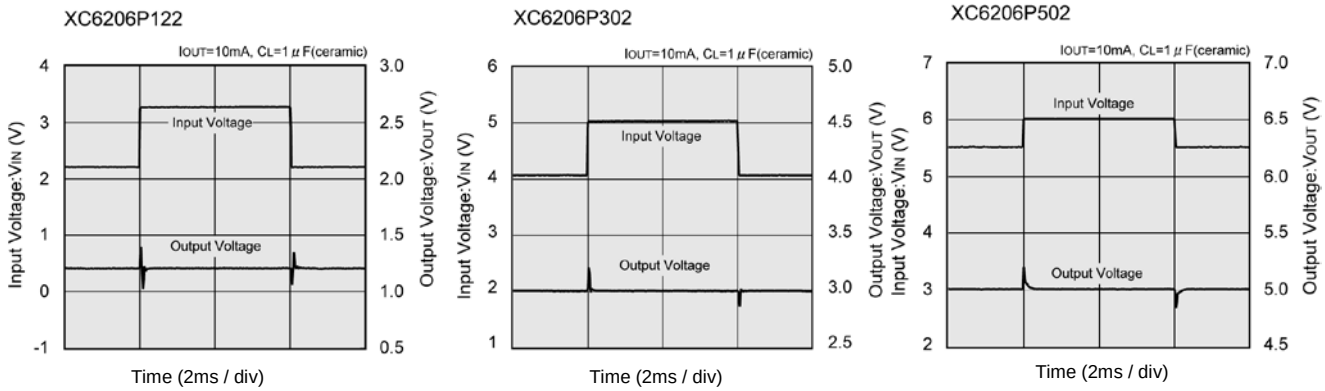


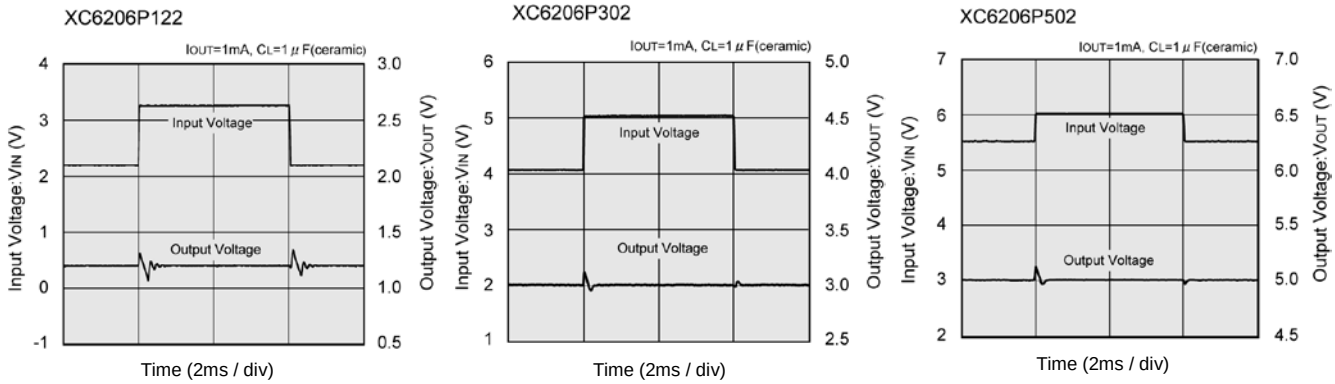




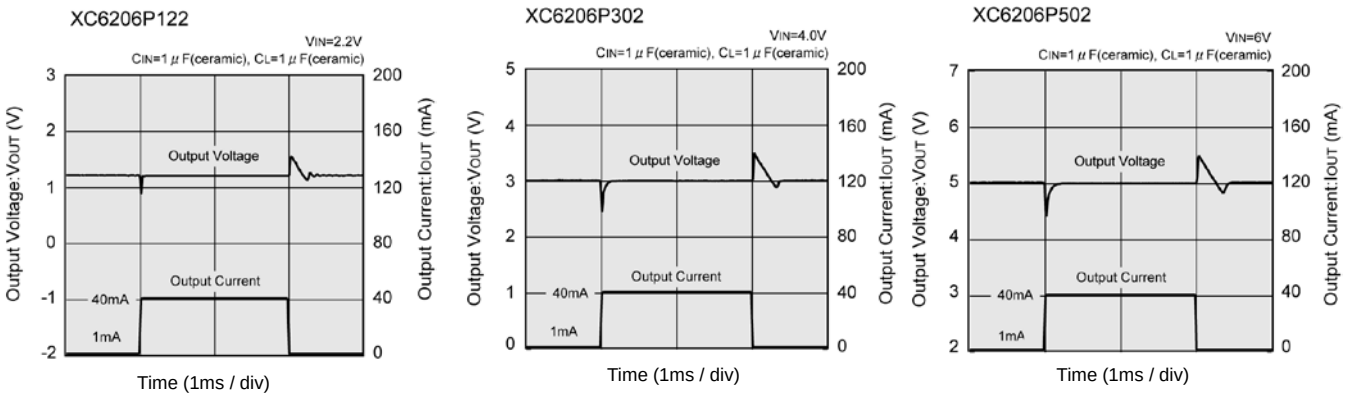
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(9) Input Transient Response 2



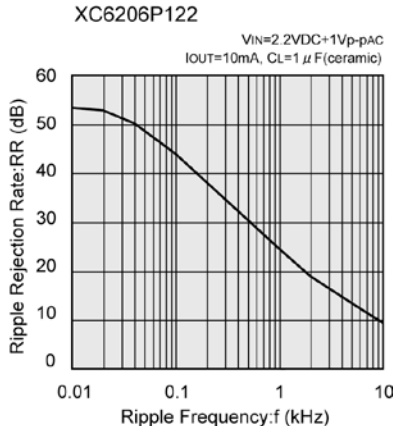


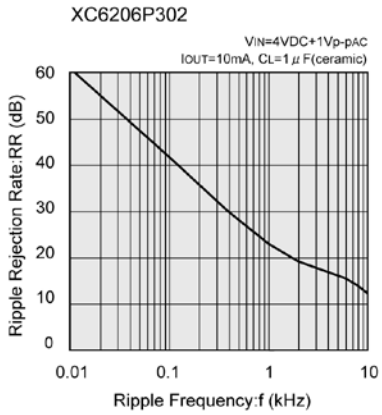
(10) Load Transient Response

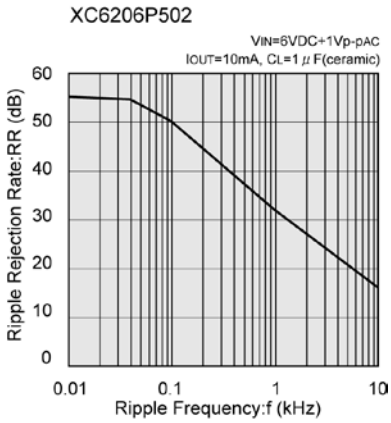


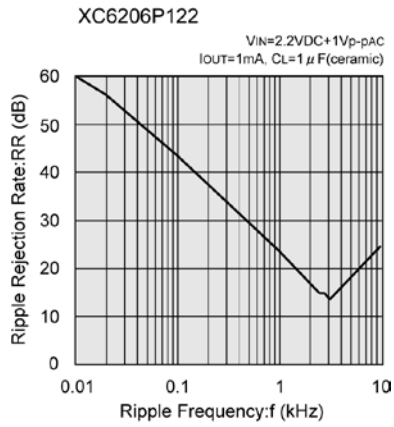
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

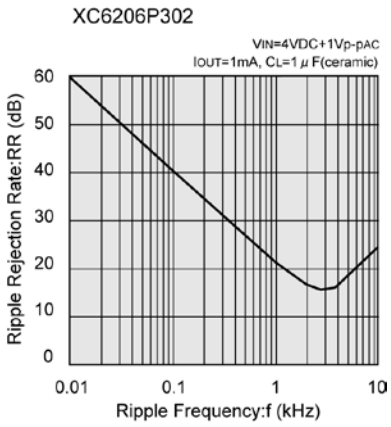
(11) Ripple Rejection Rate

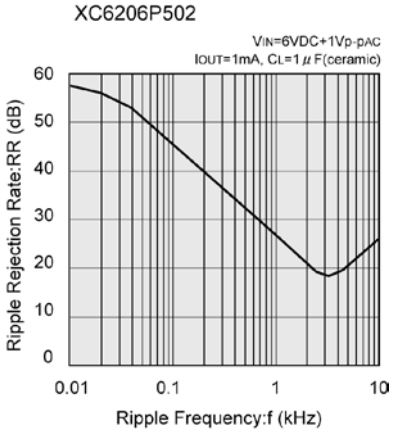












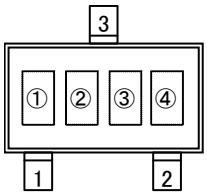
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

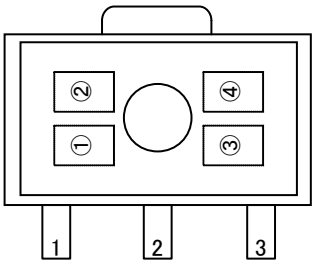
PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS	
SOT-23	SOT-23 PKG	Standard Board	SOT-23 Power Dissipation
SOT-89	SOT-89 PKG	Standard Board	SOT-89 Power Dissipation
USP-6B	USP-6B PKG	Standard Board	USP-6B Power Dissipation

■MARKING RULE

●SOT-23, SOT-89



SOT-23
(TOP VIEW)



SOT-89
(TOP VIEW)

① represents product number

MARK	PRODUCT SERIES
6	XC6206P*****

② represents 3 pins regulator

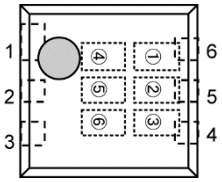
MARK		PRODUCT SERIES
VOLTAGE＝0.1 ~ 3.0V	VOLTAGE＝3.1 ~ 6.0V	
5	6	XC6206P*****

③ represents output voltage

MARK	VOLTAGE (V)			MARK	OUTPUT VOLTAGE (V)		
0	-	3.1	-	F	1.6	4.6	-
1	-	3.2	-	H	1.7	4.7	-
2	-	3.3	-	K	1.8	4.8	-
3	-	3.4	-	L	1.9	4.9	-
4	-	3.5	-	M	2.0	5.0	-
5	-	3.6	-	N	2.1	-	-
6	-	3.7	-	P	2.2	-	-
7	-	3.8	-	R	2.3	-	-
8	-	3.9	-	S	2.4	-	-
9	-	4.0	-	T	2.5	-	-
A		4.1	-	U	2.6	-	-
B	1.2	4.2	-	V	2.7	-	-
C	1.3	4.3	-	X	2.8	-	-
D	1.4	4.4	-	Y	2.9	-	-
E	1.5	4.5	-	Z	3.0	-	-

④ represents production lot number
0 to 9, A to Z repeated. (G, I, J, O, Q, W excluded)

●USP-6B



USP-6B
(TOP VIEW)

①② represents product number

MARK		PRODUCT SERIES
①	②	
0	6	XC6206P***D*

③ represents 3 pins regulator

MARK	PRODUCT SERIES
P	XC6206P***D*

④⑤ represents output voltage

MARK		OUTPUT VOLTAGE(V)	PRODUCT SERIES
④	⑤		
3	3	3.3	XC6206P33*D*
5	0	5.0	XC6206P50*D*

⑥ represents production lot number
0 to 9, A to Z repeated. (G, I, J, O, Q, W excluded)

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.

TPS55340-Q1 Integrated 5-A, Wide Input Range Boost, SEPIC, or Flyback DC/DC Converter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Internal 5-A, 40-V Low-Side MOSFET Switch
- 2.9 to 38-V Input Voltage Range
- ±0.7% Reference Voltage
- 0.5-mA Operating Quiescent Current
- 2.7-µA Shutdown Supply Current
- Fixed-Frequency Current Mode PWM Control
- Frequency Adjustable from 100 kHz to 2.5 MHz (see *Switching Frequency*)
- Synchronization Capability to External Clock
- Adjustable Soft-Start Time
- Pulse-Skipping for Higher Efficiency at Light Loads
- Cycle-by-Cycle Current-Limit, Thermal Shutdown, and UVLO Protection
- WQFN-16 (3 mm × 3 mm) Package with PowerPad™
- Wide –40°C to +150°C Operating T_J Range
- Create a Custom Design Using the TPS55340-Q1 with the WEBENCH Power Designer

2 Applications

- Boost, SEPIC, and Flyback Topologies
- Automotive Pre-Boost Applications to Support Start-Stop Requirements
- USB Power Delivery
- Industrial Power Systems

3 Description

The TPS55340-Q1 device is a monolithic non-synchronous switching converter with integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC and isolated flyback. The device has a wide input voltage range to support applications with input voltage from 2.9 to 38-V.

The TPS55340-Q1 device regulates the output voltage with current mode PWM (pulse width modulation) control, and has an internal oscillator. The switching frequency of PWM is set by either an external resistor or by synchronizing to an external clock signal. The user can program the switching frequency from 100 kHz to 2.5 MHz.

The device features a programmable soft-start function to limit inrush current during start-up and has other built-in protection features including cycle-by-cycle over current-limit and thermal shutdown.

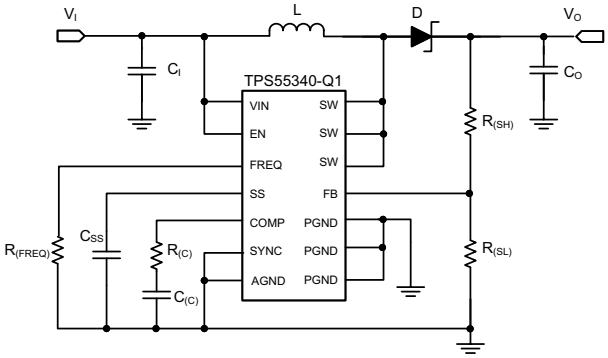
The TPS55340-Q1 device is available in a small 3-mm × 3-mm 16-pin WQFN package with PowerPad for enhanced thermal performance.

Device Information(1)

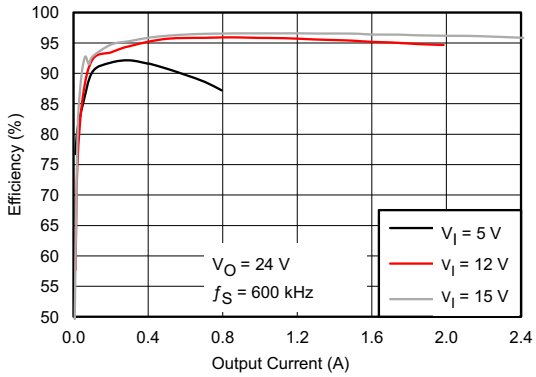
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS55340-Q1	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application for Boost



Efficiency vs Output Current



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4 Revision History

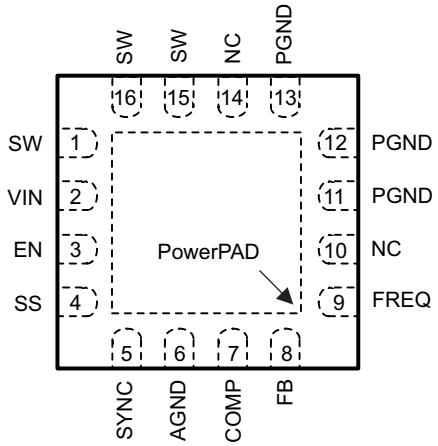
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2016) to Revision B	Page
• Added links for Webench	1
• Added text note under pin configuration diagram.	3

Changes from Original (June 2014) to Revision A	Page
• Changed the *Applications* section	1
• Changed title from *DC-DC Regulator* to *DC-DC Converter*	1
• Changed the *Handling Ratings* table to *ESD Ratings* and moved the storage temperature to the *Absolute Maximum Ratings* table	4
• Changed the *Switching Frequency* section to add recommendation for using an external synchronous clock when setting the switching frequency higher than 1.2 MHz	10
• Changed the equation to calculate R3 in the *Compensating the Control Loop (R3, C4, and C5)* section	22
• Added the *Receiving Notification of Documentation Updates* and *Community Resources* sections	30

5 Pin Configuration and Functions

16-Pin QFN With PowerPAD
RTE Package
Top View



TI recommends connecting NC with AGND.

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	6	Signal ground of the IC
COMP	7	Output of the transconductance error amplifier. An external RC network connected to this pin compensates the regulator feedback loop.
EN	3	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1 ms, the IC turns off.
FB	8	Error amplifier input and feedback pin for positive voltage regulation. Connect the FB pin to the center tap of a resistor divider to program the output voltage.
FREQ	9	Switching frequency program pin. An external resistor connected between the FREQ pin and the AGND pin sets the switching frequency.
NC	10	This pin is reserved and must be connected to ground.
	14	
PGND	11	Power ground of the IC. The PGND pin is connected to the source of the internal power MOSFET switch.
	12	
	13	
SS	4	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start timing.
SW	1	SW is the drain of the internal power MOSFET. Connect the SW pin to the switched side of the boost or SEPIC inductor or the flyback transformer.
	15	
	16	
SYNC	5	Switching-frequency synchronization pin. An external clock signal can set the switching frequency between 200 kHz and 1 MHz. If this pin is not used, it must be tied to AGND.
VIN	2	The input supply pin to the IC. Connect the VIN pin to a supply voltage between 2.9 V and 32 V. The voltage on the VIN pin can be different from the boost power-stage input.
PowerPAD		The PowerPAD must be soldered to the AGND. If possible, use thermal vias to connect the PowerPAD to PCB ground-plane layers for improved power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	VIN[2]	–0.3	40	V
	EN[2]	–0.3	40	V
	FB, FREQ, and COMP[2]	–0.3	3	V
	SS[2]	–0.3	5	V
	SYNC[2]	–0.3	7	V
Output voltage	SW[2]	–0.3	40	V
	SW (<10 ns transient)[2]	–5	40	V
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.9		38	V
V_O	Output voltage	V_I		38	V
$V_{(EN)}$	EN voltage	0		38	V
V_{SYN}	External switching-frequency logic input	0		5	V
T_A	Operating free-air temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS55340-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_I = 5 V, T_J = –40°C to 150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.9		38	V
I_Q	Operating quiescent current into VIN	Device non-switching, $V_{(FB)}$ = 2 V		0.5		mA
$I_{L(sd)}$	Shutdown current	EN = GND		2.7	10	µA
$V_{(UVLO)}$	Under-voltage lockout threshold	$V_{I(f)}$		2.5	2.7	V
V_{hys}	Under-voltage lockout hysteresis		120	140	160	mV
ENABLE AND REFERENCE CONTROL						
$V_{(EN)(r)}$	EN threshold voltage	EN rising input	0.9	1.08	1.3	V
$V_{(EN)(f)}$	EN threshold voltage	EN falling input	0.74	0.92	1.125	V
$V_{(EN)(hys)}$	EN threshold hysteresis			0.16		V
$R_{(EN)}$	EN pull down resistor		400	950	1600	kΩ
t_{off}	Shutdown delay, SS discharge	EN high to low		1		ms
$V_{(SYNC)H}$	SYN logic high voltage		1.2			
$V_{(SYNC)L}$	SYN logic low voltage				0.4	V
VOLTAGE AND CURRENT CONTROL						
V_{ref}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
		T_A = 25°C	1.22	1.229	1.238	
$I_{IB(FB)}$	Voltage feedback input bias current	T_A = 25°C		1.6	20	nA
$I_{(COMP\_sink)}$	COMP-pin sink current	$V_{(FB)} = V_{ref}$ + 200 mV, $V_{(COMP)}$ = 1 V		42		µA
$I_{S(COMP)}$	COMP-pin source current	$V_{(FB)} = V_{ref}$ – 200 mV, $V_{(COMP)}$ = 1 V		42		µA
$V_{C(COMP)}$	COMP pin Clamp Voltage	High Clamp, $V_{(FB)}$ = 1 V		3.1		V
		Low Clamp, $V_{(FB)}$ = 1.5 V		0.75		
$V_{(COMP\_th)}$	COMP pin threshold	Duty cycle = 0%		1.04		V
$g_{m(ea)}$	Error amplifier transconductance		240	360	440	µmho
$R_{O(ea)}$	Error amplifier output resistance			10		MΩ
$f_{(ea)}$	Error amplifier crossover frequency			500		kHz
FREQUENCY						
f	Frequency	$R_{(FREQ)}$ = 480 kΩ	75	94	130	kHz
		$R_{(FREQ)}$ = 80 kΩ	460	577	740	
		$R_{(FREQ)}$ = 40 kΩ	920	1140	1480	
		$R_{(FREQ)}$ = 18 kΩ	2261	2549	2837	
D_{max}	Maximum duty cycle	$V_{(FB)}$ = 1 V, $R_{(FREQ)}$ = 80 kΩ	89%	96%		
$V_{(FREQ)}$	FREQ pin voltage			1.25		V
$t_{W(on)}$min	Minimum on pulse width	$R_{(FREQ)}$ = 80 kΩ		77	107	ns
POWER SWITCH						
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_I = 5 V		60	110	mΩ
		V_I = 3 V		70	120	
I_{LN_NFET}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C			2.1	µA
OCP AND SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	5.25	6.6	7.75	A
$I_{B(SS)}$	Soft-start bias current	$V_{(SS)}$ = 0 V		6		µA
THERMAL SHUTDOWN						
T_{sd}	Thermal shutdown threshold			165		°C
T_{hys}	Thermal shutdown threshold hysteresis			15		°C

6.6 Typical Characteristics

V_I = 5 V, T_A = 25°C (unless otherwise noted)

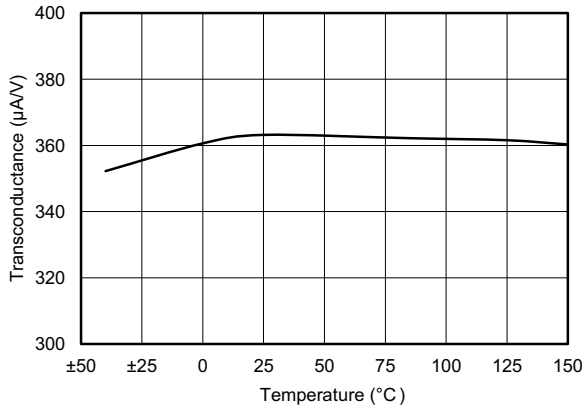


Figure 1. Error Amplifier Transconductance vs Temperature

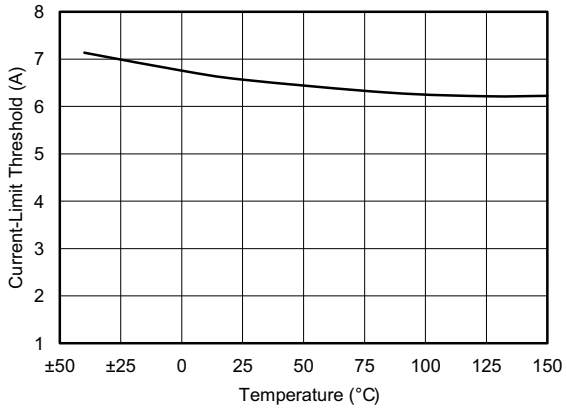


Figure 2. Switch Current-Limit vs Temperature

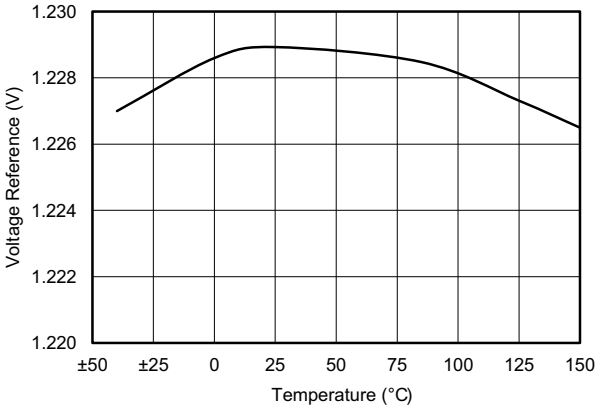


Figure 3. Feedback Voltage Reference vs Temperature

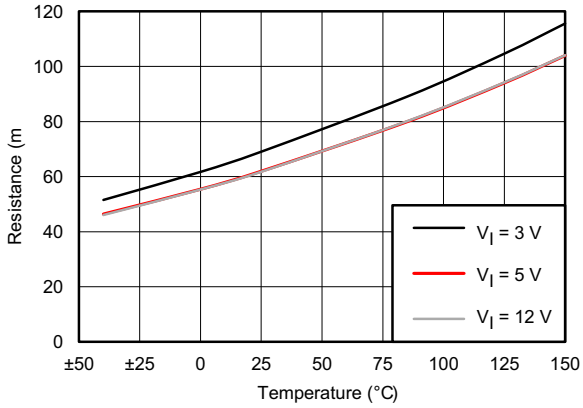


Figure 4. Static Drain-Source On-State Resistance ($r_{DS(on)}$) vs Temperature

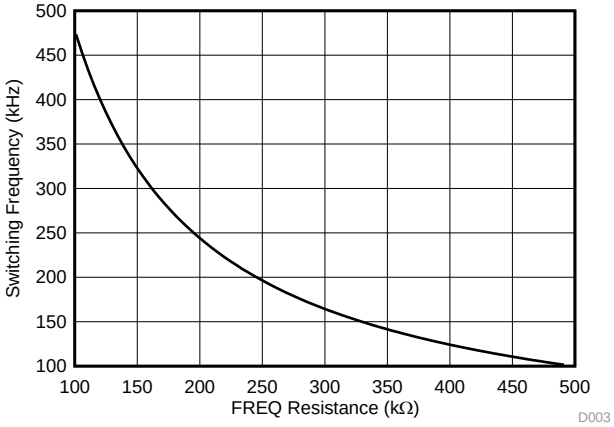


Figure 5. Frequency vs FREQ Resistance Low Frequency Range

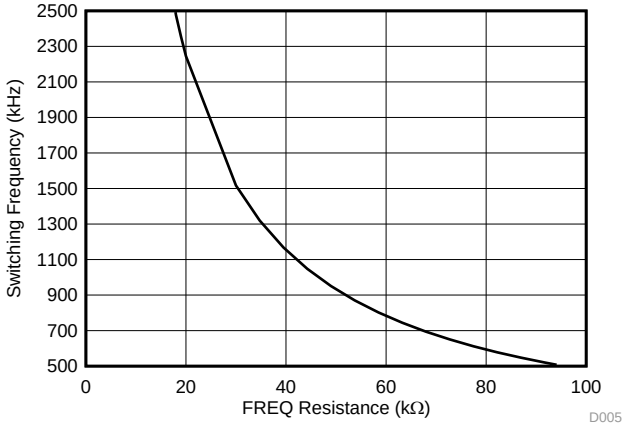


Figure 6. Frequency vs FREQ Resistance High Frequency Range

Typical Characteristics (continued)

V_I = 5 V, T_A = 25°C (unless otherwise noted)

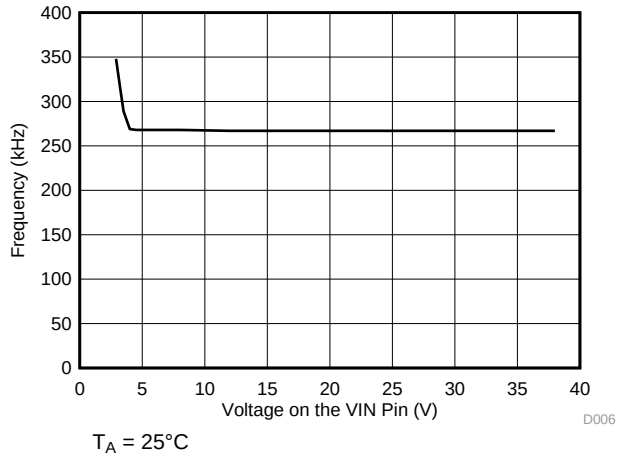


Figure 7. Minimum Switching Frequency for Quick Recovery from Frequency Foldback

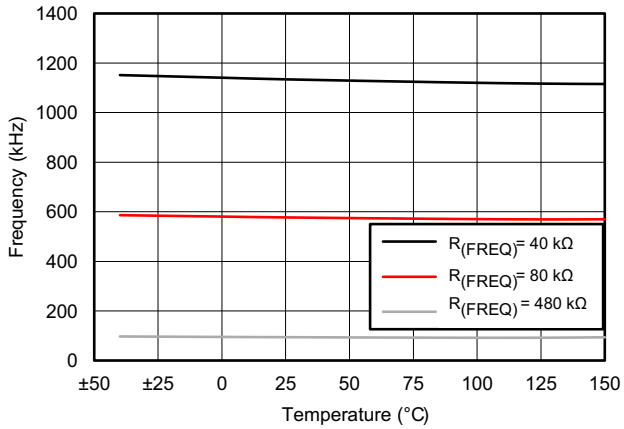


Figure 8. Frequency vs Temperature

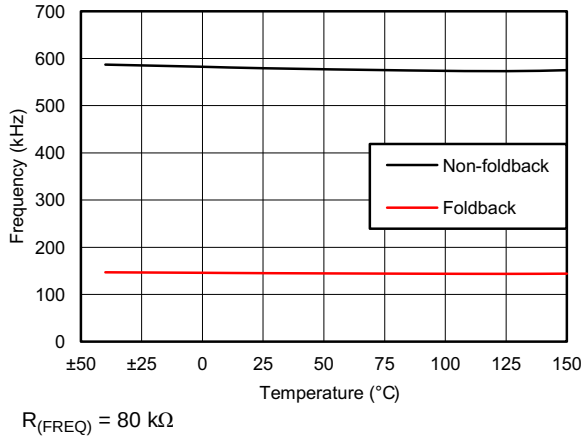


Figure 9. Non-Foldback Frequency vs Foldback Frequency

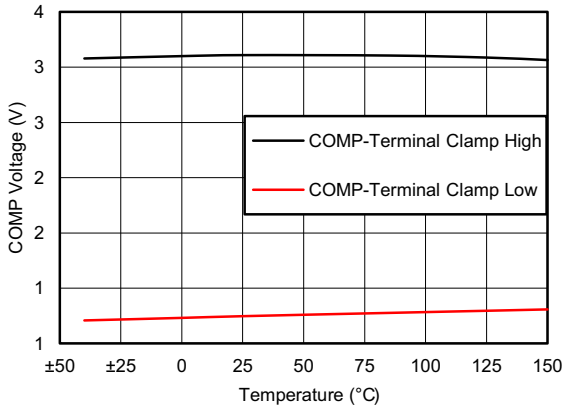


Figure 10. COMP Clamp Voltage vs Temperature

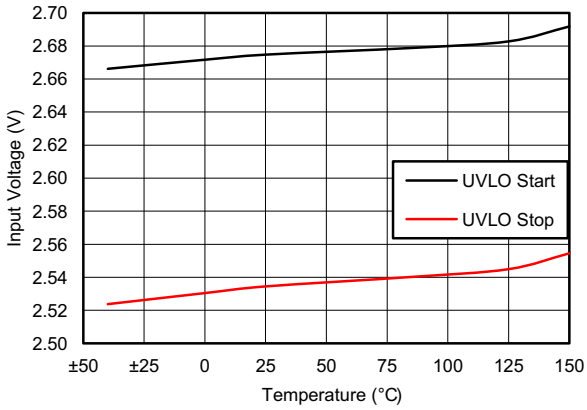


Figure 11. Input Voltage UVLO vs Temperature

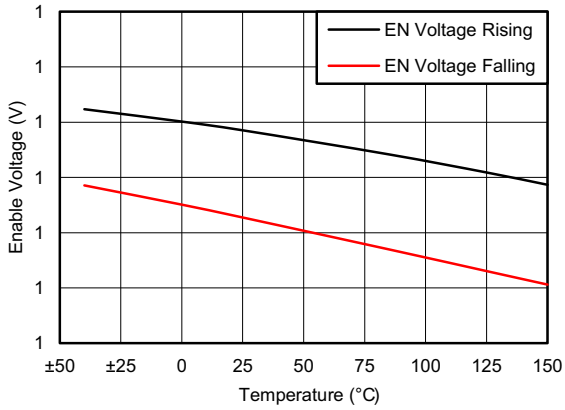
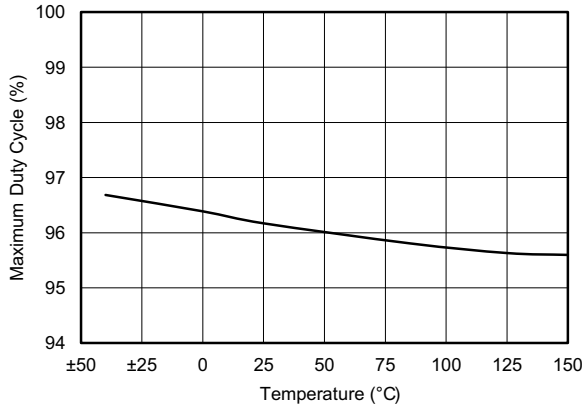


Figure 12. Enable Voltage vs Temperature

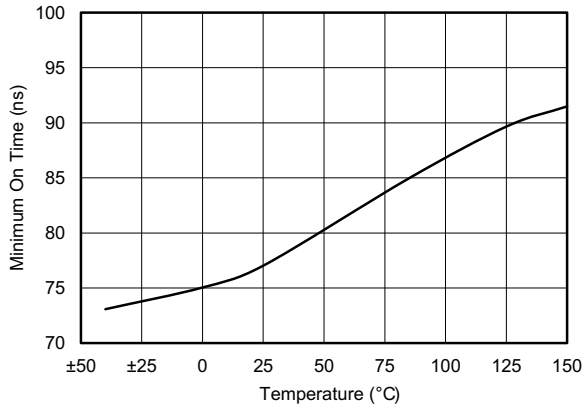
Typical Characteristics (continued)

V_I = 5 V, T_A = 25°C (unless otherwise noted)



$R_{(FREQ)}$ = 80 kΩ

Figure 13. Maximum Duty Cycle vs Temperature



$R_{(FREQ)}$ = 80 kΩ

Figure 14. Minimum On Time vs Temperature

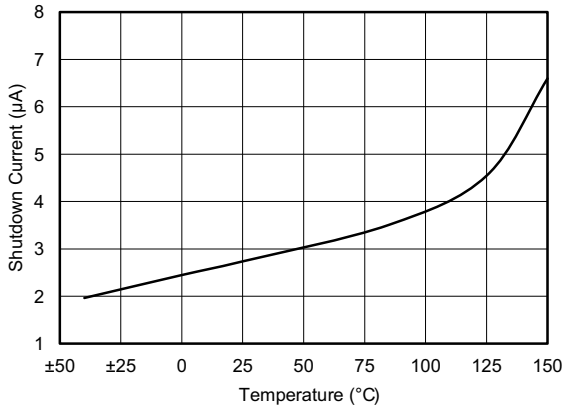


Figure 15. Shutdown Current vs Temperature

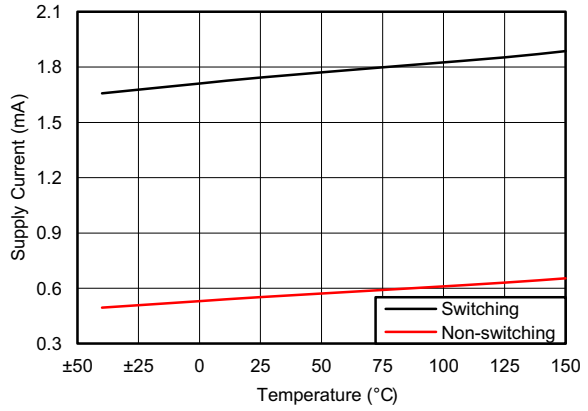


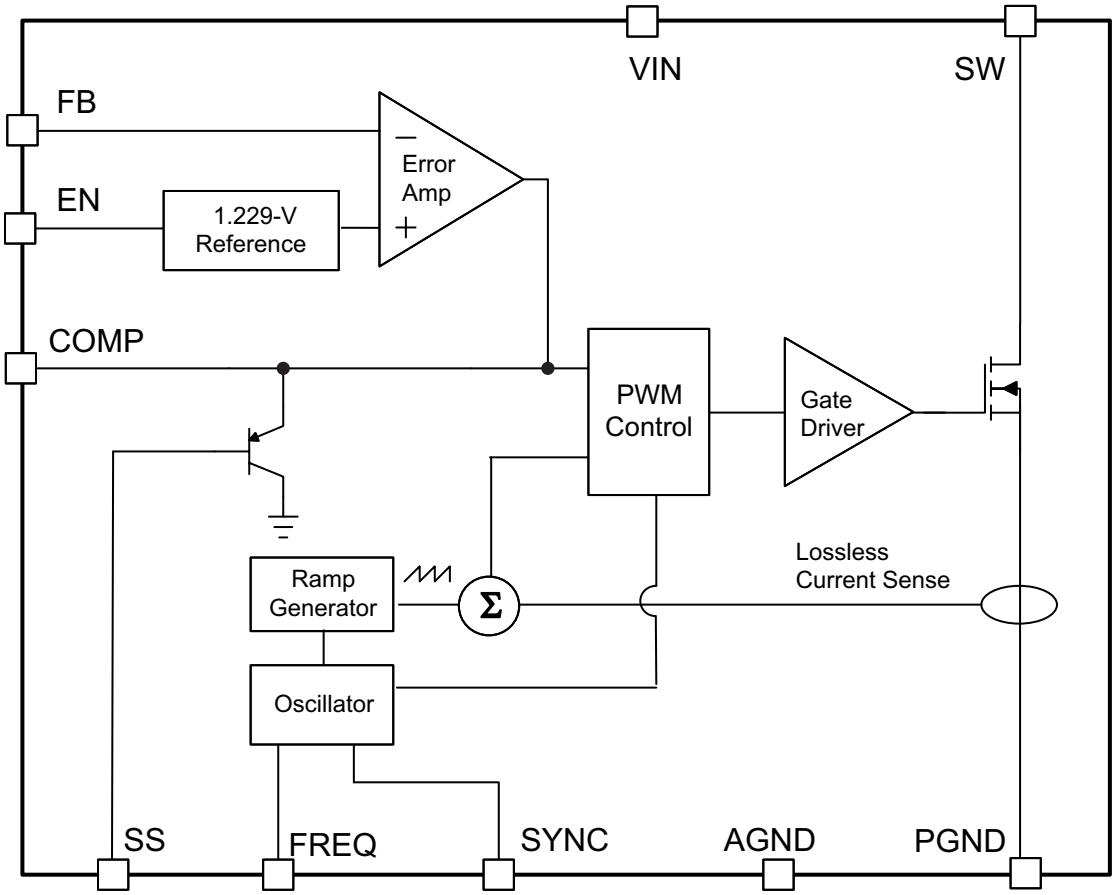
Figure 16. Supply Current vs Temperature

7 Detailed Description

7.1 Overview

The TPS55340-Q1 device is a monolithic non-synchronous switching converter with an integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multi-cell batteries or regulated 3.3-V, 5-V, 12-V, and 24-V power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation

If designed as a boost converter, the TPS55340-Q1 device regulates the output with current-mode pulse-width-modulation (PWM) control. The PWM-control circuitry turns on the switch at the beginning of each oscillator clock cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current reaches a threshold level set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased to allow the inductor current to flow to the output. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The duty cycle of the converter is determined by the PWM-control comparator which compares the error amplifier output and the current signal. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal.

Feature Description (continued)

A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. Slope compensation is required to avoid sub-harmonic oscillation that is intrinsic to peak-current mode control at duty cycles higher than 50%. If the inductor value is too small, the internal slope compensation may not be adequate to maintain stability.

The PWM control feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC-compensation network connected to the COMP pin is chosen for feedback loop stability and optimum transient response.

7.3.2 Switching Frequency

The switching frequency is set by a resistor ($R_{(FREQ)}$) connected to the FREQ pin of the TPS55340-Q1 device. The relationship between the resistance of $R_{(FREQ)}$ and frequency is shown in the Figure 5. Do not leave this pin open. A resistor must always be connected from the FREQ pin to ground for proper operation. Use Equation 1 to calculate the resistor value required for a desired frequency.

$$R_{(FREQ)}\ (k\Omega) = 57500 \times f_S^{\ -1.03}\ (kHz) \tag{1}$$

For the given resistor value, use Equation 2 to calculate the corresponding frequency.

$$f_S\ (kHz) = 41600 \times R_{(FREQ)}^{\ -0.97}\ (k\Omega) \tag{2}$$

The TPS55340-Q1 switching frequency can synchronized to an external clock signal that is applied to the SYNC pin. The required logic levels of the external clock are shown in the Electrical Characteristics table. The recommended duty cycle of the clock is in the range of 10% to 90%. A resistor must be connected from the FREQ pin to ground when the converter is synchronized to the external clock and the external clock frequency must be within ±20% of the corresponding frequency set by the resistor. For example, if the frequency programmed by the FREQ pin resistor is 600 kHz, the external clock signal must be in the range of 480 to 720 kHz.

With a switching frequency below 280 kHz (typical) after the TPS55340-Q1 enters frequency foldback as described in the *Overcurrent Protection and Frequency Foldback* section, if a load remains when the overcurrent condition is removed the output may not recover to the set value. For the output to return to the set value the load must be removed completely or the TPS55340-Q1 power cycled with the EN pin or VIN pin. Select a nominal switching frequency of 350 kHz for quicker recovery from frequency foldback.

When setting the switching frequency higher than 1.2 MHz, TI recommends using an external synchronous clock as the switching frequency to ensure that the pulse-skipping function works at a light load. When using the internal switching frequency above 1.2 MHz, the TPS55340-Q1 device might not pulse skip as described in the *Minimum On Time and Pulse Skipping* section. When the pulse-skipping function does not work at light loads, the TPS55340-Q1 device always operates in PWM mode with a minimum ON pulse width. This causes the output voltage to be higher than the set value with the resistor divider at the FB pin. This occurs in minimum duty cycle conditions such as when there is light output load or when the input voltage is close to the set output voltage in a boost topology. In the light load condition a minimum output load will keep the output voltage at the set value in a boost topology. The minimum load needed can be estimated with Equation 3 or Equation 4 using the maximum minimum on time of 107 ns and a parasitic $C_{(SW)}$ capacitance of 150 pF. For example when boosting 5 V to 12 V with 2.5 MHz switching frequency and 2-µH inductor the worst case minimum output load is 36 mA.

$$I_O\,min = \frac{\left(V_I \times t_{W(on)}\,min + \left(V_O - V_I\right) \times \sqrt{L \times C_{SW}}\right)^2 \times fs}{2 \times L \times \left(V_O - V_I\right)} \quad \text{when } V_O - V_I < V_I \tag{3}$$

$$I_O\,min = \frac{\left(V_I \times t_{W(on)}\,min + V_I \times \sqrt{L \times C_{SW}}\right)^2 \times fs}{2 \times L \times \left(V_O - V_I\right)} \quad \text{when } V_O - V_I > V_I \tag{4}$$

Feature Description (continued)

7.3.3 Overcurrent Protection and Frequency Foldback

The TPS55340-Q1 device provides cycle-by-cycle over-current protection that turns off the power switch when the inductor current reaches the overcurrent limit threshold. The PWM circuitry resets at the beginning of the next switch cycle. During an overcurrent event, the output voltage begins to droop as a function of the load on the output. When the FB voltage through the feedback resistors, drops lower than 0.9 V, the switching frequency is automatically reduced to ¼ of the normal value. Figure 9 shows the non-foldback frequency with an 80-kΩ timing resistor and the corresponding foldback frequency. The switching frequency does not return to normal until the overcurrent condition is removed and the FB voltage increases above 0.9 V. The frequency foldback feature is disabled during soft-start.

7.3.3.1 Minimum On Time and Pulse Skipping

The TPS55340-Q1 PWM control system has a minimum PWM pulse width of 77 ns (typical). This minimum on-time determines the minimum duty cycle of the PWM, for any set switching frequency. When the voltage regulation loop of the TPS55340-Q1 device requires a minimum on-time pulse width less than 77 ns, the IC enters pulse-skipping mode. In this mode, the device power switches off for several switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the PWM operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in Figure 23.

7.3.4 Voltage Reference and Setting Output Voltage

An internal voltage reference provides a precise 1.229-V voltage reference at the error amplifier non-inverting input. To set the output voltage, select the FB pin resistor $R_{(SH)}$ and $R_{(SL)}$ as shown in Equation 5.

$$V_O = 1.229\ V \times \left(\frac{R_{(SH)}}{R_{(SL)}} + 1 \right) \tag{5}$$

7.3.5 Soft-Start

The TPS55340-Q1 device has a built-in soft-start circuit that significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (6 µA typical) charges a capacitor ($C_{(SS)}$) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the peak current and duty cycle of the PWM controller. Limiting the peak switch current during start-up with a slow ramp on the SS pin reduces in-rush current and output voltage overshoot. When the capacitor reaches 1.8 V, the soft-start cycle is complete and the soft-start voltage no longer clamps the error amplifier output. When the EN is pulled low for at least 1 ms, the IC enters the shutdown mode and the SS capacitor is discharged through a 5-kΩ resistor to prepare for the next soft-start sequence.

7.3.6 Slope Compensation

To prevent sub-harmonic oscillations, the TPS55340-Q1 device uses internal slope compensation. Use Equation 6 to calculate the sensed current slope of boost converter.

$$S_{(n)} = \frac{V_I}{L} \times R_{(SENSE)} \tag{6}$$

Use Equation 7 to calculate the slope compensation dv/dt.

$$S_{(e)} = \frac{\left(\frac{0.32\ V}{R_{(FREQ)}} \right)}{16 \times (1 - D) \times 6\ pF} + \frac{0.5\ \mu A}{6\ pF} \tag{7}$$

In a converter with current mode control, in addition to the output voltage feedback loop, the inner current loop including the inductor current sampling effect as well as the slope compensation on the small-signal response must be taken into account as calculated in Equation 8.

Feature Description (continued)

$$He\ (s) = \frac{1}{1 + \frac{s \times \left[\left(1 + \frac{S_{(e)}}{S_{(n)}}\right) \times (1 - D) - 0.5\right]}{f_S} + \frac{s^2}{(\pi \times f_S)^2}}$$

where

- $R_{(SENSE)}$ (15 mΩ) is the equivalent current-sense resistor
- $R_{(FREQ)}$ is the timing resistor used to set frequency
- D is the duty cycle (8)

NOTE

If $S_{(n)} << S_{(e)}$, the converter operates in voltage mode control rather than operating current mode control, and Equation 8 is no longer valid.

7.3.7 Enable and Thermal Shutdown

The TPS55340-Q1 device enters shutdown when the EN voltage is less than 0.68 V (minimum) for more than 1ms. In shutdown, the input supply current for the device is less than 10 µA (maximum). The EN pin has an internal 950-kΩ pulldown resistor to disable the device if the pin is floating.

An internal thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical). The device restarts when the junction temperature drops by 15°C.

7.3.8 Undervoltage Lockout (UVLO)

An undervoltage-lockout circuit prevents misoperation of the device at input voltages below 2.5 V (typical). When the input voltage is below the UVLO threshold, the device remains off and the internal power MOSFET turns off. The UVLO threshold is set below the minimum operating voltage of 2.9 V to ensure that a transient VIN dip does not cause the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are **not** ensured.

7.3.9 Thermal Considerations

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55340-Q1 device. The TPS55340-Q1 device features a thermally enhanced QFN package. This package includes a PowerPad that improves the thermal capabilities of the package. The thermal resistance of the QFN package in any application greatly depends on the PCB layout and the PowerPad connection. The PowerPad must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPad to achieve good thermal performance.

7.4 Device Functional Modes

7.4.1 Operation With V_I < 2.9 V (Minimum V_I)

The TPS55340-Q1 device operates with input voltages above 2.9 V. The typical UVLO voltage (turning off) is 2.5 V and the TPS55340-Q1 device remains off at input voltages lower than that point. For the input voltages between UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are NOT ensured.

7.4.2 Operation With EN Control

The enable rising-edge threshold voltage is 1.08 V (typical) with 0.16 V hysteresis (typical). With the EN pin held below the turn-off voltage the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When the input voltage is above the UVLO threshold and the EN pin voltage increases above the rising edge threshold, the device becomes active. Switching enables and the soft-start sequence initiates. The TPS55340-Q1 device starts at the soft-start time determined by the external soft-start capacitor.

Device Functional Modes (continued)

7.4.3 Operation at Light Loads

The device is designed to operate in high-efficiency pulse-skipping mode under light load conditions. Discontinuous-conduction-mode (DCM) operation initiates when the switch current falls to 0 A. During DCM operation, the catch diode stops conducting when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of discontinuous-conduction-mode (DCM) operation as shown in Figure 22. As the load decreases further and when the voltage-regulation loop of TPS55340-Q1 device requires an on-time pulse width less than the minimum PWM pulse width of 77 ns (typical), the IC enters pulse-skipping mode. In this mode, the device holds the power switch off for several switching cycles to prevent the output voltage from rising too much above the desired regulated voltage.

8 Application and Implementation

8.1 Application Information

The TPS55340-Q1 device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. For example, the device configured in boost topology is widely used to convert a lower DC voltage to a higher DC voltage with a maximum available switching current of 5.25 A. Use the following design procedure to select component values for a boost converter design or SEPIC design for the TPS55340-Q1 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Applications

The following section provides a step-by-step design approach for configuring the TPS55340-Q1 device as a voltage regulating boost converter, as shown in Figure 17. When configured as SEPIC or flyback converter, a different design approach is required. A design example of SEPIC converter is provided in the *TPS55340-Q1 SEPIC Converter* section.

8.2.1 TPS55340-Q1 Boost Converter

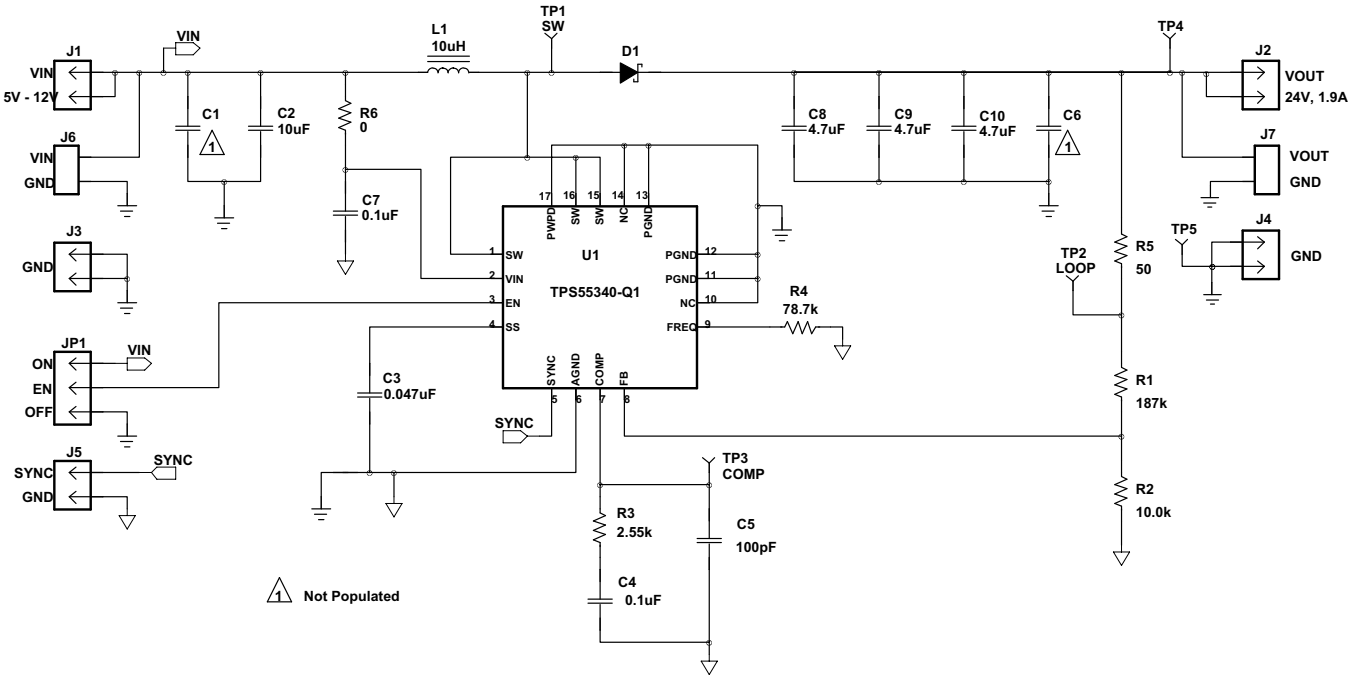


Figure 17. Boost Converter Application Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1. These parameters are typically determined at the system level.

Table 1. Key Parameters of Boost Converter Example

DESIGN PARAMETER	EXAMPLE VALUE
Output Voltage	24 V
Input Voltage	5 V to 12 V
Maximum Output Current	800 mA
Transient Response 50% load step (ΔV_O = 3%)	960 mV
Output Voltage Ripple (0.5% of V_O)	120 mV

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS55340-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Selecting the Switching Frequency (R4)

The first step of this design procedure is to determine the switching frequency of the regulator. Consider the tradeoffs of a higher switching frequency versus a lower switching frequency. A higher switching frequency allows for the use of a lower-valued inductor and smaller output capacitors which leads to the smallest solution size. A lower switching frequency results in a larger solution size but better efficiency. In general, the selected switching frequency allows for the minimum tolerable efficiency to avoid excessively large external components.

A switching frequency of 600 kHz is a good trade-off between efficiency and solution size. The appropriate resistor value is selected based on the resistance versus frequency graph (see Figure 5) or calculated using Equation 1. The value of R4 is calculated to be 78.4 kΩ and the nearest standard value resistor of 78.7 kΩ is selected. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

8.2.1.2.3 Determining the Duty Cycle

The input-to-output voltage-conversion ratio of the TPS55340-Q1 device is limited by the worst-case maximum duty cycle of 89% and the minimum duty cycle which is determined by the minimum on-time of 77 ns and the switching frequency. Use Equation 9 to calculate the minimum duty cycle. Selecting a 600-kHz switching frequency, the minimum duty cycle is calculated as 4%.

$$D_{(PS)} = t_{on}min \times f_S \quad (9)$$

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in discontinuous conduction mode (DCM), where the inductor current ramps to zero at the end of each cycle, the duty cycle varies with changes of the load much more than when running in continuous conduction mode (CCM). In continuous conduction mode, where the inductor maintains a minimum DC current, the duty cycle is related primarily to the input and output voltages as calculated with Equation 10. Assume a 0.5-V drop ($V_{(D)}$) across the Schottky rectifier. At the minimum input of 5 V, the duty cycle is 80%. At the maximum input of 12 V, the duty cycle is 51%.

$$D = \frac{V_O + V_{(D)} - V_I}{V_O + V_{(D)}} \tag{10}$$

At light loads the converter operates in DCM. In this case the duty cycle is a function of the load, input voltage, output voltages, inductance, and switching frequency as calculated in Equation 11. The light-load duty cycle can be calculated only after an inductance is selected (see the *Selecting the Inductor (L1)* section). While operating in DCM with very-light load conditions the duty cycle demand forces the TPS55340-Q1 device to operate with the minimum on time. The converter then begins pulse skipping which can increase the output ripple.

$$D = \frac{\sqrt{2 \times (V_O + V_{(D)} - V_I) \times L \times I_O \times f_S}}{V_I} \tag{11}$$

All converters using a diode as the freewheeling or catch component have a load-current level at which the converters transition from DCM to CCM. The transit from DCM to CCM is the point when the inductor current falls to zero during the off-time of the power switch. At higher load currents, the inductor current does not fall to zero and the diode and switch current assume a trapezoidal wave-shape as opposed to a triangular wave-shape. The load current boundary between discontinuous conduction and continuous conduction is calculated for a set of converter parameters as shown in Equation 12.

$$I_{O(cr)} = \frac{\left(V_O + V_{(D)} - V_I\right) \times V_I^2}{2 \times \left(V_O + V_{(D)}\right)^2 \times f_S \times L}$$

where

- V_O is the output voltage of the converter in volts (V)
- $V_{(D)}$ is the forward conduction voltage drop across the rectifier or catch diode in volts (V)
- V_I is the input voltage to the converter in volts (V)
- I_O is the output current of the converter in amperes (A)
- L is the inductor value in henries (H)
- f_S is the switching frequency in hertz (Hz) (12)

For loads higher than the result of the Equation 12, the duty cycle is given by Equation 10. For loads less than the results of Equation 12, the duty cycle is given Equation 11.

Unless otherwise stated, the design equations that follow assume that the converter is running in continuous conduction mode, which typically results in a higher efficiency for the power levels of this converter.

8.2.1.2.4 Selecting the Inductor (L1)

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. Because of these factors, the inductor is the most important component in the power-regulator design. There are three important inductor specifications: inductor value, DC resistance, and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The minimum value of the inductor must meet the inductor current ripple (ΔI_L) requirement at worst case. In a boost converter, the maximum inductor-current ripple occurs at 50% duty cycle. For applications where duty cycle is always smaller or larger than 50%, use Equation 14 to calculate the minimum inductance with the duty cycle as close to 50% as possible and corresponding input voltage. For applications that must operate with 50% duty cycle when input voltage is somewhere between the minimum and the maximum input voltage, use Equation 15. $K_{(IND)}$ is a coefficient that represents the amount of inductor ripple current relative to the maximum

input current ($I_{(M\_DC)}$ = $I_L$avg). Use Equation 13 to calculate the maximum input current, with an estimated efficiency based on similar applications ($\eta_{(EST)}$). The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal-to or greater-than the inductor ripple current. In general, the inductor ripple value ($K_{(IND)}$) is at the discretion of the designer. However, the following guidelines can be used for selecting the value for $K_{(IND)}$.

For CCM operation, TI recommends to use $K_{(IND)}$ values in the range of 0.2 to 0.4. Selecting a value for $K_{(IND)}$ that is closer to 0.2 results in a larger inductance value, maximizes the potential output current of the converter, and minimizes electromagnetic interference (EMI). Selecting a value for $K_{(IND)}$ that is closer to 0.4 results in a smaller inductance value, a physically smaller inductor, and improved transient response. However, a $K_{(IND)}$ value close to 0.4 can result in potentially worse EMI and lower efficiency. Using an inductor with a smaller inductance value can result in the converter operating in DCM. Operating in DCM reduces the maximum output current of the boost converter, causes larger input voltage and output voltage ripple, and reduces efficiency. For this design, a value of 0.3 for $K_{(IND)}$ was selected along with a conservative efficiency estimate of 85% with the minimum input voltage and maximum output current. Use Equation 14 to calculate the minimum output inductance with the maximum input voltage because this equation corresponds to duty cycle closest to 50%. The maximum input current is estimated at 4.52 A and the minimum inductance is 7.53 µH. A standard value of 10 µH is selected.

$$I_{(M\_DC)} = \frac{V_O \times I_O}{\eta_{(EST)} \times V_I \min} \tag{13}$$

$$L_O \min \geq \frac{V_I}{I_{(M\_DC)} \times K_{(IND)}} \times \frac{D}{f_S}, \; D \neq 50\%, \; V_I \text{ with D closest to 50\%} \tag{14}$$

$$L_O \min \geq \frac{\left(V_O + V_{(D)}\right)}{I_{(M\_DC)} \times K_{(IND)}} \times \frac{1}{4 \times f_S}, \; D = 50\% \tag{15}$$

After selecting the inductance, the required current ratings can be calculated. Use Equation 16 to calculate the ripple using the selected inductance. At a minimum input voltage, the inductor has the largest current ripple, therefore $V_I$min is used in Equation 16. Use Equation 17 and Equation 18 to calculate the root mean square (RMS) and peak inductor current. For this design the current ripple is 663 mA, the RMS inductor current is 4.52 A, and the peak inductor current is 4.85 A. TI recommends that the peak inductor current rating of the selected inductor be 20% higher to account for transients during power up, faults, or transient load conditions. The most conservative approach is to specify an inductor with a saturation current greater than the maximum peak current-limit of the TPS55340-Q1 device. This approach helps to avoid saturation of the inductor. The selected inductor for this design was a Würth Elektronik 74437368100. This inductor has a saturation current rating of 12.5 A, RMS current rating of 5.2 A, and typical DCR of 27 mΩ.

$$\Delta I_L = \frac{V_I \min}{L_O} \times \frac{D \max}{f_S} \tag{16}$$

$$I_{L(RMS)} = \sqrt{\left(I_{I(DC)}\right)^2 + \left(\frac{\Delta I_L}{12}\right)^2} \tag{17}$$

$$I_{L(peak)} = I_{I(DC)} + \frac{\Delta I_L}{2} \tag{18}$$

The TPS55340-Q1 device has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too small, the slope compensation may not be adequate, and the loop can be unstable.

8.2.1.2.5 Computing the Maximum Output Current

The overcurrent limit for the integrated power MOSFET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power because of power conversion losses. Therefore, the current-limit setting, input voltage, output voltage, and efficiency can all change the maximum current output ($I_O$max). The current-limit clamps the peak inductor current and therefore the ripple must be subtracted to derive maximum DC current. Decreasing the $K_{(IND)}$ value or designing for a higher efficiency increases the maximum output current. Use the selected inductance or the selected $K_{(IND)}$ value to calculate the maximum output current. Use Equation 19, the minimum input voltage, and minimum peak current-limit ($I_{(LIM)}$) of 5.25 A to calculate the maximum output current.

$$I_O\,max = \frac{V_I\,min \times \left(I_{(LIM)} - \frac{\Delta I_L}{2}\right) \times \eta_{(EST)}}{V_O} = \frac{V_I\,min \times I_{(LIM)} \times \left(1 - \frac{K_{(IND)}}{2}\right) \times \eta_{(EST)}}{V_O} \tag{19}$$

For this design, with a 5-V input boosted to 24-V output, a 10-µH inductor with an assumed the Schottky forward voltage of 0.5 V, and estimated efficiency of 85%, the maximum output current is calculated to be 871 mA. With a 12-V input and increased estimated efficiency of 90%, the maximum output current calculated value increases to 2.13 A. This circuit was evaluated to the maximum output currents with both the minimum and maximum input voltage.

8.2.1.2.6 Selecting the Output Capacitor (C8 through C10)

At least 4.7 µF of ceramic type X5R or X7R capacitance is recommended at the output. This output capacitance was selected to meet the requirements for the output ripple (V_{rip}) and voltage change during a load transient. The loop is then compensated for the selected output capacitor. The output capacitance must be selected based on the most stringent of these criteria. The output-ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, use Equation 20 to calculate the minimum capacitance required for a given ripple. Using high ESR capacitors causes additional ripple. Use Equation 21 to calculate the maximum ESR for a specified ripple. ESR ripple can be neglected for ceramic capacitors but must be considered if tantalum or electrolytic capacitors are used. Use Equation 22 to calculate the minimum ceramic output capacitance required to meet a load transient requirement. Use Equation 23 to calculate the RMS current required by the output capacitor for support.

$$C_O \geq \frac{D\,max \times I_O}{f_S \times V_{rip}} \tag{20}$$

$$ESR \leq \frac{\left(V_{rip} - \frac{D\,max \times I_O}{f_S \times C_O}\right)}{\Delta I_L} \tag{21}$$

$$C_O \geq \frac{\Delta I_{(TRAN)}}{2 \times \pi \times f_{BW} \times \Delta V_{(TRAN)}} \tag{22}$$

$$I_{CO(RMS)} = I_O \sqrt{\frac{D\,max}{(1 - D\,max)}} \tag{23}$$

Using Equation 20 for this design, the minimum output capacitance for the specified 120-mV output ripple is 8.8 µF. For a maximum transient-voltage change ($\Delta V_{(TRAN)}$) of 960 mV with a 400 mA load transient ($\Delta I_{(TRAN)}$), and a 6 kHz control loop bandwidth (f_{BW}) with Equation 22, the minimum output capacitance is calculated as 11.1 µF. The most stringent criteria is the 11.1 µF for the required load transient. Equation 23 calculates a 1.58-A RMS current in the output capacitor. The capacitor must also be properly rated for the desired output voltage.

Care must be taken when evaluating ceramic capacitors that derate under DC bias, aging, and AC signal conditions. For example, larger form factor capacitors (in 1206 size) have self-resonant frequencies in the range of converter switching frequency. Self-resonance significantly decreases the effective capacitance. The DC bias also significantly reduces capacitance. Ceramic capacitors can lose as much as 50% of the capacitance when operated at the rated voltage. Therefore, leave a margin when selecting the capacitor voltage rating to ensure adequate capacitance at the required output voltage. For this example, three 4.7-µF, 50-V 1210 X7R ceramic capacitors are used in parallel leading to a negligible ESR. Selecting 50-V capacitors instead of 35-V capacitors reduces the effects of DC bias and allows this example circuit to be rated for the maximum output voltage range of the TPS55340-Q1 device.

8.2.1.2.7 Selecting the Input Capacitors (C2 and C7)

At least 4.7-µF of ceramic input capacitance is recommended. Additional input capacitance may be required to meet ripple requirements, transient requirements, or both. High-quality ceramic-type X5R or X7R capacitors are recommended to minimize capacitance variations over temperature. The capacitor must also have an RMS-current rating greater than the maximum RMS-input current of the TPS55340-Q1 device as calculated with Equation 24. The input capacitor must also be rated greater than the maximum input voltage. Use Equation 25 to calculate the input voltage ripple.

$$I_{CI(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \tag{24}$$

$$V_{I(rip)} = \frac{\Delta I_L}{4 \times f_S \times C_I} + \Delta I_L \times R_{(CI)} \tag{25}$$

In the design example, the input RMS current is calculated to be 191 mA. The selected input capacitor is a 10-µF, 35-V 1210 X7R with 3 mΩ ESR. Although a capacitor with a lower voltage rating can be used, a 35-V rated capacitor was selected to limit the affects of DC bias and to allow the circuit to be rated for the entire input range of the TPS55340-Q1 device. The input ripple is calculated to be 30 mV. An additional 0.1-µF, 50-V 0603 X5R is located close to the VIN pin and the GND pin for additional decoupling.

8.2.1.2.8 Setting the Output Voltage (R1 and R2)

To set the output voltage in either DCM or CCM, use Equation 26 and Equation 27 to calculate the values of R1 and R2.

$$V_O = 1.229\ V \times \left(\frac{R1}{R2} + 1\right) \tag{26}$$

$$R1 = R2 \times \left(\frac{V_O}{1.229\ V} - 1\right) \tag{27}$$

Considering the leakage current through the resistor divider and noise decoupling into FB pin, an optimum value for R2 is around 10 kΩ. The output voltage tolerance depends on the $V_{(FB)}$ accuracy and the tolerance of R1 and R2. In this example, with a 24 V output, R1 is calculated to 185.3 kΩ using Equation 27. The nearest standard value of 187 kΩ is used.

8.2.1.2.9 Setting the Soft-Start Time (C7)

Select the appropriate capacitor to set soft-start time and avoid overshoot. Increasing the soft-start time reduces the overshoot during start-up. A 0.047 µF ceramic capacitor is used in this example.

8.2.1.2.10 Selecting the Schottky Diode (D1)

The high switching frequency of the TPS55340-Q1 device demands high-speed rectification for optimum efficiency. Ensure that the average current rating and peak current rating of the diode exceed the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the regulated output voltage. The diode must also be rated for the power dissipated which is calculated using Equation 28.

$$P_D = V_{(D)} \times I_O \tag{28}$$

In this conservative design example, the selected diode is rated for the maximum output current of 2.13 A. During normal operation with 800-mA output current and assuming a Schottky diode drop of 0.5 V, the diode must be capable of dissipating 400 mW. The recommended minimum ratings for this design are a 40-V, 3-A diode. However to improve the flexibility of this design, a Diodes Inc B540-13-F in an SMC package with voltage and current ratings of 40 V and 5 A was selected for this desigh.

8.2.1.2.11 Compensating the Control Loop (R3, C4, and C5)

The TPS55340-Q1 device requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor (R3) and ceramic capacitor (C4) are connected to the COMP pin to provide a pole and a zero as shown in the application circuit (see Figure 17). This pole and zero, along with the inherent pole and zero of a boost converter, determine the closed loop frequency response which is important for converter stability and transient response. Loop compensation must be designed for the minimum operating voltage.

The following equations summarize the loop equations for the TPS55340-Q1 device configured as a CCM boost converter. The equations include the power stage output pole (f_O) and the right-half-plane zero ($f_{(RHPZ)}$) of a boost converter calculated using Equation 29 and Equation 30 respectively. When calculating f_O, including the derating of ceramic output capacitors is important. In the example with an estimated 10.2-µF capacitance, these frequencies are calculated to be 980 kHz and 22.1 kHz respectively. Use Equation 29 to calculate the DC gain (A) of the power stage which is 39.9 dB in this design. Use Equation 32 and Equation 33 to calculate the compensation pole ($f_{(P)}$) and zero ($f_{(Z)}$) generated by R3, C4, and the internal transconductance amplifier (respectively).

Most CCM boost converters have a stable control loop if $f_{(Z)}$ is set slightly above $f_{(P)}$ through proper sizing of R3 and C4. To start, select a value of 0.1 µF for C4 and a value of 2 kΩ for R3. Increasing R3 or reducing C4 increases the closed loop bandwidth and therefore improves the transient response. Adjusting R3 and C4 in opposite directions increases the phase and gain margin of the loop, which improves loop stability. TI recommends to limit the bandwidth of the loop to the lower of either 1/5 of the switching frequency (f_S) or 1/3 the RHPZ frequency ($f_{(RHPZ)}$) which is calculated using Equation 30. Use the spreadsheet tool located as an aid in compensation design. See the TPS55340-Q1 product folder at www.TI.com.

$$f_O \approx \frac{2}{2\pi \times R_O \times C_O}$$

where

- C_O is the equivalent output capacitor (C_O = C8 + C9 + C10)
- R_O is the equivalent load resistance (V_O / I_O) (29)

$$f_{(RHPZ)} \approx \frac{R_O}{2\pi \times L} \times \left(\frac{V_I}{V_O}\right)^2 \tag{30}$$

$$A = \frac{1.229}{V_O} \times g_{M(ea)} \times 10\ M\Omega \times \frac{V_I}{V_O \times R_{(SENSE)}} \times R_O \times \frac{1}{2}$$

where

- g_{ea} is the error amplifier transconductance located in the Electrical Characteristics table
- $R_{(SENSE)}$ (15 mΩ, typical) is the sense resistor in the current control loop (31)

$$f_{(P)} = \frac{1}{2\pi \times 10\ M\Omega \times C4} \tag{32}$$

$$f_{(Z)} = \frac{1}{2\pi \times R3 \times C4} \tag{33}$$

$$f_{CO(1)} = \frac{f_S}{5}$$

where

- $f_{CO(1)}$ is possible bandwidth (34)

$$f_{CO(2)} = \frac{f_{(RHPZ)}}{3}$$

where

- $f_{CO(2)}$ is possible bandwidth (35)

An additional capacitor from the COMP pin to the GND pin (C5) can be used to place a high frequency pole in the control loop. Using this additional capacitor is not always required when using ceramic output capacitors. If a non-ceramic output capacitor is used, an additional zero ($f_{(ZESR)}$) is located in the control loop. Use Equation 37 to calculate $f_{(ZESR)}$. Use Equation 38 and Equation 36 to calculate the value of C5 and the pole created by C5 (respectively). Finally if additional phase margin is required, add an additional zero ($f_{(ZFF)}$) by placing a capacitor ($C_{(FF)}$) in parallel with the top feedback resistor (R1). TI recommends to place the zero at the target cross-over frequency or higher. The feed forward capacitor also adds a pole at a higher frequency. Use Equation 39 to calculate the recommended value of $C_{(FF)}$.

$$f_{(P2)} = \frac{1}{2\pi \times R3 \times C5} \tag{36}$$

$$f_{(ZESR)} \approx \frac{1}{2\pi \times R_{(ESR)} \times C_O} \tag{37}$$

$$C5 = \frac{R_{(ESR)} \times C_O}{R3}$$

where

- $R_{(ESR)}$ is the ESR of the output capacitor (38)

$$C_{(FF)} = \frac{1}{2\pi \times R1 \times f_{(ZFF)} \times \sqrt{\frac{V_{ref}}{V_O}}} \tag{39}$$

If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the minimum 5-V input and maximum 800-mA load. Figure 18 shows this measurement. In this design only one pole and one zero are used and therefore the maximum phase increase from the compensation is 180 degrees. For a 60 degree phase margin, the power stage phase must be –120 degrees at the lowest point. Based on the target 6-kHz bandwidth, the measured power stage gain, $K_{(PS)}$ (f_{BW}), is 24.84 dB and the phase is –110.3 degrees.

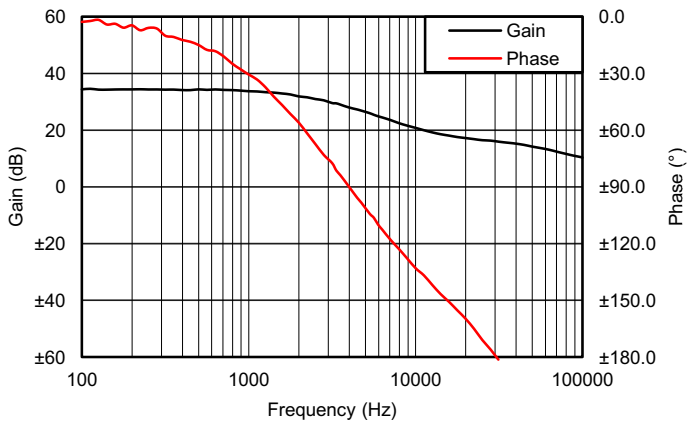


Figure 18. Power Stage Gain and Phase of the Boost Converter

The value of R3 is then selected to set the compensation gain as the reciprocal of the power stage gain at the target bandwidth using Equation 40. The value of C4 is then selected to place a zero at 1/10 the target bandwidth using Equation 41. In this case R3 is calculated to be 2.56 kΩ, the nearest standard value 2.55 kΩ is used. The value of C4 is calculated to be 0.104 µF and the nearest standard value of 0.100 µF is used. A 100-pF capacitor is selected for C5 to add a high frequency pole at a frequency 100 times the target bandwidth, however adding 100 pF for C5 is not necessary because this design uses all ceramic capacitors.

$$R3 = \frac{1}{\left(g_{M(ea)} \times \frac{R2}{(R1 + R2)} \times 10^{\frac{K_{(PS)}(f_{BW})}{20}} \right)} \tag{40}$$

$$C4 = \frac{1}{2\pi \times R3 \times \frac{f_{BW}}{10}} \tag{41}$$

8.2.1.3 Application Curves

The following application curves are characteristics of the boost converter.

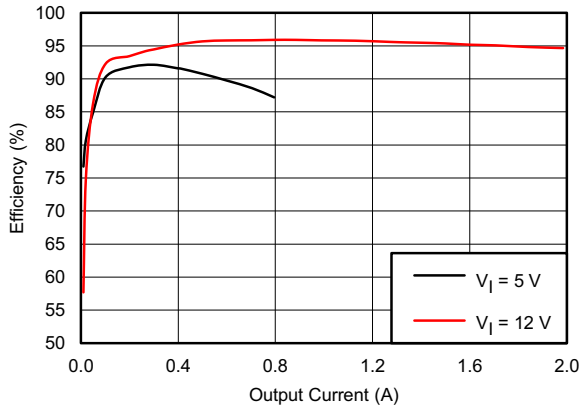
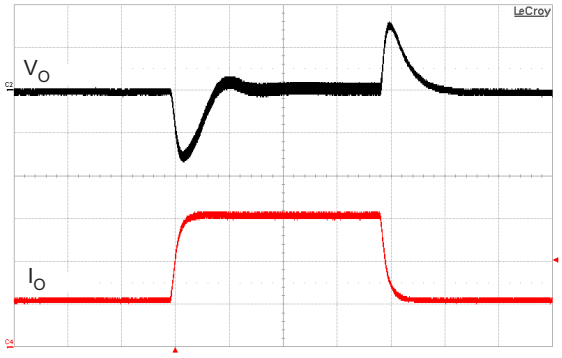
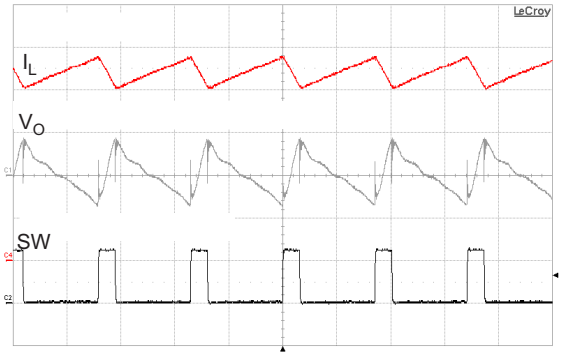


Figure 19. Efficiency Versus Output Current



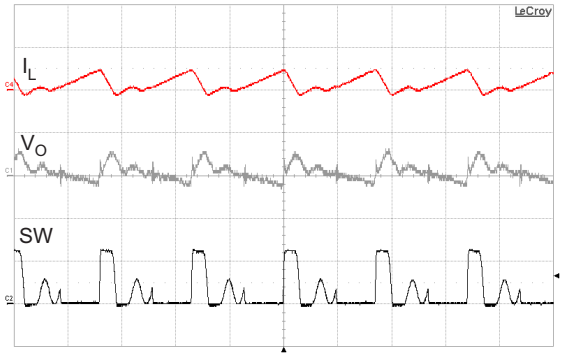
Time — 1 ms/div
V_O (AC-coupled) = 500 mV/div
I_O = 200 mA/div

Figure 20. Load Transient Response



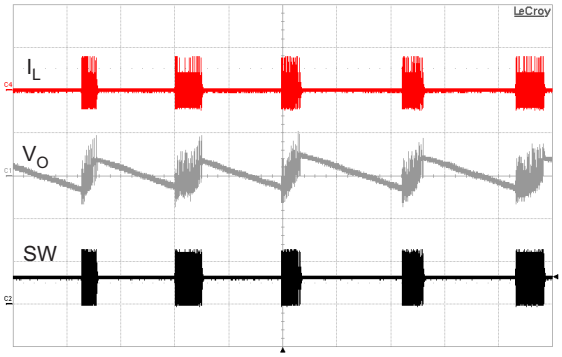
Time — 1 ms/div
I_L = 1 A/div
V_O (AC-coupled) = 100 mV/div
$V_{(SW)}$ = 20 V/div

Figure 21. CCM PWM Operation



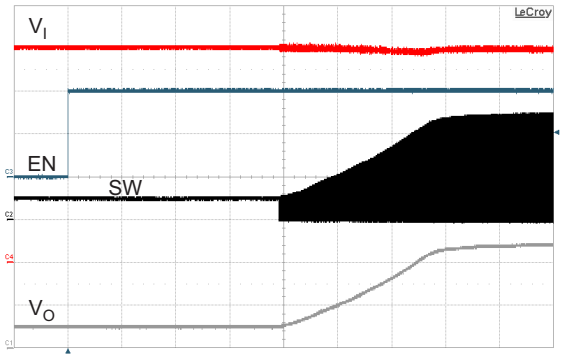
Time — 1 µs/div
I_L = 1 A/div
V_O (AC-coupled) = 10 mV/div
$V_{(SW)}$ = 20 V/div

Figure 22. DCM PWM operation



Time — 50 µs/div
I_L = 200 mA/div
V_O (AC-coupled) = 20 mV/div
$V_{(SW)}$ = 20 V/div

Figure 23. Pulse Skipping



Time — 500 µs/div
V_I = 1 V/div
$V_{(EN)}$ = 2 V/dvi
$V_{(SW)}$ = 10 V/div
V_O = 10 V/div

Figure 24. Startup

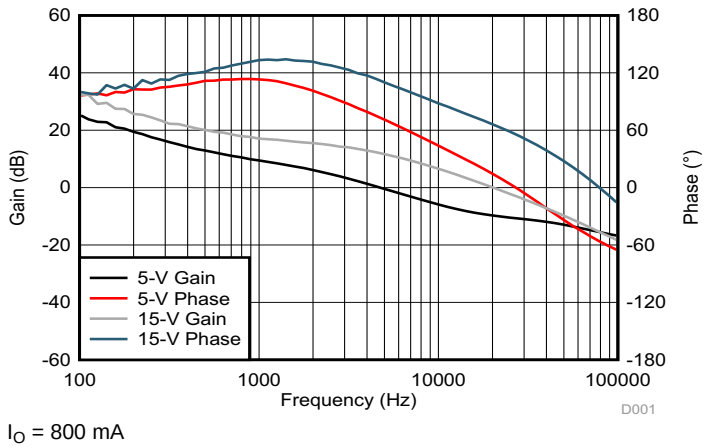


Figure 25. Closed Loop Gain and Phase of the Boost Converter

8.2.2 TPS55340-Q1 SEPIC Converter

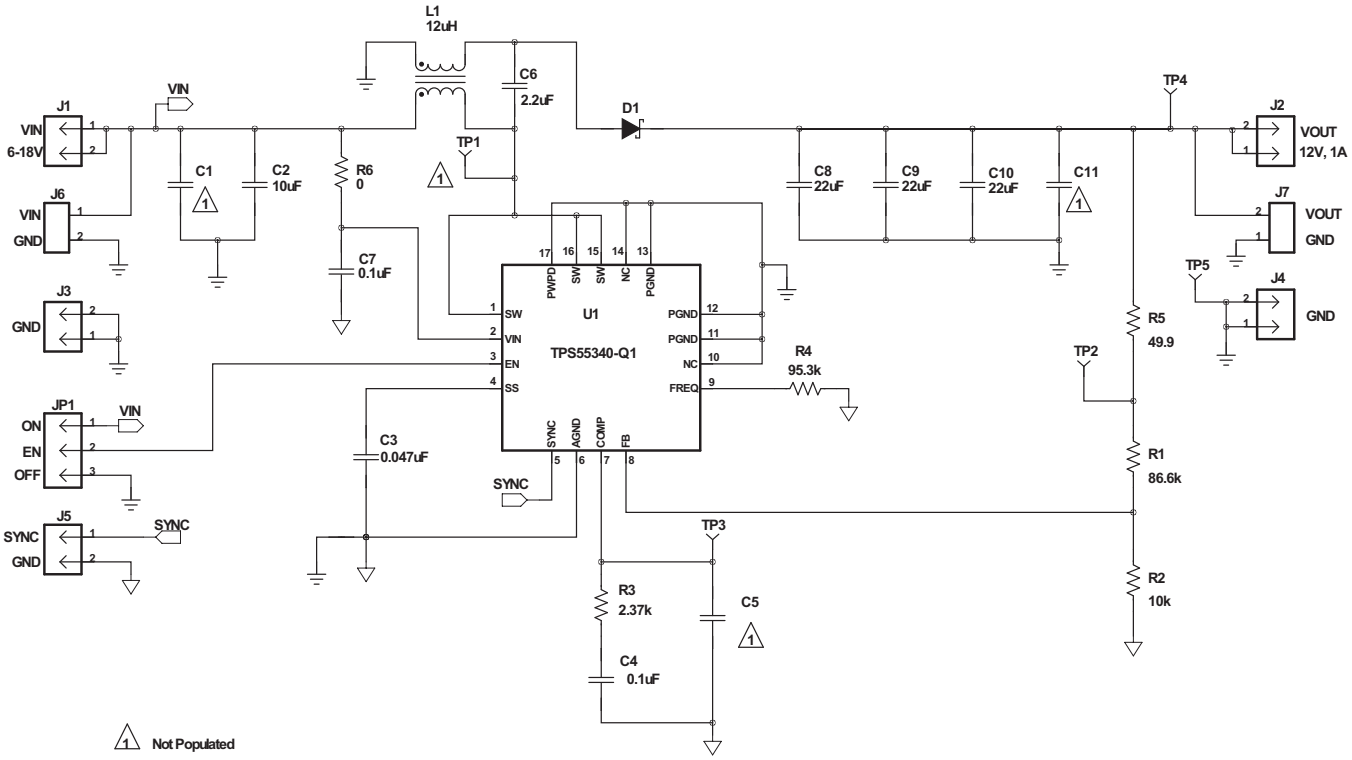


Figure 26. SEPIC-Converter Application Schematic

8.2.2.1 Design Requirements

The parameters listed in Table 2 are used for a SEPIC converter design. These calculations are performed only for CCM operation. The use of a coupled inductor is assumed.

Table 2. Key Parameters of SEPIC Converter Example

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	12 V
Input voltage	6 V to 18 V, 12 V nominal
Maximum output current	1 A
Transient response 50% load step (ΔV_O = 4%)	480 mV
Output voltage ripple (0.5% of V_O)	60 mV

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Selecting the Switching Frequency (R4)

A 500-kHz switching frequency (f_S) was selected for this design. Use Equation 1 and the nearest standard value 95.3 kΩ to calculate the value of R4.

8.2.2.2.2 Duty Cycle

Use Equation 42 to calculate the duty cycle of a SEPIC converter. Selecting the 6-V minimum input the duty cycle is calculated as 68%. Selecting the 18-V maximum input voltage the duty cycle is calculated as 41%.

$$D = \frac{V_O + V_{(D)}}{V_O + V_{(D)} + V_I} \tag{42}$$

8.2.2.2.3 Selecting the Inductor (L1)

With an estimated 85% efficiency, the input current is calculated to be 2.35 A using Equation 11. The minimum inductance is calculated to be 10.5 µH using Equation 43 with a $K_{(IND)}$ value of 0.3 and a maximum input value of 18-V. The nearest standard value of 12 µH is used. This equation assumes that a coupled inductor is used.

$$L \geq \frac{V_I\,max \times D\,min}{2 \times f_S \times I_{I(DC)} \times K_{(IND)}} \tag{43}$$

The inductor ripple current is recalculated to be 615 mA using Equation 44. The peak current is calculated to be 3.69 A. For the saturation rating of the selected inductor, use the typical current-limit. The RMS current for La is approximately the average input current 2.35 A. The RMS current for Lb is approximately the output current of 1 A. For this design a CoilCraft MSD1260-123 was used with 6.86-A saturation, 74-mΩ DCR, and 3.12-A RMS current rating for one winding.

$$\Delta I_L = \frac{V_I\,max \times D\,min}{2 \times f_S \times L} \tag{44}$$

$$I_{L(peak)} = I_{L(a\_peak)} + I_{L(b\_peak)} = \left(I_{I(DC)} + \frac{\Delta I_L}{2}\right) + \left(I_O + \frac{\Delta I_L}{2}\right) \tag{45}$$

8.2.2.2.4 Calculating the Maximum Output Current

The maximum output current is calculated to be 1.47 A using Equation 46 with the minimum input voltage of 6 V, selected inductance of 12 µH, 5.25-A minimum current-limit, and estimated 85% efficiency.

$$I_O\,max = \frac{\left(I_{(LIM)} - \Delta I_L\right)}{\left(\frac{V_O}{V_I\,min \times \eta_{(EST)}} + 1\right)} = \frac{\left(I_{(LIM)} - I_{I(DC)} \times K_{(IND)}\right)}{\left(\frac{V_O}{V_I\,min \times \eta_{(EST)}} + 1\right)} \tag{46}$$

8.2.2.2.5 Selecting the Output Capacitor (C8 through C10)

To meet the 60-mV ripple specification, the minimum output capacitance is calculated to be 22.5 µF with Equation 47. This design uses ceramic output capacitors and the effects of ESR are ignored. To meet the transient response of 500 mA with less than 480-mV voltage change and a 7-kHz control loop bandwidth, the minimum output capacitance is calculated to be 23.7µF using Equation 48. The RMS current is calculated to be 1.44 A using Equation 24. The output capacitors used in this design is three 22-µF, 25-V X7R 1210 ceramic capacitors. With voltage derating, the effective total output capacitance is estimated to be 30.4 µF.

$$C_O \geq \frac{D_{max} \times I_O}{f_S \times V_{rip}} \tag{47}$$

$$C_O \geq \frac{\Delta I_{(TRAN)}}{2\pi \times f_{BW} \times \Delta V_{(TRAN)}} \tag{48}$$

8.2.2.2.6 Selecting the Series Capacitor (C6)

The series capacitor is chosen to limit the ripple current to 5% of the maximum input voltage. Using Equation 49 the minimum capacitance is 1.5 µF. Using Equation 50 the RMS current is calculated to be 1.63 A. A 2.2-µF ceramic capacitor in a 1206 package was selected for this design.

$$C_{(P)} \geq \frac{I_O \times D_{max}}{0.05 \times V_I max \times f_S} \tag{49}$$

$$I_{(CP\_RMS)} = I_{I(DC)} \times \sqrt{\frac{(1 - D_{max})}{D_{max}}} \tag{50}$$

8.2.2.2.7 Selecting the Input Capacitor (C2 and C7)

Based on the minimum 4.7-µF ceramic recommended for the TPS55340-Q1 device, a 10-µF X7R input capacitor was used with an additional 0.1 µF placed close to the VIN pin and the GND pin. With an estimated 6-µF capacitance after voltage derating, the input ripple voltage is calculated to be 39.9 mV using Equation 51. The RMS current of the input capacitance is calculated to be 0.177 A using Equation 52.

$$V_{I(rip)} = \frac{\Delta I_L}{4 \times f_S \times C_I} \tag{51}$$

$$I_{(CI\_RMS)} = \frac{\Delta I_L}{\sqrt{12}} \tag{52}$$

8.2.2.2.8 Selecting the Schottky Diode (D1)

The selected diode must have a minimum breakdown voltage ($V_{(BR)}$). Use Equation 53 to calculate $V_{(BR)}$ which is 30.5 V in this design. The average current rating is recommended to be greater than the maximum output current. With the maximum 18-V input, average current is calculated to be 2.6 A using Equation 19. The package must also be capable of handling the power dissipation. With an estimated 0.5 V forward voltage, power dissipation is calculated with Equation 28 to be 500 mW. Diodes Inc B340B was chosen for this design with a 40-V, 3-A rating in a SMB package.

$$V_{(BR)} = V_O + V_I max + V_F \tag{53}$$

8.2.2.2.9 Setting the Output Voltage (R1 and R2)

With R2 fixed at 10 kΩ, use Equation 27 to calculate the nearest standard value of 86.6 kΩ for R1.

8.2.2.2.10 Setting the Soft-Start Time (C3)

The recommended 0.047-µF soft-start capacitor is used for C3.

8.2.2.2.11 Mosfet Rating Considerations

In this design, with the maximum input voltage of 18 V and output voltage of 12 V, the FET receives approximately 30 V across drain and source. A 10% tolerance for the MOSFET V_{DS} rating is recommended to account for any ringing. The 40-V rating of the TPS55340-Q1 power MOSFET comfortably satisfies this requirement.

8.2.2.2.12 Compensating the Control Loop (R3 and C4)

This design was compensated by measuring the frequency response of the power stage at the lowest input voltage of 6 V and choosing the components for the desired bandwidth. The lowest right-half plane zero ($f_{(RHPZ)}$) is calculated with Equation 54 to be 36.7 kHz. When using the recommendation of limiting the bandwidth to 1/3 of $f_{(RHPZ)}$ or less, the recommended maximum bandwidth is 12.2 kHz.

$$f_{(RHPZ)} = \frac{\frac{V_O}{I_O}}{2 \times \pi \times L \times \left(\frac{D}{(1-D)}\right)^2} \tag{54}$$

This design also uses only one pole and one zero. To achieve approximately 60 degrees of phase margin, the power stage phase must be no lower than approximately –120 degrees at the desired bandwidth. To ensure a stable design, R3 was initially set to 1 kΩ and C4 was set to 1 µF. Figure 27 shows the measurement of the power stage. At 7 kHz the power stage has a gain of 19.52 dB and phase of –118.1 degrees.

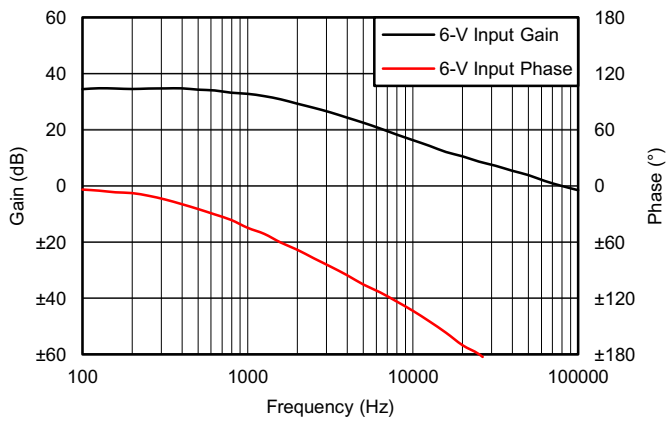


Figure 27. SEPIC Power Stage Gain and Phase

Because no changes occur in the transconductance amplifier, the equations used to calculate the external compensation components in a boost design can be used in the SEPIC design. Using the maximum $g_{m(ea)}$ from the electrical specification of 440 µmho, Equation 40 calculates the nearest standard value of R3 to be 2.37 kΩ. Using Equation 41, C4 is calculated to the nearest standard value of 0.1 µF.

8.2.2.3 Application Curves

The following curves are characteristics of the SEPIC converter.

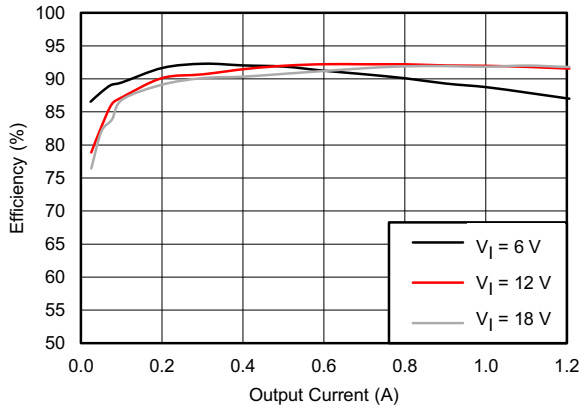


Figure 28. Efficiency Versus Output Current

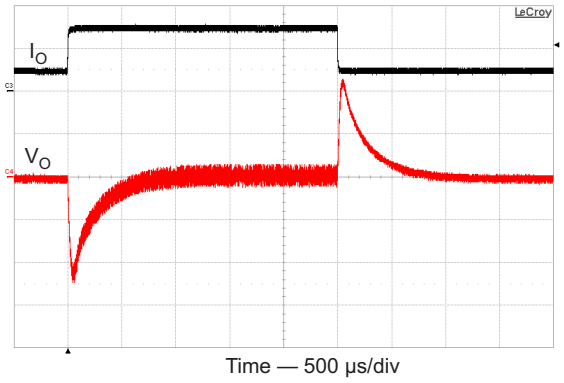


Figure 29. Load Transient Response

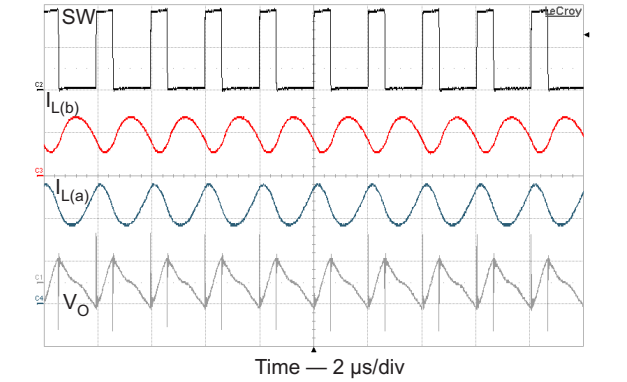


Figure 30. CCM PWM Operation

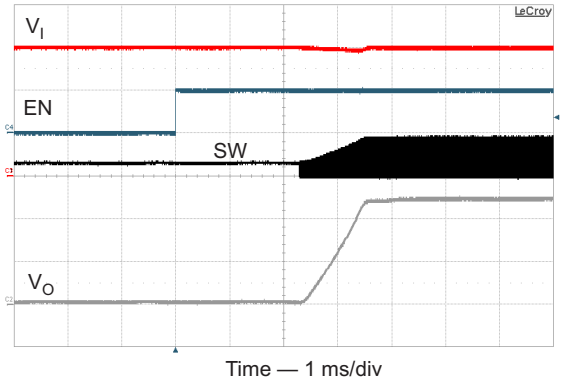


Figure 31. Output Voltage Soft-start

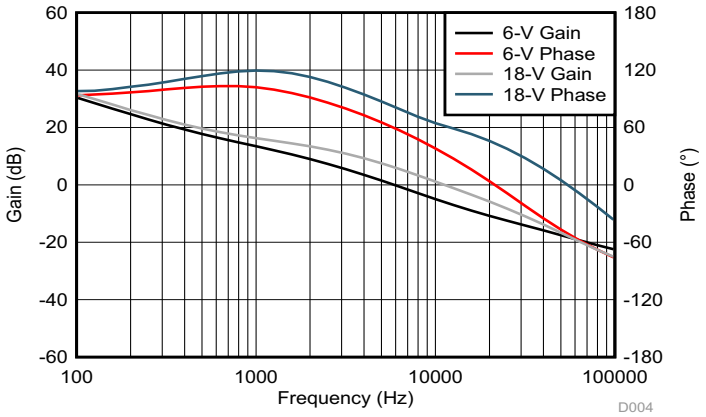


Figure 32. Closed Loop Gain and Phase of the SEPIC Converter

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.9 V and 32 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS55340-Q1 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those with high frequency and high switch current, printed circuit board (PCB) layout is an important design step. If the layout is not carefully designed, the regulator can suffer from instability as well as noise problems. The following guidelines are recommended for good PCB layout.

- To maximize efficiency, keep switch rise and fall times as short as possible.
- To prevent radiation of high frequency resonance problems, use proper layout of the high frequency switching path.
- Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.
- The high current path including the internal MOSFET switch, Schottky diode, and output capacitor, contains nanosecond rise times and fall times. Keep these rise times and fall times as short as possible.
- Place the input capacitor as close to the VIN pin and the AGND pin as possible to reduce the IC supply ripple.

10.2 Layout Example

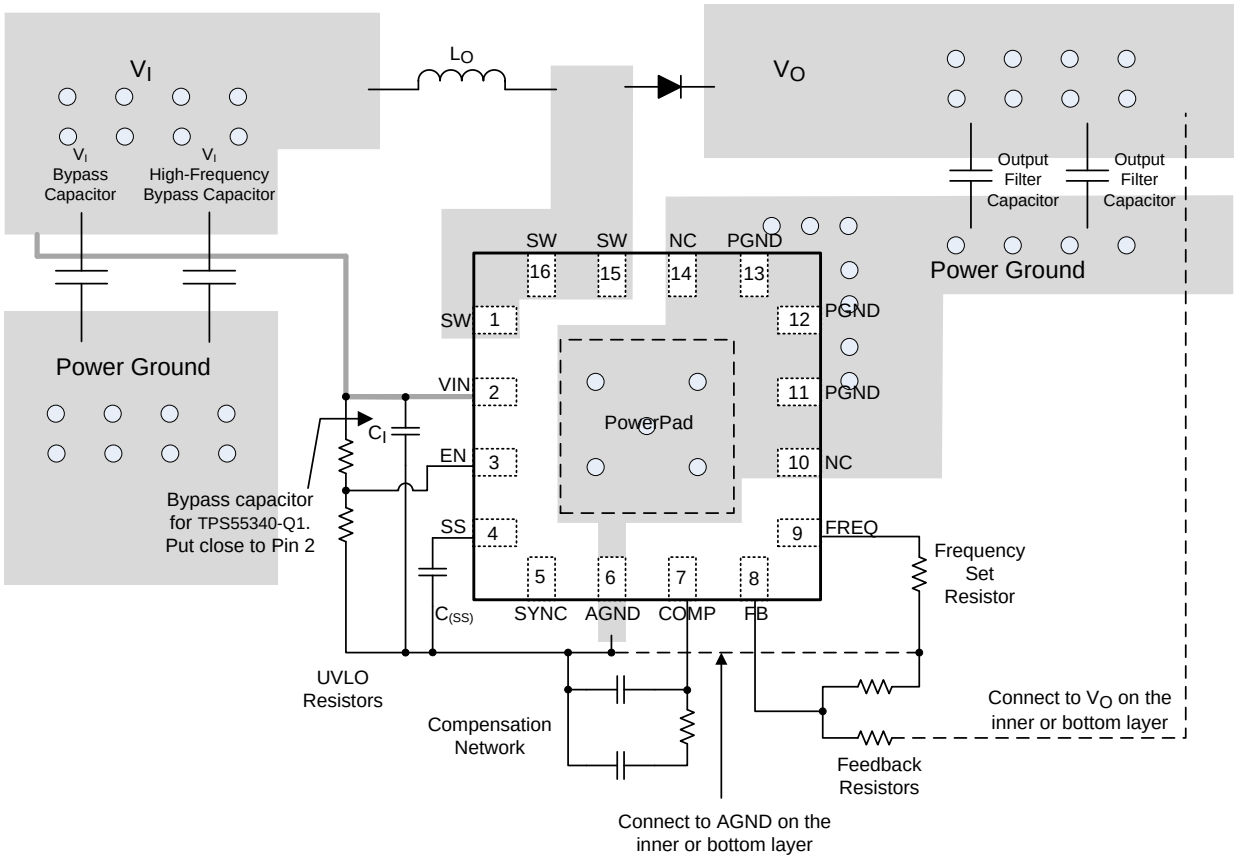


Figure 33. TPS55340-Q1 Example Board Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS55340-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPad, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55340QRTERQ1	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	55340Q	Samples
TPS55340QRTETQ1	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	55340Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS55340-Q1 :

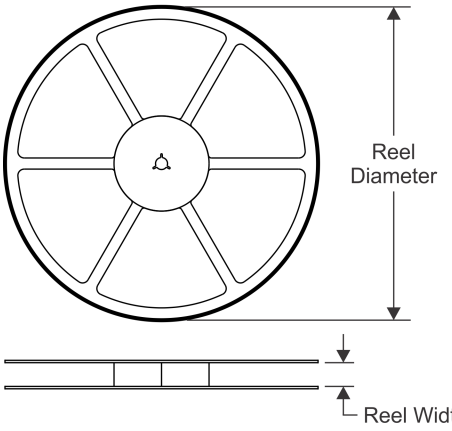
- Catalog: TPS55340
- Enhanced Product: TPS55340-EP

NOTE: Qualified Version Definitions:

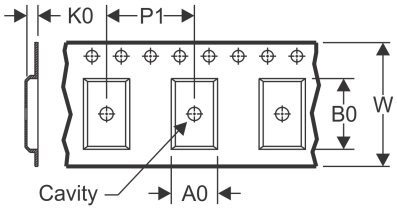
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

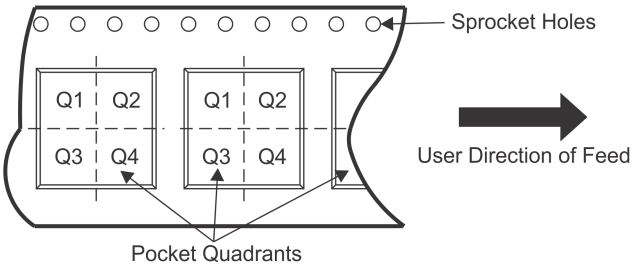


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

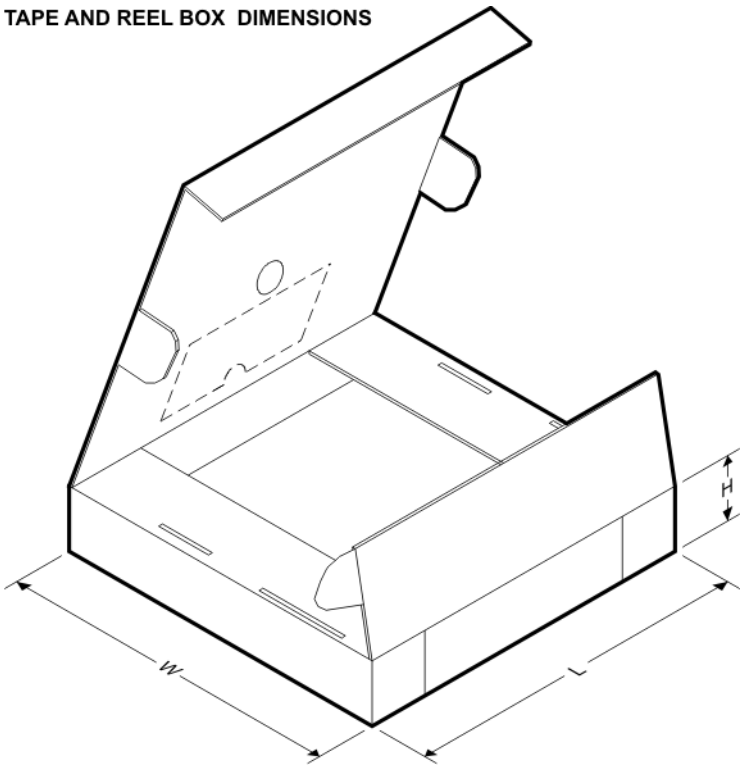
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55340QRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55340QRTETQ1	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

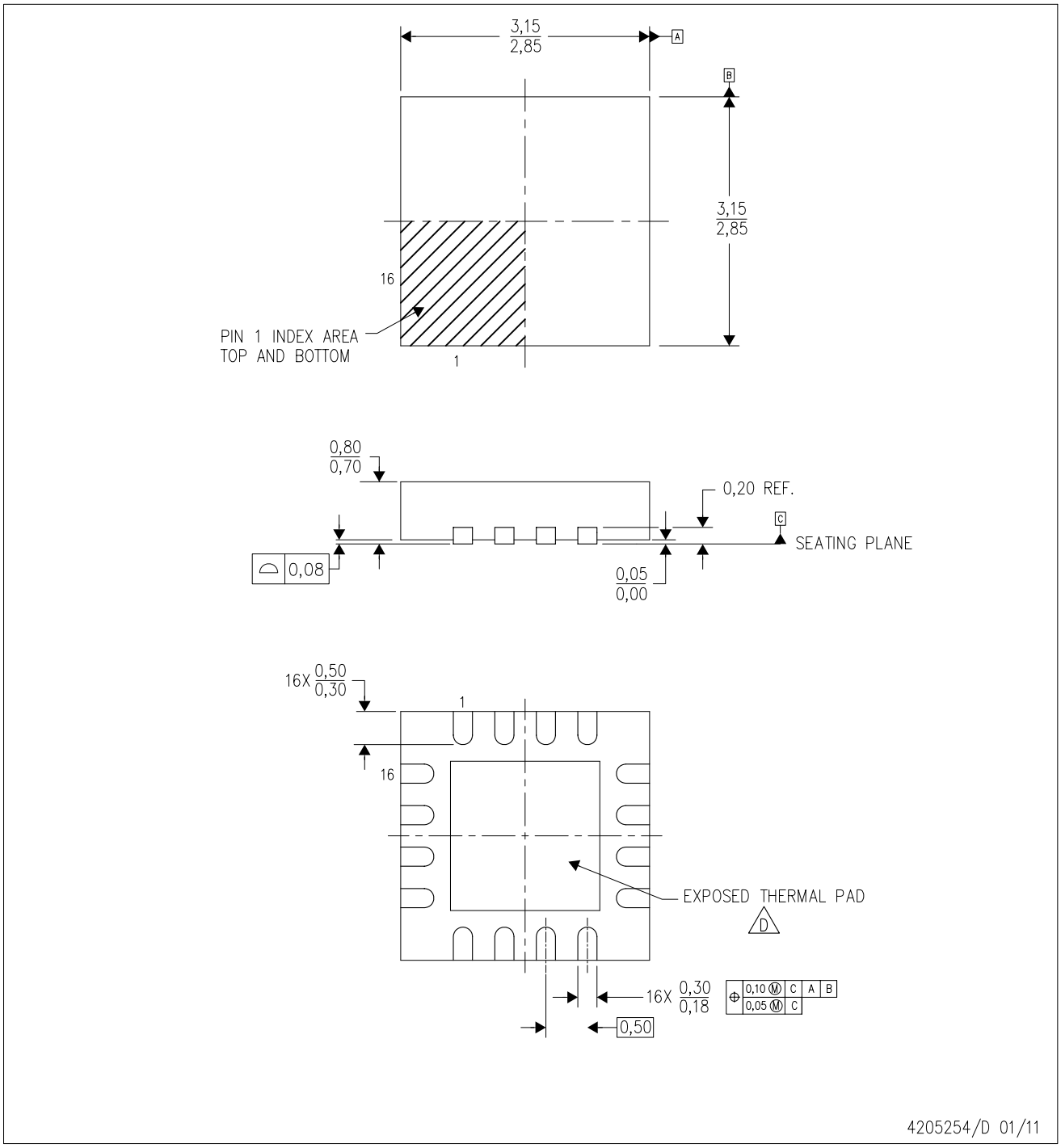
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55340QRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS55340QRTETQ1	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

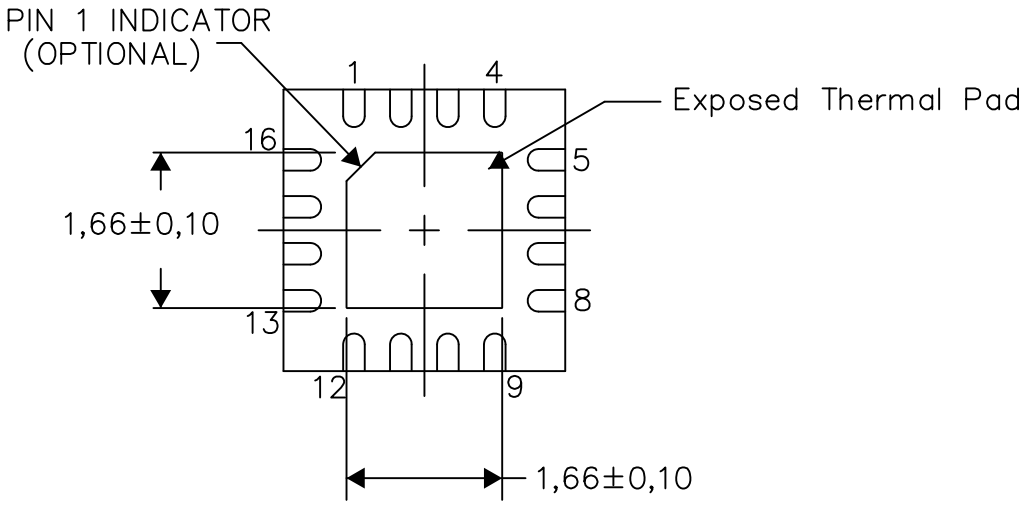
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



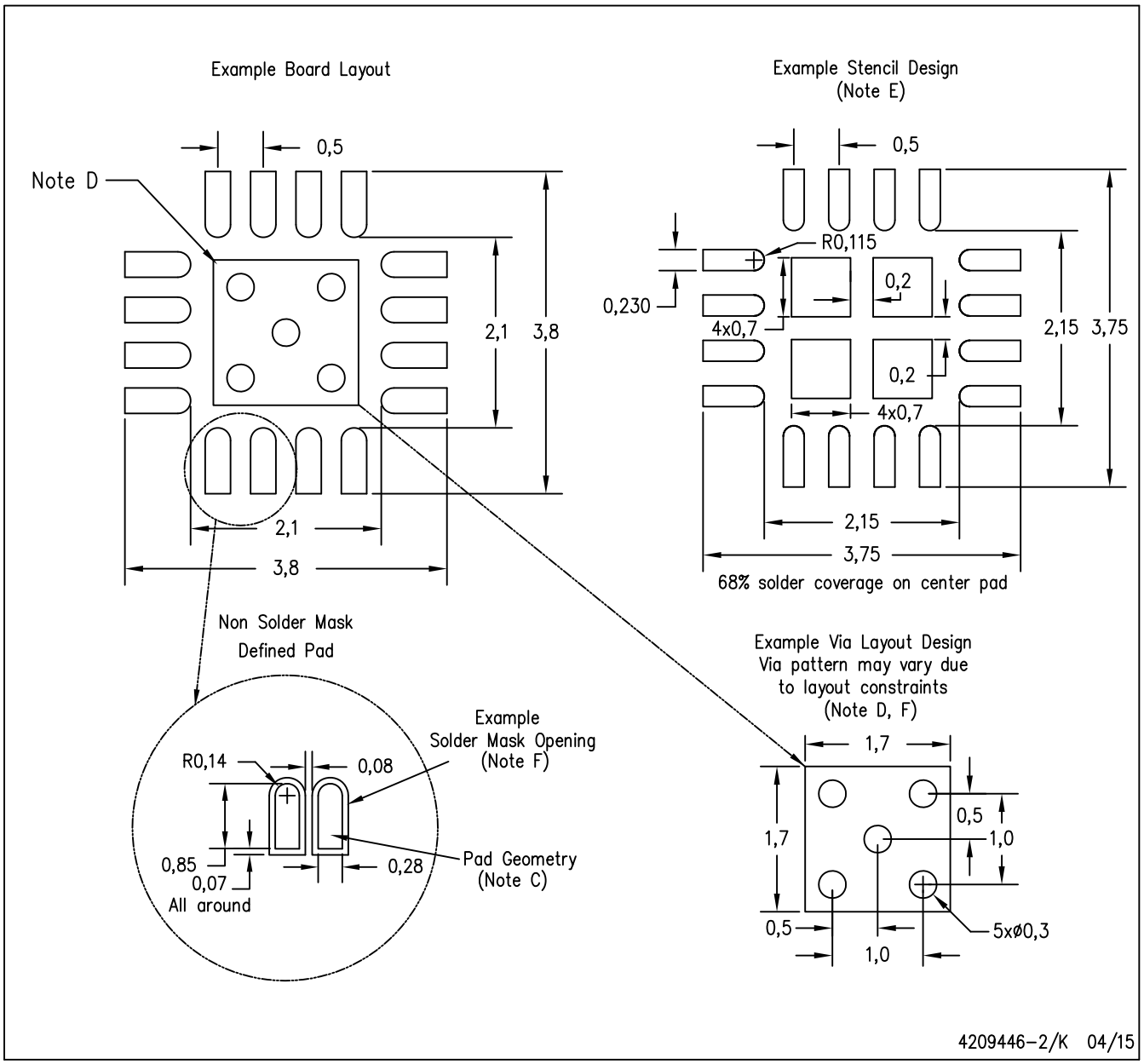
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

TPS61178x 20-V, 10-A Fully-Integrated Synchronous Boost with Load Disconnect Control

1 Features

- Input Voltage Range: 2.7 V to 20 V
- Output Voltage Range: 4.5 V to 20 V
- Programmable Switch Peak Current: up to 10 A
- Two 16-mΩ FETs Integrated
- Efficiency up to 96%: V_{IN} = 7.2 V, V_{OUT} = 16 V, I_{OUT} = 2 A
- Adjustable Switching Frequency: up to 2.2 MHz
- External Clock Synchronization: 200 kHz to 2.2 MHz
- Gate Driver for Load Disconnect
- Hiccup Short Protection
- Over Voltage Protection
- Auto PFM Operation - TPS61178
- Forced PWM Mode - TPS611781
- 3.0-mm x 3.5-mm 13-pin VQFN Hotrod Package
- Create a Custom Design Using the TPS61178 With the WEBENCH® Power Designer

2 Applications

- Portable Speaker
- Source Driver of LCD Display
- Supply for the Power Amplifier
- Supply for the Motor Driver
- USB Type-C Power Delivery

3 Description

The TPS61178x family is a 20-V synchronous Boost converter with the gate driver built-in for load disconnect. The TPS61178x integrates two low on-resistance power FETs: A 16-mΩ switching FET and a 16-mΩ rectifier FET.

The TPS61178x uses the fixed frequency peak current mode control with the slope compensation integrated. At the light load, the TPS61178 enters into the auto PFM mode while TPS611781 is in the forced PWM mode.

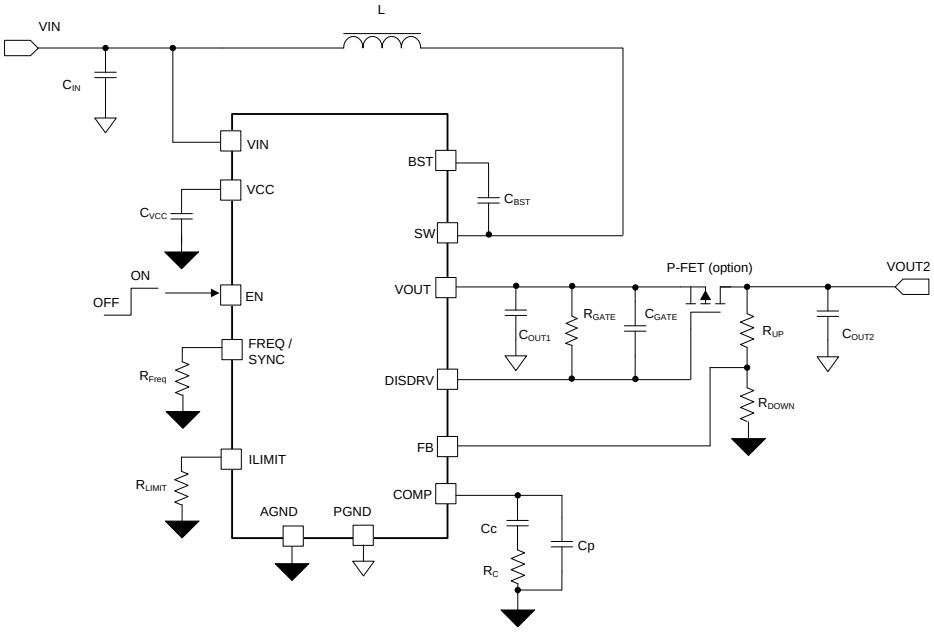
The TPS61178x could isolate the output from input side when shutdown. Once the output is shorted, it enters into the hiccup mode to lower the thermal stress and can recover automatically after the short releases. Additionally, the TPS61178x also has OVP and thermal protection to avoid the fault operation. The TPS61178x is in a 3.0-mm x 3.5-mm 13-pin VQFN package with enhanced thermal dissipation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61178	QFN (13)	3.00 mm × 3.5 mm
TPS611781		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2019) to Revision E — **Page**

- Restored hyperlink cross reference at the Thermal Information table footnote. ... 4
- Deleted right-hand column (A/B/S) in the Electrical Characteristics table. ... 5

Changes from Revision C (March 2018) to Revision D — **Page**

- Corrected term 1–DR to 1–D in Equation 21 ... 23

Changes from Revision B (September 2017) to Revision C — **Page**

- Changed Equation 21 ... 23

Changes from Revision A (April 2017) to Revision B — **Page**

- Changed graphs for Figure 1 through Figure 6 to include 3-A load ... 7

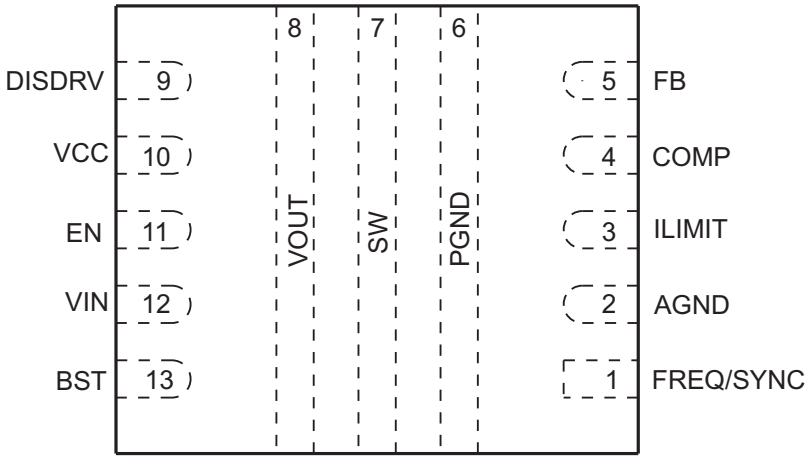
Changes from Original (February 2017) to Revision A — **Page**

5 Device Comparison Table

Part Number	Operation Mode at Light Load
TPS61178	Auto PFM
TPS611781	Forced PWM

6 Pin Configuration and Functions

(RNW)
(13-Pin QFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
FREQ / SYNC	1	I	The switching frequency is programmed by a resistor between this pin and the AGND. The internal oscillator can be synchronized by an external clock connecting into this pin. This pin can not be float in application.
AGND	2	-	Analog signal ground of the IC. Connect the AGND to PGND via a single point on the printed circuit board.
ILIMIT	3	I	Programming the switching peak current limit by a resistor between this pin and AGND.
COMP	4	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and AGND.
FB	5	I	Output voltage feedback, a resistor divider connecting to this pin sets the output voltage.
PGND	6	PWR	Power ground
SW	7	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power FET and the source of the internal high-side power FET.
VOUT	8	PWR	Boost converter output
DISDRV	9	O	A gate drive output for the external disconnect FET. Connect the DISDRV pin to the gate of the external FET. Leave it floating if not using the load disconnect function.
VCC	10	O	Output of the internal regulator. A ceramic capacitor of more than 1.0 µF is required between this pin and ground
EN	11	I	Enable logic input. Logic high level enables the device and low level shutdown the device.
VIN	12	I	IC power supply input.
BST	13	O	Power supply for high-side FET gate driver. A capacitor must be connected between this pin and the SW pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage range at terminals [2]	BST	–0.3	SW + 7	V
	VIN, SW, VOUT, DISCRG, EN	–0.3	23	V
	VCC, FB, COMP, FREQ / SYNC, ILIMIT	–0.3	7	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ [1] Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[2]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[3]	±750	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		20	V
V_{OUT}	Outputvoltage	4.5		20	V
L	Effective inductance range	0.47	3.3		µH
R_{FB}	Feedback resistance (low side)			200	kΩ
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS61178 RNR (QFN Package) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report..

7.5 Electrical Characteristics

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

			MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		20	V
V_{IN_UVLO}	Input voltage under voltage lockout (UVLO) threshold	V_{IN} rising		2.6	2.7	V
		V_{IN} falling		2.2	2.3	
V_{IN_HYS}	VIN UVLO hysteresis			400		mV
V_{CC}	VCC regulation voltage	ICC = 5mA, VIN = 8V		6		V
V_{CC_UVLO}	VCC UVLO threshold	VCC falling		2.1		V
I_Q (TPS61178)	Quiescent current into V_{IN} pin	IC enabled, no load, no ext. FET V_{IN} = 6 V, V_{OUT} = 20 V, V_{FB} = 1.3 V, T_J up to 85 ºC		1.5	3	µA
	Quiescent current into V_{IN} pin	IC enabled, no load, no ext. FET V_{IN} = 20 V, V_{OUT} = 20 V, V_{FB} = 1.3 V,T_J up to 85 ºC		270	320	µA
	Quiescent current into V_{OUT} pin	IC enabled, no load, no ext. FET V_{IN} = 6 V, V_{FB} = 1.3 V, V_{OUT} = 20 V, T_J up to 85 ºC		250	300	µA
	Quiescent current into V_{OUT} pin	IC enabled, no load, no ext. FET V_{IN} = 20 V, V_{OUT} = 20 V, V_{FB} = 1.3 V, T_J up to 85 ºC		5	12	µA
I_{SD}	Shutdown current into V_{IN} pin	IC disabled, V_{IN} = 6 V, –40 °C ≤ T_J ≤ 85°C		1	3.5	µA
		IC disabled, VIN = 20 V, –40 °C ≤ T_J ≤ 85°C		3	6	µA
I_{LS_LKG}	Reverse leakage current into SW	IC disabled, VIN = V_{OUT} = SW = 20 V –40 °C ≤ T_J ≤ 85°C		0.1	6.5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage range	Freq = 500kHz	4.5		20	V
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 8 V, V_{OUT} rising	20.5	21	21.5	V
POWER SWITCHES						
$R_{DS(on)}$	High-side MOSFET on resistance	V_{CC} = 6 V		16	25	mΩ
	Low-side MOSFET on resistance	V_{CC} = 6 V		16	25	mΩ
Gm	Power stage trans-conductance (peak current ratio with comp voltage)	V_{CC} = 6 V		12		A/V
CURRENT LIMIT						
I_{LIM_SW}	TPS61178	R_{LIMIT} = 80.6 kΩ	6.4	8	9.4	A
I_{LIM_SW}	TPS611781	R_{LIMIT} = 80.6 kΩ	5.7	7.4	8.7	A
I_{LIM_SHORT}	TPS61178 short current limit			20		A
VOLTAGE REFERNCE						
V_{REF}	Reference Voltage at FB pin	PWM mode	1.180	1.198	1.210	V
		PFM mode		101%		V_{REF}
I_{FB_LKG}	Leakage current into FB pin			10	60	nA
EN / SYNC LOGIC						
V_{EN_H}	EN Logic high threshold				1.2	V
V_{EN_L}	EN Logic Low threshold		0.4			V

Electrical Characteristics (continued)

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

			MIN	TYP	MAX	UNIT
R_{EN}	EN pulldown resistor			800		kΩ
V_{SYNC_H}	SYNC clock high threshold				1.2	V
V_{SYNC_L}	SYNC clock low threshold		0.4			V
ERROR AMPLIFIER						
V_{COMPH}	COMP output high voltage	High threshold, V_{FB} = V_{REF} - 200 mV		1.9		V
V_{COMPL}	COMP output low voltage	Low threshold, V_{FB} = V_{REF} + 200 mV		1.25		V
G_{mEA}	Error amplifier trans conductance	V_{COMP} = 1.5 V		195		uS
I_{SINK}	Comp pin sink current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1.5 V		20		uA
I_{SOURCE}	Comp pin source current	V_{FB} = V_{REF} –200 mV, V_{COMP} = 1.5 V		20		uA

7.6 Timing Requirements

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

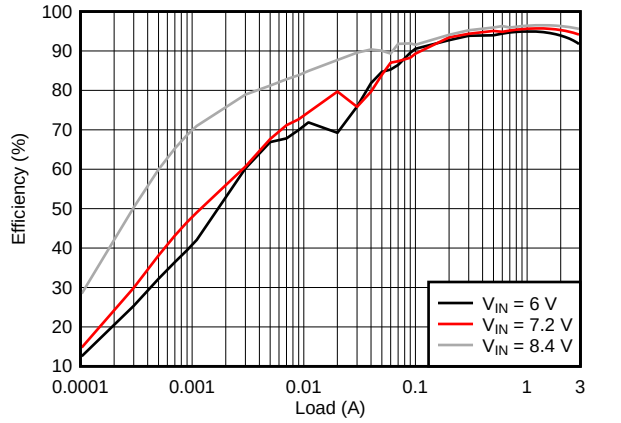
			MIN	TYP	MAX	UNIT
CURRENT LIMIT						
t_{SHORT_ON}	Short active time			4		ms
t_{SHORT_OFF}	Time for Auto retry protection off time			90		ms
SOFT START						
$t_{STARTUP}$	Startup time	V_{IN} = 8 V, V_{OUT} = 16 V		3.2		ms
t_{PRE_CHARG}	Pre charge time	Pre charge time	1.8	2.6	3.4	ms
PROTECTION						
t_{SD_R}	Thermal shutdown rising threshold	TJ rising		150		°C
t_{SD_F}	Thermal shutdown falling threshold	TJ falling		130		°C

7.7 Switching Characteristics

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

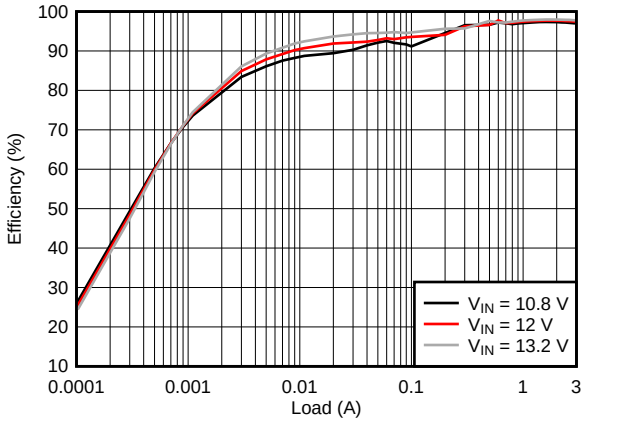
			MIN	TYP	MAX	Unit
SWITCHING FREQUENCY / SYNC						
f_{SW}	Switching frequency	R_{FREQ} = 342 kΩ	400	500	600	kHz
		R_{FREQ} = 842 kΩ	160	200	240	kHz
		R_{FREQ} = 75 kΩ	1900	2200	2500	kHz
t_{ON_min}	Minimum on time			105	135	ns
t_{OFF_min}	Minimum off time			140	180	ns
f_{SYNC_MIN}	Min Frequency using external clock		190	200	210	kHz
f_{SYNC_MAX}	Max Frequency using external clock		2090	2200	2310	kHz
GATE DRIVER FOR LOAD DISCONNECT						
I_{GH_SINK}	External PFET drive current			55		uA

7.8 Typical Characteristics



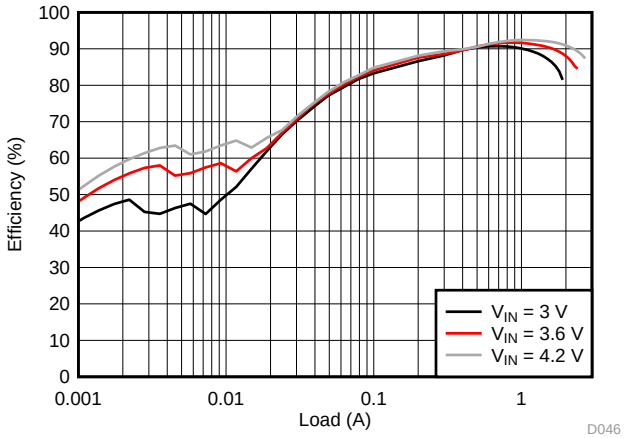
V_{OUT} = 16 V L = 3.3 µH Auto PFM

Figure 1. Efficiency vs. Output Current



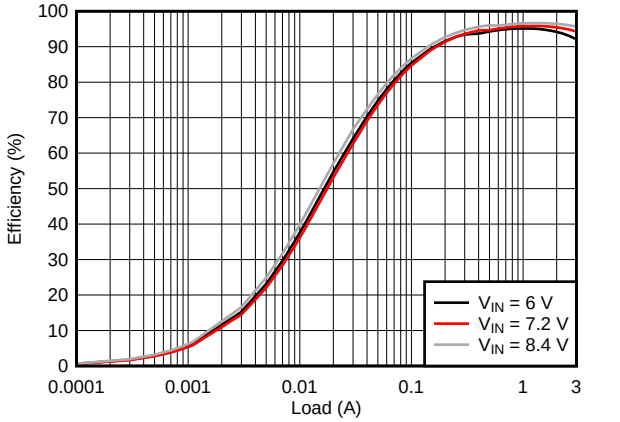
V_{OUT} = 16 V L = 3.3 µH Auto PFM

Figure 2. Efficiency vs. Output Current



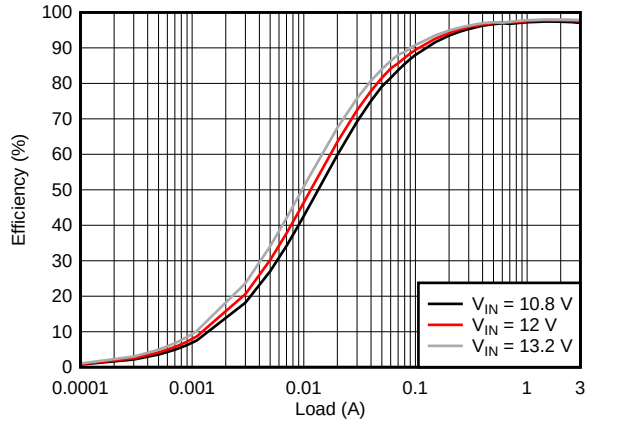
V_{OUT} = 14 V L = 1.8 µH Auto PFM

Figure 3. Efficiency vs. Output Current



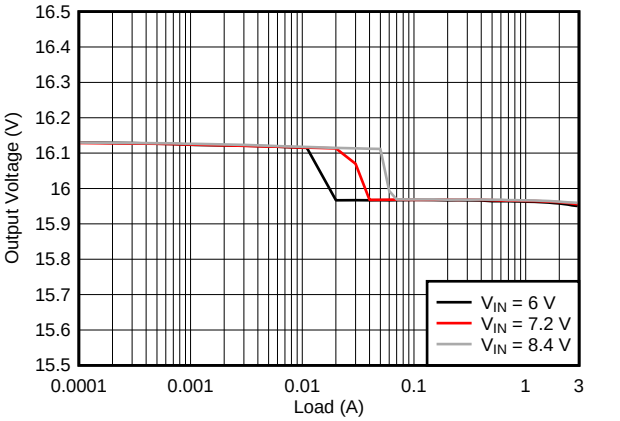
V_{OUT} = 16 V L = 3.3 µH Forced PWM

Figure 4. Efficiency vs. Output Current



V_{OUT} = 16 V L = 3.3 µH Forced PWM

Figure 5. Efficiency vs. Output Current



V_{OUT} = 16 V L = 3.3 µH Auto PFM

Figure 6. Output Voltage vs. Load

Typical Characteristics (continued)

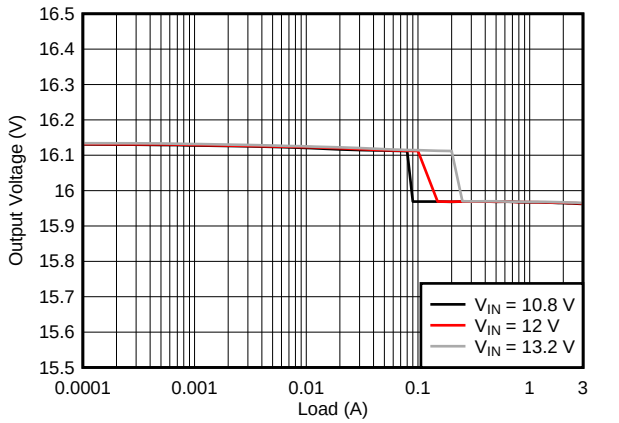


Figure 7. Output Voltage vs. Load

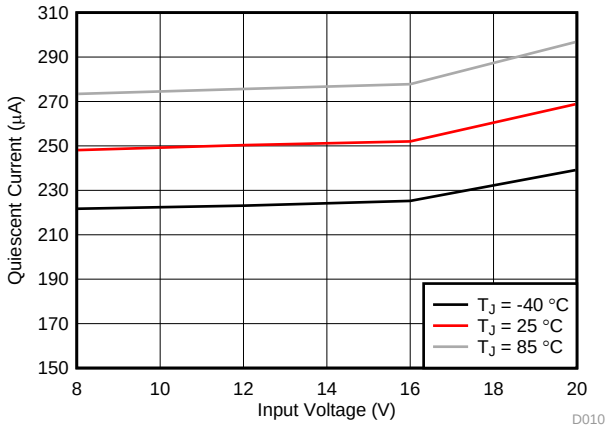


Figure 8. Quiescent Current vs V_{IN}

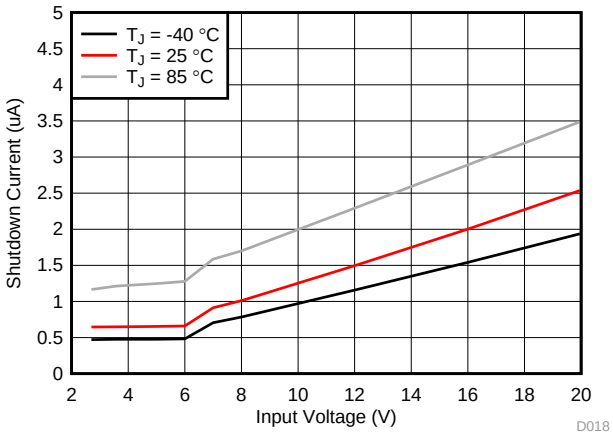


Figure 9. Shutdown Current vs V_{IN}

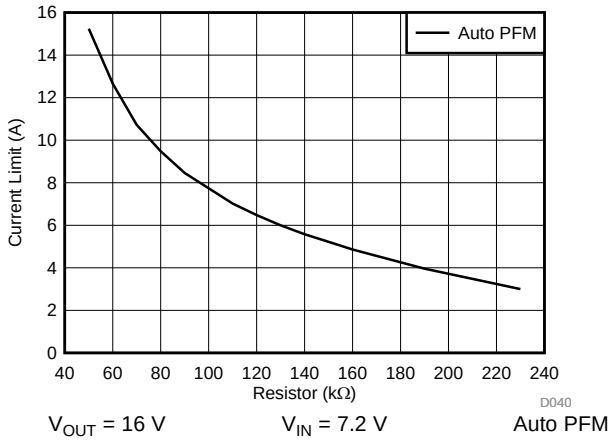


Figure 10. Switch Current Limit vs Setting Resistor

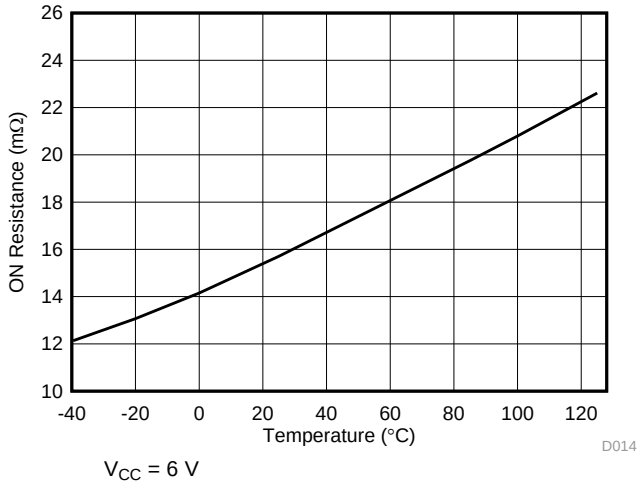


Figure 11. LS Rdson vs Temperature

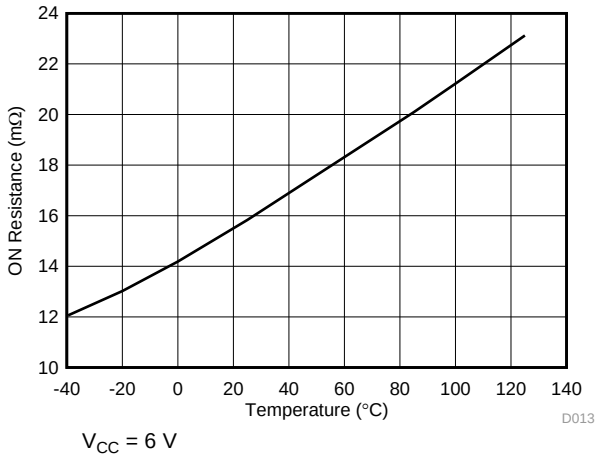


Figure 12. HS Rdson vs Temperature

Typical Characteristics (continued)

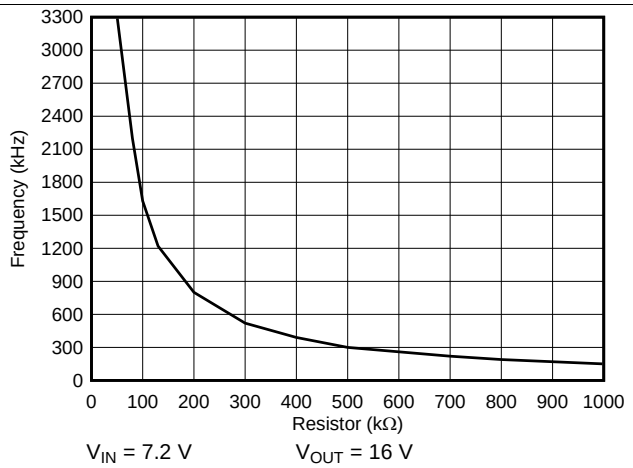


Figure 13. Frequency vs Setting Resistor

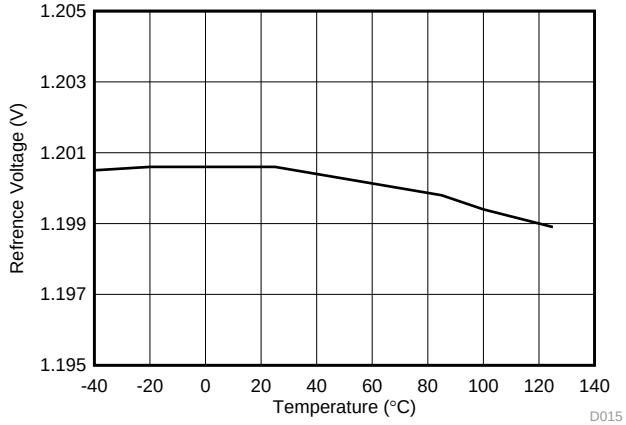


Figure 14. Reference Voltage vs Temperature

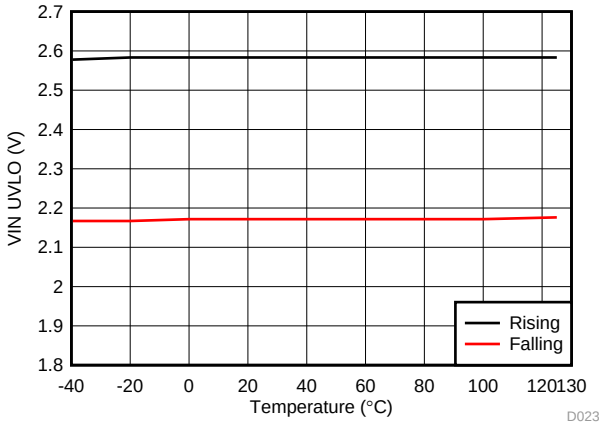


Figure 15. V_{IN} UVLO Rising / Falling vs Temperature

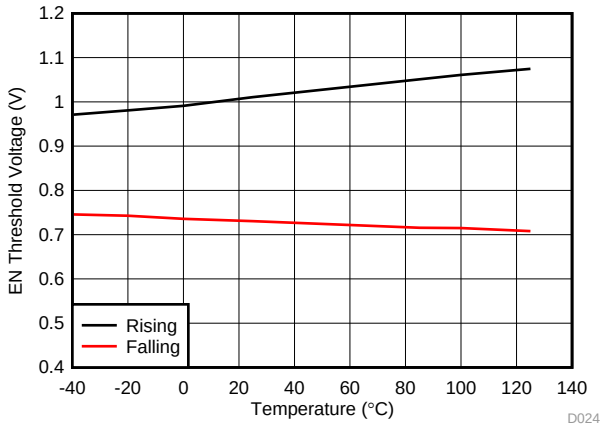


Figure 16. EN Threshold Rising / Falling vs Temperature

8 Detailed Description

8.1 Overview

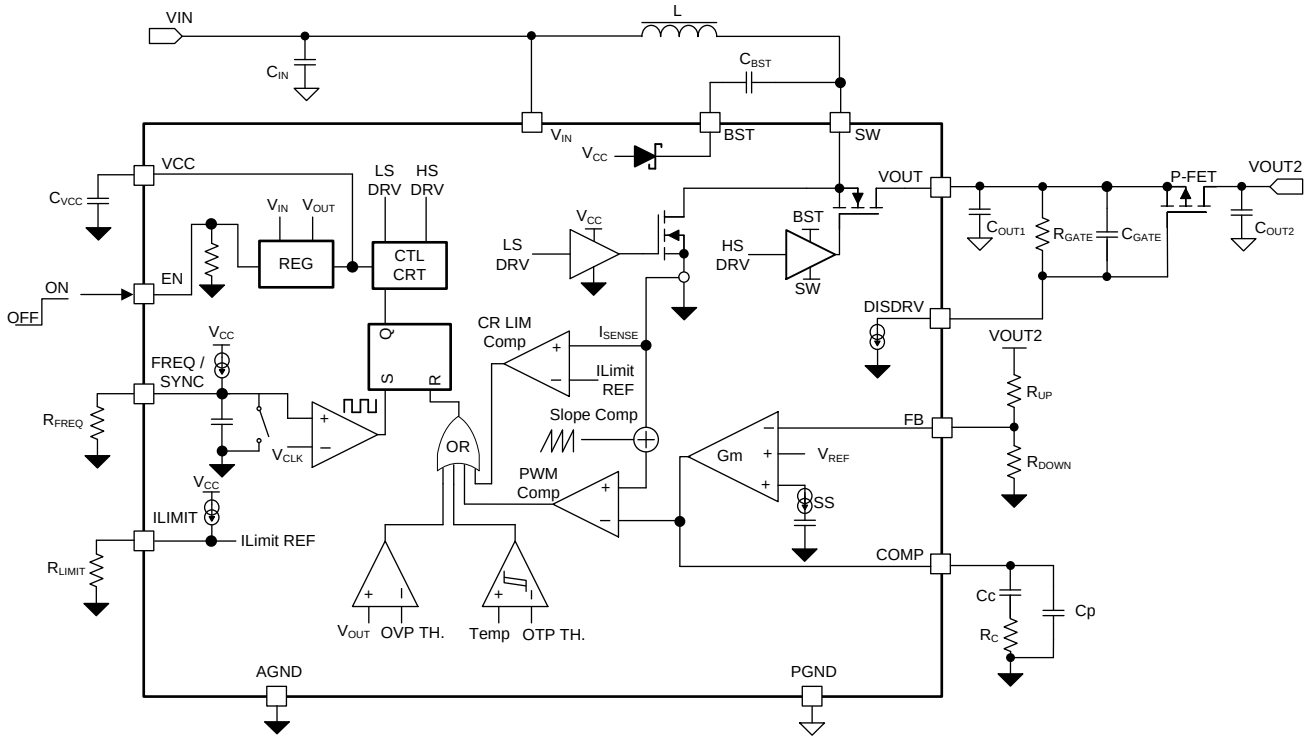
The TPS61178x family is a synchronous boost converter designed for delivering the switch peak current up to 10 A and output voltage reaching to 20 V. The TPS61178x family operates at a fixed frequency pulse-width modulation (PWM) at the moderate to heavy load currents. At the light load current, the TPS61178 operates in the PFM mode while the TPS611781 operates in the Forced PWM mode. The PFM mode brings the high efficiency crossing the entire load range while the Forced PWM mode can avoid the noise interference at the light load.

With the peak current mode control scheme, the TPS61178x provides the excellent line and load transient response with the minimal output capacitance. The external loop compensation brings the flexibility to use a wider range of the inductor and output capacitor combinations.

The TPS61178x supports the adjustable switching frequency up to 2.2 MHz. The device implements a cycle-by-cycle current limit to protect the device from overload during the boost operation phase. Additionally, if the output current further increases and exceeds the short current threshold or the output voltage drops below the short threshold. The TPS61178x triggers the hiccup short protection and recovers automatically once the short condition releases.

Additionally, the TPS61178x provides the gate driver for the external FET to isolate the output from input end during shutdown.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Under-voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.3 V. A hysteresis of 400 mV is added so that the device cannot be enabled again until the input voltage exceeds 2.7 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.3 V and 2.7 V.

8.3.2 Enable and Disable

When the input voltage is above UVLO rising threshold of 2.7 V and the EN pin is pulled high above 1.2 V, the TPS61178X is enabled. When the EN pin is pulled below 0.4 V, the TPS61178x goes into the shutdown mode and stops switching.

8.3.3 Startup

When the input voltage to the device exceeds the UVLO threshold and EN pin pulled to high as well, the TPS61178x starts to ramp up the output voltage. There is a switching pre-charge phase and the output voltage is charged up to 10% higher than the input voltage (1.1 x V_{IN}). The switching frequency is a fixed 500 kHz at the pre-charge phase.

After the pre-charge phase ends (typical 2.6 ms), The TPS61178x regulates the FB pin to the internal soft start voltage and results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft start time is typical 3.2 ms, which helps the regulator to gradually reach the steady state setting point, thus reducing the startup stresses and surges. The switching frequency follows the oscillator setting by the resistor connecting with the FREQ / SYNC pin.

If the device is synchronized by the external clock, the switching frequency is fixed 500 kHz at the soft start phase and changes to the external clock when the soft start phase ends.

8.3.4 Load Disconnect Gate Driver

The TPS61178 device provides a DISDRV pin to drive the external FET at the output side, which completely disconnects the output from the input end during shutdown or output short happens. During the device's start-up phase, the disconnect FET is controlled by the gate driver voltage of the external disconnect FET, there is an internal 55 µA (typical) sink current. The load disconnect FET connection is shown as *Figure 17*

The driver voltage and turn on / off timing can be set via the resistor and capacitor connecting between with the DISDRV pin and the source of the external FET. See the Application and Implementation section for the details of how to select the gate resistor and capacitor

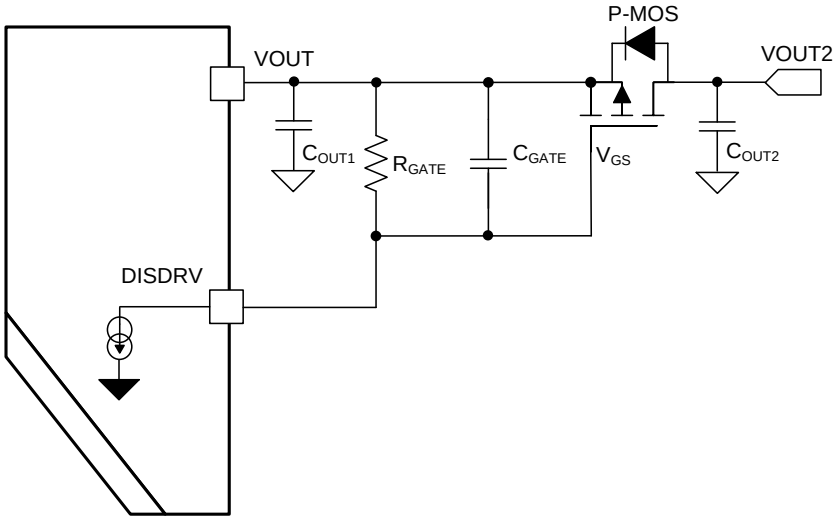


Figure 17. The Load Disconnect FET Connected

Feature Description (continued)

8.3.5 Adjustable Peak Current Limit

When the TPS61178x is in the normal boost switching phase, the device is prevented from the over current condition via the cycle by cycle current limit by sensing the current through the internal low-side FET. When the peak switch current triggers the current limit threshold, the low-side switch turns off to prevent the switching current further increasing.

The peak switch current limit can be set by a resistor connecting with the I_{LIMIT} pin. The relationship between the current limit and the resistor is determined by Equation 1

$$R_{LIMIT} = \frac{745}{I_{LIMIT}} \tag{1}$$

Where R_{LIMIT} is the resistor for setting the current limit, with the unit of kΩ, I_{LIMIT} is switching peak current limit, the unit is A. For instance, when the resistor value is 50 kΩ, the switch peak current limit is 15 A.

Figure 18 shows the current limit versus the setting resistor for both TPS61178 (Auto PFM) and TPS611781 (Forced PWM) with 7.2-V input to 16-V output.

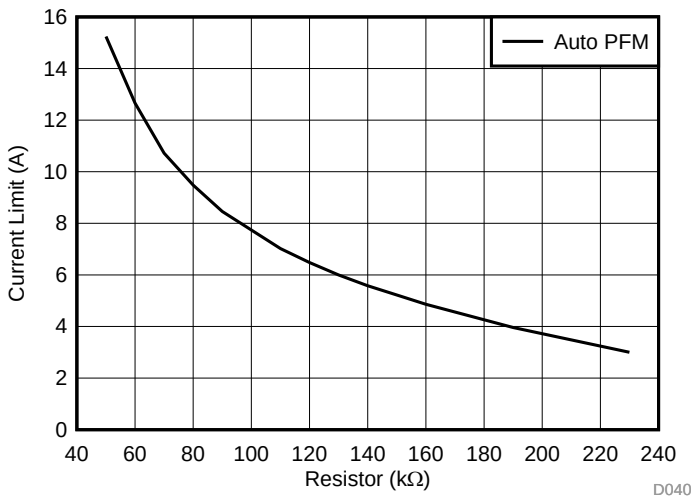


Figure 18. Switch Current Limit vs. Setting Resistor

The current limit value varies with the duty cycle, Figure 30 shows the bench measurement current limit at different duty cycles at R_{LIMIT} = 80.6 kΩ.

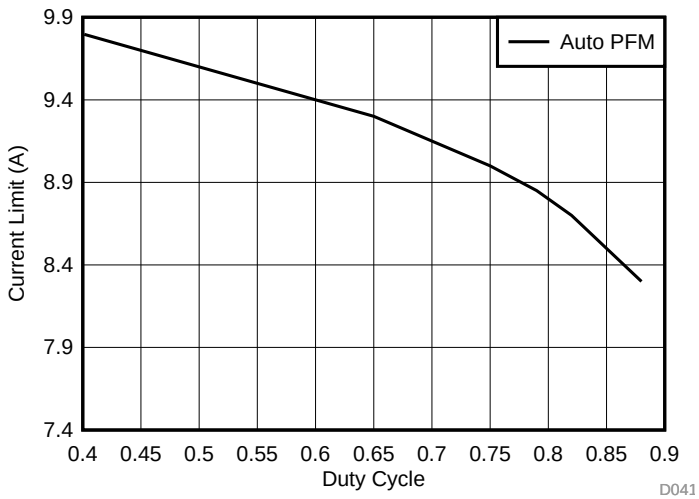


Figure 19. Switch Current Limit vs. Duty Cycle

Feature Description (continued)

For the TPS611781, which works in the Forced PWM mode at the light load, the current limit is typically 0.8 A lower than TPS61178 (Auto PFM) with the same setting resistor.

8.3.6 Output Short Protection (with load disconnected FET)

In addition to the cycle-by-cycle current limiting, the TPS61178x also has the output short protection. If the inductor current reaches the short protection limit threshold (typical 20A) or the output voltage drops below 30% (typical) of the normal output voltage, the device enters into the hiccup protection mode. In the hiccup mode, the device shuts down itself and restarts after 90ms (typical) waiting time which helps to reduce the total thermal dissipation. After the short condition releases, the device can recover automatically and restart the start-up phase. The hiccup protection scheme is illustrated in Figure 20.

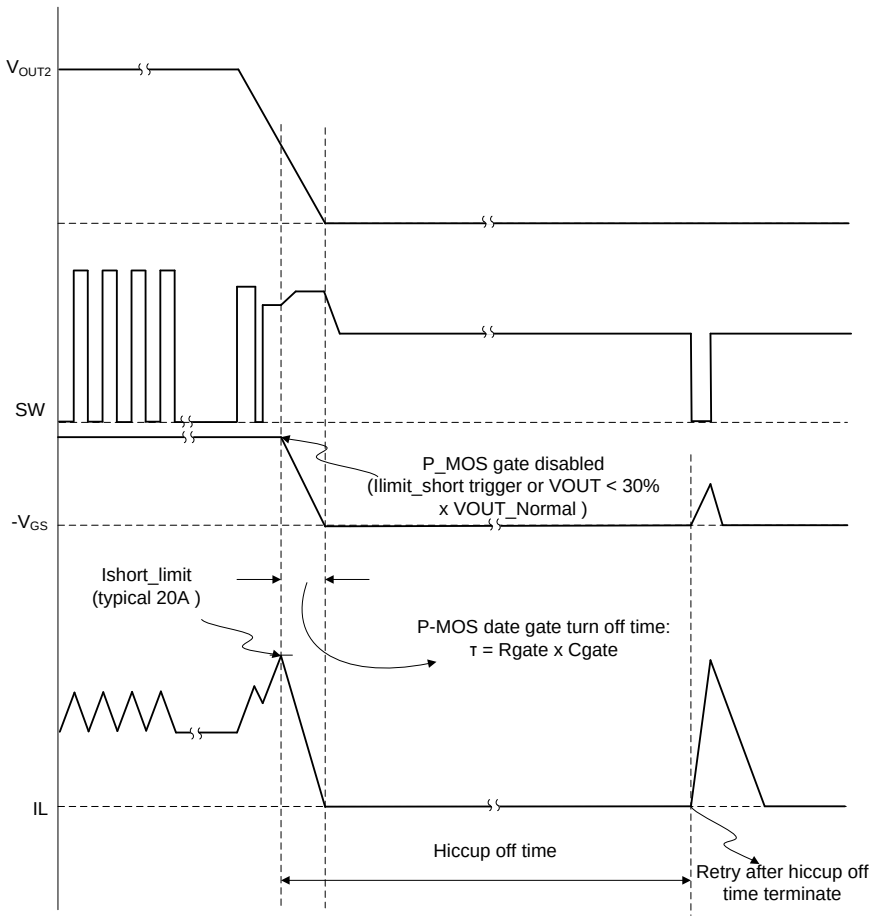


Figure 20. Output Short Protection

8.3.7 Adjustable Switching Frequency

The TPS61178x features of a wide adjustable switching frequency ranging up to 2.2 MHz. The switching frequency is set by a resistor connecting with the FREQ / SYNC pin. This pin cannot be left floating in the application. Use Equation 2 and Equation 3 to calculate the resistor value for a desired frequency.

$$T = \frac{1}{Freq} = k \times C_{FREQ} \times R_{FREQ} + T_{DELAY} \tag{2}$$

$$R_{FREQ} = \frac{\frac{1}{Freq} - T_{DELAY}}{k \times C_{FREQ}}$$

where

Feature Description (continued)

- T_{DELAY} = 50 nS, k = 3, C_{FREQ} = 1.8 pF (3)

For instance, if the R_{FREQ} is 342 kΩ, the frequency is 500 kHz.

Figure 21 shows the switching frequency versus the setting resistor, which is measured with V_{OUT} = 16 V from V_{IN} = 7.2 V .

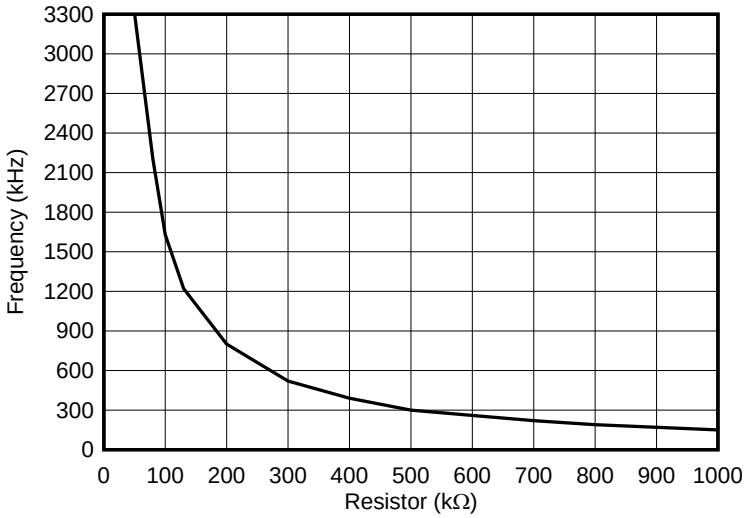


Figure 21. Switching Frequency vs Setting Resistor

8.3.8 External Clock Synchronization (TPS611781)

The FREQ/ SYNC pin can be used to synchronize the internal oscillator by an external clock. A positive voltage at the FREQ / SYNC pin must exceed the rising threshold (1.2 V) while must be lower than the falling threshold (0.4 V) to trip the internal synchronization pulse detector. The recommended frequency for the external clock is between 200 kHz and 2.2 MHz.

8.3.9 Error Amplifier

The TPS61178x has a trans-conductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft start voltage during startup phase). The trans-conductance of the error amplifier is 195 µA / V typically. The loop compensation components are required to be placed between the COMP terminal and ground to balance the loop stability and the transient response time.

8.3.10 Slope Compensation

The TPS61178x adopts the peak current mode control and adds a compensating ramp to the switch current signal. This slope compensation prevents the sub-harmonic oscillations when the duty cycle is larger than 50%. The available peak inductor current varies a little bit with operating duty cycles shown in Figure 19.

8.3.11 Start-up with the Output Pre-Biased

The TPS61178x has been designed to prevent the low-side FET from discharging a pre-biased output. During the pre-biased startup, both high-side and low-side FETs are not allowed to be turned on until the internal soft start voltage is higher than the sensed output voltage at FB pin.

8.3.12 Bootstrap Voltage (BST)

The TPS61178x has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

Feature Description (continued)

8.3.13 Over-voltage Protection

If the output voltage at the V_{OUT} pin is detected above over-voltage protection threshold, typically 21 V, the TPS61178x stops switching immediately until the voltage at the V_{OUT} pin drops lower than the output over-voltage protection threshold (with 500mV hysteresis). This function prevents the devices against the over-voltage and secures the circuits connected to the output from excessive over voltage.

8.3.14 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recover when the junction temperature falls below 130°C (typical).

8.4 Device Functional Modes

8.4.1 Operation

TPS61178x operates at the peak current-mode pulse-width-modulation (PWM). At the beginning of each switching cycle, the low-side FET switch turns on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. The PWM controller turns off the low-side FET when the peak inductor current reaches a threshold level set by the error amplifier output. After the low-side FET turns off, the high-side synchronous FET is turned on after a short dead time until the beginning of the next oscillator clock cycle or until the inductor current reaches the reverse current sense threshold.

During the portion of the switching cycle when the low-side FET is on, the input voltage is applied across the inductor and stores the energy as the inductor current ramps up. Meanwhile only the output capacitor supplies the load current. When it turns off the low-side FET, the inductor transfers the stored energy via the high-side synchronous FET to replenish the output capacitor and also supply the load current. This operation repeats every switching cycle.

The device features the internal slope compensation to avoid sub-harmonic oscillation that is intrinsic to peak-current mode control at duty cycle larger than 50%. The internal slope compensation may not be adequate to maintain stability for a very low inductance in application.

At the light load condition, the TPS61178x implements two options: Auto PFM mode (TPS61178) and Forced PWM mode (TPS611781) to meet different application requirements.

8.4.2 Auto PFM Mode (TPS61178)

The TPS61178 integrates a Power Save Mode with pulse frequency modulation (PFM) at the light load. When a light load condition occurs, the COMP pin voltage naturally decreases and reduces the peak current. When the COMP pin voltage further goes down with the load lowered and reaches the pre-set low threshold, the output of the error amplifier is clamped at this threshold and does not go down any more. If the load is further lowered, the output voltage of TPS61178 exceeds the nominal voltage and the device skips the switching cycles and regulate the output voltage at a higher threshold (typical 101%*V_{OUT_NORMAL}).

The Auto PFM mode reduces the switching losses and improves efficiency at the light load condition by reducing the average switching frequency.

8.4.3 Forced PWM Mode (TPS611781)

In the Forced PWM mode, the TPS611781 keeps the switching frequency being constant for the whole load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and delivers less power from input to output. The high-side FET is not turned off even if the current through the FET goes negative to keep the switching frequency being the same as that of the heavy load.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61178x family is the step up DC / DC converter. The following design procedure can be used to select component values for the TPS61178x. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an interactive design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

9.2 Typical Application

The application described is for 6-V to 14-V input, 16-V output converter.

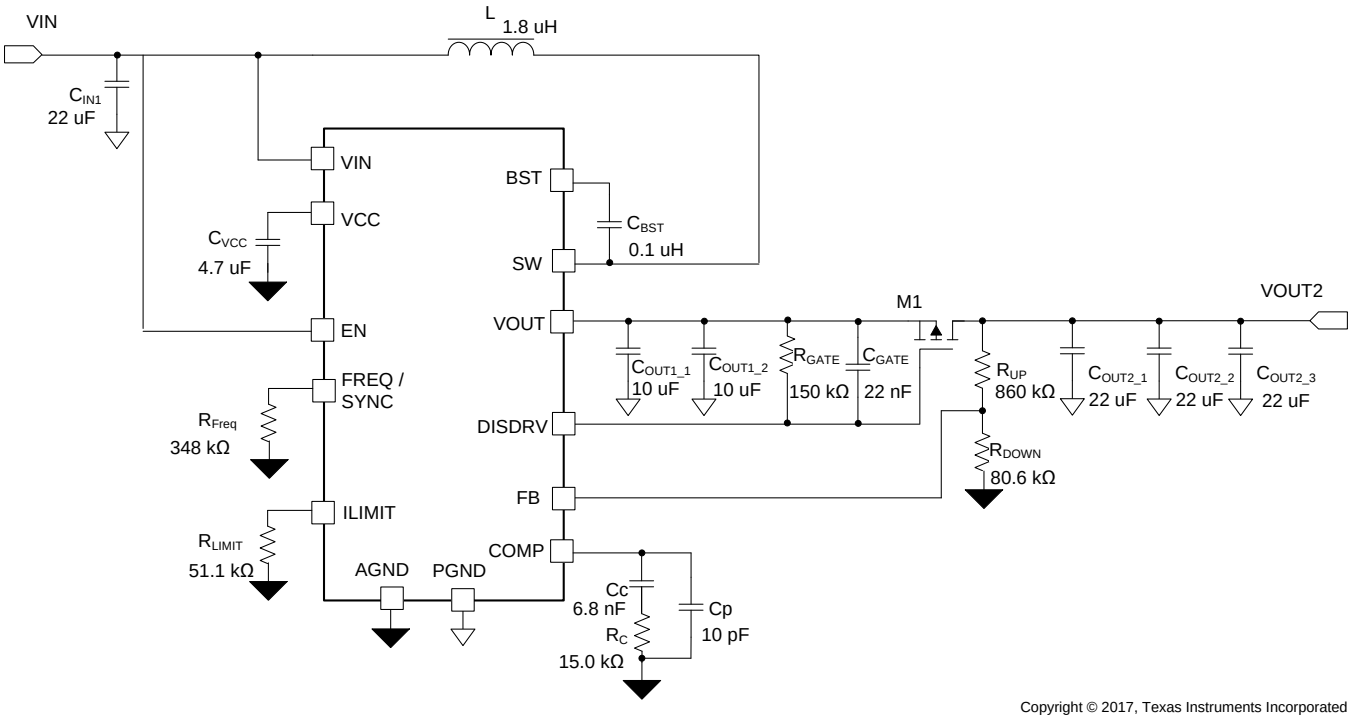


Figure 22. TPS61178 16-V Output with Load Disconnect Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use Table 1 as the design parameters.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	6 V to 14 V
Output voltage	16 V
Output ripple voltage	±3%
Output current rating	3 A
Operating frequency	500 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61178 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Output ripple voltage
- Output current rating
- Operating frequency
- Load disconnect needed or not

9.2.2.2 Setting the Switching Frequency

The switching frequency of the TPS61178 is set at 500 kHz. Use Equation 2 to calculate the required resistor value. The calculated value is 342 kΩ. Use the next higher standard value of 348 kΩ.

9.2.3 Setting the Current Limit

The current limit of the TPS61178 could be programmed by an external resistor. For a target current limit of 13 A, the calculated resistor value is 57 kΩ. However, the minimum current limit is around 1.6 A lower than the typical one. Here, selecting the 51.1 kΩ resistor to deliver 13-A peak current at the worst case.

9.2.4 Setting the Output Voltage

The output voltage of the TPS61178 is externally adjustable using a resistor divider network. The relationship between the output voltage and the resistor divider is given by Equation 4.

$$V_{OUT} = V_{FB} \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

where

- V_{OUT} is the output voltage
- R_{UP} the top divider resistor
- R_{DOWN} is the bottom divider resistor (4)

Choose R_{DOWN} to be approximately 80.6 kΩ. Slightly increasing or decreasing R_{DOWN} can result in closer output voltage matching when using standard value resistors. In this design, R_{DOWN} = 80.6 kΩ and R_{UP} = 1000 kΩ, resulting in an output voltage of 16 V.

For the best accuracy, R_{DOWN} is recommended to be smaller than 100 kΩ to ensure that the current following through R_{DOWN} is at least 100 times larger than FB pin leakage current. Changing R_{DOWN} towards the lower value increases the robustness against noise injection. Changing the R_{DOWN} towards the higher values reduces the quiescent current for achieving higher efficiency at the light load currents.

9.2.4.1 Selecting the Inductor

A boost converter normally requires two main passive components for storing the energy during the power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency) as well as the transient behavior and loop stability, which makes the inductor to be the most critical component in application.

When selecting the inductor, as well as the inductance, the other parameters of importance are:

- The maximum current rating (RMS and peak current should be considered),
- The series resistance,
- Operating temperature

Choosing the inductor ripple current with the low ripple percentage of the average inductor current results in a larger inductance value, maximizes the converter's potential output current and minimizes EMI. The larger ripple results in a smaller inductance value, and a physically smaller inductor, improves transient response but results in potentially higher EMI.

The rule of thumb to choose the inductor is that to make the inductor ripple current (ΔIL) is a certain percentage (Ripple % = 20 – 30 %) of the average current. The inductance can be calculated by Equation 5, Equation 6, and Equation 7:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{5}$$

$$\Delta I_{L\_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \tag{6}$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}}$$

where

- Δ_{IL} is the peak-peak inductor current ripple
- V_{IN} is the input voltage
- D is the duty cycle
- L is the inductor
- f_{SW} is the switching frequency
- Ripple % is the ripple ration versus the DC current
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- η is the efficiency (7)

The current flowing through the inductor is the inductor ripple current plus the average input current. During power-up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

The TPS61178x has built-in slope compensation to avoid sub-harmonic oscillation associated with the current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 4 A, the slope compensation may not be adequate, and the loop can be unstable. Therefore, it is recommended to make the peak-to-peak current ripple below 4 A when selecting the inductor.

Inductor values can have ± 20% or even ± 30% tolerance with no current bias. When the inductor current approaches the saturation level, its inductance can decrease 20% to 35% from the value at 0-A bias current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, the switching frequency, the input and output voltages and it can be calculated by Equation 8 and Equation 9.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L$$

where

- I_{PEAK} is the peak current of the inductor
- I_{IN} is the input average current
- Δ_{IL} is the ripple current of the inductor (8)

The input DC current is determined by the output voltage, the output current and efficiency can be calculated by :

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

where

- I_{IN} is the input current of the inductor
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency (9)

While the inductor ripple current depends on the inductance, the frequency, the input voltage and duty cycle calculated by Equation 5, replace Equation 5, Equation 9 into Equation 8 and get the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- η is the efficiency
- V_{IN} is the input voltage
- L is the inductor
- f_{SW} is the switching frequency (10)

The heat rating current (RMS) is as below:

$$I_{L\_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2}$$

where

- I_{L_RMS} is the RMS current of the inductor
- I_{IN} is the input current of the inductor
- Δ_{IL} is the ripple current of the inductor (11)

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print.

The following inductor series in Table 2 from the different suppliers are recommended. 74437368033 from Würth is used for this application case with balancing the size and power loss.

Table 2. Recommended Inductors for TPS61178x(1)

PART NUMBER	L (µH)	DCR Typ (mΩ) Max	SATURATION CURRENT / Heat Rating Current (A)	SIZE (L × W × H mm)	VENDOR(1)
744325180	1.8	3.5	18	5 x 10 x 4	Würth
74437368033	3.3	11.8	23 / 8	10 x 10 x 3.8	Würth
DFEH10040D-3R3M#	3.3	12	10 / 10	10.9 x 10 x 4	Murata / TOKO
PIMB104T-4R7MS	4.7	20.0	15 / 8.5	10.9 x 10 x 3.8	Cyntec
74437368068	6.8	17.5	14	11 x 10 x 3.8	Würth
74437368100	10	27	12.5	11 x 10 x 3.8	Würth

(1) See *Third-party Products Disclaimer*

9.2.4.2 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. Then the loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 12:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}}$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency (12)

The additional output ripple component caused by ESR is calculated by Equation 13:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR}$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor (13)

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using Equation 14:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}}$$

where

- ΔI_{STEP} is the transient load current step

- ΔV_{TRAN} is the allowed voltage dip for the load current step
- f_{BW} is the control loop bandwidth (i.e., the frequency where the control loop gain crosses zero) (14)

Care must be taken when evaluating a ceramic capacitor's derating under the DC bias. Ceramic capacitors can derate by as much as 70% of its capacitance at its rated voltage. Therefore, enough margins on the voltage rating should be considered to ensure adequate capacitance at the required output voltage.

In applications of TPS61178x, it is recommended to run the converter with a reasonable amount of effective output capacitance, for instance 3 x 22-µF X5R or X7R MLCC capacitors connected in parallel.

If the load disconnect FET is connected, the output capacitor should be split shown in Figure 23. C_{OUT2} should be no larger than 10 x C_{OUT1} to avoid the inrush current when turning on the disconnect FET.

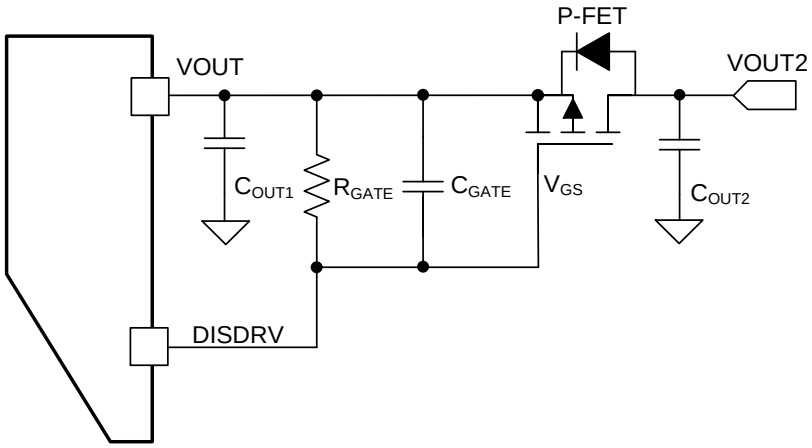


Figure 23. Output Capacitor Configuration with the Load Disconnect FET

9.2.4.3 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22-µF input capacitor is sufficient for the most applications, larger values may be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

9.2.4.4 Loop Stability and Compensation

9.2.4.4.1 Small Signal Model

The TPS61178x uses the fixed frequency peak current mode control; there is an internal adaptive slope compensation to avoid the sub-harmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with the loop compensation. Figure 24 shows the equivalent small signal elements of a boost converter.

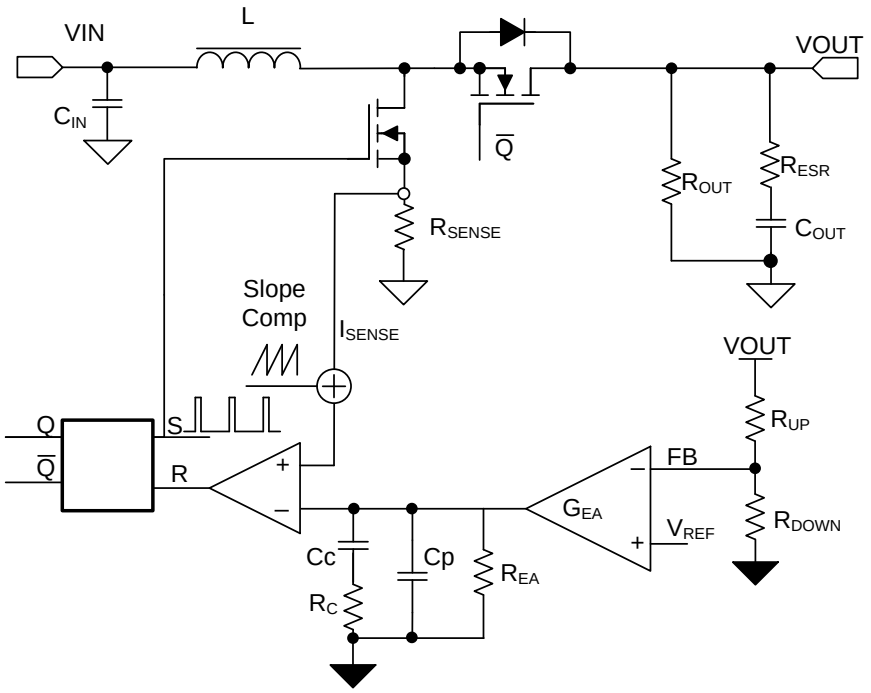


Figure 24. TPS61178x Control Equivalent Circuitry Model

The small signal of power stage including the slope compensation is:

$$G_{PS}(S) = \frac{R_{OUT} \times (1 - D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{S}{2\pi \times f_{ESR}}\right)\left(1 - \frac{S}{2\pi \times f_{RHP}}\right)}{1 + \frac{S}{2\pi \times f_P}} \times He(S)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- R_{SENSE} is the equivalent internal current sense resistor, which is typically 0.083 Ω of TPS61178x (15)

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}}$$

where

- C_{OUT} is the output capacitance, for a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance (16)

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor. (17)

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1 - D)^2}{2\pi \times L}$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- L is the inductance (18)

Using He(s) to model the inductor current sampling effect as well as the slope compensation effect on the small signal response, is shown in Equation 19

$$He(S) = \frac{1}{1 + \frac{S \times \left[(1 + \frac{Se}{Sn}) \times (1 - D) - 0.5 \right]}{f_{SW}} + \frac{S^2}{(\pi \times f_{SW})^2}} \tag{19}$$

$$Sn = \frac{V_{IN}}{L} \times R_{SENSE}$$

where

- Sn is the slew rate of the inductor current ramping up (20)

$$Se = 0.06 \times \frac{f_{SW}}{1 - D} \times R_{dson\_LS}$$

where

- Se is the slope compensation slew rate
- R_{dson_LS} is the on resistance of Low-side FET (21)

The slope compensation adaptively changes with the switching frequency and duty cycle.

He(s) models the inductor current sampling effect as well as the slope compensation effect on the small signal response. Note that if Sn > Se, e.g., when L is too small, the converter operates as a voltage mode converter and the above model no longer holds.

The TPS61178x COMP pin is the output of the internal trans-conductance amplifier.

Equation 22 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times \frac{1 + \frac{S}{2 \times \pi \times f_Z}}{(1 + \frac{S}{2 \times \pi \times f_{P1}}) \times (1 + \frac{S}{2 \times \pi \times f_{P2}})}$$

where

- k_{COMP} and R_{EA} are the ratio of peak current / comp voltage, for TPS61178x, the typical value is k_{COMP} = 12 A / V and R_{EA} = 20 MΩ.
- f_{P1}, f_{P2} is the pole's frequency of the compensation, f_Z is the zero's frequency of the compensation network. network (22)

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_c}$$

where

- C_C is the zero capacitor compensation (23)

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P}$$

where

- C_P is the pole capacitor compensation
- R_C is the resistor of the compensation network (24)

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \tag{25}$$

9.2.4.4.2 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Cross Over Frequency, f_C**
   - The first step is to set the loop crossover frequency, f_C. The higher crossover frequency, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. Then calculate the loop compensation network values of R_C, C_C, and C_P by following below equations.
2. **Set the Compensation Resistor, R_C**
   - By placing f_Z below f_C, for frequencies above f_C, R_C | | R_{EA} ~= R_C and so $R_C \times G_{EA}$ sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at f_Z, results in the total loop gain, $T_{(s)} = G_{PS(s)} \times H_{EA(s)} \times He(s)$ being zero at f_C.
   - Therefore, to approximate a single-pole roll-off up to f_{P2}, rearrange Equation 22 to solve for RC so that the compensation gain, K_{EA}, at f_C is the negative of the gain, K_{PS}, read at frequency f_C for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \tag{26}$$

   where
   - K_{EA} is gain of the error amplifier network
   - K_{PS} is the gain of the power stage
   - G_{EA} is the amplifier's trans-conductance, the typical value of G_{EA} = 195 µA / V
3. **Set the compensation zero capacitor, C_C**
   - Place the compensation zero at the power stage R_{OUT} ,C_{OUT} pole's position, so to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \tag{27}$$

   - Set $f_Z = f_P$, and get the

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \tag{28}$$

4. **Set the compensation pole capacitor, C_P**
   - Place the compensation pole at the zero produced by the R_{ESR} and the C_{OUT}, it is useful for canceling unhelpful effects of the ESR zero.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \tag{29}$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{30}$$

   - Set $f_{P2} = f_{ESR}$, and get the

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \tag{31}$$

   - If the calculated value of C_P is less than 10 pF, it can be neglected.

   Designing the loop for greater than 45° of phase margin and greater than 6-dB gain margin eliminates output voltage ringing during the line and load transient. The R_C = 15 kΩ , C_C = 6.8 nF, C_p = 10 pF for this design example.

9.2.4.4.3 Selecting the Disconnect FET

The TPS61178x provides a gate driver to control an external FET to disconnect the output from the input at shutdown or output short conditions, shown in Figure 25.

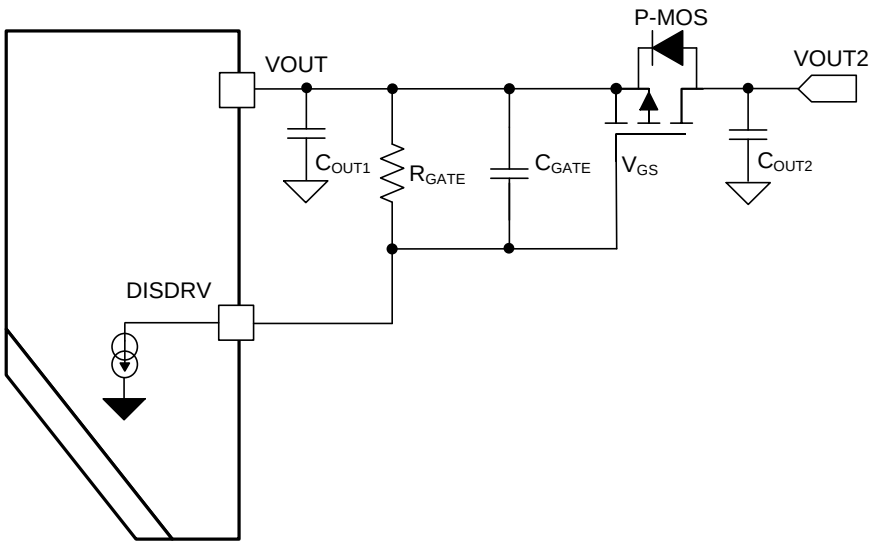


Figure 25. Load Disconnect FET Connection

The V_{DS}, I_{DS} and safe operation area (SOA) should be taken into consideration when selecting the FET:

- The drain-to-source voltage rating should be higher than the output max. voltage, $V_{DS\_DIS\_MAX} = V_{OUT}$,
- The drain-to-source RMS current rating is the maximum output current. $I_{DS\_DIS\_RMS} = I_{OUT}$,
- The SOA should be considered when the output short occurs, and there is heat caused by the short protection response time and surge current, SOA > Q_{SHORT}.

$$Q_{SHORT} = \frac{1}{2} \times V_{OUT} \times I_{SHORT} \times T_{SHORT}$$

where

- $V_{DS\_DIS\_Max}$ is the maximum drain-source voltage
- I_{DS_DIS} is the drain-source RMS current
- I_{SHORT} is the short current
- T_{SHORT} is the response time before the short protection triggered
- Q_{SHORT} is the heat produced for the output short (32)

For instance: V_{OUT} = 16 V, I_{SHORT} = 20 A , T_{SHORT} = 30 µs.
SOA ≥ 4.8 mJ, $V_{DS\_DIS\_MAX}$ ≥ 16 V.
The CSD25404Q3 –20 V P-Channel NexFET™ Power FET is used for this design example.

An additional capacitor between the gate and source of the external FET is required to slow the turn-on speed.

$$T_{ON\_PFET} = \frac{V_{TH\_PFET} \times C_{GS\_PFET}}{I_{DIS\_PFET}}$$

where

- T_{ON_PFET} is the on time of external FET
- V_{TH_PFET} is the gate threshold of external FET
- C_{GS_PFET} is the total gate capacitance of connected between gate and source external FET. (including the self-gate-source capacitance of the FET)
- $_{IDIS\_PFET}$ is the discharge current inside of TPS61178x, it is 55 µA typically (33)

Given 1.5 V threshold, C_{GS_PFET} is 10 nF, the T_{ON_PFET} is around 300 µs.Please be aware that the maximum turn-on time should not exceed 3 ms, and the maximum capacitance C_{GS_PFET} should be < 100 nF. Otherwise, the TPS61178x could not startup normally if the disconnect FET could not be turn on within the 3 ms.

The gate resistor depends on the gate-source voltage of the external FET,

$$V_{GATE} = R_{GATE} \times I_{DIS\_PFET} \quad (34)$$

$$R_{GATE} = \frac{V_{GATE}}{I_{DIS\_PFET}} \tag{35}$$

Given the 5-V V_{GATE}, the R_{GATE} = 100 kΩ

9.2.4.4.4 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1 µF to 1 µF. C_{BST} should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1 µF was selected for this design example.

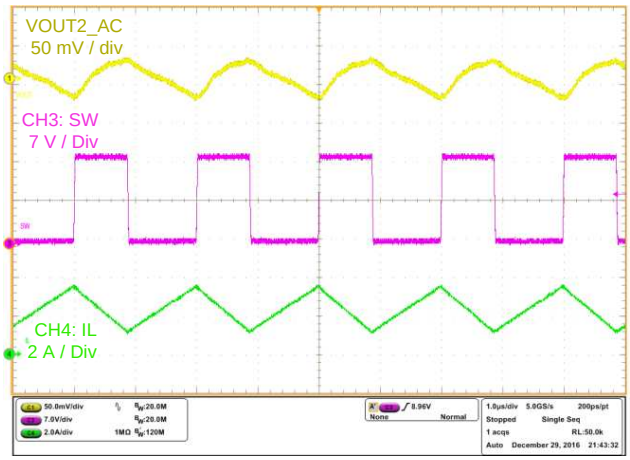
9.2.4.4.5 V_{CC} Capacitor

The primary purpose of the V_{CC} capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the V_{CC} regulator. The value of C_{VCC} should be at least 10 times greater than the value of C_{BST}, and should be a good quality, low ESR, ceramic capacitor. C_{VCC} should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7 µF was selected for this design example.

9.2.5 TPS61178 Application Waveform

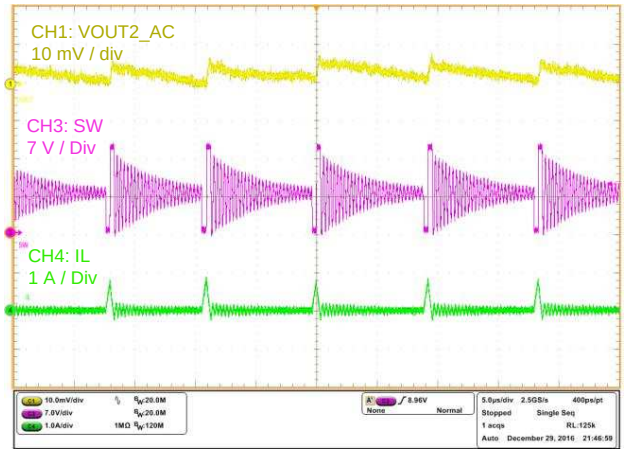
Typical condition V_{IN} = 6 V to 14 V, V_{OUT} = 16 V, R_{LIMIT} = 51.1 kΩ, R_{FREQ} = 348 kΩ

Application waveforms are measured with the inductor 3.3 µH, Würth 74437368033, and the output capacitance: 3 x 22 µF, GRM32ER61E226KE15L plus 2 x 10 µF, GRM188R61E106MA73D.



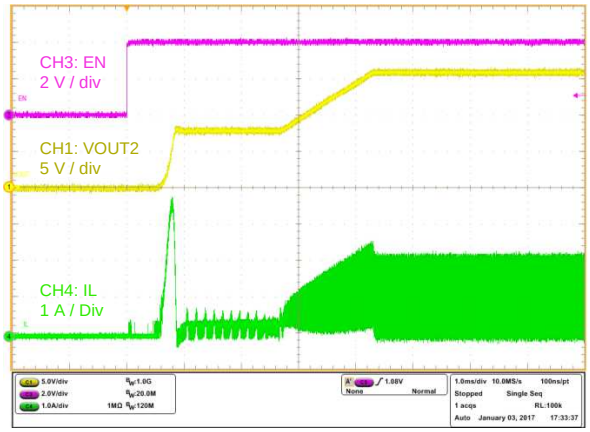
V_{IN} = 7.2 V V_{OUT}= 16 V
L = 3.3 µH C_{OUT}= 86 µF Load = 1000 mA

Figure 26. Steady State 1000 mA



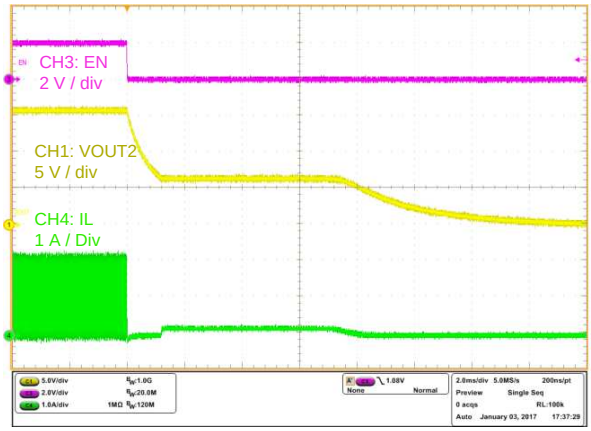
V_{IN} = 7.2 V V_{OUT}= 16 V Auto PFM
L = 3.3 µH C_{OUT}= 86 µF Load = 10 mA

Figure 27. Steady-state 10 mA



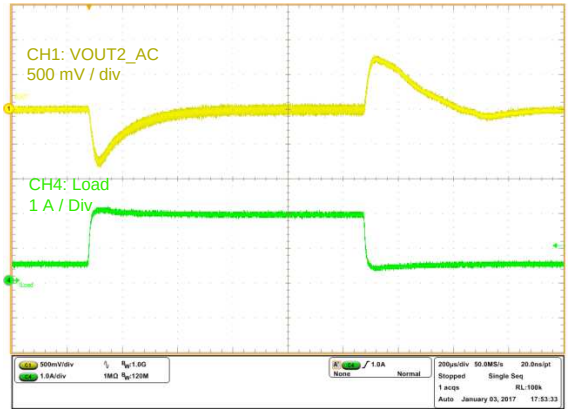
V_{IN} = 7.2 V V_{OUT}= 16 V Auto PFM
L = 3.3 µH C_{OUT}= 86 µF Load = 32 Ω

Figure 28. Startup by EN



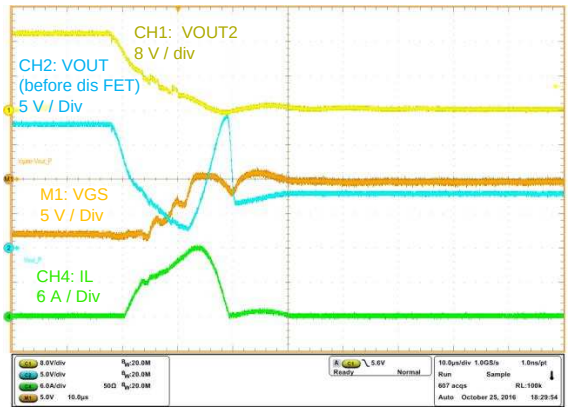
V_{IN} = 7.2 V V_{OUT}= 16 V Auto PFM
L = 3.3 µH C_{OUT}= 86 µF Load = 32 Ω

Figure 29. Shutdown by EN



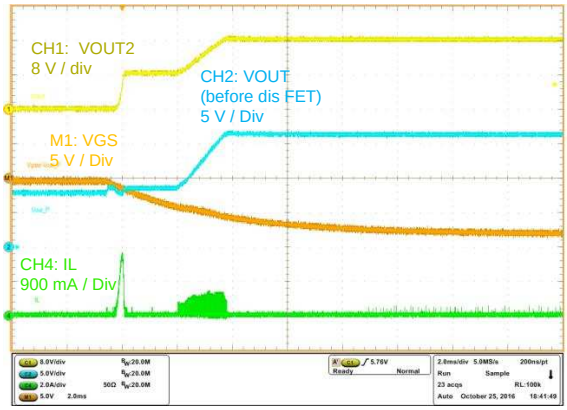
V_{IN} = 7.2 V V_{OUT}= 16 V Load = 500 mA to 2 A,
L = 3.3 µH C_{OUT}= 86 µF 0.1 A/µs slew rate

Figure 30. Load Transient



V_{IN} = 7.2 V V_{OUT}= 16 V
L = 3.3 µH C_{OUT}= 86 µF

Figure 31. Output Short (with Disconnect FET)



V_{IN} = 7.2 V V_{OUT}= 16 V
L = 3.3 µH C_{OUT}= 86 µF

Figure 32. Output Short Release (with Disconnect FET)

9.3 System Examples

9.3.1 TPS61178 with 14-V Output from 2.7-V to 4.4-V Input Voltage

The Figure 33 is the typical application schematic for 2.7-V to 4.4-V input (single cell Li+ battery) to output 14-V output converter. The inductor can be lower to 1.8 µH for the 14-V output.

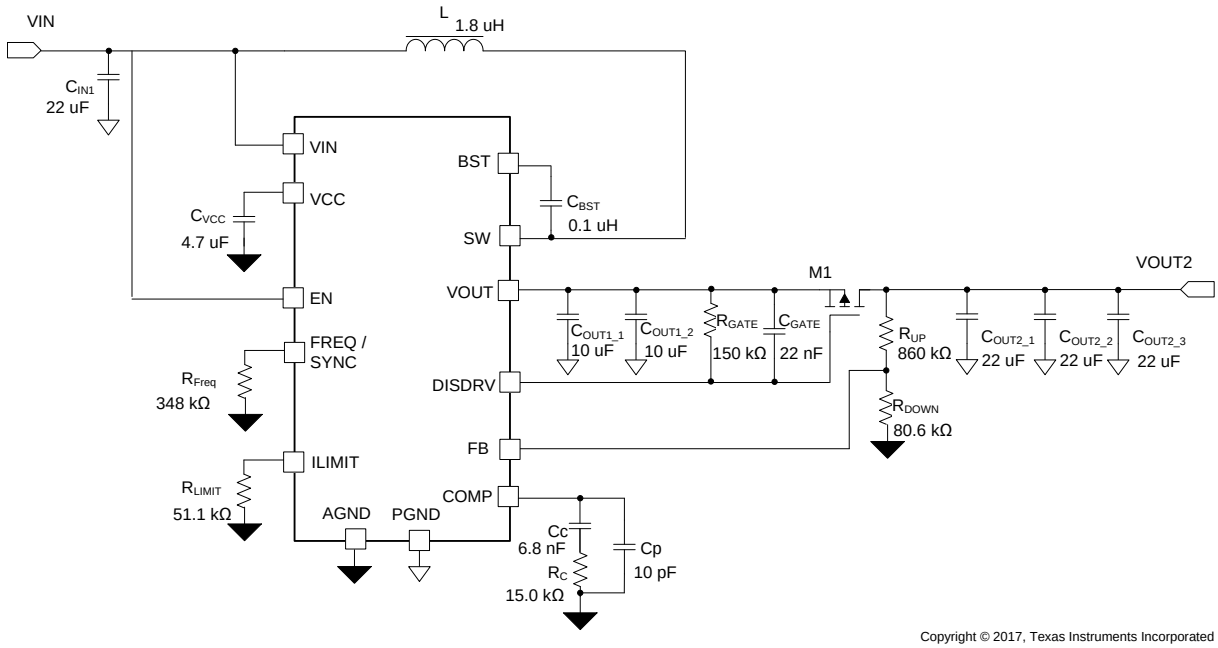


Figure 33. 14-V Output Voltage from 2.7-V to 4.4-V Input Voltage

9.3.2 TPS61178 Without Load Disconnect Function

The Figure 34 is the typical application schematic is for 6-V to 14-V input (2 / 3 cells Li+ battery or 12-V bus) to output 14-V output converter without load disconnect. With removing the load disconnect FET, it simplifies the design and minimizes the external components.

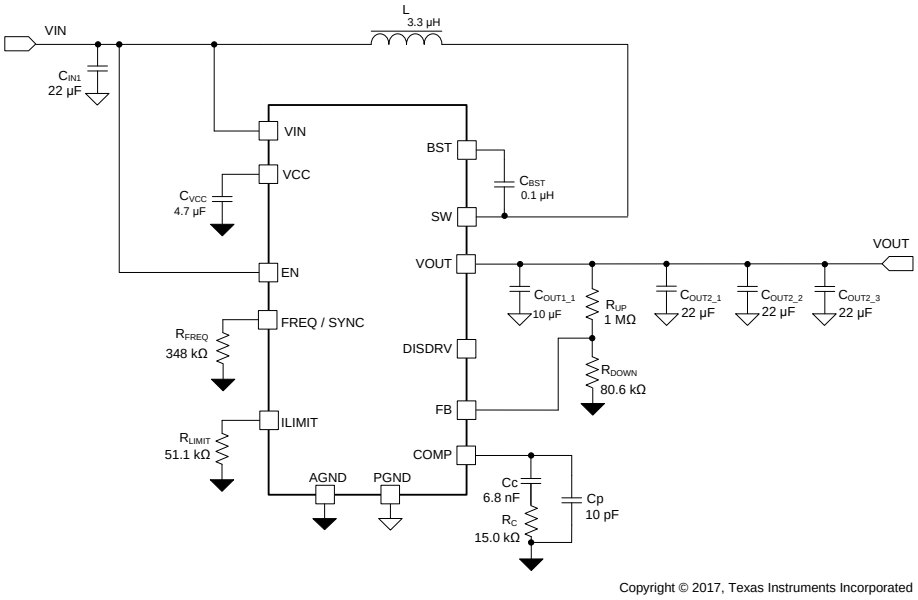


Figure 34. 16-V Output Voltage Without Load Disconnect Function

System Examples (continued)

9.3.3 TPS611781 External Clock Synchronization

The Figure 35 is the typical application schematic for synchronized by an external clock of 2.2 MHz. It is for the Forced PWM mode operation to avoid the noise-sensitive frequency range, for instance the audible noise and AM band.

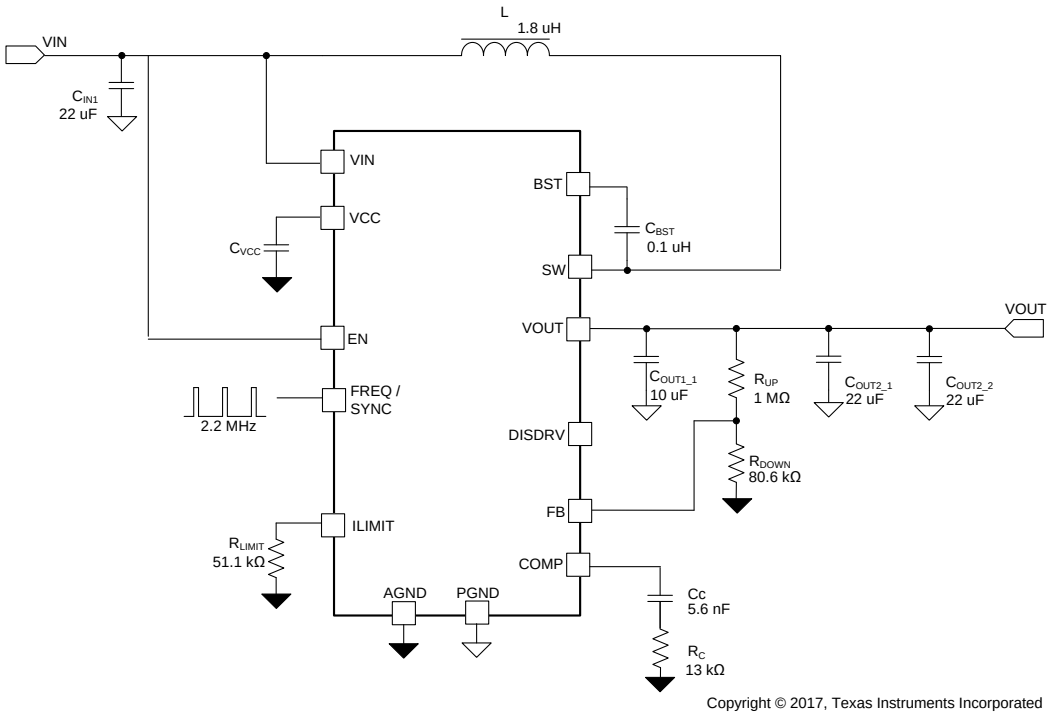


Figure 35. 16-V Output Voltage Synchronized by 2.2 MHz External Clock

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply ranging from 2.7 V to 20 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS61178x, the bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems.

The checklist below is suggested that be followed to get good performance for a well-designed board:

1. Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di/dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise;
2. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize inter plane coupling;
3. Use a combination of bulk capacitors and smaller ceramic capacitors with low series resistance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for decoupling the noise;
4. The ground area near the IC must provide adequate heat dissipating area. Connect the wide power bus (e.g., V_{OUT}, SW, GND) to the large area of copper, or to the bottom or internal layer ground plane, using vias for enhanced thermal dissipation;
5. Place the input capacitor being close to the V_{IN} pin and the PGND pin in order to reduce the input supply ripple;
6. Place the noise sensitive network like the feedback and compensation being far away from the SW trace;
7. Use a separate ground trace to connect the feedback, compensation, frequency set, and the current limit set circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.

11.2 Layout Example

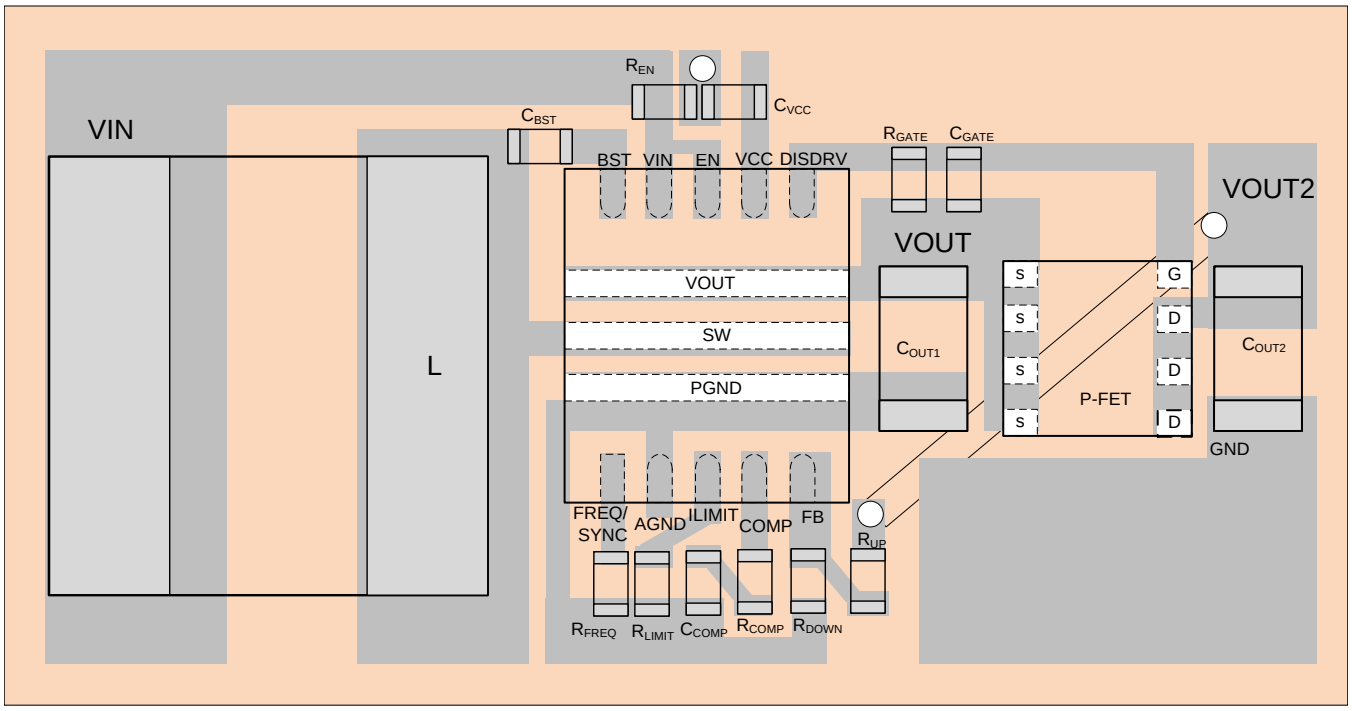


Figure 36. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61178 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- TPS61178EVM Evaluation Board User's Guide, SLVUB05
-

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61178	Click here	Click here	Click here	Click here	Click here
TPS611781	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS611781RNWR	ACTIVE	VQFN-HR	RNW	13	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1CDI	Samples
TPS611781RNWT	ACTIVE	VQFN-HR	RNW	13	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1CDI	Samples
TPS61178RNWR	ACTIVE	VQFN-HR	RNW	13	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	15RI	Samples
TPS61178RNWT	ACTIVE	VQFN-HR	RNW	13	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	15RI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

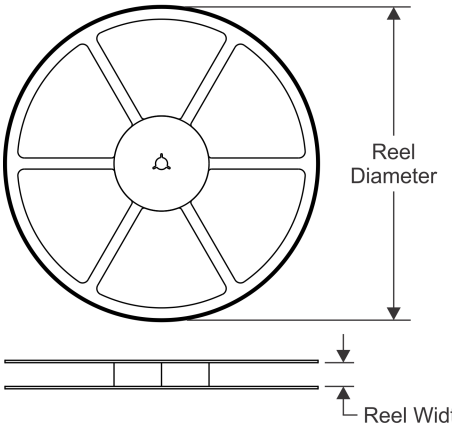
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

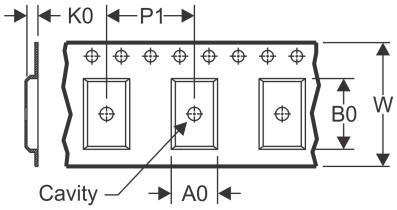
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

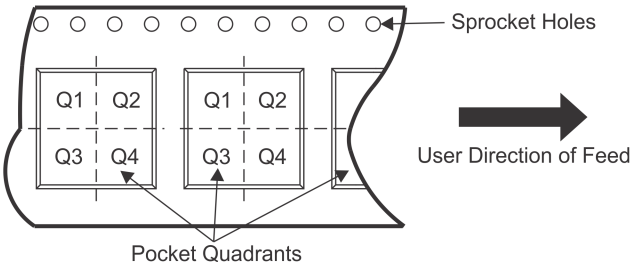


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

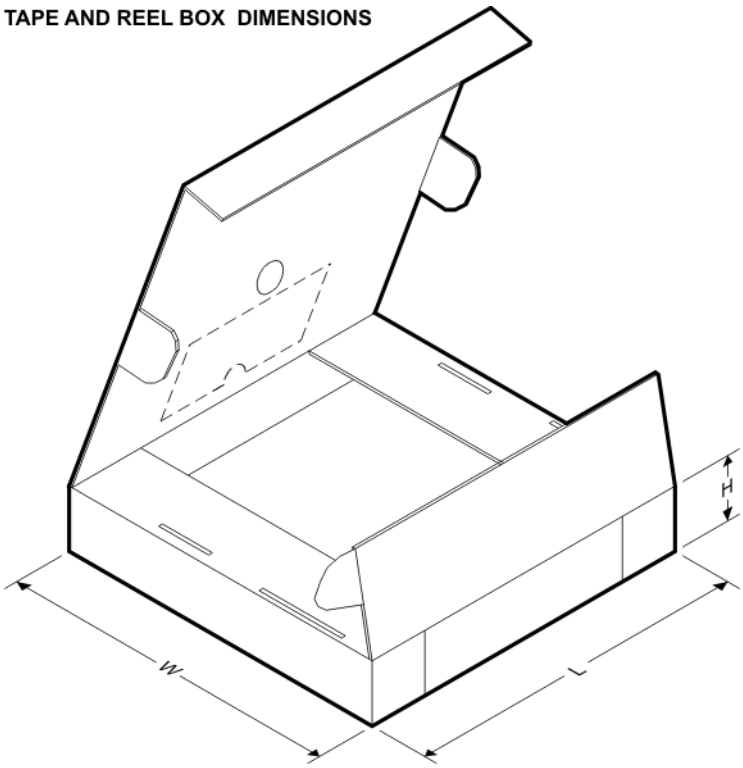
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

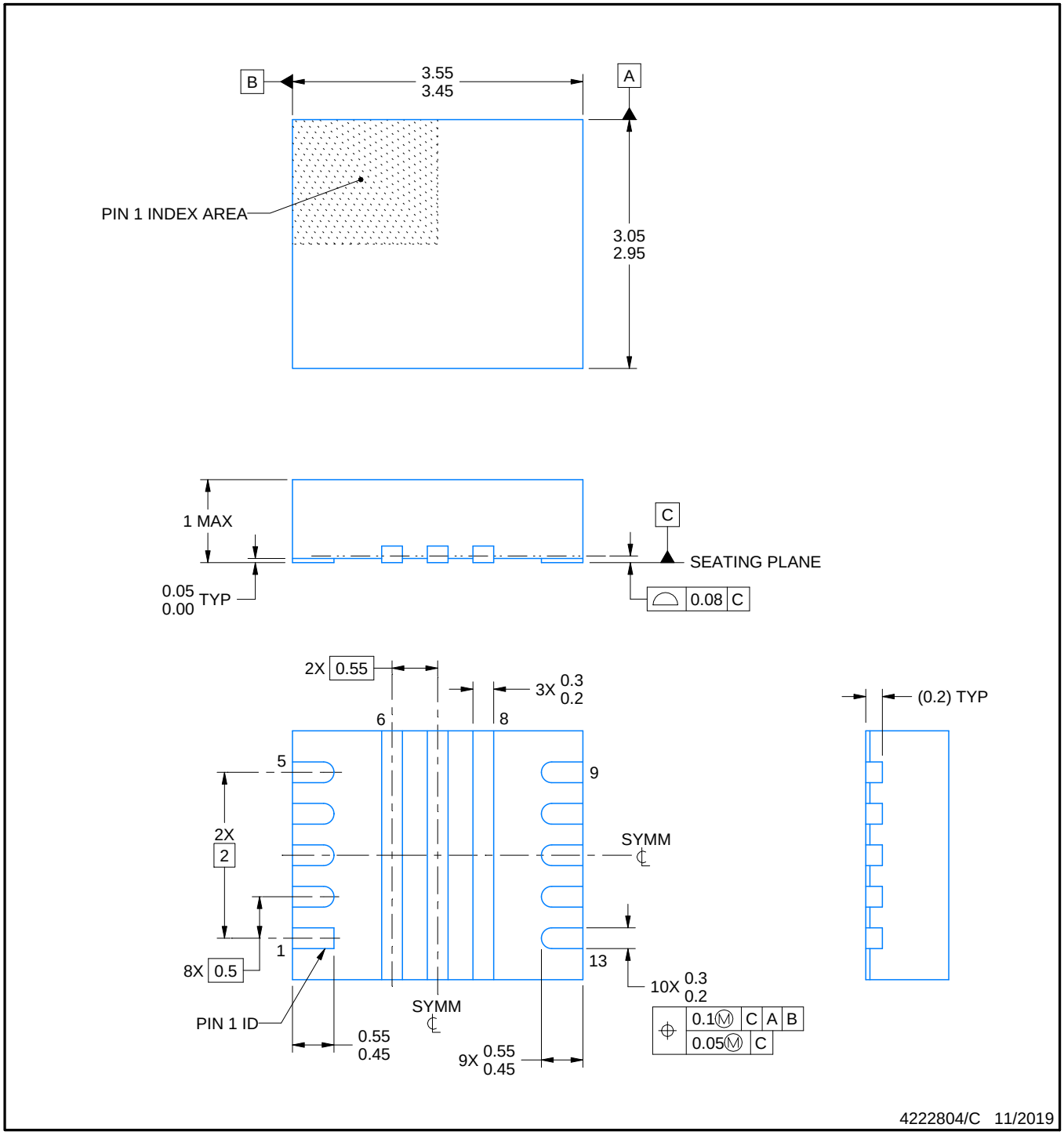
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS611781RNWR	VQFN-HR	RNW	13	3000	330.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2
TPS611781RNWT	VQFN-HR	RNW	13	250	180.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2
TPS61178RNWR	VQFN-HR	RNW	13	3000	330.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2
TPS61178RNWT	VQFN-HR	RNW	13	250	180.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



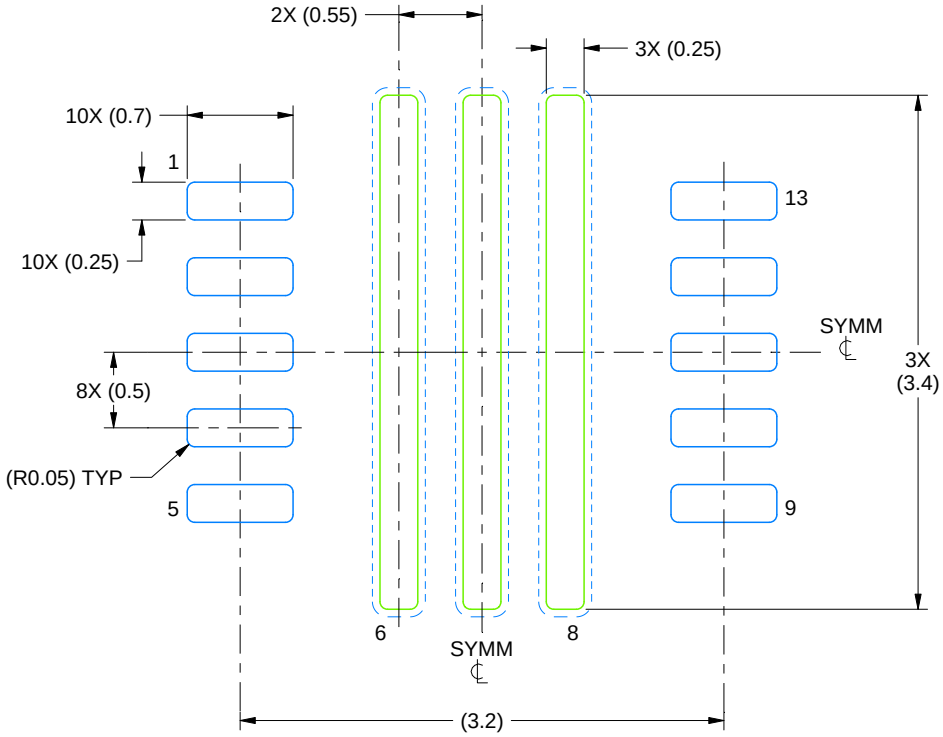
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS611781RNWR	VQFN-HR	RNW	13	3000	367.0	367.0	35.0
TPS611781RNWT	VQFN-HR	RNW	13	250	210.0	185.0	35.0
TPS61178RNWR	VQFN-HR	RNW	13	3000	367.0	367.0	35.0
TPS61178RNWT	VQFN-HR	RNW	13	250	210.0	185.0	35.0

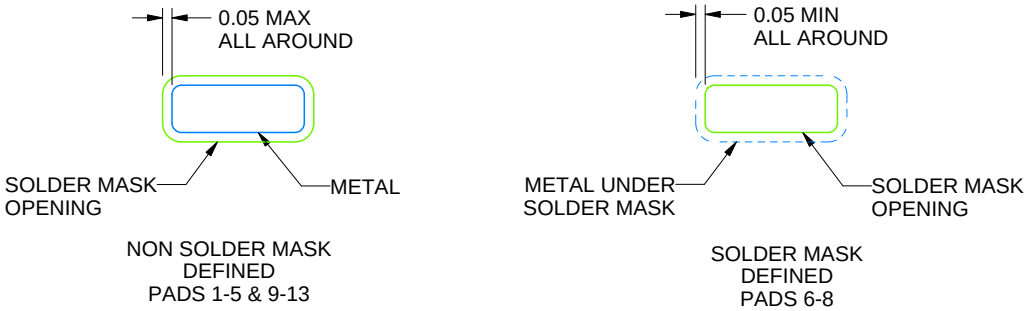


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X

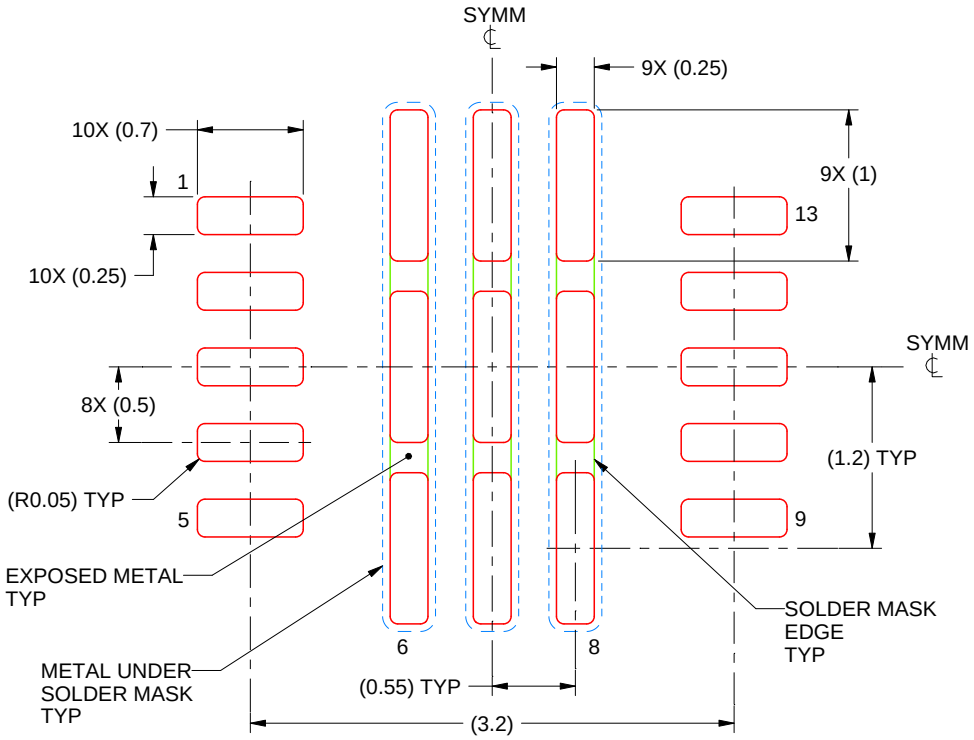


SOLDER MASK DETAILS

4222804/C 11/2019

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PADS 6-8
87% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

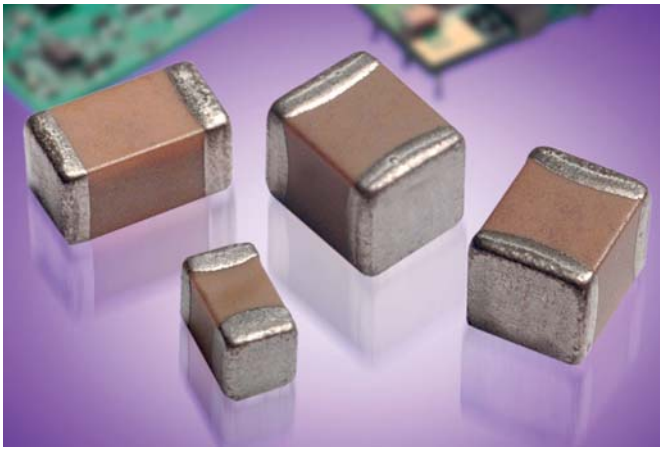
4222804/C 11/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

C0G (NP0) Dielectric

General Specifications



C0G (NP0) is the most popular formulation of the "temperature-compensating," EIA Class I ceramic materials. Modern C0G (NP0) formulations contain neodymium, samarium and other rare earth oxides.

C0G (NP0) ceramics offer one of the most stable capacitor dielectrics available. Capacitance change with temperature is 0 ±30ppm/°C which is less than ±0.3% ΔC from -55°C to +125°C. Capacitance drift or hysteresis for C0G (NP0) ceramics is negligible at less than ±0.05% versus up to ±2% for films. Typical capacitance change with life is less than ±0.1% for C0G (NP0), one-fifth that shown by most other dielectrics. C0G (NP0) formulations show no aging characteristics.

RoHS COMPLIANT

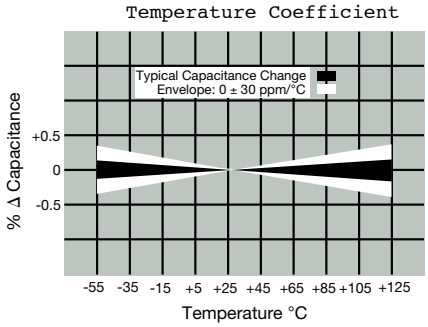
PART NUMBER (see page 2 for complete part number explanation)

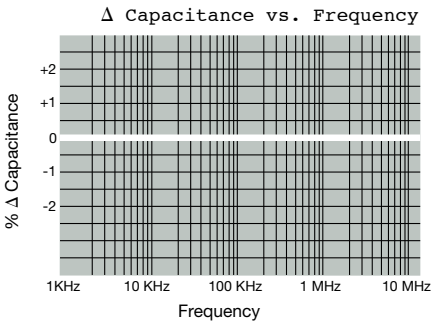
0805	5	A	101	J	A	T	2	A
Size (L" x W")	**Voltage** 6.3V = 6, 10V = Z, 16V = Y, 25V = 3, 50V = 5, 100V = 1, 200V = 2, 500V = 7	**Dielectric** C0G (NP0) = A	**Capacitance Code (In pF)** 2 Sig. Digits + Number of Zeros	**Capacitance Tolerance** B = ±.10 pF (<10pF), C = ±.25 pF (<10pF), D = ±.50 pF (<10pF), F = ±1% (≥ 10 pF), G = ±2% (≥ 10 pF), J = ±5%, K = ±10%	**Failure Rate** A = Not Applicable	**Terminations** T = Plated Ni and Sn	**Packaging** 2 = 7" Reel, 4 = 13" Reel, U = 4mm TR (01005)	**Special Code** A = Std. Product

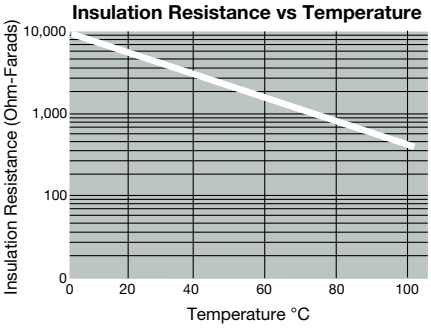
Contact Factory For
1 = Pd/Ag Term
7 = Gold Plated
NOT RoHS COMPLIANT

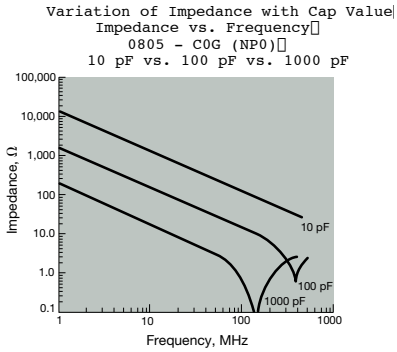
Contact Factory For Multiples

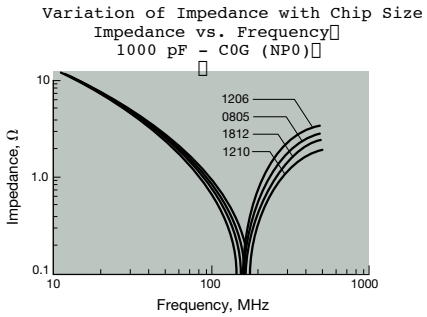
NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.
Contact factory for non-specified capacitance values.

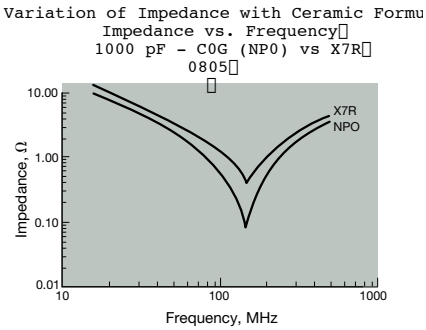






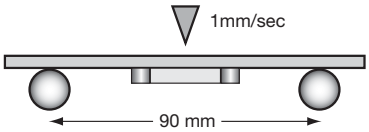






C0G (NP0) Dielectric

Specifications and Test Methods

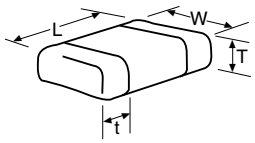
Parameter/Test		NP0 Specification Limits	Measuring Conditions	
Operating Temperature Range		-55ºC to +125ºC	Temperature Cycle Chamber	
Capacitance		Within specified tolerance	Freq.: 1.0 MHz ± 10% for cap ≤ 1000 pF 1.0 kHz ± 10% for cap > 1000 pF Voltage: 1.0Vrms ± .2V	
Q		<30 pF: Q≥ 400+20 x Cap Value ≥30 pF: Q≥ 1000		
Insulation Resistance		100,000MΩ or 1000MΩ - µF, whichever is less	Charge device with rated voltage for 60 ± 5 secs @ room temp/humidity	
Dielectric Strength		No breakdown or visual defects	Charge device with 300% of rated voltage for 1-5 seconds, w/charge and discharge current limited to 50 mA (max) Note: Charge device with 150% of rated voltage for 500V devices.	
Resistance to Flexure Stresses	Appearance	No defects	Deflection: 2mm Test Time: 30 seconds 	
	Capacitance Variation	±5% or ±.5 pF, whichever is greater		
	Q	Meets Initial Values (As Above)		
	Insulation Resistance	≥ Initial Value x 0.3		
Solderability		≥ 95% of each terminal should be covered with fresh solder	Dip device in eutectic solder at 230 ± 5ºC for 5.0 ± 0.5 seconds	
Resistance to Solder Heat	Appearance	No defects, <25% leaching of either end terminal	Dip device in eutectic solder at 260ºC for 60 seconds. Store at room temperature for 24 ± 2 hours before measuring electrical properties.	
	Capacitance Variation	≤ ±2.5% or ±.25 pF, whichever is greater		
	Q	Meets Initial Values (As Above)		
	Insulation Resistance	Meets Initial Values (As Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Thermal Shock	Appearance	No visual defects	Step 1: -55ºC ± 2º	30 ± 3 minutes
	Capacitance Variation	≤ ±2.5% or ±.25 pF, whichever is greater	Step 2: Room Temp	≤ 3 minutes
	Q	Meets Initial Values (As Above)	Step 3: +125ºC ± 2º	30 ± 3 minutes
	Insulation Resistance	Meets Initial Values (As Above)	Step 4: Room Temp	≤ 3 minutes
	Dielectric Strength	Meets Initial Values (As Above)	Repeat for 5 cycles and measure after 24 hours at room temperature	
Load Life	Appearance	No visual defects	Charge device with twice rated voltage in test chamber set at 125ºC ± 2ºC for 1000 hours (+48, -0). Remove from test chamber and stabilize at room temperature for 24 hours before measuring.	
	Capacitance Variation	≤ ±3.0% or ± .3 pF, whichever is greater		
	Q (C=Nominal Cap)	≥ 30 pF: Q≥ 350 ≥10 pF, <30 pF: Q≥ 275 +5C/2 <10 pF: Q≥ 200 +10C		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Load Humidity	Appearance	No visual defects	Store in a test chamber set at 85ºC ± 2ºC/ 85% ± 5% relative humidity for 1000 hours (+48, -0) with rated voltage applied. Remove from chamber and stabilize at room temperature for 24 ± 2 hours before measuring.	
	Capacitance Variation	≤ ±5.0% or ± .5 pF, whichever is greater		
	Q	≥ 30 pF: Q≥ 350 ≥10 pF, <30 pF: Q≥ 275 +5C/2 <10 pF: Q≥ 200 +10C		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		

C0G (NP0) Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

SIZE	0101*	0201		0402			0603					0805					1206					
Soldering	Reflow Only	Reflow Only		Reflow/Wave			Reflow/Wave					Reflow/Wave					Reflow/Wave					
Packaging	All Paper	All Paper		All Paper			All Paper					Paper/Embossed					Paper/Embossed					
(L) Length mm	0.40 ± 0.02	0.60 ± 0.09		1.00 ± 0.10			1.60 ± 0.15					2.01 ± 0.20					3.20 ± 0.20					
(L) Length (in.)	(0.016 ± 0.0008)	(0.024 ± 0.004)		(0.040 ± 0.004)			(0.063 ± 0.006)					(0.079 ± 0.008)					(0.126 ± 0.008)					
(W) Width mm	0.20 ± 0.02	0.30 ± 0.09		0.50 ± 0.10			0.81 ± 0.15					1.25 ± 0.20					1.60 ± 0.20					
(W) Width (in.)	(0.008 ± 0.0008)	(0.011 ± 0.004)		(0.020 ± 0.004)			(0.032 ± 0.006)					(0.049 ± 0.008)					(0.063 ± 0.008)					
(t) Terminal mm	0.10 ± 0.04	0.15 ± 0.05		0.25 ± 0.15			0.35 ± 0.15					0.50 ± 0.25					0.50 ± 0.25					
(t) Terminal (in.)	(0.004 ± 0.0016)	(0.006 ± 0.002)		(0.010 ± 0.006)			(0.014 ± 0.006)					(0.020 ± 0.010)					(0.020 ± 0.010)					
WVDC	16	25	50	16	25	50	16	25	50	100	200	16	25	50	100	200	16	25	50	100	200	500
Cap (pF) 0.5		A		C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
1.0	B	A		C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
1.2	B	A		C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
1.5	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
1.8	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
2.2	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
2.7	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
3.3	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
3.9	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
4.7	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
5.6	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
6.8	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
8.2	B	A	A	C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
10	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
12	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
15	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
18	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
22	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
27	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
33	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
39	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
47	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
56	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
68	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
82	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
100	B	A	A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
120				C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
150				C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
180				C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
220				C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	M
270				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
330				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
390				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
470				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
560				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
680				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	P
820				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	M	
1000				C	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	Q	
1200							G	G	G			J	J	J	J		J	J	J	J	Q	
1500							G	G	G			J	J	J	J		J	J	J	M	Q	
1800							G	G	G			J	J	J	N		J	J	M	M	Q	
2200							G	G	G			N	N	N	N		J	J	M	P	Q	
2700							G	G	G			N	N	N	N		J	J	M	P	Q	
3300							G	G	G			P	P	P	N		J	J	M	P	Q	
3900							G	G	G			P	P	P	N		J	J	M	P		
4700							G	G	G			P	P	P	N		J	J	M	P		
5600												P	P	P			J	J	M	P		
6800												P	P	P			M	M	M	P		
8200												P	P	P			M	M	M	P		
Cap (µF) 0.010												P	P	P			P	P	P	P		
0.012																						
0.015																						
0.018																						
0.022																						
0.027																						
0.033																						
0.039																						
0.047																						
0.068																						
0.082																						
0.1																						
WVDC	16	25	50	16	25	50	16	25	50	100	200	16	25	50	100	200	16	25	50	100	200	500
SIZE	0101*	0201		0402			0603					0805					1206					



Letter	A	B	C	E	G	J	K	M	N	P	Q	X	Y	Z
Max. Thickness	0.33 (0.013)	0.22 (0.009)	0.56 (0.022)	0.71 (0.028)	0.90 (0.035)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.78 (0.070)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)
	PAPER						EMBOSSED							

PAPER and EMBOSSED available for 01005

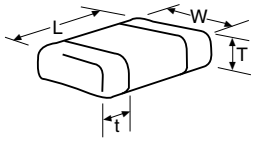
*EIA 01005

C0G (NP0) Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

SIZE		1210					1812					1825			2220			2225		
Soldering		Reflow Only					Reflow Only					Reflow Only			Reflow Only			Reflow Only		
Packaging		Paper/Embossed					All Embossed					All Embossed			All Embossed			All Embossed		
(L) Length	mm (in.)	3.20 ± 0.20 (0.126 ± 0.008)					4.50 ± 0.30 (0.177 ± 0.012)					4.50 ± 0.30 (0.177 ± 0.012)			5.70 ± 0.40 (0.225 ± 0.016)			5.72 ± 0.25 (0.225 ± 0.010)		
(W) Width	mm (in.)	2.50 ± 0.20 (0.098 ± 0.008)					3.20 ± 0.20 (0.126 ± 0.008)					6.40 ± 0.40 (0.252 ± 0.016)			5.00 ± 0.40 (0.197 ± 0.016)			6.35 ± 0.25 (0.250 ± 0.010)		
(t) Terminal	mm (in.)	0.50 ± 0.25 (0.020 ± 0.010)					0.61 ± 0.36 (0.024 ± 0.014)					0.61 ± 0.36 (0.024 ± 0.014)			0.64 ± 0.39 (0.025 ± 0.015)			0.64 ± 0.39 (0.025 ± 0.015)		
	WVDC	25	50	100	200	500	25	50	100	200	500	50	100	200	50	100	200	50	100	200
Cap (pF)	0.5																			
	1.0																			
	1.2																			
	1.5																			
	1.8																			
	2.2																			
	2.7																			
	3.3																			
	3.9																			
	4.7																			
	5.6																			
	6.8																			
	8.2																			
	10					J														
	12					J														
	15					J														
	18					J														
	22					J														
	27					J														
	33					J														
	39					J														
	47					J														
	56					J														
	68					J														
	82					J														
	100					J														
	120					J														
	150					J														
	180					J														
	220					J														
	270					J														
	330					J														
	390					M														
	470					M														
	560	J	J	J	J	M														
	680	J	J	J	K	P														
	820	J	J	J	K	P														
	1000	J	J	P	P	P	K	K	N	N	M	M	M	M				M	M	P
	1200	P	P	P	P	P	K	K	N	N	M	M	M	M				M	M	P
	1500	P	P	P	P	P	K	K	N	N	M	M	M	M				M	M	P
	1800	P	P	P	P	P	K	K	N	N	M	M	M	M				M	M	P
	2200	P	P	P	P	N	K	K	N	N	P	X	X	M				M	M	P
	2700	P	P	P	P		K	K	N	P	Q	X	X	M				M	M	P
	3300	P	P	P	P		K	K	N	P	Q	X	X	X			X	M	M	P
	3900	P	P	P			K	K	N	P	Q	X	X	X			X	M	M	P
	4700	P	P	P			K	K	N	P	Y	X	X	X	X	X	X	M	M	P
	5600	P	P	P			K	K	P	P	Y	X	X	X	X	X	X	M	M	P
	6800	P	P	P			K	K	Q	Q		X	X	X	X	X	X	M	M	P
	8200	P	P				K	M	Q	Q		X	X	X	X	X	X	M	M	P
Cap (µF)	0.010	N	N				K	M	Q	Q		X	X	X	X	X	X	M	M	P
	0.012	N	N				K	M	Q			X	X	X	X	X	X	M	M	P
	0.015						P	P	Q			X	X	X	X	X	X	M	M	Y
	0.018						P	P	Q			X	X	X	X	X	X	M	M	Y
	0.022						P	P	Q			X	X	X	X	X		M	Y	Y
	0.027						Q	Q	X			X	X	Y	X	X		P	Y	Y
	0.033						Q	Q	X			X	X		X	X		X	Y	Y
	0.039						X	X	X			X			Y			X	Y	Y
	0.047						X	X	X			X			Y			X	Z	
	0.068						Z	Z	Y						Z			X	Z	
	0.082						Z	Z	Y						Z			X	Z	
	0.1						Z	Z	Z						Z			Z	Z	
	WVDC	25	50	100	200	500	25	50	100	200	500	50	100	200	50	100	200	50	100	200
	SIZE	1210					1812					1825			2220			2225		

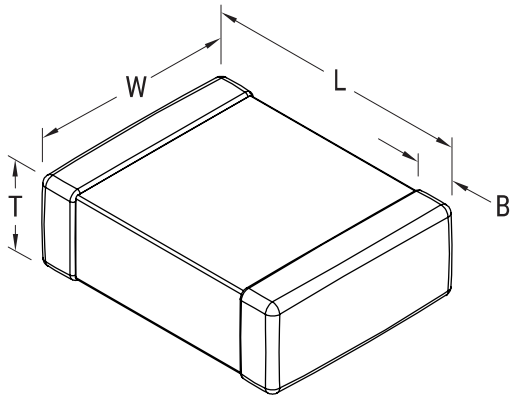


Letter	A	C	E	G	J	K	M	N	P	Q	X	Y	Z
Max. Thickness	0.33 (0.013)	0.56 (0.022)	0.71 (0.028)	0.90 (0.035)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.78 (0.070)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)
	PAPER					EMBOSSED							

KEMET Part Number: C1206C102KGRACTU

(C1206C102KGRAC7800)

SMD Comm X7R HV, Ceramic, 1000 pF, 10%, 2000 VDC, X7R, SMD, MLCC, High Voltage, Temperature Stable, 1206



General Information	
Supplier:	KEMET
Series:	SMD Comm X7R HV
Style:	SMD Chip
Description:	SMD, MLCC, High Voltage, Temperature Stable
Features:	High Voltage
RoHS:	Yes
Termination:	Tin
Marking:	No
Miscellaneous:	Note: Referee time for X7R dielectric for this part number is 1000 hours
Chip Size:	1206

Dimensions	
L	3.2mm +/-0.2mm
W	1.6mm +/-0.2mm
T	1.2mm +/-0.15mm
B	0.5mm +/-0.25mm

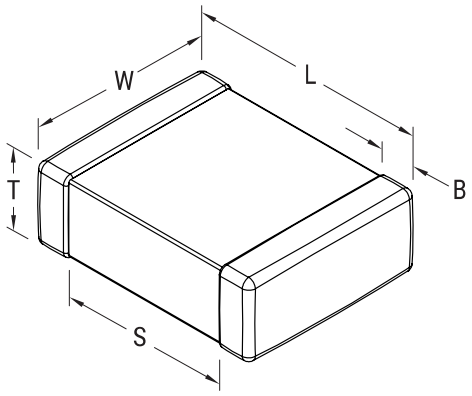
Packaging Specifications	
Packaging:	T&R, 180mm, Plastic Tape
Packaging Quantity:	2500

Specifications	
Capacitance:	1000 pF
Capacitance Tolerance:	10%
Voltage DC:	2000 VDC
Dielectric Withstanding Voltage:	2,400 V
Temperature Range:	-55/+125C
Temperature Coefficient:	X7R
Dissipation Factor:	2.50% 1kHz 25C
Aging Rate:	3% Loss/Decade Hour
Insulation Resistance:	100 GOhms

KEMET Part Number: C0603C122K5RACTU

(C0603C122K5RAC7867)

SMD Comm X7R, Ceramic, 1200 pF, 10%, 50 VDC, X7R, SMD, MLCC, Temperature Stable, Class II, 0603



General Information	
Supplier:	KEMET
Series:	SMD Comm X7R
Style:	SMD Chip
Description:	SMD, MLCC, Temperature Stable, Class II
Features:	Temperature Stable, Class II
RoHS:	Yes
Termination:	Tin
Marking:	No
Miscellaneous:	Note: Referee time for X7R dielectric for this part number is 1000 hours
Chip Size:	0603

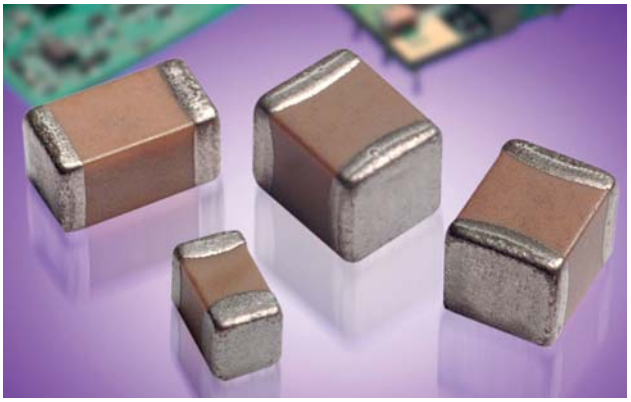
Dimensions	
L	1.6mm +/-0.15mm
W	0.8mm +/-0.15mm
T	0.8mm +/-0.07mm
S	0.7mm MIN
B	0.35mm +/-0.15mm

Packaging Specifications	
Packaging:	T&R, 180mm, Paper Tape
Packaging Quantity:	4000

Specifications	
Capacitance:	1200 pF
Capacitance Tolerance:	10%
Voltage DC:	50 VDC
Dielectric Withstanding Voltage:	125 V
Temperature Range:	-55/+125C
Temperature Coefficient:	X7R
Dissipation Factor:	2.50% 1kHz 25C
Aging Rate:	3% Loss/Decade Hour
Insulation Resistance:	100 GOhms

X7R Dielectric

General Specifications



X7R formulations are called “temperature stable” ceramics and fall into EIA Class II materials. X7R is the most popular of these intermediate dielectric constant materials. Its temperature variation of capacitance is within ±15% from -55°C to +125°C. This capacitance change is non-linear.

Capacitance for X7R varies under the influence of electrical operating conditions such as voltage and frequency.

X7R dielectric chip usage covers the broad spectrum of industrial applications where known changes in capacitance due to applied voltages are acceptable.

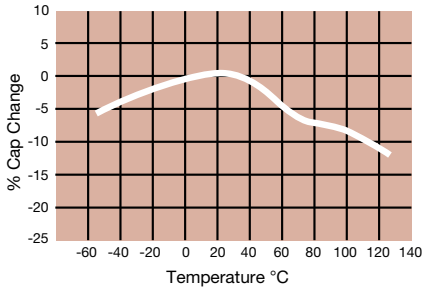
RoHS COMPLIANT

PART NUMBER (see page 2 for complete part number explanation)

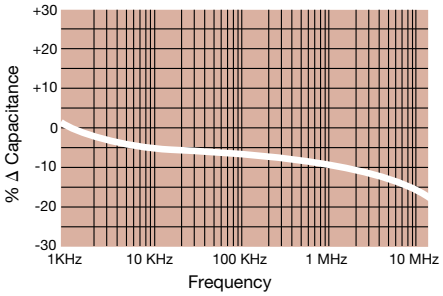
0805	5	C	103	M	A	T	2	A
Size (L" x W")	**Voltage** 4V = 4, 6.3V = 6, 10V = Z, 16V = Y, 25V = 3, 50V = 5, 100V = 1, 200V = 2, 500V = 7	**Dielectric** X7R = C	**Capacitance Code (In pF)** 2 Sig. Digits + Number of Zeros	**Capacitance Tolerance** J = ± 5%*, K = ±10%, M = ± 20%; *≤1µF only, contact factory for additional values	**Failure Rate** A = Not Applicable	**Terminations** T = Plated Ni and Sn, 7 = Gold Plated*, Z = FLEXITERM®**; *Optional termination; **See FLEXITERM® X7R section	**Packaging** 2 = 7" Reel, 4 = 13" Reel; **Contact Factory For Multiples**	**Special Code** A = Std. Product

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.
Contact factory for non-specified capacitance values.

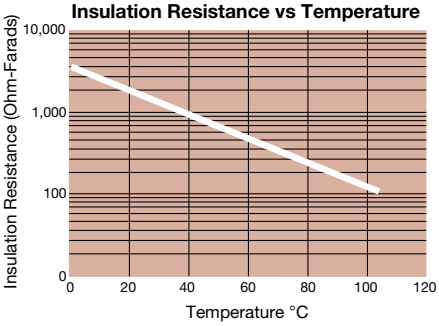
X7R Dielectric Typical Temperature Coefficient



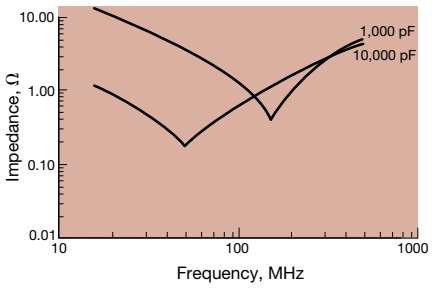
Δ Capacitance vs. Frequency



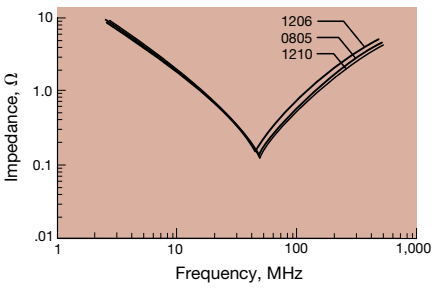
Insulation Resistance vs Temperature



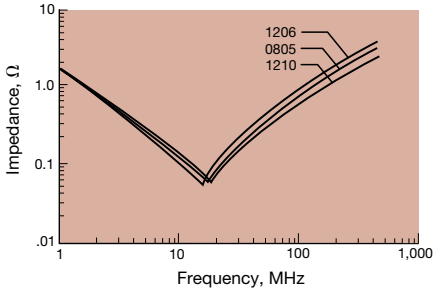
Variation of Impedance with Cap Value Impedance vs. Frequency 1,000 pF vs. 10,000 pF - X7R 0805



Variation of Impedance with Chip Size Impedance vs. Frequency 10,000 pF - X7R

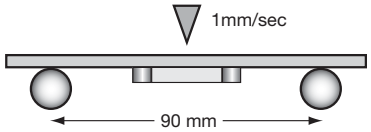


Variation of Impedance with Chip Size Impedance vs. Frequency 100,000 pF - X7R



X7R Dielectric

Specifications and Test Methods

Parameter/Test		X7R Specification Limits	Measuring Conditions	
Operating Temperature Range		-55ºC to +125ºC	Temperature Cycle Chamber	
Capacitance		Within specified tolerance	Freq.: 1.0 kHz ± 10% Voltage: 1.0Vrms ± .2V	
Dissipation Factor		≤ 10% for ≥ 50V DC rating ≤ 12.5% for 25V DC rating ≤ 12.5% for 25V and 16V DC rating ≤ 12.5% for ≤ 10V DC rating		
Insulation Resistance		100,000MΩ or 1000MΩ - µF, whichever is less	Charge device with rated voltage for 120 ± 5 secs @ room temp/humidity	
Dielectric Strength		No breakdown or visual defects	Charge device with 250% of rated voltage for 1-5 seconds, w/charge and discharge current limited to 50 mA (max) Note: Charge device with 150% of rated voltage for 500V devices.	
Resistance to Flexure Stresses	Appearance	No defects	Deflection: 2mm Test Time: 30 seconds 	
	Capacitance Variation	≤ ±12%		
	Dissipation Factor	Meets Initial Values (As Above)		
	Insulation Resistance	≥ Initial Value x 0.3		
Solderability		≥ 95% of each terminal should be covered with fresh solder	Dip device in eutectic solder at 230 ± 5ºC for 5.0 ± 0.5 seconds	
Resistance to Solder Heat	Appearance	No defects, <25% leaching of either end terminal	Dip device in eutectic solder at 260ºC for 60 seconds. Store at room temperature for 24 ± 2 hours before measuring electrical properties.	
	Capacitance Variation	≤ ±7.5%		
	Dissipation Factor	Meets Initial Values (As Above)		
	Insulation Resistance	Meets Initial Values (As Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Thermal Shock	Appearance	No visual defects	Step 1: -55ºC ± 2º	30 ± 3 minutes
	Capacitance Variation	≤ ±7.5%	Step 2: Room Temp	≤ 3 minutes
	Dissipation Factor	Meets Initial Values (As Above)	Step 3: +125ºC ± 2º	30 ± 3 minutes
	Insulation Resistance	Meets Initial Values (As Above)	Step 4: Room Temp	≤ 3 minutes
	Dielectric Strength	Meets Initial Values (As Above)	Repeat for 5 cycles and measure after 24 ± 2 hours at room temperature	
Load Life	Appearance	No visual defects	Charge device with 1.5 rated voltage (≤ 10V) in test chamber set at 125ºC ± 2ºC for 1000 hours (+48, -0) Remove from test chamber and stabilize at room temperature for 24 ± 2 hours before measuring.	
	Capacitance Variation	≤ ±12.5%		
	Dissipation Factor	≤ Initial Value x 2.0 (See Above)		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Load Humidity	Appearance	No visual defects	Store in a test chamber set at 85ºC ± 2ºC/ 85% ± 5% relative humidity for 1000 hours (+48, -0) with rated voltage applied. Remove from chamber and stabilize at room temperature and humidity for 24 ± 2 hours before measuring.	
	Capacitance Variation	≤ ±12.5%		
	Dissipation Factor	≤ Initial Value x 2.0 (See Above)		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		

X7R Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

SIZE	0101*	0201				0402					0603							0805							1206							
Soldering	Reflow Only	Reflow Only				Reflow/Wave					Reflow/Wave							Reflow/Wave							Reflow/Wave							
Packaging	Paper/Embossed	All Paper				All Paper					All Paper							Paper/Embossed							Paper/Embossed							
(L) Length mm (in.)	0.40 ± 0.02 (0.016 ± 0.0008)	0.60 ± 0.09 (0.024 ± 0.004)				1.00 ± 0.10 (0.040 ± 0.004)					1.60 ± 0.15 (0.063 ± 0.006)							2.01 ± 0.20 (0.079 ± 0.008)							3.20 ± 0.20 (0.126 ± 0.008)							
(W) Width mm (in.)	0.20 ± 0.02 (0.008 ± 0.0008)	0.30 ± 0.09 (0.011 ± 0.004)				0.50 ± 0.10 (0.020 ± 0.004)					0.81 ± 0.15 (0.032 ± 0.006)							1.25 ± 0.20 (0.049 ± 0.008)							1.60 ± 0.20 (0.063 ± 0.008)							
(t) Terminal mm (in.)	0.10± 0.04 (0.004 ± 0.0016)	0.15 ± 0.05 (0.006 ± 0.002)				0.25 ± 0.15 (0.010 ± 0.006)					0.35 ± 0.15 (0.014 ± 0.006)							0.50 ± 0.25 (0.020 ± 0.010)							0.50 ± 0.25 (0.020 ± 0.010)							
WVDC	16	10	16	25	50	6.3	10	16	25	50	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	500
Cap (pF) 100 101	B	A	A	A	A			C	C	C					G	G	G															
150 151	B	A	A	A	A			C	C	C					G	G	G															
220 221	B	A	A	A	A			C	C	C					G	G	G															
330 331	B	A	A	A	A			C	C	C					G	G	G		J	J	J	J	J	J								K
470 471	B	A	A	A	A			C	C	C					G	G	G		J	J	J	J	J	J								K
680 681	B	A	A	A				C	C	C					G	G	G		J	J	J	J	J	J								K
1000 102	B	A	A	A			C	C	C	C					G	G	G		J	J	J	J	J	J								K
1500 152	B	A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	J	M
2200 222	B	A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	J	M
3300 332		A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	J	M
4700 472		A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	J	M
6800 682		A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	J	P
Cap (µF) 0.01 103		A	A	A			C	C	C	C				G	G	G			J	J	J	J	J	J		J	J	J	J	J	J	P
0.015 153							C	C	C	C				G	G	G			J	J	J	J	J	J		J	J	J	J	J	M	P
0.022 223							C	C	C	C				G	G	G			J	J	J	J	J	N		J	J	J	J	J	M	X
0.033 333							C	C	C	C				G	G	J			J	J	J	J	N			J	J	J	J	J	M	X
0.047 473							C	C	C	C			G	G	G	J			J	J	J	J	N			J	J	J	J	J	M	
0.068 683							C	C	C	C			G	G	G	J			J	J	J	J	N			J	J	J	J	J	P	
0.1 104							C	C	C	C		G	G	G	G	J			J	J	J	J	N			J	J	J	J	P	P	
0.15 154											G	G	G	G					J	J	J	N	N			J	J	J	J	Q		
0.22 224							C				G	G	J	J	J				J	J	N	N	N			J	J	J	J	Q		
0.33 334											J	J	J	J					N	N	N	N	N			J	J	M	P	Q		
0.47 474						C					J	J	J	J	J				N	N	N	N	N			M	M	M	P	Q		
0.68 684											J	J	J						N	N	N					M	M	Q	Q	Q		
1.0 105						C					J	J	J	J					N	N	N	N				M	M	Q	Q	Q		
2.2 225											J	J	J						P	P	P	P**				Q	Q	Q	Q	Q**		
4.7 475																			P	P	P					Q	Q	Q	Q			
10 106																		P	P							Q	Q	Q				
22 226																									Q	Q						
47 476																																
100 107																																
WVDC	16	10	16	25	50	6.3	10	16	25	50	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	500
SIZE	0101	0201				0402					0603							0805							1206							

Letter	A	B	C	E	G	J	K	M	N	P	Q	X	Y	Z
Max. Thickness	0.33 (0.013)	0.22 (0.009)	0.56 (0.022)	0.71 (0.028)	0.90 (0.035)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.80 (0.071)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)
	PAPER						EMBOSSED							

PAPER and EMBOSSED available for 01005

NOTE: Contact factory for non-specified capacitance values

*EIA 01005

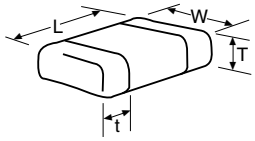
**Contact Factory for Specifications

X7R Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

SIZE	1210							1812						1825			2220					2225		
Soldering	Reflow Only							Reflow Only						Reflow Only			Reflow Only					Reflow Only		
Packaging	Paper/Embossed							All Embossed						All Embossed			All Embossed					All Embossed		
(L) Length mm (in.)	3.30 ± 0.4 (0.130± 0.016)							4.50 ± 0.30 (0.177 ± 0.012)						4.50 ± 0.30 (0.177 ± 0.012)			5.70 ± 0.40 (0.225 ± 0.016)					5.72 ± 0.25 (0.225 ± 0.010)		
(W) Width mm (in.)	2.50 ± 0.20 (0.098 ± 0.008)							3.20 ± 0.20 (0.126 ± 0.008)						6.40 ± 0.40 (0.252 ± 0.016)			5.00 ± 0.40 (0.197 ± 0.016)					6.35 ± 0.25 (0.250 ± 0.010)		
(t) Terminal mm (in.)	0.50 ± 0.25 (0.020 ± 0.010)							0.61 ± 0.36 (0.024 ± 0.014)						0.61 ± 0.36 (0.024 ± 0.014)			0.64 ± 0.39 (0.025 ± 0.015)					0.64 ± 0.39 (0.025 ± 0.015)		
WVDC	10	16	25	50	100	200	500	16	25	50	100	200	500	50	100	200	25	50	100	200	500	50	100	200
Cap (pF) 100 101																								
150 151																								
220 221																								
330 331																								
470 471																								
680 681																								
1000 102																								
1500 152	J	J	J	J	J	J	M																	
2200 222	J	J	J	J	J	J	M																	
3300 332	J	J	J	J	J	J	M																	
4700 472	J	J	J	J	J	J	M																	
6800 682	J	J	J	J	J	J	M																	
Cap (µF) 0.01 103	J	J	J	J	J	J	M		K	K	K	K	K	M	M	M		X	X	X	X	M	P	P
0.015 153	J	J	J	J	J	J	P		K	K	K	K	P	M	M	M		X	X	X	X	M	P	P
0.022 223	J	J	J	J	J	J	Q		K	K	K	K	P	M	M	M		X	X	X	X	M	P	P
0.033 333	J	J	J	J	J	J	Q		K	K	K	K	X	M	M	M		X	X	X	X	M	P	P
0.047 473	J	J	J	J	J	J	Q		K	K	K	K	Z	M	M	M		X	X	X	X	M	P	P
0.068 683	J	J	J	J	J	M	Q		K	K	K	K	Z	M	M	M		X	X	X	X	M	P	P
0.1 104	J	J	J	J	J	M	X		K	K	K	K	Z	M	M	M		X	X	X	X	M	P	P
0.15 154	J	J	J	J	M	Z			K	K	K	P	Z	M	M	M		X	X	X	X	M	P	X
0.22 224	J	J	J	J	P	Z			K	K	K	P	Z	M	M	M		X	X	X	X	M	P	X
0.33 334	J	J	J	J	Q				K	K	M	X		M	M			X	X	X	X	M	P	X
0.47 474	M	M	M	M	Q				K	K	P	X		M	M			X	X	X	X	M	P	X
0.68 684	M	M	P	X	X				M	M	Q			M	P			X	X			M	P	X
1.0 105	N	N	P	X	Z				M	M	X	Z		M	P			X	X			M	P	X
1.5 155	N	N	Z	Z	Z				Z	Z	Z			M				X	X			M	X	Z
2.2 225	X	X	Z	Z	Z				Z	Z	Z							X	X			M	X	Z
3.3 335	X	X	Z	Z	Z				Z	Z	Z							X	Z					
4.7 475	Z	Z	Z	Z					Z	Z								X	Z					
10 106	Z	Z	Z	Z				Z										Z	Z					
22 226	Z	Z	Z														Z							
47 476	Z																							
100 107																								
WVDC	10	16	25	50	100	200	500	16	25	50	100	200	500	50	100	200	25	50	100	200	500	50	100	200
SIZE	1210							1812						1825			2220					2225		



Letter	A	B	C	E	G	J	K	M	N	P	Q	X	Y	Z
Max. Thickness	0.33 (0.013)	0.22 (0.009)	0.56 (0.022)	0.71 (0.028)	0.90 (0.035)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.78 (0.070)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)
	PAPER						EMBOSSED							

NOTE: Contact factory for non-specified capacitance values

TDK

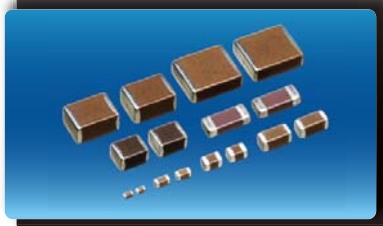
MULTILAYER CERAMIC CHIP CAPACITORS

C Series
Commercial Grade
Mid Voltage (100 to 630V)

Type:

C1005 [EIA CC0402]
C1608 [EIA CC0603]
C2012 [EIA CC0805]
C3216 [EIA CC1206]
C3225 [EIA CC1210]
C4532 [EIA CC1812]
C5750 [EIA CC2220]

Issue date:
Mar 2015



C Series

Mid Voltage (100 to 630V)

Type: C1005 [EIA CC0402], C1608 [EIA CC0603], C2012 [EIA CC0805], C3216 [EIA CC1206], C3225 [EIA CC1210], C4532 [EIA CC1812], C5750 [EIA CC2220]

Lead Free · RoHS COMPLIANT · Ecological

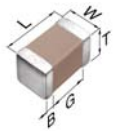
Features

- Voltage rating of 100V to 630V with capacitance range up to 15μF.
- High capacitance has been achieved through precision technologies that enable the use of multiple thinner ceramic dielectric layers.
- Low residual inductance assures superior frequency characteristics.
- Excellent DC Bias properties.
- A lineup with wide-ranging rated voltages that enables selections that are suitable for needs.

Applications

- Snubber in power supply
- Electric flash circuits in digital still camera
- Power factor improvement
- Input-output filter in power supply
- Driver circuit in plasma display
- Noise bypass

Shape & Dimensions



L	Body Length
W	Body Width
T	Body Height
B	Terminal Width
G	Terminal Spacing

Catalog Number Construction

C • 3225 • X7R • 2A • 105 • K • 200 • A • A

Series Name

Dimensions L x W (mm)

Code	Length	Width	Terminal
C1005	1.00 ± 0.05	0.50 ± 0.05	0.10 min.
C1608	1.60 ± 0.10	0.80 ± 0.10	0.20 min.
C2012	2.00 ± 0.20	1.25 ± 0.20	0.20 min.
C3216	3.20 ± 0.20	1.60 ± 0.20	0.20 min.
C3225	3.20 ± 0.40	2.50 ± 0.30	0.20 min.
C4532	4.50 ± 0.40	3.20 ± 0.40	0.20 min.
C5750	5.70 ± 0.40	5.00 ± 0.40	0.20 min.

*Dimension tolerance are typical values

Temperature Characteristics

Temperature Characteristics	Temperature Coefficient or Capacitance Change	Temperature Range
CH	0±60 ppm/°C	-25 to +85°C
C0G	0±30 ppm/°C	-55 to +125°C
JB	±10%	-25 to +85°C
X5R	±15%	-55 to +85°C
X6S	±22%	-55 to +105°C
X7R	±15%	-55 to +125°C
X7S	±22%	-55 to +125°C
X7T	+22/-33%	-55 to +125°C

Rated Voltage (DC)

Code	Voltage (DC)
2A	100V
2E	250V
2V	350V
2W	450V
2J	630V

Nominal Capacitance (pF)

The capacitance is expressed in three digit codes and in units of pico Farads (pF). The first and second digits identify the first and second significant figures of the capacitance. The third digit identifies the multiplier. R designates a decimal point.
Ex. 0R2 = 0.2pF; 103 = 10,000pF; 105 = 1,000,000pF = 100nF

Capacitance Tolerance

Code	Tolerance
C	± 0.25pF
D	± 0.50pF
F	± 1%
G	± 2%
J	± 5%
K	± 10%
M	± 20%

Nominal Thickness

Code	Thickness	Code	Thickness
050	0.50 mm	130	1.30 mm
060	0.60 mm	160	1.60 mm
080	0.80 mm	200	2.00 mm
085	0.85 mm	230	2.30 mm
115	1.15 mm	250	2.50 mm
125	1.25 mm	280	2.80 mm
		320	3.20 mm

Packaging Style

Code	Style
A	178 mm Reel, 4 mm Pitch
B	178 mm Reel, 2 mm Pitch
K	178 mm Reel, 8 mm Pitch

Special Reserved Code

Code	Description
A, B, C	TDK Internal Code

Capacitance Range Chart

EIA CC0603 [C1608]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC), CH (0 ± 60ppm/ºC), JB (±10%), X5R (±15%), X7R (±15%), X7S (±22%)
Rated Voltage: 250V (2E), 100V (2A)

Capacitance (pF)	Code	Tolerance	C0G		CH		JB	X5R	X7R	X7S
			2E (250V)	2A (100V)	2E (250V)	2A (100V)	2A (100V)	2A (100V)	2A (100V)	2A (100V)
1	010	C : ± 0.25pF		■		■				
1.5	1R5	D : ± 0.50pF		■		■				
2	020	F : ± 1%		■		■				
2.2	2R2	G : ± 2%		■		■				
3	030	J : ± 5%		■		■				
3.3	3R3	K : ± 10%		■		■				
4	040	M : ± 20%		■		■				
4.7	4R7			■		■				
5	050			■		■				
6	060			■		■				
6.8	6R8			■		■				
7	070			■		■				
8	080			■		■				
9	090			■		■				
10	100			■		■				
12	120			■		■				
15	150			■		■				
18	180			■		■				
22	220			■		■				
27	270			■		■				
33	330			■		■				
39	390			■		■				
47	470			■		■				
56	560			■		■				
68	680			■		■				
82	820			■		■				
100	101		■	■	■	■				
120	121		■	■	■	■				
150	151		■	■	■	■				
180	181		■	■	■	■				
220	221		■	■	■	■				
270	271		■	■	■	■				
330	331		■	■	■	■				
390	391		■	■	■	■				
470	471		■	■	■	■				
560	561		■	■	■	■				
680	681		■	■	■	■				
820	821		■	■	■	■				
1,000	102		■	■	■	■	■	■	■	
1,200	122		■	■	■	■				
1,500	152		■	■	■	■	■	■	■	
1,800	182		■	■	■	■				
2,200	222		■	■	■	■	■	■	■	
2,700	272			■		■				
3,300	332			■		■	■	■	■	
3,900	392			■		■				
4,700	472			■		■	■	■	■	
5,600	562			■		■				
6,800	682			■		■	■	■	■	
8,200	822			■		■				
10,000	103			■		■	■	■	■	
15,000	153						■	■	■	
22,000	223						■	■	■	
33,000	333									■
47,000	473									■
68,000	683									■
100,000	104									■

Standard Thickness
■ 0.80 mm

• All specifications are subject to change without notice.

Capacitance Range Table

Class 1 (Temperature Compensating)

Temperature Characteristics: C0G (-55 to +125ºC, 0±30 ppm/ºC)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	Catalog Number			
				Rated Voltage Edc: 630V	Rated Voltage Edc: 450V	Rated Voltage Edc: 250V	Rated Voltage Edc: 100V
10 nF	3225	1.25 ± 0.20	± 10%	C3225C0G2J103K125AA			
			± 5%	C3225C0G2J103J125AA			
		1.60 ± 0.20	± 10%			C3225C0G2E103K160AA	
			± 5%			C3225C0G2E103J160AA	
	4532	1.60 ± 0.20	± 10%	C4532C0G2J103K160KA			
			± 5%	C4532C0G2J103J160KA			
15 nF	2012	0.85 ± 0.15	± 10%				C2012C0G2A153K085AC
			± 5%				C2012C0G2A153J085AC
	3216	1.15 ± 0.15	± 10%				C3216C0G2A153K115AA
			± 5%				C3216C0G2A153J115AA
		1.60 ± 0.20	± 10%			C3216C0G2E153K160AA	
			± 5%			C3216C0G2E153J160AA	
		1.60 +0.3/-0.1	± 10%		C3216C0G2W153K160AA		
			± 5%		C3216C0G2W153J160AA		
	3225	1.25 ± 0.20	± 10%				C3225C0G2A153K125AA
			± 5%				C3225C0G2A153J125AA
		1.60 ± 0.20	± 10%	C3225C0G2J153K160AA			
			± 5%	C3225C0G2J153J160AA			
		2.00 ± 0.20	± 10%			C3225C0G2E153K200AA	
			± 5%			C3225C0G2E153J200AA	
	4532	2.50 ± 0.30	± 10%	C4532C0G2J153K250KA			
			± 5%	C4532C0G2J153J250KA			
22 nF	2012	1.25 ± 0.20	± 10%				C2012C0G2A223K125AC
			± 5%				C2012C0G2A223J125AC
	3216	1.60 ± 0.20	± 10%				C3216C0G2A223K160AA
			± 5%				C3216C0G2A223J160AA
		1.60 +0.3/-0.1	± 10%			C3216C0G2E223K160AA	
			± 5%			C3216C0G2E223J160AA	
	3225	1.60 ± 0.20	± 10%			C3225C0G2E223K160AA	C3225C0G2A223K160AA
			± 5%			C3225C0G2E223J160AA	C3225C0G2A223J160AA
		2.30 ± 0.20	± 10%	C3225C0G2J223K230AA	C3225C0G2W223K230AA		
			± 5%	C3225C0G2J223J230AA	C3225C0G2W223J230AA		
	4532	1.60 ± 0.20	± 10%			C4532C0G2E223K160KA	
			± 5%			C4532C0G2E223J160KA	
		3.20 ± 0.30	± 10%	C4532C0G2J223K320KA			
			± 5%	C4532C0G2J223J320KA			
33 nF	2012	1.25 ± 0.20	± 10%				C2012C0G2A333K125AC
			± 5%				C2012C0G2A333J125AC
	3216	1.60 +0.3/-0.1	± 10%				C3216C0G2A333K160AA
			± 5%				C3216C0G2A333J160AA
	3225	2.00 ± 0.20	± 10%				C3225C0G2A333K200AA
			± 5%				C3225C0G2A333J200AA
		2.30 ± 0.20	± 10%			C3225C0G2E333K230AA	
			± 5%			C3225C0G2E333J230AA	
		2.50 ± 0.30	± 10%	C3225C0G2J333K250AA	C3225C0G2W333K250AA		
			± 5%	C3225C0G2J333J250AA	C3225C0G2W333J250AA		
	4532	2.00 ± 0.20	± 10%	C4532C0G2J333K200KA		C4532C0G2E333K200KA	
			± 5%	C4532C0G2J333J200KA		C4532C0G2E333J200KA	
47 nF	3216	1.15 ± 0.15	± 10%				C3216C0G2A473K115AC
			± 5%				C3216C0G2A473J115AC
	3225	2.30 ± 0.20	± 10%				C3225C0G2A473K230AA
			± 5%				C3225C0G2A473J230AA
		2.50 ± 0.30	± 10%			C3225C0G2E473K250AA	
			± 5%			C3225C0G2E473J250AA	
	4532	2.00 ± 0.20	± 10%				C4532C0G2A473K200KA
			± 5%				C4532C0G2A473J200KA
		2.30 ± 0.20	± 10%		C4532C0G2W473K230KA		
			± 5%		C4532C0G2W473J230KA		
		3.20 ± 0.30	± 10%	C4532C0G2J473K320KA		C4532C0G2E473K320KA	
			± 5%	C4532C0G2J473J320KA		C4532C0G2E473J320KA	

• All specifications are subject to change without notice.

Capacitor Data Sheet

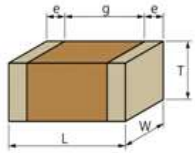
GRM55DR72E105KW01#

"#" indicates a package specification code.

Recommended | In Production | 125℃ | RoHS | REACH

< List of part numbers with package codes >
GRM55DR72E105KW01L , GRM55DR72E105KW01K

Shape



L size	5.7 ±0.4mm
W size	5.0 ±0.4mm
T size	2.0 +0.0/-0.3mm
External terminal width e	0.3mm min.
Distance between external terminals g	3.0mm min.
Size code in inch(mm)	2220 (5750)

Specifications

Capacitance	1.0μF ±10%
Rated voltage	250Vdc
Temperature characteristics (complied standard)	X7R(EIA)
Capacitance change rate	±15.0%
Temperature range of temperature characteristics	-55 to 125℃
Operating temperature range	-55 to 125℃

References

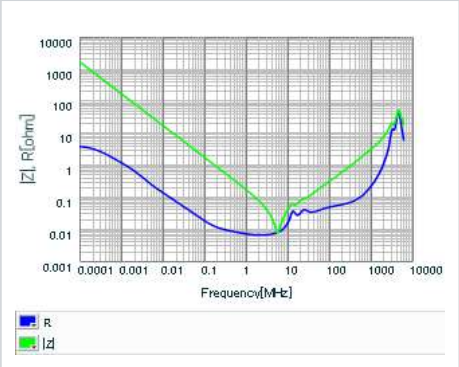
Packaging	Specifications	Minimum quantity
L	φ180mm Embossed taping	1000
K	φ330mm Embossed taping	4000

Mass (typ.)	
1 piece	290mg
φ180mm Reel	347g

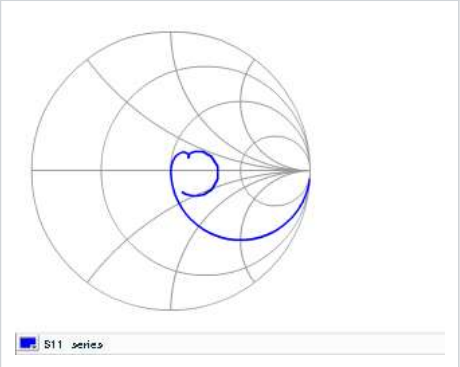
Murata Manufacturing Co., Ltd.
URL : http://www.murata.com/
Last updated: 2015/12/04

Chart of characteristic data (The charts below may show another part number which shares its characteristics.)

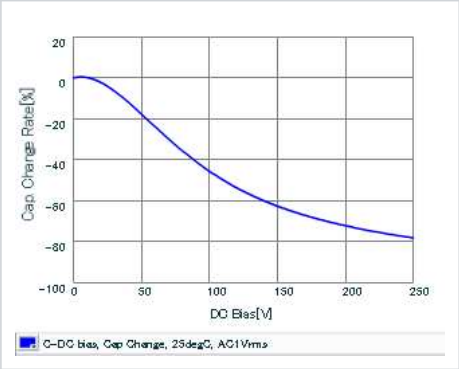
- Frequency characteristics (ESR, Impedance)



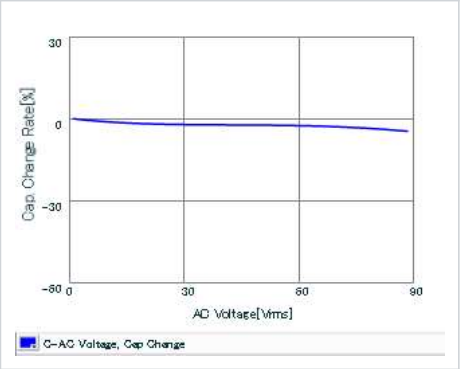
- S parameter (Smith chart S11)



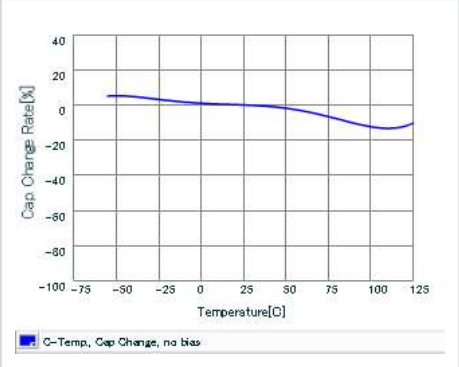
- DC bias characteristics



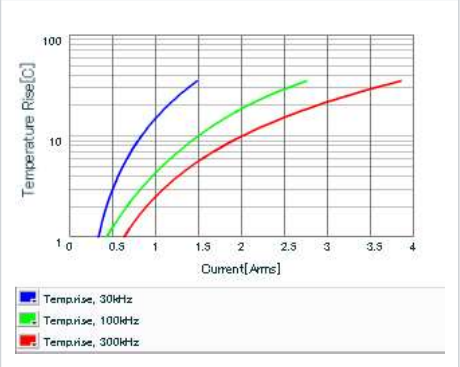
- AC voltage characteristics



- Capacitance - temperature characteristics



- Calorific property by ripple current



Murata Manufacturing Co., Ltd.
Last updated: 2015/12/04

Chip Monolithic Ceramic Capacitor meet AEC-Q200 for Infotainment

GRT21BR61H475KE13_ (0805, X5R, 4.7uF, DC50V)

_: packaging code

Reference Sheet

1.Scope

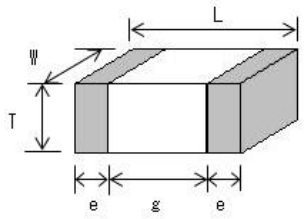
This product specification is applied to Chip Monolithic Ceramic Capacitor used for Car Multimedia, Car Interior, Car Comfort application and General Electronic equipment.
Please contact us when using this product for any other applications than described in the above.
Do not use these products in applications critical to passenger safety and car driving function (e.g. ABS, AIRBAG, etc.).

2.MURATA Part NO. System

(Ex.)

GRT	21	B	R6	1H	475	K	E13	L
	(1)L/W Dimensions	(2)T Dimensions	(3)Temperature Characteristics	(4)Rated Voltage	(5)Nominal Capacitance	(6)Capacitance Tolerance	(7)Murata's Control Code	(8)Packaging Code

3. Type & Dimensions



(Unit:mm)

(1)-1 L	(1)-2 W	(2) T	e	g
2.0±0.15	1.25±0.15	1.25±0.15	0.2 to 0.7	0.7 min.

4.Rated value

(3) Temperature Characteristics (Public STD Code):X5R(EIA)		(4) Rated Voltage	(5) Nominal Capacitance	(6) Capacitance Tolerance	Specifications and Test Methods (Operating Temp. Range)
Temp. coeff or Cap. Change	Temp. Range (Ref.Temp.)				
-15 to 15 %	-55 to 85 °C (25 °C)	DC 50 V	4.7 uF	±10 %	-55 to 85 °C

5.Package

mark	(8) Packaging	Packaging Unit
L	ϕ180mm Reel EMBOSSED W8P4	3000 pcs./Reel
K	ϕ330mm Reel EMBOSSED W8P4	10000 pcs./Reel

Product specifications in this catalog are as of Apr.17,2015,and are subject to change or obsolescence without notice.
Please consult the approval sheet before ordering.
Please read rating and !Cautions first.

TDK

February 2019

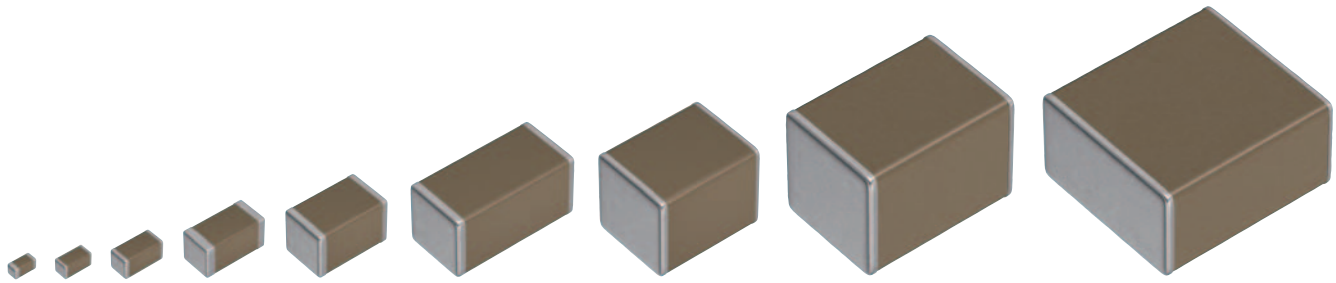
MULTILAYER CERAMIC CHIP CAPACITORS

Commercial grade, general (Up to 75V)

C series

C0402	**[01005 inch]**
C0603	**[0201 inch]**
C1005	**[0402 inch]**
C1608	**[0603 inch]**
C2012	**[0805 inch]**
C3216	**[1206 inch]**
C3225	**[1210 inch]**
C4532	**[1812 inch]**
C5750	**[2220 inch]**

* Dimensions code: JIS[EIA]



C series

General (Up to 75V)

Type: C0402 [01005 inch], C0603 [0201 inch], C1005 [0402 inch], C1608 [0603 inch], C2012 [0805 inch], C3216 [1206 inch], C3225 [1210 inch], C4532 [1812 inch], C5750 [2220 inch]

SERIES OVERVIEW

TDK multilayer ceramic chip capacitor C series is a product for surface mount which multiple sheets of dielectric and conductive material are layered alternately. The monolithic structure ensures superior mechanical strength and reliability.
Also the lower ESR, ESL and better frequency characteristics are offered by the simple structure than other capacitors. The capacitance range is up to 100uF and the line-up has been expanding to the region of the film capacitor or electrolytic capacitor.

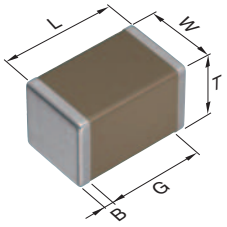
FEATURES

- The superior mechanical strength and reliability due to the monolithic structure.
- Low ESR, ESL and excellent frequency characteristics allow for a circuit design that closely conforms to theoretical values.
- Low self-heating and high ripple resistance due to low ESR.
- No polarity.

APPLICATIONS

- general electronic equipment
- mobile devices
- Servers, PCs, tablets
- Power supply circuit

SHAPE & DIMENSIONS



L	Body length
W	Body width
T	Body height
B	Terminal width
G	Terminal spacing

Dimensions in mm

Type	L	W	T	B	G
C0402	0.40±0.02	0.20±0.02	0.20±0.02	0.07 min.	0.14 min.
C0603	0.60±0.03	0.30±0.03	0.30±0.03	0.10 min.	0.20 min.
C1005	1.00±0.05	0.50±0.05	0.50±0.05	0.10 min.	0.30 min.
C1608	1.60±0.10	0.80±0.10	0.80±0.10	0.20 min.	0.30 min.
C2012	2.00±0.20	1.25±0.20	1.25±0.20	0.20 min.	0.50 min.
C3216	3.20±0.20	1.60±0.20	1.60±0.20	0.20 min.	1.00 min.
C3225	3.20±0.40	2.50±0.30	2.50±0.30	0.20 min.	—
C4532	4.50±0.40	3.20±0.40	3.20±0.40	0.20 min.	—
C5750	5.70±0.40	5.00±0.40	2.80±0.30	0.20 min.	—

∗Dimensional tolerances are typical values.

CATALOG NUMBER CONSTRUCTION

C	3216	X5R	1A	107	M	160	A	C
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)

(1) Series

(2) Dimensions L x W (mm)

Code	EIA	Length	Width	Terminal width
0402	CC01005	0.40	0.20	0.07
0603	CC0201	0.60	0.30	0.10
1005	CC0402	1.00	0.50	0.10
1608	CC0603	1.60	0.80	0.20
2012	CC0805	2.00	1.25	0.20
3216	CC1206	3.20	1.60	0.20
3225	CC1210	3.20	2.50	0.20
4532	CC1812	4.50	3.20	0.20
5750	CC2220	5.70	5.00	0.20

(3) Temperature characteristics

Temperature characteristics	Temperature coefficient or capacitance change	Temperature range
CH	0±60 ppm/°C	–25 to +85°C
C0G	0±30 ppm/°C	–55 to +125°C
JB	±10%	–25 to +85°C
X5R	±15%	–55 to +85°C
X6S	±22%	–55 to +105°C
X7R	±15%	–55 to +125°C
X7S	±22%	–55 to +125°C

(4) Rated voltage (DC)

Code	Voltage (DC)
0G	4V
0J	6.3V
1A	10V
1C	16V
1E	25V
1V	35V
1H	50V
1N	75V

(5) Nominal capacitance (pF)

The capacitance is expressed in three digit codes and in units of pico Farads (pF). The first and second digits identify the first and second significant figures of the capacitance. The third digit identifies the multiplier. R designates a decimal point.

(Example)0R5 = 0.5pF
101 = 100pF
225 = 2,200,000pF = 2.2μF

(6) Capacitance tolerance

Code	Tolerance
B	±0.10pF
C	±0.25pF
D	±0.50pF
F	±1%
G	±2%
J	±5%
K	±10%
M	±20%

(7) Thickness

Code	Thickness
020	0.20 mm
030	0.30 mm
050	0.50 mm
060	0.60 mm
080	0.80 mm
085	0.85 mm
115	1.15 mm
125	1.25 mm
130	1.30 mm
160	1.60 mm
200	2.00 mm
230	2.30 mm
250	2.50 mm
280	2.80 mm
320	3.20 mm

(8) Packaging style

Code	Style
A	178mm reel, 4mm pitch
B	178mm reel, 2mm pitch
K	178mm reel, 8mm pitch

(9) Special reserved code

Code	Description
A, B, C	TDK internal code

Capacitance range chart

C3216 [1206 inch]

Capacitance		C0G	CH	JB					
(pF)	Code	1H (50V)	1H (50V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1A (10V)	0J (6.3V)
3,900	392								
4,700	472								
5,600	562								
6,800	682								
8,200	822								
10,000	103								
15,000	153								
22,000	223								
33,000	333								
47,000	473								
68,000	683								
100,000	104								
1,000,000	105								
1,500,000	155								
2,200,000	225								
3,300,000	335								
4,700,000	475								
6,800,000	685								
10,000,000	106								
15,000,000	156								
22,000,000	226								
33,000,000	336								
47,000,000	476								
68,000,000	686								
100,000,000	107								

Standard thickness

- 0.60 mm
- 0.85 mm
- 1.15 mm
- 1.30 mm
- 1.60 mm

Capacitance		X5R						
(pF)	Code	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1A (10V)	0J (6.3V)	0G (4V)
1,000,000	105							
1,500,000	155							
2,200,000	225							
3,300,000	335							
4,700,000	475							
6,800,000	685							
10,000,000	106							
15,000,000	156							
22,000,000	226							
33,000,000	336							
47,000,000	476							
68,000,000	686							
100,000,000	107							

Standard thickness

- 0.85 mm
- 1.15 mm
- 1.30 mm
- 1.60 mm

Background gray: The product which is not recommended to a new design.

■ Please refer to the capacitance range table at P-24 and after for the details such as product thickness and capacitance tolerance.

Capacitance range table Temperature characteristics: JB (–25 to +85°C, ±10%)

Capacitance	Dimensions	Thickness (mm)	Capacitance tolerance	Catalog number Rated voltage Edc: 10V	Rated voltage Edc: 6.3V	Rated voltage Edc: 4V
680 nF	1608	0.80+0.15, -0.10	±10%	C1608JB1A684K080AC		
			±20%	C1608JB1A684M080AC		
1 µF	1608	0.80+0.15, -0.10	±10%	C1608JB1A105K080AC		
			±20%	C1608JB1A105M080AC		
1.5 µF	1005	0.50±0.05	±10%	C1005JB1A155K050BC	C1005JB0J155K050BB	
			±20%	C1005JB1A155M050BC	C1005JB0J155M050BB	
2.2 µF	1005	0.50±0.05	±10%	C1005JB1A225K050BC	C1005JB0J225K050BC	C1005JB0G225K050BB
			±20%	C1005JB1A225M050BC	C1005JB0J225M050BC	C1005JB0G225M050BB
	2012	0.85±0.15	±10%	C2012JB1A225K085AA		
			±20%	C2012JB1A225M085AA		
3.3 µF	1005	0.50±0.10	±10%	C1005JB1A335K050BC	C1005JB0J335K050BC	C1005JB0G335K050BB
			±20%	C1005JB1A335M050BC	C1005JB0J335M050BC	C1005JB0G335M050BB
	1608	0.80±0.10	±10%	C1608JB1A335K080AB		
			±20%	C1608JB1A335M080AB		
	2012	1.25±0.20	±10%	C2012JB1A335K125AA		
			±20%	C2012JB1A335M125AA		
4.7 µF	1005	0.50+0.15, -0.10	±10%	C1005JB1A475K050BC	C1005JB0J475K050BC	C1005JB0G475K050BB
			±20%	C1005JB1A475M050BC	C1005JB0J475M050BC	C1005JB0G475M050BB
	1608	0.80±0.10	±10%	C1608JB1A475K080AB		
			±20%	C1608JB1A475M080AB		
	2012	0.60±0.15	±10%	C2012JB1A475K060AB		
			±20%	C2012JB1A475M060AB		
		1.25±0.20	±10%	C2012JB1A475K125AA		
			±20%	C2012JB1A475M125AA		
6.8 µF	1608	0.80±0.10	±10%	C1608JB1A685K080AC	C1608JB0J685K080AB	
			±20%	C1608JB1A685M080AC	C1608JB0J685M080AB	
	2012	0.60±0.15	±10%	C2012JB1A685K060AC		
			±20%	C2012JB1A685M060AC		
10 µF	1608	0.80±0.10	±10%	C1608JB1A106K080AC	C1608JB0J106K080AB	
			±20%	C1608JB1A106M080AC	C1608JB0J106M080AB	
	3216	1.60±0.20	±10%	C3216JB1A106K160AA		
			±20%	C3216JB1A106M160AA		
15 µF	1608	0.80+0.20, -0.10	±20%	C1608JB1A156M080AC	C1608JB0J156M080AC	C1608JB0G156M080AA
	2012	0.85±0.15	±20%	C2012JB1A156M085AC	C2012JB0J156M085AB	
		1.25±0.20	±20%	C2012JB1A156M125AB	C2012JB0J156M125AC	
	3225	2.30±0.20	±20%	C3225JB1A156M230AA		
22 µF	1608	0.80+0.20, -0.10	±20%	C1608JB1A226M080AC	C1608JB0J226M080AC	C1608JB0G226M080AA
	2012	0.85±0.15	±20%	C2012JB1A226M085AC	C2012JB0J226M085AB	
		1.25±0.20	±20%	C2012JB1A226M125AB	C2012JB0J226M125AC	
	3225	2.50±0.30	±20%	C3225JB1A226M250AA		
33 µF	2012	1.25±0.20	±20%	C2012JB1A336M125AC	C2012JB0J336M125AC	
	3216	1.30±0.20	±20%		C3216JB0J336M130AC	
		1.60±0.20	±20%	C3216JB1A336M160AB		
47 µF	2012	1.25±0.20	±20%	C2012JB1A476M125AC	C2012JB0J476M125AC	
	3216	1.60±0.20	±20%	C3216JB1A476M160AB	C3216JB0J476M160AC	
68 µF	3216	1.60+0.30, -0.10	±20%	C3216JB1A686M160AC	C3216JB0J686M160AB	
	3225	2.00±0.20	±20%		C3225JB0J686M200AC	
100 µF	3216	1.60+0.30, -0.10	±20%	C3216JB1A107M160AC	C3216JB0J107M160AB	
	3225	2.50±0.30	±20%		C3225JB0J107M250AC	

■ Gray item: The product which is not recommended to a new design.

Capacitor Data Sheet

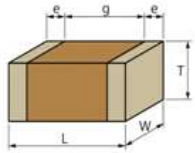
GRM188R60J226MEA0#

"#" indicates a package specification code.

Recommended | Available | General | 85℃ | Reflow OK | Flow OK | RoHS | REACH | Derating

< List of part numbers with package codes >
GRM188R60J226MEA0D , GRM188R60J226MEA0J

Shape



L size	1.6 ±0.2mm
W size	0.8 ±0.2mm
T size	0.8 ±0.2mm
External terminal width e	0.2 to 0.55mm
Distance between external terminals g	0.6mm min.
Size code in inch(mm)	0603 (1608)

Specifications

Capacitance	22μF ±20%
Rated voltage	6.3Vdc
Temperature characteristics (complied standard)	X5R(EIA)
Capacitance change rate	±15.0%
Temperature range of temperature characteristics	-55 to 85℃
Operating temperature range	-55 to 85℃

Notes

Volt. & temp. derating recommended product

References

Packaging	Specifications	Minimum quantity
D	φ180mm Paper taping	4000
J	φ330mm Paper taping	10000

Mass (typ.)	
1 piece	9.1mg
φ180mm Reel	166g

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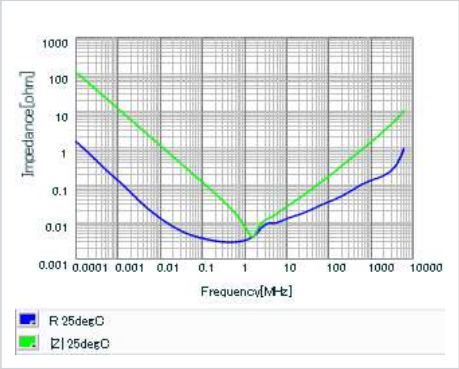
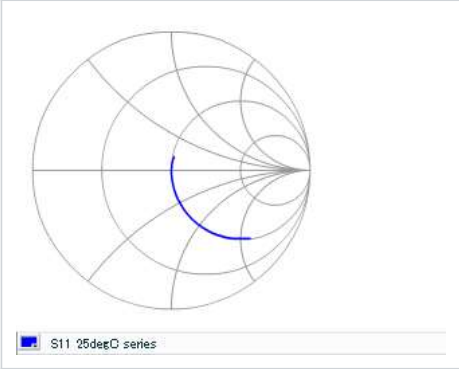
Last updated: 2015/08/17

Chart of characteristic data (The charts below may show another part number which shares its characteristics.)

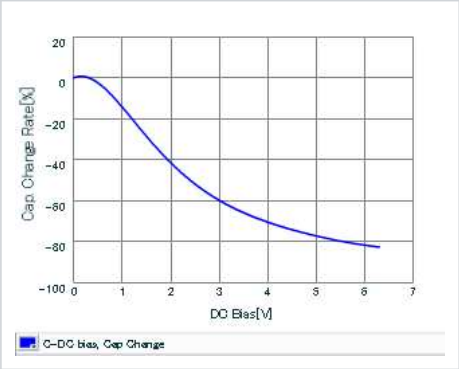
- Frequency characteristics (ESR, Impedance)



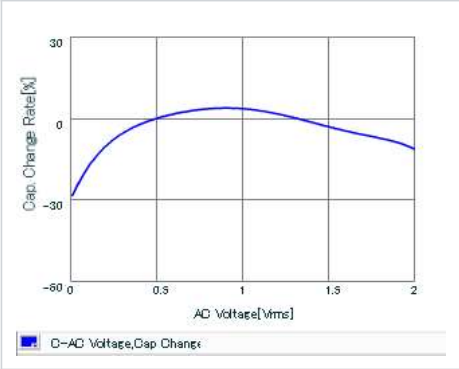
- S parameter (Smith chart S11)



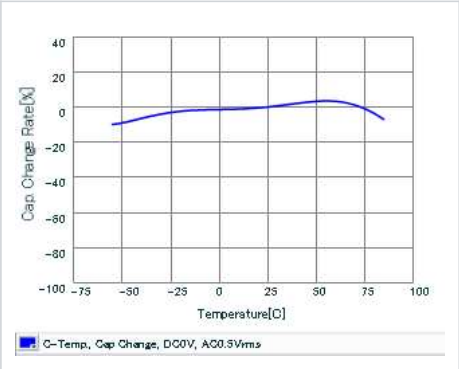
- DC bias characteristics



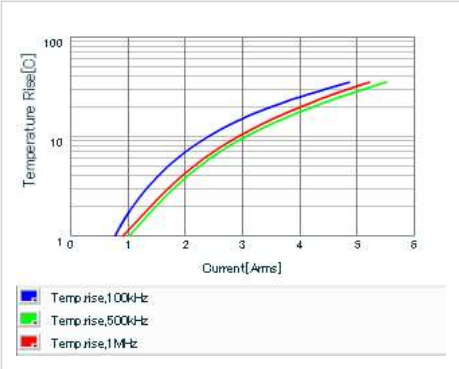
- AC voltage characteristics



- Capacitance - temperature characteristics



- Calorific property by ripple current



Murata Manufacturing Co., Ltd.
Last updated: 2015/08/17

Capacitor Data Sheet

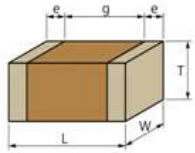
GRM32ER70J476KE20#

"#" indicates a package specification code.

In Production | General | 125℃ | Reflow OK | RoHS | REACH

< List of part numbers with package codes >
GRM32ER70J476KE20L , GRM32ER70J476KE20K

Shape



L size	3.2 ±0.3mm
W size	2.5 ±0.2mm
T size	2.5 ±0.2mm
External terminal width e	0.3mm min.
Distance between external terminals g	1.0mm min.
Size code in inch(mm)	1210 (3225)

Specifications

Capacitance	47µF ±10%
Rated voltage	6.3Vdc
Temperature characteristics (complied standard)	X7R(EIA)
Capacitance change rate	±15.0%
Temperature range of temperature characteristics	-55 to 125℃
Operating temperature range	-55 to 125℃

References

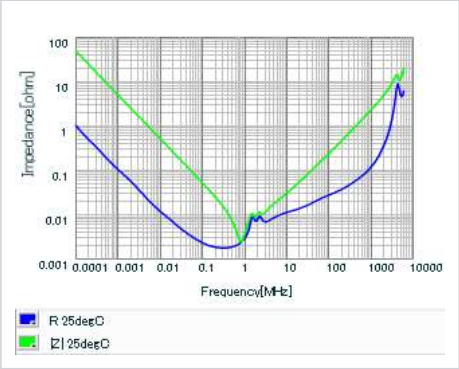
Packaging	Specifications	Minimum quantity
L	φ180mm Embossed taping	1000
K	φ330mm Embossed taping	4000

Mass (typ.)	
1 piece	110mg
φ180mm Reel	168g

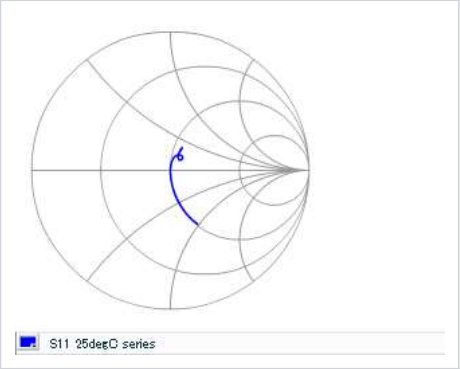
Murata Manufacturing Co., Ltd.
URL : http://www.murata.com/
Last updated: 2015/12/04

Chart of characteristic data (The charts below may show another part number which shares its characteristics.)

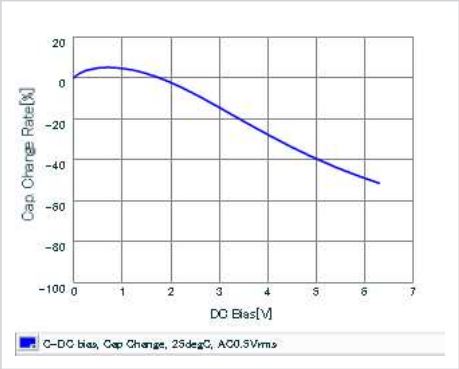
- Frequency characteristics (ESR, Impedance)



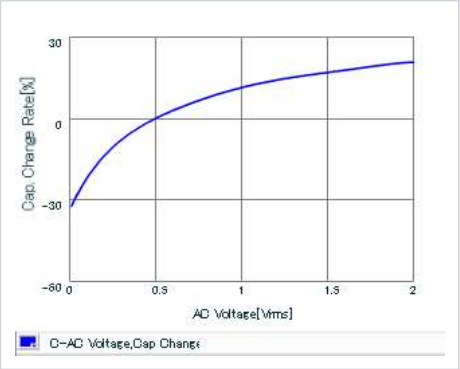
- S parameter (Smith chart S11)



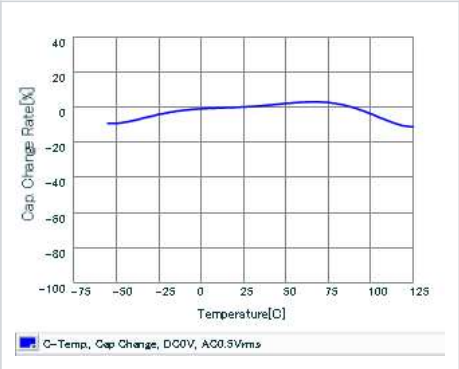
- DC bias characteristics



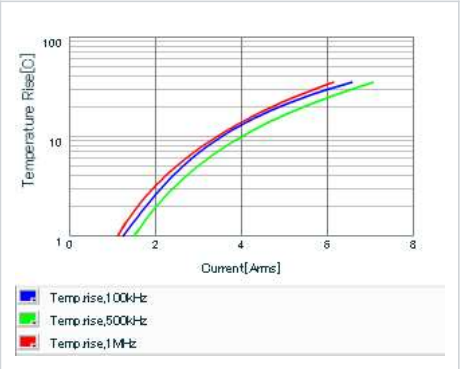
- AC voltage characteristics



- Capacitance - temperature characteristics



- Calorific property by ripple current



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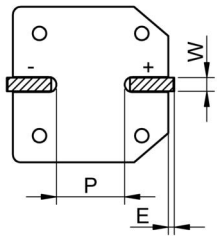
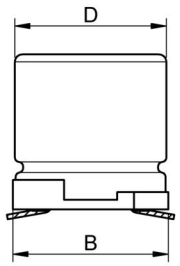
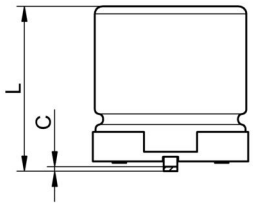
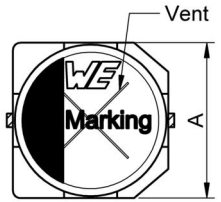
Last updated: 2015/12/04

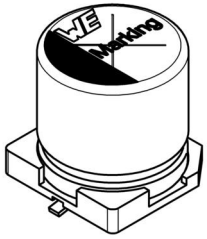
A Dimensions: [mm]





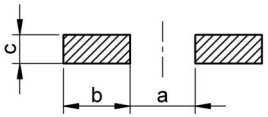




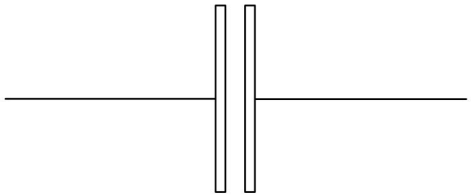


L max.	10.5		
D ±0.5	10.0		
A ±0.2	10.3		
B ±0.2	10.3		
C max.	0.15		
W ±0.1	0.9	a	4.3
E ±0.05	0.35	b	4.4
P ±0.2	4.5	c	1.9

B Recommended hole pattern: [mm]



C Schematic:



D1 Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Capacitance	0.25V; 120Hz	C	560	µF	± 20%
Rated voltage		U_R	6.3	V (DC)	max.
Leakage current	after 2 min.	I_{Leak}	176.4	µA	max.
Dissipation factor	120 Hz	DF	24	%	typ.
Ripple current	100kHz @85°C	I_{ripple}	220	mA	max.

E General information:

Aluminium Electrolytic Capacitors	
Storage Conditions:	35°C, <45% RH
Operating Temperature:	-40 °C bis +85 °C
Load Life:	2000 h @ +85°C / 6.3 V (DC)
Test conditions of Electrical Properties:	20°C, 33% RH; if not specified differently
FIT according to	separate documentation

REV	DATE	BY	CHECKED
1.0	2014-11-11	SSt	PSL

Projection

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WCAP-ASNP Aluminum Electrolytic Capacitors

Order.- No.

865250157010

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 10.0 x 10.5

Component Marking:

Print	Description
1st Line	Capacitance value: 560 µF
2nd Line	Rated Voltage: 6.3
3rd Line	WCAP-ASNP & datecode: YWW

D2 Multiplier for Ripple Current vs. Frequency:

Frequency [Hz]	60 (50)	120	500	1000	≥ 100000
Multiplier	0.80	1.00	1.20	1.30	1.50

REV	DATE	BY	CHECKED
1.0	2014-11-11	SSt	PSL

Projection

Würth Elektronik eiSos GmbH & Co. KG
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Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WCAP-ASNP Aluminum Electrolytic Capacitors

Order.- No.

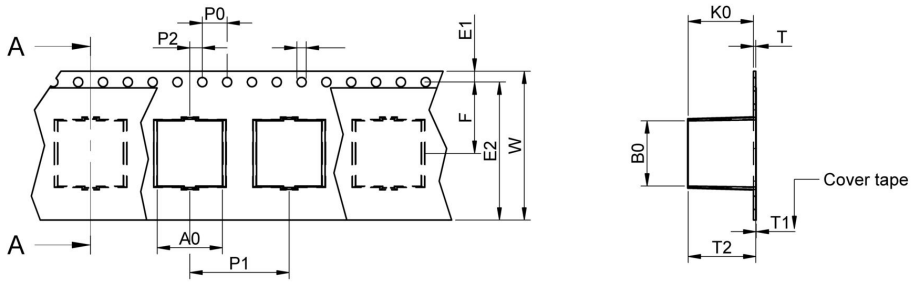
865250157010

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

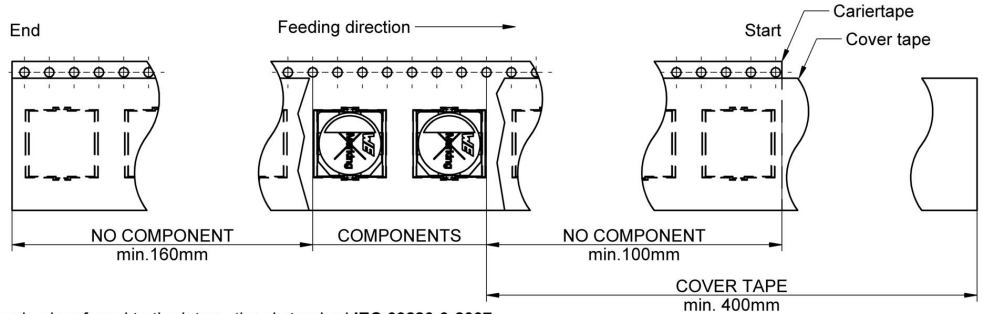
SIZE: A4

Size: 10.0 x 10.5

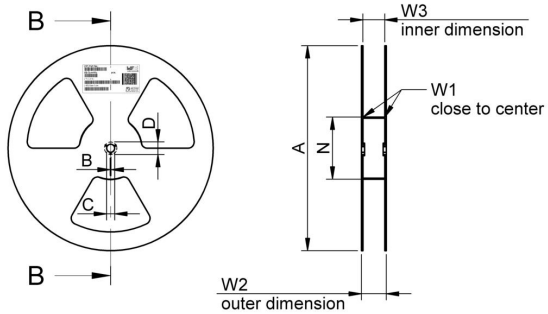
G1 Packaging Specification - Tape and Reel [mm]:



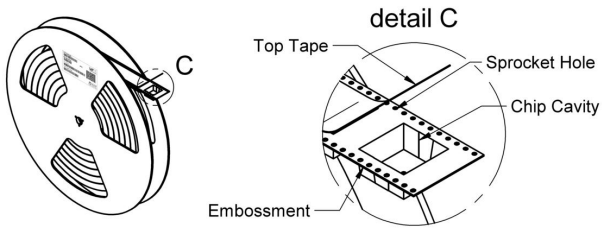
		A0	B0	W	P1	T	T1	T2	K0	D1	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	±0,3	±0,1	max.	min.	ref.	typ.	min.	±0,1	min.	±0,05	±0,1	±0,05		
size	**Ø 4 x 5,5**	4,70	4,70	12,00	8,00	0,40	0,10	5,70	5,20	1,50	1,75	10,25	3,75	4,00	2,00	Polystyrene	2000
	Ø 5 x 5,5	5,70	5,70	12,00	12,00	0,40	0,10	5,70	5,20	1,50	1,75	10,25	3,75	4,00	2,00	Polystyrene	1000
	Ø 5 x 5,8	5,70	5,70	12,00	12,00	0,40	0,10	6,10	5,60	1,50	1,75	10,25	3,75	4,00	2,00	Polystyrene	1000
	Ø 6,3 x 5,5	7,00	7,00	16,00	12,00	0,40	0,10	5,70	5,20	1,50	1,75	14,25	5,75	4,00	2,00	Polystyrene	1000
	Ø 6,3 x 5,8	7,00	7,00	16,00	12,00	0,40	0,10	6,20	5,70	1,50	1,75	14,25	5,75	4,00	2,00	Polystyrene	1000
	Ø 6,3 x 7,7	7,00	7,00	16,00	12,00	0,40	0,10	8,10	7,60	1,50	1,75	14,25	5,75	4,00	2,00	Polystyrene	900
	Ø 8 x 6,5	8,70	8,70	16,00	12,00	0,40	0,10	7,00	6,50	1,50	1,75	14,25	5,75	4,00	2,00	Polystyrene	1000
	Ø 8 x 7,7	8,70	8,70	16,00	12,00	0,40	0,10	8,20	7,70	1,50	1,75	14,25	5,75	4,00	2,00	Polystyrene	700
	Ø 8 x 10,5	8,70	8,70	24,00	16,00	0,40	0,10	11,00	10,50	1,50	1,75	22,25	9,25	4,00	2,00	Polystyrene	500
	Ø 8 x 11,7	8,70	8,70	24,00	16,00	0,40	0,10	13,00	12,50	1,50	1,75	22,25	9,25	4,00	2,00	Polystyrene	400
	Ø 10 x 8,7	10,70	10,70	24,00	16,00	0,40	0,10	11,00	10,50	1,50	1,75	22,25	9,25	4,00	2,00	Polystyrene	500
	Ø 10 x 10,5	10,70	10,70	24,00	16,00	0,40	0,10	11,00	10,50	1,50	1,75	22,25	9,25	4,00	2,00	Polystyrene	500
	Ø 10 x 12,4	10,70	10,70	24,00	16,00	0,40	0,10	12,90	12,40	1,50	1,75	22,25	9,25	4,00	2,00	Polystyrene	400

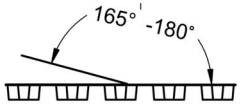


Packaging is referred to the international standard **IEC 60286-3:2007**



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	min.	+ 2	max.	min.	max.
Tape width	**12 mm**	330,00	1,50	13,00	20,20	60,00	12,40	18,40	11,90	15,40
	16 mm	330,00	1,50	13,00	20,20	60,00	16,40	22,40	15,90	19,40





		Pull-of force
Tape width	**12 mm**	0,1 N - 1,3 N
	16 mm	0,1 N - 1,3 N

REV	DATE	BY	CHECKED
1.0	2014-11-11	SSt	PSL

Projection

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WCAP-ASNP Aluminum Electrolytic Capacitors

Order.- No.

865250157010

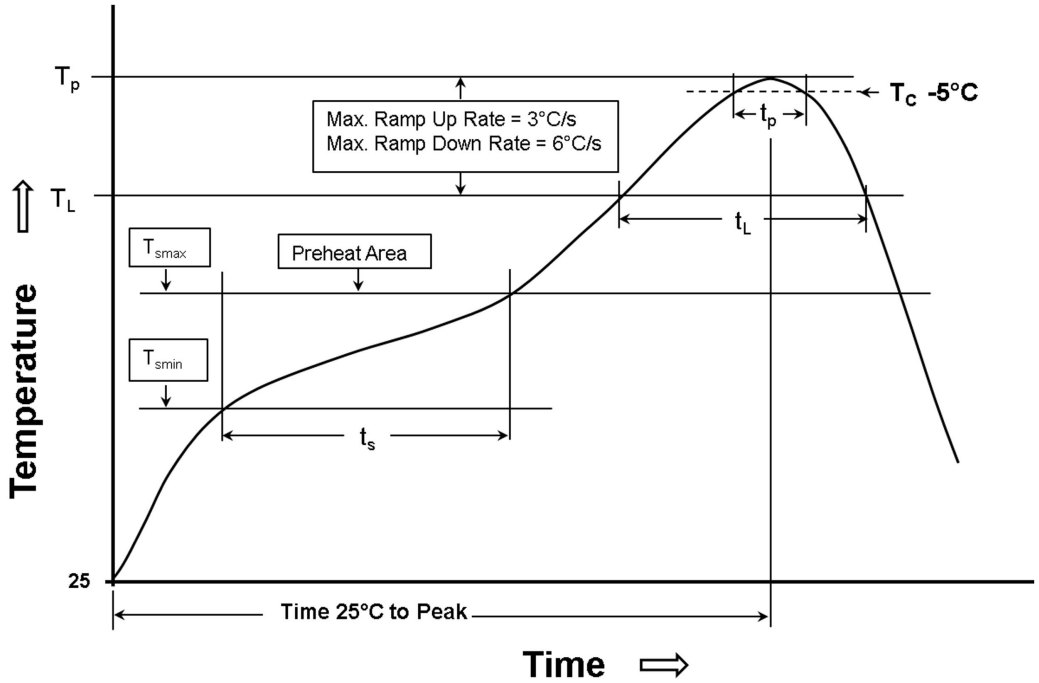
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 10.0 x 10.5

H Soldering Specifications:

H1: Classification Reflow Profile for SMT components:



H2: Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/ second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_p)	See Table H3
Time within 5°C of actual peak temperature (t_p)	20-30 seconds
Ramp-down rate (T_P to T_L)	6°C/ second max.
Time 25°C to peak temperature	8 minutes max.

refer to IPC/JEDEC J-STD-020D

H3: Package Classification Reflow Temperature

	Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
PB-Free Assembly	< 1.6 mm	260°C	260°C	260°C
PB-Free Assembly	1.6 - 2.5 mm	260°C	250°C	245°C
PB-Free Assembly	≥ 2.5 mm	250°C	245°C	245°C

refer to IPC/JEDEC J-STD-020D

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Order.- No.

865250157010

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 10.0 x 10.5

I Cautions and Warnings:

The following conditions apply to all goods within the product series of WCAP-ASNP of Würth Elektronik eiSos GmbH & Co. KG:

1.1 Polarity
An Aluminum Electrolytic Capacitor has a polarity. In operation this polarity needs to be considered and adhered.
Reverse voltage can damage or destroy an Aluminum Electrolytic Capacitor. This can finally lead to a malfunction.
If the polarity in a circuit will be switched or possibly can be reversed, the usage of a non-polar capacitor shall be applied.
The polarity of an Aluminum Electrolytic Capacitor is for SMT V-Chip types marked like following.
On the top of the component the negative terminal is marked with a colored semicircle or bar.

1.2 Overvoltage
Avoid any overvoltage and do not apply a continuous overvoltage. If an overvoltage is applied to the capacitor, the leakage current can increase drastically. The applied working voltage is not allowed to exceed the rated working voltage of the specific capacitor.

1.3 Operating Temperature
The capacitor shall not be operated above the operating temperature, which is stated within this datasheet of the specific capacitor. The achievable lifetime of the capacitor is correlating to the applied temperature. In order to achieve the maximum lifetime, the capacitor should be operated by the lowest possible temperature conditions within the application.

1.4 Ripple Current
The applied ripple current shall not exceed the specified maximum ripple current of the capacitor.
If a higher ripple current is applied as permitted, it can cause excessive heat generation and higher temperature inside the capacitor. This happens due to pole change effects, if ripple current is applied to the capacitor. This can result in damage or lifetime shortage of the capacitor and may cause deterioration.
Electrolytic capacitors are regularly not designed for usage in AC applications and ripple current is applied / based due to parasitic effects on DC signal.
Please see electrical specification within this datasheet for maximum allowed ripple current.

1.5 Charge and Discharge
Frequent and quick charge / discharge cycles may generate heat inside the capacitor. In worst case this can cause a decrease of capacitance, an increase of leakage current or breakdown.
Applications with rapid charge and discharge cycles should be avoided. For assistance with your application please consult our technical support.

1.6 Vent
On most Aluminum Electrolytic Types types, a predetermined breaking point is given on the top of the component, which is the so called vent. The vent is there to assure a possible pressure relief and to avoid that the capacitor can explode due to internal pressure, which can occur by applying reverse voltage or a too high ripple current.
A space of at least 3mm above the vent is recommended, in order to assure the full function of the vent. If less space is present the vent maybe cannot operate correctly / completely.

1.7 Storage Conditions
The storage conditions for a capacitor are recommended to be 5 °C up to 35 °C and less than 75 % rel. humidity.
Do not expose the capacitor to environments with hazardous gas, ozone, ultraviolet rays or any kind of radiation. Avoid any contact of the capacitor with direct sunshine, saltwater, spray of water or types of oil during storage..
If a capacitor is stored for a long time without applying voltage or storage conditions of 35 °C or above and more than 75 % relative humidity, the leakage current may increase.
The leakage current will return to normal level when applying the rated voltage to the capacitor before use. If the capacitor was stored for more than 6 months, it is recommended to apply DC working voltage to the capacitor for 30 minutes through a 1 kΩ protective series resistor.
All products shall be used before the end of the period of 12 months based on the product date code, if not a 100 % solderability cannot be guaranteed. The capacitance tolerance as specified within the datasheet is only valid on the date of delivery.

1.8 Reflow Soldering
The detailed soldering instruction is given at H Soldering Specification in this datasheet.

1.9 Hand Soldering
Take care that the tip of solder iron will only contact pins or leadframe of the capacitor to avoid any possible damage of the capacitor

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DESCRIPTION

WCAP-ASNP Aluminum Electrolytic Capacitors

Order.- No.

865250157010

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 10.0 x 10.5

I Cautions and Warnings (2):

The following conditions apply to all goods within the product series of WCAP-ASNP of Würth Elektronik eiSos GmbH & Co. KG:

1.10 Cleaning

Do not wash the assembled capacitors with the following cleaning agents:

- petroleum system solvents: may cause degeneration of the rubber seal material
- alkali system solvents: may cause corrosion and dissolve of the aluminum case
- halogenated solvents: may cause corrosion and failure of the capacitor
- acetone: component marking may be erased
- xylene: may cause deterioration of the rubber seal material

Verify the following points when washing is are applied to capacitors:

- Please monitor conductivity, ph-value, specific gravity and the water content of cleaning agents. Contamination adversely affects these characteristics.
- Be sure to not expose the capacitors under solvent rich conditions or keep capacitors inside a closed container. In addition, please dry the solvents on the PCB and the capacitor sufficiently with an air knife (temperature should be less than the maximum rated category temperature of the capacitor) for 10 minutes.
- Capacitors can be characteristically and catastrophically damaged by halogen ions, particularly by chlorine ions. The degree of the damage mainly depends upon the characteristics of the electrolyte and rubber seal material. When halogen ions come into contact with the inside of the capacitors, the foil may corrode, when a voltage is applied. This corrosion causes an extremely high leakage current, which results in venting and an open circuit defect.

All other cleaning processes and cleaning agents are not approved by Würth Elektronik eiSos. All cleaning methods need to be tested and validated by the customer.

1.11 Adhesives and Coating Materials

The usage of any adhesive or coating material, which is containing halogenated solvents, is not allowed.

Before applying adhesives or coating materials, make sure that the following points are fulfilled:

- Take care that the surface and capacitor is dry and clean before applying adhesive or coating, to avoid any contamination with flux residues or cleaning solvents.
- Assure that no flux residue or spot is left between the rubber seal material of the capacitor and the PCB.
- Do not fully cover the entire rubber seal surface with adhesive, coating or molding materials. Otherwise the covering of the full rubber seal surface may restrain the natural diffusion of hydrogen gas. Block maximum 80% of the sealed section of a capacitor.
- If the used adhesive, coating or molding material is containing halogen ions in a large amount, the halogen ions can diffuse and creep into the capacitor and can damage the capacitor. Both above explained circumstances can result in serious failures.
- Follow the specified heating and curing instructions given by supplier of the used adhesive or coating material. Avoid excessive pressure or heat on the capacitor by applying coating or adhesive.
- Take care that hardening of adhesive, coating material was correctly done, so that no solvents do remain.
- Be aware, that used solvents within adhesive and coating materials can damage the sleeve of the capacitor and can result in changes of the appearance of the sleeve (color, shine and marking).

1.12 Mechanical Stress on lead wire and terminal

Do not stress the capacitor with the following actions:

- Applying any excessive force to the lead wire or terminal.
- Move or turn the capacitor after soldering to the PCB.
- Bending pins after soldering.
- Carrying the PCB by picking / holding the board via a capacitor.

1.13 Operation and Usage of the Capacitor

In operation and usage take care about the following points.

Do not use the capacitor within the following environmental conditions:

- Environment with high mechanical stress / shocks or vibration (please see this specific datasheet for permitted limits).
- Environment with high amount of damp condensation, water or types of oil.
- Direct sunlight, ozone, any kind of radiation or ultraviolet rays.
- Toxic gases (e.g. ammonium, chlorine and compounds, bromine and compounds, hydrogen sulfide, sulfuric acid).

User should never touch the terminals of the capacitor directly.

Avoid short circuit between terminals with any kind of conductive material (e.g. metal, fluid, acid, alkaline solution).

1.14 Maintenance

For industrial applications it is recommended to perform periodic inspections. Power supplies shall be turned off before inspection to discharge the capacitor. Check the following points in case of an inspection:

- Visual inspection of the capacitor to see, if the vent operated for pressure relief and if any leakage of electrolyte has taken place.
- Measurement of electrical characteristics of the capacitor (according to datasheet, especially leakage current, capacitance and dissipation factor).

In case of deviation or failure according to the specified characteristics, take care to start appropriate actions (e.g. replacement of capacitor).

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DESCRIPTION

WCAP-ASNP Aluminum Electrolytic Capacitors

Order.- No.

865250157010

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE: A4

Size: 10.0 x 10.5

I Cautions and Warnings (3):

The following conditions apply to all goods within the product series of WCAP-ASNP of Würth Elektronik eiSos GmbH & Co. KG:

1.15 Emergency Case

In case of excessive pressure within the capacitor the vent may operate and release this pressure. In case of vent operation gas becomes visible, when the component is in operation. If so, directly turn off the application and disconnect it from the power source. If the application will not be turned off, a possible short circuit of capacitor or a short circuit due to bridging of liquefied gas can possibly damage the circuit and in worst case the application may be dramatically damaged.
Do not stay or position body or face above or in direction of the vent, because in the event of any vent operation, the releasing gas temperature may have over 100 °C.
In case of contact with the electrolyte on skin, wash the skin immediately with soap and water. If the eyes will get in contact with the releasing gas, immediately wash the eyes with water. Whether the gas was inhaled, directly use gargle.

1.16 Disposal

Please contact your local responsible or organization for proper disposal of capacitor.
Also take care to be compliant in order to your local governmental law and restrictions. In case incineration, it should be done with more than 800 °C. Lower temperatures at incineration can result in toxic gases (e.g. chlorine). To avoid any explosion of capacitor, punch holes into the can or crush the capacitor before incineration.

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Order.- No.

865250157010

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE: A4

Size: 10.0 x 10.5

J Important Notes:

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications.

In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Therefore, customer is cautioned to verify that data sheets are current before placing orders. The current data sheets can be downloaded at www.we-online.com.

3. Best Care and Attention
Any product-specific notes, cautions and warnings must be strictly observed. Any disregard will result in the loss of warranty.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered.
The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG.

Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.

REV	DATE	BY	CHECKED
1.0	2014-11-11	SSt	PSL

Projection

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DESCRIPTION

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Order.- No.

865250157010

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE: A4

Size: 10.0 x 10.5

NOT RECOMMENDED FOR NEW DESIGN
USE MB10S or MB10F

HD01 - HD06

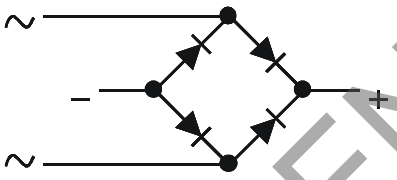
0.8A SURFACE MOUNT GLASS PASSIVATED BRIDGE RECTIFIER

Features and Benefits

- Glass Passivated Die Construction
- Low Forward Voltage Drop
- Surge Overload Rating to 30A Peak
- Ideally Suited for Automated Assembly
- Miniature Package Saves Space on PC Boards
- UL Listed Under Recognized Component Index, File Number E94661
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**

Mechanical Data

- Case: MiniDIP
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Tin. Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Polarity: As Marked on Case
- Marking: Product Type Marking Code, Date Code & Polarity Markings
- Weight: 0.125 grams (Approximate)



Equivalent Circuit

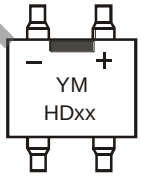
Ordering Information (Note 3)

Part Number*	Packaging	Shipping
HDxx-T	MiniDIP	3k/Tape & Reel, 13-inch

*xx = Device type, e.g. HD02-T or HD04-T, etc.

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



HDxx = Product Type Marking Code (ex: HD04)
YM = Date Code Marking
Y = Last Digit of the Year
M = See Month/Code Table Below

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Single phase, half wave, 60Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

Characteristic	Symbol	HD01	HD02	HD04	HD06	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RMM} V_{RWM} V_{DC}	100	200	400	600	V
RMS Reverse Voltage	V_{RMS}	70	140	280	420	V
Average Forward Rectified Current (Note 4) @T_A = +40°C	I_O	0.8				A
Non-Repetitive Peak Forward Surge Current, 8.3ms Single Half Sine-Wave Superimposed on Rated Load	I_{FSM}	30				A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Typical Thermal Resistance, Junction to Ambient (Note 4)	$R_{\theta JA}$	75	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Instantaneous Voltage Drop @ 0.4A (Per Element)	V_F	1.0	V
Peak Reverse Current at Rated @T_A = +25°C DC Blocking Voltage (Per Element) @T_A = +125°C	I_R	5.0 500	µA
Typical Total Capacitance (Per Element) (Note 5)	C_T	10	pF

Notes: 4. Mounted on PC Board.
5. Measured at 1.0MHz and applied reverse voltage of 4.0V.

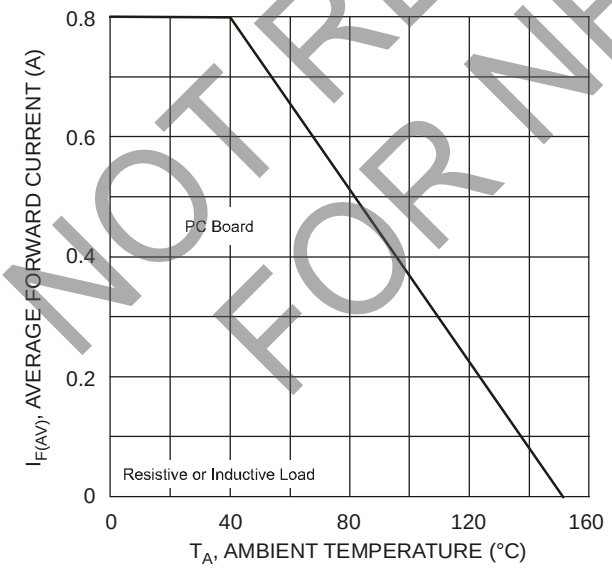


Fig. 1 Output Current Derating Curve

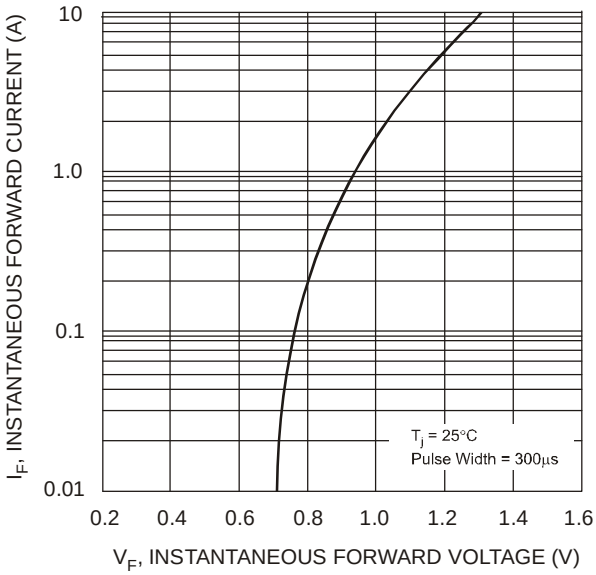


Fig. 2 Typical Forward Characteristics (per element)

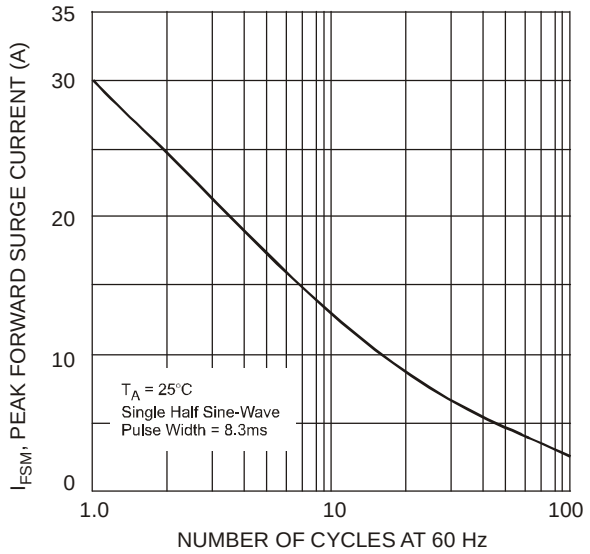


Fig. 3 Maximum Peak Forward Surge Current (per element)

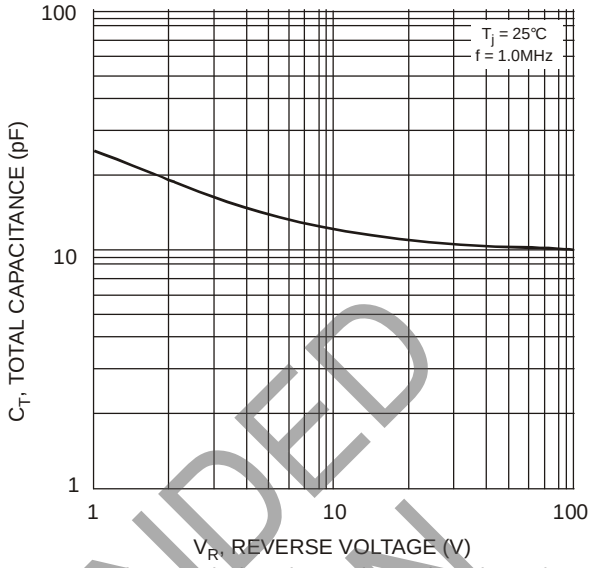


Fig. 4 Typical Total Capacitance (per element)

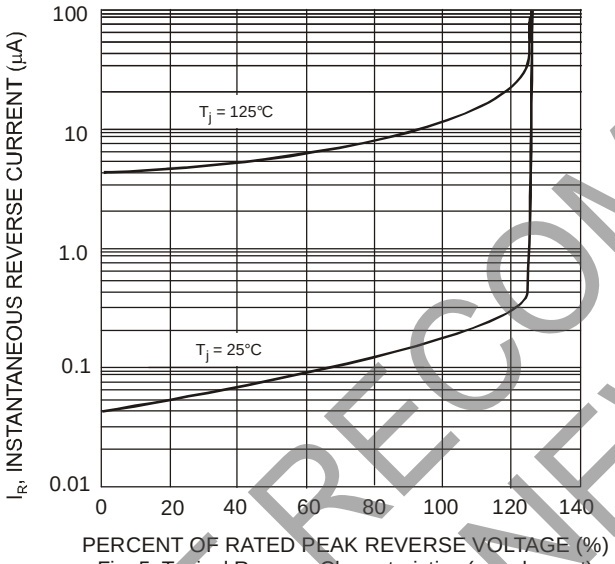
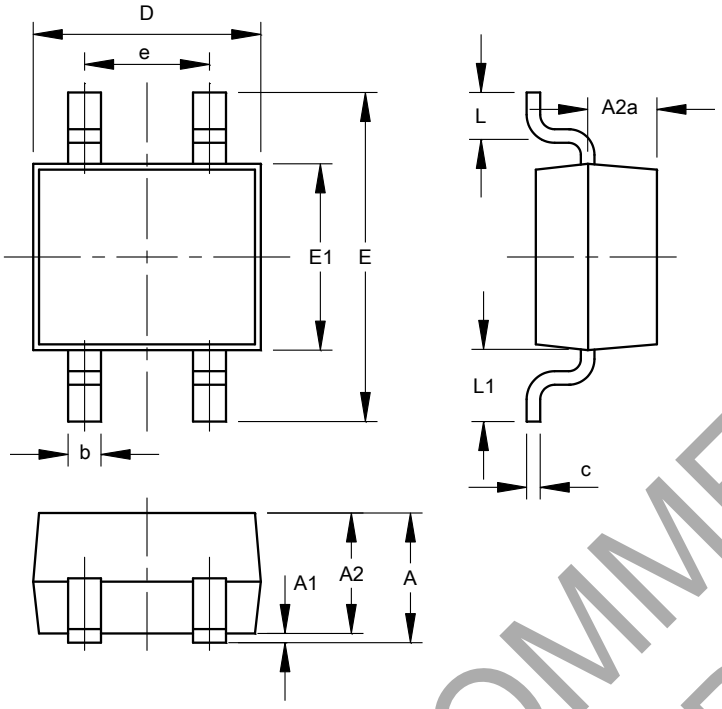


Fig. 5 Typical Reverse Characteristics (per element)

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

MiniDIP

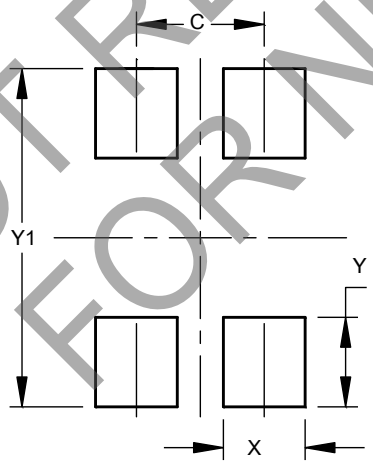


MiniDIP		
Dim	**Min**	**Max**
A	--	3.00
A1	--	0.20
A2	2.30	2.70
A2a	1.20	1.60
b	0.50	0.80
c	0.15	0.35
D	4.50	4.90
E	--	7.00
E1	3.60	4.00
e	2.30	2.70
L	0.70	1.10
L1	1.10	2.12
All Dimensions in mm		

Suggested Pad Layout

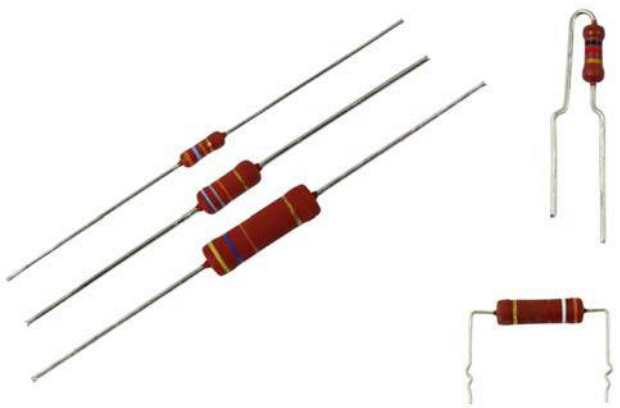
Please see http://www.diodes.com/package-outlines.html for the latest version.

MiniDIP



Dimensions	Value (in mm)
C	2.50
X	1.65
Y	1.80
Y1	6.80

Power Metal Film Leaded Resistors



FEATURES

- High power in small packages (1 W / 0207 size to 3 W / 0617 size)
- Defined fusing characteristics
- Technology: metal film
- Meets active and passive flammability requirements as defined in IEC 60115-1
- AEC-Q200 qualified (PR01 and PR02)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

DESIGN SUPPORT TOOLS

click logo to get started

3D Models Available

DESCRIPTION

A homogeneous film of metal alloy is deposited on a high grade ceramic body. After a helical groove has been cut in the resistive layer, tinned connecting wires of electrolytic copper or copper-clad iron are welded to the end-caps. The resistors are coated with a red, non-flammable lacquer which provides electrical, mechanical and climatic protection. This coating is not resistant to aggressive fluxes and cleaning solvents. The encapsulation is resistant to all cleaning solvents in accordance with IEC 60068-2-45.

APPLICATIONS

- All general purpose power applications
- Automotive electronics
- Lighting ballast

TECHNICAL SPECIFICATIONS

DESCRIPTION	PR01	PR02 Cu-lead	PR02 FeCu-lead	PR03 Cu-lead	PR03 FeCu-lead
DIN size	0207	0411	0411	0617	0617
Resistance range [1]	0.22 Ω to 1 MΩ	0.33 Ω to 1 MΩ	1 Ω to 1 MΩ	0.68 Ω to 1 MΩ	1 Ω to 1 MΩ
Resistance tolerance [2]	± 1 %; ± 5 %	± 1 %; ± 5 %	± 1 %; ± 5 %	± 1 %; ± 5 %	± 1 %; ± 5 %
Temperature coefficient	± 250 ppm/K	± 250 ppm/K	± 250 ppm/K	± 250 ppm/K	± 250 ppm/K
Rated dissipation, P_{70}					
1 Ω ≤ R	1 W	2 W	1.3 W	3 W	2.5 W
R < 1 Ω	0.6 W	1.2 W	-	1.6 W	-
Thermal resistance (R_{th})	135 K/W	75 K/W	115 K/W	60 K/W	75 K/W
Operating voltage, $U_{max.}$ AC/DC	350 V	500 V	500 V	750 V	750 V
E-series	E24, E96 (± 1 %); E24 (± 5 %)				
Basic specification	IEC 60115-1				
Stability after:					
Endurance test (1000 h, P_{70})	ΔR max.: ± (5 % R + 0.1 Ω)				
Damp heat test (56 days)	ΔR max.: ± (3 % R + 0.1 Ω)				
Soldering (10 s, 260 °C)	ΔR max.: ± (1 % R + 0.05 Ω)				

Notes

[1] R value is measured with probe distance of 24 mm ± 1 mm using 4-terminal method

[2] 1 % tolerance is available for R_n-range from 1 Ω upwards

TERMINATION WIRE TYPES					
PRODUCT TYPE	PACKAGING CODE	STYLE	MATERIAL	WIRE DIAMETER	PITCH
PR01	A1, A5, R5	Axial	Cu	0.58 mm	n/a
	N4	Radial	Cu	0.58 mm	4.8 mm
	L1	Radial	Cu	0.58 mm	17.8 mm
	L1	Radial	FeCu	0.58 mm	17.8 mm
	K1	Radial	FeCu	0.58 mm	12.5 mm
PR02	A1, R5	Axial	Cu	0.78 mm	n/a
	A1	Axial	FeCu	0.58 mm	n/a
	N3, R2	Radial	Cu	0.78 mm	4.8 mm
	L1	Radial	Cu	0.78 mm	17.8 mm
	L1	Radial	FeCu	0.58 mm	17.8 mm
	B1	Radial	FeCu	0.78 mm	15 mm
PR03	AC	Axial	Cu	0.78 mm	n/a
	AC	Axial	FeCu	0.58 mm	n/a
	DC	Radial	Cu	0.78 mm	25.4 mm
	DC	Radial	FeCu	0.58 mm	25.4 mm
	PC	Radial	FeCu	0.78 mm	20 mm

APPLICATION INFORMATION

The power dissipation on the resistor generates a temperature rise against the local ambient, depending on the heat flow support of the printed-circuit board (thermal resistance). The rated dissipation applies only if the permitted film temperature is not exceeded. Furthermore, a high level of ambient temperature or of power dissipation may raise the temperature of the solder joint, hence special solder alloys or board materials may be required to maintain the reliability of the assembly.

These resistors do not feature a limited lifetime when operated within the permissible limits. However, resistance value drift increasing over operating time may result in exceeding a limit acceptable to the specific application, thereby establishing a functional lifetime. The designer may estimate the performance of the particular resistor application or set certain load and temperature limits in order to maintain a desired stability.

OPERATION MODE		POWER
		P_{70}
Rated dissipation	**PR01**	1 W
	PR02	2 W
	PR03	3 W
Applied maximum film temperature, $\vartheta_{F\ max.}$		250 °C
Max. resistance change at rated dissipation for resistance range:	**PR01**	0.22 Ω to 1 MΩ
	PR02	0.33 Ω to 1 MΩ
	PR03	0.68 Ω to 1 MΩ
$\lvert\Delta R/R\rvert_{max.}$ (at P_{70}) after:	1000 h	5.0 % R + 0.1 Ω

PART NUMBER AND PRODUCT DESCRIPTION

Part Number: PR02000201001JA100

P	R	0	2	0	0	0	2	0	1	0	0	1	J	A	1	0	0

TYPE/SIZE	VARIANT	WIRE TYPES	TCR/MATERIAL	RESISTANCE	TOLERANCE	PACKAGING	SPECIAL
PR0100 **PR0200** **PR0300**	**0** = neutral **Z** = value overflow (special)	**1** = Cu 0.58 (PR01) **2** = Cu 0.78 (PR02, PR03) **3** = FeCu 0.58 (PR01, PR02, PR03) **4** = FeCu 0.78 (PR02, PR03)	**0** = standard	3 digit value 1 digit multiplier **Multiplier** **7** = $*10^{-3}$ **8** = $*10^{-2}$ **9** = $*10^{-1}$ **0** = $*10^{0}$ **1** = $*10^{1}$ **2** = $*10^{2}$ **3** = $*10^{3}$ **4** = $*10^{4}$	**F** = ± 1 % **J** = ± 5 %	**N4** **R2** **N3** **L1** **A5** **DC** **A1** **K1** **AC** **B1** **R5** **PC**	**00** = standard

Product Description: PR02 5 % A1 1K0

PR02	5 %	A1	1K0
TYPE	TOLERANCE	PACKAGING	RESISTANCE VALUE
PR01 **PR02** **PR03**	**1 %** **5 %**	**N4** **R2** **N3** **L1** **A5** **DC** **A1** **K1** **AC** **B1** **R5** **PC**	**1K0** = 1 kΩ **4K75** = 4.75 kΩ

Note

- The products can be ordered using either the PRODUCT DESCRIPTION or the PART NUMBER

PACKAGING

PRODUCT TYPE	CODE	QUANTITY	DESCRIPTION	PITCH	TAPE WIDTH	DIMENSION
PR01	A5	5000	Ammo pack acc. to IEC 60286-1	5 mm	52 mm	75 mm x 114 mm x 260 mm
	A1	1000	Ammo pack acc. to IEC 60286-1	5 mm	52 mm	78 mm x 31 mm x 260 mm
	N4	4000	Ammo pack acc. to IEC 60286-2	-	-	45 mm x 262 mm x 330 mm
	L1	1000	Loose in bulk	-	-	105 mm x 70 mm x 205 mm
	K1	1000	Loose in bulk	-	-	105 mm x 70 mm x 205 mm
	R5	5000	Reel pack acc. to IEC 60286-1	5 mm	52 mm	93 mm x 300 mm x 298 mm
PR02	A1	1000	Ammo pack acc. to IEC 60286-1	5 mm	52 mm	72 mm x 60 mm x 258 mm
	N3	3000	Ammo pack acc. to IEC 60286-2	-	-	45 mm x 262 mm x 330 mm
	L1	1000	Loose in bulk	-	-	105 mm x 70 mm x 205 mm
	B1	1000	Loose in bulk	-	-	105 mm x 70 mm x 205 mm
	R5	5000	Reel pack acc. to IEC 60286-1	5 mm	52 mm	100 mm x 375 mm x 375 mm
	R2	2000	Reel pack acc. to IEC 60286-2	-	-	90 mm x 375 mm x 375 mm
PR03	AC	500	Ammo pack acc. to IEC 60286-1	10 mm	63 mm	83 mm x 58 mm x 256 mm
	DC	500	Loose in bulk	-	-	105 mm x 70 mm x 205 mm
	PC	500	Loose in bulk	-	-	105 mm x 70 mm x 205 mm

DESCRIPTION

Production is strictly controlled and follows an extensive set of instructions established for reproducibility. A homogeneous film of metal alloy is deposited on a high grade ceramic body and conditioned to achieve the desired temperature coefficient. Plated steel termination caps are firmly pressed on the metalized rods. Mostly, a special laser is used to achieve the target value by smoothly cutting a helical groove in the resistive layer without damaging the ceramics. Connecting wires of electrolytic copper plated with 100 % pure tin are welded to the termination caps. The resistor elements are covered by a red, non-flammable lacquer protective coating designed for electrical, mechanical, and climatic protection. Four or five color code rings designate the resistance value and tolerance in accordance with **IEC 60062**.

The result of the determined production is verified by an extensive testing procedure performed on 100 % of the individual resistors. Only accepted products are stuck directly on the adhesive tapes in accordance with **IEC 60286-1** or for the radial versions in accordance to **IEC 60286-2**.

MATERIALS

Vishay acknowledges the following systems for the regulation of hazardous substances:

- IEC 62474, Material Declaration for Products of and for the Electrotechnical Industry, with the list of declarable substances given therein [(1)]
- The Global Automotive Declarable Substance List (GADSL) [(2)]
- The REACH regulation (1907/2006/EC) and the related list of substances with very high concern (SVHC) [(3)] for its supply chain

The products do not contain any of the banned substances as per IEC 62474, GADSL, or the SVHC list, see www.vishay.com/how/leadfree.

Hence the products fully comply with the following directives:

- 2000/53/EC End-of-Life Vehicle Directive (ELV) and Annex II (ELV II)
- 2011/65/EU Restriction of the Use of Hazardous Substances Directive (RoHS) with amendment 2015/863/EU
- 2012/19/EU Waste Electrical and Electronic Equipment Directive (WEEE)

Vishay pursues the elimination of conflict minerals from its supply chain, see the Conflict Minerals Policy at www.vishay.com/doc?49037.

ASSEMBLY

The resistors are suitable for processing on automatic insertion equipment and cutting and bending machines. Excellent solderability is proven, even after extended storage. They are suitable for automatic soldering using wave or dipping.

The resistors are completely lead (Pb)-free, the pure tin plating provides compatibility with lead (Pb)-free and lead-containing soldering processes. The immunity of the plating against tin whisker growth, in compliance with IEC 60068-2-82, has been proven under extensive testing.

The encapsulant is resistant to cleaning solvent specified in IEC 60115-1. The suitability of conformal coatings, if applied, shall be qualified by appropriate means to ensure the long-term stability of the whole system.

RELATED PRODUCTS

For a correlated range of Metal Film Resistors see the datasheet:

“High Ohmic / High Voltage Metal Film Leaded Resistors”, www.vishay.com/doc?30260

For product that offers high power dissipation and metal oxide film technology see the datasheet:

“High Power Metal Oxide Leaded Resistors”, www.vishay.com/doc?20128

Notes

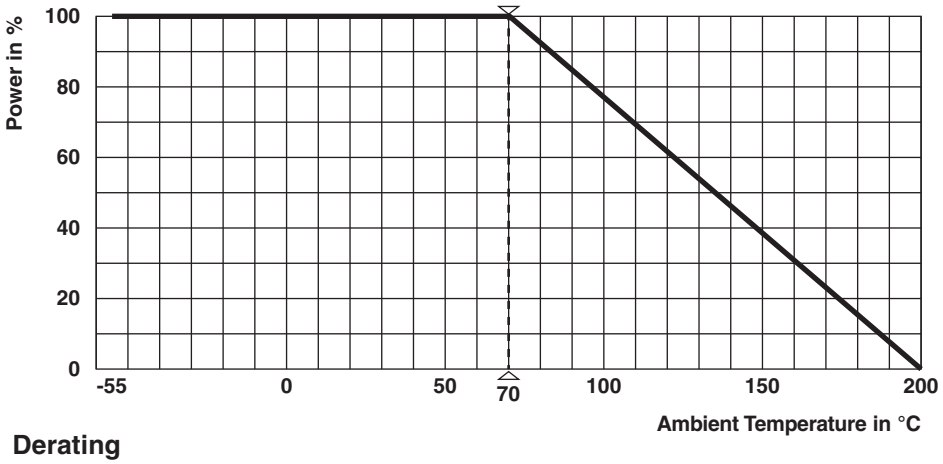
(1) The IEC 62474 list of declarable substances is maintained in a dedicated database, which is available at http://std.iec.ch/iec62474

(2) The Global Automotive Declarable Substance List (GADSL) is maintained by the American Chemistry Council, and available at www.gadsl.org

(3) The SVHC list is maintained by the European Chemical Agency (ECHA) and available at http://echa.europa.eu/candidate-list-table

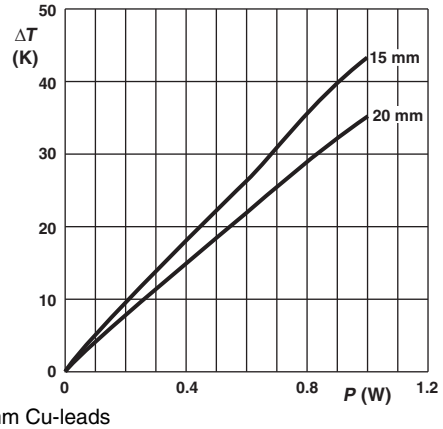
FUNCTIONAL PERFORMANCE

The power that the resistor can dissipate depends on the operating temperature.



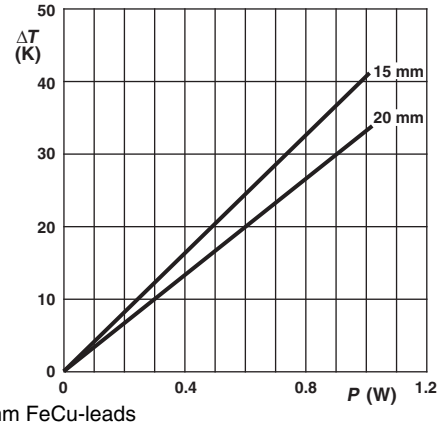
Derating

Maximum dissipation ($P_{max.}$) in percentage of rated power as a function of the ambient temperature (T_{amb})



Ø 0.58 mm Cu-leads
Minimum distance from resistor body to PCB = 1 mm

PR01 Temperature rise (Δ*T*) at the lead end (soldering point) as a function of dissipated power at various lead lengths after mounting.



Ø 0.58 mm FeCu-leads
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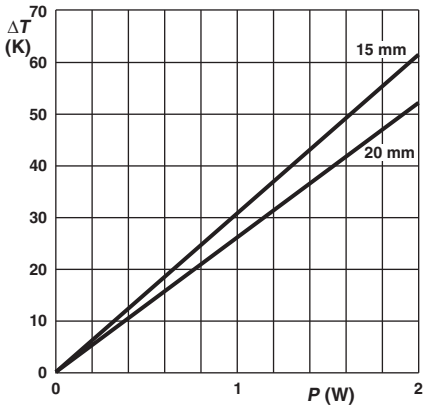
PR01 Temperature rise (Δ*T*) at the lead end (soldering point) as a function of dissipated power at various lead lengths after mounting.



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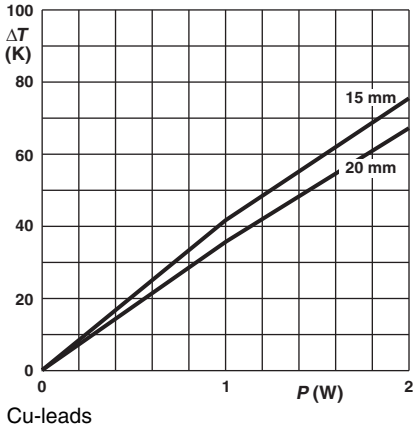
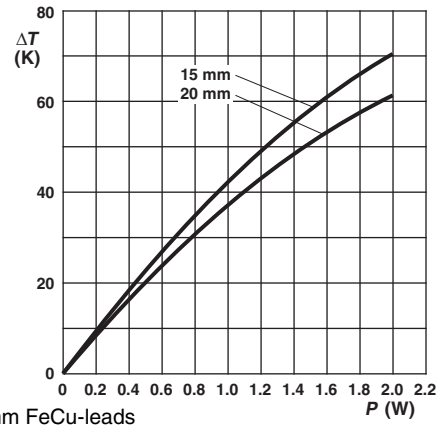


Ø 0.78 mm Cu-leads
Minimum distance from resistor body to PCB = 1 mm

PR02 Temperature rise (Δ*T*) at the lead end (soldering point) as a function of dissipated power at various lead lengths after mounting.



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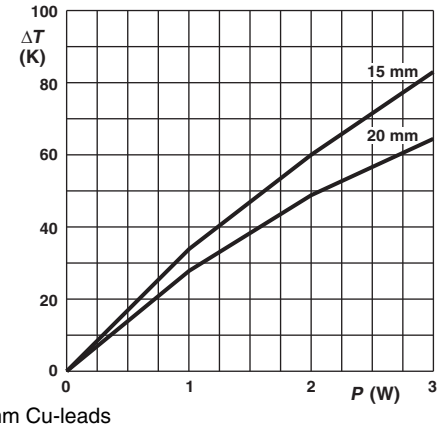

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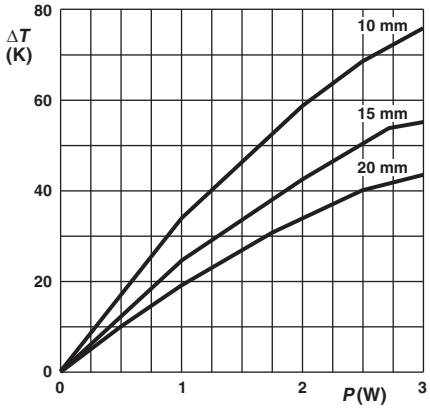
PR03 Temperature rise (Δ*T*) at the lead end (soldering point) as a function of dissipated power at various lead lengths after mounting.



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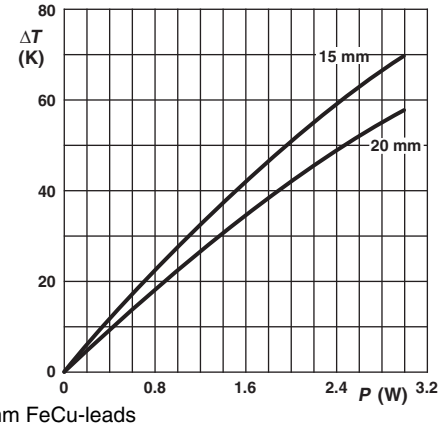

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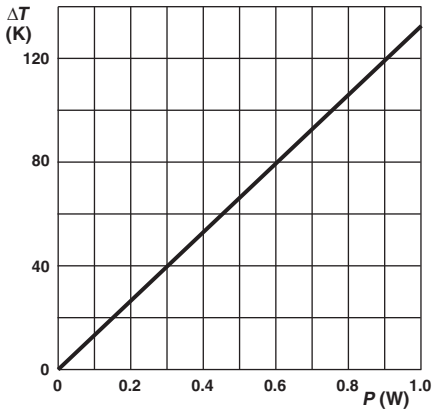
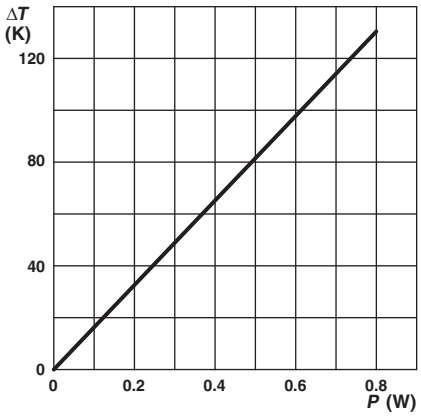


Ø 0.58 mm Cu-leads

PR01 Hot-spot temperature rise (Δ*T*) as a function of dissipated power.



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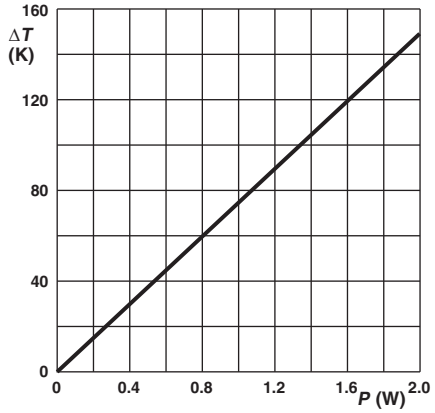
PR01 Hot-spot temperature rise (Δ*T*) as a function of dissipated power.



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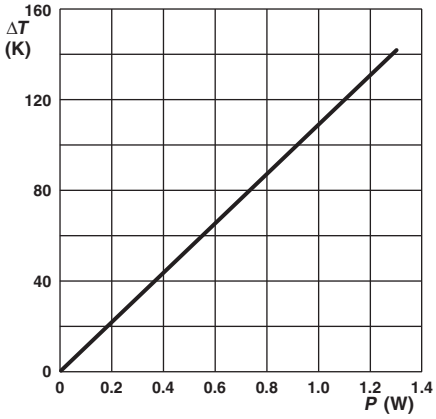
PR02 Hot-spot temperature rise (Δ*T*) as a function of dissipated power.



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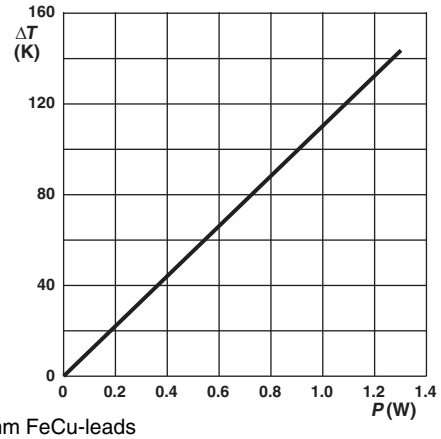
PR02 Hot-spot temperature rise (Δ*T*) as a function of dissipated power.



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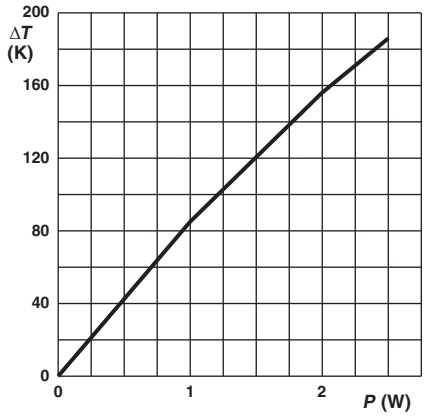

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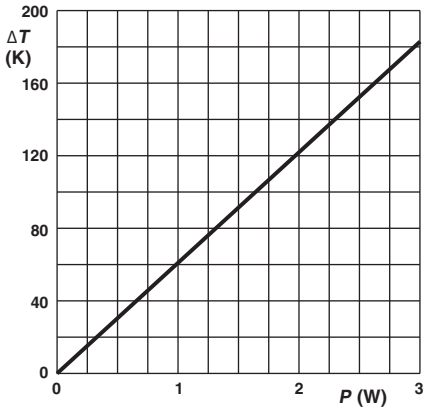
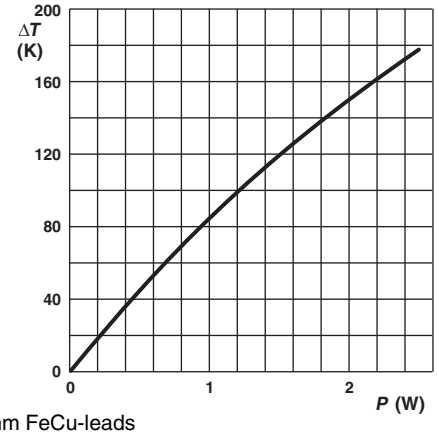
PR03 Hot-spot temperature rise (Δ*T*) as a function of dissipated power.



Ø 0.78 mm Cu-leads

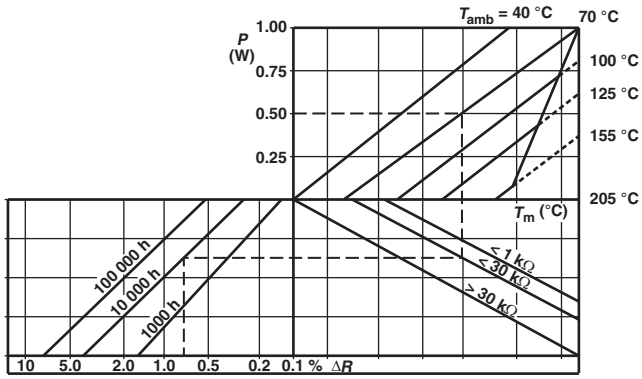
PR03 Hot-spot temperature rise (Δ*T*) as a function of dissipated power.



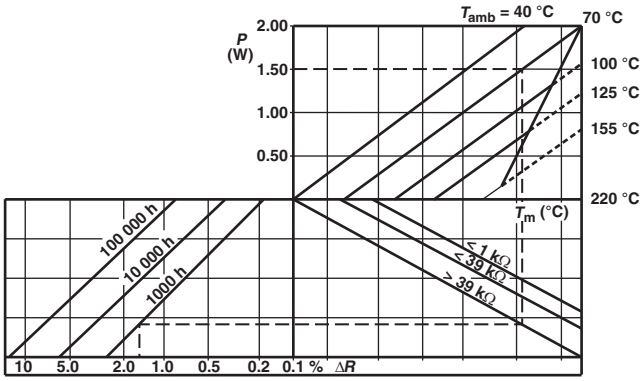
Ø 0.78 mm FeCu-leads

PR03 Hot-spot temperature rise (Δ*T*) as a function of dissipated power.

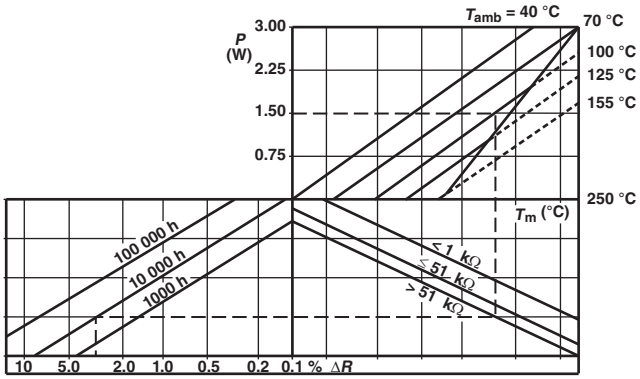
The maximum permissible hot-spot temperature is 205 °C for PR01, 220 °C for PR02 and 250 °C for PR03.



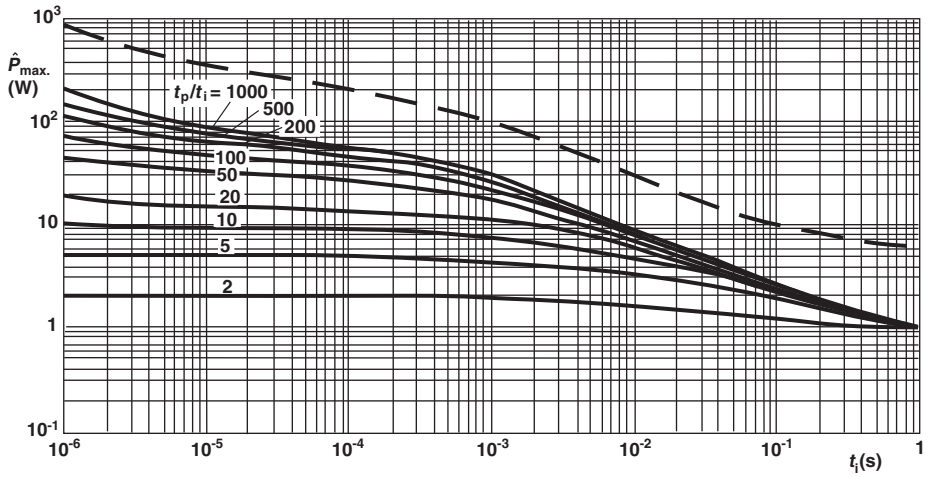
PR01 Drift nomogram



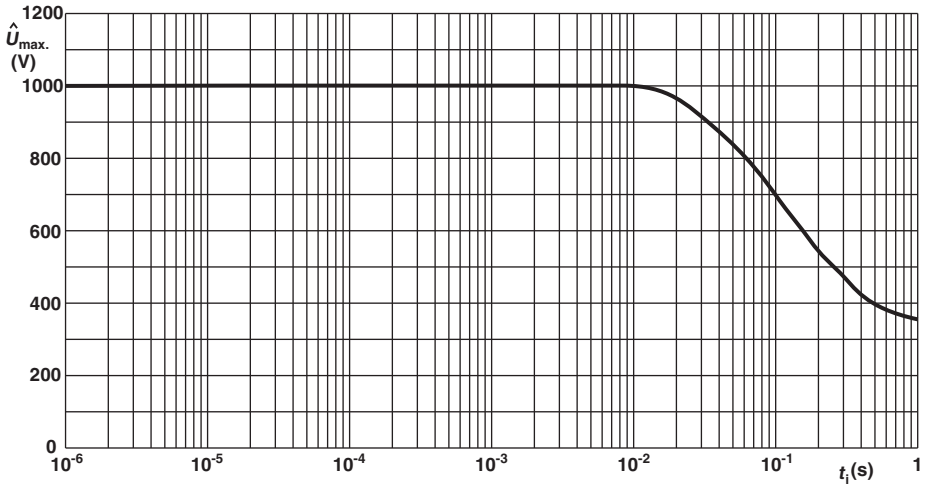
PR02 Drift nomogram



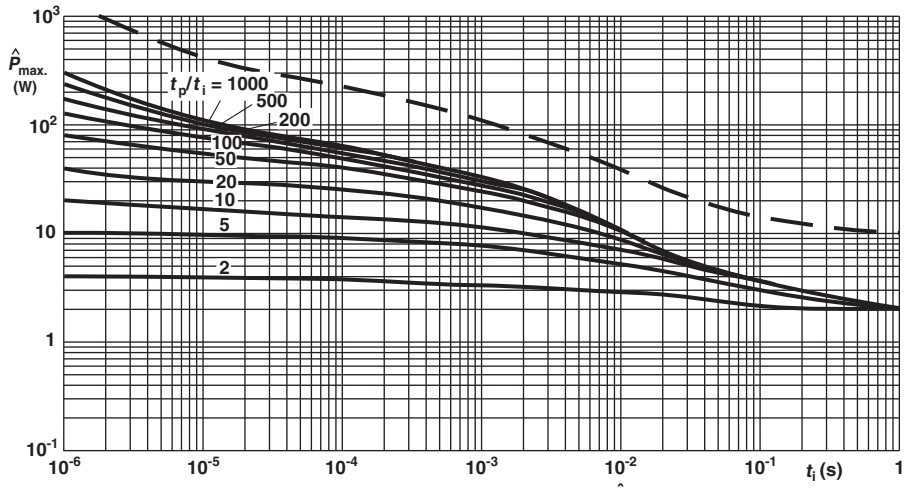
PR03 Drift nomogram



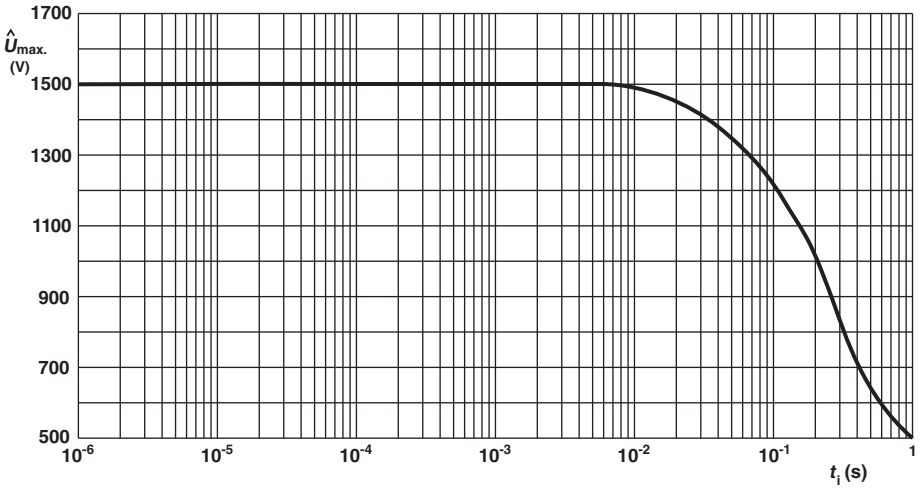
PR01 Pulse on a regular basis; maximum permissible peak pulse power ($\hat{P}_{max.}$) as a function of pulse duration (t_i)



PR01 Pulse on a regular basis; maximum permissible peak pulse voltage ($\hat{U}_{max.}$) as a function of pulse duration (t_i)



PR02 Pulse on a regular basis; maximum permissible peak pulse power ($\hat{P}_{max.}$) as a function of pulse duration (t_i)



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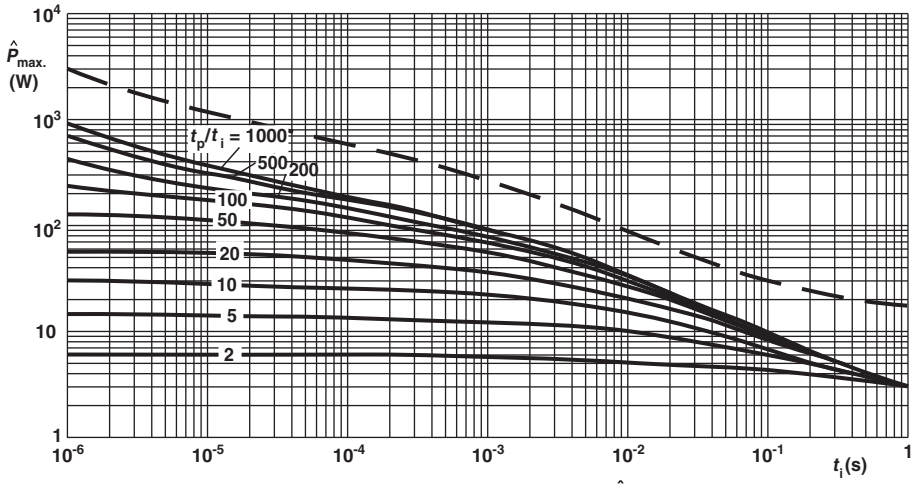
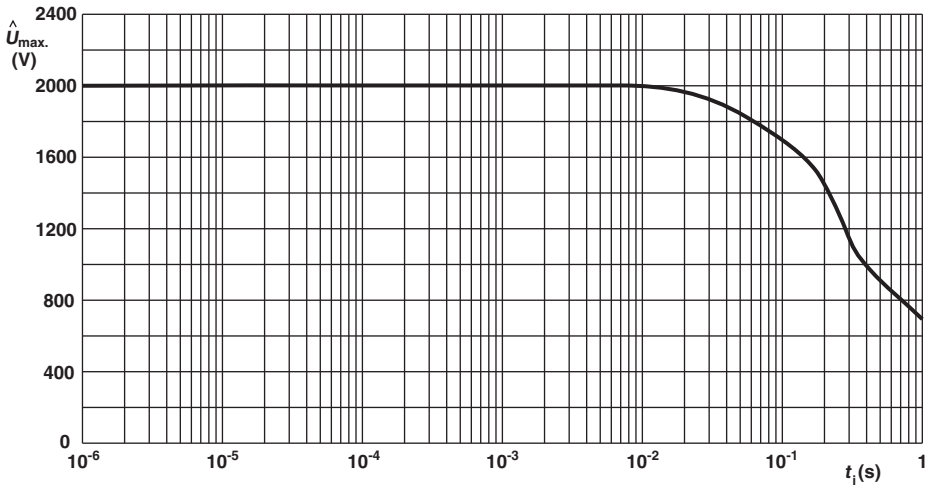
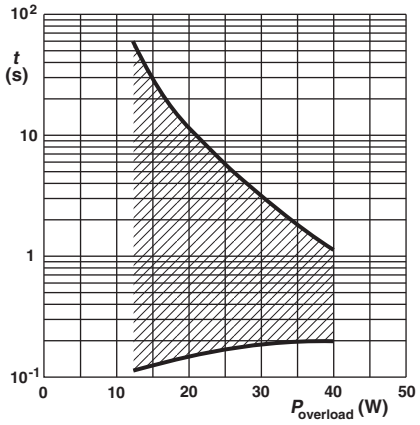


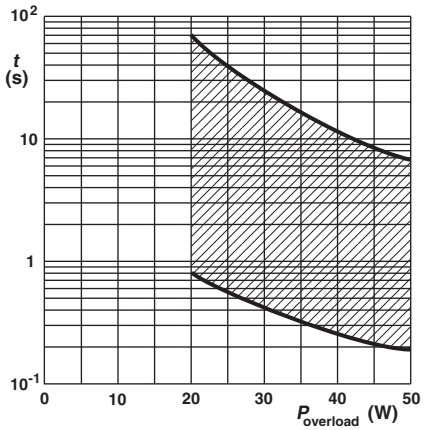
PR03 Pulse on a regular basis; maximum permissible peak pulse power ($\hat{P}_{max.}$) as a function of pulse duration (t_i)



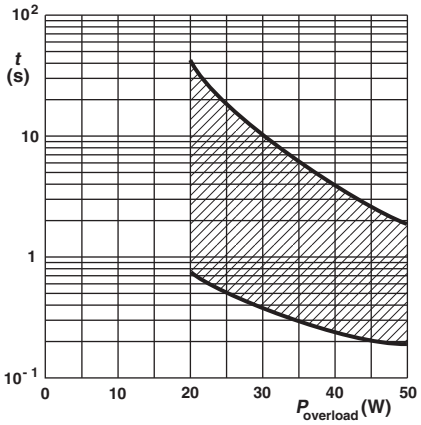
PR03 Pulse on a regular basis; maximum permissible peak pulse voltage ($\hat{U}_{max.}$) as a function of pulse duration (t_i)



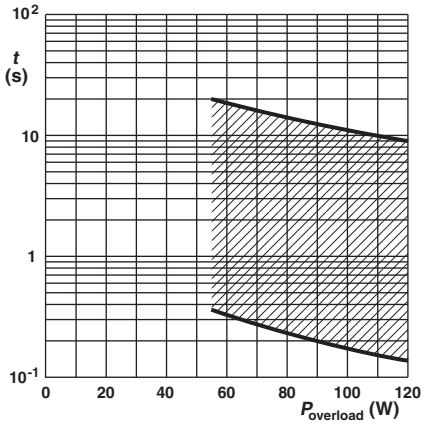
PR01 Time to interruption as a function of overload power for range: 0.22 Ω ≤ R_n < 1 Ω
This graph is based on measured data under constant voltage conditions; the data may deviate according to the applications.



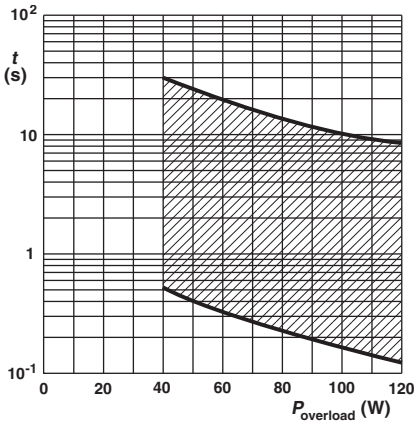
PR01 Time to interruption as a function of overload power for range: 16 Ω ≤ R_n ≤ 560 Ω
This graph is based on measured data under constant voltage conditions; the data may deviate according to the applications.



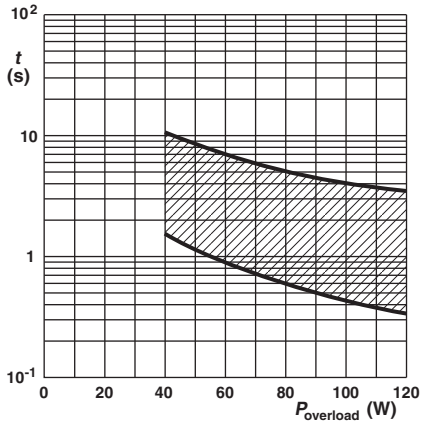
PR01 Time to interruption as a function of overload power for range: 1 Ω ≤ R_n ≤ 15 Ω
This graph is based on measured data under constant voltage conditions; the data may deviate according to the applications.



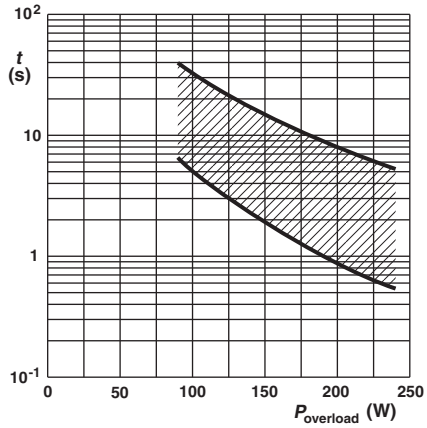
PR02 Time to interruption as a function of overload power for range: 0.33 Ω ≤ R_n ≤ 5 Ω
This graph is based on measured data under constant voltage conditions; the data may deviate according to the applications.



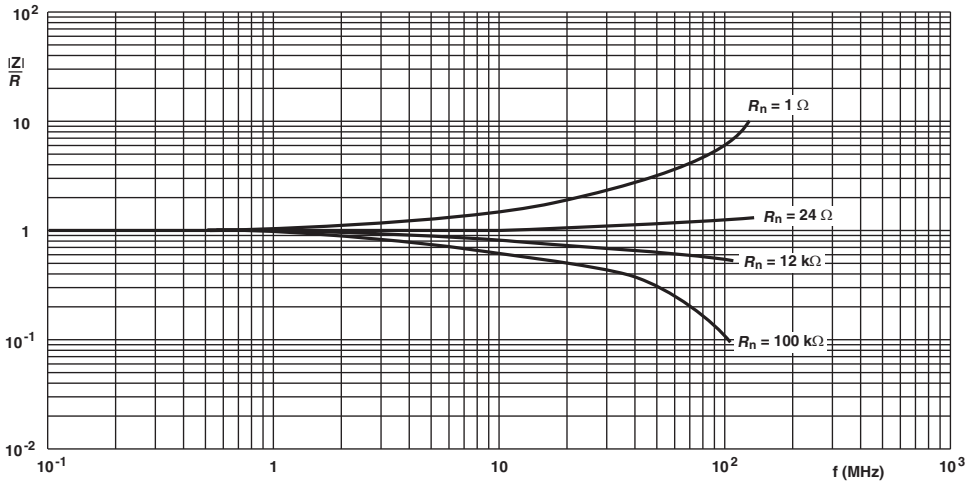
PR02 Time to interruption as a function of overload power for range: 5 Ω ≤ R_n ≤ 68 Ω
This graph is based on measured data under constant voltage conditions; the data may deviate according to the applications.



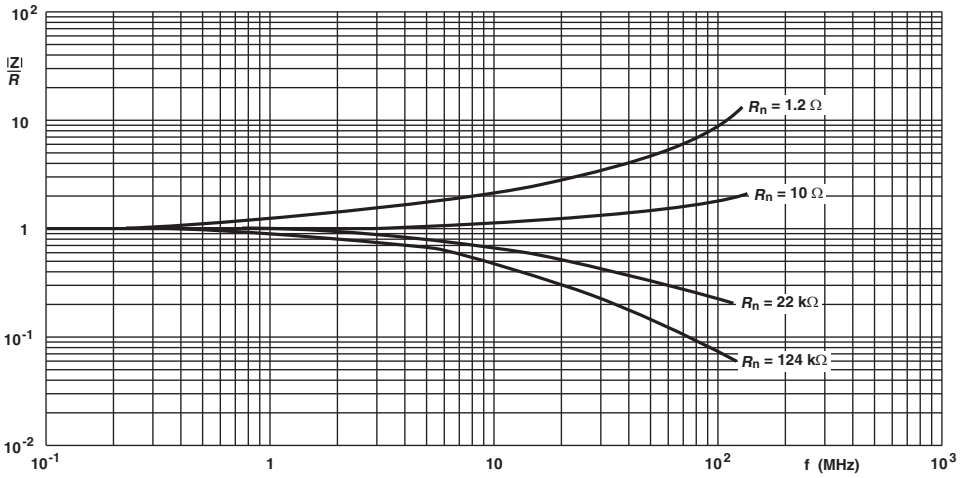
PR02 Time to interruption as a function of overload power for range: 68 Ω ≤ R_n ≤ 560 Ω
This graph is based on measured data under constant voltage conditions; the data may deviate according to the applications.



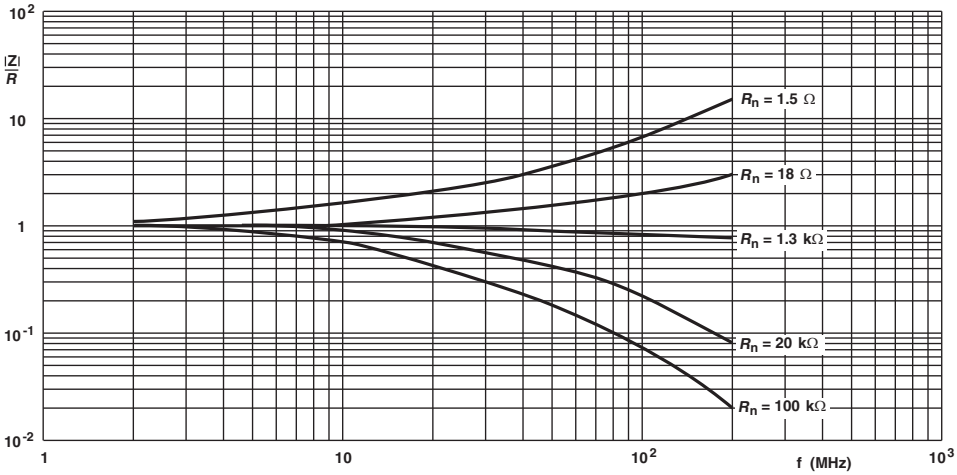
PR03 Time to interruption as a function of overload power for range: 0.68 Ω ≤ R_n ≤ 560 Ω
This graph is based on measured data under constant voltage conditions; the data may deviate according to the applications.



PR01 Impedance as a function of applied frequency



PR02 Impedance as a function of applied frequency



PR03 Impedance as a function of applied frequency

TESTS PROCEDURES AND REQUIREMENTS

All tests are carried out in accordance with the following specifications:

- IEC 60115-1, generic specification (includes tests)

The test and requirements table contains only the most important tests. For the full test schedule refer to the documents listed above.

The tests are carried out in accordance with IEC 60068-2-xx test method and under standard atmospheric conditions in accordance with IEC 60068-1, 5.3.

Climatic category LCT / UCT / 56 (rated temperature range: lower category temperature, upper category temperature; damp heat, steady state, test duration: 56 days) is valid.

Unless otherwise specified the following values apply:

- Temperature: 15 °C to 35 °C
- Relative humidity: 45 % to 75 %
- Air pressure: 86 kPa to 106 kPa (860 mbar to 1060 mbar).

For performing some of the tests, the components are mounted on a test board in accordance with IEC 60115-1, 4.31.

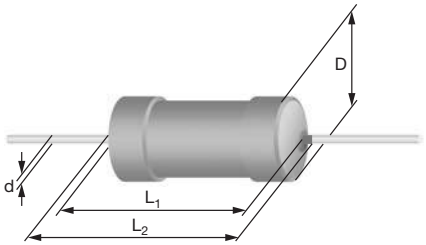
In test procedures and requirements table, only the tests and requirements are listed with reference to the relevant clauses of IEC 60115-1 and IEC 60068-2-xx test methods. A short description of the test procedure is also given.

TEST PROCEDURES AND REQUIREMENTS

IEC 60115-1 CLAUSE	IEC 60068-2-TEST METHOD	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE ($\Delta R_{max.}$)
4.4.1	-	Visual examination		No holes; clean surface; no damage
4.4.2	-	Dimensions (outline)	Gauge (mm)	See Straight and Kinked Dimensions tables
4.5	-	Resistance		± 5 % R
4.6.1.1	-	Insulation resistance	Maximum voltage (DC) after 1 min; metal block method	$R_{ins\ min.}$: 10^4 MΩ
4.7	-	Voltage proof	$U_{RMS} = U_{ins}$; 60 s	No breakdown or flashover
4.8	-	Temperature coefficient	At (20 / -55 / 20) °C and (20 / 155 / 20) °C	≤ ± 250 ppm/K
4.16	21 (Ua_1) 21 (Ub) 21 (Uc)	Robustness of terminations	Tensile, bending, and torsion	No damage $\Delta R_{max.}$: ± (0.5 % R + 0.05 Ω)
4.17	20 (Ta)	Solderability	+235 °C; 2 s; solder bath method; SnPb40	Good tinning (≥ 95 % covered, no visible damage)
			+245 °C; 3 s; solder bath method; SnAg3Cu0.5	Good tinning (≥ 95 % covered, no visible damage)
4.18.2	20 (Tb)	Resistance to soldering heat	Unmounted components (260 ± 5) °C; (10 ± 1) s	$\Delta R_{max.}$: ± (1 % R + 0.05 Ω)
4.19	14 (Na)	Rapid change of temperature	30 min at -55 °C and 30 min at +200 °C; 5 cycles	No visual damage **PR01**: $\Delta R_{max.}$: ± (1 % R + 0.05 Ω) **PR02**: $\Delta R_{max.}$: ± (1 % R + 0.05 Ω) **PR03**: $\Delta R_{max.}$: ± (2 % R + 0.05 Ω)
4.20	29 (Eb)	Bump	3 x 1500 bumps in three directions; 40 g	No damage $\Delta R_{max.}$: ± (0.5 % R + 0.05 Ω)
4.22	6 (Fc)	Vibration	10 sweep cycles per direction; 10 Hz to 2000 Hz; 1.5 mm or 200 m/s^2	No damage $\Delta R_{max.}$: ± (0.5 % R + 0.05 Ω)

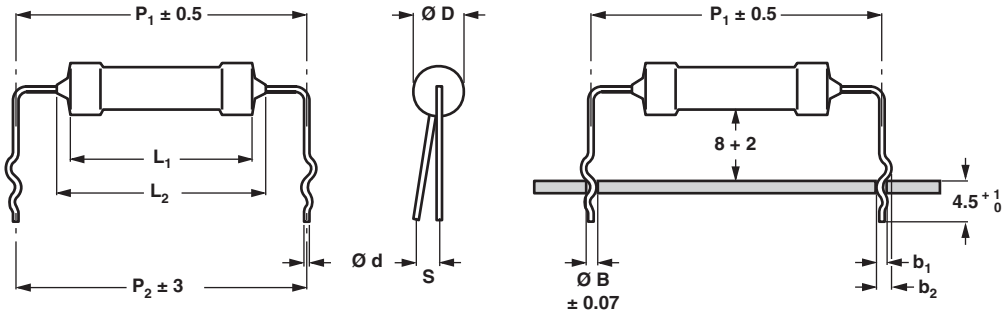
TEST PROCEDURES AND REQUIREMENTS				
IEC 60115-1 CLAUSE	IEC 60068-2-TEST METHOD	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE ($\Delta R_{max.}$)
4.23		Climatic sequence:		$R_{ins\ min.}$: 10^3 MΩ $\Delta R_{max.}$: ± (1.5 % R + 0.1 Ω)
4.23.2	2 (Ba)	Dry heat	200 °C; 16 h	
4.23.3	30 (Db)	Damp heat, cyclic	55 °C; 24 h; 90 % to 100 % RH; 1 cycle	
4.23.4	1 (Aa)	Cold	-55 °C; 2 h	
4.23.5	13 (M)	Low air pressure	8.5 kPa; 2 h; 15 °C to 35 °C	
4.23.6	30 (Db)	Damp heat, cyclic	55 °C; 5 days; 95 % to 100 % RH; 5 cycles	
4.24	78 (Cab)	Damp heat (steady state)	(40 ± 2) °C; 56 days; (93 ± 3)% RH	$\Delta R_{max.}$: ± (3 % R + 0.1 Ω)
4.25.1	-	Endurance (at 70 °C)	$U = \sqrt{P_{70} \times R}$ or $U = U_{max.}$; 1.5 h on; 0.5 h off; 70 °C; 1000 h	$\Delta R_{max.}$: ± (5 % R + 0.1 Ω)
4.26	-	Active flammability	Accidental overload test	No damage, no flamming of gauze cylinder
4.29	45 (Xa)	Component solvent resistance	Isopropyl alcohol (used in industrial application) +23 °C; toothbrush method	Marking legible; no visible damage
4.35	-	Passive flammability	Needle flame test	No ignition of product, no ignition of under layer burning time is less than 30 s

DIMENSIONS



Type with straight leads

DIMENSIONS - Straight lead type and relevant physical dimensions; see straight leads outline						
TYPE	**Ø $D_{MAX.}$ (mm)**	**$L_{1\ MAX.}$ (mm)**	**$L_{2\ MAX.}$ (mm)**	**TERMINATION WIRE MATERIAL (Cu OR FeCu) AND WIRE DIAMETER (Ø d)**		**MASS (mg)**
				MATERIAL	**Ø d (mm)**	
PR01	2.5	6.5	8.0	Cu	0.58 ± 0.05	212
				FeCu	0.58 ± 0.05	207
PR02	3.9	10.0	12.0	Cu	0.78 ± 0.05	504
				FeCu	0.58 ± 0.05	455
				FeCu	0.78 ± 0.05	496
PR03	5.2	16.7	19.5	Cu	0.78 ± 0.05	1192
				FeCu	0.58 ± 0.05	1079
				FeCu	0.78 ± 0.05	1185



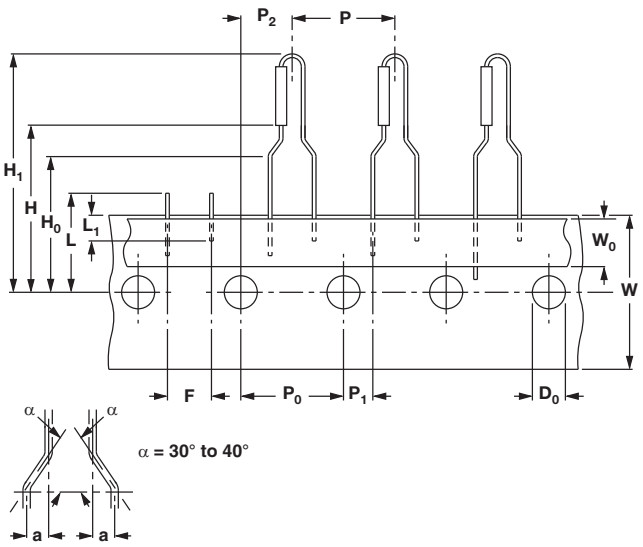
Type with double kink

Dimensions in millimeters

DIMENSIONS - Double kink lead type and relevant physical dimensions; see double kinked outline													
TYPE	**Ø $D_{MAX.}$ (mm)**	**$L_{1\ MAX.}$ (mm)**	**$L_{2\ MAX.}$ (mm)**	**TERMINATION WIRE MATERIAL (Cu OR FeCu) AND WIRE DIAMETER (Ø d)**		**MASS (mg)**	**PITCH (mm)**	**P_1 (mm)**	**P_2 (mm)**	**b_1 (mm)**	**b_2 (mm)**	**$S_{MAX.}$ (mm)**	**Ø B (mm)**
				MATERIAL	**Ø d (mm)**								
PR01	2.5	6.5	8.0	Cu	0.58 ± 0.05	212	17.8	17.8 ± 0.5	17.8 ± 3	1.10 + 0.25 / - 0.20	1.45 + 0.25 / - 0.20	2	0.8 ± 0.07
				FeCu	0.58 ± 0.05	207	12.5	12.5 ± 0.5	12.5 ± 3	1.10 + 0.25 / - 0.20	1.45 + 0.25 / - 0.20	2	0.8 ± 0.07
				FeCu	0.58 ± 0.05	207	17.8	17.8 ± 0.5	17.8 ± 3	1.10 + 0.25 / - 0.20	1.45 + 0.25 / - 0.20	2	0.8 ± 0.07
PR02	3.9	10.0	12.0	Cu	0.78 ± 0.05	504	17.8	17.8 ± 0.5	17.8 ± 3	1.10 + 0.25 / - 0.20	1.45 + 0.25 / - 0.20	2	1.0 ± 0.07
				FeCu	0.58 ± 0.05	455	17.8	17.8 ± 0.5	17.8 ± 3	1.10 + 0.25 / - 0.20	1.45 + 0.25 / - 0.20	2	0.8 ± 0.07
				FeCu	0.78 ± 0.05	496	15.0	15.0 ± 0.5	15.0 ± 3	1.30 + 0.25 / - 0.20	1.65 + 0.25 / - 0.20	2	1.0 ± 0.07
PR03	5.2	16.7	19.5	Cu	0.78 ± 0.05	1192	25.4	25.4 ± 0.5	25.4 ± 3	1.10 + 0.25 / - 0.20	1.65 + 0.25 / - 0.20	2	1.0 ± 0.07
				FeCu	0.58 ± 0.05	1079	25.4	25.4 ± 0.5	25.4 ± 3	1.10 + 0.25 / - 0.20	1.65 + 0.25 / - 0.20	2	1.0 ± 0.07
				FeCu	0.78 ± 0.05	1185	20	22.0 ± 0.5	20.0 ± 3	1.30 + 0.25 / - 0.20	2.15 + 0.25 / - 0.20	2	1.0 ± 0.07

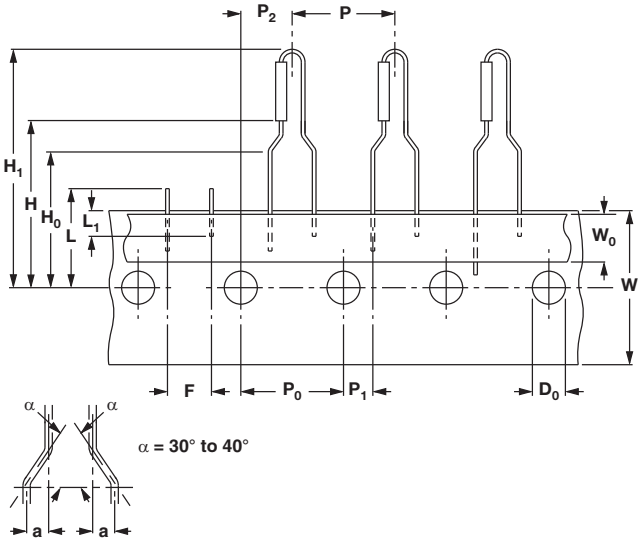
PR01, PR02 WITH RADIAL TAPING

PR01 - Height for insertion (max.) = 32 mm



DIMENSIONS in millimeters		
Pitch of components	P	12.7 ± 1.0
Feed-hole pitch	P_0	12.7 ± 0.2
Feed-hole centre to lead at topside at the tape	P_1	3.85 ± 0.5
Feed-hole center to body center	P_2	6.35 ± 1.0
Lead spacing	F	4.8 +0.7/-0
Width of carrier tape	W	18.0 ± 0.5
Minimum hold down tape width	W_0	5.5
Height for insertion (max.)	H1	32
Lead wire clinch height	H_0	16.5 ± 0.5
Body to hole center	H	19.5 ± 1
Feed-hole diameter	D_0	4.0 ± 0.2
Height for cutting (max.)	L	11.0
Minimum lead wire (tape portion) shortest lead	L_1	2.5

PR02 - Height for insertion (max.) = 29 mm



DIMENSIONS in millimeters		
Pitch of components	P	12.7 ± 1.0
Feed-hole pitch	P_0	12.7 ± 0.2
Feed-hole centre to lead at topside at the tape	P_1	3.85 ± 0.5
Feed-hole center to body center	P_2	6.35 ± 1.0
Lead spacing	F	4.8 +0.7/-0
Width of carrier tape	W	18.0 ± 0.5
Minimum hold down tape width	W_0	5.5
Height for insertion (max.)	H1	29
Lead wire clinch height	H_0	16.5 ± 0.5
Body to hole center	H	19.5 ± 1
Feed-hole diameter	D_0	4.0 ± 0.2
Height for cutting (max.)	L	11.0
Minimum lead wire (tape portion) shortest lead	L_1	2.5

MARKING

The nominal resistance and tolerance are marked on the resistor using four or five colored bands in accordance with IEC 60062, marking codes for resistors and capacitors.

12NC INFORMATION FOR HISTORICAL CODING REFERENCE

The resistors have a 12-digit numeric code starting with 23

For 5 % tolerance:

- The next 7 digits indicate the resistor type and packing
- The remaining 3 digits indicate the resistance value:
  - The first 2 digits indicate the resistance value
  - The last digit indicates the resistance decade

For 1 % tolerance:

- The next 6 digits indicate the resistor type and packing
- The remaining 4 digits indicate the resistance value:
  - The first 3 digits indicate the resistance value
  - The last digit indicates the resistance decade

Last Digit of 12NC Indicating Resistance Decade

RESISTANCE DECADE	LAST DIGIT
0.22 Ω to 0.91 Ω	7
1 Ω to 9.76 Ω	8
10 Ω to 97.6 Ω	9
100 Ω to 976 Ω	1
1 Ω to 9.76 kΩ	2
10 Ω to 97.6 kΩ	3
100 Ω to 976 kΩ	4
1 MΩ	5

12NC Example

The 12NC for resistor type PR02 with Cu leads and a value of 750 Ω with 5 % tolerance, supplied on a bandolier of 1000 units in ammopack, is: 2306 198 53751.

12NC - Resistor Type and Packaging [1]

TYPE	LEAD Ø mm	TOL. (%)	23.. ... . (BANDOLIER)						
			AMMOPACK					REEL	
			RADIAL TAPED		STRAIGHT LEADS				RADIAL TAPED
					52 mm	52 mm	63 mm	52 mm	
			4000 UNITS	3000 UNITS	5000 UNITS	1000 UNITS	500 UNITS	5000 UNITS	2000 UNITS
PR01	Cu 0.58	1	-	-	**22 196 1....**	06 191 2....	-	06 191 5....	-
		5	06 197 03...	-	**22 193 14...**	06 197 53...	-	**06 197 23...**	-
PR02	Cu 0.78	1	-	22 197 2....	-	**22 197 1....**	-	-	**2322 197 5....**
		5	-	06 198 03...	-	**06 198 53...**	-	-	**2322 198 04...**
	FeCu 0.58	5	-	-	-	22 194 54...	-	-	-
PR03	Cu 0.78	5	-	-	-	-	**22 195 14...**	-	-
		1	-	-	-	-	**06 199 6...**	-	-
	FeCu 0.58	5	-	-	-	-	**22 195 54...**	-	-

Notes

- Preferred types in bold

[1] Other packaging versions are available on request

12NC - Resistor Type and Packaging

TYPE	LEAD Ø mm	TOL. (%)	23.. ... . (LOOSE IN BOX)			
			DOUBLE KINK			
			PITCH = 17.8 mm	PITCH = 25.4 mm	PITCH [2][3][4]	
			1000 UNITS	500 UNITS	1000 UNITS	500 UNITS
PR01	Cu 0.58	5	22 193 03...	-	-	-
	FeCu 0.58	5	22 193 43...	-	**22 193 53...** [2]	-
PR02	Cu 0.78	5	22 194 23...	-	-	-
	FeCu 0.58	5	22 194 83...	-	-	-
	FeCu 0.78	5	-	-	**22 194 63...** [3]	-
PR03	Cu 0.78	5	-	22 195 23...	-	-
	FeCu 0.58	5	-	22 195 83...	-	-
	FeCu 0.78	5	-	-	-	**22 195 63...** [4]

Notes

- Preferred types in bold

[2] PR01 pitch 12.5 mm

[3] PR02 pitch 15.0 mm

[4] PR03 pitch 20.0 mm, with reversed kinking direction as opposed to the drawing for the type with double kink figure

3.0A SURFACE MOUNT SCHOTTKY BARRIER RECTIFIER

Product Summary

B320A-B340A:

V_{RRM} (V)	I_O(A)	$V_{F(MAX)}$ @ 3A (V)	$I_{R(MAX)}$ @ V_{RRM} (mA)
20, 30, 40	3.0	0.50	0.5

B350-B360A:

V_{RRM} (V)	I_O(A)	$V_{F(typ)}$ @ +125°C (V)	$I_{R(MAX)}$ @ V_{RRM} (mA)
50, 60	3.0	0.70	0.5

Features

- Guard Ring Die Construction for Transient Protection
- Ideally Suited for Automated Assembly
- Low Power Loss, High Efficiency
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Notes 3 & 4)**
- **Qualified to AEC-Q101 Standards for High Reliability**

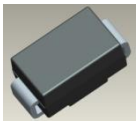
Description and Applications

For use in low-voltage, high-frequency inverters, freewheeling, DC-DC converters, and polarity protection applications.

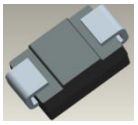
Mechanical Data

- Case: SMA
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Lead Free Plating (Matte-Tin Finish). Solderable per MIL-STD-202, Method 208 e3
- Polarity: Cathode Band
- Weight: 0.064 grams (Approximate)

SMA



Top View



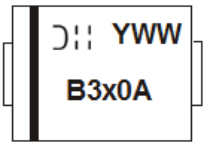
Bottom View

Ordering Information (Note 5)

Part Number*	Compliance	Case	Packaging
B3XXA-13-F	Standard	SMA	5,000/Tape & Reel

* XX = Device Type, e.g. B320A-13-F (SMA Package).

Marking Information (Note 6)



B3x0A = Product Type Marking Code, ex: B320A
= Manufacturers' Code Marking
YWW = Date Code Marking
Y = Last Digit of Year (ex: 15 for 2015)
WW = Week Code (01 to 53)

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Products manufactured with Date Code 0924 (week 24, 2009) and newer are built with Green Molding Compound.
5. For packaging details, go to our website at http://www.diodes.com/products/packages.html.
6. Device has a cathode band (as shown above) and may also have a cathode notch.

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Single phase, half wave, 60Hz, resistive or inductive load.
For capacitance load, derate current by 20%.

Characteristic	Symbol	B320A	B330A	B340A	B350A	B360A	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	50	60	V
Average Rectified Output Current @ T_T = +100°C	I_O	3.0					A
Non-Repetitive Peak Forward Surge Current 8.3ms Single Half Sine-Wave Superimposed on Rated Load	I_{FSM}	80					A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Maximum Total Power Dissipation - Steady State, T_A = +25°C (Note 7)	P_D	850	mW
Typical Thermal Resistance, Junction to Ambient (Note 7)	$R_{\theta JA}$	140	°C/W
Typical Thermal Resistance, Junction to Terminal (Note 8)	$R_{\theta JT}$	25	°C/W
Typical Thermal Resistance, Junction to Ambient (Note 8)	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
Forward Voltage Drop	B320A, B330A, B340A	V_F	—	—	0.50	V	I_F = 3.0A, T_A = +25°C
	B350A, B360A		—	—	0.70		
Leakage Current (Note 9)		I_R	—	—	0.5	mA	@ Rated V_R, T_A = +25°C
			—	—	20		@ Rated V_R, T_A = +100°C
Total Capacitance		C_T	—	200	—	pF	V_R = 4V, f = 1MHz

Notes: 7. Device mounted on FR-4 PCB, with minimum recommended pad layout.
8. Device mounted on glass epoxy substrate with 2x3mm copper pad.
9. Short duration pulse test used to minimize self-heating effect.

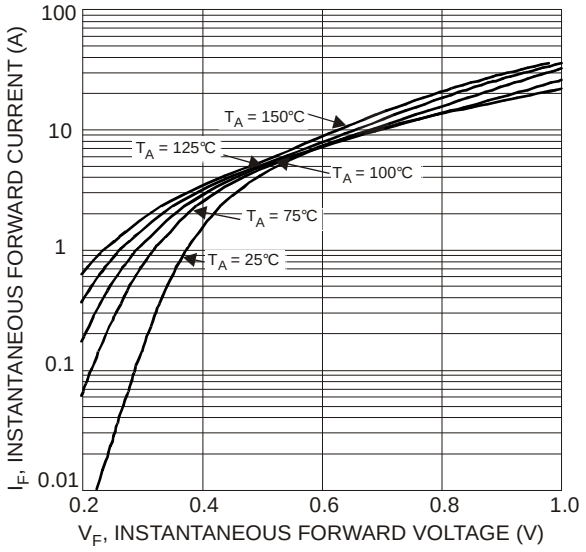


Fig. 1 Typical Forward Characteristics - B320A thru B340A

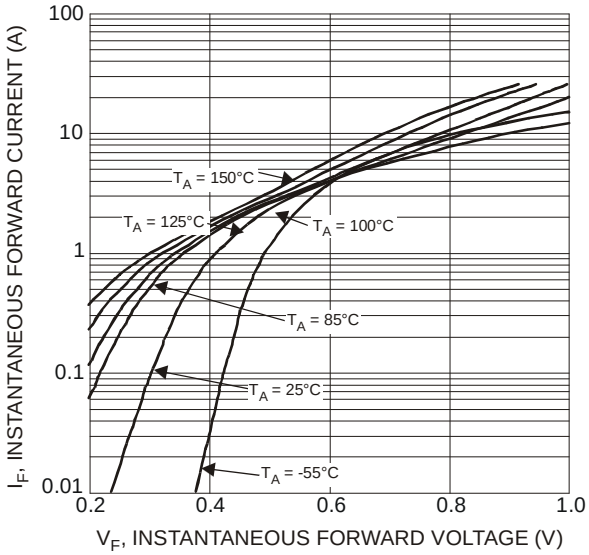


Fig. 2 Typ. Forward Characteristics - B350A thru B360A

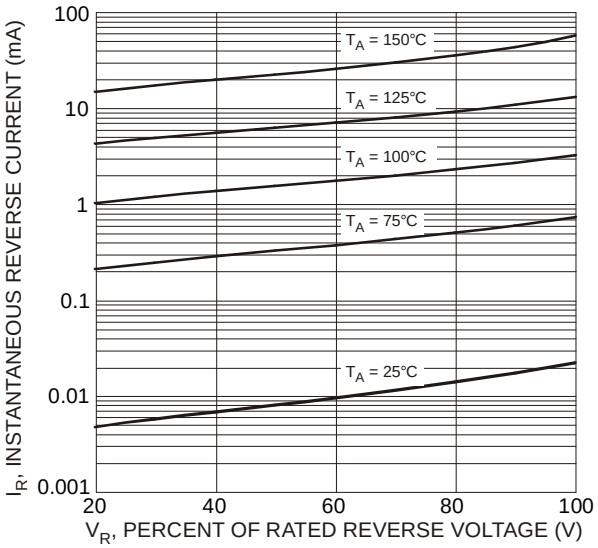


Fig. 3 Typical Reverse Characteristics, B320A thru B340A

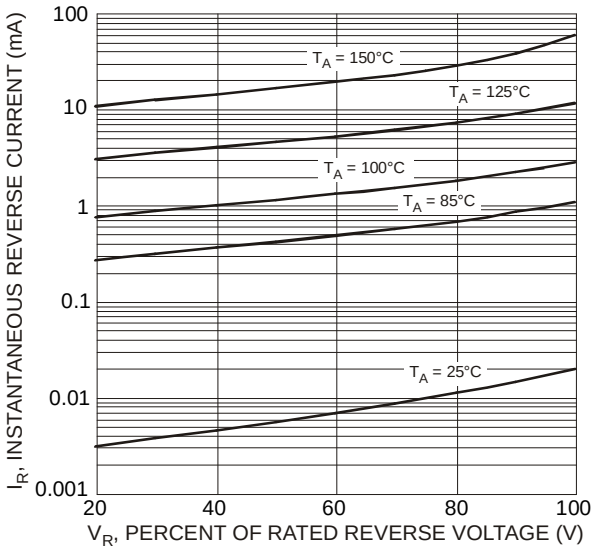


Fig. 4 Typical Reverse Characteristics, B350A thru B360A

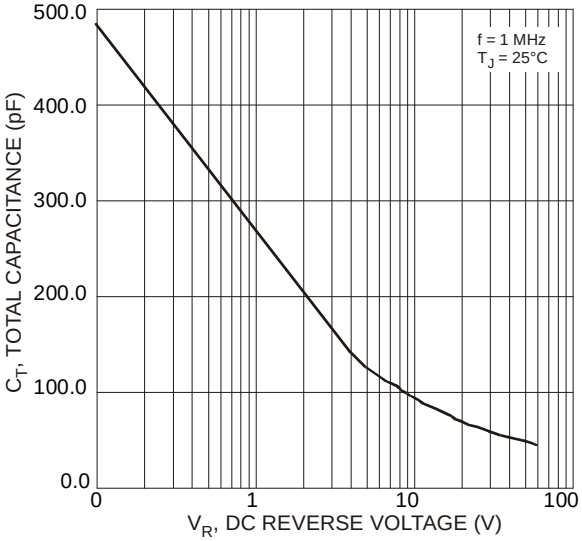


Fig. 5 Total Capacitance vs. Reverse Voltage

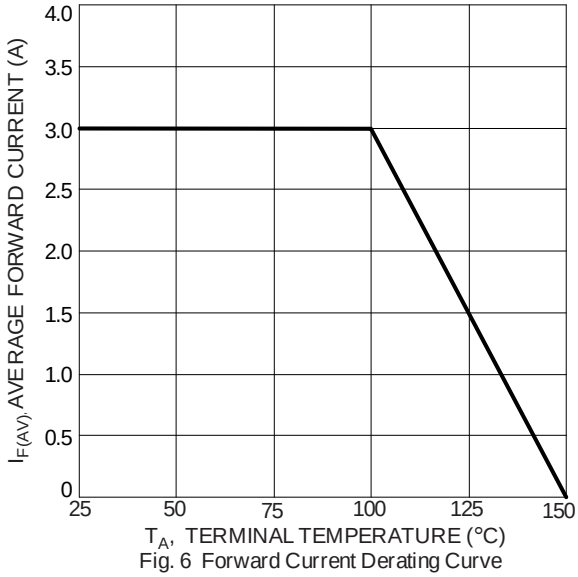


Fig. 6 Forward Current Derating Curve

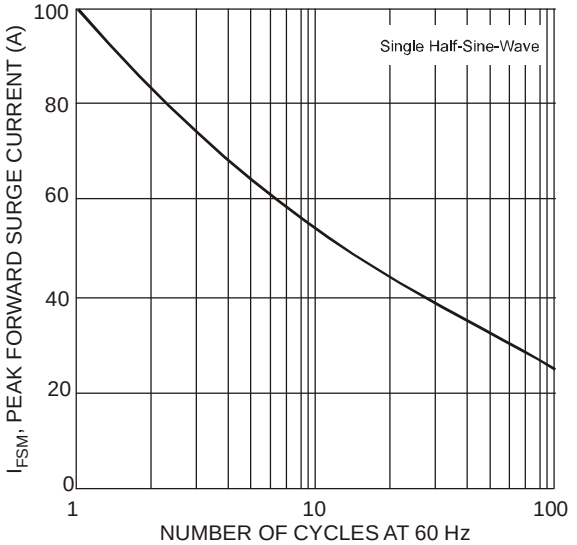


Fig. 7 Max Non-Repetitive Peak Fwd Surge Current

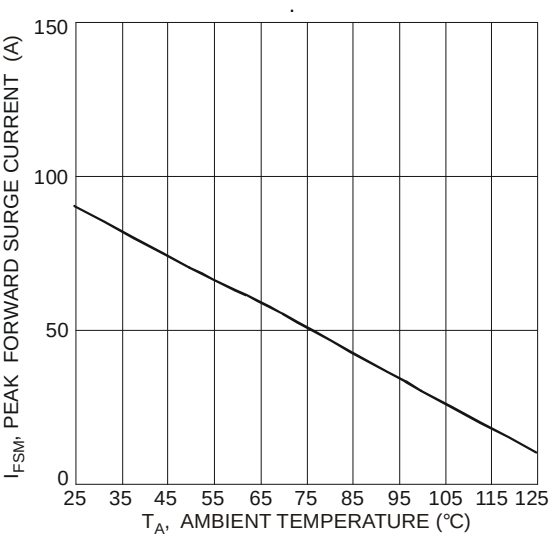


Fig. 8 Non-Repetitive Forward Surge Current Derating Curve

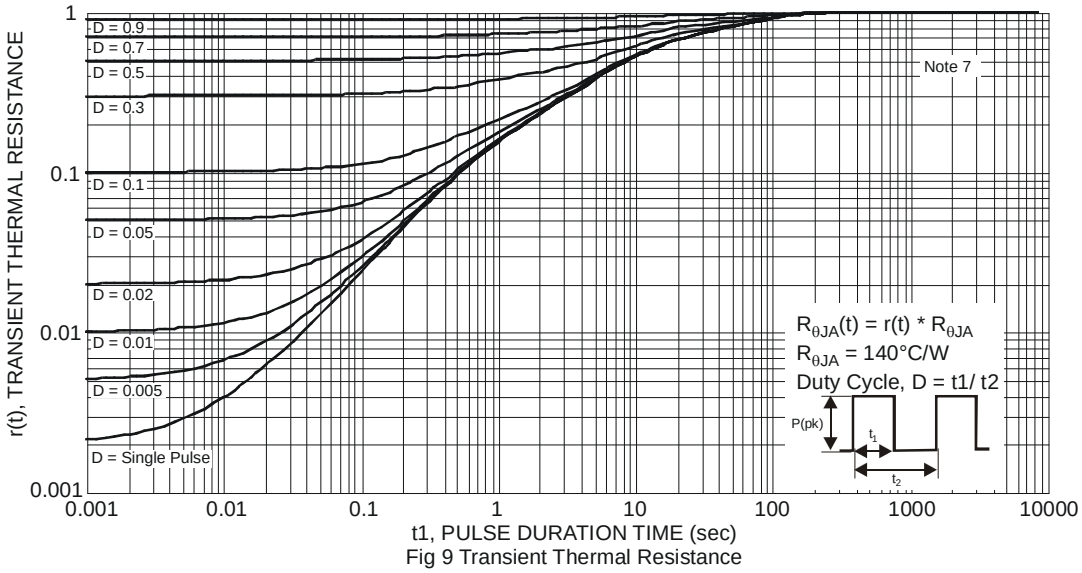


Fig 9 Transient Thermal Resistance
B320A-B340A

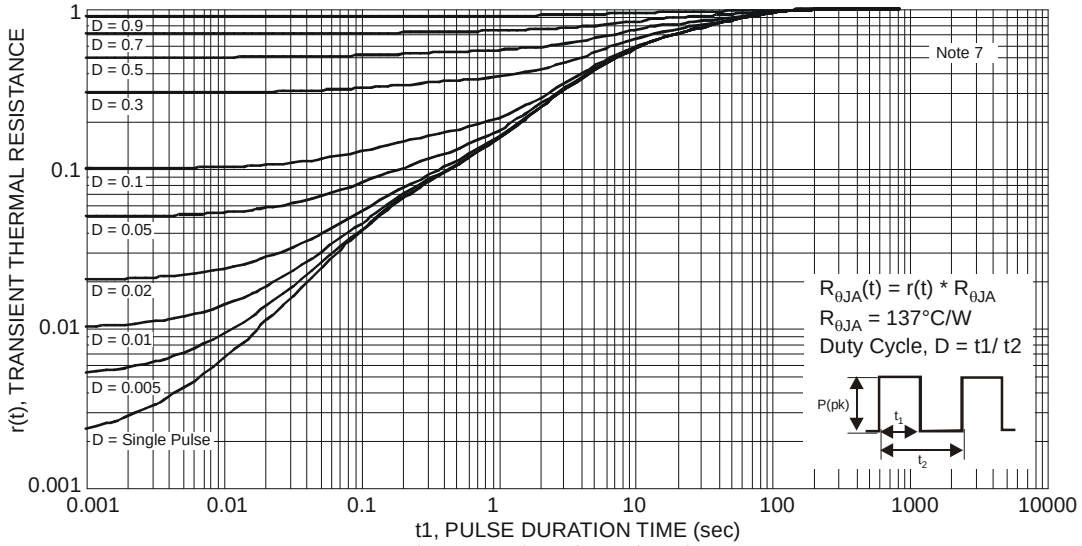


Fig 10 Transient Thermal Resistance
B350A-B360A

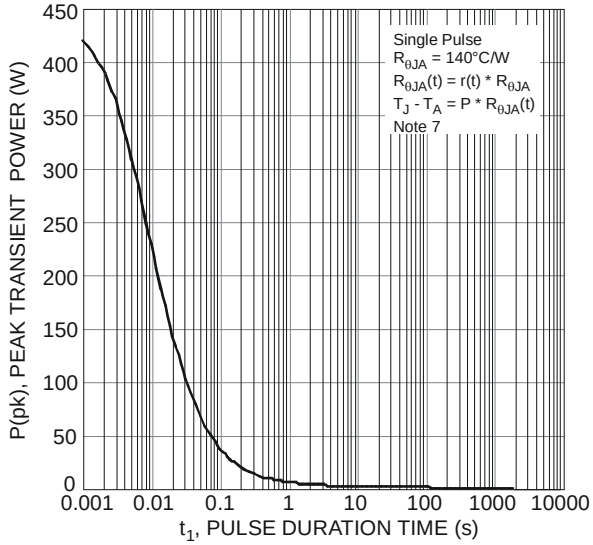


Fig. 11 Single Pulse Maximum Power Dissipation
(B320A-B340A)

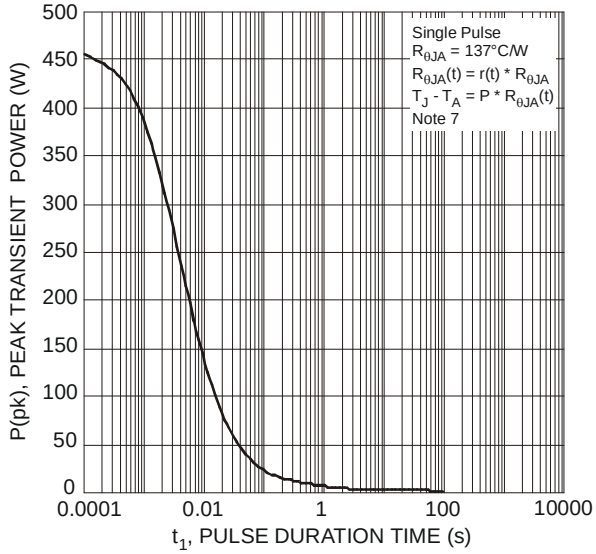
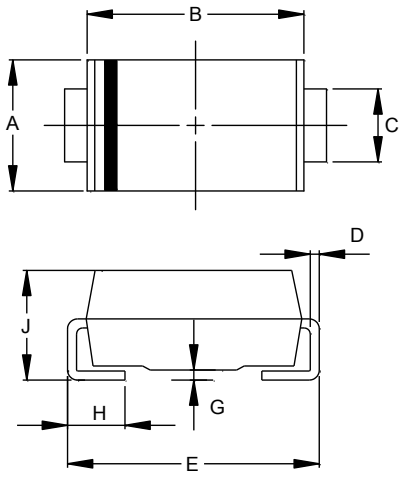


Fig. 12 Single Pulse Maximum Power Dissipation
(B350A-B360A)

Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

SMA

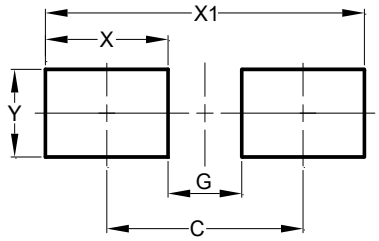


SMA		
Dim	**Min**	**Max**
A	2.29	2.92
B	4.00	4.60
C	1.27	1.63
D	0.15	0.31
E	4.80	5.59
G	0.05	0.20
H	0.76	1.52
J	1.96	2.40
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

SMA

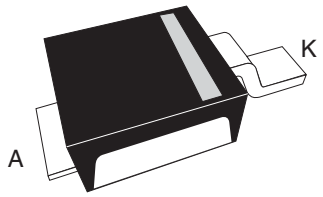


Dimensions	Value (in mm)
C	4.00
G	1.50
X	2.50
X1	6.50
Y	1.70

SM2T3V3A

Low voltage Transil™

Datasheet - production data



DO-216AA
(STmite)

Description

The SM2T3V3A is a Transil diode designed specifically for portable equipment and miniaturized electronic devices subject to ESD transient overvoltages. It's low stand-off voltage makes it suitable for low voltage applications very sensitive to EOS and ESD events.

Transil diodes provide high overvoltage protection by clamping action.

Features

- Unidirectional Transil diode
- High peak pulse power: 200 W (10/1000 µs)
- Stand-off voltage 3.3 V
- Low clamping factor V_{CL}/V_{BR}
- Fast response time
- JEDEC registered package outline

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute rating (limiting value)

Symbol	Parameter		Value	Unit
P_{PP}	Peak pulse power dissipation(1)	T_j initial = T_{amb}	200	W
P	Power dissipation on infinite heatsink	T_{amb} = 100°C	2.5	W
I_{FSM}	Non repetitive surge peak forward current	t_p = 10 ms T_j initial = T_{amb}	25	A
T_{stg} T_j	Storage temperature range Maximum operating junction temperature		-65 to +175 150	°C
T_l	Lead solder temperature (10 seconds duration)		260	°C

1. 10/1000 µs pulse waveform

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction to leads	20	°C/W
$R_{th(j-a)}$	Junction to ambient on PCB with recommended pad layout	250	°C/W

Table 3. Electrical characteristics - parameters (T_{amb} = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Peak pulse current.
αT	Voltage temperature coefficient
V_F	Forward voltage drop

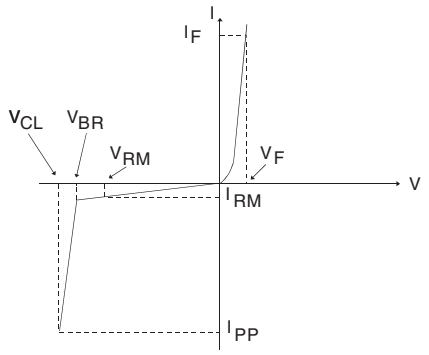
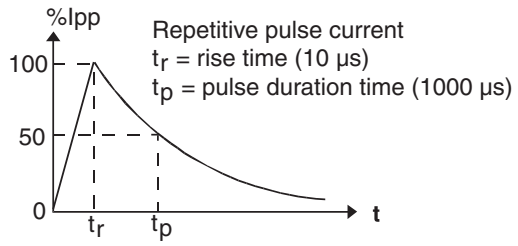


Table 4. Electrical characteristics - values (T_{amb} = 25 °C)

Order code	I_{RM} max @ V_{RM}		V_{BR} min @ I_R(1)		V_{CL} max @ I_{PP} 10/1000 µs		V_{CL} max @ I_{PP} 10/1000 µs		αT max(2)	C max(3)
	µA	V	V	mA	V	A	V	A	10^{-4}/°C	pF
SM2T3V3A	500	3.3	3.6	1	6.5	25	6.8	30	-5.3	2500

1. Pulse test t_p < 50 ms
2. $\Delta V_{BR} = \alpha T * (T_{amb} - 25) * V_{BR}$ (25 °C)
3. V_R = 0 V, F = 1 MHz

Figure 1. Pulse waveform



2 Package information

- Epoxy meets ul94, v0
- Band indicates cathode

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 2. Package dimensions - parameters

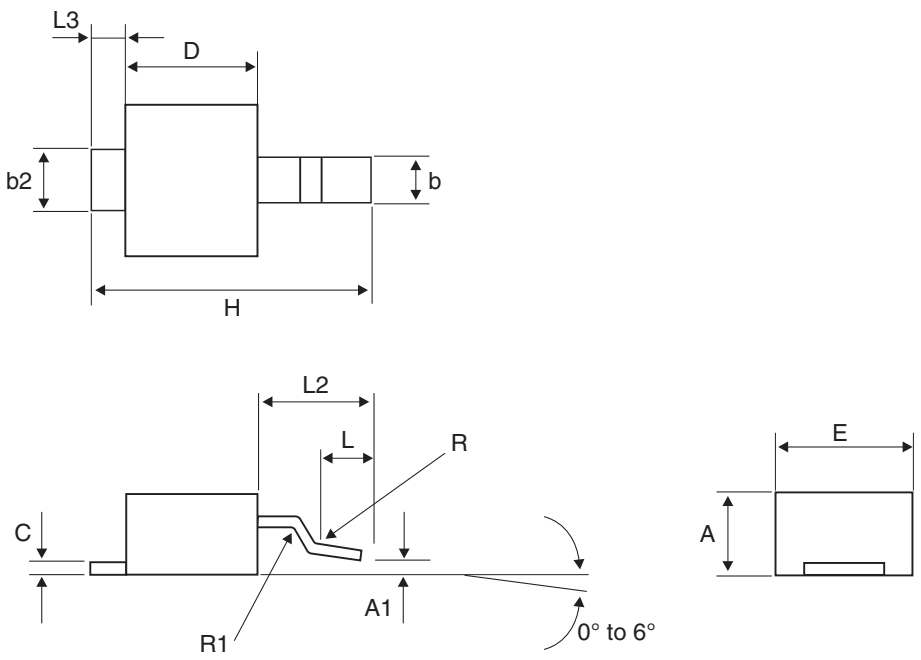
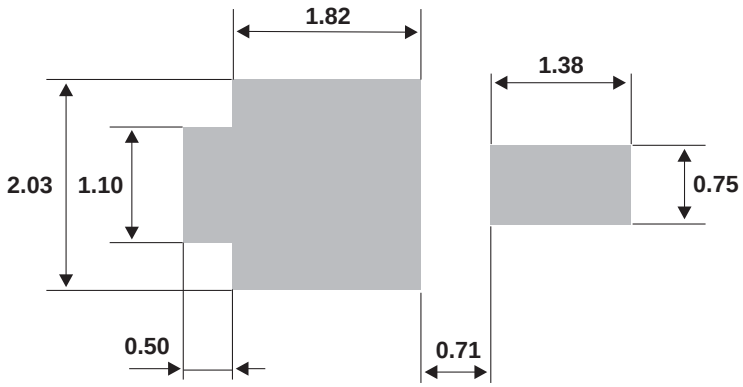


Table 5. Package dimensions - values

Ref.	Dimensions					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.85	1.00	1.15	0.033	0.039	0.045
A1	-0.05		0.105	-0.002		0.002
b	0.40		0.65	0.016		0.025
b2	0.70		1.00	0.027		0.039
c	0.10		0.25	0.004		0.010
D	1.75	1.90	2.05	0.069	0.007	0.081
E	1.75	1.90	2.05	0.069	0.007	0.081
H	3.60	3.75	3.90	0.142	0.148	0.154
L	0.50	0.63	0.80	0.047	0.025	0.031
L2	1.20	1.35	1.50	0.047	0.053	0.059
L3		0.50 ref			0.019 ref	
R	0.07			0.003		
R1	0.07			0.003		

Figure 3. Recommended footprint (dimensions in mm)



SS24FL, SS26FL

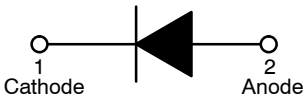
Surface Mount Schottky Barrier Rectifier

ON Semiconductor®

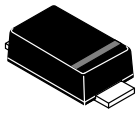
www.onsemi.com

Features

- Ultra Thin Profile – Maximum Height of 1.08 mm
- UL Flammability 94V–0 Classification
- MSL 1
- Green Mold Compound
- These Devices are Pb–Free, Halogen Free Free and are RoHS Compliant



Schottky Barrier Rectifier



SOD–123F
CASE 425AD

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value		Unit
		SS24FL	SS26FL	
V_{RRM}	Peak Reverse Voltage	40	60	V
V_R	Reverse Voltage	40	60	V
$I_{F(AV)}$	Average Rectified Current at T_A = 75°C	2.0		A
I_{FSM}	Non–Repetitive Peak Forward Surge Current at t = 8.3 ms	50		A
T_J	Operating Junction Temperature Range	–55 to +125		°C
T_{STG}	Storage Temperature Range	–55 to +125		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAMS

Band Indicates Cathode

&Y = Binary Calendar Year Coding Scheme
&Z = Assembly Plant Code
GP = Specific Device Code
&G = Single Digit Weekly Data Code

Band Indicates Cathode

&Y = Binary Calendar Year Coding Scheme
&Z = Assembly Plant Code
GQ = Specific Device Code
&G = Single Digit Weekly Data Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Value	Unit
$R_{\theta JA}$	Typical Thermal Resistance, Junction−to−Ambient (Note 1)	140	°C/W

1. Mounted with minimum recommended pad size, PC board FR4.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
BV_R	Reverse Breakdown Voltage	I_R = 500 μA	SS24FL	40	–	–	V
			SS26FL	60	–	–	
V_F	Forward Voltage	I_F = 2.0 A	SS24FL	–	–	0.55	V
			SS26FL	–	–	0.70	
I_R	Reverse Leakage Current	$V_R = V_{RRM}$	SS24FL	–	–	100	μA
			SS26FL	–	–	40	
T_{rr}	Reverse Recovery Time	I_F = 0.5 A, I_R = 1 A, I_{rr} = 0.25 A	SS24FL	–	9.495	–	ns
			SS26FL	–	8.260	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping†
SS24FL	GP	SOD−123F (Pb−Free/Halogen Free)	3000 / Tape & Reel
SS26FL	GQ	SOD−123F (Pb−Free/Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL PERFORMANCE CHARACTERISTICS

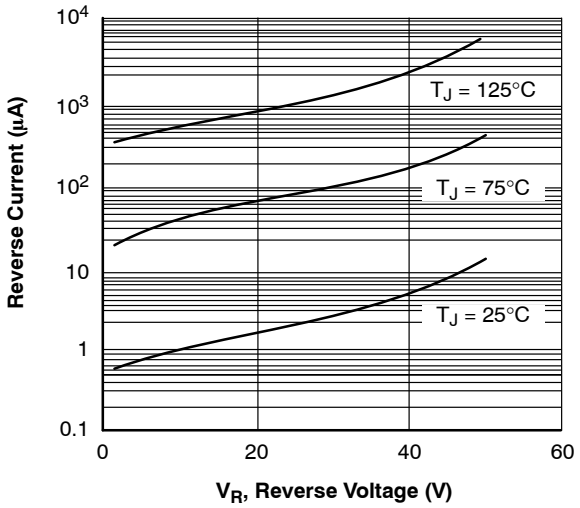


Figure 1. Typical Reverse Characteristics

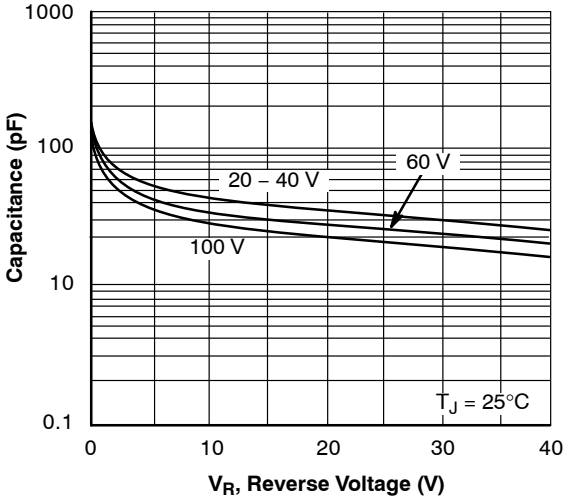


Figure 2. Typical Junction Characteristics

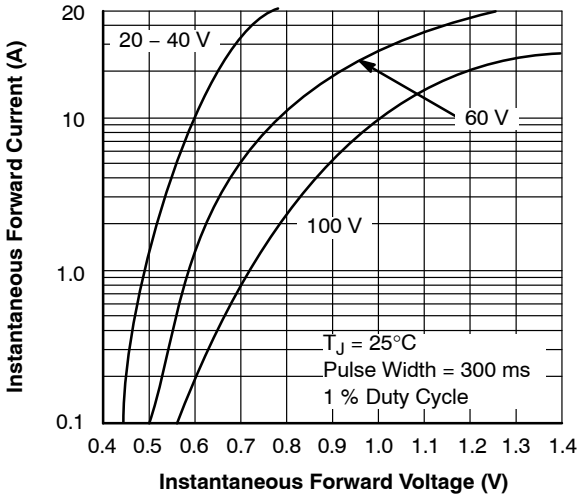
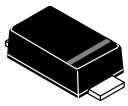


Figure 3. Typical Instantaneous Forward Characteristics

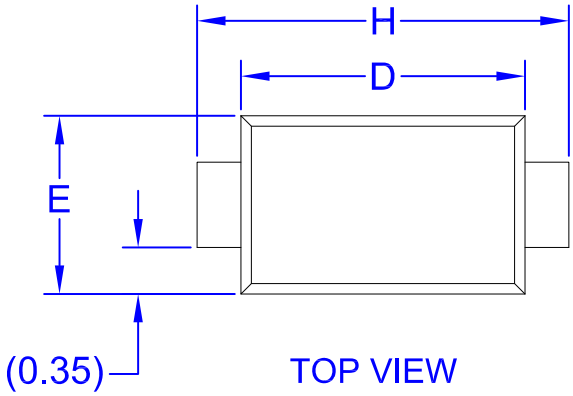


SCALE 4:1

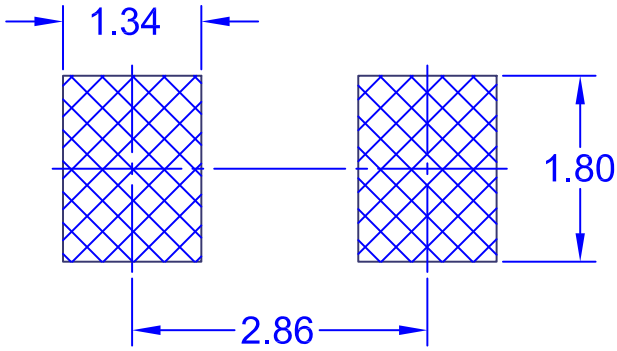
SOD−123FL
CASE 425AD
ISSUE A

DATE 04 AUG 2017

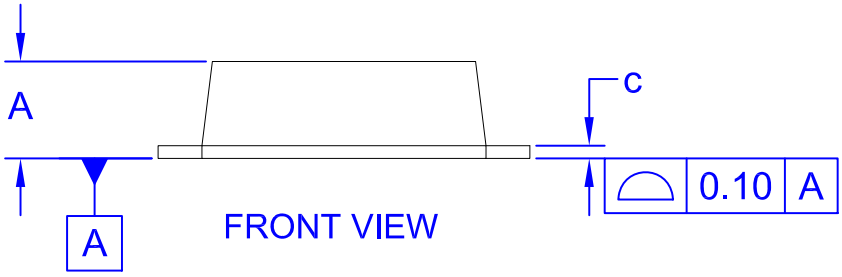
NOTES:
A. NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.



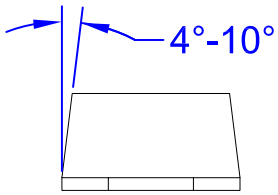
TOP VIEW



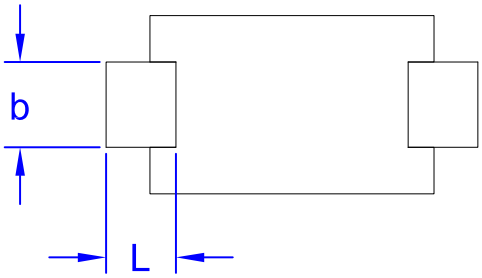
LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.031	0.043	0.80	1.08
b	0.020	0.045	0.50	1.15
c	0.002	0.008	0.05	0.20
D	0.098	0.118	2.50	3.00
E	0.059	0.077	1.50	1.95
H	0.130	0.154	3.30	3.90
L	0.018	0.035	0.45	0.90

DOCUMENT NUMBER:	**98AON13725G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOD−123FL**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

Technical Data
Data Sheet N0942, Rev. A

Green Products

SK220A SCHOTTKY RECTIFIER

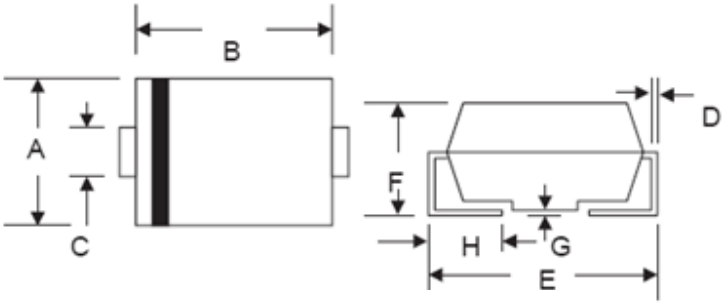
Applications:

- **Switching power supply**
- **Converters**
- **Free-Wheeling diodes**
- **Reverse battery protection**

Features:

- **Small foot print, surface mountable**
- **Very low forward voltage drop**
- **High frequency operation**
- **Guard ring for enhanced ruggedness and long term reliability**
- **Green products in compliance the ROHS directive**
- **Pure tin plated, solderable per MIL-STD-750, Method 2026**
- **This is a Halogen Free device**
- **All SMC parts are traceable to the wafer lot**
- **Additional testing can be offered upon request**

Mechanical Dimensions (In mm / Inches)

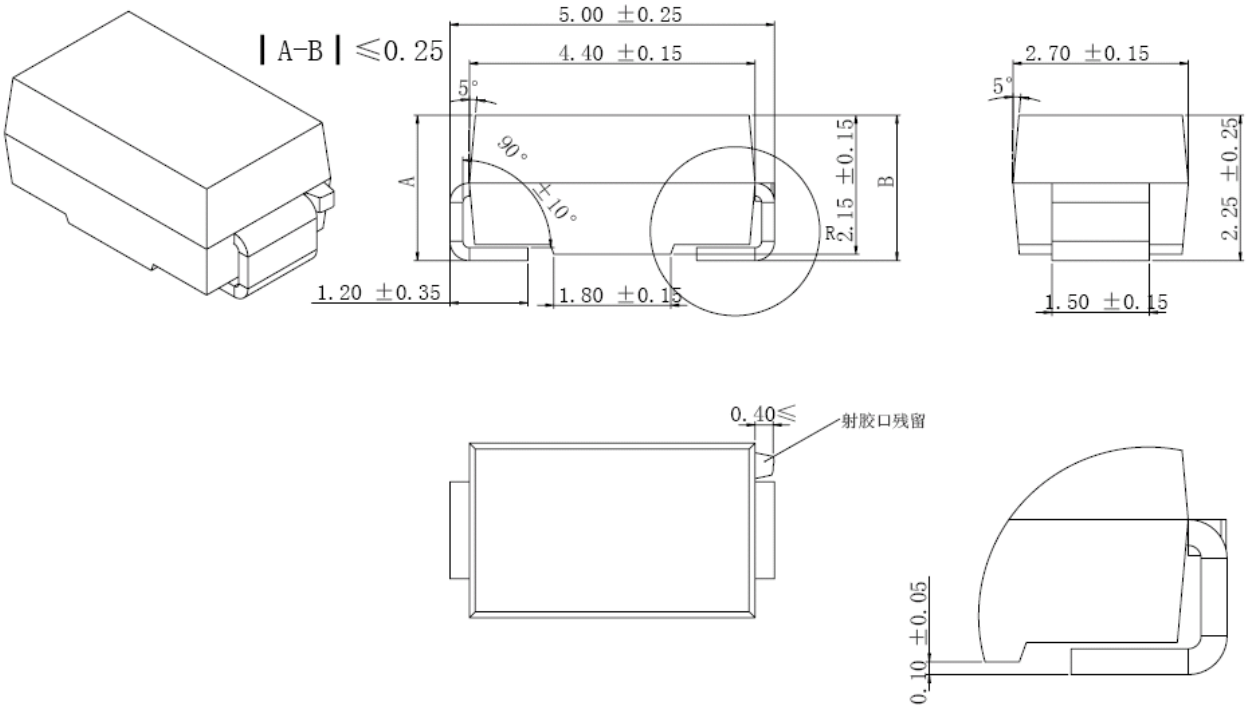


SMA/DO-214AC				
Dim	Min	Max	Min	Max
A	2.50	2.90	0.098	0.114
B	4.00	4.60	0.157	0.181
C	1.40	1.60	0.055	0.063
D	0.152	0.305	0.006	0.012
E	4.80	5.28	0.189	0.208
F	2.00	2.44	0.079	0.096
G	0.051	0.203	0.002	0.008
H	0.76	1.52	0.030	0.060
	In mm		In inch	

OPTION 1

Technical Data
Data Sheet N0942, Rev. A

Green Products



OPTION 2(JK)

SMA

SK220A

Technical Data
Data Sheet N0942, Rev. A

Green Products

Marking Diagram:

Where XXXXX is YYWWL

SK	= Device Type
2	= Forward Current (2A)
20	= Reverse Voltage (200V)
A	= Package type
YY	= Year
WW	= Week
L	= Lot Number

Cautions: Molding resin
Epoxy resin UL:94V-0

Ordering Information:

Device	Package	Shipping
SK220A	SMA (Pb-Free)	5000pcs / reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification.

Maximum Ratings:

Characteristics	Symbol	Condition	Max.	Units
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	-	200	V
Average Rectified Forward Current	$I_{F\ (AV)}$	50% duty cycle @T_L=105℃ rectangular wave form(L=0.375")	2.0	A
Peak One Cycle Non-Repetitive Surge Current	I_{FSM}	8.3 ms, half Sine pulse	50	A

Technical Data
Data Sheet N0942, Rev. A

Green Products

Electrical Characteristics:

Characteristics	Symbol	Condition	Typ.	Max.	Units
Forward Voltage Drop*	V_{F1}	@ 2A, Pulse, T_J = 25℃	0.89	0.9	V
Reverse Current*	I_{R1}	@V_R = rated VR T_J = 25℃	0.05	0.5	mA
	I_{R2}	@V_R = rated VR T_J = 100℃	-	20.0	mA
Typical Junction Capacitance	Cj	@V_R = 5.0 V, Tc=25℃ f_{SIG} = 1MHz	150	170	PF

* Pulse Width < 300µs, Duty Cycle <2%

Thermal-Mechanical Specifications:

Characteristics	Symbol	Condition	Specification	Units
Junction Temperature	T_J	-	-55 to +150	℃
Storage Temperature	T_{stg}	-	-55 to +150	℃
Typical Thermal Resistance Junction to Lead	$R_{\theta JL}$	DC operation	23	℃/W
Typical Thermal Resistance, Case to Heat Sink	$R_{\theta JA}$	DC operation	88	℃/W
Approximate Weight	wt	-	0.11	g
Case Style	SMA			

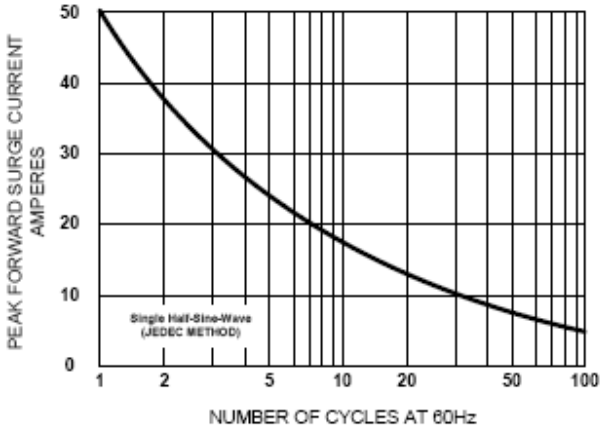


Figure 1. Maximum Non-repetitive Surge Current

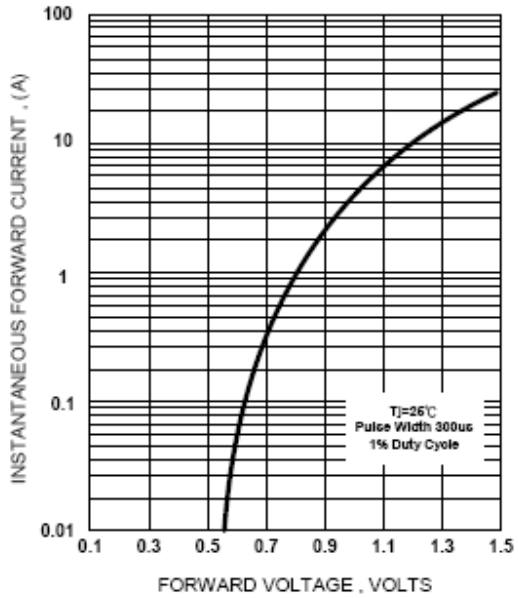


Figure 3. Typical Forward Characteristics

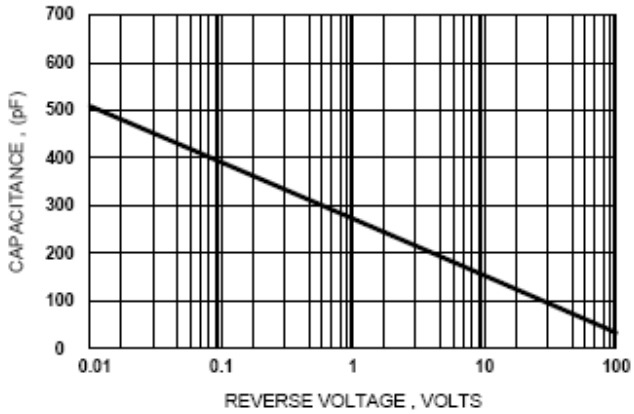


Figure 2. Typical Junction Capacitance

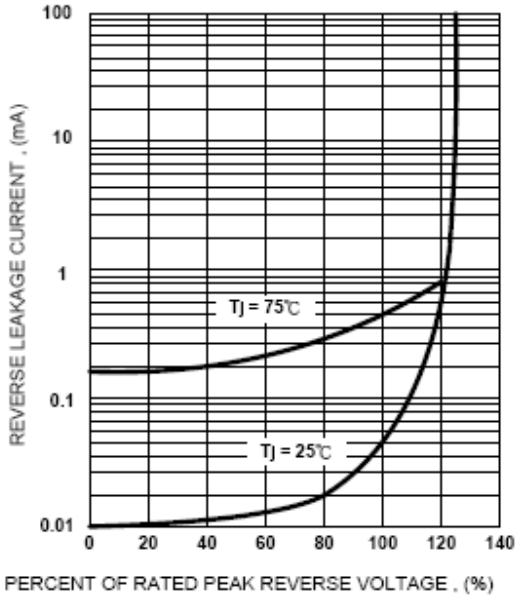


Figure 4. Typical Reverse Characteristics

MBRD835L, SBRD8835L

Switch-mode Power Rectifier

DPAK Surface Mount Package

This switch−mode power rectifier which uses the Schottky Barrier principle with a proprietary barrier metal, is designed for use as output rectifiers, free wheeling, protection and steering diodes in switching power supplies, inverters and other inductive switching circuits.

Features

- Low Forward Voltage
- 150°C Operating Junction Temperature
- Epoxy Meets UL 94 V−0 @ 0.125 in
- Compact Size
- Lead Formed for Surface Mount
- SBRD8 Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Mechanical Characteristics

- Case: Epoxy, Molded
- Weight: 0.4 Gram (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Shipped 75 Units Per Plastic Tube
- ESD Rating:
  - Machine Model = C (> 400 V)
  - Human Body Model = 3B (> 8000 V)

ON Semiconductor®

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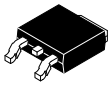
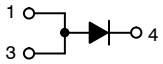
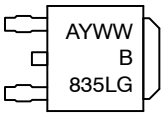
SCHOTTKY BARRIER RECTIFIER
8.0 AMPERES, 35 VOLTS



DPAK
CASE 369C



MARKING DIAGRAM



B835LG	= Specific Device Number
A	= Assembly Location*
Y	= Year
WW	= Work Week
G	= Pb−Free Device

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

ORDERING INFORMATION

Device	Package	Shipping†
MBRD835LG	DPAK (Pb−Free)	75 Units / Rail
SBRD8835LG	DPAK (Pb−Free)	75 Units / Rail
SBRD8835LG−VF01	DPAK (Pb−Free)	75 Units / Rail
MBRD835LT4G	DPAK (Pb−Free)	2,500 / Tape & Reel
SBRD835LT4G−VF01	DPAK (Pb−Free)	2,500 / Tape & Reel
SBRD8835LT4G	DPAK (Pb−Free)	2,500 / Tape & Reel
SBRD8835LT4G−VF01	DPAK (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

June, 2017 − Rev. 12

Publication Order Number:
MBRD835L/D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	35	V
Average Rectified Forward Current (At Rated V_R, T_C = 88°C)	$I_{F(AV)}$	8.0	A
Peak Repetitive Forward Current (At Rated V_R, Square Wave, 20 kHz, T_C = 80°C)	I_{FRM}	16	A
Non−Repetitive Peak Surge Current (Surge applied at rated load conditions, halfwave, single phase, 60 Hz)	I_{FSM}	75	A
Repetitive Avalanche Current (Current Decaying Linearly to Zero in 1 μs, Frequency Limited by T_{Jmax})	I_{AR}	2.0	A
Storage / Operating Case Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature (Note 1)	T_J	−65 to +150	°C
Voltage Rate of Change (Rated V_R)	dv/dt	10,000	V/μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The heat generated must be less than the thermal conductivity from Junction−to−Ambient: $dP_D/dT_J < 1/R_{\theta JA}$.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance − Junction−to−Case	$R_{\theta JC}$	2.8	°C/W
Thermal Resistance − Junction−to−Ambient (Note 2)	$R_{\theta JA}$	80	°C/W

2. Rating applies when surface mounted on the minimum pad size recommended.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum Instantaneous Forward Voltage (Note 3) (i_F = 8 Amps, T_C = +25°C) (i_F = 8 Amps, T_C = +125°C)	V_F	 0.51 0.41	V
Maximum Instantaneous Reverse Current (Note 3) (Rated dc Voltage, T_C = +25°C) (Rated dc Voltage, T_C = +100°C)	I_R	 1.4 35	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

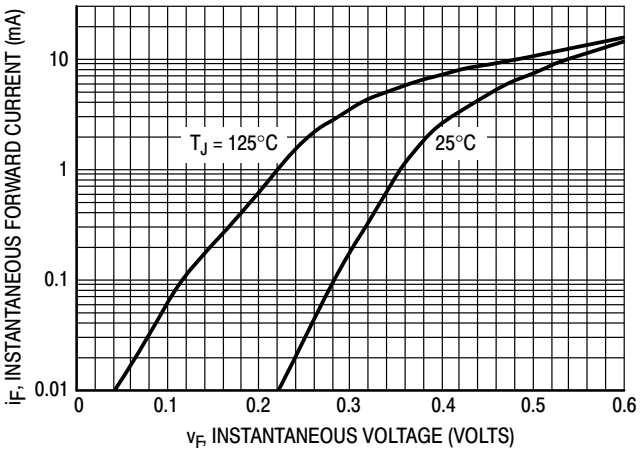


Figure 1. Maximum Forward Voltage

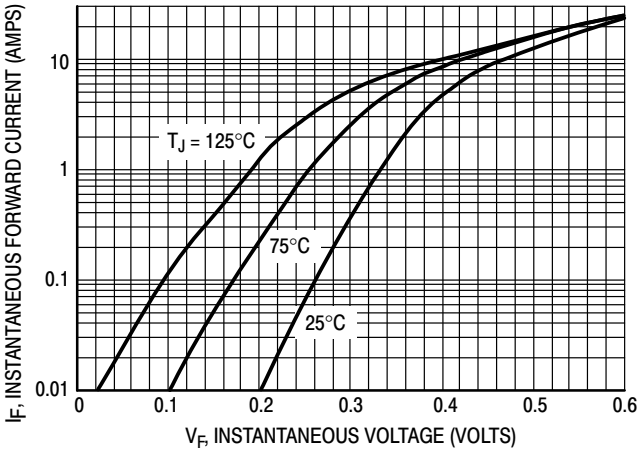


Figure 2. Typical Forward Voltage

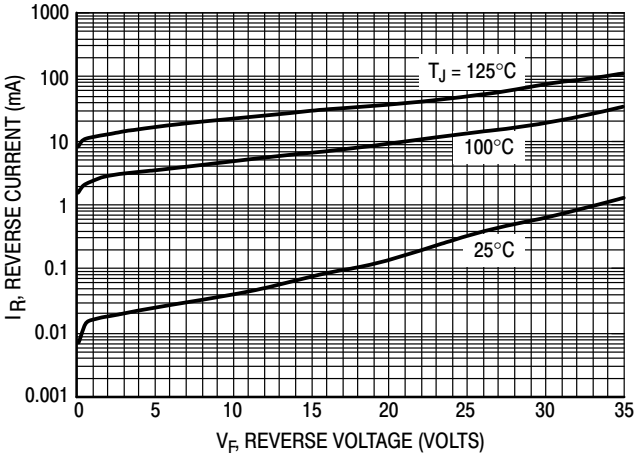


Figure 3. Maximum Reverse Current

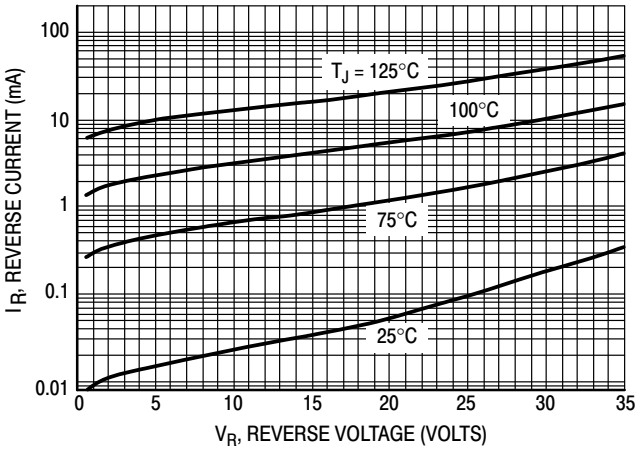


Figure 4. Typical Reverse Current

TYPICAL CHARACTERISTICS

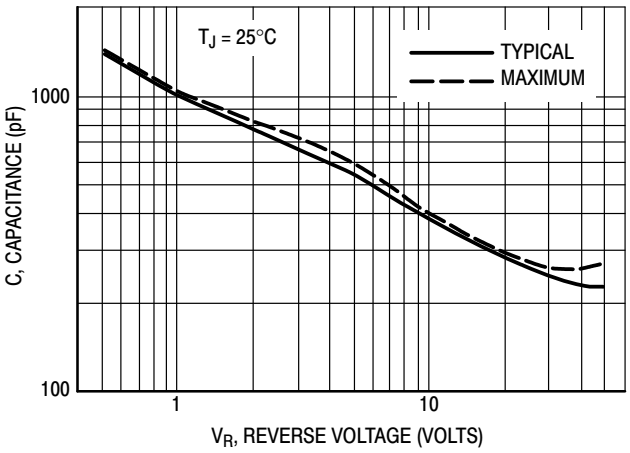


Figure 5. Maximum and Typical Capacitance

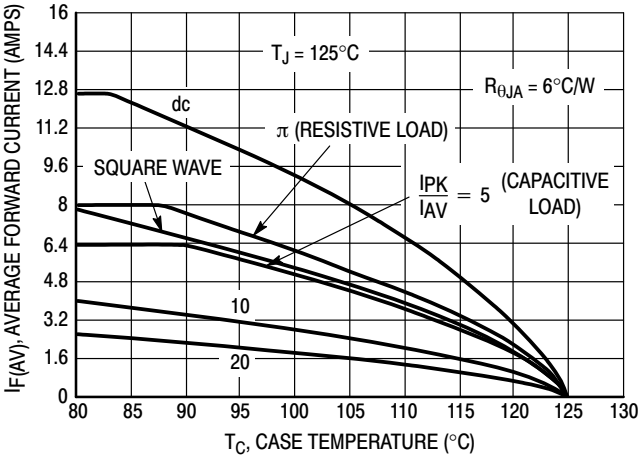


Figure 6. Current Derating, Infinite Heatsink

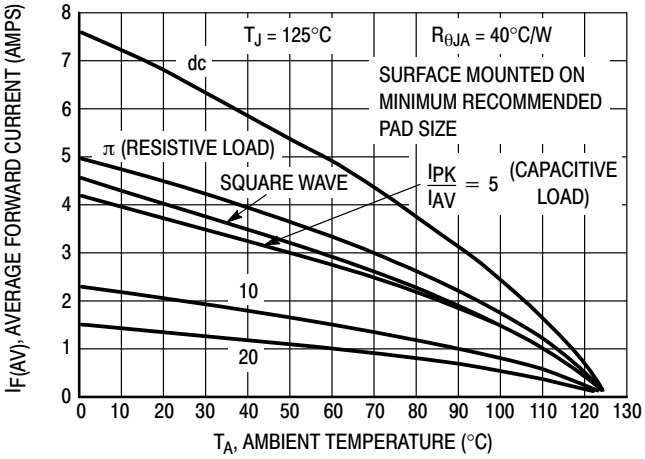


Figure 7. Current Derating

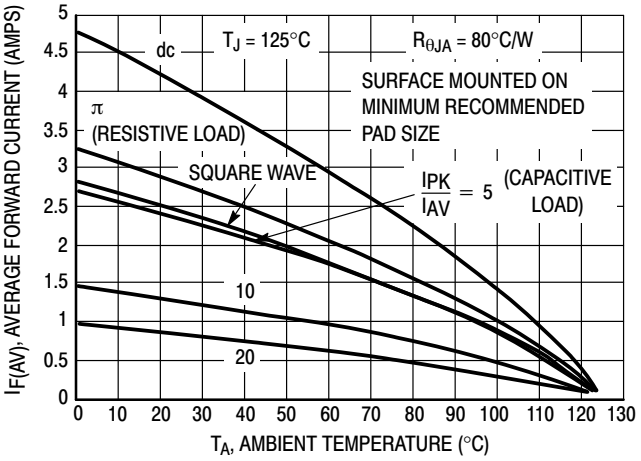


Figure 8. Current Derating, Free Air

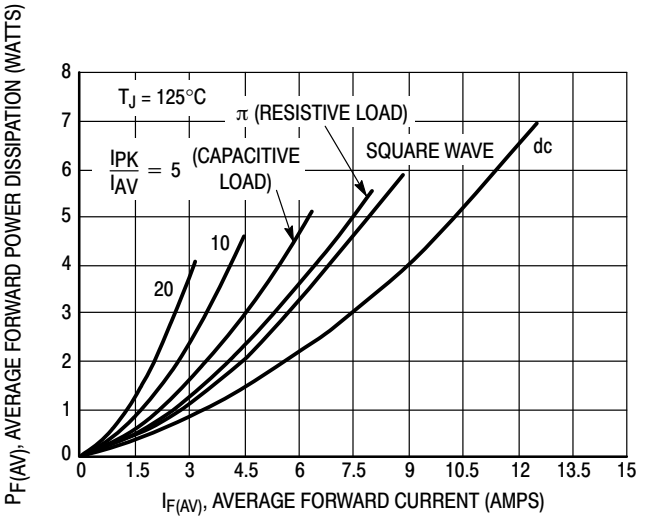
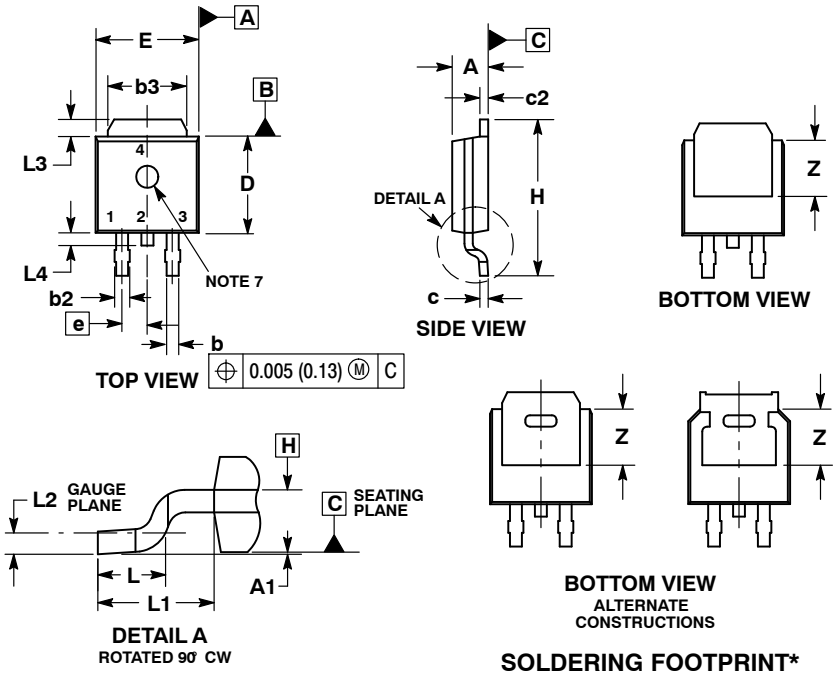


Figure 9. Forward Power Dissipation

PACKAGE DIMENSIONS

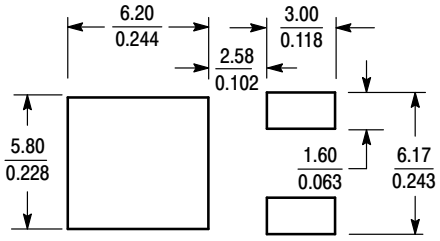
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Kingbright

APG1608ZGCK

1.6 x 0.8 x 0.25 mm (0603) SMD Chip LED Lamp

DESCRIPTIONS

- The Green source color devices are made with InGaN on Sapphire Light Emitting Diode
- Electrostatic discharge and power surge could damage the LEDs
- It is recommended to use a wrist band or anti-electrostatic glove when handling the LEDs
- All devices, equipments and machineries must be electrically grounded

FEATURES

- 1.6 mm x 0.8 mm SMD LED, 0.25 mm thickness
- Low power consumption
- Wide viewing angle
- Compatible with automatic placement equipment
- Ideal for backlight and indicator
- Package: 4000 pcs / reel
- Moisture sensitivity level: 3
- RoHS compliant

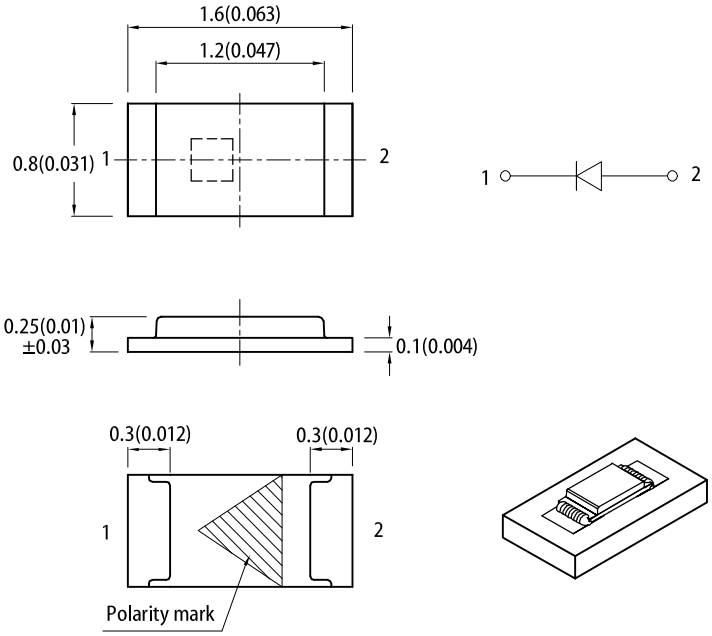
APPLICATIONS

- Backlight
- Status indicator
- Home and smart appliances
- Wearable and portable devices
- Healthcare applications

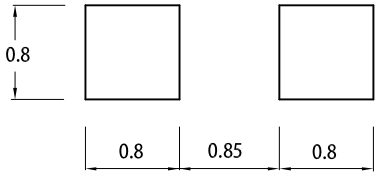
ATTENTION

Observe precautions for handling electrostatic discharge sensitive devices

PACKAGE DIMENSIONS



RECOMMENDED SOLDERING PATTERN
(units : mm; tolerance : ± 0.1)



Mask open area ratio: 80%
Mask thickness: 80~100um

Notes:
1. All dimensions are in millimeters (inches).
2. Tolerance is ±0.1(0.004") unless otherwise noted.
3. The specifications, characteristics and technical data described in the datasheet are subject to change without prior notice.
4. The device has a single mounting surface. The device must be mounted according to the specifications.

SELECTION GUIDE

Part Number	Emitting Color (Material)	Lens Type	Iv (mcd) @ 20mA [2]		Viewing Angle [1]
			Min.	Typ.	2θ1/2
APG1608ZGCK	Green (InGaN)	Water Clear	300	400	130°

Notes:
1. θ1/2 is the angle from optical centerline where the luminous intensity is 1/2 of the optical peak value.
2. Luminous intensity / luminous flux: +/-15%.
3. Luminous intensity value is traceable to CIE127-2007 standards.

ELECTRICAL / OPTICAL CHARACTERISTICS at T_A=25°C

Parameter	Symbol	Emitting Color	Value		Unit
			Typ.	Max.	
Wavelength at Peak Emission I_F = 20mA	λ_{peak}	Green	515	-	nm
Dominant Wavelength I_F = 20mA	λ_{dom} [1]	Green	525	-	nm
Spectral Bandwidth at 50% Φ REL MAX I_F = 20mA	Δλ	Green	35	-	nm
Capacitance	C	Green	45	-	pF
Forward Voltage I_F = 20mA	V_F [2]	Green	3.3	4.1	V
Reverse Current (V_R = 5V)	I_R	Green	-	50	μA
Temperature Coefficient of λ_{peak} I_F = 20mA, -10°C ≤ T ≤ 85°C	$TC_{\lambda peak}$	Green	0.05	-	nm/°C
Temperature Coefficient of λ_{dom} I_F = 20mA, -10°C ≤ T ≤ 85°C	$TC_{\lambda dom}$	Green	0.03	-	nm/°C
Temperature Coefficient of V_F I_F = 20mA, -10°C ≤ T ≤ 85°C	TC_V	Green	-3.0	-	mV/°C

Notes:
1. The dominant wavelength (λd) above is the setup value of the sorting machine. (Tolerance λd : ±1nm.)
2. Forward voltage: ±0.1V.
3. Wavelength value is traceable to CIE127-2007 standards.
4. Excess driving current and / or operating temperature higher than recommended conditions may result in severe light degradation or premature failure.

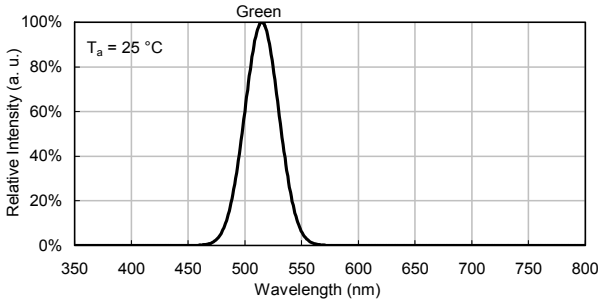
ABSOLUTE MAXIMUM RATINGS at T_A=25°C

Parameter	Symbol	Value	Unit
Power Dissipation	P_D	102.5	mW
Reverse Voltage	V_R	5	V
Junction Temperature	T_j	115	°C
Operating Temperature	T_{op}	-40 to +85	°C
Storage Temperature	T_{stg}	-40 to +85	°C
DC Forward Current	I_F	25	mA
Peak Forward Current	I_{FM} [1]	150	mA
Electrostatic Discharge Threshold (HBM)	-	450	V
Thermal Resistance (Junction / Ambient)	$R_{th\ JA}$ [2]	570	°C/W
Thermal Resistance (Junction / Solder point)	$R_{th\ JS}$ [2]	420	°C/W

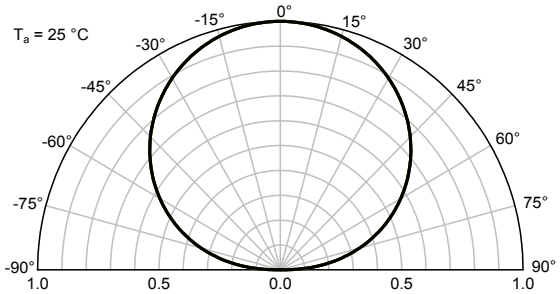
Notes:
1. 1/10 Duty Cycle, 0.1ms Pulse Width.
2. $R_{th\ JA}$,$R_{th\ JS}$ Results from mounting on PC board FR4 (pad size ≥ 16 mm^2 per pad).
3. Relative humidity levels maintained between 40% and 60% in production area are recommended to avoid the build-up of static electricity – Ref JEDEC/JESD625-A and JEDEC/J-STD-033.

TECHNICAL DATA

RELATIVE INTENSITY vs. WAVELENGTH

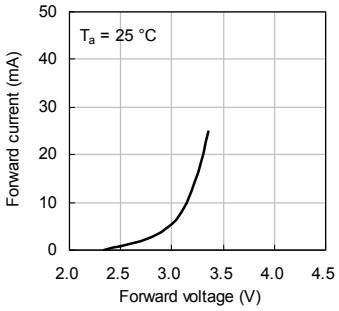


SPATIAL DISTRIBUTION

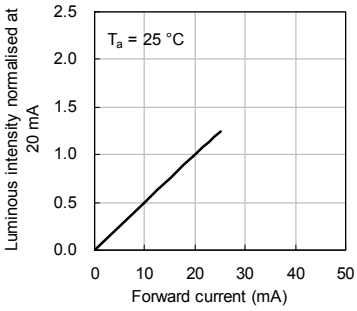


GREEN

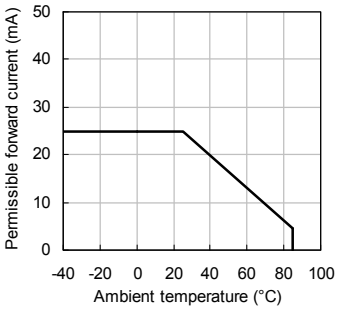
Forward Current vs. Forward Voltage



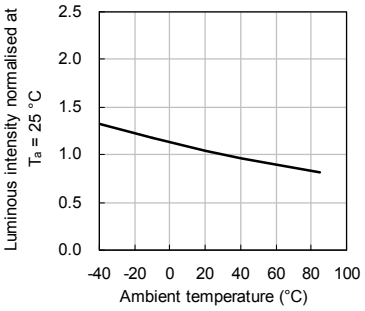
Luminous Intensity vs. Forward Current



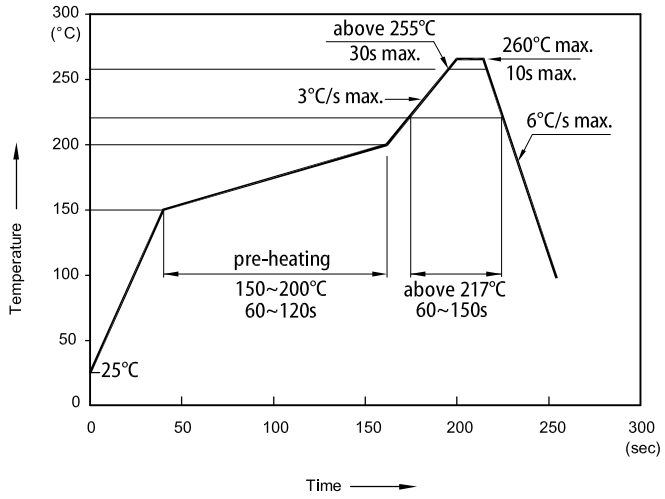
Forward Current Derating Curve



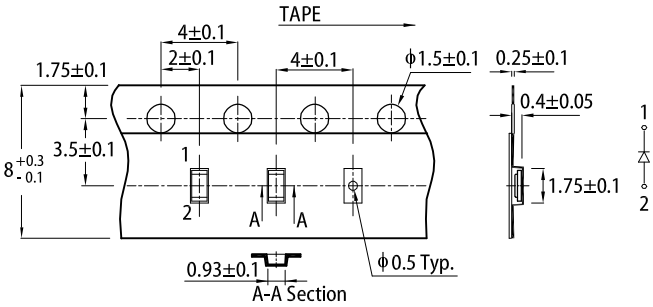
Luminous Intensity vs. Ambient Temperature



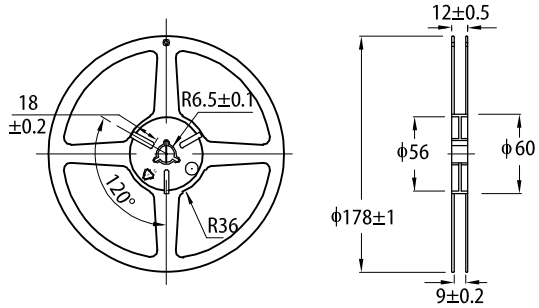
REFLOW SOLDERING PROFILE for LEAD-FREE SMD PROCESS



TAPE SPECIFICATIONS (units : mm)

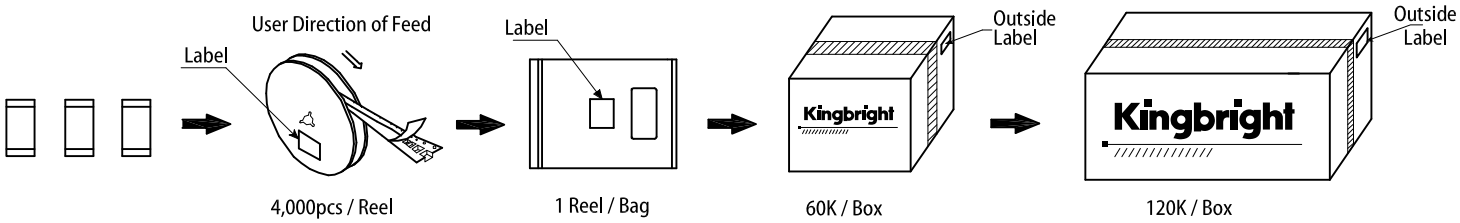


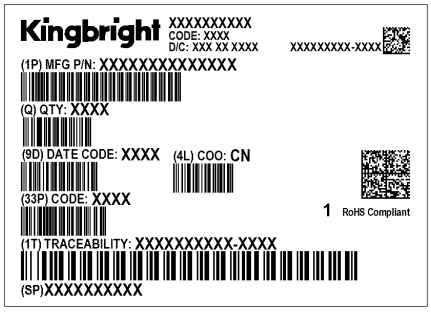
REEL DIMENSION (units : mm)



Notes:
1. Don't cause stress to the LEDs while it is exposed to high temperature.
2. The maximum number of reflow soldering passes is 2 times.
3. Reflow soldering is recommended. Other soldering methods are not recommended as they might cause damage to the product.

PACKING & LABEL SPECIFICATIONS





PRECAUTIONARY NOTES

1. The information included in this document reflects representative usage scenarios and is intended for technical reference only.
2. The part number, type, and specifications mentioned in this document are subject to future change and improvement without notice. Before production usage customer should refer to the latest datasheet for the updated specifications.
3. When using the products referenced in this document, please make sure the product is being operated within the environmental and electrical limits specified in the datasheet. If customer usage exceeds the specified limits, Kingbright will not be responsible for any subsequent issues.
4. The information in this document applies to typical usage in consumer electronics applications. If customer's application has special reliability requirements or have life-threatening liabilities, such as automotive or medical usage, please consult with Kingbright representative for further assistance.
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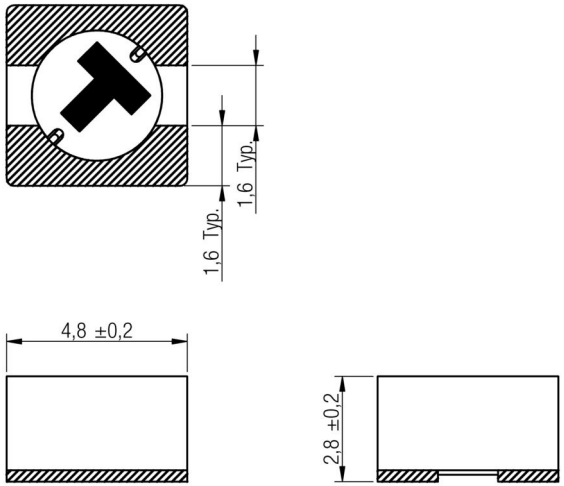
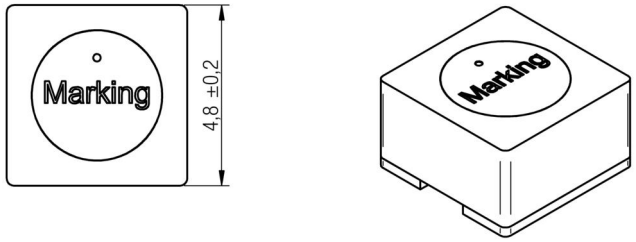
6. All design applications should refer to Kingbright application notes available at https://www.KingbrightUSA.com/ApplicationNotes

A Dimensions: [mm]

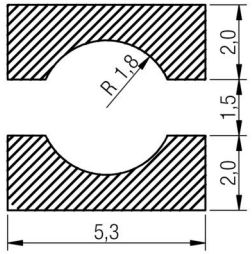




Scale - 5:1

Reference on drawing	Description
•	Start of winding
Marking	471 (Inductance Code)

B Recommended land pattern: [mm]



Scale - 5:1

C Schematic:

D Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 100 mV	L	470	µH	±30%
Rated current	ΔT = 30 K	I_R	0.24	A	max.
Saturation current	|ΔL/L| < 35%	I_{sat}	0.125	A	typ.
DC Resistance	@ 20°C	R_{DC}	2310	mΩ	typ.
DC Resistance	@ 20°C	R_{DC}	2600	mΩ	max.
Self resonant frequency		f_{res}	3	MHz	typ.

E General information:

It is recommended that the temperature of the part does not exceed 125°C under worst case operating conditions.

- Ambient temperature: -40°C to +95°C (refering to I_R)
- Operating temperature: -40°C to +125°C
- Storage temperature (on tape & reel): -20°C to +40°C; 75% RH max.
- Test conditions of Electrical Properties: 20°C, 33% RH if not specified differently

REV	DATE	BY	CHECKED
6.4	2015-01-29	SSt	JRS
6.3	2014-09-11	SSt	JRS
6.2	2014-04-01	SSt	SSt
6.1	2013-04-08	SSt	COt
6.0	2010-08-01	CZ	-

Projection

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Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WE-TPC SMD Shielded Tiny Power Inductor

Order.- No.

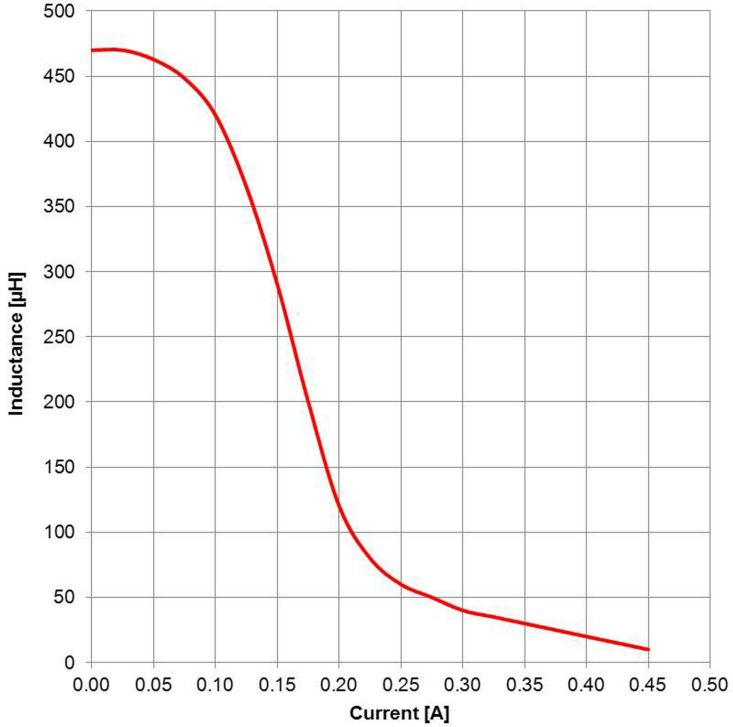
744043471

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 4828

F1 Typical Inductance vs. Current Characteristics:



REV	DATE	BY	CHECKED
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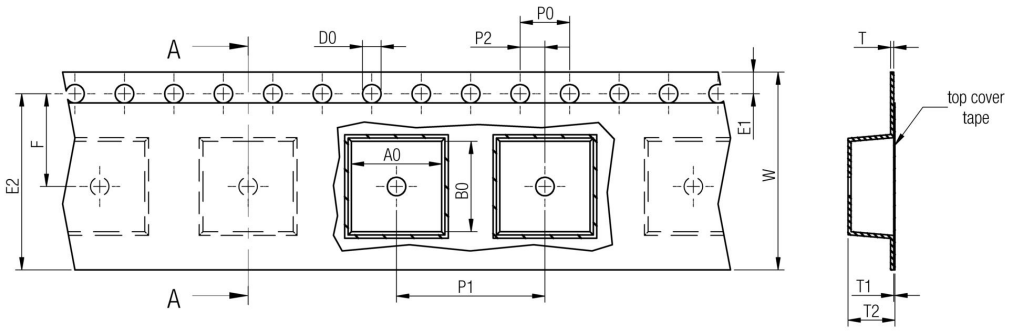
SIZE

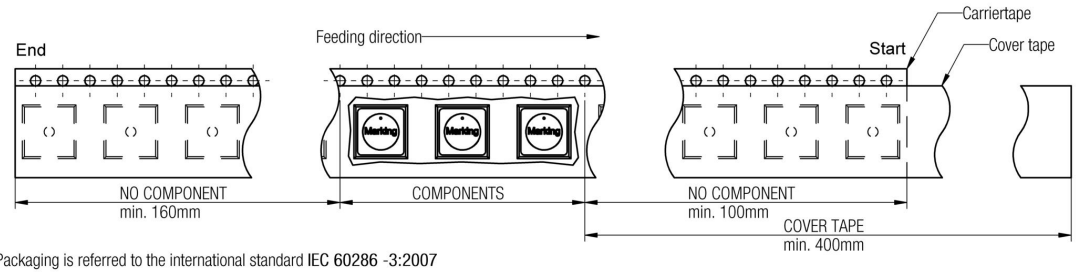
A4

Size: 4828

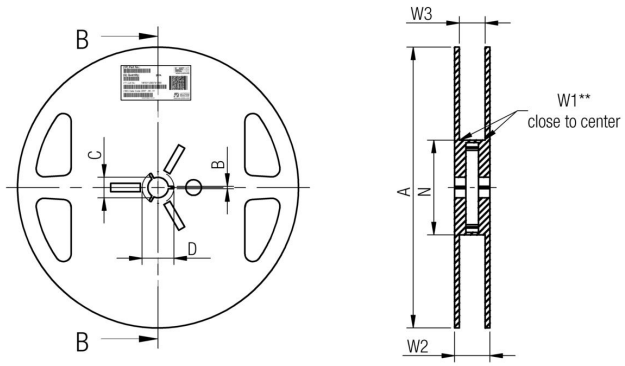
G Packaging Specification - Tape and Reel [mm]:



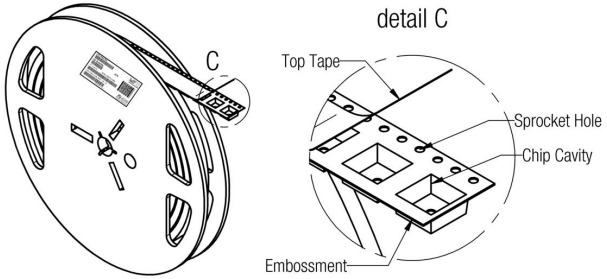
		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	+0,3 -0,1	± 0,1	± 0,1	max.	typ.	+0,1 -0,0	± 0,1	min.	± 0,05	± 0,1	± 0,05		
size	**3816**	4,30	4,30	12,00	8,00	0,25	0,10	2,00	1,50	1,75	10,25	5,50	4,00	2,00	Polystyrene	1000
	4818	5,30	5,30	12,00	8,00	0,25	0,10	2,50	1,50	1,75	10,25	5,50	4,00	2,00	Polystyrene	800
	4828	5,30	5,30	12,00	8,00	0,25	0,10	3,00	1,50	1,75	10,25	5,50	4,00	2,00	Polystyrene	500
	5818	6,30	6,30	16,00	12,00	0,25	0,10	2,50	1,50	1,75	14,25	7,50	4,00	2,00	Polystyrene	500
	5828	6,30	6,30	16,00	12,00	0,25	0,10	3,00	1,50	1,75	14,25	7,50	4,00	2,00	Polystyrene	400
	6823	7,30	7,30	16,00	12,00	0,25	0,10	3,00	1,50	1,75	14,25	7,50	4,00	2,00	Polystyrene	500

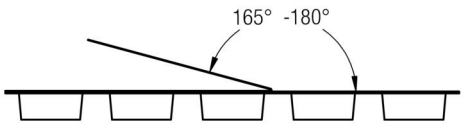


Packaging is referred to the international standard IEC 60286 -3:2007



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	min.	+ 1,5	max.	min.	max.
Tape width	**12 mm**	178,00	1,50	13,00	20,20	50,00	12,40	18,40	11,90	15,40
	16 mm	178,00	1,50	13,00	20,20	50,00	16,40	22,40	15,90	19,40





		Pull-of force
Tape width	**12 mm**	0,1 N - 1,0 N
	16 mm	0,1 N - 1,3 N

REV	DATE	BY	CHECKED
6.4	2015-01-29	SSt	JRS
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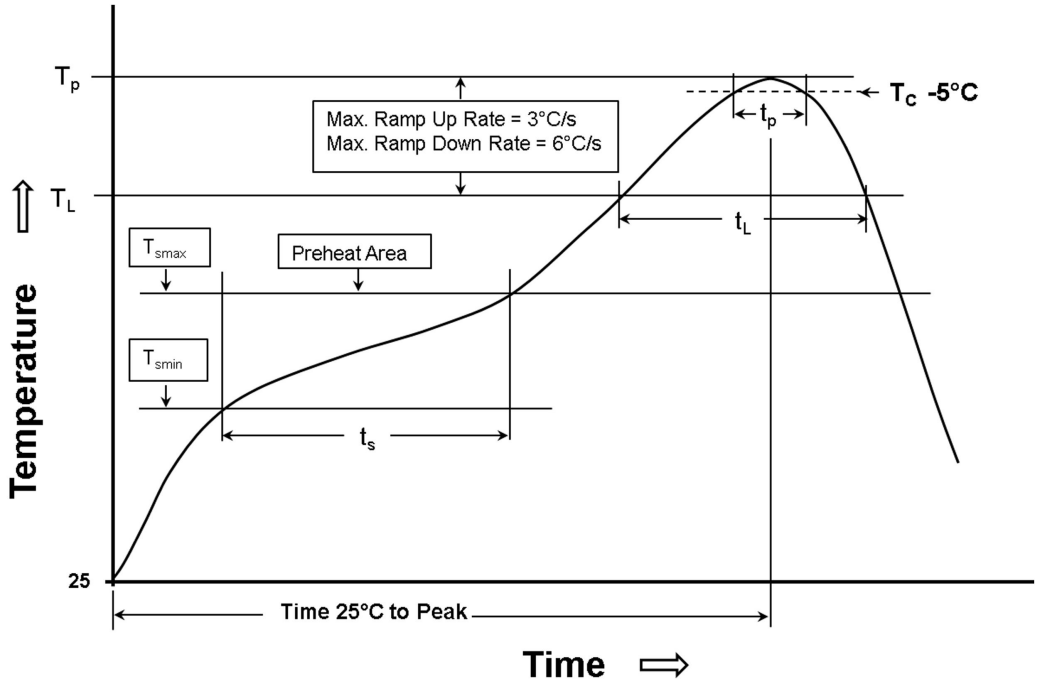
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 4828

H Soldering Specifications:

H1: Classification Reflow Profile for SMT components:



H2: Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/ second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_p)	See Table H3
Time within 5°C of actual peak temperature (t_p)	20-30 seconds, except T_p 260°C at t_p 10 seconds
Ramp-down rate (T_P to T_L)	6°C/ second max.
Time 25°C to peak temperature	8 minutes max.

refer to IPC/JEDEC J-STD-020D

H3: Package Classification Reflow Temperature

	Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
PB-Free Assembly	< 1.6 mm	260°C	260°C	260°C
PB-Free Assembly	1.6 - 2.5 mm	260°C	250°C	245°C
PB-Free Assembly	≥ 2.5 mm	250°C	245°C	245°C

refer to IPC/JEDEC J-STD-020D

REV	DATE	BY	CHECKED
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COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 4828

HIGH CURRENT SHIELDED SMD POWER INDUCTORAIG

ASPIAIG-F SERIES

Dimensions vary

MSL = 1

RoHS/RoHS II Compliant

SERIES DESCRIPTION

The ASPIAIG-F series of molded smd power inductors come in a variety of package sizes. The series supports current handling up to 36A and DCR of only 1.75mΩ. This series is perfect for DC/DC converters in distributed power systems, DC/DC converters for FPGAs, voltage regulator module for servers, and high current, low profile POL converters.

FEATURES

- PPAP ready and supported
- TS16949 production certified lines
- AEC-Q200 qualified
- Excellent current handling – up to 36A
- Exceptionally low DCR – only 1.75 mΩ
- Soft saturation
- Low profile for compact design
- Shielded construction reduces EMI

APPLICATIONS

- Automotive grade 1 and electric vehicles
- ADAS and body electronics
- Infotainment systems
- Lighting
- Motor control
- Solar inverters and solar power
- DC/DC converters in distributed power systems
- DC/DC converters for FPGA (Field Programmable Gate Array)
- Battery powered device
- Thin type on-board power supply module for exchangers
- VRM (Voltage Regulator Module) for server
- High current, low profile POL (Point of Load) converters
- Graphics card (Buck converters)

OPTIONS AND PART IDENTIFICATION

ASPIAIG-F [ ] - [ ] [ ] - [ ]

SERIES #
4020
LR4020
5020
5030
6030
6050
7020
7030

INDUCTANCE CODE
Please refer to Electrical Spec Table

TOLERANCE
M: ±20%

SERIES #	PACKAGING (T = TAPE AND REEL)
4020	T: 3k pcs / reel
LR4020	T: 3k pcs / reel
5020	T: 3k pcs /reel
5030	T: 1k pcs /reel
6030	T: 1k pcs /reel
6050	T: 800 pcs /reel
7020	T: 2k pcs/reel
7030	T: 1.5k pcs/reel

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HIGH CURRENT SHIELDED SMD POWER INDUCTORAIG

ASPIAIG-F SERIES

Dimensions vary

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RoHS/RoHS II Compliant

ELECTRICAL SPECIFICATIONS

OPERATING TEMPERATURE	STORAGE CONDITION
-40°C - 125°C (including self-temperature rise)	-10°C - +40°C and R.H. 60%max

PART NUMBER	INDUCTANCE	TOLERANCE	DC RESISTANCE	SATURATION CURRENT	TEMPERATURE RISE CURRENT
	0.1MHz/0.1V		MAX	MAX	MAX
UNITS	µH	%	mΩ	A	A
SYMBOL	L	M	DCR	Isat	Irms
ASPIAIG-F4020-R10	0.10	20%	2.42	33.0	18.0
ASPIAIG-F4020-R22	0.22	20%	4.60	18.8	16.8
ASPIAIG-F4020-R36	0.36	20%	6.30	15.0	14.5
ASPIAIG-F4020-R40	0.40	20%	7.73	13.5	14.0
ASPIAIG-F4020-R56	0.56	20%	9.30	12.6	12.0
ASPIAIG-F4020-R60	0.60	20%	9.52	12.3	11.7
ASPIAIG-F4020-R72	0.72	20%	11.60	10.6	10.5
ASPIAIG-F4020-1R0	1.00	20%	14.60	8.8	9.6
ASPIAIG-F4020-1R2	1.20	20%	17.90	7.8	9.0
ASPIAIG-F4020-1R5	1.50	20%	23.50	7.4	7.6
ASPIAIG-F4020-1R8	1.80	20%	28.00	7.0	7.0
ASPIAIG-F4020-2R2	2.20	20%	38.70	6.0	5.6
ASPIAIG-FLR4020-R47	0.47	20%	6.8	12.5	13.2
ASPIAIG-FLR4020-R68	0.68	20%	8.2	10.0	12.0
ASPIAIG-FLR4020-R82	0.82	20%	9.5	9.0	11.5
ASPIAIG-FLR4020-1R0	1.00	20%	11.7	8.0	11.0
ASPIAIG-FLR4020-1R2	1.20	20%	13.4	7.5	9.5
ASPIAIG-FLR4020-1R5	1.50	20%	15.8	6.7	9.1
ASPIAIG-FLR4020-2R0	2.00	20%	23.3	5.0	8.2
ASPIAIG-FLR4020-2R2	2.20	20%	23.5	4.8	8.0
ASPIAIG-FLR4020-3R3	3.30	20%	38.3	4.4	5.5
ASPIAIG-FLR4020-4R7	4.70	20%	57.2	3.5	5.1
ASPIAIG-F5020-R15	0.15	20%	4.60	27.0	18.8
ASPIAIG-F5020-R16	0.16	20%	4.60	27.0	18.8
ASPIAIG-F5020-R33	0.33	20%	7.00	24.0	14.4
ASPIAIG-F5020-R47	0.47	20%	8.05	20.0	14.1
ASPIAIG-F5020-R56	0.56	20%	9.54	16.0	13.9
ASPIAIG-F5020-R68	0.68	20%	10.2	14.0	13.4
ASPIAIG-F5020-R80	0.80	20%	11.8	13.5	13.0
ASPIAIG-F5020-R82	0.82	20%	12.7	13.0	12.0
ASPIAIG-F5020-1R0	1.00	20%	13.8	12.8	10.5
ASPIAIG-F5020-1R2	1.20	20%	16.3	12.2	9.40
ASPIAIG-F5020-1R5	1.50	20%	18.7	11.7	8.80

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HIGH CURRENT SHIELDED SMD POWER INDUCTORAIG

ASPIAIG-F SERIES

Dimensions vary

MSL = 1

RoHS/RoHS II Compliant

ELECTRICAL SPECIFICATIONS

PART NUMBER	INDUCTANCE	TOLERANCE	DC RESISTANCE	SATURATION CURRENT	TEMPERATURE RISE CURRENT
	0.1MHz/0.1V		MAX	MAX	MAX
UNITS	µH	%	mΩ	A	A
SYMBOL	L	M	DCR	Isat	Irms
ASPIAIG-F5030-R15	0.15	20%	2.31	32.5	22.2
ASPIAIG-F5030-R16	0.16	20%	2.33	32.0	22.2
ASPIAIG-F5030-R33	0.33	20%	3.52	26.0	19.2
ASPIAIG-F5030-R56	0.56	20%	4.52	20.2	17.7
ASPIAIG-F5030-R60	0.60	20%	4.52	20.0	17.7
ASPIAIG-F5030-R80	0.80	20%	5.65	18.0	13.1
ASPIAIG-F5030-R82	0.82	20%	5.78	17.6	12.9
ASPIAIG-F5030-1R0	1.00	20%	7.60	14.3	12.2
ASPIAIG-F5030-1R2	1.20	20%	9.70	13.5	11.0
ASPIAIG-F5030-1R5	1.50	20%	11.2	12.5	10.5
ASPIAIG-F5030-1R8	1.80	20%	12.7	11.3	10.1
ASPIAIG-F5030-2R2	2.20	20%	14.5	9.0	9.70
ASPIAIG-F5030-3R3	3.30	20%	23.1	8.7	8.10
ASPIAIG-F5030-4R7	4.70	20%	36.3	7.0	5.90
ASPIAIG-F6050-1R0	1.00	20%	4.52	18.0	20.0
ASPIAIG-F6050-1R2	1.20	20%	5.83	16.0	18.0
ASPIAIG-F6050-1R5	1.50	20%	6.3	14.5	17.0
ASPIAIG-F6050-1R8	1.80	20%	7.1	13.5	16.0
ASPIAIG-F6050-2R2	2.20	20%	8.5	12.0	13.0
ASPIAIG-F6050-3R3	3.30	20%	12.5	10.0	11.0
ASPIAIG-F6050-4R3	4.30	20%	16.2	8.5	9.0
ASPIAIG-F6050-4R7	4.70	20%	18.4	8.0	8.5

PART NUMBER	INDUCTANCE	TOLERANCE	SELF-RESONANT FREQUENCY	DC RESISTANCE	SATURATION CURRENT	TEMPERATURE RISE CURRENT
	0.1MHz/0.1V		REF	MAX	MAX	MAX
UNITS	µH	%	MHz	mΩ	A	A
SYMBOL	L	M	SRF	DCR	Isat	Irms
ASPIAIG-F6030-R18	0.18	20%	143	1.75	36.0	32.0
ASPIAIG-F6030-R33	0.33	20%	78	2.50	28.0	25.0
ASPIAIG-F6030-R56	0.56	20%	70	3.31	25.0	22.0
ASPIAIG-F6030-1R0	1.00	20%	52	6.05	18.0	18.0
ASPIAIG-F6030-1R2	1.20	20%	47	7.40	16.0	16.0
ASPIAIG-F6030-1R8	1.80	20%	33	10.2	13.0	14.0
ASPIAIG-F6030-2R2	2.20	20%	29	12.2	11.0	10.0
ASPIAIG-F6030-3R3	3.30	20%	25	20.8	9.00	8.00
ASPIAIG-F6030-4R5	4.50	20%	20	25.3	8.00	7.00

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Dimensions vary

MSL = 1

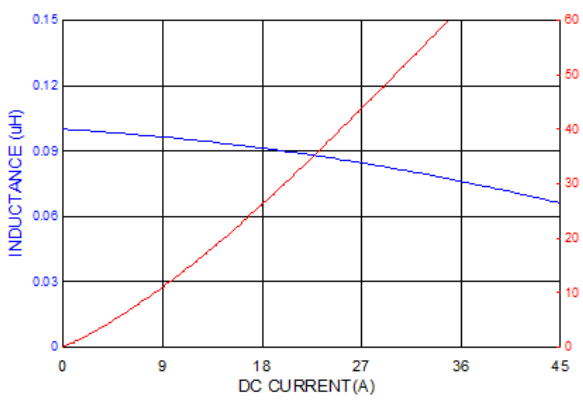
RoHS/RoHS II Compliant

ELECTRICAL SPECIFICATIONS

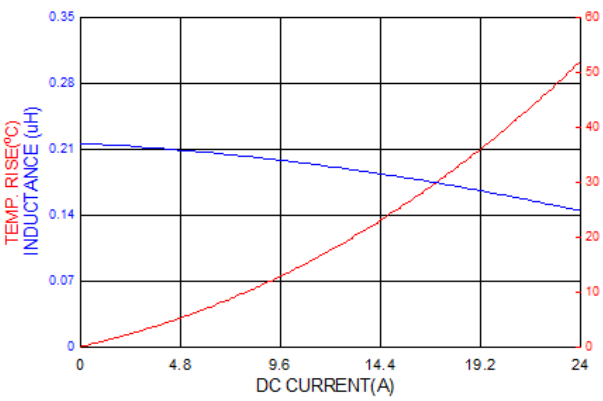
PART NUMBER	INDUCTANCE	TOLERANCE	DC RESISTANCE	SATURATION CURRENT	TEMPERATURE RISE CURRENT	D
	0.1MHz/0.1V		MAX	MAX	MAX	±0.3
UNITS	µH	%	mΩ	A	A	mm
SYMBOL	L	M	DCR	Isat	Irms	
ASPIAIG-F7020-R27	0.27	20%	3.5	32.0	21.0	6.6
ASPIAIG-F7020-R31	0.31	20%	4.8	31.0	20.0	6.2
ASPIAIG-F7020-R33	0.33	20%	4.8	31.0	19.0	6.2
ASPIAIG-F7020-R47	0.47	20%	6.2	25.0	17.0	6.2
ASPIAIG-F7020-R68	0.68	20%	9.2	23.0	13.0	6.2
ASPIAIG-F7020-1R0	1.00	20%	10.8	20.0	11.0	6.2
ASPIAIG-F7030-R60	0.60	20%	3.2	32.0	23.0	6.6
ASPIAIG-F7030-1R0	1.00	20%	5.0	28.0	21.8	6.6
ASPIAIG-F7030-1R5	1.50	20%	8.25	23.5	15.3	6.6
ASPIAIG-F7030-2R2	2.20	20%	13.7	17.0	13.0	6.2
ASPIAIG-F7030-3R3	3.30	20%	18.0	13.0	10.0	6.2
ASPIAIG-F7030-4R7	4.70	20%	26.7	12.2	9.0	6.2
ASPIAIG-F7030-5R6	5.60	20%	33.2	11.5	7.3	6.2
ASPIAIG-F7030-6R8	6.80	20%	42.5	11.0	6.8	6.2
ASPIAIG-F7030-8R2	8.20	20%	48.73	9.0	5.9	6.2

ELECTRICAL CHARACTERISTICS

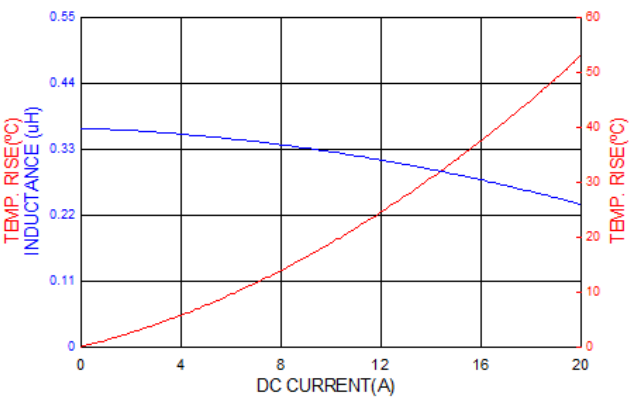
ASPIAIG-F4020-R10



ASPIAIG-F4020-R22



ASPIAIG-F4020-R36



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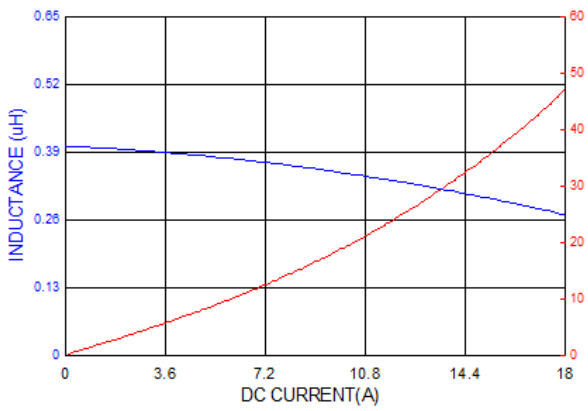

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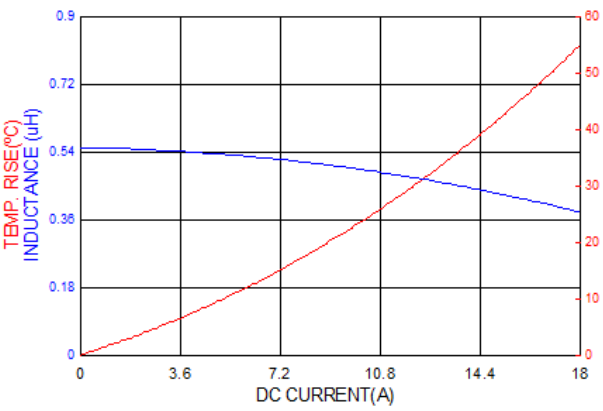

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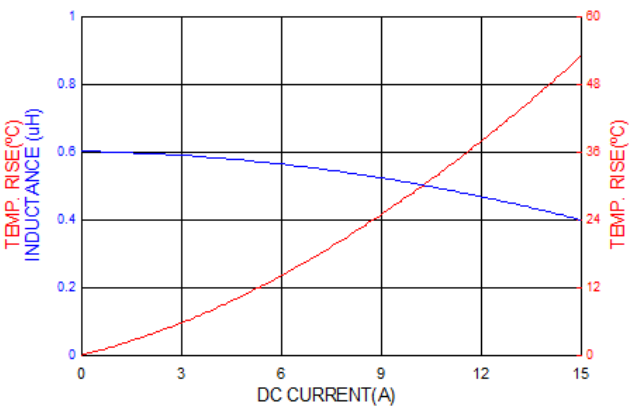


REVISED: 11.07.2017

ABRACON LLC
The Power of Linking Together

1501 Hidden Creek Lane Spicewood TX 78751
Phone: 512-371-6159 | Fax: 512-351-8858
For terms and conditions of sales visit:
www.abracon.com

ABRACON IS ISO9001-2008 CERTIFIED

HIGH CURRENT SHIELDED SMD POWER INDUCTORAIG

ASPIAIG-F SERIES

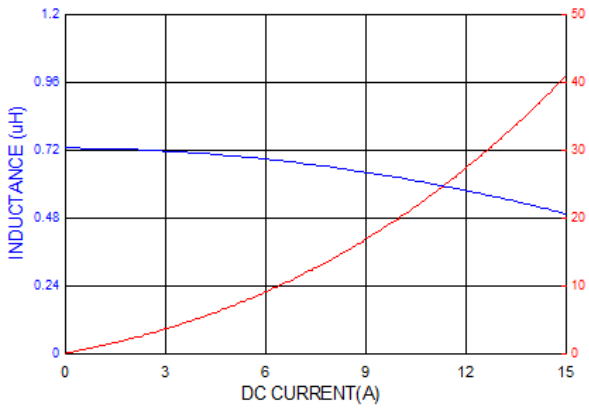
Dimensions vary

MSL = 1

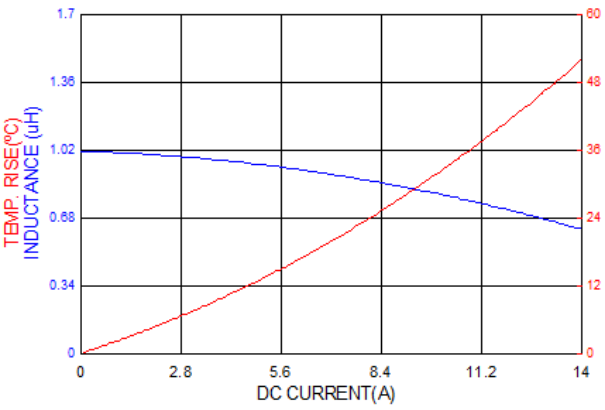
RoHS/RoHS II Compliant

ELECTRICAL SPECIFICATIONS

ASPIAIG-F4020-R72



ASPIAIG-F4020-1R0



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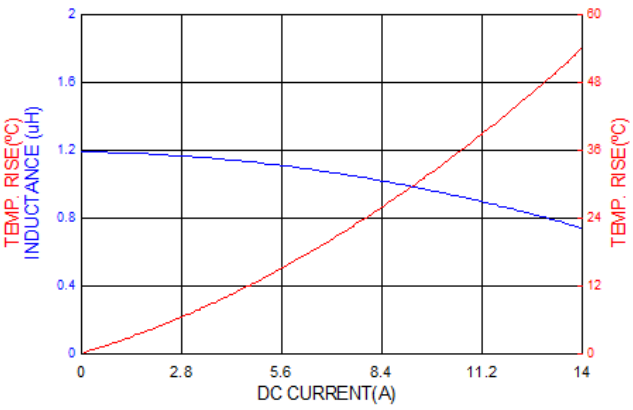

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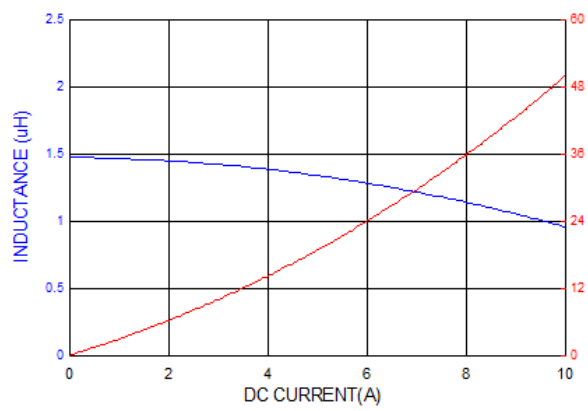

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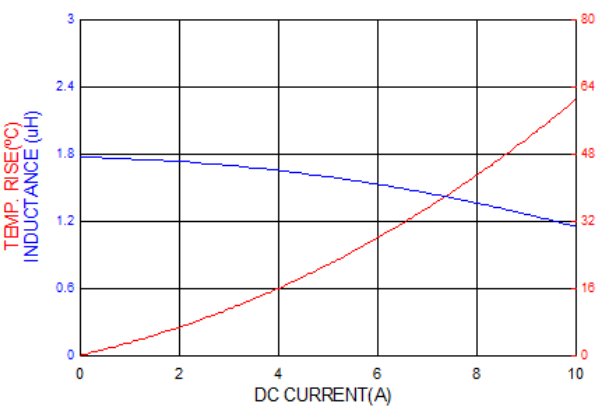

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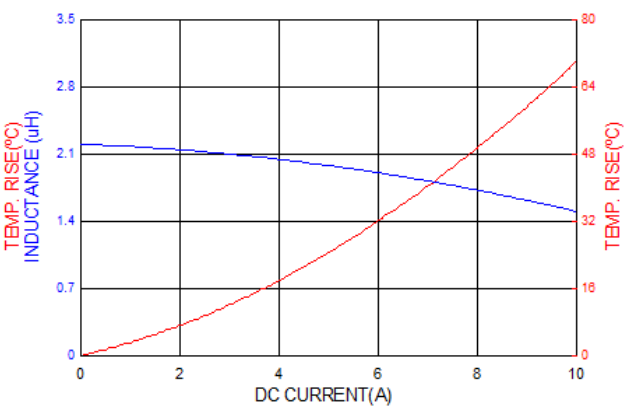

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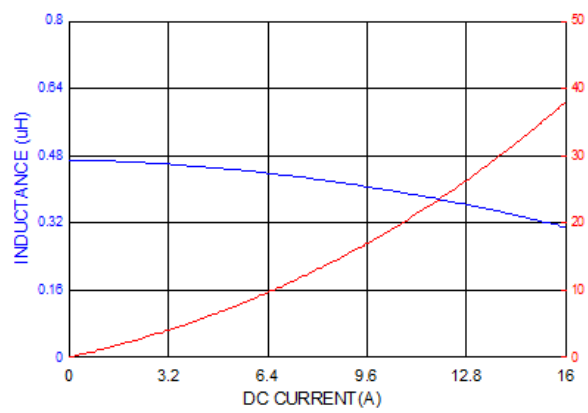

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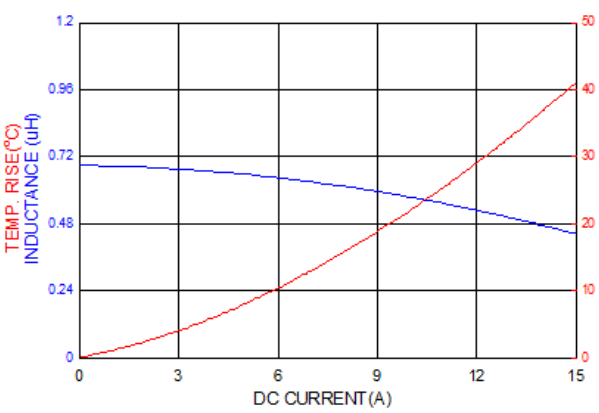

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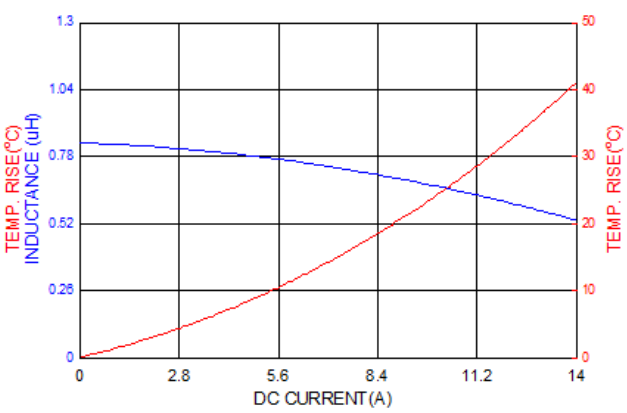
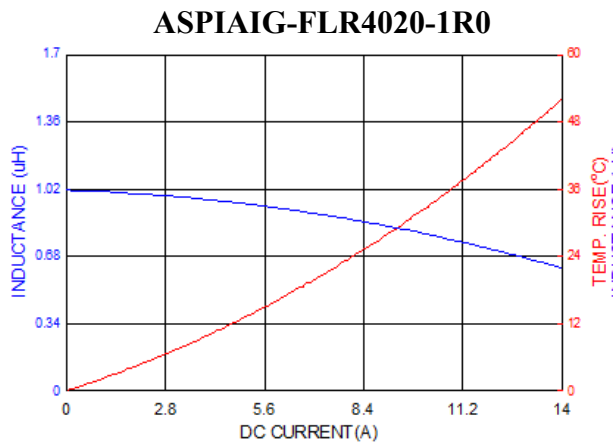
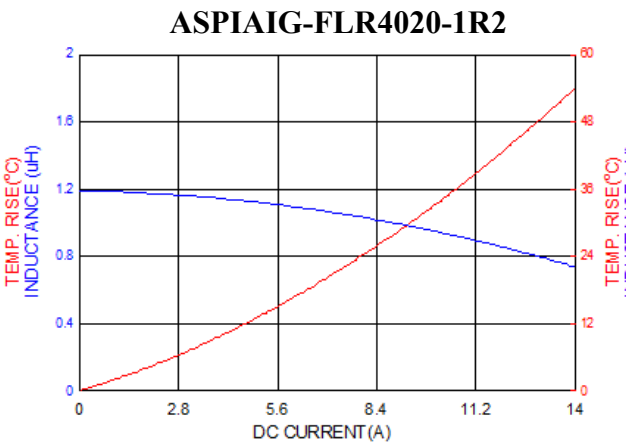


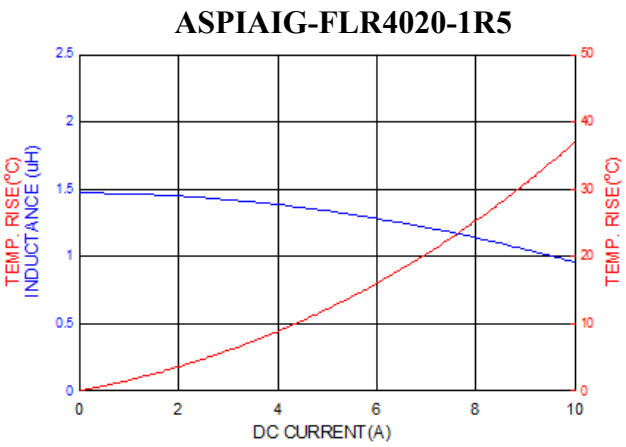
ASPIAIG-FLR4020-1R0



ASPIAIG-FLR4020-1R2



ASPIAIG-FLR4020-1R5



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REVISED: 11.07.2017

ABRACON IS
ISO9001-2008
CERTIFIED

Inductor Data Sheet

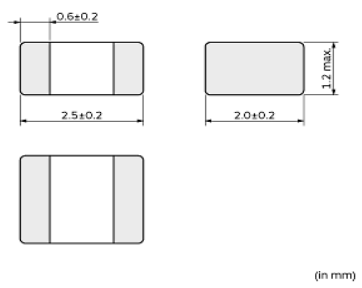
DFE252012P-1R0M#

"#" indicates a package specification code.

In Production | General | 125 ℃max. | Wound (Metal) | Reflow OK | RoHS | REACH

< List of part numbers with package codes >
DFE252012P-1R0M=P2

Shape



L size	2.5 ±0.2mm
W size	2.0 ±0.2mm
T size	1.2 mm
Size code in inch (mm)	1008 (2520)

Notes

Rated current (Isat) is specified when the decrease of the initial inductance value at 30%. (The ambient reference temperature is 20℃.)
Rated current (Itemp) is specified when temperature of inductor the is raised 40℃ by DC current. (The ambient reference temperature is 20℃.)

References

Packaging code	Specifications	Minimum quantity
=P2	ϕ180mm Embossed taping	3000

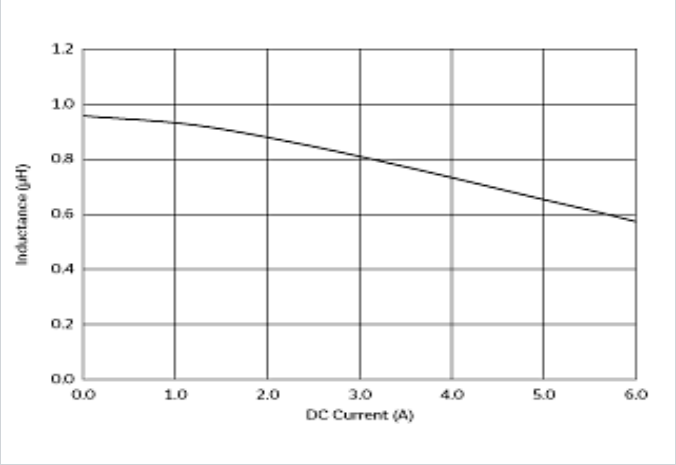
Mass (Typ.)	
1 piece	0.02835g

Specifications

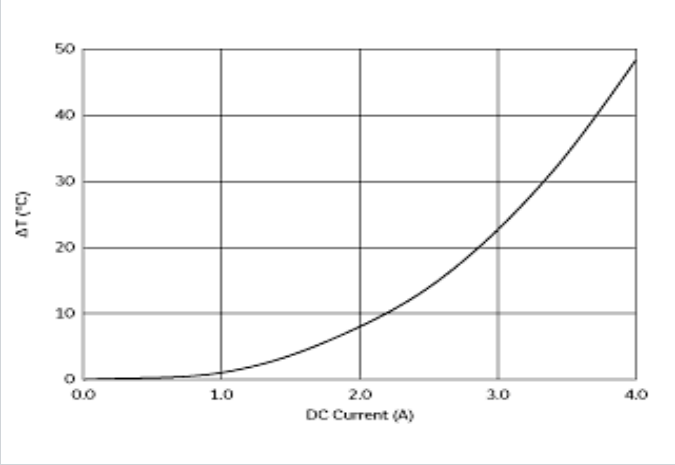
Inductance	1.0µH ±20%
Inductance test frequency	1MHz
Rated current (Isat) (Based on Inductance change)	4300mA
Rated current (Itemp) (Based on Temperature rise)	3200mA
Max. of DC resistance	0.042Ω
Operating temperature range (Self-temperature rise is included)	-40～125℃
Class of magnetic shield	Metal Alloy
Absolute maximum voltage	20V DC
Series	DFE252012P

Chart of characteristic data (The charts below may show another part number which shares its characteristics.)

- Inductance-Current characteristics (Typ.)



- Temperature rise characteristics (Typ.)



Inductor Data Sheet

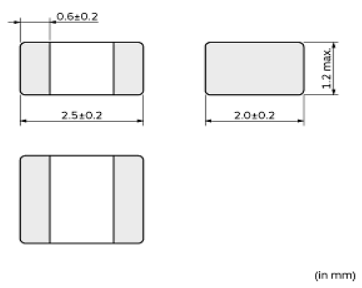
DFE252012P-1R5M#

"#" indicates a package specification code.

In Production | General | 125 ℃max. | Wound (Metal) | Reflow OK | RoHS | REACH

< List of part numbers with package codes >
DFE252012P-1R5M=P2

Shape



L size	2.5 ±0.2mm
W size	2.0 ±0.2mm
T size	1.2 mm
Size code in inch (mm)	1008 (2520)

Notes

Rated current (Isat) is specified when the decrease of the initial inductance value at 30%. (The ambient reference temperature is 20℃.)
Rated current (Itemp) is specified when temperature of inductor the is raised 40℃ by DC current. (The ambient reference temperature is 20℃.)

References

Packaging code	Specifications	Minimum quantity
=P2	ϕ180mm Embossed taping	3000

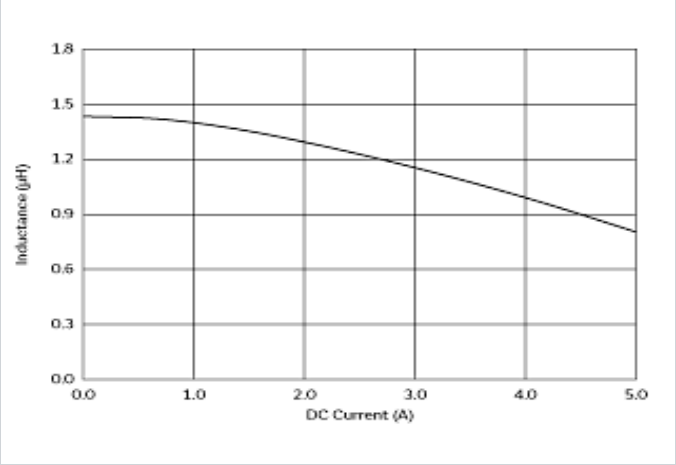
Mass (Typ.)	
1 piece	0.02835g

Specifications

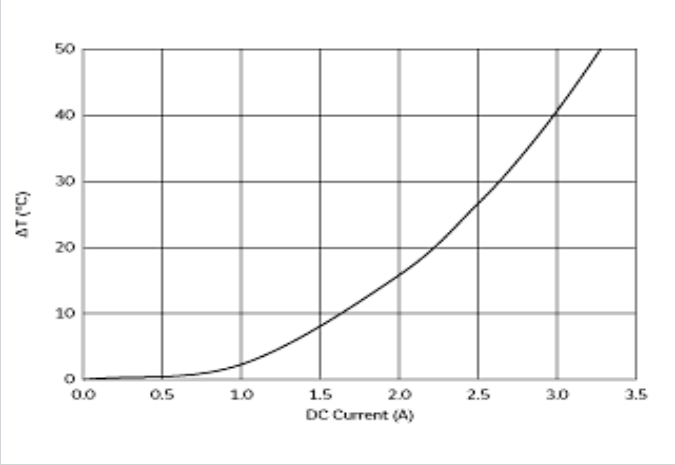
Inductance	1.5µH ±20%
Inductance test frequency	1MHz
Rated current (Isat) (Based on Inductance change)	3500mA
Rated current (Itemp) (Based on Temperature rise)	2600mA
Max. of DC resistance	0.060Ω
Operating temperature range (Self-temperature rise is included)	-40～125℃
Class of magnetic shield	Metal Alloy
Absolute maximum voltage	20V DC
Series	DFE252012P

Chart of characteristic data (The charts below may show another part number which shares its characteristics.)

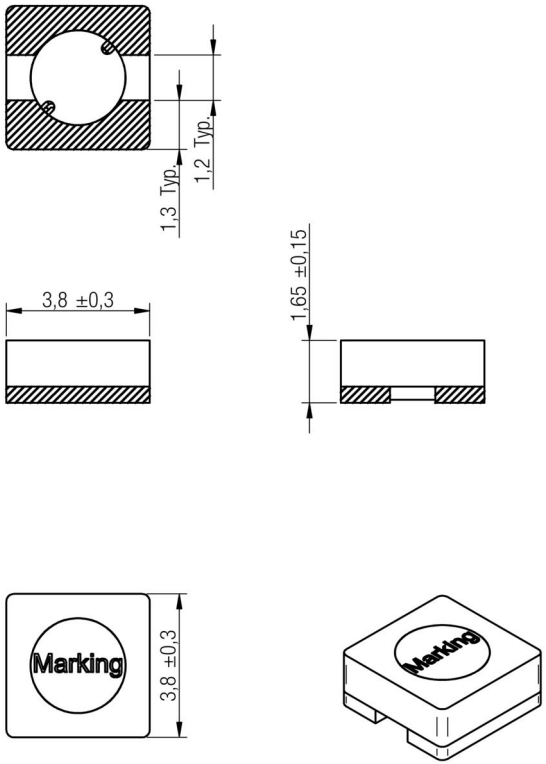
- Inductance-Current characteristics (Typ.)



- Temperature rise characteristics (Typ.)



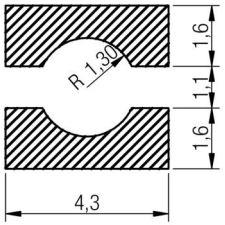
A Dimensions: [mm]



Scale - 5:1

Reference on drawing	Description
Marking	2R5 (Inductance Code)

B Recommended land pattern: [mm]



Scale - 5:1

C Schematic:

D Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 100 mV	L	2.5	µH	±30%
Rated current	ΔT = 30 K	I_R	1.45	A	max.
Saturation current	|ΔL/L| < 35%	I_{sat}	1.25	A	typ.
DC Resistance	@ 20°C	R_{DC}	50	mΩ	typ.
DC Resistance	@ 20°C	R_{DC}	58	mΩ	max.
Self resonant frequency		f_{res}	120	MHz	typ.

E General information:

It is recommended that the temperature of the part does not exceed 125°C under worst case operating conditions.

- Ambient temperature: -40°C to +95°C (refering to I_R)
- Operating temperature: -40°C to +125°C
- Storage temperature (on tape & reel): -20°C to +40°C; 75% RH max.
- Test conditions of Electrical Properties: 20°C, 33% RH if not specified differently

REV	DATE	BY	CHECKED
6.4	2015-01-29	SSt	JRS
6.3	2014-09-11	SSt	JRS
6.2	2014-04-01	SSt	SSt
6.1	2013-04-08	SSt	COt
6.0	2009-01-15	ME	-

Projection

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EMC & Inductive Solutions
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74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WE-TPC SMD Shielded Tiny Power Inductor

Order.- No.

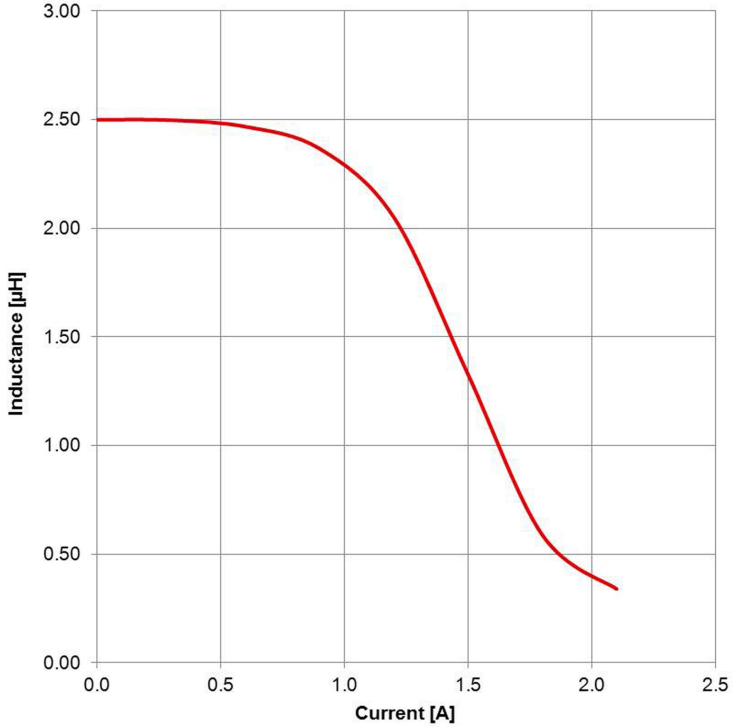
744031002

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 3816

F1 Typical Inductance vs. Current Characteristics:



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6.4	2015-01-29	SSt	JRS
6.3	2014-09-11	SSt	JRS
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Order.- No.

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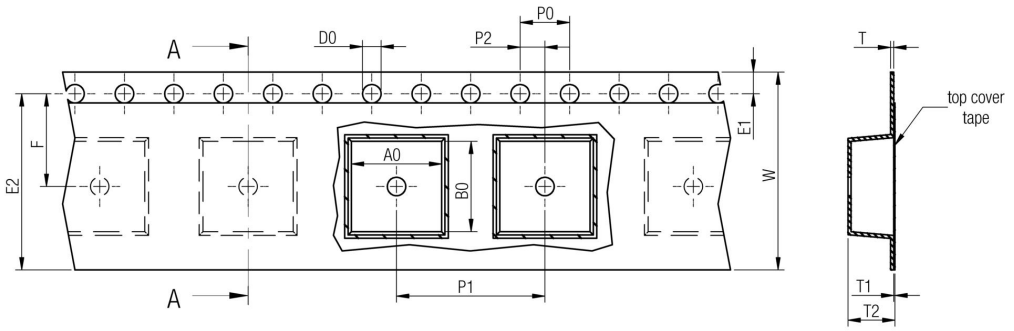
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE

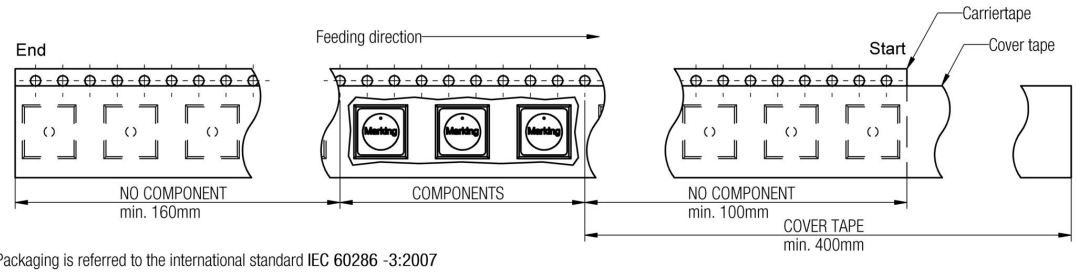
A4

Size: 3816

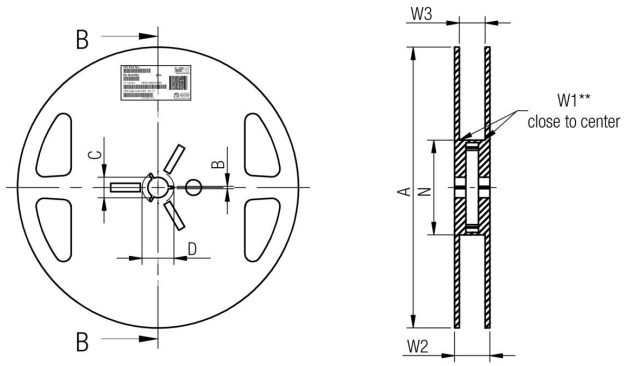
G Packaging Specification - Tape and Reel [mm]:



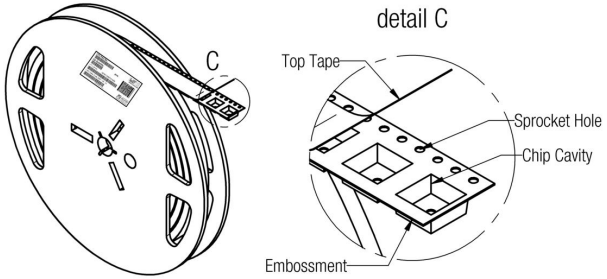
		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	+0,3 -0,1	± 0,1	± 0,1	max.	typ.	+0,1 -0,0	± 0,1	min.	± 0,05	± 0,1	± 0,05		
size	**3816**	4,30	4,30	12,00	8,00	0,25	0,10	2,00	1,50	1,75	10,25	5,50	4,00	2,00	Polystyrene	1000
	4818	5,30	5,30	12,00	8,00	0,25	0,10	2,50	1,50	1,75	10,25	5,50	4,00	2,00	Polystyrene	800
	4828	5,30	5,30	12,00	8,00	0,25	0,10	3,00	1,50	1,75	10,25	5,50	4,00	2,00	Polystyrene	500
	5818	6,30	6,30	16,00	12,00	0,25	0,10	2,50	1,50	1,75	14,25	7,50	4,00	2,00	Polystyrene	500
	5828	6,30	6,30	16,00	12,00	0,25	0,10	3,00	1,50	1,75	14,25	7,50	4,00	2,00	Polystyrene	400
	6823	7,30	7,30	16,00	12,00	0,25	0,10	3,00	1,50	1,75	14,25	7,50	4,00	2,00	Polystyrene	500

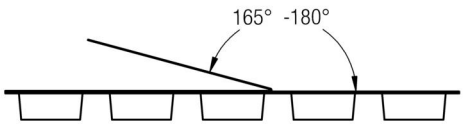


Packaging is referred to the international standard IEC 60286 -3:2007



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	min.	+ 1,5	max.	min.	max.
Tape width	**12 mm**	178,00	1,50	13,00	20,20	50,00	12,40	18,40	11,90	15,40
	16 mm	178,00	1,50	13,00	20,20	50,00	16,40	22,40	15,90	19,40





		Pull-of force
Tape width	**12 mm**	0,1 N - 1,0 N
	16 mm	0,1 N - 1,3 N

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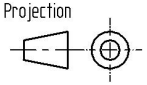
6.4	2015-01-29	SSt	JRS
6.3	2014-09-11	SSt	JRS
6.2	2014-04-01	SSt	SSt
6.1	2013-04-08	SSt	COt
6.0	2009-01-15	ME	-

Projection



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DESCRIPTION

WE-TPC SMD Shielded Tiny Power Inductor

Order.- No.

744031002

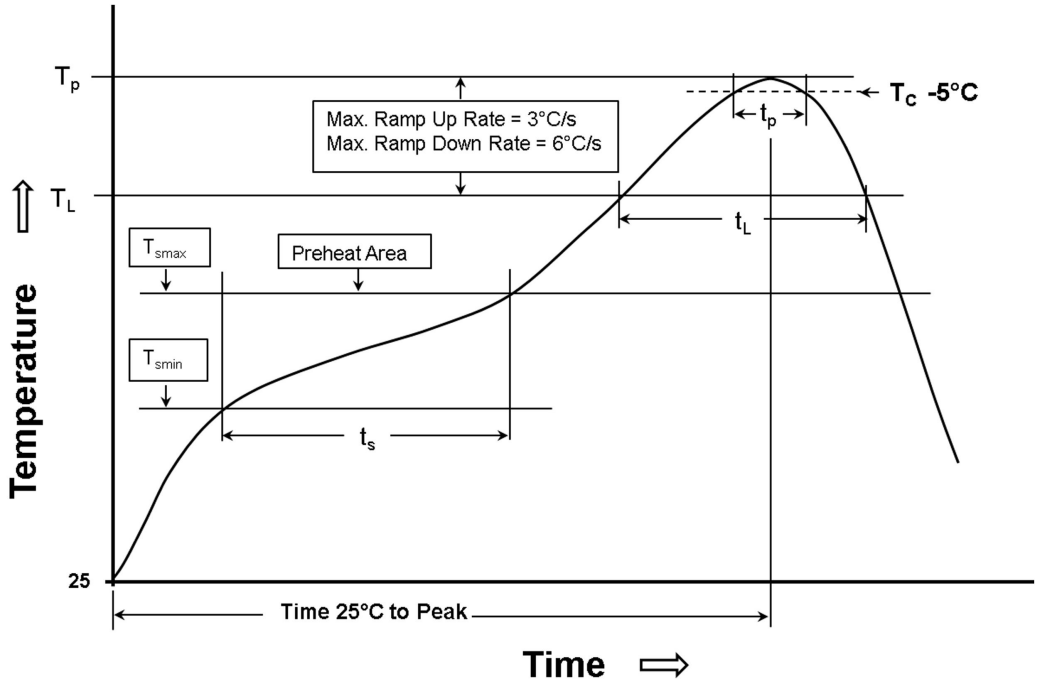
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 3816

H Soldering Specifications:

H1: Classification Reflow Profile for SMT components:



H2: Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/ second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_p)	See Table H3
Time within 5°C of actual peak temperature (t_p)	20-30 seconds, except T_p 260°C at t_p 10 seconds
Ramp-down rate (T_P to T_L)	6°C/ second max.
Time 25°C to peak temperature	8 minutes max.

refer to IPC/JEDEC J-STD-020D

H3: Package Classification Reflow Temperature

	Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
PB-Free Assembly	< 1.6 mm	260°C	260°C	260°C
PB-Free Assembly	1.6 - 2.5 mm	260°C	250°C	245°C
PB-Free Assembly	≥ 2.5 mm	250°C	245°C	245°C

refer to IPC/JEDEC J-STD-020D

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6.2	2014-04-01	SSt	SSt
6.1	2013-04-08	SSt	COt
6.0	2009-01-15	ME	-

Projection

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DESCRIPTION

WE-TPC SMD Shielded Tiny Power Inductor

Order.- No.

744031002

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 3816

I Cautions and Warnings:

The following conditions apply to all goods within the product series of WE-TPC of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data sheet have to be complied with.

The usage and operation of the product within ambient conditions, which probably alloy or harm the wire isolation, has to be avoided.

If the product is potted in customer applications, the potting material might shrink during and after hardening. The product is exposed to the pressure of the potting material with the effect that the core, wire and termination is possibly damaged by this pressure and so the electrical as well as the mechanical characteristics are endangered to be affected. After the potting material is cured, the core, wire and termination of the product have to be checked if any reduced electrical or mechanical functions or destructions have occurred.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply to customer specific products.

Cleaning agents that are used to clean the customer application might damage or change the characteristics of the component, body, pins or termination.

Direct mechanical impact to the product shall be prevented as the ferrite material of the core could flake or in the worst case it could break.

Product specific:
Follow all instructions mentioned in the data sheet, especially:

- The soldering profile has to be complied with according to the technical reflow soldering specification, otherwise this will void the warranty.
- All products shall be used before the end of the period of 12 months based on the product date code, if not a 100% solderability can´t be ensured.
- Violation of the technical product specifications such as exceeding the nominal rated current will void the warranty.

The general and product specific cautions comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable; however, no responsibility is assumed for inaccuracies or incompleteness.

REV	DATE	BY	CHECKED
6.4	2015-01-29	SSt	JRS
6.3	2014-09-11	SSt	JRS
6.2	2014-04-01	SSt	SSt
6.1	2013-04-08	SSt	COt
6.0	2009-01-15	ME	-

Projection

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WE-TPC SMD Shielded Tiny Power Inductor

Order.- No.

744031002

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE: A4

Size: 3816

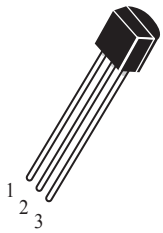
WEITRON

S8050

NPN General Purpose Transistors

Lead(Pb)-Free

TO-92



1. EMITTER
2. BASE
3. COLLECTOR

ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base VOltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	500	mAdc
Total Device Dissipation T_A=25℃	P_D	0.625	W
Junction Temperature	T_j	150	°C
Storage, Temperature	Tstg	-55 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage (I_C= 0.1 mAdc, I_B=0)	$V_{(BR)CEO}$	25	-	Vdc
Collector-Base Breakdown Voltage (I_C= 100 μAdc, I_E=0)	$V_{(BR)CBO}$	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E= 100 μAdc, I_C=0)	$V_{(BR)EBO}$	5.0	-	Vdc
Collector Cutoff Current (V_{CE}= 20 Vdc, I_B=0)	I_{CEO}	-	0.1	uAdc
Collector Cutoff Current (V_{CB}= 40 Vdc, I_E=0)	I_{CBO}	-	0.1	uAdc
Emitter Cutoff Current (V_{EB}= 3.0Vdc, I_C=0)	I_{EBO}	-	0.1	uAdc

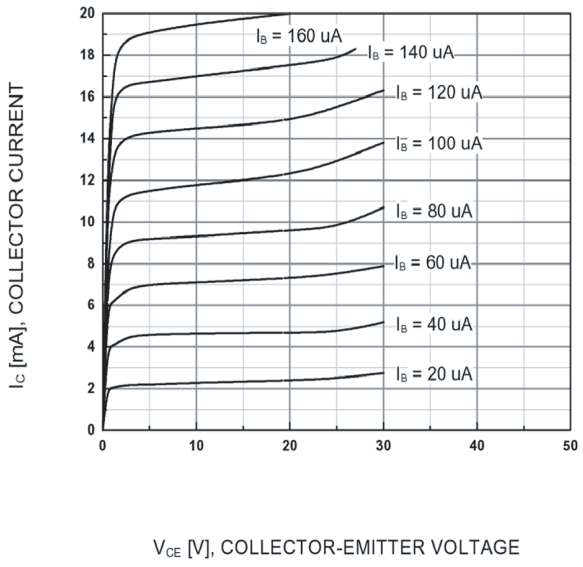
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted) (Countinued)

Characteristics	Symbol	Min	TYP	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C= 50 Adc, V_{CE}=1.0 Vdc)	h_{FE} (1)	85	-	300	-
DC Current Gain (I_C= 500 mAdc, V_{CE}= 1.0 Vdc)	h_{FE} (2)	50	-	-	-
Collector-Emitter Saturation Voltage (I_C= 500 Adc, I_B= 50 mAdc)	$V_{CE(sat)}$	-	-	0.6	Vdc
Base-Emitter Saturation Voltage (I_C= 500 mAdc, I_B= 50 mAdc)	$V_{BE(sat)}$	-	-	1.2	Vdc
Current-Gain-Bandwidth Product (I_C= 20 mAdc, V_{CE}=6.0 Vdc, f=30MHz)	f_T	150	-	-	MHz

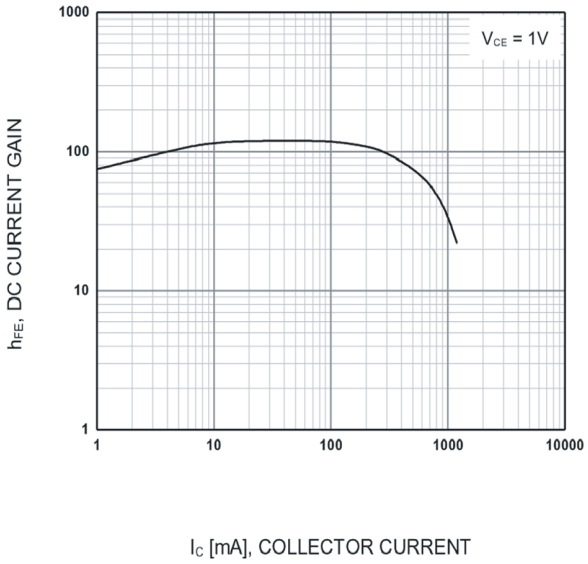
Classification of $h_{FE(1)}$

Rank	B	C	D
Range	85-160	120-200	160-300

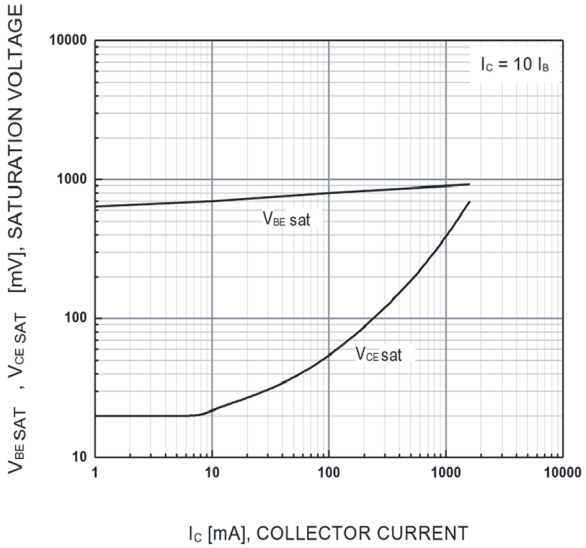
Typical Characteristics



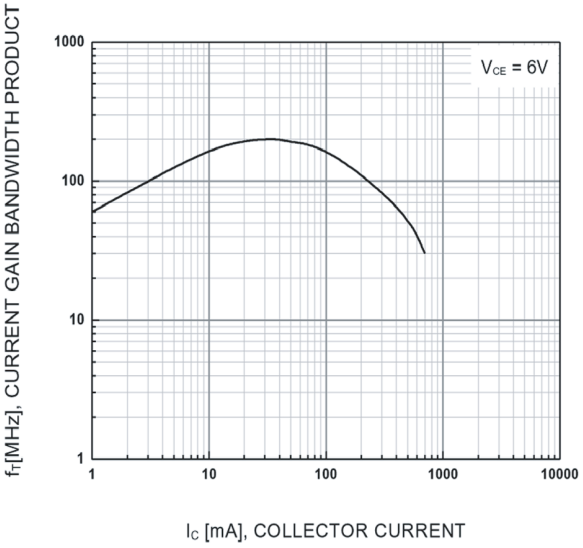
Static Characteristic



DC current Gain



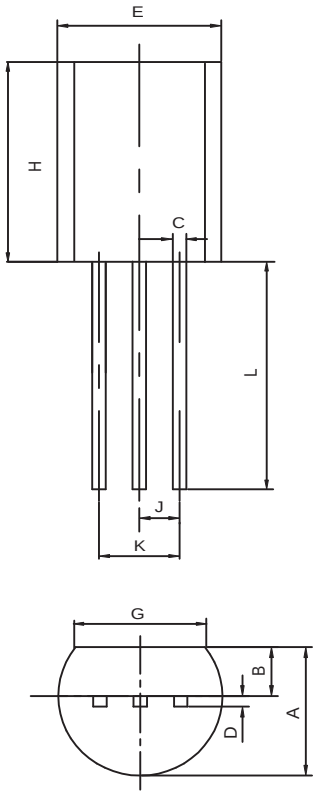
Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage



Current Gain Bandwidth Product

TO-92 Outline Dimensions

unit:mm



TO-92		
Dim	**Min**	**Max**
A	3.30	3.70
B	1.10	1.40
C	0.38	0.55
D	0.36	0.51
E	4.40	4.70
G	3.43	-
H	4.30	4.70
J	1.270TYP	
K	2.44	2.64
L	14.10	14.50

Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected Up To 3KV**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

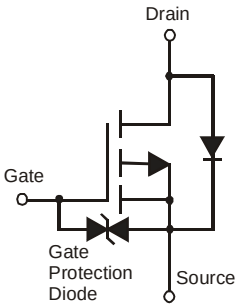
Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Weight: 0.008 grams (approximate)

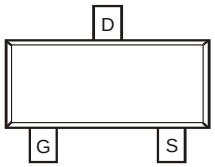
ESD PROTECTED TO 3kV

SOT23

Top View



Internal Schematic



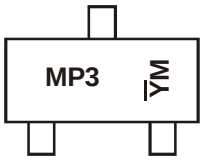
Top View

Ordering Information (Note 4)

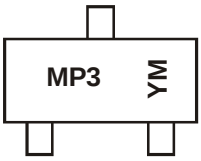
Part Number	Compliance	Case	Packaging
DMP2035U-7	Standard	SOT23	3000 / 7” Tape & Reel
DMP2035UQ-7	Automotive	SOT23	3000 / 7” Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

MP3 = Product Type Marking Code
YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
$\overline{Y}\overline{M}$ = Date Code Marking for CAT (Chengdu Assembly/ Test site)
Y or $\overline{Y}$ = Year (ex: A = 2013)
M = Month (ex: 9 = September)

Date Code Key

Year	2009	2010	2011	2012	2013	2014	2015
Code	W	X	Y	Z	A	B	C

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current (Note 5)	Steady State	T_A = +25°C T_A = +70°C	I_D	-3.6 -2.9	A
Pulsed Drain Current (Note 6)			I_{DM}	-24	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	0.81	W
Thermal Resistance, Junction to Ambient @T_A = +25°C	$R_{\theta JA}$	153.5	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

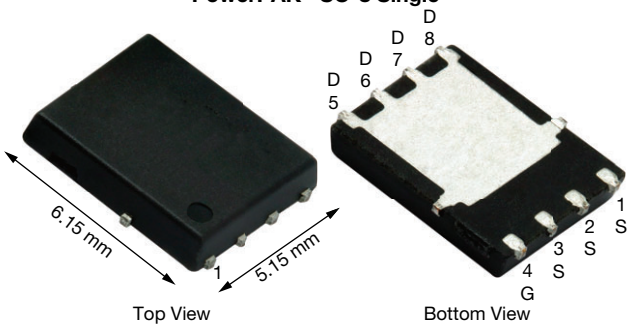
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1.0	μA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-0.7	-1.0	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	23 30 41	35 45 62	mΩ	V_{GS} = -4.5V, I_D = -4.0A V_{GS} = -2.5V, I_D = -4.0A V_{GS} = -1.8V, I_D = -2.0A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	14	—	S	V_{DS} = -5V, I_D = -4A
Diode Forward Voltage	V_{SD}	—	-0.7	-1.0	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1610	—	pF	V_{DS} = -10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	157	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	145	—	pF	
Gate Resistance	R_g	—	9.45	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	15.4	—	nC	V_{GS} = -4.5V, V_{DS} = -10V, I_D = -4A
Gate-Source Charge	Q_{gs}	—	2.5	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.3	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	16.8	—	ns	V_{DS} = -10V, V_{GS} = -4.5V, R_L = 10Ω, R_G = 6.0Ω, I_D = -1A
Turn-On Rise Time	t_r	—	12.4	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	94.1	—	ns	
Turn-Off Fall Time	t_f	—	42.4	—	ns	

Notes:
5. Device mounted on FR-4 PCB with 2 oz. Copper and test pulse width t ≦10s.
6. Repetitive rating, pulse width limited by junction temperature.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

P-Channel 20 V (D-S) MOSFET

PowerPAK® SO-8 Single



Top View Bottom View

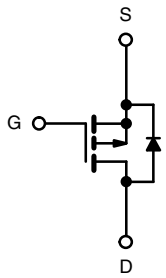
FEATURES

- TrenchFET® power MOSFET
- 100 % UIS tested
- Material categorization:
  for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Adapter switch



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0033
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.0055
Q_g typ. (nC)	85
I_D (A) [a]	-60
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	Si7633DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	-60 [a]	A
	T_C = 70 °C		-60 [a]	
	T_A = 25 °C		-34 [b, c]	
	T_A = 70 °C		-27 [b, c]	
Pulsed drain current		I_{DM}	-100	
Continuous source-drain diode current	T_C = 25 °C	I_S	-60 [a]	
	T_A = 25 °C		-5.6 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	-25	
Single pulse avalanche energy		E_{AS}	31	mJ
Maximum power dissipation	T_C = 25 °C	P_D	104	W
	T_C = 70 °C		66.6	
	T_A = 25 °C		6.25 [b, c]	
	T_A = 70 °C		4 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.9	1.2	

Notes
a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 54 °C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-19	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	6.4	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-1	-	-3	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	-	-	-1	µA
		V_{DS} = -20 V, V_{GS} = 0 V, T_J = 55 °C	-	-	-10	
On-state drain current [a]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	-30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -20 A	-	0.0027	0.0033	Ω
		V_{GS} = -4.5 V, I_D = -15 A	-	0.0044	0.0055	
Forward transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -20 A	-	80	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	-	9500	-	pF
Output capacitance	C_{oss}		-	1830	-	
Reverse transfer capacitance	C_{rss}		-	1740	-	
Total gate charge	Q_g	V_{DS} = - 0 V, V_{GS} = -10 V, I_D = -20 A	-	173	260	nC
		V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -20 A	-	85	130	
Gate-source charge	Q_{gs}		-	24	-	
Gate-drain charge	Q_{gd}		-	37	-	
Gate resistance	R_g	f = 1 MHz	-	1.5	-	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 10 Ω, $I_D \cong$ -1 A, V_{GEN} = -10 V, R_g = 1 Ω	-	21	40	ns
Rise time	t_r		-	12	30	
Turn-off delay time	$t_{d(off)}$		-	100	150	
Fall time	t_f		-	25	40	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 10 Ω, $I_D \cong$ - 1 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	100	150	
Rise time	t_r		-	90	140	
Turn-off delay time	$t_{d(off)}$		-	85	130	
Fall time	t_f		-	50	75	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	60	A
Pulse diode forward current [a]	I_{SM}		-	-	100	
Body diode voltage	V_{SD}	I_S = -5 A	-	-0.74	-1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 3.5 A, di/dt = 100 A/µs, T_J = 25 °C	-	65	130	ns
Body diode reverse recovery charge	Q_{rr}		-	85	170	nC
Reverse recovery fall time	t_a		-	34	-	ns
Reverse recovery rise time	t_b		-	31	-	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STD3NK80Z-1, STD3NK80ZT4, STF3NK80Z, STP3NK80Z

N-channel 800 V, 3.8 Ω typ., 2.5 A SuperMESH™ Power MOSFETs in IPAK, DPAK, TO-220FP, TO-220 packages

Datasheet - production data

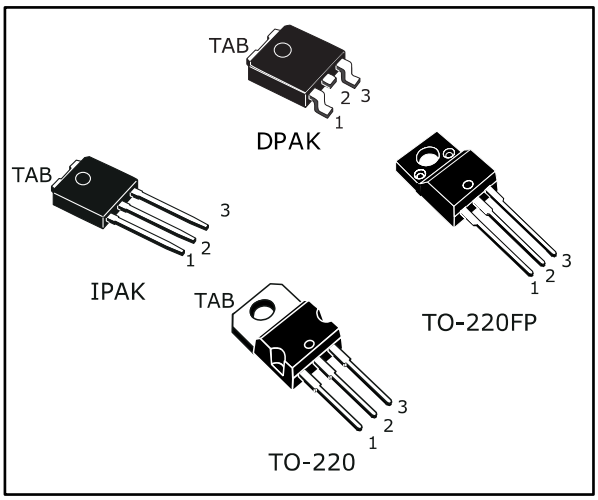
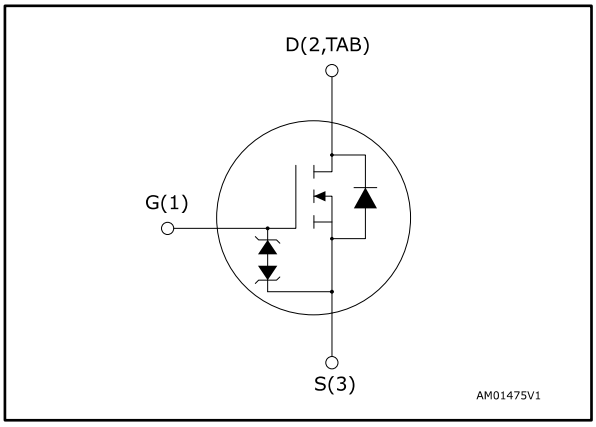


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD3NK80Z-1	800 V	4.5 Ω	2.5 A
STD3NK80ZT4	800 V	4.5 Ω	2.5 A
STF3NK80Z	800 V	4.5 Ω	2.5 A
STP3NK80Z	800 V	4.5 Ω	2.5 A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

These high voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications. Such series complements ST's full range of high voltage MOSFETs including the revolutionary MDmesh™ products.

Table 1: Device summary

Order code	Marking	Package	Packaging
STD3NK80Z-1	D3NK80Z	IPAK	Tube
STD3NK80ZT4	D3NK80Z	DPAK	Tape and reel
STF3NK80Z	F3NK80Z	TO-220FP	Tube
STP3NK80Z	P3NK80Z	TO-220	Tube

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK, IPAK	TO-220FP	
V_{DS}	Drain-source voltage	800		V
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	2.5	2.5(1)	A
	Drain current (continuous) at T_C = 100 °C	1.57	1.57(1)	A
I_{DM}(2)	Drain current (pulsed)	10	10(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	W
ESD	Gate-source, human body model, R = 1.5 kΩ, C = 100 pF	2		kV
dv/dt(3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)		2.5	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_j	Operation junction temperature range			

Notes:

(1)This value is limited by package.

(2)Pulse width is limited by safe operating area.

(3)I_{SD} ≤ 2.5 A, di/dt ≤ 200 A/µs, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 640 V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		TO-220	TO-220FP	DPAK	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	1.78	5	1.78		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5			100	°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb			50		°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{J\,max}$)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_J =25 °C, I_D = I_{AR}, V_{DD}= 50 V)	170	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 1.25 A		3.8	4.5	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	-	485	-	pF
C_{oss}	Output capacitance		-	57	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
$C_{oss\ eq}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 640 V	-	22	-	pF
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 2.5 A, V_{GS} = 0 to 10 V (see *Figure 17: "Test circuit for gate charge behavior"*)	-	19	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	nC
Q_{gd}	Gate-drain charge		-	10.8	-	nC

Notes:

(1)$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 1.25 A, R_G = 4.7 Ω, V_{GS} =10 V (see *Figure 16: "Test circuit for resistive load switching times"* and *Figure 21: "Switching time waveform"*)	-	17	-	ns
t_r	Rise time		-	27	-	ns
$t_{d(off)}$	Turn-off delay time		-	36	-	ns
t_f	Fall time		-	40	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		10	A
V_{SD}(2)	Forward on voltage	I_{SD} = 2.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs V_{DD} = 50 V (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	384		ns
Q_{rr}	Reverse recovery charge		-	1.6		µC
I_{RRM}	Reverse recovery current		-	8.4		A
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs, V_{DD} = 50 V , T_J = 150 °C (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	474		ns
Q_{rr}	Reverse recovery charge		-	2.1		µC
I_{RRM}	Reverse recovery current		-	8.8		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

(2)Pulse width is limited by safe operating area.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

APPROVAL SHEET

WW25P, WW20P, WW12P

±1%, ±5%

Thick Film High Power Low Ohm Chip Resistors

Size 2512 2W, 2010 1W, 1206 1/2W

*Contents in this sheet are subject to change without prior notice.

QUICK REFERENCE DATA

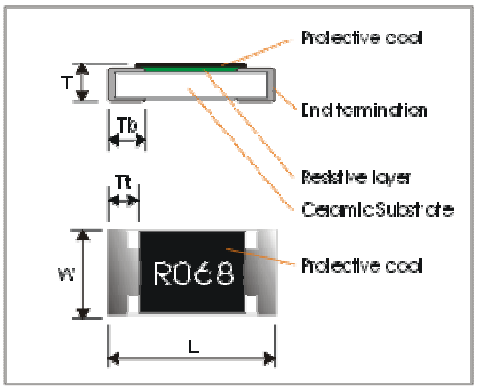
Item	General Specification		
Series No.	WW25P	WW20P	WW12P
Size code	2512 (6432)	2010 (5025)	1206 (3216)
Resistance Tolerance	±1%, ±5%		
Resistance Range	0.047Ω ~ 0.976Ω		0.020Ω ~ 0.976Ω
TCR (ppm/°C) 100mohm ~ 976mohm 47mohm ~ 97.6mohm 20 mohm ~ 43mohm	±100ppm ±150ppm -	±100ppm ±150ppm -	±100ppm ±200ppm ±1000ppm
Max. dissipation at T_{amb}=70°C	2 W	1 W	1/2 W
Max. Operation Voltage (DC or RMS)	300V	200V	200V
Max. Overload Voltage (DC or RMS)	500V	400V	400V
Climatic category (IEC 60068)	55/155/56		

Note :

1. This is the maximum voltage that may be continuously supplied to the resistor element, see "IEC publication 60115-8"
2. Max. Operation Voltage : So called RCWV (Rated Continuous Working Voltage) is determined by

   $$RCWV = \sqrt{Rated\,Power \times Resistance\,Value}$$ or Max. RCWV listed above, whichever is lower.
3. 2W loading with total solder-pad and trace size of 300 mm^2
4. Resistance value will be changed by soldering condition and design of soldering pad, please design products in consideration of this change of resistance value.

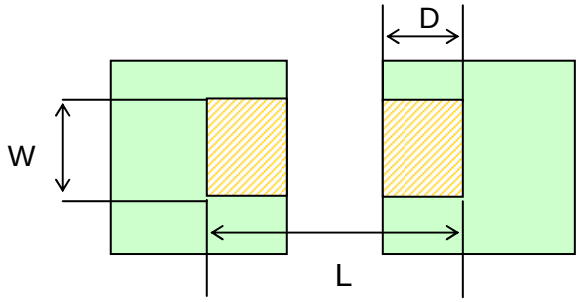
MECHANICAL DATA



Unit: mm

Symbol	WW25P	WW20P	WW12P
L	6.30 ± 0.20	5.00 ± 0.20	3.10 ± 0.15
W	3.10 ± 0.20	2.50 ± 0.20	1.60 ± 0.15
T	0.60 ± 0.15	0.60 ± 0.10	0.55 ± 0.10
Tt	0.60 ± 0.25	0.60 ± 0.25	0.50 ± 0.25
Tb	1.80 ± 0.25	0.60 ± 0.25	0.50 ± 0.25

Recommended Solder Pad Dimensions



Type	W	D	L
WW25P	3.7mm	2.45mm	7.6mm

MARKING

Each resistor is marked with a four-digit code on the protective coating to designate the nominal resistance value.

Example:

R100 = 0.100Ω
R910 = 0.910Ω

FUNCTIONAL DESCRIPTION

Product characterization

Standard values of nominal resistance are taken from the E96 & E24 series for resistors with a tolerance of ±5% & ±1%. The values of the E24/E96 series are in accordance with “IEC publication 60063”.

Derating curve

The power that the resistor can dissipate depends on the operating temperature; see Fig.2

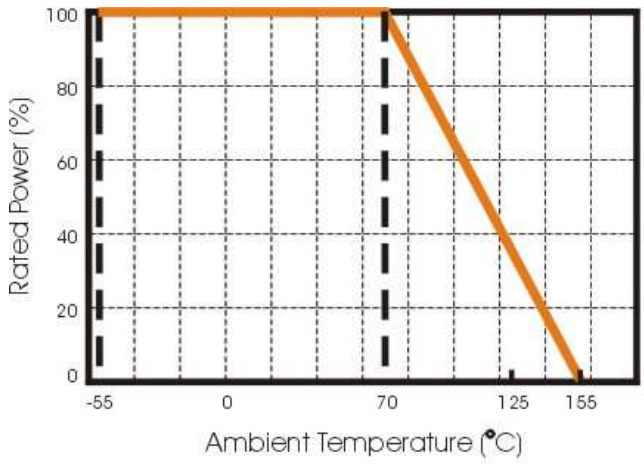


Figure 2 Maximum dissipation in percentage of rated power as a function of the ambient temperature

MOUNTING

Due to their rectangular shapes and small tolerances, Surface Mountable Resistors are suitable for handling by automatic placement systems.

Chip placement can be on ceramic substrates and printed-circuit boards (PCBs).

Electrical connection to the circuit is by individual soldering condition.

The end terminations guarantee a reliable contact.

SOLDERING CONDITION

The robust construction of chip resistors allows them to be completely immersed in a solder bath of 260°C for 10 seconds. Therefore, it is possible to mount Surface Mount Resistors on one side of a PCB and other discrete components on the reverse (mixed PCBs).

Surface Mount Resistors are tested for solderability at 235°C during 2 seconds. The test condition for no leaching is 260°C for 30 seconds. Typical examples of soldering processes that provide reliable joints without any damage are given in Fig 3.

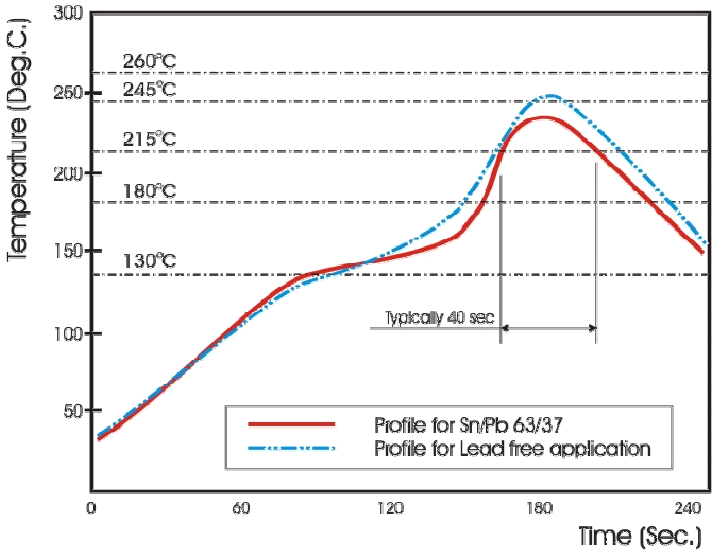


Fig 3. Infrared soldering profile for Chip Resistors

CATALOGUE NUMBERS

The resistors have a catalogue number starting with.

WW25	P	R100	J	T	L
Size code WW25 : 2512 WW20 : 2010 WW12 : 1206	**Type code** P :Power 2512 size=2 watt 2010 size=1 watt 1206 size=0.5 watt	**Resistance code** E96 +E24: "R" is first digit followed by 3 significant digits. e.g.: 0.1ohm = R100 0.047ohm = R047 0.56ohm = R560	**Tolerance** J : ±5% F : ±1%	**Packaging code** T : 7" Reel taping G : 13" Reel taping	**Termination code** L = Sn base (lead free)

Tape packaging WW12 : 8mm width paper taping 5,000pcs per 7" reel. 20,000pcs per 13" reel.

WW25；WW20: 12mm width plastic taping 4,000pcs per reel.

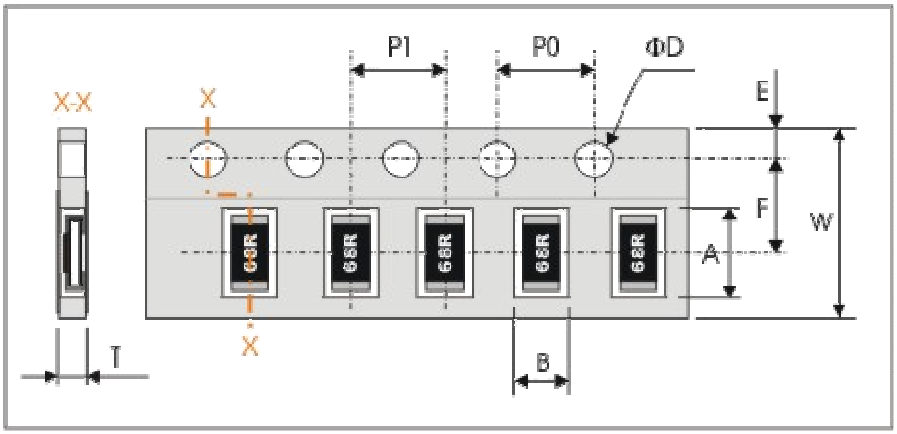
TEST AND REQUIREMENTS

Basic specification : JIS C 5201-1 : 1998

TEST	PROCEDURE	REQUIREMENT
Clause 4.8 Temperature Coefficient of Resistance (TCR)	Natural resistance change per change in degree centigrade. $\frac{R_2 - R_1}{R_1(t_2 - t_1)} \times 10^6$ (ppm/°C) R_1 : Resistance at reference temperature R_2 : Resistance at test temperature t_1 : 20℃+5℃-1℃	Refer to quick reference data for T.C.R specification
Clause 4.13 Short time overload	Permanent resistance change after 5 second application of a power 5.0 times of rated power or the maximum overload voltage specified in the above list, whichever is less.	ΔR/R max. J:≦ ±(2%+0.5mΩ) F:≦ ±(1%+0.5mΩ)
Clause 4.18 Resistance to soldering heat(R.S.H)	Un-mounted chips completely immersed for 10±1second in a SAC solder bath at 260℃±5°C	No visible damage ΔR/R max. J:≦ ±(1%+0.5mΩ) F:≦ ±(0.5%+0.5mΩ)
Clause 4.17 Solderability	Un-mounted chips completely immersed for 2±0.5second in a SAC solder bath at 235℃±5℃	Good tinning (>95% covered) No visible damage
Clause 4.19 Temperature cycling	30 minutes at -55°C±3°C, 2~3 minutes at 20℃+5℃-1℃, 30 minutes at +155°C±3°C, 2~3 minutes at 20℃+5℃-1℃, total 5 continuous cycles	No visible damage ΔR/R max. J≦ ±(1%+1mΩ) F≦ ±(0.5%+1mΩ)
Clause 4.25 Load life (endurance)	1000 +48/-0 hours, loaded with RCWV or Vmax in chamber controller 70±2ºC, 1.5 hours on and 0.5 hours off	No visible damage ΔR/R max. J≦ ±(3%+0.5mΩ) F≦ ±(1%+0.5mΩ)
Clause 4.24 Load life in Humidity	1000 +48/-0 hours, loaded with RCWV or Vmax in humidity chamber controller at 40℃±2℃ and 90~95% relative humidity, 1.5hours on and 0.5 hours off	No visible damage ΔR/R max. J≦ ±(3%+0.5mΩ) F≦ ±(1%+0.5mΩ)
Clause 4.33 Bending strength	Resistors mounted on a 90mm glass epoxy resin PCB(FR4); bending : 2 mm(2512;2010) 3mm(1206), once for 10 seconds	No visible damage ΔR/R max. J≦ ±(1%+1mΩ) F≦ ±(0.5%+1mΩ)
Clause 4.32 Adhesion	Pressurizing force: 5N, Test time: 10±1sec	No remarkable damage or removal of the terminations
Insulation Resistance **Clause 4.6**	Apply the maximum overload voltage (DC) for 1minutes	R≧10GΩ
Dielectric Withstand Voltage **Clause 4.7**	Apply the maximum overload voltage (AC) for 1 minutes	No breakdown or flashover

PACKAGING

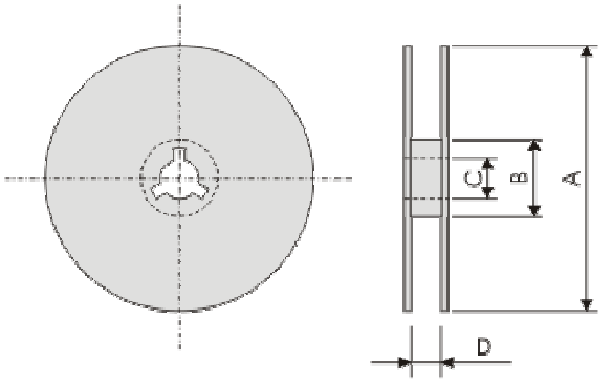
Paper Tape(WW12P) & Plastic Tape(WW25P;WW20P) specifications (unit :mm)



Series No.	A	B	W	F	E
WW25P	6.90±0.20	3.60±0.20	12.00±0.30	5.50±0.10	1.75±0.10
WW20P	5.50±0.20	2.80±0.20			
WW12P	3.60±0.20	2.00±0.20	8.00±0.30	3.50±0.20	

Series No.	P1	P0	ΦD	T
WW25P	4.00±0.10	4.00±0.10	$\Phi 1.50^{+0.1}_{-0.0}$	Max. 1.2
WW20P				
WW12P				Max. 1.0

Reel dimensions



(unit : mm)

Reel / Tape	A	B	C	D
7” reel for 8mm tape	Φ178.0±2.0	Φ60.0±1.0	13.0±0.2	9.00±0.50
7” reel for 12mm tape				12.4±1.00
13” reel for 8mm tape	Φ330.0±2.00	Φ100.0±1.00	13.0±0.2	9.00±0.50

Metal Film (Thin Film) Chip Resistors, High Reliability Type

Series: ERA 1A, 2A, 3A, 6A, 8A

Features

- High reliability·····Stable at high temperature and humidity
  (85 °C 85 %RH rated load, Category temperature range : −55 °C to +155 °C)
- High accuracy·····Low resistance tolerance and Temperature Coefficient of Resistance
- High performance···Low current noise, excellent linearity
- Reference Standard····· IEC 60115-8, JIS C 5201-8, JEITA RC-2133C
- AEC-Q200 compliant (except ERA1A)
- RoHS compliant

■ **As for Packaging Methods, Land Pattern, Soldering Conditions and Safety Precautions,**
Please see Data Files

Explanation of Part Numbers

● E24 Series

1	2	3	4	5	6	7	8	9	10	11
E	R	A	3	A	E	B	1	0	2	V

Product Code

Thin Film Chip Resistors

Size, Power Rating

Code	inch size	Power Rating
1A	0201	0.05 W
2A	0402	0.063 W
3A	0603	0.1 W
6A	0805	0.125 W
8A	1206	0.25 W

Temp. Coefficient

Code	T.C.R.
R	$\pm10\times10^{-6}$/K
P	$\pm15\times10^{-6}$/K
E	$\pm25\times10^{-6}$/K
H	$\pm50\times10^{-6}$/K
K	$\pm100\times10^{-6}$/K

Resistance Tolerance

Code	Tolerance
W	±0.05 %
B	±0.1 %
C	±0.25 %
D	±0.5 %

Resistance Value

Consist of three figures for E24 series resistance value.
The first two digits are significant figures of resistance and the third one denotes number of zeros following.
(example) 102 : 1 kΩ

Packaging Methods

Code	Packaging	Part No.
C	Pressed Carrier Taping 2 mm pitch, 15,000 pcs	ERA1A
X	Punched Carrier Taping 2 mm pitch, 10,000 pcs	ERA2A
V	Punched Carrier Taping 4 mm pitch, 5,000 pcs	ERA3A ERA6A ERA8A

● E96 Series and other Resistance values

1	2	3	4	5	6	7	8	9	10	11	12
E	R	A	3	A	E	B	1	0	5	1	V

Product Code

Thin Film Chip Resistors

Size, Power Rating

Code	inch size	Power Rating
1A	0201	0.05 W
2A	0402	0.063 W
3A	0603	0.1 W
6A	0805	0.125 W
8A	1206	0.25 W

Temp. Coefficient

Code	T.C.R.
R	$\pm10\times10^{-6}$/K
P	$\pm15\times10^{-6}$/K
E	$\pm25\times10^{-6}$/K
H	$\pm50\times10^{-6}$/K
K	$\pm100\times10^{-6}$/K

Resistance Tolerance

Code	Tolerance
W	±0.05 %
B	±0.1 %
C	±0.25 %
D	±0.5 %

Resistance Value

Consist of four figures for E96 series resistance value.
The first three digits are significant figures of resistance and the fourth one denotes number of zeros following.
(example)
1051 : 1.05 kΩ

Packaging Methods

Code	Packaging	Part No.
C	Pressed Carrier Taping 2 mm pitch, 15,000 pcs	ERA1A
X	Punched Carrier Taping 2 mm pitch, 10,000 pcs	ERA2A
V	Punched Carrier Taping 4 mm pitch, 5,000 pcs	ERA3A ERA6A ERA8A

Note : Duplicated resistance values as E24 series part umbers shall follow E24 part numbers.
(apply three digit resistance value)

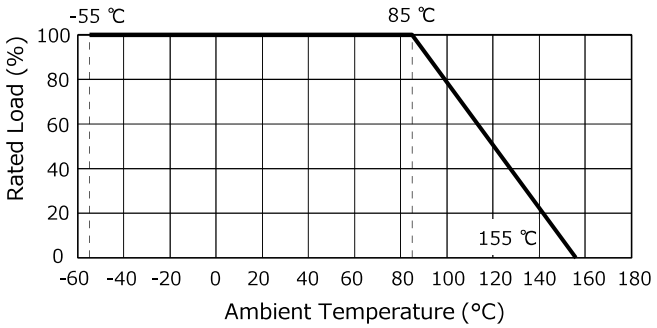
Ratings

Part No. (inch size)	Power Rating at 85 °C(1) (W)	Limiting Element Voltage(2) (V)	Maximum Overload Voltage(3) (V)	Part No. (detail)	Resistance Tolerance (%)	T.C.R. (×10⁻⁶/K)	Resistance Range(4)(5) (Ω)	Category Temperature Range (℃)	AEC-Q200 Grade
ERA1A (0201)	0.05	25	50	ERA1AEB	±0.1	±25	100 to 10 k (E24,E96)	−55 to +155	-
				ERA1AEC	±0.25				
				ERA1ARC	±0.25	±10	100 to 10 k (E24,E96)		
				ERA1ARB	±0.1				
				ERA1ARW	±0.05		1 k to 10 k (E24,E96)		
ERA2A (0402)	0.063	50	100	ERA2AKD	±0.5	±100	10 to 46.4 (E24,E96)		Grade 1
				ERA2AED	±0.5	±25	47 to 100 k (E24,E96)		
				ERA2AEC	±0.25				
				ERA2AEB	±0.1				
				ERA2APC	±0.25	±15	200 to 47 k (E24,E96)		
				ERA2APB	±0.1				
				ERA2ARC	±0.25	±10	200 to 47 k (E24,E96)		
				ERA2ARB	±0.1				
ERA3A (0603)	0.1	75	150	ERA3AHD	±0.5	±50	10 to 46.4 (E24,E96)		Grade 0
				ERA3AED	±0.5	±25	47 to 330 k (E24,E96)		
				ERA3AEC	±0.25				
				ERA3AEB	±0.1				
				ERA3APC	±0.25	±15	470 to 100 k (E24,E96)		
				ERA3APB	±0.1				
				ERA3ARC	±0.25	±10	1 k to 100 k (E24,E96)		
				ERA3ARB	±0.1				
				ERA3ARW	±0.05				
ERA6A (0805)	0.125	100	200	ERA6AHD	±0.5	±50	10 to 46.4 (E24,E96)		Grade 0
				ERA6AED	±0.5	±25	47 to 1 M (E24,E96)		
				ERA6AEC	±0.25				
				ERA6AEB	±0.1				
				ERA6APC	±0.25	±15	470 to 100 k (E24,E96)		
				ERA6APB	±0.1				
				ERA6ARC	±0.25	±10	1 k to 100 k (E24,E96)		
				ERA6ARB	±0.1				
				ERA6ARW	±0.05				
ERA8A (1206)	0.25	150	300	ERA8AHD	±0.5	±50	10 to 46.4 (E24,E96)		Grade 0
				ERA8AED	±0.5	±25	47 to 1 M (E24,E96)		
				ERA8AEC	±0.25				
				ERA8AEB	±0.1				
				ERA8APC	±0.25	±15	470 to 100 k (E24,E96)		
				ERA8APB	±0.1				
				ERA8ARC	±0.25	±10	1 k to 100 k (E24,E96)		
				ERA8ARB	±0.1				
				ERA8ARW	±0.05				

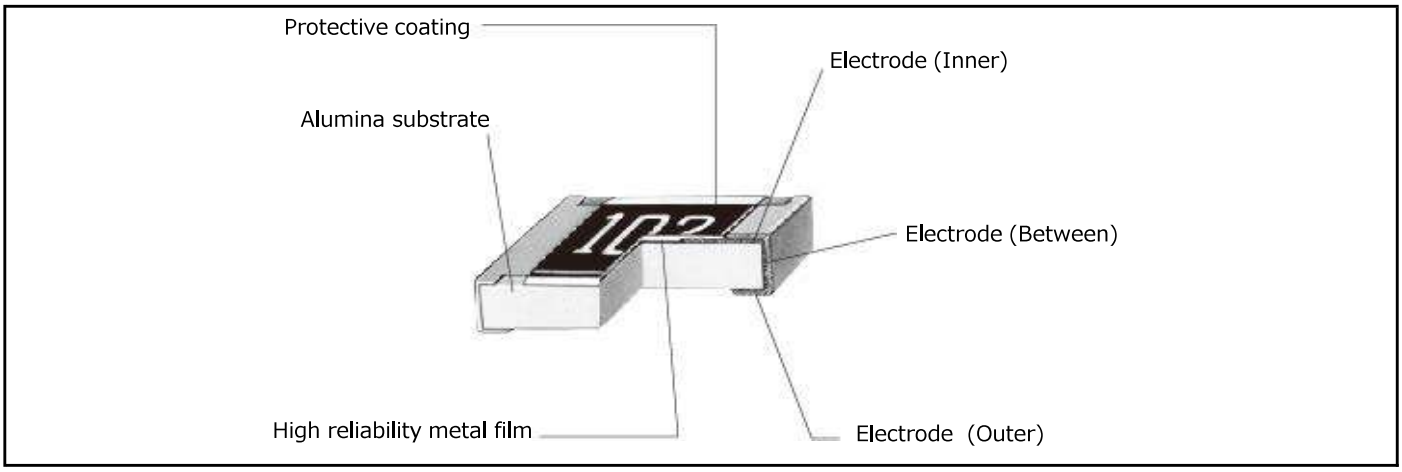
(1) Use it on the condition that the case temperature is below the upper category temperature.
(2) Rated Continuous Working Voltage (RCWV) shall be determined from RCWV=√Power Rating × Resistance Values, or Limiting Element Voltage listed above, whichever less.
(3) Overload Test Voltage (OTV) shall be determined from OTV=Specified Magnification (2.5) × RCWV or Maximum Overload Voltage listed above, whichever less.
(4) E192 series resistance values are also available. Please contact us for details.
(5) Duplicated resistance values between E96, E192 and E24 series shall follow E24 Part Numbers. (apply three digit resistance value)

Power Derating Curve

For resistors operated in ambient temperatures above 85 °C, power rating shall be derated in accordance with the figure on the right.

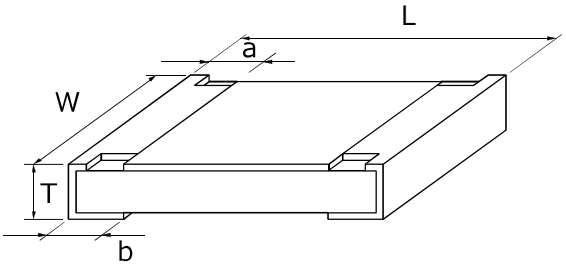


Construction



*0402 size, 0603 size and E96 series do not have value markings.

Dimensions in mm (not to scale)



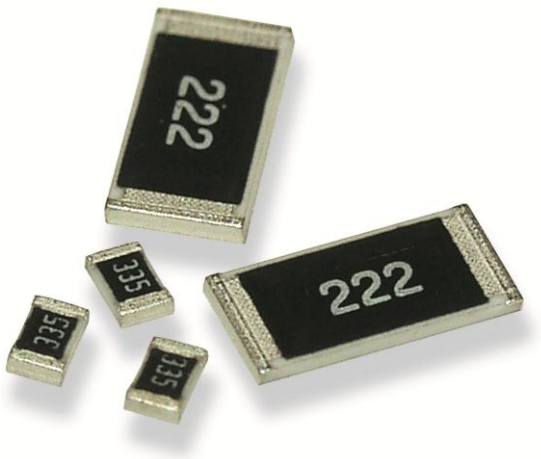
Part No.	Dimensions (mm)					Mass (Weight)
	L	W	a	b	T	(g/1000 pcs)
ERA1A	0.60±0.03	0.30±0.03	0.15±0.05	0.15±0.05	0.23±0.03	0.14
ERA2A	1.00±0.10	0.50+0.10/-0.05	0.15±0.10	0.25±0.10	0.35±0.05	0.6
ERA3A	1.60±0.20	0.8±0.20	0.30±0.20	0.30±0.15	0.45±0.10	2
ERA6A	2.00±0.20	1.25±0.10	0.40±0.25	0.40±0.25	0.60±0.10	4
ERA8A	3.20±0.20	1.60+0.05/-0.15	0.50±0.25	0.50±0.25	0.60±0.10	8

PRODUCT SPECIFICATION

Description: CRGH Series High Power Thick Film Chip Resistors

Product Type: (Resistance range: 1.0Ω ~ 10MΩ)

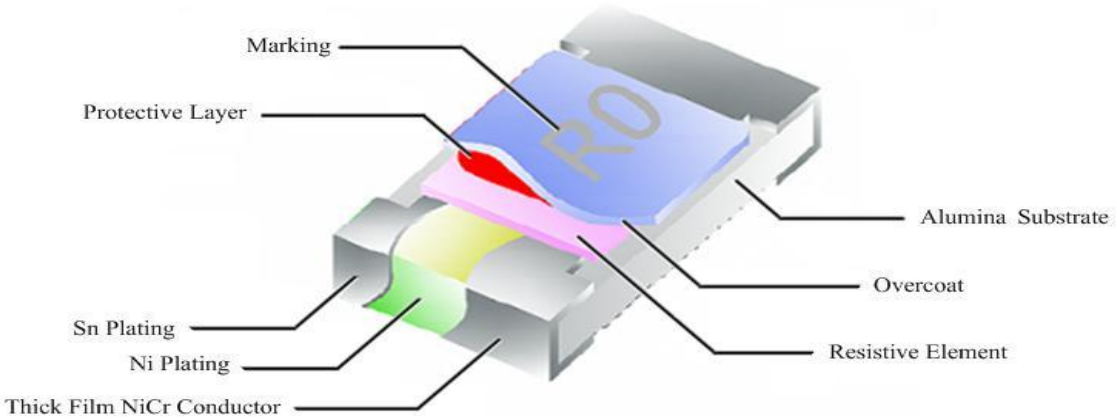
CRGH0603_XXX	(CRGH0603 1/5W +/- 1% & 5% Taped)
CRGH0805_XXX	(CRGH0805 1/3W +/- 1% & 5% Taped)
CRGH1206_XXX	(CRGH1206 1/2W +/- 1% & 5% Taped)
CRGH2010JXXX	(CRGH2010 1W +/- 1% & 5% Taped)
CRGH2512JXXX	(CRGH2512 2W +/- 1% & 5% Taped)



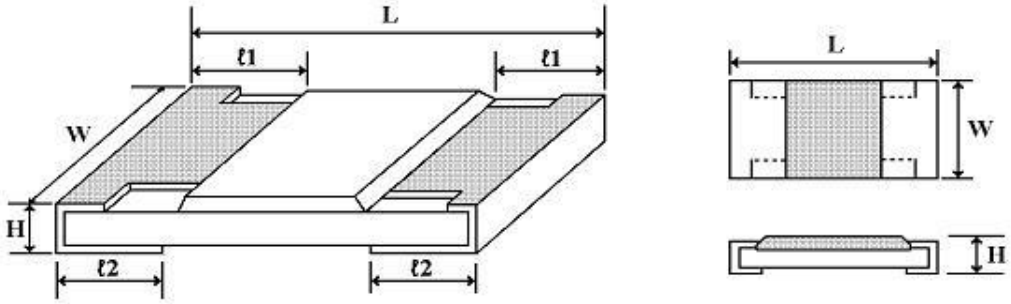
Parts corresponding to RoHS Compliant: 2005-Apr.-1

High Power Thick Film Chip Resistors

4. Construction :



5. Power rating and dimensions



Dimension :

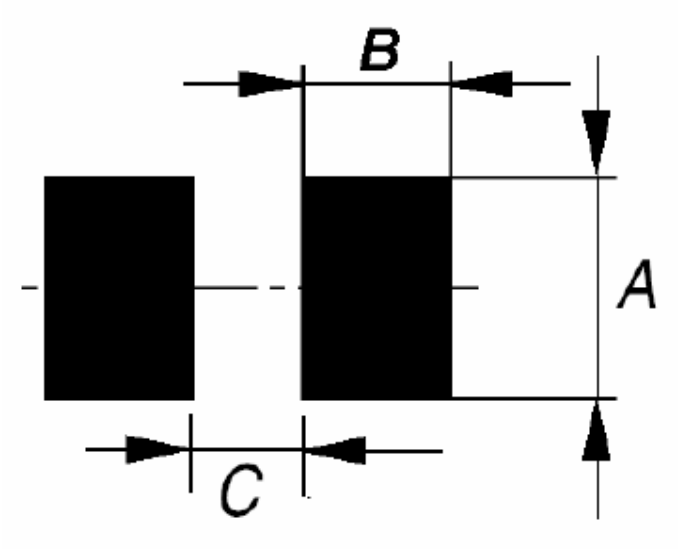
Type	Dimension (mm)				
	L	W	H	ℓ1	ℓ2
CRGH0603	1.60 ± 0.10	0.80 + 0.15 - 0.10	0.45 ± 0.10	0.30 ± 0.20	0.30 ± 0.20
CRGH0805	2.00 ± 0.15	1.25 + 0.15 - 0.10	0.55 ± 0.10	0.40 ± 0.20	0.40 ± 0.20
CRGH1206	3.10 ± 0.15	1.55 + 0.15 - 0.10	0.55 ± 0.10	0.45 ± 0.20	0.45 ± 0.20
CRGH2010	5.00 ± 0.20	2.50 ± 0.15	0.55 ± 0.10	0.60 ± 0.25	0.50 ± 0.20
CRGH2512	6.35 ± 0.10	3.20 ± 0.15	0.55 ± 0.10	0.60 ± 0.25	1.80 ± 0.20

Power Rating :

Type	Power Rating at 70°C	Tolerance %	Resistance Range	Standard Series	TCR
CRGH0603	0.20W	± 1	1Ω ~ 10MΩ	E-96	≤ 10Ω ±200PPM/°C < 10Ω ±100PPM/°C
		± 5	1Ω ~ 10MΩ	E-24	
CRGH0805	0.33W	± 1	1Ω ~ 10MΩ	E-96	≤ 10Ω ±200PPM/°C <
		± 5	1Ω ~ 10MΩ	E-24	
CRGH1206	0.50W	± 1	1Ω ~ 10MΩ	E-96	≤ 10Ω ±200PPM/°C <
		± 5	1Ω ~ 10MΩ	E-24	
CRGH2010	1.00W	± 1	1Ω ~ 10MΩ	E-24	< 10Ω ±200PPM/°C <
		± 5	1Ω ~ 10MΩ		
CRGH2512	2.00W	± 1	1Ω ~ 9.76Ω	E-96	< 10Ω ±200PPM/°C <
		± 5	1.1MΩ ~ 10MΩ	E-24	

High Power Thick Film Chip Resistors

5.1 PCB Layout Plan:



Dimension :

Type	Dimension (mm)		
	A	B	C
CRGH0603	1.00	1.00	0.60
CRGH0805	1.30	1.20	1.00
CRGH1206	1.80	1.20	2.20
CRGH2010	3.00	1.50	3.80
CRGH2512	3.50	1.90	5.00

High Power Thick Film Chip Resistors

6. Marking :

6.1 Resistors

A. ± 5% Tolerance : the first two digits are significant figures of resistance and the third denoted number of zeros.

Ex. | | 333 | | 33KΩ

B. For ohmic values below 10 Ω, read letter "R" as decimal point.

Ex. | | 2R2 | | 2.2Ω

C. For E-96 series [±1% (F) tolerance] in CRGH0603 size 3 digit system (due to space restrictions) please refer to page 4. for coding formula

Ex. | | 02C | | 10.2KΩ

D. ±1% Toler CRGH0805_XXX (CRGH0805 1/3W +/- 1% & 5% Taped) resistance and the fourth digit denoted number of zeros. Letter"R" is for decimal point.

Ex. | CRGH | 2701 | | 2.7KΩ

| | 10R5 | | 10.5Ω

6.2 Labels

Label shall be marked with the following item :

Label shall be marked with the following item :

A. Nominal Resistance and Resistance Tolerance
B. Power Rating and Size
C. Quantity
D. Part No.
E. P.O.No.
F. Lot No.

Ex.

tyco / Electronics
CHIP RESISTORS
NEOHM

RESISTANCE:	330K	Ω	± 5 %
WATTAGE:	1/2W	SIZE:	CRGH0603
QUANTITY:	5,000	PCS	Pb-Free
PART NO.:	CRGH0603F330K	RoHS	2002/95/EC
LOT NO. :	825723	REF #	2456319325

Remark : **For CRGH0603** ± 1 % : Label is 332K, value is 332KΩ, marking is 51D
± 5 % : Label is 330K, value is 330KΩ, marking is 334
± 1 % : Label is 330K, value is 330KΩ, marking is 3303

High Power Thick Film Chip Resistors

Mutiplier Code :

Code	A	B	C	D	E	F	G	H	X	Y	Z
	0	1	2	3	4	5	6	7	-1	-2	-3
Multiplier	10	10	10	10	10	10	10	10	10	10	10

Coding

XX

Resistance Code

Formula

X

Multiplier Code

Example :

10K2 = 102 X 10^{2} = 02C

102 → 02, 10^{2} → C

33R2 = 332 X 10^{-1} = 51X

332 → 51, 10^{-1} → X

Value	Code	Value	Code	Value	Code	Value	Code	Value	Code
100	**01**	162	**21**	261	**41**	422	**61**	681	**81**
102	**02**	165	**22**	267	**42**	432	**62**	698	**82**
105	**03**	169	**23**	274	**43**	442	**63**	715	**83**
107	**04**	174	**24**	280	**44**	453	**64**	732	**84**
110	**05**	178	**25**	287	**45**	464	**65**	750	**85**
113	**06**	182	**26**	294	**46**	475	**66**	768	**86**
115	**07**	187	**27**	301	**47**	487	**67**	787	**87**
118	**08**	191	**28**	309	**48**	499	**68**	806	**88**
121	**09**	196	**29**	316	**49**	511	**69**	825	**89**
124	**10**	200	**30**	324	**50**	523	**70**	845	**90**
127	**11**	205	**31**	332	**51**	536	**71**	866	**91**
130	**12**	210	**32**	340	**52**	549	**72**	887	**92**
133	**13**	215	**33**	348	**53**	562	**73**	909	**93**
137	**14**	221	**34**	357	**54**	576	**74**	931	**94**
140	**15**	226	**35**	365	**55**	590	**75**	953	**95**
143	**16**	232	**36**	374	**56**	604	**76**	976	**96**
147	**17**	237	**37**	383	**57**	619	**77**		
150	**18**	243	**38**	392	**58**	634	**78**		
154	**19**	249	**39**	402	**59**	649	**79**		
158	**20**	255	**40**	412	**60**	665	**80**		

*Marking for CRGH0603 E-96 series, the resistance value that no have multiplier code indicate marking follow this:
The first two digits are significant figures of resistance and the third one denoted number of zeros
and under line the marking letters.

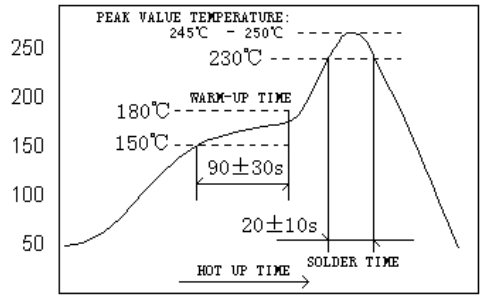
Ex.

	122	

1.2KΩ

High Power Thick Film Chip Resistors

7. Performance specification :

Characteristics	Limits	Test Methods (JIS C 5201-1)
Dielectric withstanding voltage	No evidence of flashover mechanical damage, arcing or insulation break down	4.7 Clamped in the trough of a 90°C metallic v-block and shall be tested at ac potential respectively specified in the type for 60-70 seconds
Temperature Coefficient	See Page 2	4.8 Natural resistance change per temp. degree centigrade. $\frac{R2-R1}{R1(t2-t1)} \times 10^6$ (PPM/°C) R1: Resistance value at room temperature (T1) R2: Resistance value at room temp. plus 100°C (T2) Test pattern: room temp. (T1), room temp. +100°C (T2)
Short time Overload	Resistance change rate is ± 5% (2.0% + 0.1Ω) Max. ± 1% (1.0% + 0.1Ω) Max.	4.13 Permanent resistance change after the application of a potential of 2.5 times RCWV for 5 seconds.
Solderability	95 % coverage Min.	Wave Solder: Test temperature of solder: 245°C ±3°C dipping time in solder : 2-3 seconds. Reflow Solder: 
Soldering heat	Resistance change rate is: ±(1%+0.05Ω) Max.	4.18 Dip the resistor into a solder bath having a temperature of 260°C ± 3°C and hold it for 10 ± 1 seconds.
Temperature cycling	Resistance Change Rate Is ± 5% (1.0% + 0.05Ω) Max. ± 1% (0.5% + 0.05Ω) Max.	4.19 Resistance change after continuous 5 cycles for duty cycle specified below :

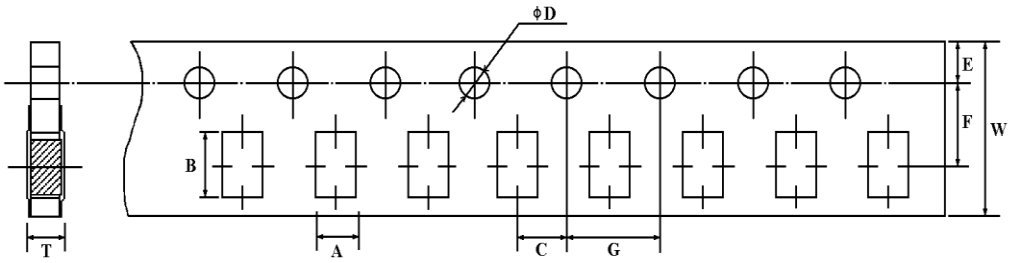
Step	Temperature	Time
1	-55°C ± 3°C	30 mins
2	Room temp.	10 ~ 15 mins
3	+155°C ± 2°C	30 mins
4	Room temp.	10 ~ 15 mins

Humidity	Resistance change rate is ± 5% (3.0% + 0.1Ω) Max. ± 1% (1.0% + 0.1Ω) Max.	4.24 Temporary resistance change after 240 hours exposure in a humidity test chamber controlled at 40±2°C and 90-95% relative humidity
Load life in Humidty	Resistance change rate is ± 5% (3.0% + 0.1Ω) Max. ± 1% (1.0% + 0.1Ω) Max.	7.9 Resistance change after 1,000 hours (1.5 hours "on", 0.5 hour "off") at RCWV in a humidity chamber controlled at 40°C ± 2°C and 90 to 95% relative humidity
Load Life	Resistance change rate is ± 5% (3.0% + 0.1Ω) Max. ± 1% (1.0% + 0.1Ω) Max.	4.25.1 Permanent resistance change after 1,000 hours operating at RCWV, with duty cycle of (1.5 hours"on", 0.5 hour"off") at 70°C ± 2°C ambient
Terminal Bending	Resistance change rate is ± (1.0% + 0.05Ω) Max.	4.33 Twist of Test Board : Y/X = 3/90 mm for 60 seconds

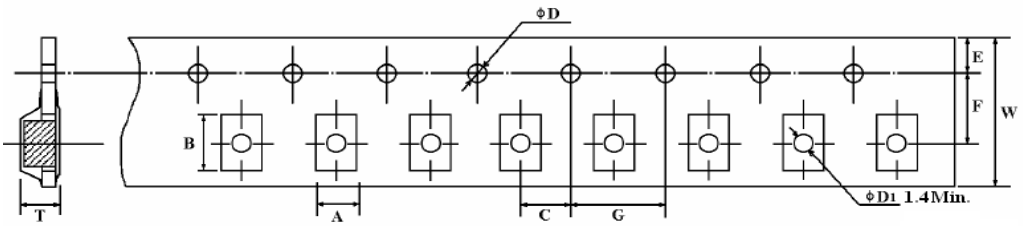
6. Packing specification :

6.1 Taping Dimension (mm)

A. Paper tape



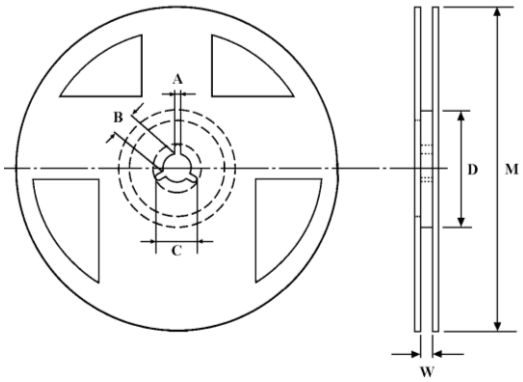
B. Plastic tape



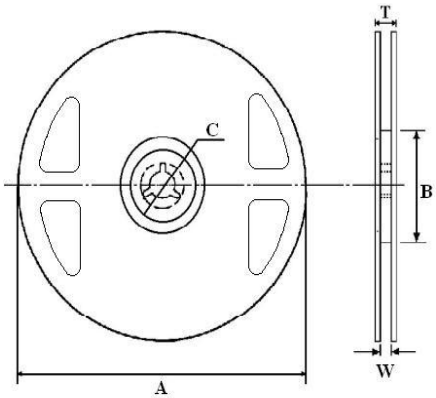
Type	A ± 0.2	B ± 0.2	C ± 0.05	ϕ D +0.1 - 0	E ± 0.1	F ± 0.05	G ± 0.1	W ± 0.2	T ± 0.1
CRGH0603	1.10	1.90	2.0	1.5	1.75	3.5	4.0	8.0	0.67
CRGH0805	1.65	2.40	2.0	1.5	1.75	3.5	4.0	8.0	0.81
CRGH1206	2.00	3.60	2.0	1.5	1.75	3.5	4.0	8.0	0.81
CRGH2010	2.80	5.50	2.0	1.5+0.25	1.75	5.5	4.0	12.0	1.2±0.0
CRGH2512	3.60	6.90	2.0	1.5+0.25	1.75	5.5	4.0	12.0	1.2±0.0

7.2 Reel Dimension (mm)

A. Paper tape



B. Plastic tape



Type	Packaging	Quantity Per Reel	A	B	C	D	M ± 2	W ± 1	T ± 1
CRGH0603	Paper	5,000 pcs.	2±0.5	13±0.5	21±0.5	60±1.0	178±2.0	10±1.0	-
CRGH0805	Paper	5,000 pcs.	2±0.5	13±0.5	21±0.5	60±1.0	178±2.0	10±1.0	-
CRGH1206	Paper	5,000 pcs.	2±0.5	13±0.5	21±0.5	60±1.0	178±2.0	10±1.0	-
CRGH2010	Plastic	4,000 pcs.	180-3.0	60+1.0	13±0.2	-	-	13.5±0.5	15.4±1.0
CRGH2512	Plastic	4,000 pcs.	180-3.0	60+1.0	13±0.2	-	-	13.5±0.5	15.4±1.0

Precision Thick Film Chip Resistors

Series: ERJ XG, 1G
ERJ 1R, 2R, 3R, 6R
ERJ 3E, 6E, 8E, 14, 12, 1T

Features

- Small size and lightweight
- High reliability…Metal glaze thick film resistive element and three layers of electrodes
- Compatible with placement machines … Taping packaging available
- Suitable for both reflow and flow soldering
- Low Resistance Tolerance : ERJXG, 1G, 2R, 3E, 6E, 8E, 14, 12, 1T : ±1 %
  ERJ1R, 2R, 3R, 6R : ±0.5 %
- Reference Standard … IEC 60115-8, JIS C 5201-8, JEITA RC-2134C
- AEC-Q200 compliant (except ERJXG, ERJ1R)
- RoHS compliant

■ **As for Packaging Methods, Land Pattern, Soldering Conditions and Safety Precautions,**
Please see Data Files

Explanation of Part Numbers

- Series ERJ1R, 2R, 3R, 6R, ±0.5 %

1	2	3	4	5	6	7	8	9	10	11	12
E	R	J	3	R	B	D	1	0	0	2	V

Product Code

Thick Film Chip Resistors

Size, Power Rating

Code	inch	Power Rating
1R	0201	0.05 W
2R	0402	0.063 W
3R	0603	0.1 W
6R	0805	0.1 W

T.C.R., Marking

Code	T.C.R.
H	±50 ×10^{-6}/K (1R, 2R)
B	±50 ×10^{-6}/K (3R, 6R)
K	±100 ×10^{-6}/K (2R)
E	±100 ×10^{-6}/K (3R, 6R)

Resistance Tolerance

Code	Tolerance
D	±0.5 %

Resistance Value

The first three digits are significant figures of resistance and the last one denotes number of zeros following.
(Ex.) 1002: 10 KΩ

Packaging Methods

Code	Packaging	Part No.
C	Pressed Carrier Taping 2 mm pitch, 15,000 pcs	ERJ1R
X	Punched Carrier Taping 2 mm pitch, 10,000 pcs	ERJ2R
V	Punched Carrier Taping 4 mm pitch, 5,000 pcs	ERJ3R ERJ6R

● Series ERJXGN, 1GN, 2RC, 2RK, 3EK, 6EN, 8EN, 14N, 12N, 12S, 1TN, ±1 %

1	2	3	4	5	6	7	8	9	10	11	12
E	R	J	8	E	N	F	1	0	0	2	V

Product Code

Thick Film Chip Resistors

Size, Power Rating

Code	inch	Power Rating
XGN	01005	0.031 W
1GN	0201	0.05 W
2RC	0402	0.1 W
2RK	0402	0.1 W
3EK	0603	0.1 W
6EN	0805	0.125 W
8EN	1206	0.25 W
14N	1210	0.5 W
12N	1812	0.75 W
12S	2010	0.75 W
1TN	2512	1 W

Resistance Tolerance

Code	Tolerance
F	±1 %

Resistance Value

The first three digits are significant figures of resistance and the last one denotes number of zeros following. Decimal point is expressed by "R".
(Ex.) 1002: 10 kΩ

Packaging Methods

Code	Packaging	Part No.
Y	Pressed Carrier Taping W8P2, 20,000 pcs	ERJXGN
U	Embossed Carrier Taping W4P1, 40,000 pcs	ERJXGN
C	Pressed Carrier Taping 2 mm pitch, 15,000 pcs	ERJ1GN
X	Punched Carrier Taping 2 mm pitch, 10,000 pcs	ERJ2RC ERJ2RK
V	Punched Carrier Taping 4 mm pitch, 5,000 pcs	ERJ3EK ERJ6EN ERJ8EN
U	Embossed Carrier Taping 4 mm pitch, 5,000 pcs	ERJ14N ERJ12N ERJ12S
	Embossed Carrier Taping 4 mm pitch, 4,000 pcs	ERJ1TN

Ratings

<±0.5 %>

Part No. (inch size)	Power Rating at 70 °C (1) (W)	Limiting Element Voltage(2) (V)	Maximum Overload Voltage(3) (V)	Resistance Tolerance (%)	Resistance Range (Ω)		T.C.R. ($\times 10^{-6}$/K)	Category Temperature Range (℃)	AEC-Q200 Grade
ERJ1RH (0201)	0.05	15	30	±0.5	1 k to 1 M	(E24,E96)	±50	-55 to +125	-
ERJ2RH (0402)	0.063	50	100	±0.5	100 to 100 k	(E24,E96)	±50	-55 to +155	Grade 0
ERJ2RK (0402)	0.063	50	100	±0.5	10 to 97.6 102 k to 1 M	(E24,E96)	±100	-55 to +155	Grade 0
ERJ3RB (0603)	0.1	50	100	±0.5	100 to 100 k	(E24,E96)	±50	-55 to +155	Grade 0
ERJ3RE (0603)	0.1	50	100	±0.5	10 to 97.6 102 k to 1 M	(E24,E96)	±100	-55 to +155	Grade 0
ERJ6RB (0805)	0.1	150	200	±0.5	100 to 100 k	(E24,E96)	±50	-55 to +155	Grade 0
ERJ6RE (0805)	0.1	150	200	±0.5	10 to 97.6 102 k to 1 M	(E24,E96)	±100	-55 to +155	Grade 0

(1) Use it on the condition that the case temperature is below the upper category temperature.

(2) Rated Continuous Working Voltage (RCWV) shall be determined from RCWV=$\sqrt{\text{Power Rating} \times \text{Resistance Value}}$, or Limiting Element Voltage listed above, whichever less.

(3) Overload Test Voltage (OTV) shall be determined from OTV=Specified Magnification (refer to performance) × RCWV or Maximum Overload Voltage listed above, whichever less.

Ratings

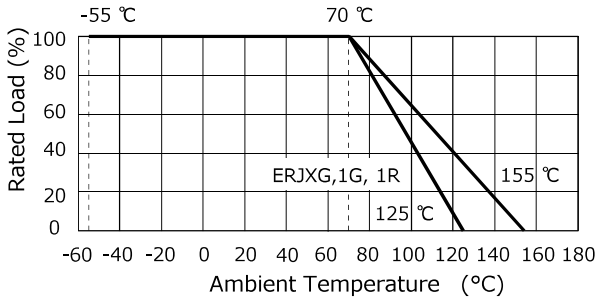
<±1 %>

Part No. (inch size)	Power Rating at 70 °C (1) (W)	Limiting Element Voltage(2) (V)	Maximum Overload Voltage(3) (V)	Resistance Tolerance (%)	Resistance Range (Ω)	T.C.R. ($\times 10^{-6}$/K)	Category Temperature Range (℃)	AEC-Q200 Grade
ERJXGN (01005)	0.031	15	30	±1	10 to 1 M (4) (E24,E96)	R<100 Ω : ±300 100 Ω ≤R : ±200	-55 to +125	-
ERJ1GN (0201)	0.05	25	50	±1	10 to 1 M (4) (E24,E96)	±200	-55 to +125	Grade 1
ERJ2RC (0402)	0.1	50	100	±1	1 to 9.76 (E24,E96)	−100 to +600	-55 to +155	Grade 0
ERJ2RK (0402)	0.1	50	100	±1	10 to 1 M (E24,E96)	±100	-55 to +155	Grade 0
ERJ3EK (0603)	0.1	75	150	±1	10 to 1 M (E24,E96)	±100	-55 to +155	Grade 0
ERJ6EN (0805)	0.125	150	200	±1	10 to 2.2 M (E24,E96)	±100	-55 to +155	Grade 0
ERJ8EN (1206)	0.25	200	400	±1	10 to 2.2 M (E24,E96)	±100	-55 to +155	Grade 0
ERJ14N (1210)	0.5	200	400	±1	10 to 1 M (E24,E96)	±100	-55 to +155	Grade 0
ERJ12N (1812)	0.75	200	500	±1	10 to 1 M (E24,E96)	±100	-55 to +155	Grade 0
ERJ12S (2010)	0.75	200	500	±1	10 to 1 M (E24,E96)	±100	-55 to +155	Grade 0
ERJ1TN (2512)	1	200	500	±1	10 to 1 M (E24,E96)	±100	-55 to +155	Grade 0

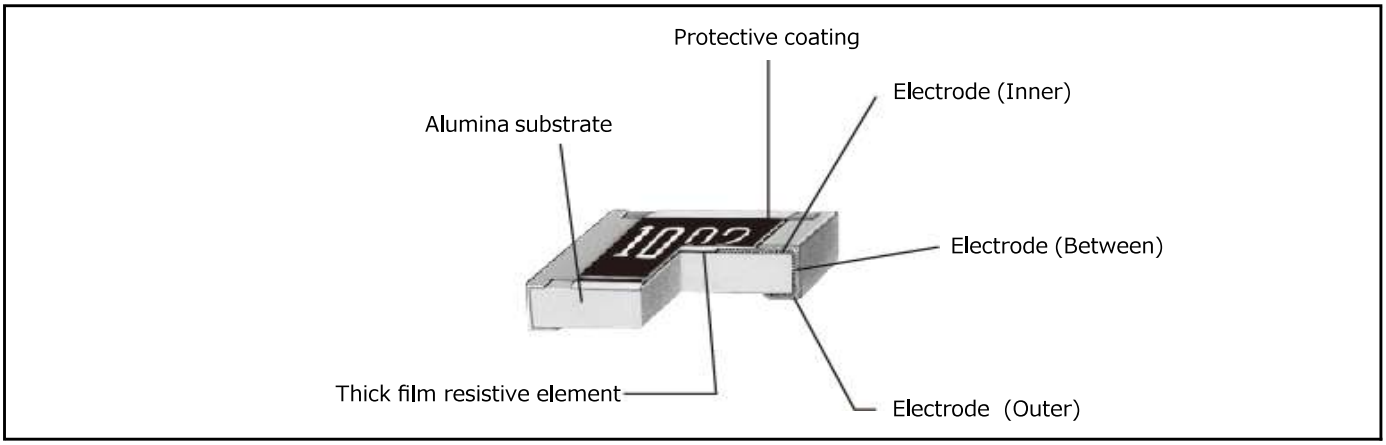
(1) Use it on the condition that the case temperature is below the upper category temperature.
(2) Rated Continuous Working Voltage (RCWV) shall be determined from RCWV=$\sqrt{\text{Power Rating} \times \text{Resistance Value}}$, or Limiting Element Voltage listed above, whichever less.
(3) Overload Test Voltage (OTV) shall be determined from OTV=Specified Magnification (refer to performance) × RCWV or Maximum Overload Voltage listed above, whichever less.
(4) Please contact us when you need a type with a resistance of less than 10 Ω.

Power Derating Curve

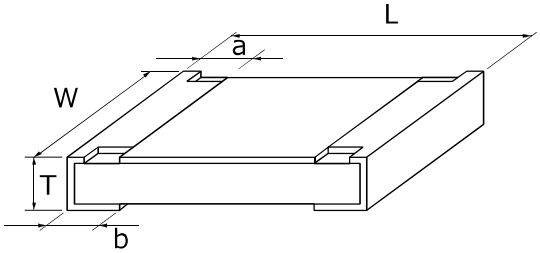
For resistors operated in ambient temperatures above 70 °C, power rating shall be derated in accordance with the figure on the right.



Construction



Dimensions in mm (not to scale)



Part No.	Dimensions (mm)					Mass (Weight) (g/1000 pcs)
	L	W	a	b	T	
ERJXGN	0.40±0.02	0.20±0.02	0.10±0.03	0.10±0.03	0.13±0.02	0.04
ERJ1GN ERJ1R□	0.60±0.03	0.30±0.03	0.10±0.05	0.15±0.05	0.23±0.03	0.15
ERJ2R□	1.00±0.05	0.50±0.05	0.20±0.10	0.25±0.05	0.35±0.05	0.8
ERJ3R□ ERJ3EK	1.60±0.15	0.80+0.15/-0.05	0.30±0.20	0.30±0.15	0.45±0.10	2
ERJ6R□ ERJ6EN	2.00±0.20	1.25±0.10	0.40±0.20	0.40±0.20	0.60±0.10	4
ERJ8EN	3.20+0.05/-0.20	1.60+0.05/-0.15	0.50±0.20	0.50±0.20	0.60±0.10	10
ERJ14N	3.20±0.20	2.50±0.20	0.50±0.20	0.50±0.20	0.60±0.10	16
ERJ12N	4.50±0.20	3.20±0.20	0.50±0.20	0.50±0.20	0.60±0.10	27
ERJ12S	5.00±0.20	2.50±0.20	0.60±0.20	0.60±0.20	0.60±0.10	27
ERJ1TN	6.40±0.20	3.20±0.20	0.65±0.20	0.60±0.20	0.60±0.10	45

Performance

● Series ERJ1R, 2R, 3R, 6R, ±0.5 %(D)

Test Item	Performance Requirements ⊿R	Test Conditions
Resistance	Within Specified Tolerance	20 °C
T. C. R.	Within Specified T. C. R.	+25 °C/+125 °C
Overload	±2 %	Rated Voltage× 2.5, 5 s
Resistance to Soldering Heat	±1 %	270 °C, 10 s
Rapid Change of Temperature	±1 %	−55 °C (30 min.) / +155 °C (ERJ1R : +125 °C)(30 min.), 100 cycles
High Temperature Exposure	±1 %	+155 °C (ERJ1R : +125 °C), 1000 h
Damp Heat, Steady State	±1 %	60 °C, 90 % to 95 %RH, 1000 h
Load Life in Humidity	±2 % ERJ1R : ±3 %	60 °C, 90 % to 95 %RH, Rated Voltage, 1.5 h ON / 0.5 h OFF cycle, 1000 h
Endurance at 70 °C	±2 % ERJ1R : ±3 %	70 °C, Rated Voltage, 1.5 h ON / 0.5 h OFF cycle, 1000 h

● Series ERJXGN, 1GN, 2RC, 2RK, 3EK, 6EN, 8EN, 14N, 12N, 12S, 1TN, ±1 %(F)

Test Item	Performance Requirements ⊿R	Test Conditions
Resistance	Within Specified Tolerance	20 °C
T. C. R.	Within Specified T. C. R.	+25 °C/+155 °C (ERJXG,ERJ1G : +25℃/+125 °C)
Overload	±2 %	Rated Voltage× 2.5, 5 s
Resistance to Soldering Heat	±1 %	270 °C, 10 s
Rapid Change of Temperature	±1 %	−55 °C (30 min.)/+155 °C (ERJXG,ERJ1G : +125 °C)(30 min.), 100 cycles
High Temperature Exposure	±1 %	+155 °C (ERJXG,ERJ1G : +125 °C), 1000 h
Damp Heat, Steady State	±1 %	60 °C, 90 % to 95 %RH, 1000 h
Load Life in Humidity	±2 % ERJXG,1G : ±3 %	60 °C, 90 % to 95 %RH, Rated Voltage, 1.5 h ON / 0.5 h OFF cycle, 1000 h
Endurance at 70 °C	±2 % ERJXG,1G : ±3 %	70 °C, Rated Voltage, 1.5 h ON / 0.5 h OFF cycle, 1000 h

Innovative Service Around the Globe YAGEO

DATA SHEET

GENERAL PURPOSE CHIP RESISTORS

RC_L series

±0.1%, ±0.5%, ±1%, ±5%

Sizes 0075/0100/0201/0402/0603/0805/1206/1210/1218/2010/2512

RoHS compliant & Halogen free

YAGEO Phycomp

Product specification – January 22, 2016 V.4

SCOPE

This specification describes RC series chip resistors with lead free terminations made by thick film process.

APPLICATIONS

- All general purpose application

FEATURES

- Halogen Free Epoxy
- RoHS compliant
  - Products with lead free terminations meet RoHS requirements
  - Pb-glass contained in electrodes, resistors element and glass are exempted by RoHS
- Reducing environmentally hazardous wastes
- High component and equipment reliability
- Saving of PCB space
- None forbidden-materials used in products/production

ORDERING INFORMATION - GLOBAL PART NUMBER

Global part numbers are identified by the series, size, tolerance, packing type, temperature coefficient, taping reel and resistance value.

GLOBAL PART NUMBER

RC	XXXX	X	X	X	XX	XXXX	L
	(1)	(2)	(3)	(4)	(5)	(6)	(7)

(1) SIZE

0075/0100/0201/0402/0603/0805/1206/1210/1218/2010/2512

(2) TOLERANCE

B = ±0.1%
D = ±0.5%
F = ±1.0%
J = ±5.0% (for jumper ordering, use code of J)

(3) PACKAGING TYPE

R = Paper taping reel
K = Embossed taping reel
S = ESD safe reel (0075/0100 only)

(4) TEMPERATURE COEFFICIENT OF RESISTANCE

- = Based on spec.

(5) TAPING REEL

07= 7 inch dia. Reel
13=13 inch dia. Reel
7W = 7 inch dia. Reel & 2 x standard power
7N = 7 inch dia. Reel, ESD safe reel (0075/0100 only)

(6) RESISTANCE VALUE

There are 2~4 digits indicated the resistance value.
Letter R/K/M is decimal point
Example:
97R6 = 97.6Ω
9K76 = 9760Ω
1M = 1,000,000Ω

(7) DEFAULT CODE

Letter L is the system default code for ordering only.(Note)

ORDERING EXAMPLE

The ordering code for a RC0402 0.0625W chip resistor value 100KΩwith ±5% tolerance, supplied in 7-inch tape reel of 10,000 units per reel is: RC0402JR-07100KL.

NOTE

1. All our RSMD products meet RoHS compliant and Halogen Free. "LFP" of the internal 2D reel label mentions "Lead Free Process".
2. On customized label, "LFP" or specific symbol can be printed.

MARKING

RC0075 / RC0100 / RC0201 / RC0402

Fig. 1

No Marking

RC0603

Fig. 2 Value = 10 KΩ

E24 series: 3 digits
First two digits for significant figure and 3rd digit for number of zeros

RC0805 / RC1206 / RC1210 / RC2010 / RC2512

Fig. 3 Value = 10 KΩ

E24/E96 series: 4 digits
First three digits for significant figure and 4th digit for number of zeros

RC1218

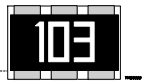


Fig. 4 Value = 10 KΩ

E-24 series: 3 digits, ±5%
First two digits for significant figure and 3rd digit for number of zeros

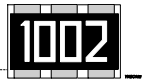


Fig. 5 Value = 10 KΩ

Both E-24 and E-96 series: 4 digits, ±1% & ±0.5%
First three digits for significant figure and 4th digit for number of zeros

For further marking information, please see special data sheet "Chip resistors marking".

CONSTRUCTION

The resistor is constructed on top of a high-grade ceramic body. Internal metal electrodes are added on each end to make the contacts to the thick film resistive element. The composition of the resistive element is a noble metal imbedded into a glass and covered by a second glass to prevent environmental influences. The resistor is laser trimmed to the rated resistance value. The resistor is covered with a protective epoxy coat, finally the two external terminations (matte tin on Nibarrier) are added, as shown in Fig.4.

Outlines

For dimensions, please refer to Table 1

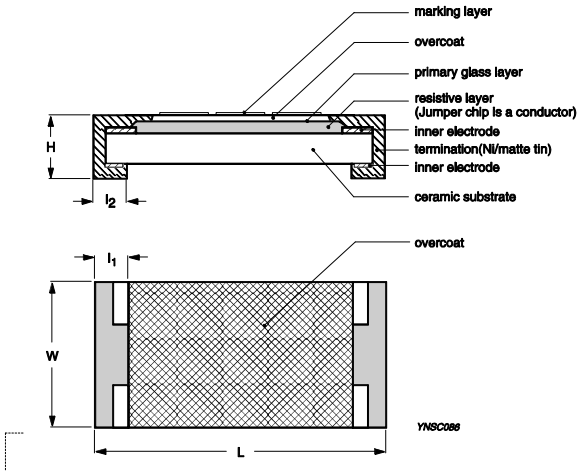


Fig. 4 Chip resistor outlines

DIMENSION

Table 1

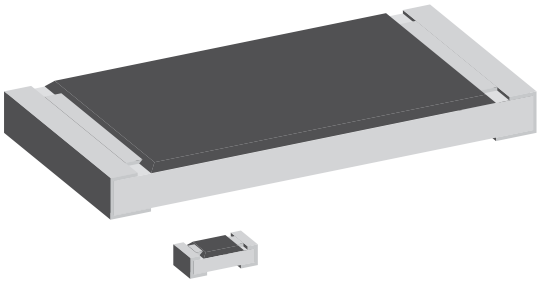
TYPE	L (mm)	W (mm)	H (mm)	I_1 (mm)	I_2 (mm)
RC0075	0.30±0.01	0.15±0.01	0.10±0.01	0.08±0.03	0.08±0.03
RC0100	0.40±0.02	0.20±0.02	0.13±0.02	0.10±0.03	0.10±0.03
RC0201	0.60±0.03	0.30±0.03	0.23±0.03	0.10±0.05	0.15±0.05
RC0402	1.00±0.05	0.50±0.05	0.35±0.05	0.20±0.10	0.25±0.10
RC0603	1.60±0.10	0.80±0.10	0.45±0.10	0.25±0.15	0.25±0.15
RC0805	2.00±0.10	1.25±0.10	0.50±0.10	0.35±0.20	0.35±0.20
RC1206	3.10±0.10	1.60±0.10	0.55±0.10	0.45±0.20	0.40±0.20
RC1210	3.10±0.10	2.60±0.15	0.50±0.10	0.45±0.15	0.50±0.20
RC1218	3.10±0.10	4.60±0.10	0.55±0.10	0.45±0.20	0.40±0.20
RC2010	5.00±0.10	2.50±0.15	0.55±0.10	0.45±0.15	0.50±0.20
RC2512(1W)	6.35±0.10	3.10±0.15	0.55±0.10	0.60±0.20	0.50±0.20
RC2512(2W)	6.35±0.10	3.10±0.15	0.55±0.10	0.60±0.20	1.15±0.20

ELECTRICAL CHARACTERISTICS

Table 2

CHARAC-TERISTICS	POWER	OPERATING TEMPERATURE RANGE	MAXIMUM WORKING VOLTAGE	MAXIMUM OVERLOAD VOLTAGE	DIELECTRIC WITHSTANDING VOLTAGE	RESISTANCE RANGE	TEMPERATURE COEFFICIENT	JUMPER CRITERIA
RC0075	1/50 W	-55°C to 125°C	10V	25V	25V	5% (E24) 10Ω≦R≦1MΩ 1% (E24/E96) 10Ω≦R≦1MΩ Jumper<50mΩ	10Ω≦R<100Ω -200~+600ppm°C 100Ω≦R≦1MΩ ±200ppm°C	Rated Current 0.5A Maximum Current 1.0A
RC0100	1/32 W	-55°C to 125°C	15V	30V	30V	5% (E24) 1Ω≦R≦22MΩ 1% (E24/E96) 1Ω≦R≦10MΩ 0.5% (E24/E96) 33Ω≦R≦470KΩ Jumper<50mΩ	1Ω≦R<10Ω -200~+600ppm°C 10Ω≦ R < 100Ω: ±300ppm/°C 100Ω≦ R ≦ 10MΩ: ±200ppm/°C 10MΩ< R ≦ 22MΩ: ±250ppm/°C	Rated Current 0.5A Maximum Current 1.0A
RC0201	1/20 W	-55°C to 125°C	25V	50V	50V	5% (E24) 1Ω≦R≦10MΩ 1% (E24/E96) 1Ω≦R≦10MΩ 0.1%, 0.5% (E24/E96) 10Ω≦R≦1MΩ Jumper<50mΩ	1Ω≦R≦10Ω -100~+350ppm°C 10Ω<R≦10MΩ ±200ppm°C	Rated Current 0.5A Maximum Current 1.0A

Standard Thick Film Chip Resistors



D/CRCW e3 standard thick film chip resistors are the perfect choice for most fields of modern electronics where high reliability and stability are of major concern. Typical applications include automotive, telecommunications, and industrial.

FEATURES

- Stability at different environmental conditions $\Delta R/R \leq 1$ % (1000 h rated power at 70 °C)
- 2 mm pitch packaging option for 0603 size
- AEC-Q200 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Automotive
- Industrial
- Telecommunication

TECHNICAL SPECIFICATIONS

DESCRIPTION	D10/CRCW0402 e3	D11/CRCW0603 e3	D12/CRCW0805 e3	D25/CRCW1206 e3	CRCW1210 e3	CRCW1218 e3	CRCW2010 e3	CRCW2512 e3
Imperial size	0402	0603	0805	1206	1210	1218	2010	2512
Metric size code	RR1005M	RR1608M	RR2012M	RR3216M	RR3225M	RR3246M	RR5025M	RR6332M
Resistance range	1 Ω to 10 MΩ; jumper (0 Ω)					1 Ω to 2.2 MΩ; jumper (0 Ω)	1 Ω to 10 MΩ; jumper (0 Ω)	
Resistance tolerance	± 5 %; ± 1 %							
Temperature coefficient	± 200 ppm/K; ± 100 ppm/K							
Rated dissipation, P_{70} (1)	0.063 W	0.10 W	0.125 W	0.25 W	0.5 W	1.0 W	0.75 W	1.0 W
Operating voltage, $U_{max.}$ AC_{RMS}/DC	50 V	75 V	150 V	200 V	200 V	200 V	400 V	500 V
Permissible film temperature, $\vartheta_{F\ max.}$ (1)	155 °C							
Operating temperature range	-55 °C to +155 °C							
Max. resistance change at P_{70} for resistance range, $\lvert\Delta R/R\rvert$, after (2):								
1000 h	≤ 1 %							
8000 h	≤ 2 %							
Permissible voltage against ambient (insulation):								
1 min, U_{ins}	75 V	100 V	200 V	300 V	300 V	300 V	300 V	300 V

Notes
(1) Please refer to "Application Information" below
(2) Apply to components with stability class 1

APPLICATION INFORMATION

When the resistor dissipates power, a temperature rise above the ambient temperature occurs, dependent on the thermal resistance of the assembled resistor together with the printed circuit board. The rated dissipation applies only if the permitted film temperature is not exceeded.

These resistors do not feature a limited lifetime when operated within the permissible limits. However, resistance value drift increasing over operating time may result in exceeding a limit acceptable to the specific application, thereby establishing a functional lifetime.

TEMPERATURE COEFFICIENT AND RESISTANCE RANGE				
TYPE / SIZE	**TCR**	**TOLERANCE**	**RESISTANCE**	**E-SERIES**
D10/CRCW0402 e3	± 200 ppm/K	± 5 %	1 Ω to 10 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 10 MΩ	E24; E96
	Jumper, $I_{max.}$ = 1.5 A	≤ 20 mΩ	0 Ω	-
D11/CRCW0603 e3	± 200 ppm/K	± 5 %	1 Ω to 10 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 10 MΩ	E24; E96
	Jumper, $I_{max.}$ = 2.0 A	≤ 20 mΩ	0 Ω	-
D12/CRCW0805 e3	± 200 ppm/K	± 5 %	1 Ω to 10 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 10 MΩ	E24; E96
	Jumper, $I_{max.}$ = 2.5 A	≤ 20 mΩ	0 Ω	-
D25/CRCW1206 e3	± 200 ppm/K	± 5 %	1 Ω to 10 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 10 MΩ	E24; E96
	Jumper, $I_{max.}$ = 3.5 A	≤ 20 mΩ	0 Ω	-
CRCW1210 e3	± 200 ppm/K	± 5 %	1 Ω to 10 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 10 MΩ	E24; E96
	Jumper, $I_{max.}$ = 5.0 A	≤ 20 mΩ	0 Ω	-
CRCW1218 e3	± 200 ppm/K	± 5 %	1 Ω to 2.2 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 2.2 MΩ	E24; E96
	Jumper, $I_{max.}$ = 7.0 A	≤ 20 mΩ	0 Ω	-
CRCW2010 e3	± 200 ppm/K	± 5 %	1 Ω to 10 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 10 MΩ	E24; E96
	Jumper, $I_{max.}$ = 6.0 A	≤ 20 mΩ	0 Ω	-
CRCW2512 e3	± 200 ppm/K	± 5 %	1 Ω to 10 MΩ	E24
	± 100 ppm/K	± 1 %	1 Ω to 10 MΩ	E24; E96
	Jumper, $I_{max.}$ = 7.0 A	≤ 20 mΩ	0 Ω	-

Note

- The temperature coefficient of resistance (TCR) is not specified for 0 Ω jumpers

PACKAGING

TYPE / SIZE	CODE	QUANTITY	CARRIER TAPE	WIDTH	PITCH	REEL DIAMETER
D10/CRCW0402 e3	ED = ET7	10 000	Paper tape acc. to IEC 60286-3, Type 1a	8 mm	2 mm	Ø 180 mm/7"
	EE = EF4	50 000				Ø 330 mm/13"
D11/CRCW0603 e3	EI = ET2	5000		8 mm	2 mm	Ø 180 mm/7"
	ED = ET3	10 000				Ø 180 mm/7"
	EL = ET4	20 000				Ø 285 mm/11.25"
	EE = ET8	50 000				Ø 330 mm/13"
	EA = ET1	5000			4 mm	Ø 180 mm/7"
	EB = ET5	10 000				Ø 285 mm/11.25"
	EC = ET6	20 000				Ø 330 mm/13"
D12/CRCW0805 e3	EA = ET1	5000		8 mm	4 mm	Ø 180 mm/7"
	EB = ET5	10 000				Ø 285 mm/11.25"
	EC = ET6	20 000				Ø 330 mm/13"
D25/CRCW1206 e3	EA = ET1	5000		8 mm	4 mm	Ø 180 mm/7"
	EB = ET5	10 000				Ø 285 mm/11.25"
	EC = ET6	20 000				Ø 330 mm/13"
CRCW1210 e3	EA = ET1	5000		8 mm	4 mm	Ø 180 mm/7"
	EB = ET5	10 000				Ø 285 mm/11.25"
	EC = ET6	20 000				Ø 330 mm/13"
CRCW1218 e3	EK = ET9	4000	Blister tape acc. to IEC 60286-3, Type 2a	12 mm	4 mm	Ø 180 mm/7"
CRCW2010 e3	EF = E02	4000		12 mm	4 mm	Ø 180 mm/7"
CRCW2512 e3	EG = E67	2000		12 mm	8 mm	Ø 180 mm/7"
	EH = E82	4000			4 mm	

PART NUMBER AND PRODUCT DESCRIPTION

Part Number: CRCW0603562RFKEA
Part Number: CRCW06030000Z0EA

C	R	C	W	0	6	0	3	5	6	2	R	F	K	E	A

TYPE / SIZE	RESISTANCE	TOLERANCE	TCR	PACKAGING
D10/CRCW0402 **D11/CRCW0603** **D12/CRCW0805** **D25/CRCW1206** **CRCW1210** **CRCW1218** **CRCW2010** **CRCW2512**	**R** = decimal **K** = thousand **M** = million **0000** = jumper	**F** = ± 1 % **J** = ± 5 % **Z** = jumper	**K** = ± 100 ppm/K **N** = ± 200 ppm/K **0** = jumper	**EA, EB,** **EC, ED,** **EE, EF,** **EG, EH,** **EI, EK,** **EL**

Product Description: D11/CRCW0603 100 562R 1% ET1 e3
Product Description: D11/CRCW0603 0R0 ET1 e3

D11/CRCW0603	100	562R	1 %	ET1	e3
TYPE / SIZE	TCR	RESISTANCE	TOLERANCE	PACKAGING	LEAD (Pb)-FREE
D10/CRCW0402 **D11/CRCW0603** **D12/CRCW0805** **D25/CRCW1206** **CRCW1210** **CRCW1218** **CRCW2010** **CRCW2512**	± **100** ppm/K ± **200** ppm/K	**10R** = 10 Ω **562R** = 562 Ω **1M** = 1 MΩ **0R0** = jumper	± **1 %** ± **5 %**	**ET1, ET2,** **ET3, ET4,** **ET5, ET6,** **ET8, ET9,** **EF4, E02,** **E67, E82**	**e3** = pure tin termination finish

Innovative Service Around the Globe YAGEO

DATA SHEET

GENERAL PURPOSE CHIP RESISTORS

RC0603

5%, 1%

RoHS compliant

YAGEO Phycomp

Product specification – Jul 15, 2008 V.3

SCOPE

This specification describes RC0603 series chip resistors with lead-free terminations made by thick film process.

APPLICATIONS

- All general purpose application

FEATURES

- RoHS compliant
  - Products with lead free terminations meet RoHS requirements
  - Pb-glass contained in electrodes
  - Resistor element and glass are exempted by RoHS
- Reducing environmentally hazardous wastes
- High component and equipment reliability
- Saving of PCB space
- None forbidden-materials used in products/production
- Halogen Free Epoxy

ORDERING INFORMATION - GLOBAL PART NUMBER & 12NC

Both part numbers are identified by the series, size, tolerance, packing type, temperature coefficient, taping reel and resistance value.

YAGEO BRAND ordering code

GLOBAL PART NUMBER (PREFERRED)

RC0603	X	R	-	XX	XXXX	L
	(1)	(2)	(3)	(4)	(5)	(6)

(1) TOLERANCE

F = ±1%
J = ±5% (for Jumper ordering, use code of J)

(2) PACKAGING TYPE

R = Paper / PE taping reel

(3) TEMPERATURE COEFFICIENT OF RESISTANCE

– = Base on spec

(4) TAPING REEL

07 = 7 inch dia. Reel
10 = 10 inch dia. Reel
13 = 13 inch dia. Reel

(5) RESISTANCE VALUE

There are 2~4 digits indicated the resistor value. Letter R/K/M is decimal point, no need to mention the last zero after R/K/M, e.g.1K2, not 1K20.

Detailed resistance rules show in table of "Resistance rule of global part number".

(6) OPTIONAL CODE

L = optional symbol (Note)

Resistance rule of global part number

Resistance code rule	Example
0R	0R = Jumper
XRXX (1 to 9.76 Ω)	1R = 1 Ω 1R5 = 1.5 Ω 9R76 = 9.76 Ω
XXRX (10 to 97.6 Ω)	10R = 10 Ω 97R6 = 97.6 Ω
XXXR (100 to 976 Ω)	100R = 100 Ω
XKXX (1 to 9.76 KΩ)	1K = 1,000 Ω 9K76 = 9760 Ω
XMXX (1 to 9.76 MΩ)	1M = 1,000,000 Ω 9M76= 9,760,000 Ω

ORDERING EXAMPLE

The ordering code of a RC0603 chip resistor, value 56 Ω with ±1% tolerance, supplied in 7-inch tape reel is: RC0603FR-0756R(L).

NOTE

1. All our RSMD products meet RoHS compliant. "LFP" of the internal 2D reel label mentions "Lead Free Process"
2. On customized label, "LFP" or specific symbol printed and the optional "L" at the end of GLOBAL PART NUMBER / 12NC can be added (both are on customer request)

PHYCOMP BRAND ordering codes

Both GLOBAL PART NUMBER (preferred) and 12NC (traditional) codes are acceptable to order Phycomp brand products.

GLOBAL PART NUMBER (PREFERRED)

For detailed information of GLOBAL PART NUMBER and ordering example, please refer to page 2.

12NC CODE

2322 / 2350 XXX XXXXX L
(1) (2) (3) (4)

TYPE/ 0603	START IN (1)	TOL. (%)	RESISTANCE RANGE	PAPER / PE TAPE ON REEL (units) (2)		
				5,000	10,000/not preferred	20,000
RC21	2322	±5%	1 to 10 MΩ	702 60xxx	702 70xxx	702 81xxx
RC22	2322	±1%	1 to 10 MΩ	704 6xxxx	704 7xxxx	704 8xxxx
HRC21	2350	±5%	11 to 22 MΩ	522 10xxx	-	-
Jumper	2322	-	0 Ω	702 96001	702 97001	702 92002

(1) The resistors have a 12-digit ordering code starting with 2322 / 2350.

(2) The subsequent 4 or 5 digits indicate the resistor tolerance and packaging.

(3) The remaining 4 or 3 digits represent the resistance value with the last digit indicating the multiplier as shown in the table of "Last digit of 12NC".

(4) "L" is optional symbol (Note).

Last digit of 12NC

Resistance decade (3)	Last digit
0.01 to 0.0976 Ω	0
0.1 to 0.976 Ω	7
1 to 9.76 Ω	8
10 to 97.6 Ω	9
100 to 976 Ω	1
1 to 9.76 KΩ	2
10 to 97.6 KΩ	3
100 to 976 KΩ	4
1 to 9.76 MΩ	5
10 to 97.6 MΩ	6

Example:
0.02 Ω = 0200 or 200
0.3 Ω = 3007 or 307
1 Ω = 1008 or 108
33 KΩ = 3303 or 333
10 MΩ = 1006 or 106

ORDERING EXAMPLE

The ordering code of a RC22 resistor, value 56 Ω with ±1% tolerance, supplied in tape of 5,000 units per reel is: 232270465609(L) or RC0603FR-0756R(L).

NOTE

1. All our RSMD products are RoHS compliant. "LFP" of the internal 2D reel label mentions "Lead Free Process"
2. On customized label, "LFP" or specific symbol printed and the optional "L" at the end of GLOBAL PART NUMBER / 12NC can be added (both are on customer request)

MARKING

RC0603

Fig. 1 Value = 10 KΩ

E-24 series: 3 digits

First two digits for significant figure and 3rd digit for number of zeros

Fig. 2 Value = 12.4 KΩ

Fig. 3 E-24 1% Value = 56 KΩ

E-96 series: 3 digits for 0603 ±1% EIA-96 marking method

For 0603 ±1% E-24 series, one short bar under marking letter

For further marking information, please see special data sheet "Chip resistors marking".

CONSTRUCTION

The resistor is constructed on top of a high-grade ceramic body. Internal metal electrodes are added on each end to make the contacts to the thick film resistive element. The composition of the resistive element is a noble metal imbedded into a glass and covered by a second glass to prevent environment influences. The resistor is laser trimmed to the rated resistance value. The resistor is covered with a protective epoxy coat, finally the two external terminations (matte tin on Ni-barrier) are added. See fig.4

DIMENSIONS

Table 1

TYPE	RC0603
L (mm)	1.60 ±0.10
W (mm)	0.80 ±0.10
H (mm)	0.45 ±0.10
l_1 (mm)	0.25 ±0.15
l_2 (mm)	0.25 ±0.15

OUTLINES

For dimension see Table 1

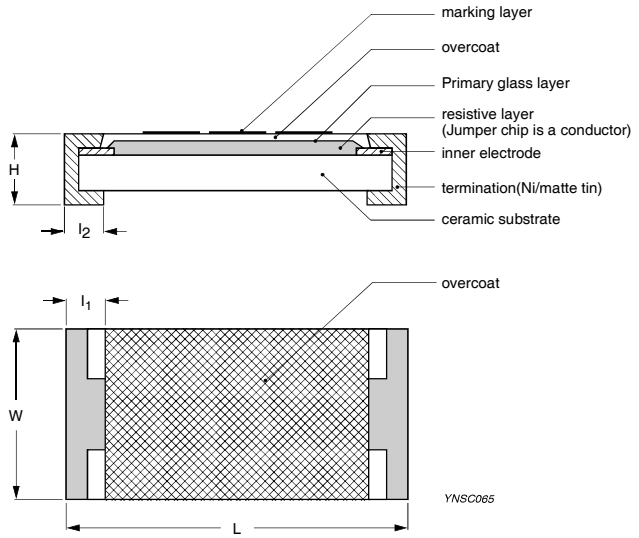


Fig. 4 Chip resistor outlines

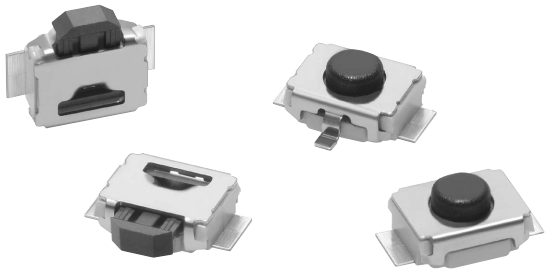
OMRON

Ultra-small Tactile Switch (SMT) B3U

Ultra-small Surface-mounting Tactile Switches with High Contact Reliability (1.2 × 3 × 2.5 mm (H × W × D)

- Smallest class in the industry for high-density mounting of compact devices.
- Surface mounted: Ideal for high-density mounting.
- Models with ground terminals are available for protection against static electricity.
- Available on embossed tape: Ideal for automatic mounting.

RoHS Compliant



■ List of Models

Operation type	Contact material	Height	Operating force (OF)	Plunger color	Locating pin	Embossed taping (standard quantity) Without ground terminal	Embossed taping (standard quantity) With ground terminal	Embossed taping (standard quantity) Minimum packing unit	Embossed taping (small quantity) Without ground terminal	Embossed taping (small quantity) With ground terminal	Embossed taping (small quantity) Minimum packing unit
B3U-1000 Series: Top-actuated	**Silver plated**	**1.6 mm**	**1.5 N {153 gf}**	**Black**	**Without boss**	B3U-1000P	B3U-1100P	3,500	B3U-1000PM	B3U-1100PM	1,000
					With boss	B3U-1000P-B	B3U-1100P-B		B3U-1000PM-B	B3U-1100PM-B	
B3U-3000 Series: Side-actuated		**3.2 mm**	**1.59 N {162 gf}**		**Without boss**	B3U-3000P	B3U-3100P	4,000	B3U-3000PM	B3U-3100PM	1,000
					With boss	B3U-3000P-B	B3U-3100P-B		B3U-3000PM-B	B3U-3100PM-B	

Note: Orders must be made in multiples of the order unit specified above.

■ Ratings/Characteristics

Item / Operation type	Top-actuated (B3U-1000 Series)	Side-actuated (B3U-3000 Series)
Rating (resistive load)	1 to 50 mA, 3 to 12 VDC	
Minimum applicable load (reference value)	10 μA at 1 VDC (resistive load)	
Ambient operating temperature	-25°C to +70°C at 60%RH max. (with no icing or condensation)	
Ambient operating humidity	35% to 85% (at +5 to +35°C)	
Contact form	SPST-NO	
Contact resistance (initial value)	100 mΩ max.	
Insulation resistance	100 MΩ min. (at 100 VDC with insulation tester)	
Dielectric strength	250 VAC, 50/60 Hz for 1 min	
Bounce time	5 ms max.	
Vibration resistance	10 to 55 Hz, 1.5 mm double amplitude	
Shock resistance	1,000 m/s^2 max.	
Durability	200,000 operations min.	100,000 operations min.
Weight	Approx. 0.022 g	
Degree of protection	IEC IP40	
Washing	Not possible	

■ Operating Characteristics

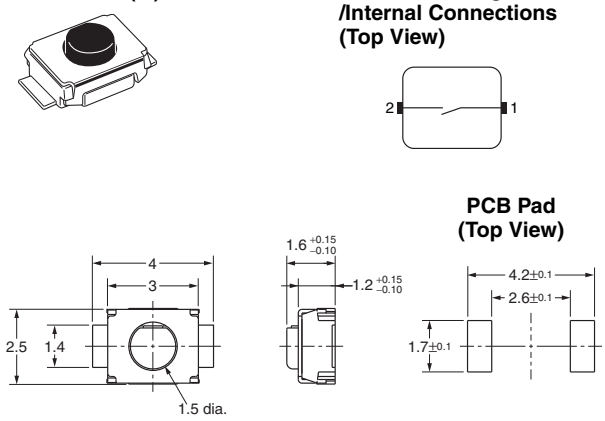
Item / Operation type	Top-actuated (B3U-1000 Series)	Side-actuated (B3U-3000 Series)
Operating force (OF)	1.50 ± 0.49 N {153 ± 50 gf}	1.59 ± 0.49 N {162 ± 50 gf}
Releasing force (RF)	0.2 N min. {20 gf}	
Pretravel (PT)	$0.15^{+0.2}_{-0.1}$ mm	$0.2^{+0.2}_{-0.1}$ mm

■ Dimensions (Unit: mm)

Top-actuated Models

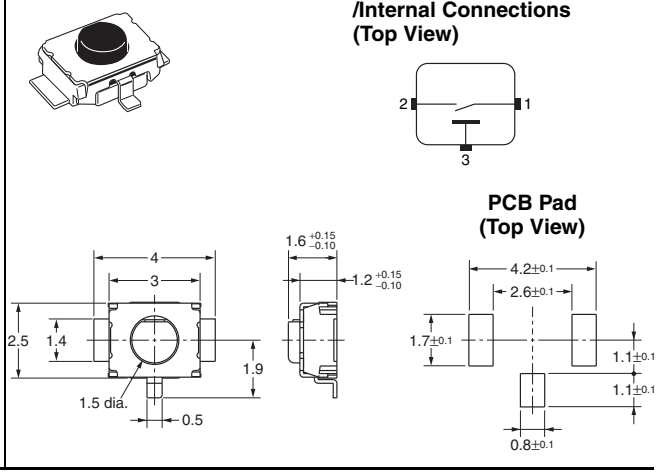
Without Ground Terminal, without Boss

B3U-1000P(M)



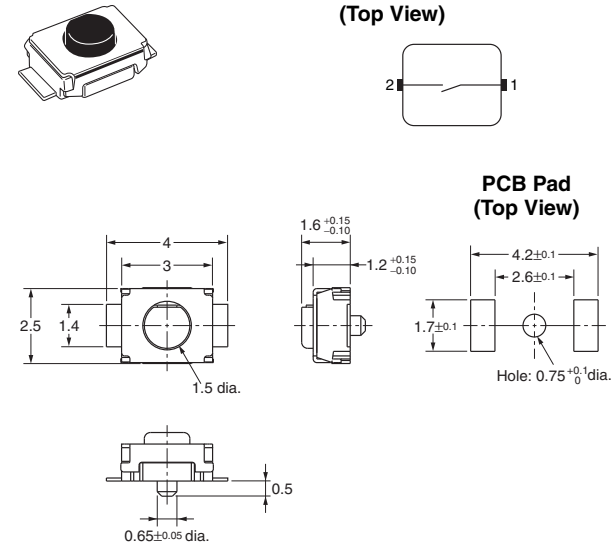
With Ground Terminal, without Boss

B3U-1100P(M)



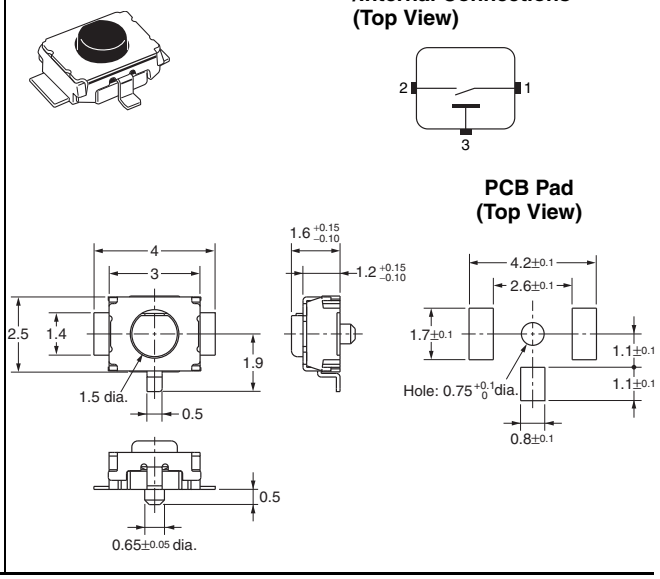
Without Ground Terminal, with Boss

B3U-1000P(M)-B



With Ground Terminal, with Boss

B3U-1100P(M)-B

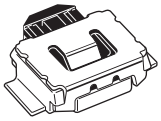


Note: Unless otherwise specified, a tolerance of ±0.2 mm applies to all dimensions. No terminal numbers are indicated on the Switches.

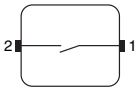
Side-actuated Models

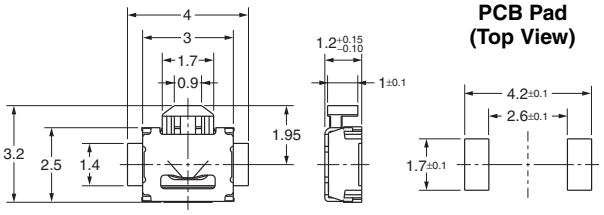
Without Ground Terminal, without Boss

B3U-3000P(M)



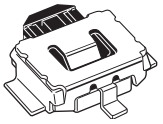
Terminal Arrangement /Internal Connections (Top View)



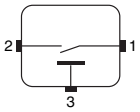


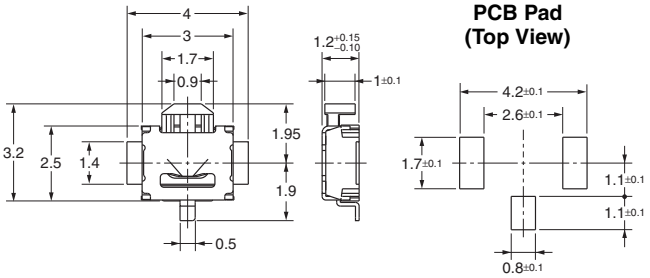
With Ground Terminal, without Boss

B3U-3100P(M)



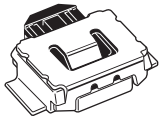
Terminal Arrangement /Internal Connections (Top View)



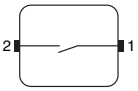


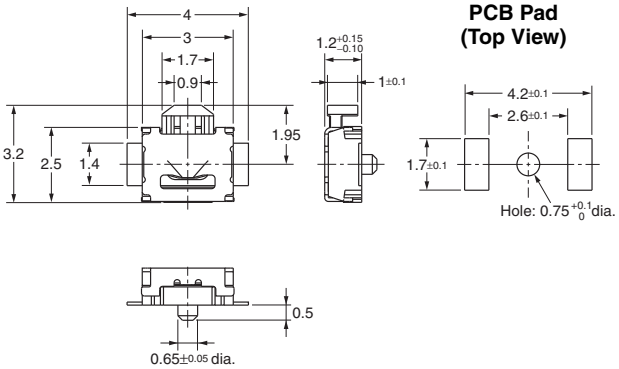
Without Ground Terminal, with Boss

B3U-3000P(M)-B



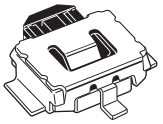
Terminal Arrangement /Internal Connections (Top View)



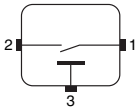


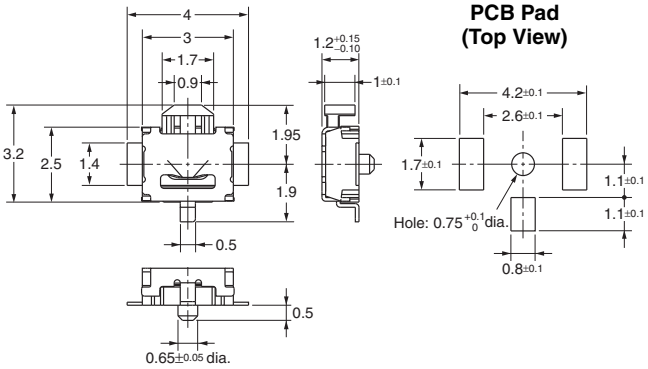
With Ground Terminal, with Boss

B3U-3100P(M)-B



Terminal Arrangement /Internal Connections (Top View)





Note: Unless otherwise specified, a tolerance of ±0.2 mm applies to all dimensions. No terminal numbers are indicated on the Switches.

■ Precautions

Be sure to read the precautions common to all Tactile Switches on pages for correct use.

Relación de documentos

(_) Memoria ..... 85 páginas

(X) Anexos .....528 páginas

La Almunia, a 22 de 09 de 2020

Firmado: Luis Arbós Gómez