

Asymmetrical Non-Complementary Modulation Strategies for Independent Power Control in Multi-Output Resonant Inverters

P. Guillén, *Student Member, IEEE*, H. Sarnago, *Senior Member, IEEE*, O. Lucía, *Senior Member, IEEE*, and J.M. Burdío, *Senior Member, IEEE*

Abstract — Domestic induction heating design trends aim at improving user experience by increasing the cooking surface flexibility while maintaining a cost-effective implementation. The design of multi-output topologies is a key development for this purpose. However, due to their complexity, output power control usually relies on low-frequency pulse density modulations which, in addition to the slow response due to significant power averaging times, presents severe restrictions as a consequence of power pulsation regulations. This paper proposes two different non-complementary asymmetrical modulation strategies that allow continuous operation avoiding both flicker and heating performance issues, and obtaining a fast-response load power control. In order to prove the feasibility of the proposed modulations, a prototype featuring 12 induction heating loads of 2000 W maximum rated power has been built, and both strategies have been tested.

I. INTRODUCTION

Domestic induction heating (IH) outperforms classical heating technologies due to its high efficiency, fast heating and safe and clean operation [1-3]. These advantages have allowed the technology to lead the home-appliances market in the last decade [4-6]. From this leading position, design tendencies aim for a better user experience, being one of the most prolific fields of research the flexibility increase of the induction cooktops [7-12].

Flexible surfaces allow the placement of a variable number of pots of any shape and any size over the cooktop. In order to implement these systems, cooktops that present a dense distribution of small to medium size inductors are built [13]. This leads to several challenges in the design of the different cooktop parts in order to achieve a high-performance and cost-effective implementation.

One of the main areas of research that have a high impact in the final product performance is the topology design. Several approaches have been prospected in recent years in order to obtain low-device-count multi-output structures. Some of the most relevant are the single-switch topologies [14, 15], multiple variants of the half-bridge [16-19], that may include inductor clustering [20], or matrix-based topologies [21].

The last group is highlighted as a promising approach. Inverters are derived from the half-bridge topology [22] and present the high side switching devices placed in a row whereas the low side ones are arranged in a column and thus are able to

power a number of inductors equal to the number of cells contained in the matrix. As a consequence, their main advantage is the significant reduction of the number of switches needed to power a high number of coils. In addition, this reduction does not compromise the independence of each inductor, showing a behavior similar to the one achieved by single-inverter single-coil topologies i.e. a half bridge powering a single induction load. Thus, an instantaneous power control over each load can be achieved and each coil can be used as a pot detection system [23].

Even though their numerous advantages, the reduction of the number of power devices is usually paired with a decrease in the number of degrees of freedom to control each individual IH load, e.g. common switching frequency. In order to solve these restrictions, low-frequency temporal multiplexation of active loads is typically used [24]. However, this approach presents severe limitations in terms of electromagnetic compatibility (EMC) performance, i.e. flicker [25], and thermal performance due to pulsating power. Consequently, it is interesting to propose continuous operation mode modulation strategies in order to improve cooktop performance.

In this paper, two non-complementary asymmetrical modulation strategies are proposed, studied, and evaluated for their use in a multiple-output matrix-based resonant inverter in order to obtain an independent fast-response power control.

The remainder of this paper is organized as follows: In Section II, the inverter and its classical modulation strategies are presented. Section III details the proposed control strategies. Section IV shows the experimental prototype and analyzes the strategies based on experimental and simulation results. Finally, the conclusions of this paper are drawn in Section V.

II. MULTI-OUTPUT ZVS INVERTER POWER CONTROL

A. Topology description

In order to power a high number of medium power loads, a matrix-based resonant inverter is proposed. This topology has been designed following a unidimensional matrix structure, with a single high side transistor so that unwanted IH load activation is prevented. This solution, when considering an implementation with a number, n , of IH loads, increases the switching devices count from $2\sqrt{n}$ to $n+1$. Additionally, in contrast with the topology described in [21], this inverter allows

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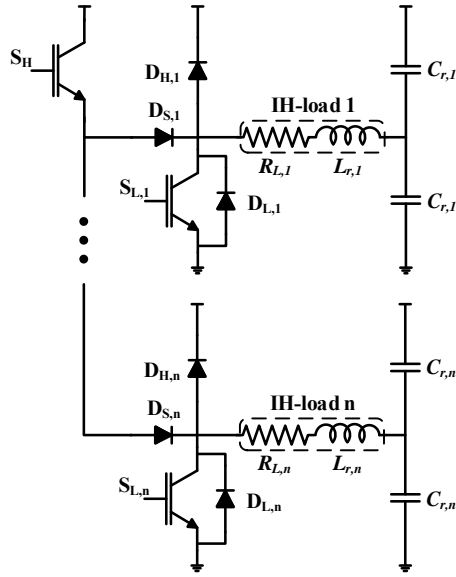


Fig. 1 Unidimensional matrix-based ZVS resonant inverter.

ZVS operation, reducing power losses and switching frequency limitations.

The proposed topology can be seen in Fig. 1. It is composed of a high-side transistor, S_H , and several output cells, each one of them associated to an IH load. Each cell contains a series diode, $D_{S,i}$, an antiparallel diode, $D_{H,i}$, and a low-side transistor, $S_{L,i}$, with a built-in antiparallel diode, $D_{L,i}$. Each IH load, is modelled as an equivalent series inductance, $L_{r,i}$, and resistance, $R_{L,i}$, whose values depend on the inductor-pot coupling, pot material or switching frequency [26], among others. To complete the resonant tank, a split capacitor, $C_{r,i}$, is connected in series.

Compared with state-of-the-art commercial cooktops, several benefits can be highlighted. On the one hand, nowadays commercial topologies depend on electromagnetic relays in order to route the power paths between the inverters and the inductors [27], which in most cases implies inductor clustering in order to power all the loads. On the other hand, the unidimensional matrix structure has fixed power paths and therefore there is no need for relays and, as there is no inductor clustering, the low-side transistors have to withstand lower currents. Another consequence of independent inductor powering is the capacity to use fast-response continuous modulations, avoiding low-frequency pulse density modulation (LF-PDM) and their issues regarding flicker and poor thermal performance.

B. State-of-the-art modulation strategies

The aforementioned independent control over each inductor is especially relevant when observing the overall behavior of flexible surfaces. As previously introduced, their purpose is to enable the placement of pots of any shape and any size in any position in the cooktop. Therefore, not only pots of different materials, but also partially covered inductors, with different coupling between the inductor and the pot and thus different R_L and L_r , are to be powered with the same inverter. That means

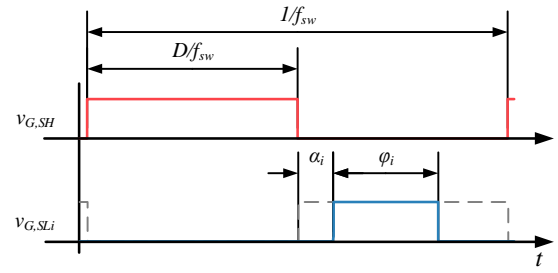


Fig. 2 General scheme of transistor gating signals for both modulations.

that different power requirements might not be only set by the user for the different pots but also by the appliance in order to produce an even heating of the pot.

In order to fulfill those power requirements, two complementary modulations have been earlier used being possible to link each of them with the different switching devices. First of all, a variable frequency duty cycle control, (VFDC) strategy, whose switching frequency, f_{sw} , and duty cycle, D , is set by the high side transistor, allows to choose the power given to each load depending on its equivalent parameters. In addition, due to the different power levels, a LF-PDM is used to connect or disconnect the different inductors, by means of the low side transistor, and available power is obtained by averaging the power transmitted to each load in the LF-PDM strategy period.

This combination of strategies obtains good performance in terms of average power. However, in practice it is limited in commercial devices due to the following reasons: regulations and user experience. For the first case, those strategies of pulsating power are severely constrained by flicker regulations that does not allow sudden input power variations. For the second one, power pulsation generates uneven boiling in the pan and acoustic noise due to the Lorentz forces variation over the different pots bus capacitor discharges.

III. PROPOSED NON-COMPLEMENTARY ASYMMETRICAL MODULATIONS

In order to address the aforementioned limitations, continuous operation mode modulation strategies are proposed in this paper. The common factor of both modulations is that the common high-side transistor is used to select the switching frequency and duty cycle, while the activation of the low-side ones will be controlled to transmit the required power. In Fig. 2, the high- and low-side transistor gate voltage, $V_{G,SH}$ and $V_{G,SLi}$, respectively, and their main modulation parameters can be seen.

In order to achieve higher efficiency, both strategies are derived from the square waveform operation i.e. the high side transistor is activated with $D = 0.5$. Therefore, the maximum output power is dependent of the switching frequency and the load. Consequently, power control is achieved by modifying the low side transistor activation. This activation is in both cases non-complementary, which means that there is a lag between each transistor deactivation and the activation of the following one. If the lag is achieved increasing the delay of the activation

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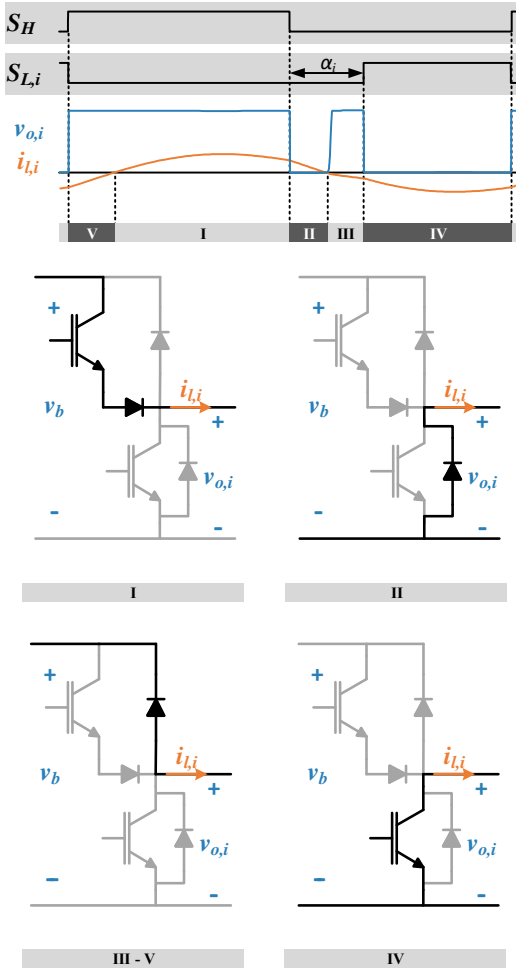


Fig. 3 Main waveforms and active devices for the NC-PDC strategy, being v_b the bus voltage, $v_{o,i}$ the voltage applied to the IH load i and $i_{L,i}$ the current through the load.

of the low side transistor, α_i , the modulation strategy is identified as non-complementary pulse delay control (NC-PDC) whereas if the lag is derived of the reduction of the low side transistor conduction time, ϕ_i , is called non-complementary pulse width modulation (NC-PWM).

In the following section, both strategies are presented and analyzed in order to obtain its main operational parameters.

A. NC-PDC

The low-side transistor activation delay variation enables power control when α_i is higher than the current zero crossing time.

To obtain this minimum delay, the load current can be evaluated based on the Fourier series analysis, being $A_{hl,i}$ and $B_{hl,i}$ the Fourier coefficients and ϕ the phase,

$$i_{L,i}(\phi) = \sum_{h=1}^H (A_{hl,i} \cos(h\phi) + B_{hl,i} \sin(h\phi)). \quad (1)$$

And the zero crossing point can be calculated assuming square voltage applied to the load and first harmonic approximation as

$$\alpha_i > \phi|_{i_{L,i}(\phi)=0} = \tan^{-1} \left(\frac{-A_{l,i}}{B_{l,i}} \right) = \tan^{-1} \left(\frac{\omega_s L_{r,i} - \frac{1}{\omega_s C_{r,i}}}{R_{L,i}} \right), \quad (2)$$

being the angular frequency $\omega_s = 2\pi f_{sw}$. Summarizing, α_i is to be higher than the load impedance argument. As a consequence, power control resolution may be affected, being this aspect more relevant in the high frequency range, that leads to an inductive behavior of the load.

Once $\alpha_i > \phi|_{i_{L,i}(\phi)=0}$ is assured, the converter operation in steady state is as described in Fig. 3. Current flows through S_H when it is activated (State I). When S_H is turned off, current flows through $D_{L,i}$ (State II) until it reaches zero. Then, due to the resonant nature of the load, $D_{H,i}$ is activated (State III). The stage after the current flows through $D_{H,i}$ depends on the low side transistor activation. For high power, $S_{L,i}$ would activate (State IV) before current through $D_{H,i}$ fades to zero while for low power current can be assumed to become zero. When $S_{L,i}$ is deactivated, current flows through $D_{H,i}$ (State V) and S_H consecutively (State I).

The voltage applied to the load and the current though it can be obtained by performing Fourier analysis.

The voltage, with $A_{hV,i}$ and $B_{hV,i}$ as Fourier coefficients is of the form

$$v_{o,i}(\phi) = V_{avg} + \sum_{h=1}^H (A_{hV,i} \cos(h\phi) + B_{hV,i} \sin(h\phi)), \quad (3)$$

with an average voltage, V_{avg} ,

$$V_{avg} = V_{bus} \frac{\pi + \alpha_i - \phi|_{i_{L,i}(\phi)=0}}{2\pi}. \quad (4)$$

The coefficients for both voltage and current are shown in equation (5) and (6).

$$\begin{cases} A_{hV,i} = (-1)^h \frac{V_{bus}}{h\pi} \left(\sin(h\alpha_i) - \sin(h\phi|_{i_{L,i}(\phi)=0}) \right) \\ B_{hV,i} = \frac{V_{bus}}{h\pi} \left(-\cos(h\alpha_i) + \cos(h\phi|_{i_{L,i}(\phi)=0}) - 1 + (-1)^h \right) \end{cases} \quad (6)$$

$$\begin{cases} A_{hl,i} = \frac{V_{bus}}{h\pi \left(R_L^2 + \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right)^2 \right)} \left(\left(\sin(h\alpha_i) - \sin(h\phi|_{i_{L,i}(\phi)=0}) \right) R_L - \left(-\cos(h\alpha_i) + \cos(h\phi|_{i_{L,i}(\phi)=0}) - 1 + (-1)^h \right) \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right) \right) \\ B_{hl,i} = \frac{V_{bus}}{h\pi \left(R_L^2 + \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right)^2 \right)} \left(\left(-\cos(h\alpha_i) + \cos(h\phi|_{i_{L,i}(\phi)=0}) - 1 + (-1)^h \right) R_L + \left(\sin(h\alpha_i) - \sin(h\phi|_{i_{L,i}(\phi)=0}) \right) \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right) \right) \end{cases} \quad (5)$$

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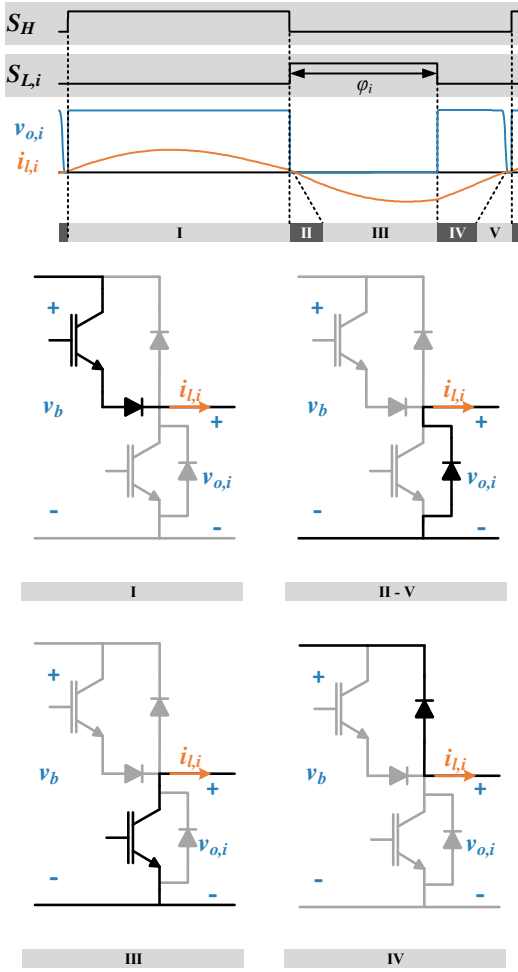


Fig. 4 Main waveforms and active devices for the NC-PWM strategy.

B. NC-PWM

For the case of non-complementary pulse width modulation, power control is achieved as in duty cycle variation. However, for low power, current reaches zero before S_H is activated. The ϕ_i for which current flows through $D_{L,i}$ before S_H activation can be calculated assuming first harmonic approximation known that to reach zero current before S_H activation $\phi|_{i_{L,i}(\phi)=0}$ has to be at maximum 2π ,

$$\phi_i < \cos^{-1} \left(\frac{\omega_s L_{r,i} - \frac{1}{\omega_s C_{r,i}}}{\sqrt{R_{L,i}^2 + \left(\omega_s L_{r,i} - \frac{1}{\omega_s C_{r,i}} \right)^2}} \right) - \tan^{-1} \left(\frac{-R_{L,i}}{\omega_s L_{r,i} - \frac{1}{\omega_s C_{r,i}}} \right). \quad (7)$$

The converter steady state operation when $D_{L,i}$ is activated before S_H activation can be seen in Fig. 4. Current flows through S_H (State I). Once S_H is turned off, current flows through $D_{L,i}$ (State II). As it is already active, when current crosses zero it flows through $S_{L,i}$ (State III) and, when it is switched off, through $D_{H,i}$ (State IV). Once the current reaches zero, $D_{L,i}$ is activated again (State V) until S_H is switched on (State I).

As for the NC-PDC case, the zero current crossing angle $\phi|_{i_{L,i}(\phi)=0}$ can be calculated as

$$\phi|_{i_{L,i}(\phi)=0} = \tan^{-1} \left(\frac{\sin(\phi) R_L + (-1 + \cos(\phi)) \left(\omega_s L_r - \frac{1}{\omega_s C_r} \right)}{(-1 + \cos(\phi)) R_L - \sin(\phi) \left(\omega_s L_r - \frac{1}{\omega_s C_r} \right)} \right), \quad (8)$$

and the load voltage and current can be evaluated by performing Fourier analysis, being the average voltage applied to the load

$$V_{avg} = V_{bus} \frac{\pi + \phi|_{i_{L,i}(\phi)=0} - \phi_i}{2\pi}, \quad (9)$$

and the coefficients are shown in equations (10) and (11).

$$\begin{cases} A_{hV,i} = \frac{V_{bus}}{h\pi} \left(\sin(h\phi|_{i_{L,i}(\phi)=0}) - \sin(h\phi_i) \right) \\ B_{hV,i} = \frac{V_{bus}}{h\pi} \left(-\cos(h\phi|_{i_{L,i}(\phi)=0}) + \cos(h\phi_i) - 1 + (-1)^h \right) \end{cases} \quad (10)$$

IV. EXPERIMENTAL PROTOTYPE AND RESULTS

A. Experimental setup

A prototype has been designed to prove the feasibility of the proposed modulations. It is designed to be integrated in a domestic cooktop that presents 12 coils of 2000 W of maximum rated power, being 3600 W the maximum power consumption per mains phase. In order to avoid limitations regarding power consumption, a two-phase implementation has been selected leading to a 7.2 kW prototype.

The power stage for each phase is based on the circuit shown in Fig. 1, composed of 6 cells per phase to minimize the number of components. The transistors have been selected so that they can operate with both non-complementary strategies. Consequently, the device ratings are calculated for the worst

$$\begin{cases} A_{hl,i} = \frac{V_{bus}}{h\pi \left(R_L^2 + \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right)^2 \right)} \left(\left(\sin(h\phi|_{i_{L,i}(\phi)=0}) - \sin(h\phi_i) \right) R_L - \left(-\cos(h\phi|_{i_{L,i}(\phi)=0}) + \cos(h\phi_i) - 1 + (-1)^h \right) \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right) \right) \\ B_{hl,i} = \frac{V_{bus}}{h\pi \left(R_L^2 + \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right)^2 \right)} \left(\left(-\cos(h\phi|_{i_{L,i}(\phi)=0}) + \cos(h\phi_i) - 1 + (-1)^h \right) R_L + \left(\sin(h\phi|_{i_{L,i}(\phi)=0}) - \sin(h\phi_i) \right) \left(\omega_s h L_r - \frac{1}{\omega_s h C_r} \right) \right) \end{cases} \quad (11)$$

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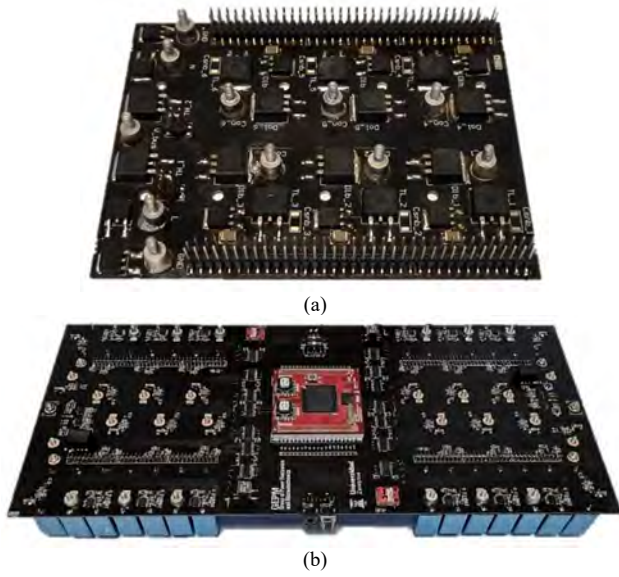


Fig. 5 Details of the designed prototype. (a) shows the design of the IMS power board while (b) depicts the FR4 control board.



Fig. 6 Experimental setup.

TABLE I
EXPERIMENTAL PROTOTYPE POWER DEVICES

Component	Reference
High side Transistor, S_H	IGB50N65S5
Low side Transistor, S_{Li}	IKB40N65ES5
Series diode, D_{Si}	DSEI 36-06AS
Antiparallel diode, D_{Hi}	VS-15EWX06FN-M3
Discrete rectifier diode, D_{rect}	VS-15AWL06FN-M3

operating condition, regardless of the chosen strategy. Thus, low-side transistors, S_L , are chosen to operate with 2000 W and square waveform, and high side transistors, S_H , are selected to operate with 3600 W when all the 6 loads are active. In addition, each PCB board includes the diodes of each cell, a discrete full-bridge diode rectifier, and power and signal connectors. The selected devices are listed in Table I.

Besides, considering the relevance of thermal performance of the prototype [28] and the number of power devices, an

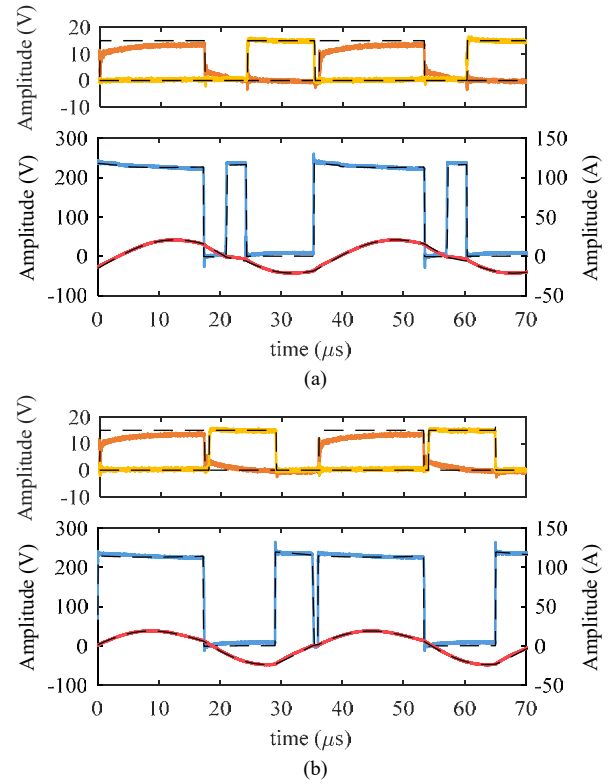


Fig. 7 Experimental and simulated waveforms showing non-complementary pulse delay control (NC-PDC) with $\alpha = 1.22$ rad (a) and non-complementary pulse width control (NC-PWM) with $\phi = 1.92$ rad (b) asymmetrical strategies. Shared switching frequency is 27.7 kHz and objective power 1200 W.

TABLE II
IH LOAD PARAMETERS AT RESONANT FREQUENCY

Parameter	Value
L_r	86 μ H
R_L	4.11 Ω
C_r	440 nF

implementation based on insulated metal substrate (IMS) has been selected for the power devices [28].

In addition, a FR4 PCB has been designed to control both power IMS and to support the resonant capacitors. This PCB presents three isolated modules; two of them include the necessary measurements and gate drivers to control the power boards and the third one powers the FPGA and the communications chipset.

Fig. 5 shows the IMS PCB for power devices (a) and the control circuit board (b). Connection is made vertically and the IMS PCBs are attached to independent heatsinks.

B. Experimental results

The designed prototype has been implemented, and performance tests have been carried out. Fig. 6 shows the experimental setup that includes the prototype, four oval-shaped inductors connected in pairs to each of the prototype phase, the pot, and the measurement equipment.

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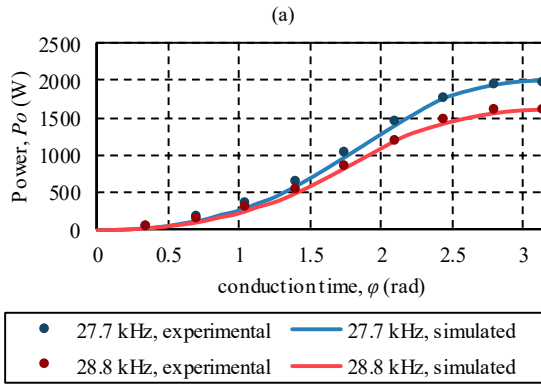
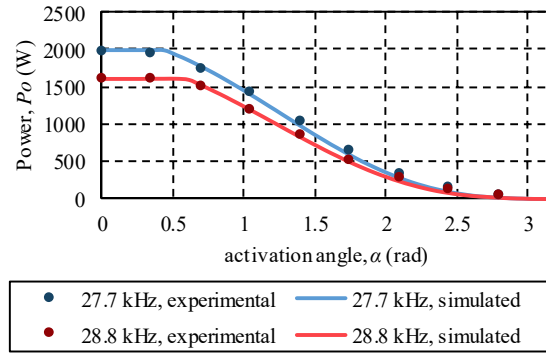


Fig. 8 Power curves for different activation angle, α , variation in NC-PDC strategy (a) and conduction time, ϕ , variation in NC-PWM strategy (b) starting with square waveform at 27.7 kHz, i.e. 2000 W, and 28.8 kHz, i.e. 1600 W. Activation angle and conduction time in radians with 2π as total switching period.

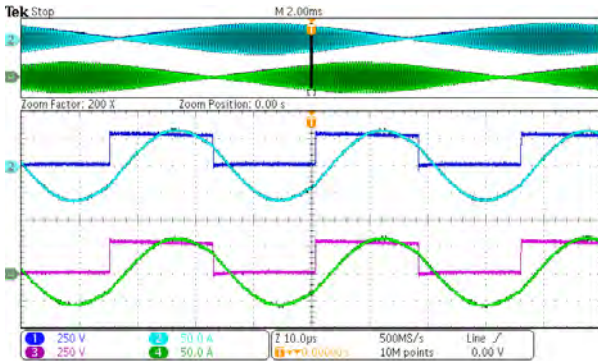


Fig. 9 Waveforms for 4 IH loads powered from two phases each at full power. From top to bottom: Phase 1 output voltage, $v_{o,1}$ (250 V/div, dark blue), Phase 1 inductor current, $i_{l,1}$ (50 A/div, cyan), Phase 2 output voltage, $v_{o,2}$ (250 V/div, pink), Phase 2 inductor current, $i_{l,2}$ (50 A/div, green). Time axis: 50 μ s/div.

In order to reduce the complexity of the analysis, pots are equally placed so that IH loads present the same equivalent parameters equal to the ones shown in Table II. Thus, in order to prove the correct behavior of the different modulations, simultaneous load activation with different objective power is to be achieved.

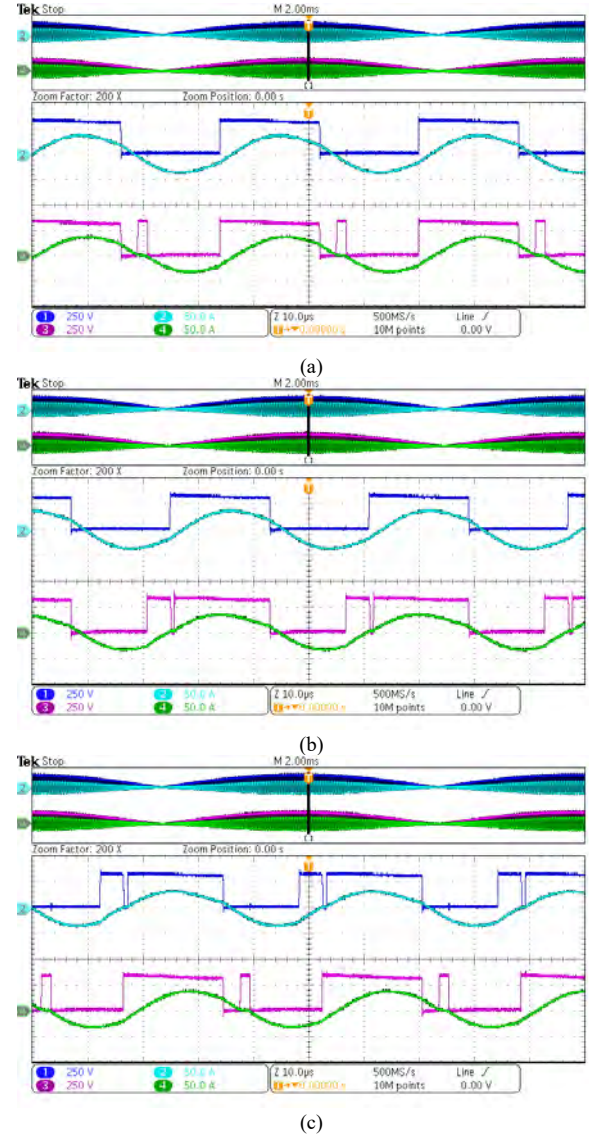


Fig. 10 Waveforms for two IH loads powered simultaneously with different modulation strategies. Square waveform, 2000 W, and NC-PDC strategy, 1600 W, (a). Square waveform, 2000 W, and NC-PWM strategy, 1600 W, (b). NC-PDC strategy, 1600 W, and NC-PDC strategy, 1600 W, (c). On each capture, from top to bottom: Load 1 output voltage, $v_{o,1}$ (250 V/div, dark blue), Load 1 inductor current, $i_{l,1}$ (50 A/div, cyan), Load 2 output voltage, $v_{o,2}$ (250 V/div, pink), Load 2 inductor current, $i_{l,2}$ (50 A/div, green). Time axis: 10 μ s/div.

In Fig. 7, the main waveforms of a single IH load can be seen for both strategies. These include the high- and low-side transistor gate voltage, $v_{G,SH}$ and $v_{G,SL}$, the voltage applied to the load, $v_{o,i}$, and the current trough the load, $i_{l,i}$.

The results presented in Fig. 7 show both the accuracy of the simulation model, and the correct load power control for a single frequency and single objective power. To complete these results, in Fig. 8 the full-range output power control can be seen, proving the versatility of the proposed control for different switching frequencies.

Once single IH load power control is assured, various loads are tested. In Fig. 9, the operation of the prototype at full power

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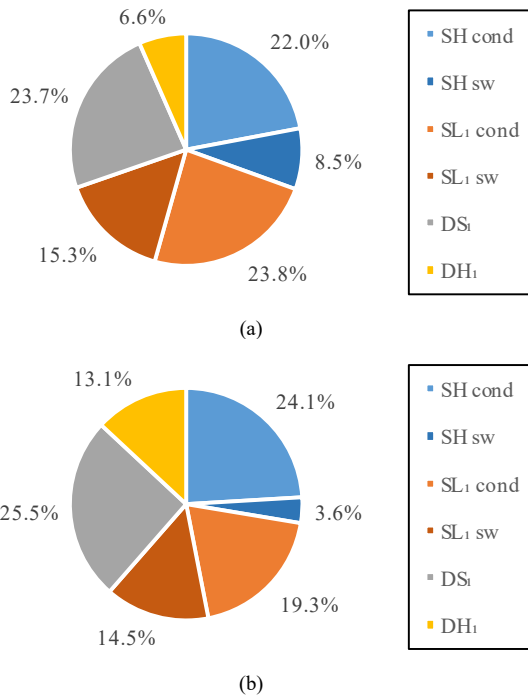


Fig. 11 Estimated power loss share using the NC-PDC strategy (a) and the NC-PWM strategy (b) with a common switching frequency of 27.7 kHz and a single load with an objective power of 1200 W.

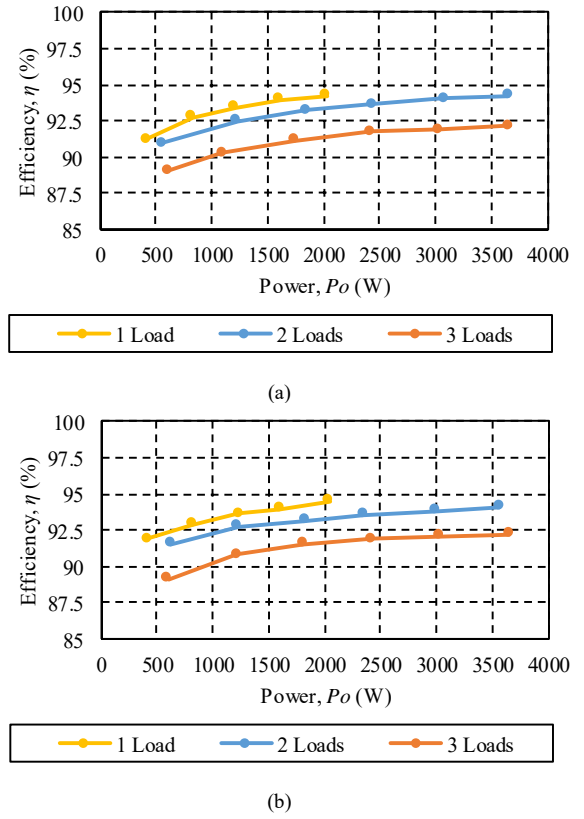


Fig. 13 Efficiency curves for different IH load count and with a base frequency of 27.7 kHz, i.e. maximum rated frequency of 2000 W for the NC-PDC strategy (a) and the NC-PWM strategy (b).

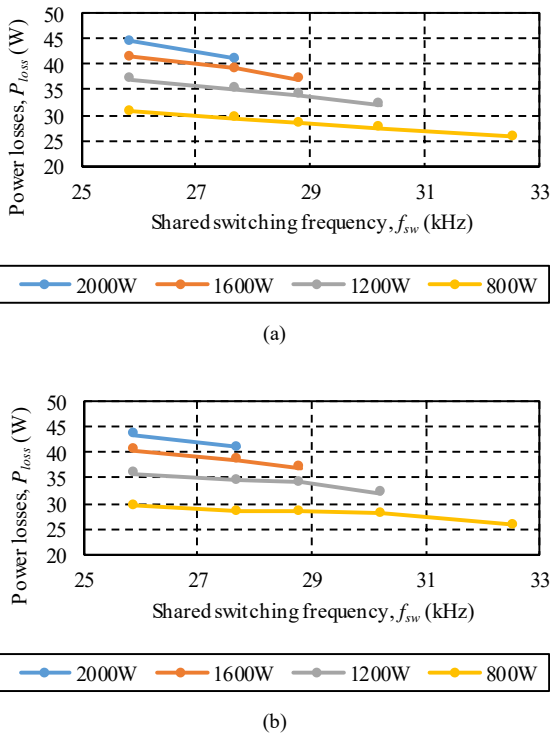


Fig. 12 Estimated power losses for different objective power and different shared switching frequencies using the NC-PDC strategy (a) and the NC-PWM strategy (b).

with 4 IH loads is shown. Independent power control when several IH loads are active can also be seen in Fig. 10, where square waveform is applied to an output while the different asymmetrical modulation strategies are applied to a second one. For the case of Fig. 10 (c) both non-complementary asymmetrical modulation strategies are simultaneously applied with the same inverter.

As depicted in Fig. 10, for the case of the NC-PDC strategy, once a_i is big enough to control power, it implies hard-switching in the low side transistor turn-on and off sequences and high side transistor turn-off but ensures a ZVS turn-on commutation in the high side transistor.

Besides, the behavior of the NC-PWM strategy presents hard-switching turn-on in the high side transistor. Additionally, due to the behavior being similar to the duty cycle modulation, RMS currents increase in the high-side diodes.

Those characteristics lead to power losses in the different devices that are interesting to analyze due to the asymmetrical nature of the modulations. The power-loss distribution among the different devices can be seen in Fig. 11, where it can be observed that they are more evenly shared for the NC-PWM strategy, meaning a decrease in the high-side transistor power losses, which is important as it is a critical device when several loads are active.

Additionally, common switching frequency selection also presents implications from the efficiency point of view. In Fig.

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12, the estimated losses for different power levels as a function of the switching frequency are represented. For both strategies and each power level, the lowest power losses are obtained at the highest possible frequency. At this frequency, the desired power is delivered using square waveform and therefore ZVS conditions for both transistors can be ensured. The power losses decrease with the frequency due to the necessary variation in the control parameters in order to maintain the output power. For the case of the NC-PDC strategy, the increment of α_i leads to a loss of ZVS and an increase of low side transistor turn-on losses while, for the NC-PWM strategy, the reduction of ϕ_i increases the low side transistor turn-off losses. As a consequence, switching frequency should be chosen the highest for a given load and desired output power.

Following the previous analysis, the efficiency of the inverter has been measured for different configurations, using 1 to 3 IH loads, and for both modulation strategies (Fig. 13). These plots show high efficiency for both strategies.

Both of them present a continuous high-efficient fast-response alternative to PDM control. However, NC-PWM control presents improved power losses sharing and higher resolution in power control.

V. CONCLUSIONS

In this paper, two non-complementary asymmetrical modulation strategies have been described, analyzed, and applied to an inverter with a shared high-side transistor in order to deliver different power to different IH loads while maintaining a common switching frequency: the non-complementary pulse delay control and the non-complementary pulse width modulation.

A power losses analysis has been carried out, allowing to perform a shared switching frequency selection for a higher efficiency, being the preferable one the highest possible that allows to provide the required power to the loads. Additionally, comparison between both strategies show that, even though they present similar efficiencies, NC-PWM shows improved losses sharing among the power devices due to the lower switching currents in the high-side transistor.

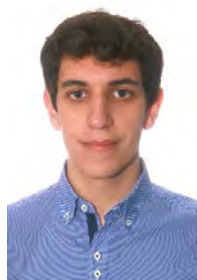
The proposed modulation strategies have been experimentally tested in a prototype with 12 outputs with 2000 W of maximum rated power that has been designed and implemented. Both non-complementary asymmetrical strategies have been proved feasible, providing a fast-response full-range independent power control to overcome the limitations of pulse density modulations.

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Pablo Guillen (S'19) received the M.Sc. degree in industrial engineering from the University of Zaragoza, Zaragoza, Spain, in 2017. During 2017, he held a research internship with the Bosch and Siemens Home Appliances Group. He is currently a Ph.D. Student with the Department of Electronic Engineering and Communications, the University of Zaragoza. His main research interests include resonant power converters and digital control applied to induction heating. Mr.

Guillen is a member of the Aragon Institute for Engineering Research (I3A).



Héctor Sarnago (S'09 M'15 SM'19) received the M.Sc. degree in Electrical Engineering and the Ph.D. degree in Power Electronics from the University of Zaragoza, Spain, in 2010 and 2013, respectively. Currently, he is a senior post-doc researcher in the the Department of Electronic Engineering and Communications at the University of Zaragoza, Spain. His main research interests include resonant converters and digital control for induction heating applications.

Dr. Sarnago is a member of the Aragon Institute for Engineering Research (I3A).



Oscar Lucía (S'04, M'11, SM'14) received the M.Sc. and Ph.D. degrees (with honors) in Electrical Engineering from the University of Zaragoza, Spain, in 2006 and 2010, respectively.

During 2006 and 2007 he held a research internship at the Bosch and Siemens Home Appliances Group. Since 2008, he has been with the Department of Electronic Engineering and Communications at the University of Zaragoza, Spain, where he is currently an Associate Professor. During part of 2009 and 2012, he was a visiting scholar at the Center of Power Electronics Systems (CPES), Virginia Tech. His main research interests include resonant power conversion, wide-bandgap devices, and digital control, mainly applied to contactless energy transfer, induction heating, electric vehicles, and biomedical applications. In these topics, he has published more than 70 international journal papers and 150 conference papers, and he has filed more than 40 international patents.

Dr. Lucía is a Senior Member of the IEEE and an active member of the Power Electronics (PELS) and Industrial Electronics (IES) societies. He was a Guest Associate Editor of the IEEE Transactions on Industrial Electronics and the IEEE Journal of Emerging and Selected Topics in Power Electronics in 2013 and 2015, respectively. Currently, he is an Associate Editor of the IEEE Transactions on Industrial Electronics, IEEE Open Journal of Industrial Electronics, and IEEE Transactions on Power Electronics. Dr. Lucía is a member of the Aragon Institute for Engineering Research (I3A).



José M. Burdío (M'97-SM'12) received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Zaragoza, Zaragoza, Spain, in 1991 and 1995, respectively.

He has been with the Department of Electronic Engineering and Communications, University of Zaragoza, where he is currently a Professor, the Head of the Group of Power Electronics and Microelectronics, and the Director of the BSH Power Electronics Laboratory at the University of Zaragoza. During 2000 he was a visiting professor at the Center for Power Electronics Systems, Virginia Tech. He is the author of more than 80 international journal papers and over 200 papers in conference proceedings and the holder of more than 60 international patents. His main research interests include modeling of switching converters and resonant power conversion for induction heating and biomedical applications. Dr. Burdío is a senior member of the IEEE and the Power Electronics and Industrial Electronics Societies. He is also a member of the Aragon Institute for Engineering Research.